UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PICTOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 6,838,651

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,838,651

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner" or "Samsung") requests *inter partes* review of claims 1-5 and 18-22 ("the challenged claims") of U.S. Patent No. 6,838,651 ("the '651 patent") (Ex. 1001), which, according to PTO records, is assigned to Pictos Technologies Inc. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: The '651 patent is at issue in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission ("the ITC Investigation").

The '651 patent was previously at issue in:

- *Imperium (IP) Holdings, Inc.*[1] *v. Apple Inc., et al.*, No. 4:11-cv-00163 (E.D. Tex.) (terminated) ("*Imperium II*");

[1] Patent Owner was formerly known as Imperium IP Holdings (Cayman) Ltd. (Ex. 1032, 1.)

- *Imperium (IP) Holdings, Inc. v. Apple Inc., et al.*, No. 6:11-cv-00128 (E.D. Tex.) (terminated) ("*Imperium I*").

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Phillip Citroën (Reg. No. 66,541). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-Pictos-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '651 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-5 and 18-22 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1 and 18 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Japanese Patent Publication 2000-12819 to Isogai *et al.* ("*Isogai*") (Ex.1005)[2];

Ground 2: Claim 2-5 and 19-22 are unpatentable under § 103(a) as being obvious over *Isogai* and U.S. Patent No. 7,133,073 to Neter ("*Neter*") (Ex.1007);

Ground 3: Claim 2-5 and 19-22 are unpatentable under § 103(a) as being obvious over *Isogai* and U.S. Patent No. 6,704,049 to Fossum *et al.* ("*Fossum*") (Ex.1008);

Ground 4: Claims 1-3 and 18-20 are unpatentable under § 102(b) as being anticipated by U.S. Patent No. 5,982,984 to Inuiya *et al.* ("*Inuiya*") (Ex.1006);

Ground 5: Claim 4-5 and 21-22 are unpatentable under § 103(a) as being obvious over *Inuiya* and *Neter*; and

Ground 6: Claim 4-5 and 21-22 are unpatentable under § 103(a) as being obvious over *Inuiya* and *Fossum*.

[2] Ex. 1005 is a compilation containing the English-language translation of *Isogai* (Ex.1005, 1-17), followed by the Japanese language version (*id.*, 18-34) and an affidavit required by 37 C.F.R. § 42.63(b) (in the form of a declaration as permitted by 37 C.F.R. § 42.2) (*id.*, 35).

The '651 patent issued January 4, 2005, from U.S. App. No. 10/113,545, filed March 28, 2002. *Isogai* was published on January 14, 2000. *Inuiya* issued November 9, 1999, from U.S. App. No. 08/594,598, filed January 31, 1996. Thus, *Isogai* and *Inuiya* qualify as prior art to the '651 patent at least under pre-AIA 35 U.S.C. § 102(b). *Fossum* issued March 9, 2004, from U.S. App. No. 09/028,961, filed February 23, 1998. *Neter* issued November 7, 2006, from U.S. App. No. 09/496,607, filed February 2, 2000. Thus, *Fossum* and *Neter* qualify as prior art to the '651 patent at least under pre-AIA 35 U.S.C. § 102(e). None of these references were considered during prosecution. (*See generally* Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '651 patent ("POSITA") would have had a bachelor's degree in electrical engineering, computer science, or the equivalent, and two or more years of experience with image processing. (Ex. 1002, ¶¶20-21.)[3] More education can supplement practical experience and vice versa. (*Id.*)

[3] Petitioner submits the declaration of Dr. R. Jacob Baker, PH.D., P.E. (Ex. 1002), an expert in the field of the '651 patent. (Ex. 1002, ¶¶5-15; Ex. 1003.)

VII. THE '651 PATENT

The '651 patent "relates generally to solid-state imaging devices" "implementing multiple analog-to-digital ('A/D') converters to obtain high frame rates." (Ex. 1001, 1:6-11; Ex. 1002, ¶¶27-29.) The '651 patent states that the imaging device has "four color channels (one red, one blue and two greens) used to define a color image based upon the Bayer Pattern of color filters." (Ex. 1001, 3:1-4.) The '651 patent discloses that "two A/D converters may be employed, where one A/D converter is used for the red and blue channels and the second A/D converter is used for the green channels." (*Id*., 3:8-10.)

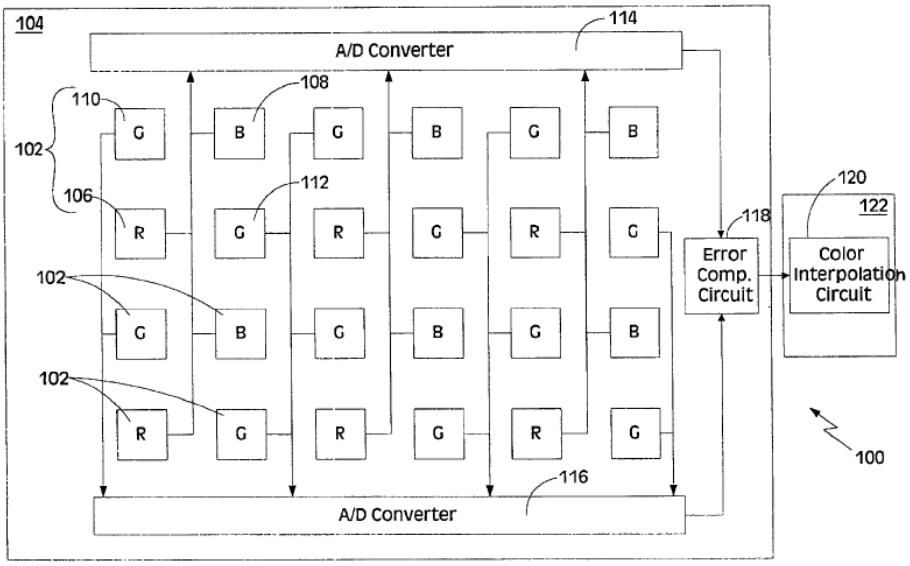


FIG. 1

(Ex. 1001, FIG. 1.)

An error compensation circuit 118 "provides an independent gain to correct the gain for each color channel" and "provides an independent offset to correct the fixed pattern noise offset for each color channel." (*Id*., 5:3-7.) "The color interpolation circuit 120 performs the interpolation for each pixel 102 to determine the color of the pixel," where "[t]he color interpolation circuit 120 may be located on a second chip 122, as shown in FIG 1" or "may be located on chip 104." (*Id*., 5: 23-27.)

VIII. CLAIM CONSTRUCTION

During IPR, claims are construed according to the "*Phillips* standard," as set forth in *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). *See* 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002, ¶30.)

IX. DETAILED EXPLANATION OF GROUNDS[4]

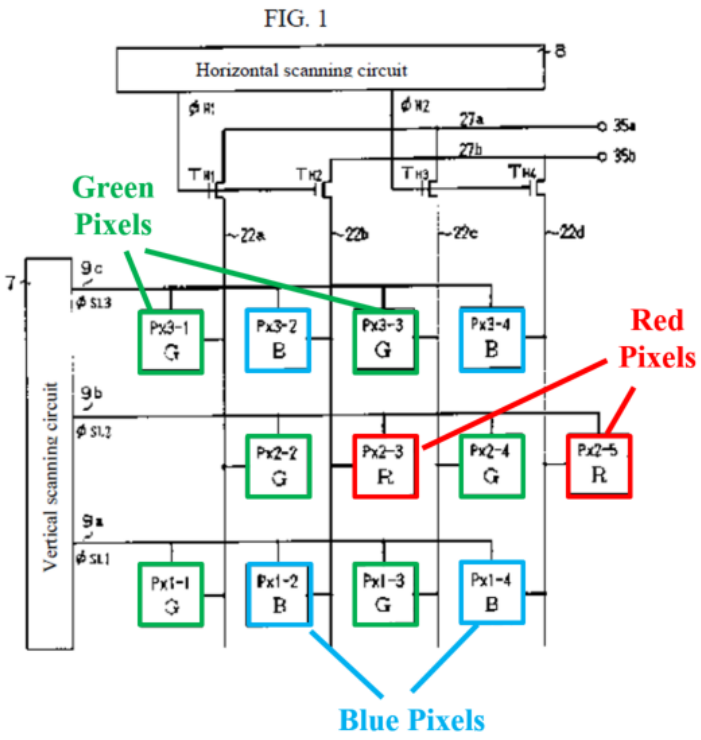
A. Ground 1: Claims 1 and 18 Are Anticipated by *Isogai*

1. Claim 1

a) A solid state imaging device, comprising:

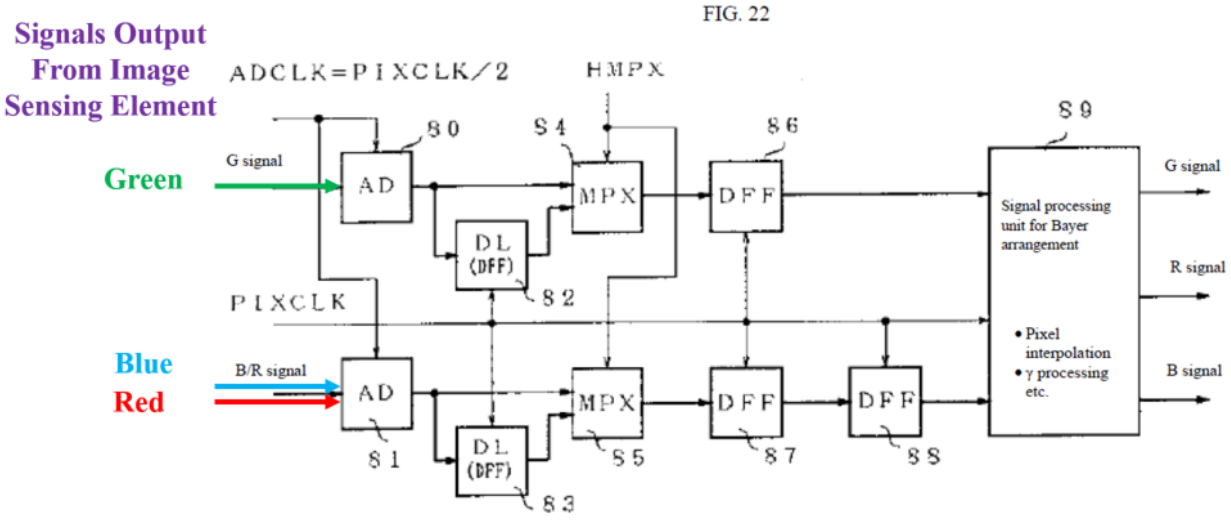
To the extent the preamble of claim 1 is limiting, *Isogai* discloses the limitations therein. (Ex. 1002, ¶¶42-46.) For instance, *Isogai* discloses a "solid-state image sensing element having a parallel output configuration," where "a signal of a specified pixel arranged in a checkered pattern is output to one of two horizontal signal lines." (Ex. 1005, Abstract; *see also id*., ¶¶[0001]; Ex. 1002, ¶42.) Annotated figure 1 of *Isogai* below shows a solid state image sensing element. (Ex. 1005, ¶[0026], FIG. 1.)

[4] Section IX below references exhibits other than the identified prior art for each ground. Such exhibits reflect the state of the art known to a POSITA at the time of the alleged invention consistent with the testimony of Dr. R. Jacob Baker, PH.D., P.E.



(*Id*., FIG. 1 (annotated); Ex. 1002, ¶43.)

Isogai also discloses a system for processing the signal outputs from the solid-state imaging sensing elements. (Ex. 1005, ¶¶[0077]-[0078], FIG. 22.) The processing system, shown in annotated figure 22 below, receives inputs from the disclosed solid-state image sensing elements and performs color imaging. (*Id*., ¶[0078], FIG. 22; Ex. 1002, ¶45.)



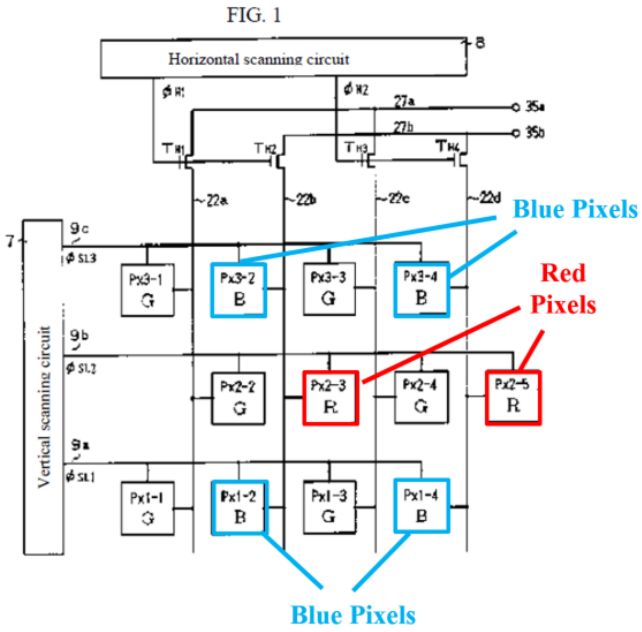
(Ex. 1005, FIG. 22 (annotated); Ex. 1002, ¶45.)

The combination of the solid-stage image sensing element shown in figure 1 with the processing system shown in figure 22 constitutes a "solid state imaging device" as recited in claim 1. (Ex. 1002, ¶46.)

b) a red pixel having an output;

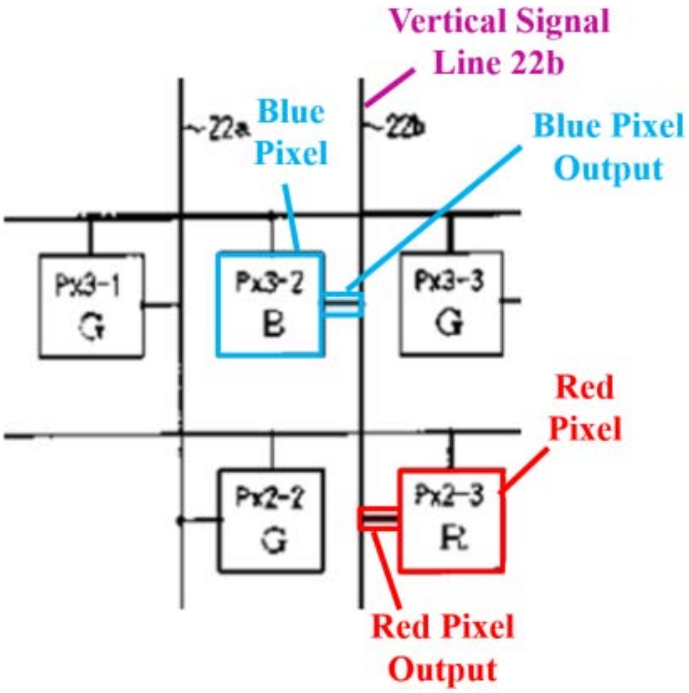
c) a blue pixel having an output;

Isogai discloses these limitations. (Ex. 1002, ¶¶47-50.) *Isogai's* "solid state imaging device" includes red and blue pixels. For example, two such red pixels and four such blue pixels are shown in annotated figure 1 below. (Ex. 1005, ¶¶[0024], ¶[0028], FIGs. 1, 3; Ex. 1002, ¶¶47, 49.)



(Ex. 1005, FIGs. 1, 3 (annotated); Ex. 1002, ¶49.)

Each of the red and blue pixels highlighted above has an output. (Ex. 1002, ¶48, 50.) *Isogai* discloses that vertical signal lines 22a-22b are used to connect alternating columns of pixels to either the first horizontal signal line 27a or the second horizontal signal line 27b. (Ex. 1005, ¶¶[0025], [0027], FIG. 1.) The outputs from the pixels are routed from the vertical signal lines to the horizontal signal lines and then output by the output terminals 35a and 35b. (*Id*., ¶¶[0025], [0027]-[0029], FIG. 1.) As shown in the annotated and enlarged excerpt of figure 1 below, each of the red pixel Px2-3 and the blue pixel pixel Px3-2 has an output ("a red pixel having an output" and "a blue pixel having an output") that connects to the vertical signal line 22b. (*Id*., ¶¶[0025], [0027]-[0029], FIG. 1; Ex. 1002, ¶¶48, 50.)

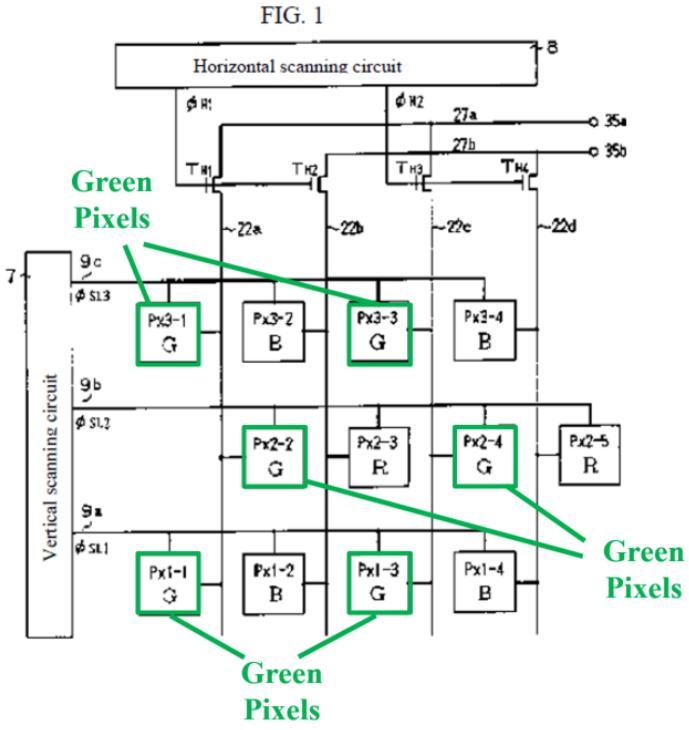


(Ex. 1005, FIG. 1 (excerpt, annotated); Ex. 1002, ¶50.)

d) a first green pixel having an output;

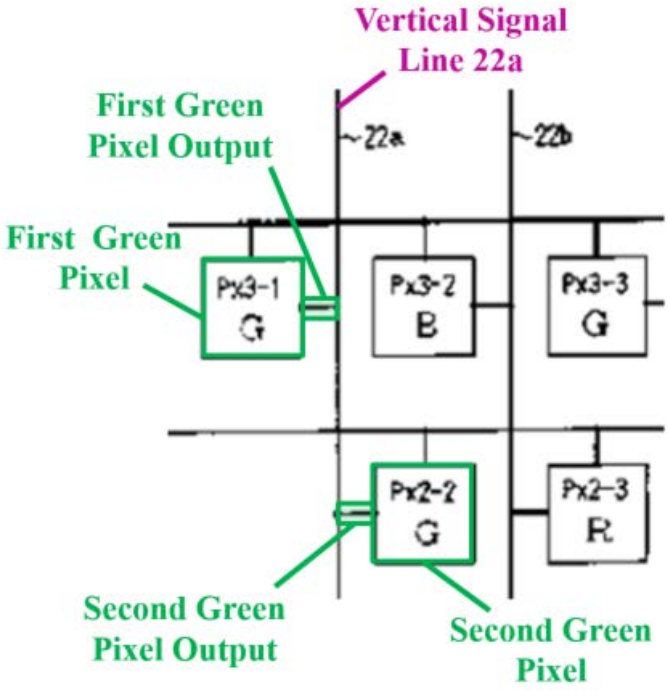
e) a second green pixel having an output;

Isogai discloses these limitations. (Ex. 1002, ¶¶51-54.) The solid-stage image sensing element that is included in *Isogai's* "solid state imaging device" includes a plurality of green pixels. For example, six such green pixels are shown in annotated figure 1 below. (Ex. 1005, ¶¶[0024], ¶[0028], FIGs. 1; Ex. 1002, ¶51.)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶51.)

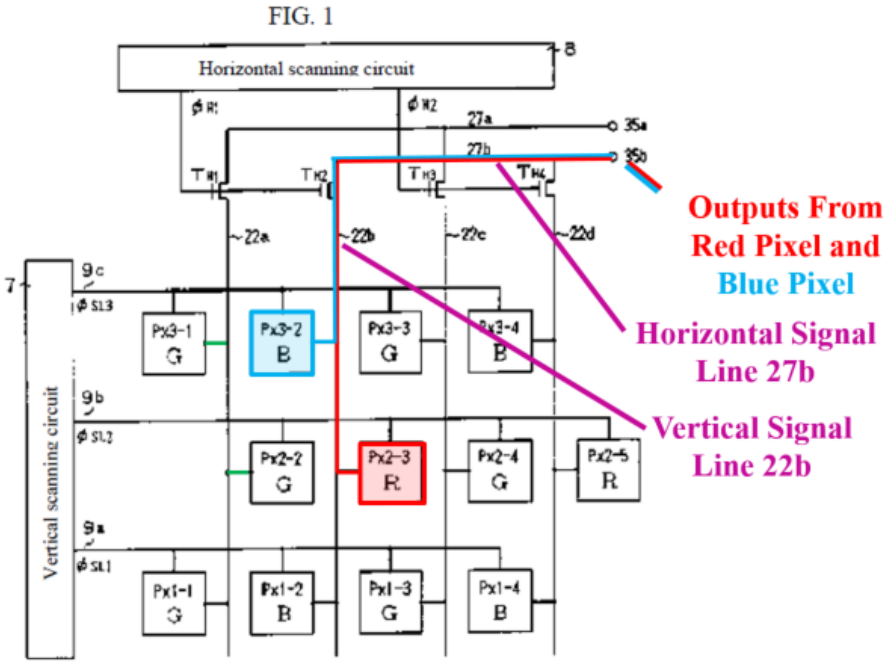
Like the red and blue pixels discussed above in Sections IX.A.1(b)-(c), each of the green pixels highlighted above has an output. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1; *supra* Sections IX.A.1(b)-(c).) For example, as shown in the annotated and enlarged excerpt of figure 1 below, each of green pixels Px3-1 and Px2-2 has an output ("a first green pixel having an output" and "a second green pixel having an output") that connects to the vertical signal line 22a. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1; Ex. 1002, ¶¶52, 54.)



(Ex. 1005, FIG. 1 (excerpt, annotated); Ex. 1002, ¶54.)

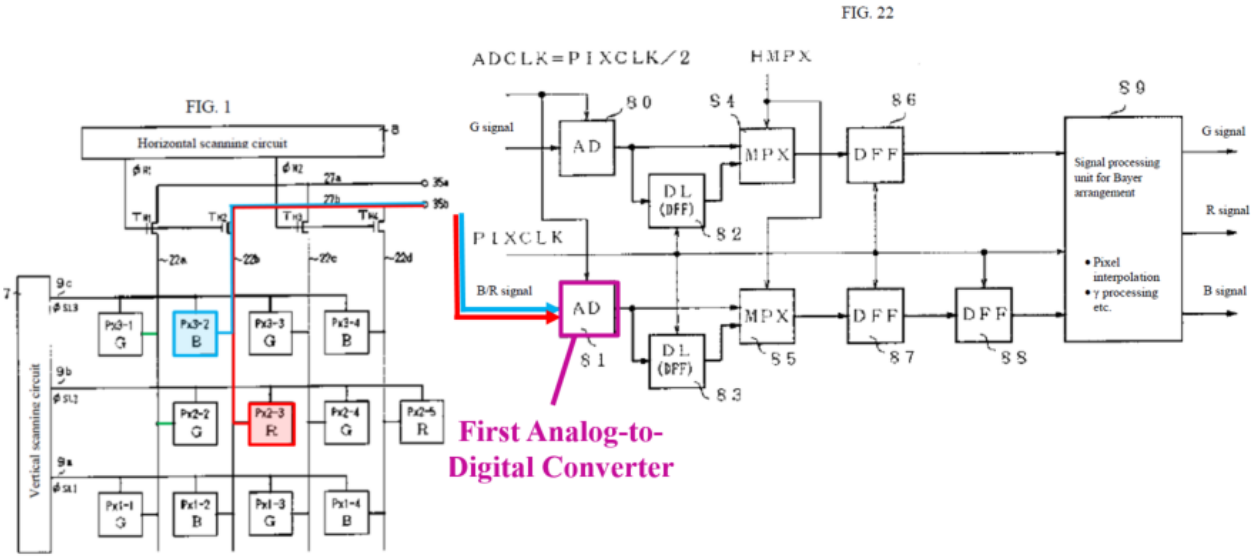
f) a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixel into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixel into a second digital signal;

Isogai discloses these limitations. (Ex. 1002, ¶¶55-64.) As discussed above in Sections IX.A.1(b)-(e), the outputs of the red pixel and blue pixel are connected to the vertical signal line 22b, whereas as the outputs of the green pixels are connected to the vertical signal line 22a. (Ex. 1005, ¶¶[0027], FIGs. 1, 3; *supra* sections IX.A.1(b)-(e).) As shown in annotated figure 1 below, the vertical signal lines 22a and 22b are connected to horizontal signal lines 27a and 27b, respectively. (*Id*., ¶[0027], FIG. 1; Ex. 1002, ¶55.)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶55.)

As shown in the demonstrative below, the output signals corresponding to the horizontal signal lines 27a and 27b are provided as inputs to the processing system that is included in *Isogai's* "solid state imaging device" and shown in figure 22. (Ex. 1002, ¶58.)



(*Id*., FIGs. 1, 22 (annotated); Ex. 1002, ¶58.)

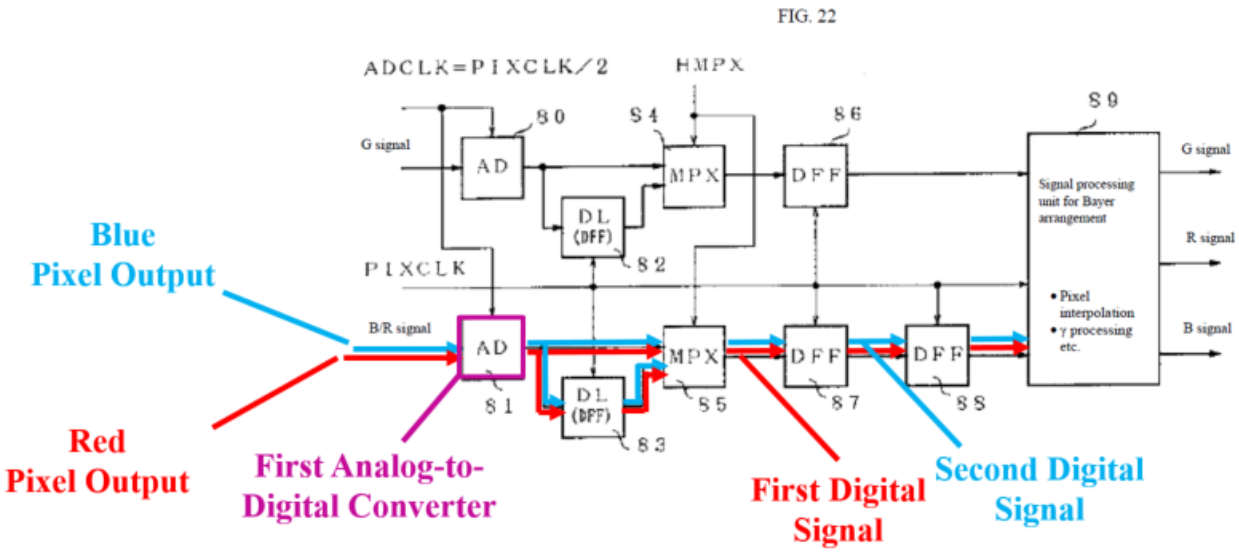
As shown above, the outputs of the red and blue pixels on the horizontal signal line 27b are provided as the "B/R signal" to the analog-to-digital converter (AD) 81. (Ex. 1005, ¶¶[0079], [0080]; Ex. 1002, ¶59.) A POSITA would have understood that AD blocks 80 and 81, which are further identified in the "Explanation of Reference Numerals" of *Isogai* as "80, 81 AD converter," are analog-to-digital (A/D) converters that are connected to the outputs of the pixels and convert those outputs into digital signals. (Ex. 1005, ¶[0079] ("The G signal . . . is AD-converted into the output signal" where the "A/D conversion frequency is 1/2 of PIXCLK."); Ex. 1002, ¶¶60-61.)

Isogai further discloses that the digital signals generated by the analog-to-digital converter 81 include a red digital signal (R signal) ("first digital signal") and a blue digital signal (B signal) ("second digital signal") that are "sequentially output"

by AD 81. (*Id*., ¶[0079] ("This apparatus output the G signal as the first channel, and output the line sequential signals of R and B as the second channel."), ¶[0080] ("The second channel, in which the B signal and the R signal are output line sequentially."); Ex. 1002, ¶62.) A POSITA would have understood that when the row select signal 55c corresponding to the top row of pixels is asserted, the blue pixel output is provided to the vertical signal line 22b and horizontal signal line 27b and converted to the first digital signal by AD 81. (Ex. 1002, ¶62.) Similarly, when the row select signal 55b corresponding to the second row of pixels is asserted, the red pixel output is provided to the vertical signal line 22b and horizontal signal line 27b and converted to the second digital signal by AD 81. (*Id*.) Thus, AD 81 will sequentially convert different red and blue pixel outputs into digital signals that are "sequentially output." (*Id*.; Ex. 1005, ¶¶[0079], [0080].)

Annotated figure 22 below shows that the signal path for the first (red) and second (blue) digital signals includes D-flip flops 83, 87, and 88, and multiplexer 85, where such elements control the timing of the presentation of the first and second digital signals to the signal processing unit 89. (Ex. 1005, ¶¶[0079], [0080], FIG. 22; Ex. 1002, ¶63.) The PIXCLK scanning clock controls the presentation of the red/blue digital pixel information to the processing block 89 by the D-flip flop (DFF) 88, whereas the HMPX signal selects which of the red/blue pixel digital signals that

are sequentially output by AD 81 is forwarded to the DFF 87 using the multiplexer (MPX) 85. (Ex. 1005, ¶¶[0079], [0080], FIG. 22; Ex. 1002, ¶63.)

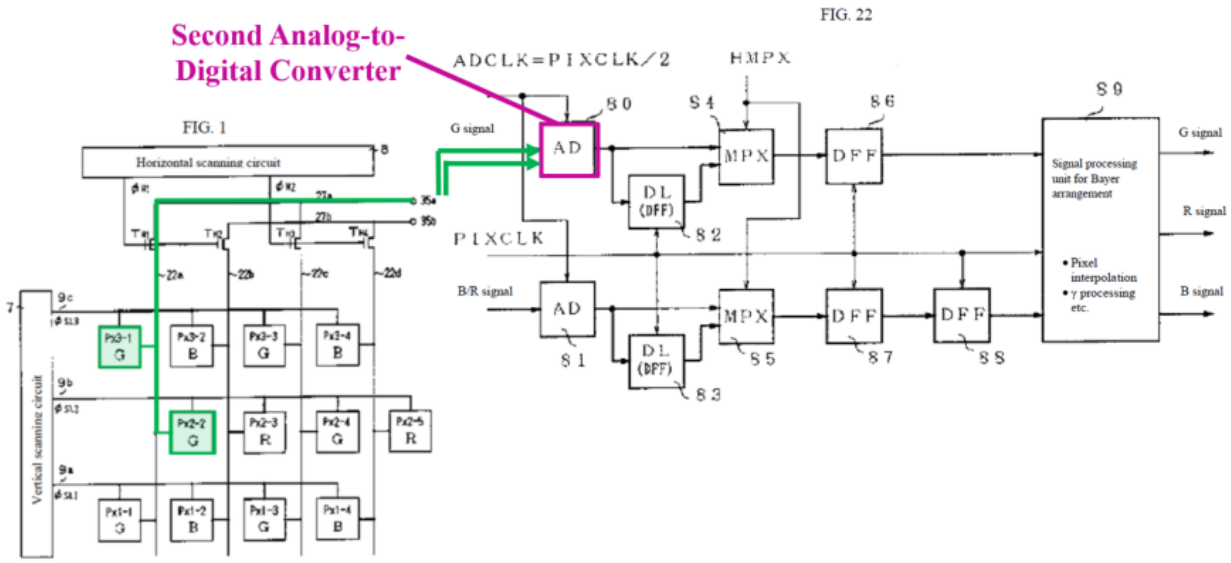


(*Id.*, FIG. 22 (annotated); Ex. 1002, ¶63.)

Analog-to-digital converter 81 constitutes "a first analog-to-digital converter" as recited in claim 1. (Ex. 1002, ¶64.)

g) a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixel into a third digital signal and connected to the output of the second green pixel for converting the output of the second green pixel into a fourth digital signal; and;

Isogai discloses these limitations. (Ex. 1002, ¶¶65-69.) Just as the analog-to-digital converter 81 converts the red and blue pixel outputs into digital signals, the analog-to-digital converter 80 is connected to and converts the outputs of the first and second green pixels on horizontal signal line 27a into digital signals. (*Supra* Section IX.A.1(f); *see also* Ex. 1005, ¶[0079], FIGs. 1, 22; Ex. 1002, ¶¶65-66.)

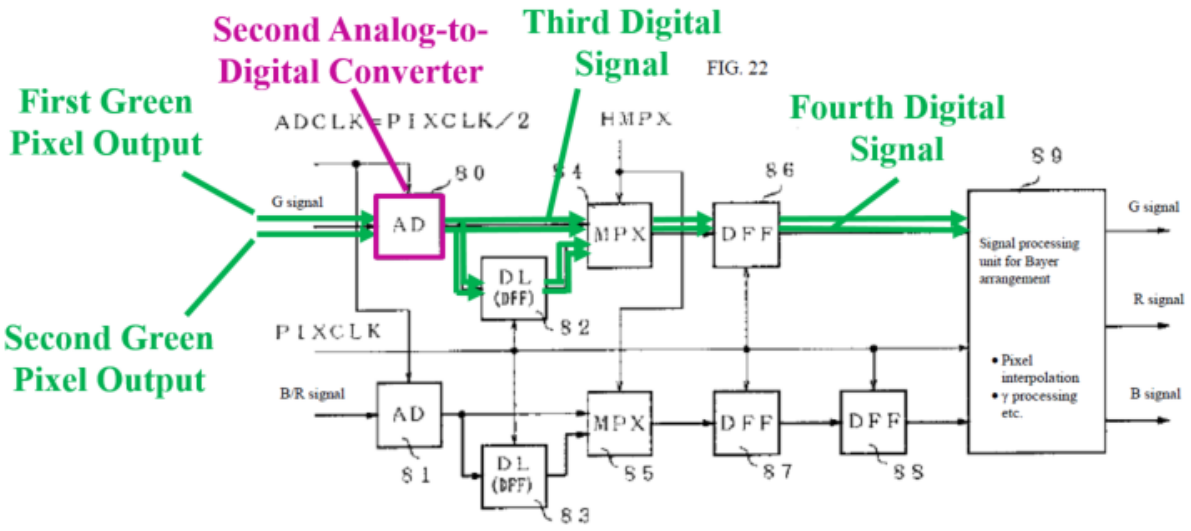


(Ex. 1005, FIGs. 1, 22 (annotated); Ex. 1002, ¶65.)

Isogai further discloses that the digital signals generated by the analog-to-digital converter 80 include first and second green digital signals (G signal) ("third digital signal" and "fourth digital signal"). (*Id*., ¶[0079] ("The G signal . . . is AD-converted into the output signal" where the "A/D conversion frequency is 1/2 of PIXCLK."); Ex. 1002, ¶67.) A POSITA would have understood that when the row select signal 55c corresponding to the top row of pixels is asserted, the first green pixel output is provided to the vertical signal line 22a and horitzontal signal line 27a and converted to the third digital signal by AD 80. (Ex. 1002, ¶67.) Similarly, when the row select signal 55b corresponding to the second row of pixels is asserted, the second green pixel output is provided to the vertical signal line 22a and horizontal signal line 27a and converted to the fourth digital signal by AD 80. (*Id*.) Thus, AD

80 will sequentially convert different green pixel outputs into two digital signals. (*Id.*; Ex.1005, ¶[0079].)

Annotated figure 22 below shows that the signal path for the third (first green) and fourth (second green) digital signals includes D-flip flops 82 and 86 as well as multiplexer 84, where such elements control the timing of the presentation of the third and fourth digital signals to the signal processing unit 89. (Ex. 1005, ¶[0079], FIG. 22; Ex. 1002, ¶68.) The PIXCLK scanning clock controls the presentation of the green digital pixel information to the processing block 89 by the D-flip flop (DFF) 86, whereas the HMPX signal selects which of the first/second green pixel digital signals that are sequentially output by AD 81 is forwarded to the DFF 86 using the multiplexer (MPX) 84.

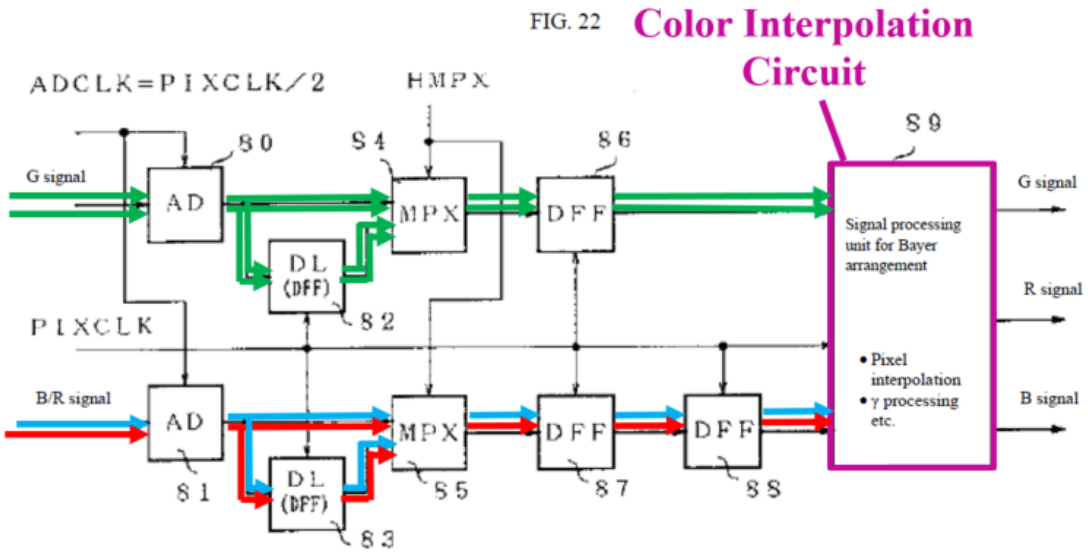


(*Id.*, FIG. 22 (annotated); Ex. 1002, ¶68.)

Analog-to-digital converter 80 constitutes "a second analog-to-digital converter" as recited in claim 1. (Ex. 1002, ¶69.)

h) a color interpolation circuit for combining the first, second, third and fourth digital signals.

Isogai discloses this limitation. (Ex. 1002, ¶¶70-74.) For instance, *Isogai* discloses a signal processing unit 89 that combines the first, second, third, and fourth digital signals ("a color interpolation circuit for combining the first, second, third and fourth digital signals"). As discussed above in Sections IX.A.1(f)-(g), the analog-to-digital converters 80, 81 convert the outputs of red, blue, first green, and second green pixels into the first, second, third, and fourth digital signals, respectively. (*Supra* Sections IX.A.1(f)-(g).) *Isogai* further discloses that the first, second, third, and fourth digital signals are provided to the signal processing unit 89. (Ex. 1005, ¶¶[0077]-[0080], FIG. 22; Ex. 1002, ¶70.)



(Ex. 1005, FIG. 22 (annotated); Ex. 1002, ¶70.)

Isogai discloses that the signal processing unit 89 performs signal processing on the digitized pixel outputs, including "**pixel interpolation** of empty grid points of each RGB color . . . to output RGB color signals with all pixels having RGB color signal." (Ex. 1005, ¶[0080] (emphasis added); Ex. 1002, ¶71.) Such pixel interpolation of empty grid points (unknown color data for a pixel) includes processing that combines the digital signals corresponding to the outputs of the pixels in a manner consistent with the disclosure of the '651 patent. (Ex. 1005, ¶[0078]; Ex. 1001, 5:13-16 ("Color interpolation is used to determine the amount of red, green and blue light incident on each pixel. This process averages the color outputs of appropriate neighboring pixels to approximate each pixel's unknown color data."); Ex. 1002, ¶72.) For example, a POSITA would have understood that *Isogai's* disclosure of "pixel interpolation" would include combining color data corresponding to neighboring pixels in order to determine the pixel color data for the empty grid points as described by the '651 patent. (Ex. 1005, ¶[0080]; Ex. 1001, 5:13-25; Ex. ; Ex. 1002, ¶73.)

2. Claim 18

a) An imaging method comprising:

To the extent the preamble of claim 18 is limiting, *Isogai* discloses the limitations therein. (Ex. 1002, ¶75.) As discussed above in Section IX.A.1(a),

Isogai discloses a solid-state image sensing element and a system for processing the signal outputs from the solid-state imaging sensing element that together form an imaging device, where the operation of such an imaging device, which includes the capture and processing of pixel data, constitutes an "imaging method." (*Id*.; *Supra* Section IX.A.1(a).)

b) converting an output of a red pixel into a first digital signal using a first analog-to-digital converter;

c) converting an output of a blue pixel into a second digital signal using the first analog-to-digital converter;

Isogai discloses these limitations. (Ex. 1002, ¶76.) As discussed above in Sections IX.A.1(b)-(c), *Isogai* discloses a red pixel and a blue pixel, each of which has a corresponding "output." (*Supra* Sections IX.A.1(b)-(c).) As discussed above in Section IX.A.1(f), the outputs of the red and blue pixels are converted to first and second digital signals, respectively, by a first analog-to-digital converter. (*Supra* Section IX.A.1(f).)

d) converting an output of a first green pixel into a third digital signal using a second analog-to-digital converter;

e) converting an output of a second green pixel into a fourth digital signal using the second analog-to-digital converter; and

Isogai discloses these limitations. (Ex. 1002, ¶77.) As discussed above in Sections IX.A.1(d)-(e), *Isogai* discloses a first and second green pixel, each of which

has a corresponding "output." (*Supra* Sections IX.A.1(b)-(c).) As discussed above in Section IX.A.1(g), the outputs of the first and second green pixels are converted to third and fourth digital signals, respectively, by a second analog-to-digital converter. (*Supra* Section IX.A.1(g).)

f) combining the first, second, third and fourth digital signals using a color interpolation circuit.

Isogai discloses this limitation for the reasons discussed above in Section IX.A.1(h). (*Supra* Section IX.A.1(h); (Ex. 1002, ¶78).)

B. Ground 2: Claims 2-5 and 19-22 Are Obvious Over *Isogai* in View of *Neter*

1. Claim 2

a) The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

Isogai in view of *Neter* discloses or suggests these features. (Ex. 1002, ¶¶79-94.) *Isogai's* imaging device discussed above with respect to claim 1 does not explicitly disclose an error compensation circuit for correcting a gain of the outputs of the red, blue, and green pixels. However, as demonstrated below, *Neter* discloses such gain correction, and a POSITA would have found it obvious in view of *Neter* to utilize gain correction in *Isogai's* imaging device. (Ex. 1002, ¶¶80-81.)

Neter, like *Isogai*, describes circuits for processing imaging pixel sensor elements. (Ex. 1007, 2:60-62, 3:4-16.) Both *Neter* and *Isogai* describe image sensing devices that include red, blue, and green pixels arranged in the Bayer pattern scheme. (*Id*., 3:12-14, FIG. 3; Ex. 1004, ¶[0028], FIG. 1.) Therefore, a POSITA implementing an image sensing device like that described in *Isogai* would have had reason to look to *Neter*. (Ex. 1002, ¶82.)

Neter discloses performing color compensation, which involves adjusting the output signals for different colored pixels as the pixel elements may be more responsive to one color of light in comparison to another color of light. (Ex. 1007, 1:50-57 ("Conventional imaging devices also require color compensation for difference in the response of the various color filters and for variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing. For example, when the primary color scheme is used, **the response of an element that absorbs red light may be different than an element that absorbs blue light even when illuminated by light of equal red and blue luminosity levels."** (emphasis added); *see also id*., 1:57-2:6; Ex. 1002, ¶84.) *Neter* further discloses performing such color compensation with separate amplification of different colored pixel outputs using programmable gain amplifiers. (Ex. 1007, 4:19-36.) For example, figure 13 of *Neter* discloses a color imaging system 330 that

includes color compensation using such programmable gain amplifiers. (*Id*., 13:39-41, FIG. 13; Ex. 1002, ¶¶85-86.)

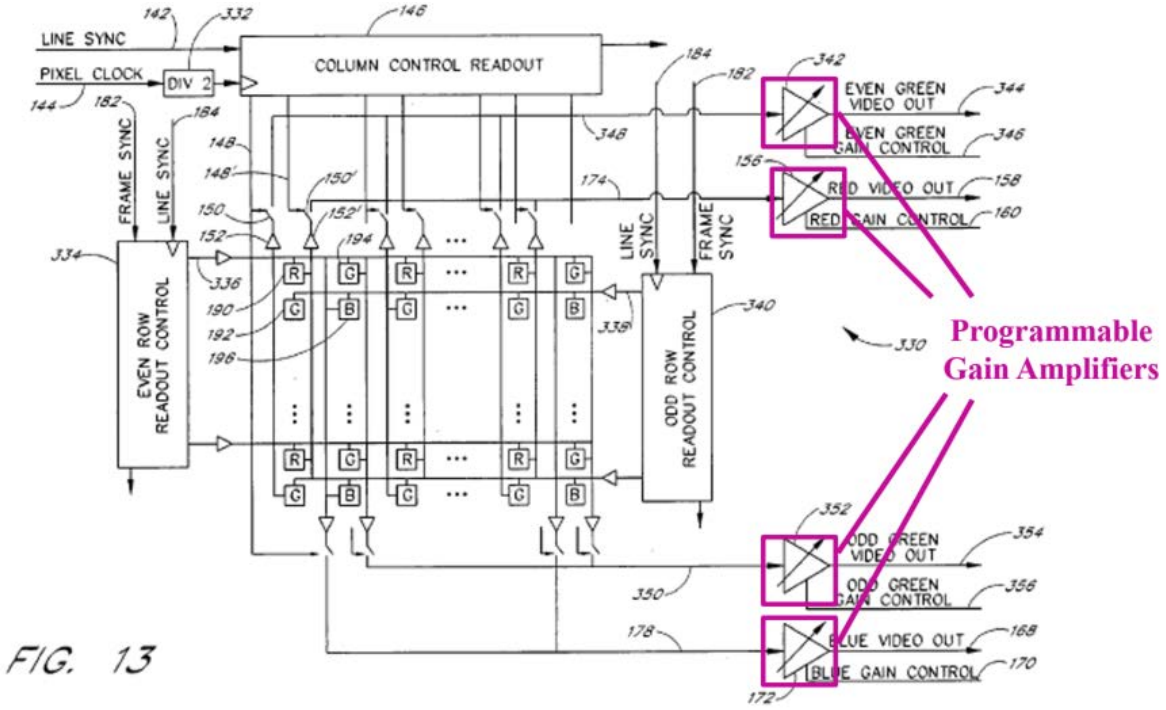


FIG. 13

(*Id*., FIG. 13 (annotated); Ex. 1002, ¶86.)

Neter further discloses that different transfer functions can be implemented by the programmable gain amplifiers such that "each color can be optimized independently for maximum dynamic range." (*Id*., 4:51-55; *see also id*., 13:55-14:4, FIG. 14; Ex. 1002, ¶87.)

Given the disclosure of color compensation in *Neter*, a POSITA would have found it obvious to combine the teachings of *Isogai* and *Neter* such that at least one of the output signals for the red, blue, first green, and second green pixels identified above in Sections IX.A.1(b)-(e) is amplified to provide color compensation for the

image sensing device. (Ex. 1002, ¶¶88-94.) A POSITA would have been motivated to do so because, as disclosed by *Neter*, such color-specific amplification compensates for differences in the response of various color filters and variations in the sensor array resulting from variations in process, materials, temperature, and manufacturing. (Ex. 1007, 13:30-33, 13:61-14:1; Ex. 1002, ¶89.) Such color compensation, which *Neter* also refers to as "color correction," provides numerous advantages, including improved dynamic range, improved image quality and "improve[ed] white balancing, which is used to compensate colors for different illumination temperatures." (Ex. 1007, 13:28-36; 14:34-38; Ex. 1010, 2094 ("To achieve white balance, it is evident from Fig. 4 that the outputs of the blue and green pixels must be amplified with respect to the outputs of the red pixels."), 2095 ("[T]hree separate and independent gains are used for pixels covered by red, green, and blue filters, respectively. White balancing can therefore be performed in the analog domain.").)

Accordingly, a POSITA would have combined the teachings of *Isogai* and *Neter* such that the output of at least one of the red, blue, first green, and second green pixels in *Isogai* is amplified to provide color compensation in order to, for example, improve color dynamic range and white balancing. (Ex. 1002, ¶¶91-94.) In such an *Isogai-Neter* combination, a POSITA would have understood that such color compensation corresponds to "correcting a gain of one of the output of the red

pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel" as recited in claim 2 of the '651 patent. (Ex. 1002, ¶91.) Moreover, such a skilled person would have understood that the programmable gain amplifiers and related circuitry to support such color compensation, which *Neter* also refers to as "color correction," would constitute an "error correction circuit" that, as recited in claim 2, performs such gain correction. (*Id*.)

Including color compensation circuity like that disclosed in *Neter* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements (the image array with pixel outputs of *Isogai* with the amplifiers of *Neter* to compensate for gain differentials between different colored pixels) using known circuit design methods, where each element performs the same function described in *Neter* and *Isogai*, to achieve the predictable result of an imaging device that is improved to provide color compensation. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). As discussed above, both *Isogai* and *Neter* describe circuits for processing imaging pixel sensor elements, but *Neter* describes additional circuitry not found in *Isogai* for color compensation. Therefore, a POSITA would have recognized that *Neter*'s teachings relating to color compensation could have been applied to *Isogai*'s system in a similar way. *Id.* at 417. (Ex. 1002, ¶92.)

Additionally, including such color compensation circuitry in *Isogai's* imaging device would have been straightforward for a POSITA given such a person's knowledge and the disclosure in *Neter*. (Ex. 1002, ¶93.) For example, the combination would have required nothing more than adding well-known, rudimentary, and widely available amplifiers for color compensation to *Isogai*'s system, which, as evidenced by *Neter* and *Loinaz*, were commonly used for color correction at the time. (*Id*.) Such a combination would not have detracted from the overall functionality of *Isogai*'s system, which would have continued to operate as described in *Isogai* with the added circuity to correct gain differentials for the different colors as necessary. (*Id*.)

2. Claim 3

a) The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

Isogai in view of *Neter* discloses or suggests these features. (Ex. 1002, ¶¶95-107.) *Isogai's* imaging device discussed above with respect to claim 1 does not explicitly disclose an error compensation circuit for correcting a fixed pattern noise offset from one of the analog signals output by the red, blue, and green pixels. However, *Neter* discloses correcting a fixed pattern noise offset for the outputs from red, blue, and green pixels, and a POSITA would have found it obvious in view of

Neter to utilize such fixed pattern noise offset correction in the solid state imaging device of *Isogai*. (Ex. 1002, ¶¶96-97.)

As discussed above in section IX.B.1, a POSITA implementing an image sensing device as disclosed in *Isogai* would have had reason to look to *Neter*. (*Supra* Section IX.B.1.) *Neter* discloses circuitry and methods for addressing fixed pattern noise corresponding to pixel outputs in an array of colored pixels like that of *Isogai* (e.g. a Bayer pattern). (Ex. 1007, 5:1-17, 15:53-16:2.) For example, *Neter* discloses that fixed pattern noise reduction is used in imaging systems to address noise related to pixel-to-pixel variation, which can be caused by dark current in the imaging array. (*Id*.; Ex. 1002, ¶¶98-99.) Figure 20 of *Neter* discloses a color imaging system that supports fixed pattern noise reduction. (Ex. 1007, 16:3-16, FIG. 20.)

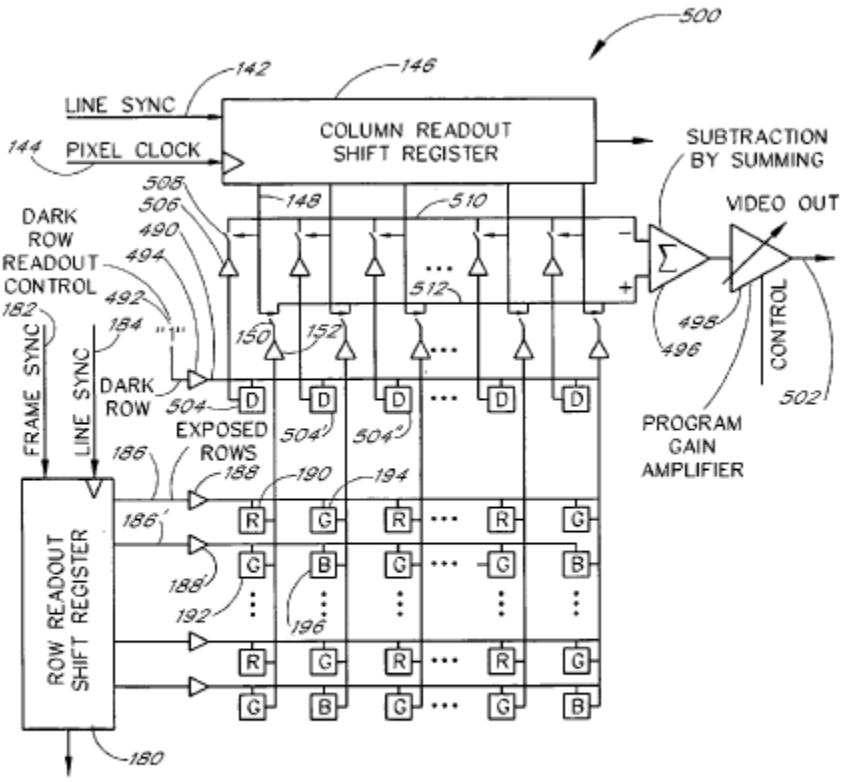


FIG. 20

(*Id*., FIG. 20.)

As shown in figure 20, a dark row of pixels is added with an opaque mask layer such that they are not exposed to light. (*Id*., 16:17-19.) In order to subtract out the dark current (correct the offset), two pixels are read out from the same column, where one pixel is from the dark row and the other is from one of the exposed rows. (*Id*., 16:30-34.) "The dark pixel value is then subtracted from the exposed pixel value by the summing amplifier 496, thereby providing fixed pattern noise reduction." (*Id*., 16:34-37; Ex. 1002, ¶100.)

Given the disclosure of a fixed pattern noise reduction in *Neter*, a POSITA would have found it obvious to combine the teachings of *Isogai* and *Neter* such that at least one of the output signals for the red, blue, first green, and second green pixels identified in sections IX.A.1.(b)-(e) has an offset corresponding to fixed pattern noise corrected. (Ex. 1002, ¶102.) A POSITA would have been motivated to do so because, as disclosed by *Neter*, fixed pattern noise reduction provides advantages, including less contamination of the image signal, thereby providing increased dynamic range and higher image quality. (*Id*.; Ex. 1007, 15:55-57, 15:64-67.)

Including fixed pattern noise reduction circuity like that disclosed in *Neter* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements (the image array with pixel outputs of *Isogai* with the dark current removal circuitry of *Neter* to compensate for fixed pattern noise) using known circuit design methods, where each element performs the same function described in *Neter* and *Isogai*, to achieve the predictable result of an imaging device that is improved have higher image quality because of reduced noise. *KSR*, 550 U.S. at 416. As discussed above, both *Isogai* and *Neter* describe circuits for processing imaging pixel sensor elements, but *Neter* describes additional circuitry not found in *Isogai* for dark current removal. Therefore, a POSITA would have recognized that *Neter*'s teachings relating to noise reduction could be applied

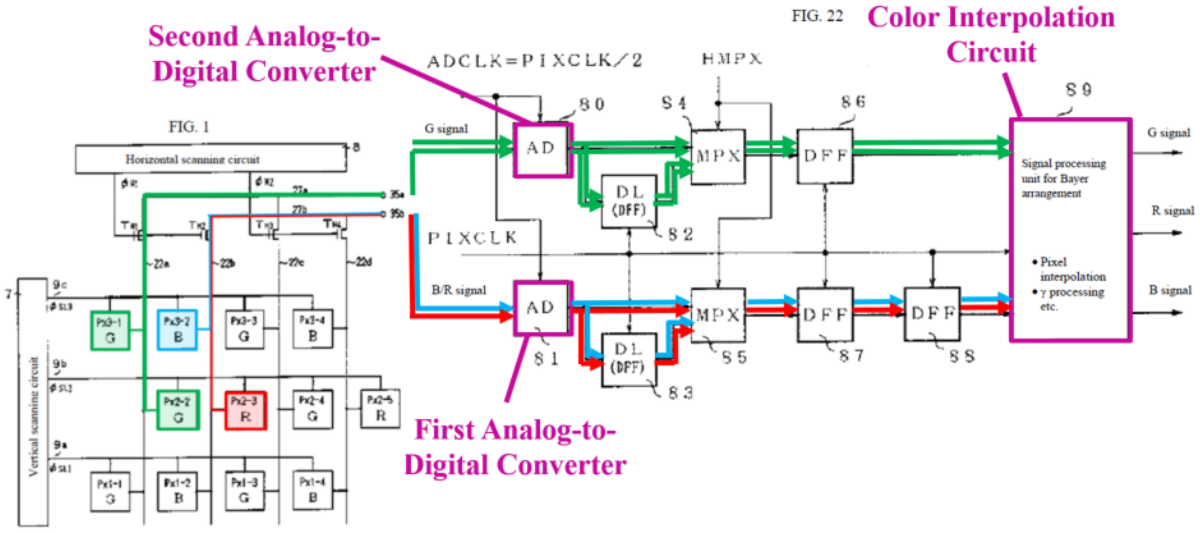
to *Isogai*'s system in a similar way to improve overall system performance, including improved image quality. *Id.* at 417. (Ex. 1002, ¶104.)

Additionally, including such fixed pattern noise correction circuitry in *Isogai's* imaging device would have been straightforward for a POSITA given such a person's knowledge and the disclosure in *Neter*. (Ex. 1002, ¶105.) For example, the combination would have required nothing more than adding well-known, straightforward circuitry to subtract dark current to *Isogai*'s system, which, as evidenced by *Neter*, was commonly used for fixed pattern noise reduction at the time. Such a combination would not have detracted from the overall functionality of *Isogai*'s system, which would have continued to operate as described in *Isogai* with the added circuity to reduce fixed pattern noise. (*Id*.) In such an *Isogai-Neter* combination, a POSITA would have understood that such fixed pattern noise correction circuitry corresponds to the "error compensation circuit" recited in claim 3. (Ex. 1002, ¶106.)

3. Claim 4

a) The solid stage imaging device of claim 1 further comprising a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

The *Isogai-Neter* combination discloses or suggests these limitations. (Ex. 1002, ¶¶108-120.) As discussed above in Section IX.A.1(a), *Isogai* discloses a solid state imaging device that includes a solid state image sensing element as shown in figure 1 in combination with the processing system shown in figure 22. (*Supra* Seciton IX.A.1(a).)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶108.)

Isogai does not explicitly disclose that the red, blue, and green pixels are disposed on a first chip with the analog-to-digital converters, while the color

interpolation circuit is disposed on a second chip as recited in claim 4. However, including the pixels and analog-to-digital converters on a first chip and the associated color interpolation circuitry on a second chip is disclosed by *Neter*, and a POSITA would have found it obvious in view of *Neter* to implement the recited components of *Isogai* on two separate chips as recited in claim 4. (Ex. 1002, ¶¶109-120.)

As above in section IX.B.1, a POSITA implementing an image sensing device as disclosed in *Isogai* would have had reason to look to *Neter*. (*Supra* Section IX.B.1.) *Neter* discloses that the disclosed imaging system, which includes red, blue, and green pixels, analog-to-digital converters, and additional processing circuitry like a color interpolation circuit can be implemented on one or more chips. (Ex. 1002, ¶111.) For example, *Neter* discloses an array of red, green, and blue pixels arranged in the Bayer color pattern (Ex. 1007, 7:33-37) where additional components of the imaging system, including analog-to-digital converters and color interpolation circuitry, may or may not be included on the same integrated circuit as the array of pixels. (*Id.*, 5:47-52 ("The imaging system in accordance with the present invention may also include additional **on-chip or off chip** amplification stages, **analog-to-digital conversion units**, memory units and various other **signal processing blocks**.") (emphasis added), 7:48-53, 7:55-63, 3:1-3; Ex. 1002, ¶111.)

Given *Neter's* disclosure of various image processing system components being included either on the same chip as the pixel array or on another chip separate from the pixel array, a POSITA would have found it obvious to combine the teachings of *Neter* and *Isogai* such that *Isogai's* imaging device would include the analog-to-digital converters on the same chip as the red, blue, and green pixels, whereas the color interpolation circuitry is on a separate chip. (Ex. 1002, ¶112) Such a skilled person would have been motivated to do so because, in some embodiments, while integration may have been desirable, the complexity of the color interpolation circuitry may require significant hardware and software that would be better implemented on a separate chip. (*Id*.; Ex. 1007, 1:32-49.) Indeed, *Isogai* recognizes that implementing components of its imaging device on on the same or different chips is a design choice. (Ex. 1005, ¶[0065] (disclosing, with respect to the embodiment shown in FIG. 17, that the output buffer amplifiers 28a-28d can be provided "inside the solid-state image sensing element in order to avoid the influence of external noise" whereas differential amplifiers 34a-b are provided "outside the solid-state image sensing element.", FIG. 17; Ex. 1002, ¶113.)

Neter discloses that in conventional image processing systems (like that disclosed by *Isogai*) the image processing **may require** significant resources that could increase the complexity, size and expense of the imaging device. (Ex. 1007, 1:32-49; Ex. 1002, ¶114.) A POSITA reading *Neter* would have understood that

Neter discloses that the color interpolation circuitry, as well as the analog-to-digital conversion circuitry, can either be placed on the same chip as the pixel array or not, where the decision as to whether to use one chip or two is a design choice that is influenced by many factors, including the complexity of pixel interpolation and other image processing, the size of the pixel array, the complexity of the analog-to-digital converters, as well as the presence or absence of additional intervening circuitry between the pixel array and the color interpolation circuitry. (Ex. 1002, ¶114.)

Indeed, a POSITA would have understood that while integration of circuitry onto a single chip can provide a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like, in some instances it is preferable to maintain the color interpolation circuitry on a separate chip while integrating the analog-to-digital converters onto the same chip as the pixel array. (Ex. 1002, ¶115.) For instance, including the analog-to-digital conversion on the same chip as the pixel array while keeping the color interpolation circuitry on a separate chip provides flexibility to support different systems/applications with different levels of color processing. (*Id*.) In such a scenario, a pixel-array chip that includes analog-to-digital converters would provide digital outputs that can be provided as the inputs to different color interpolation/processing chips with different processing capabilities in order to satisfy the needs of different applications. (*Id*.)

Such an understanding is supported by contemporaneous references that disclose analog-to-digital converters included with the pixel array on the same chip while the color interpolation circuitry resides on a separate chip. (Ex. 1002, ¶116.) For example, *Fossum* (Ex. 1008) discloses CMOS imagers with analog-to-digital conversion on the same chip as the pixel array "to provide a digital representation of the image which can be retrieved from the imager 10 through a parallel port interface." (Ex. 1008, 1:7-26, FIG. 1; Ex. 1002, ¶116.)

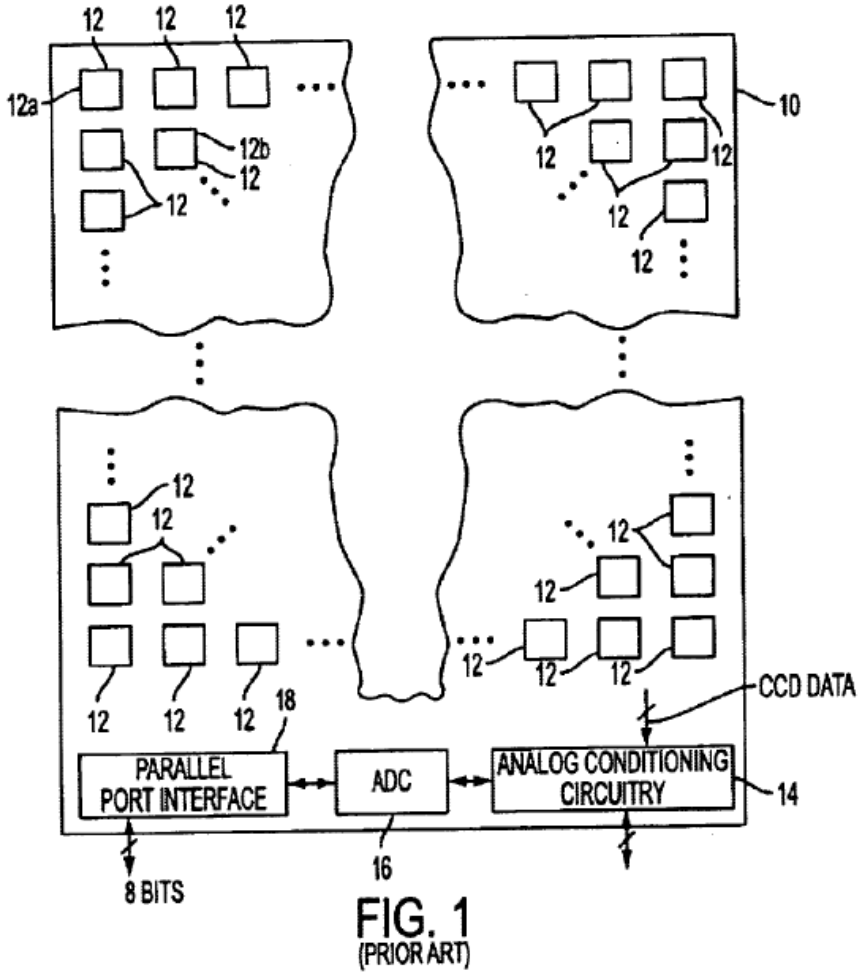


FIG. 1
(PRIOR ART)

(Ex. 1008, FIG. 1.) *Fossum* further discloses that a separate DSP chip 30 can be used with the imaging chip 10 above, where the DSP chip performs color interpolation. (*Id*., 2:5-7.)

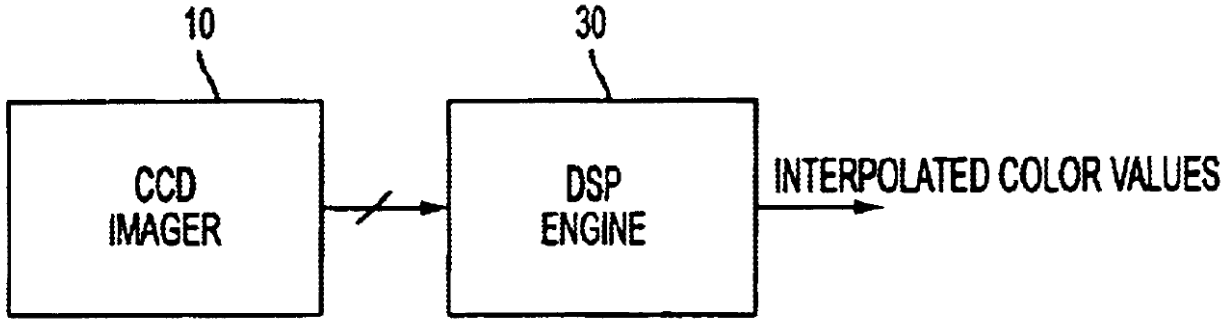


FIG. 4
(PRIOR ART)

(*Id*., FIG. 4.)

Therefore, in view of *Neter* and having knowledge of the state of the art at the relevant time, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters on the same chip as the pixel array, while providing a second chip that includes the color processing circuitry. (Ex. 1002, ¶117.) Including the analog-to-digital converters on the same chip as the pixel array in the imaging device of *Isogai* and a second chip that includes the color processing circuitry would have merely involved the use of a known technique (performing analog-to-digital conversion of the pixel outputs on the same chip as the red, blue, and green pixels and color processing on a separate chip) to improve a similar device (the device described in *Isogai*) to achieve the expected and desired result of increased integration while maintaining flexibility to support different systems/applications with different levels

of pixel interpolation. (Ex. 1002, ¶118; *KSR*, 550 U.S. at 416-417.) Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a POSITA would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation of success. *KSR*, 550 U.S. at 421. Therefore, the *Isogai-Neter* combination discloses or suggests the features recited in claim 4 of the '651 patent. (Ex. 1002, ¶119.)

Including the analog-to-digital converters of *Isogai's* imaging device on the same chip as the pixel array and the color processing circuitry on another chip would have been straightforward for a POSITA to implement given such a person's knowledge of the state of the art and the disclosure in *Neter*. (Ex. 1002, ¶120.) For example, as demonstrated by *Neter*, *Fossum*, and *Loinaz*, a POSITA at the relevant time had the capability to include both the analog-to-digital conversion circuitry and the color processing (color interpolation) circuitry on the same chip as the pixel array. (Ex. 1007, 5:47-52; Ex. 1008, FIGs. 1, 5; Ex. 1010, FIG. 1; *infra* section IX.B.4; Ex. 1002, ¶120.) Therefore, such a POSITA would also have been able to include a subset of those components on the same chip while keeping the color processing circuitry on a second chip. (Ex. 1002, ¶120.) Moreover, a POSITA

would have understood how to make any needed modifications in order to ensure that such an implementation was succesful. (*Id*.)

4. Claim 5

a) The solid stage imaging device of claim 1 further comprising a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.

The *Isogai-Neter* combination discloses or suggests these limitations. (Ex. 1002, ¶¶121-128.) *Isogai* does not explicitly disclose that the components recited in claim 5 are included on a single integrated circuit. *Neter*, however, discloses such a feature, and a POSITA would have found it obvious, in view of *Neter*, to implement the imaging device of *Isogai* such that all of the components recited in claim 5 are on the same chip. (Ex. 1002, ¶¶121-122.)

As discussed above in Section IX.B.3, *Neter* discloses including the circuitry for color interpolation and the analog-to-digital conversion circuitry on the same chip as the pixel array. (Ex. 1007, 5:47-52, 7:33-37, 7:48-53, 7:55-59, 3:1-3; Ex. 1002, ¶122.) As also discussed above in Section IX.B.3, a POSITA would have understood, based on the disclosure of *Neter* and the understanding of the state of the art, that implementing the analog-to-digital converters and color processing circuitry ("color interpolation circuit") on the same chip as the pixel array in an image processing device is a design choice. (*Supra* section IX.B.3.) Moreover, a

POSITA would have been motivated to include all of these components of an imaging device, like that disclosed by *Isogai*, on the same chip in order to realize a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like. (*Id*.; Ex. 1002, ¶121.) Therefore, in view of *Neter* and having knowledge of the state of the art at the relevant time, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters and the color processing circuitry on the same chip as the pixel array. (Ex. 1002, ¶122.)

Including the analog-to-digital converters and color processing circuitry on the same chip as the pixel array in the imaging device of *Isogai* would have merely involved the use of a known technique (performing analog-to-digital conversion and color processing on the same chip as the red, blue, and green pixels as disclosed in *Neter*) to improve a similar device (the imaging device of *Isogai*) to achieve the expected and desired result of increased integration that can provide increased speed, reduced costs, and support for smaller devices. (Ex. 1002, ¶123; *KSR*, 550 U.S. at 416-417.) Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. (Ex. 1002, ¶123.) Thus, a POSITA would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable

expectation of success. *KSR*, 550 U.S. at 421. Therefore, the *Isogai-Neter* combination discloses or suggests the features recited in claim 5 of the '651 patent. (Ex. 1002, ¶124.)

Including the analog-to-digital conversion and color processing circuitry on the same chip with *Isogai's* solid-state image sensing element as shown in figure 1 would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in *Neter*. (*Id*.) Indeed, the motivation and ability for a POSITA to perform such integration is supported by *Fossum*, which discloses CMOS imagers with analog-to-digital conversion and color interpolation circuitry on the same chip as the pixel array. (*Id*., ¶¶125-126; Ex. 1008, 4:4-6, 4:33-44, FIG. 5.)

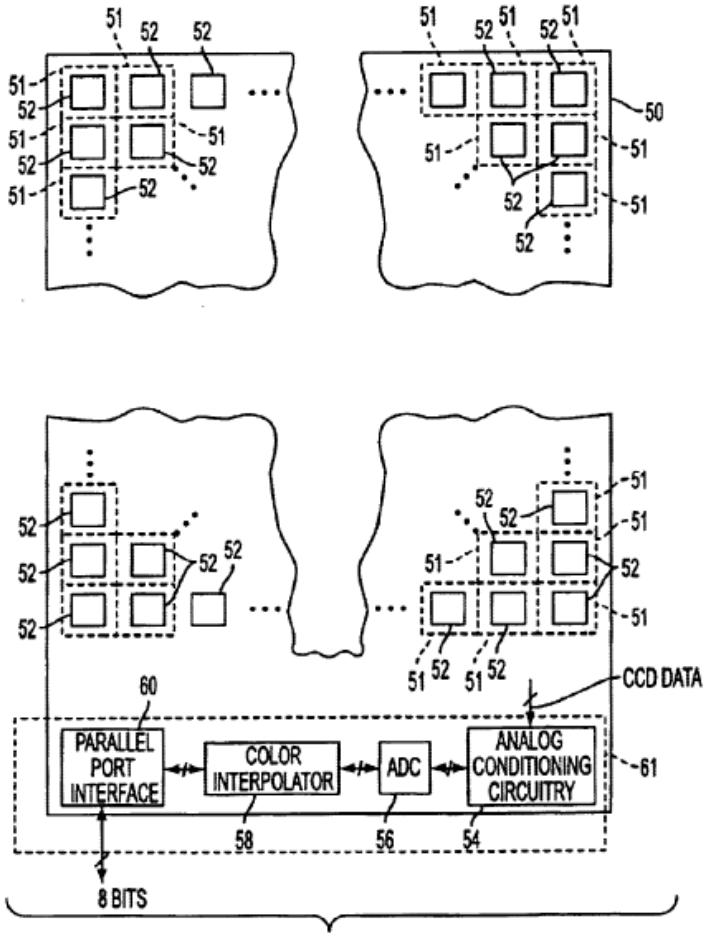
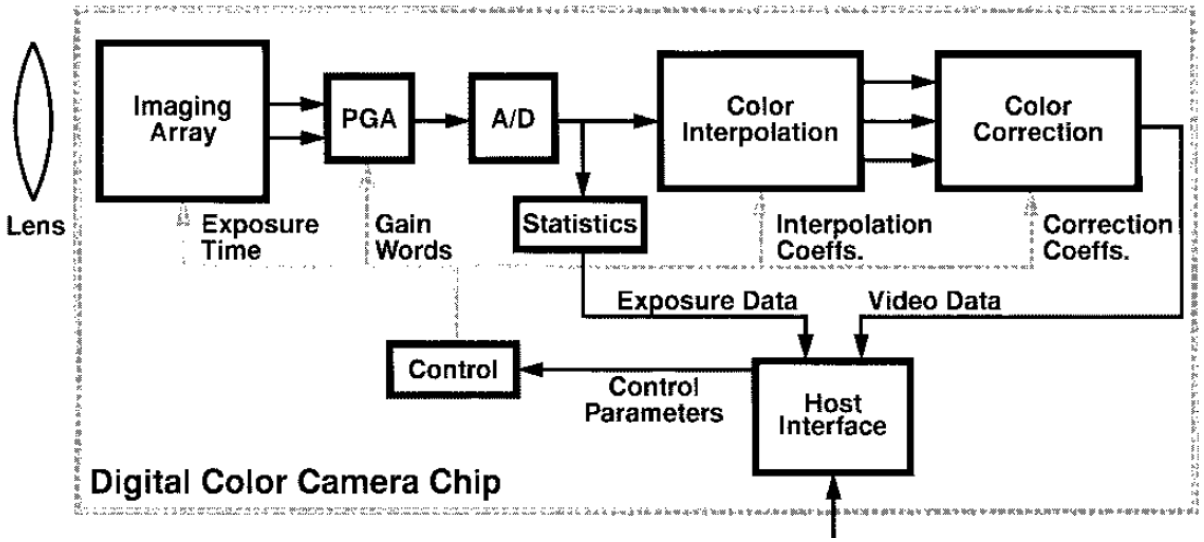


FIG. 5

(Ex. 1008, FIG. 5.)

Similarly, as shown in figure 1 below, *Loinaz* discloses a digital color camera chip that includes the imaging array, analog-to-digital conversion circuitry, and color interpolation circuitry on the same chip. (Ex. 1010, Abstract, FIG. 1; Ex. 1002, ¶¶127-128.)



(Ex. 1010, FIG. 1 (excerpt).

5. Claim 19

a) The imaging method of claim 18 further comprising: correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

The *Isogai-Neter* combination discloses these limitations for the reasons discussed above in Section IX.B.1. (*Supra* Section IX.B.1; Ex. 1002, ¶129.)

6. Claim 20

a) The imaging method of claim 18 further comprising: correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

The *Isogai-Neter* combination discloses these limitations for the reasons discussed above in Section IX.B.2. (*Supra* Section IX.B.2; Ex. 1002, ¶130.)

7. Claim 21

a) The imaging method of claim 18, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, and the second analog-to-digital converter are disposed on a first chip and the color interpolation circuit is disposed on a second chip.

The *Isogai-Neter* combination discloses these limitations for the reasons discussed above in Section IX.B.3. (*Supra* Section IX.B.3; Ex. 1002, ¶131.)

8. Claim 22

a) The imaging method of claim 18, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit is disposed on a chip.

The *Isogai-Neter* combination discloses these limitations for the reasons discussed above in Section IX.B.4. (*Supra* Section IX.B.4; Ex. 1002, ¶132.)

C. Ground 3: Claims 2-5 and 19-22 Are Obvious Over *Isogai* in View of *Fossum*

1. Claim 2

Isogai in view of *Fossum* discloses or suggests these features. (Ex. 1002, ¶¶133-145.) *Isogai's* imaging device discussed above with respect to claim 1 does not explicitly disclose an error compensation circuit for correcting a gain of the outputs of the red, blue, and green pixels. However, as demonstrated below, *Fossum* discloses correcting a gain in the form of gain control of the analog signal outputs from the pixels, and a POSITA would have found it obvious in view of *Fossum* to

utilize such gain correction in the solid state imaging device that includes the solid state image sensing element corresponding to the first embodiment of *Isogai*. (Ex. 1002, ¶¶134-135.)

Fossum, like *Isogai*, describes circuits for processing red, blue, and green imaging pixel sensor elements that includes color interpolation. (Ex. 1008, 4:45-59, FIG. 5.) As shown in figure 5 below, *Fossum* discloses color interpolation done after analog-to-digital conversion, similar to as described in *Isogai*. (Ex. 1008, FIG. 5; *see also id*., 5:7-11; Ex. 1002, ¶¶136-138.) Therefore, a POSITA implementing the image sensing device of *Isogai* would have had reason to look to *Fossum.* (Ex. 1002, ¶137.)

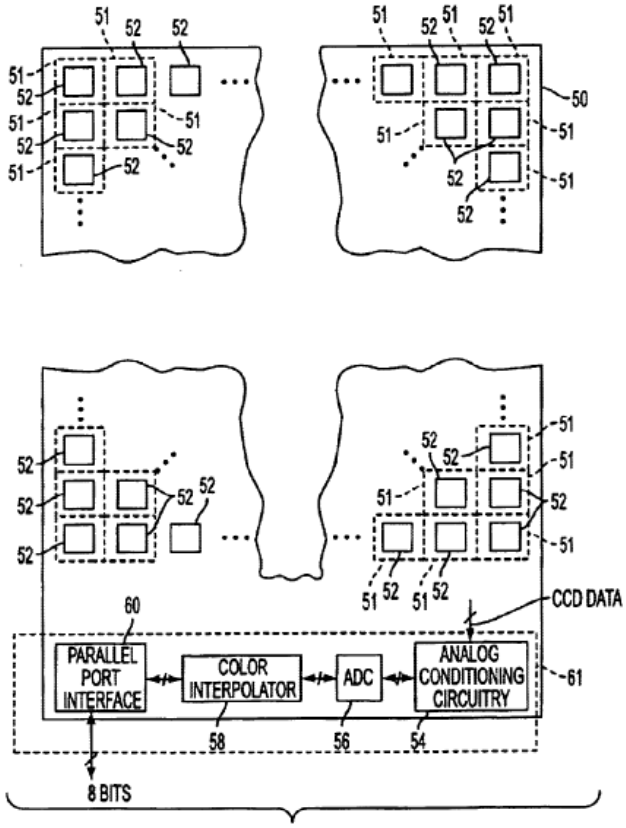


FIG. 5

(Ex. 1008, FIG. 5.)

Fossum further discloses analog conditioning circuitry 54 that performs "correlated double sampling of the analog outputs of the pixel cells 52 **and provide[s] gain control**" for the outputs of the pixels in the array. (*Id*.; Ex. 1008, 5:4-6, FIG. 6 (emphasis added).) A POSITA would have understood that *Fossum's* disclosure of gain control with respect to the analog outputs of the pixels constitutes "correcting a gain" of one of the pixel outputs as is recited in claim 2. (Ex. 1002, ¶¶138-141.) Such an understanding is supported by *Neter*, which discloses that imaging devices perform color compensation, which involves adjusting the gain of

signals for different colored pixels as the pixel elements may be more responsive to one color of light in comparison to another color of light. (Ex. 1007, 1:50-2:6, 4:19-36; *supra* Section IX.B.2.) A POSITA would also have understood *Fossum's* "analog conditioning circuitry" to correspond to an "error compensation circuit" as recited in claim 2 as it performs the gain correction ascribed to the claimed error compensation circuit in that the gain control is able to compensate for magnitude variations for the different color components. (Ex. 1002, ¶141.)

Given the disclosure of a gain control in *Fossum*, a POSITA would have found it obvious to combine the teachings of *Isogai* and *Fossum* such that at least one of the output signals for the red, blue, first green, and second green pixels identified above in Sections IX.A.1(b)-(e) is amplified in order to correct the gain for that color in the image sensing device. (Ex. 1002, ¶142.) A POSITA would have been motivated to do so because such gain correction can compensate for "differences in the response of various color filters and variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing." (*Id.*; Ex. 1007, 13:30-34.) A POSITA would have understood that such gain correction improves color dynamic range and image quality. (Ex. 1007, 13:34-39; Ex. 1002, ¶142.)

Including analog-conditioning circuitry for gain control like that disclosed in *Fossum* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements (the imaging array with pixel outputs of

Isogai with the gain control as disclosed in *Fossum* to compensate for needed gain differentials between different colored pixels) using known circuit design methods, where each element performs the same function described in *Isogai* and *Fossum*, to achieve the predictable result of an imaging device that is improved to provide color compensation. (Ex. 1002, ¶143; *KSR*, 550 at 416.) As discussed above, both *Isogai* and *Fossum* describe circuits for processing imaging pixel sensor elements, but *Fossum* describes conditioning circuitry not found in *Isogai* for providing gain control. Therefore, a POSITA would have recognized that *Fossum*'s teachings relating to gain control could have been applied to *Isogai*'s system in a similar way. *Id.* at 417. As also discussed above, a POSITA would have been encouraged to implement such gain control in *Isogai*'s system to provide similar gain control capabilities to improve overall system performance. (Ex. 1002, ¶143.)

Additionally, including such gain control circuitry in *Isogai's* imaging device would have been straightforward for a POSITA given such a person's knowledge and the disclosure in *Fossum*. (Ex. 1002, ¶144.) For example, the combination would have required nothing more than adding well-known, rudimentary, and widely available conditioning circuitry for gain control to *Isogai*'s system, which was commonly used for color correction at the time. Such a combination would not have detracted from the overall functionality of *Isogai*'s system, which would have

continued to operate as described in *Isogai* with the added circuity to improve color output as necessary. (*Id*.)

2. Claim 3

Isogai in view of *Fossum* discloses or suggests these features. (Ex. 1002, ¶¶146-155.) The solid state imaging device discussed above in Section IX.A.1 does not explicitly disclose an error compensation circuit for correcting a fixed pattern noise offset from one of the analog signals output by the red, blue, and green pixels. However, *Fossum* discloses correcting a fixed pattern noise offset in the outputs from red, blue, and green pixels, and a POSITA would have found it obvious in view of *Fossum* to utilize such fixed pattern noise offset correction in the solid state imaging device of *Isogai* that includes the solid state image sensing element corresponding to the first embodiment. (Ex. 1002, ¶¶147-148.)

As discussed above in section IX.C.1, *Fossum*, like *Isogai*, describes circuits for processing imaging pixel sensor elements, and a POSITA implementing an image sensing device as disclosed in *Isogai* would have had reason to look to *Fossum*. (*Supra* section IX.C.1.) As also discussed above in Section IX.C.1, *Fossum* discloses analog conditioning circuitry that performs correlated double sampling and gain control with respect to the analog outputs of the pixels. (*Supra* section IX.C.1; Ex. 1007, 1:20-22, 5:4-6; Ex. 1002, ¶149.)

A POSITA would have understood that the correlated double sampling of the outputs of the pixels by *Fossum's* analog conditioning circuitry reduces fixed pattern noise. (Ex. 1011, 7:34-38; Ex. 1012, 40:17-23; Ex. 1002, ¶150.) Therefore, *Fossum* discloses an "error compensation circuit for correcting a fixed pattern noise offset" from one of the outputs of the red, blue, and green pixels as recited in claim 3. (Ex. 1002, ¶151.)

Given the disclosure of fixed pattern noise offset reduction by correlated double sampling in *Fossum*, a POSITA would have found it obvious to combine the teachings of *Isogai* and *Fossum* such that at least one of the output signals for the red, blue, first green, and second green pixels is conditioned in a manner that includes correlated double sampling in order to reduce fixed pattern noise in *Isogai's* image sensing device. (Ex. 1002, ¶152.) A POSITA would have been motivated to do so because, as such a skilled person would have known, such fixed pattern noise reduction allows for increased dynamic range and higher image quality. (*Id.*; Ex. 1007, 5:12-14, 15:64-66.)

Including fixed pattern noise reduction circuity like that disclosed in *Fossum* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements (the image array with pixel outputs of *Isogai* with the correlated double sampling circuitry of *Fossum* to compensate for fixed pattern noise) using known circuit design methods, where each element

performs the same function described in *Fossum* and *Isogai*, to achieve the predictable result of an imaging device that is improved have higher image quality because of reduced noise. (Ex. 1002, ¶154; *KSR*, 550 U.S. at 416.) As discussed above, both *Isogai* and *Fossum* describe circuits for processing imaging pixel sensor elements, but *Fossum* describes additional circuitry not found in *Isogai* for correlated double sampling. Therefore, a POSITA would have recognized that *Fossum's* teachings relating to noise reduction could have been applied to *Isogai*'s system in a similar way. *Id.* at 417. As also discussed above, a POSITA would have been encouraged to implement such correlated double sampling in *Isogai*'s system to provide similar noise reduction capabilities to improve overall system performance, including improved image quality. (Ex. 1002, ¶154.)

Additionally, including such fixed pattern noise correction circuitry in *Isogai's* imaging device would have been straightforward for a POSITA given such a person's knowledge and the disclosure in *Fossum*. (Ex. 1002, ¶155.)

3. Claim 4

The *Isogai-Fossum* combination discloses or suggests these limitations. (Ex. 1002, ¶¶155.) *Isogai* does not explicitly disclose that, for the solid state imaging device discussed in section IX.A.1 above and depicted below, the pixels and analog-to-digital converters are disposed on a first chip and the color interpolation circuit is disposed on a second chip as recited in claim 4. However, such a configuration is

disclosed by *Fossum*, and a POSITA would have found it obvious in view of *Fossum* to implement the recited components in *Isogai* on two separate chips as recited in claim 4. (Ex. 1002, ¶157.)

As discussed above in section IX.C.1, a POSITA implementing an image sensing device as disclosed in *Isogai* would have had reason to look to *Fossum*. (*Supra* section IX.C.1.) *Fossum* discloses CMOS imagers with analog-to-digital conversion on the same chip as a red, blue, and green pixel array "to provide a digital representation of the image which can be retrieved from the imager 10 through a parallel port interface." (Ex. 1008, 1:7-26, FIG. 1 (showing analog to digital converter (ADC) 16 on the same chip as pixel cells 12); Ex. 1002, ¶159.)

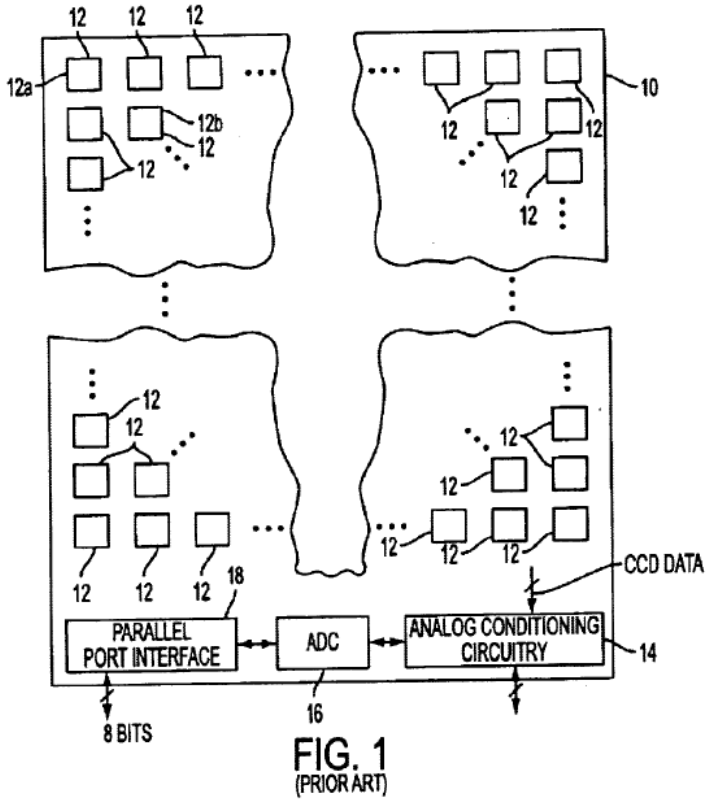


FIG. 1
(PRIOR ART)

(Ex. 1008, FIG. 1.) *Fossum* further discloses that a separate DSP chip 30 is used with the imaging chip 10 above, where the DSP chip 30 performs color interpolation. (*Id*., 2:5-7; Ex. 1002, ¶159.)

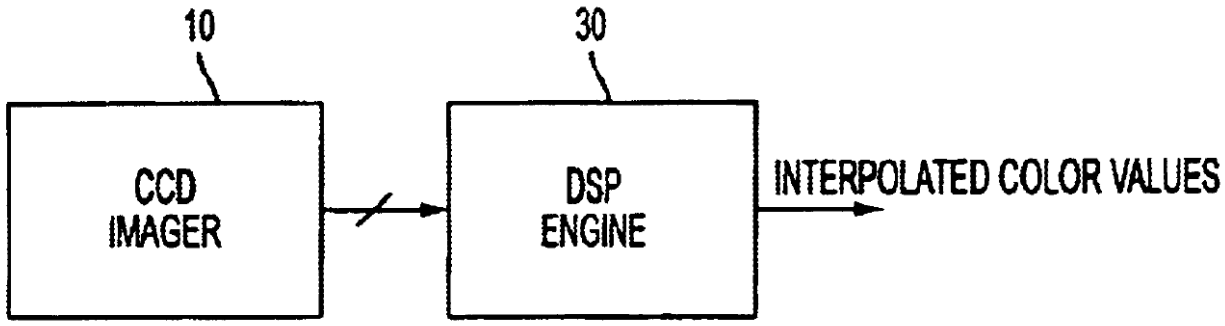


FIG. 4
(PRIOR ART)

(Ex. 1008, FIG. 4.)

Therefore, *Fossum* discloses the arrangement of components on two chips as recited in claim 4. (*Id*.; Ex. 1002, ¶160.) In view of *Fossum*, a POSITA implementing the imaging device of *Isogai* would have found it obvious to include *Isogai's* analog-to-digital conversion circuitry on the same chip with the red, blue, first green and second green pixels while maintaining the color processing circuitry on a separate chip. (Ex. 1002, ¶160.)

As discussed above in Section IX.B.3, a POSITA would have understood that while integration of circuitry onto a single chip can provide a number of advantages, in some instances it may be preferable to maintain the color interpolation circuitry

on a separate chip while integrating the analog-to-digital converters onto the same chip as the pixel array. (*Supra* section IX.B.3.) For example, such an arrangement would provide flexibility to support different systems/applications with different levels of color processing. (*Id*.; Ex. 1008, 1:24-26; Ex. 1002, ¶161.)

Moreover, a POSITA would have understood that determining whether to put the analog-to-digital converters and/or color interpolation circuitry for an image processing system on the same chip with the pixel array is a design choice that is influenced by many factors. (*Supra* section IX.B.3; Ex. 1002, ¶¶162-163.) Indeed, *Isogai* recognizes that implementing components of its imaging device on the same or different chips is a design choice. (Ex. 1007, ¶[0065], FIG. 17; Ex. 1002, ¶162.)

Therefore, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters on the same chip as the pixel array, while providing the color processing circuitry on a second chip. (Ex. 1002, ¶164.) Such a configuration would have merely involved the use of a known technique (performing analog-to-digital conversion on the same chip as the pixels as disclosed in *Fossum* and color processing on a separate chip) to improve a similar device (the device of *Isogai*) achieve the expected and desired result of increased integration while maintaining flexibility to support different systems/applications with different levels of color processing. (Ex. 1002, ¶165; *KSR*, 550 U.S. at 416-417.) Additionally, as discussed

above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a POSITA would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful. *KSR*, 550 U.S. at 421.

Including the analog-to-digital conversion with the pixel array in *Isogai's* imaging device would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in *Fossum*. (Ex. 1002, ¶¶166-167; *supra* section IX.B.3.)

4. Claim 5

The *Isogai-Fossum* combination discloses or suggests these limitations. (Ex. 1002, ¶¶168-177.) *Isogai* does not explicitly disclose that the components recited in claim 5 are included on a single integrated circuit. *Fossum*, however, discloses such a feature, and a POSITA would have found it obvious, in view of *Fossum*, to implement the imaging device of *Isogai* such that all of the components recited in claim 5 are on the same chip. (Ex. 1002, ¶169.)

Fossum discloses including the circuitry for color interpolation and the analog-to-digital conversion circuitry on the same chip as the pixel array. (Ex. 1008, 4:33-44, FIG. 5; Ex. 1002, ¶171.)

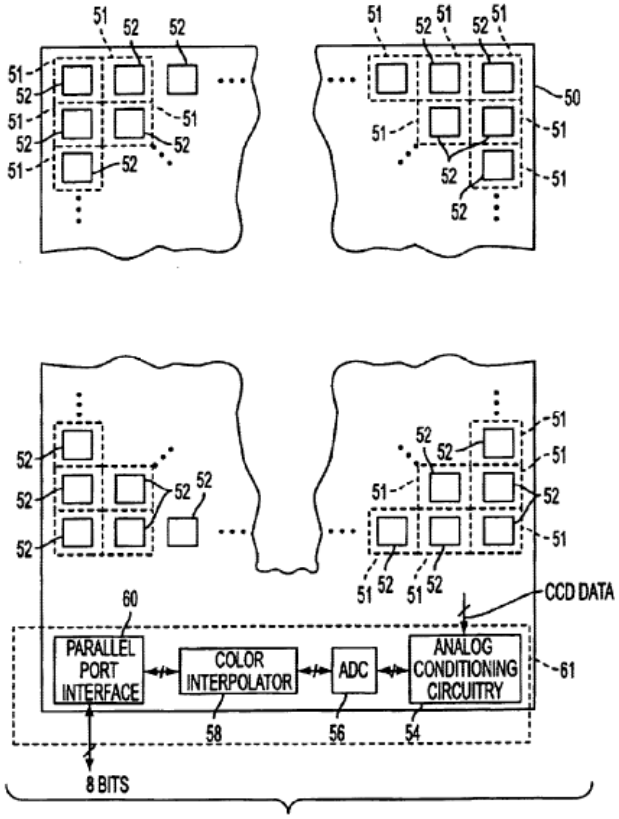


FIG. 5

(Ex. 1008, FIG. 5.)

Fossum discloses that "FIG. 5 shows a CMOS imager 50 located on a monolithic semiconductor substrate, or chip" (*id*., 4:33-34), without "requiring . . . off chip-color interpolation" (*id*., 4:40-44). According to *Fossum*, "[a]mong the advantages of the invention" is [t]rue color imaging occurs on a single semiconductor chip." (*Id*., 4:4-6; *see also id*., 4:45-58; Ex. 1002, ¶172.)

As discussed above in Section IX.C.3, a POSITA would have understood that implementing the analog-to-digital converters and color processing circuitry on the

same chip as the pixel array is a design choice. (*Supra* section IX.C.3; Ex. 1002, ¶170) Moreover, a POSITA would have been motivated to include all of these components of an imaging device, like that disclosed by *Isogai*, on the same chip in order to realize a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like. (*Supra* section IX.B.3; Ex. 1002, ¶170.) Therefore, in view of *Fossum* and having knowledge of the state of the art at the relevant time, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters and the color processing circuitry on the same chip as the pixel array. (Ex. 1002, ¶170-172.) Such integration would have merely been the use of a known technique (performing analog-to-digital conversion and color processing on the same chip as the pixels as disclosed in *Fossum*) for a similar device (the imaging device of *Isogai*) to achieve the expected and desired result of increased integration that can provide increased speed, reduced costs, and support for smaller devices. (*Id*.; *KSR*, 550 U.S. at 416-417.) Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a POSITA would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful. (Ex. 1002, ¶173; *KSR*, 550 U.S. at 421.)

Including the analog-to-digital converters and color processing circuitry in *Isogai's* solid-state image sensing element as shown in figure 1 would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in Fossum. (*Supra* section IX.B.4; Ex. 1010, Abstract, FIG. 1; Ex. 1002, *Id*., ¶¶174-177.)

5. Claims 19-22

The *Isogai-Neter* combination discloses the limitations of each of claims 19-22 for the reasons discussed above for each of claims 2-5, respectively. (*Supra* Sections IX.C.1-4; Ex. 1002, ¶178.)

D. Ground 4: Claims 1-3 and 18-20 Are Anticipated by *Inuiya*[5]

1. Claim 1

a) Claim 1[a]

To the extent the preamble of claim 1 is limiting, *Inuiya* discloses the limitations therein. (Ex. 1002, ¶¶179-181.) For instance, *Inuiya* discloses a "a solid-state electronic image sensing device and a method of reading a signal change out of the solid-state electronic image sensing device." (Ex. 1006, 1:15-18; *see also id*., 2:20-23; 4:56-67.) Figure 18 of *Inuiya* is a block diagram of a digital video tape

[5] Petitioners do not repeat the language of the challenged claims, which is presented above.

recorder that includes an image sensing section with a charge-coupled device (CCD) 100 that includes a large number of pixels. (*Id*., 20:12-22; Ex. 1002, ¶181.)

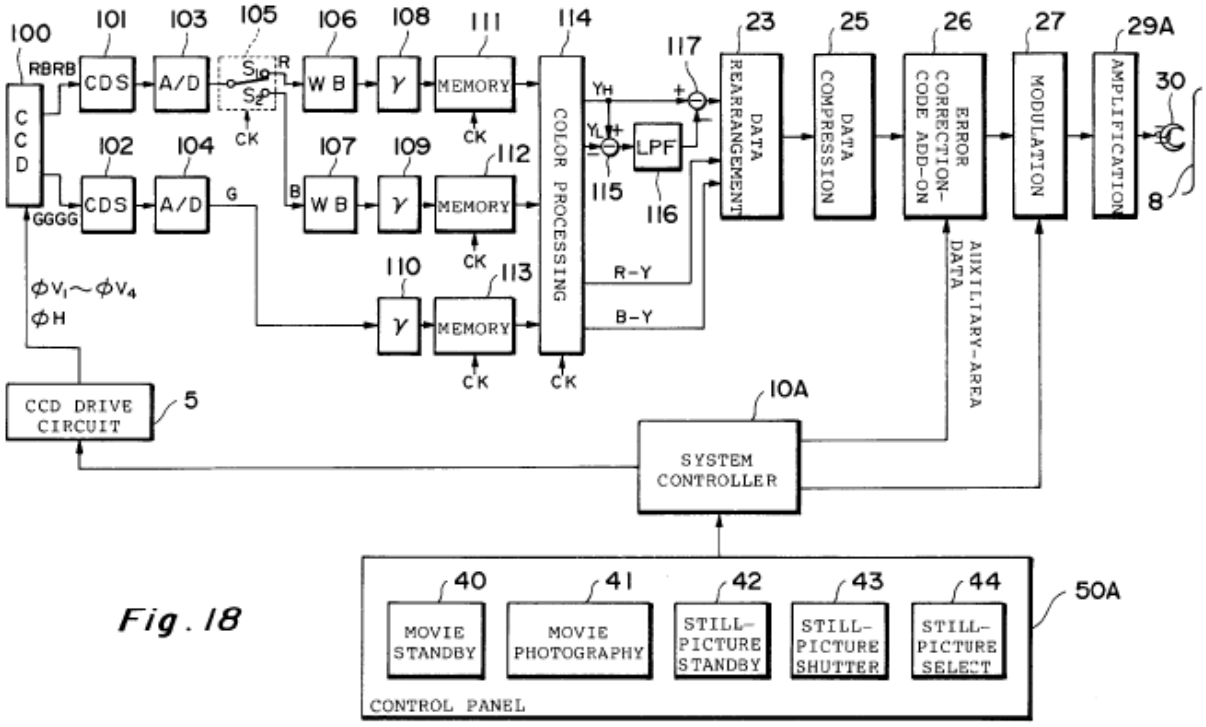


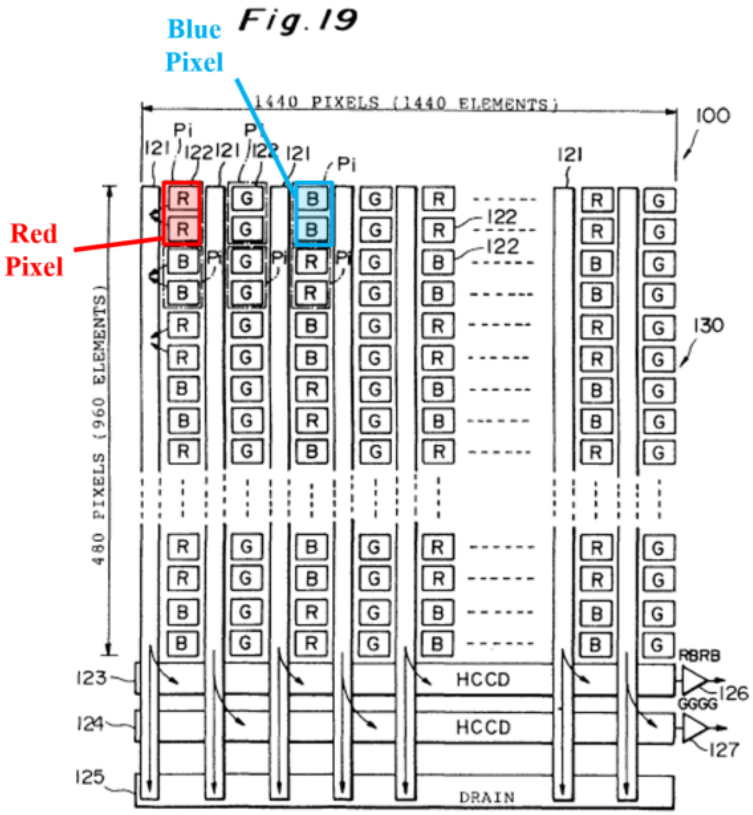
Fig. 18

(Ex. 1006, FIG. 18.) Image data from the CCD 100 is provided to color processing circuit 114, which combines the pixel data to generate luminance and color difference data. (*See infra* Section IX.D.1(h).) *Inuiya's* digital tape recorder constitutes a "solid-state image processing device" as recited in claim 1. (Ex. 1002, ¶181.)

b) Claim 1[b]

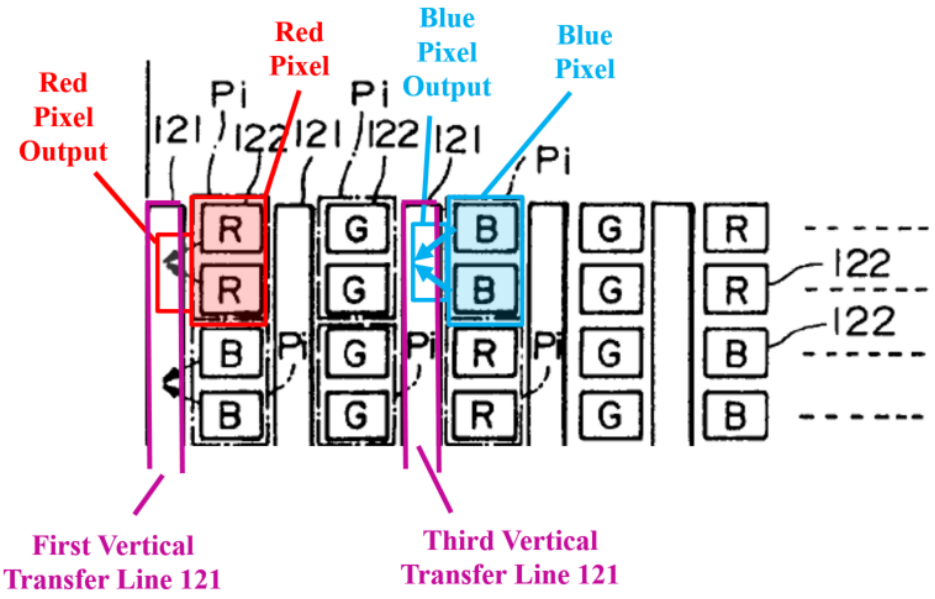
c) Claim 1[c]

Inuiya discloses these limitations. (Ex. 1002, ¶¶182-184.) Figure 19 of *Inuiya* is a schematic view of the CCD 100 included in the solid-state image processing device shown in figure 18. (Ex. 1006, 20:23.) The CCD 100 includes a plurality of red and blue pixels, including the red and blue pixels highlighted in annotated figure 19 below.



(Ex. 1006, FIG. 19 (annotated); Ex. 1002, ¶182.)

Inuiya discloses that the signal charges that have accumulated in two photodiodes are mixed in the vertical transfer lines 121 of the CCD 100 such that the pixels, which are labeled "Pi" in figure 19, are each composed of two photodiodes 122. (*Id*., 20:33-44, 20:47-62, FIG. 19; Ex. 1002, ¶¶182-183.) Therefore, each of the red and blue pixels has an output shown in annotated figure 19 below. (Ex. 1002, ¶¶183-184.) *Inuiya* discloses that a transfer gate is used to control when the charge for each pixel is applied to the vertical transfer line. (Ex. 1006, 21:7-12; Ex. 1002, ¶184.)



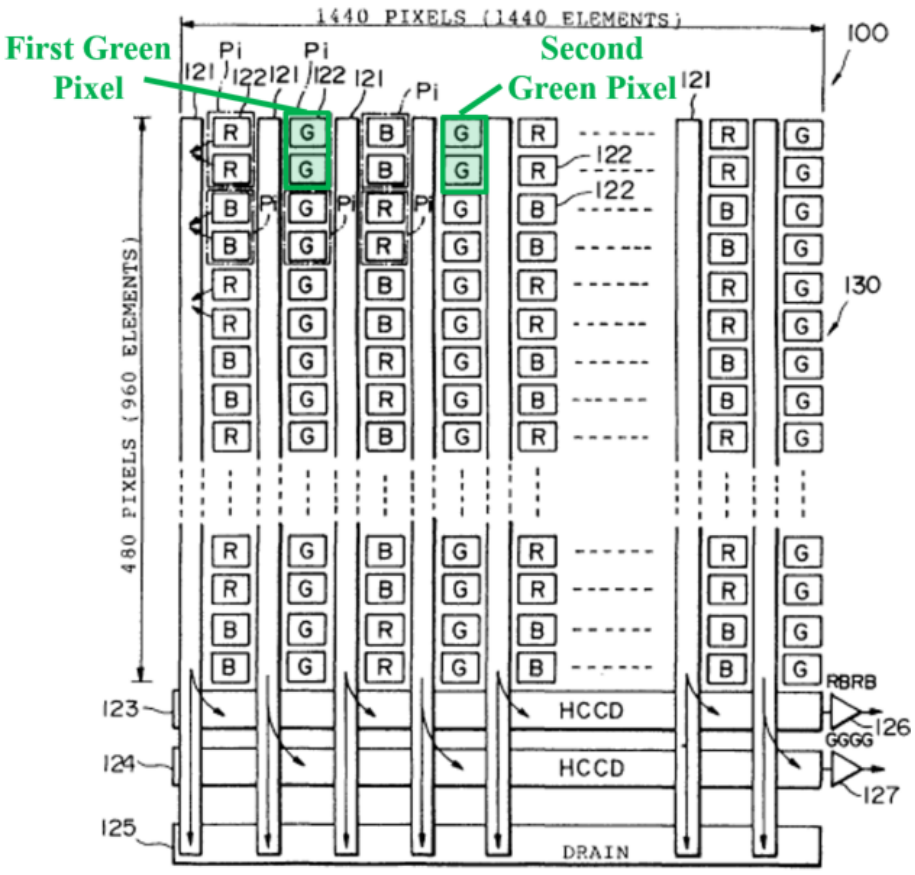
(Ex. 1006, FIG. 19 (excerpt, annotated); Ex. 1002, ¶184.)

d) Claim 1[d]

e) Claim 1[e]

Inuiya discloses these limitations. (Ex. 1002, ¶¶185-186.) As shown in annotated figure 19 below, *Inuiya's* pixel array includes first and second green pixels, which, like the red and blue pixels discussed above in Sections IX.D.1(b)-(c), are each made up of two photodiodes and have an output. (*Supra* Sections IX.D.1(b)-(c); Ex. 1006, 20:33-62.) For example, *Inuiya* discloses "a first green pixel" a "second green pixel" (fourth column), which are highlighted in annotated figure 19 below. (Ex. 1002, ¶185.)

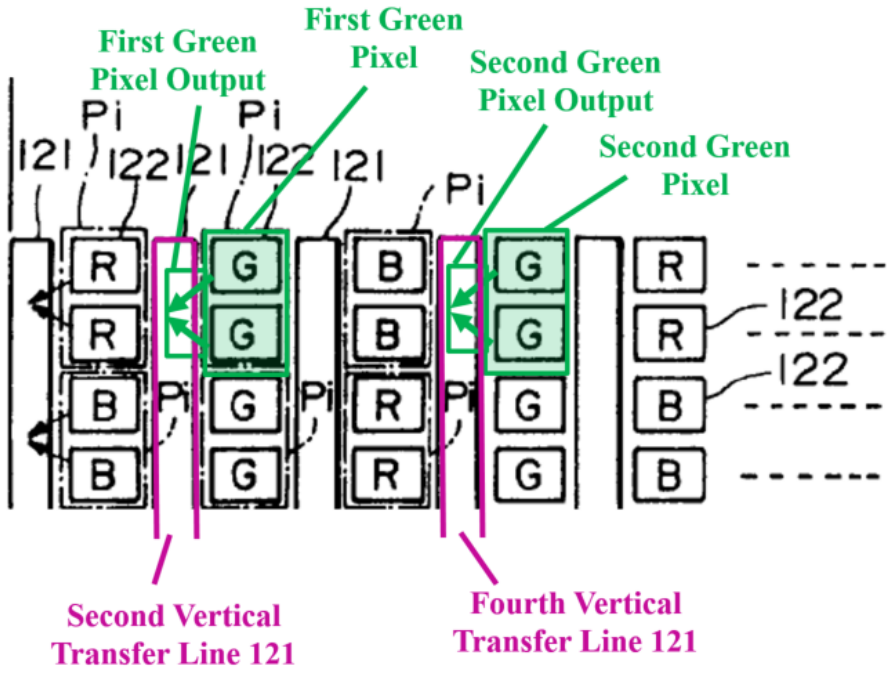
Fig. 19



(Ex. 1006, FIG. 19 (annotated); Ex. 1002, ¶185.)

Inuiya discloses that the outputs of the first green pixel and second green pixel are connected to vertical transfer lines 121 just to the left of each of the green pixels. (*Supra* Section IX.D.1(b); Ex. 1006, 20:47-62, 21:7-12, FIG. 19; Ex. 1002, ¶186.) As shown in the enlarged and annotated excerpt of figure 19 below, the output of the highlighted first green pixel is connected to the second vertical transfer line and the

output of the second green pixel is connected to the fourth vertical transfer line. (Ex. 1006, 20:47-62, 21:7-12, FIG. 19; Ex. 1002, ¶186.)



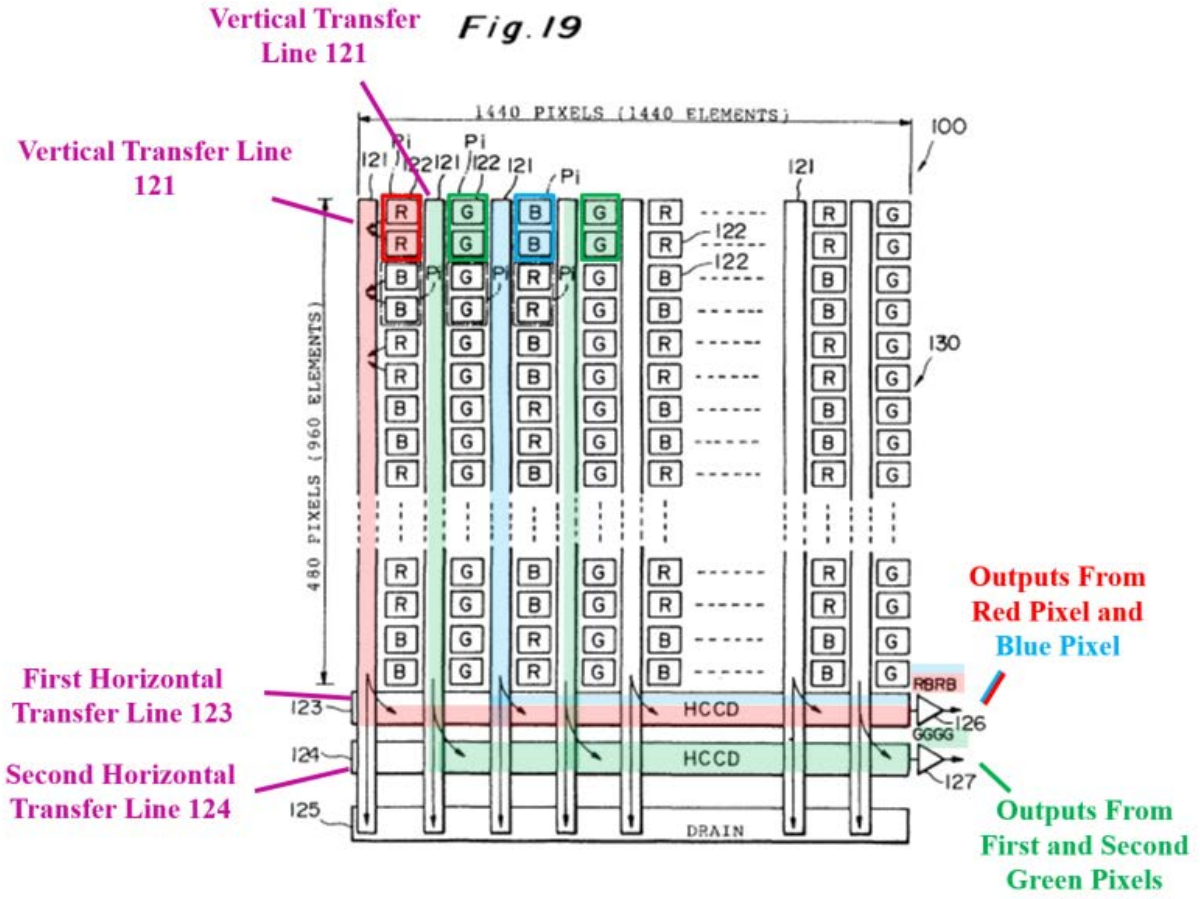
(Ex. 1006, FIG. 19 (excerpt, annotated); Ex. 1002, ¶186.)

f) Claim 1[f]

g) Claim 1[g]

Inuiya discloses these limitations. (Ex. 1002, ¶¶187-194.) As discussed above in Sections IX.D.1(b)-(e), the red pixel output is connected to the first vertical transfer line 121, and the blue pixel output is connected to the third vertical transfer line 121. Similarly, the first green pixel output is connected to the second vertical transfer line 121, and the second green pixel output is connected to the fourth vertical transfer line 121. (Ex. 1006, 20:44-53, 21:7-12, FIG. 19; *supra* Sections IX.D.1(b)-

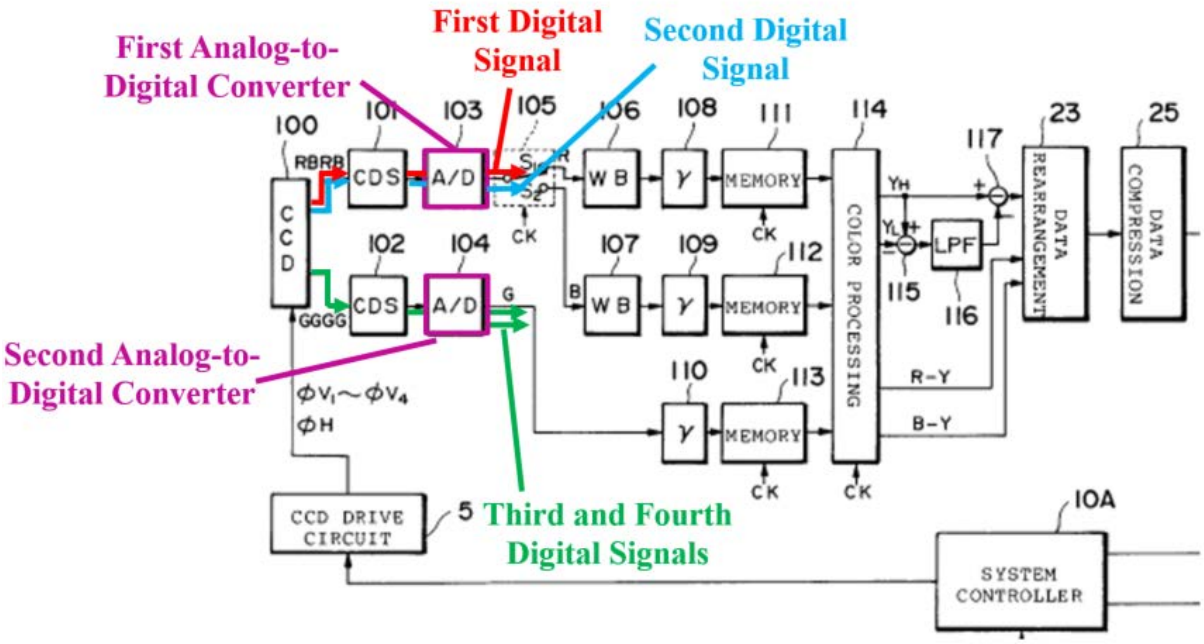
(e).) As shown in annotated figure 19 below, the first and third vertical transfer lines 121 are connected to the horizontal transfer line 123, whereas the second and fourth vertical transfer lines are connected to the horizontal transfer line 124, such that the red/blue pixel outputs are sequentially output by amplifier 126 and the first/second green pixel outputs are sequentially output by amplifier 127. (Ex. 1006, 21:36-62, 22:63-23:25; Ex. 1002, ¶¶187-189.)



(Ex. 1006, FIG. 19 (annotated); Ex. 1002, ¶189.)

As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that the output signals from the CCD 100 are provided through correlated data sampling

circuits 101, 102 to analog-to-digital converters 103, 104. (*Id*., 25:36-43; Ex. 1002, ¶190.)



(Ex. 1006, FIG. 18 (excerpt, annotated); Ex. 1002, ¶190.)

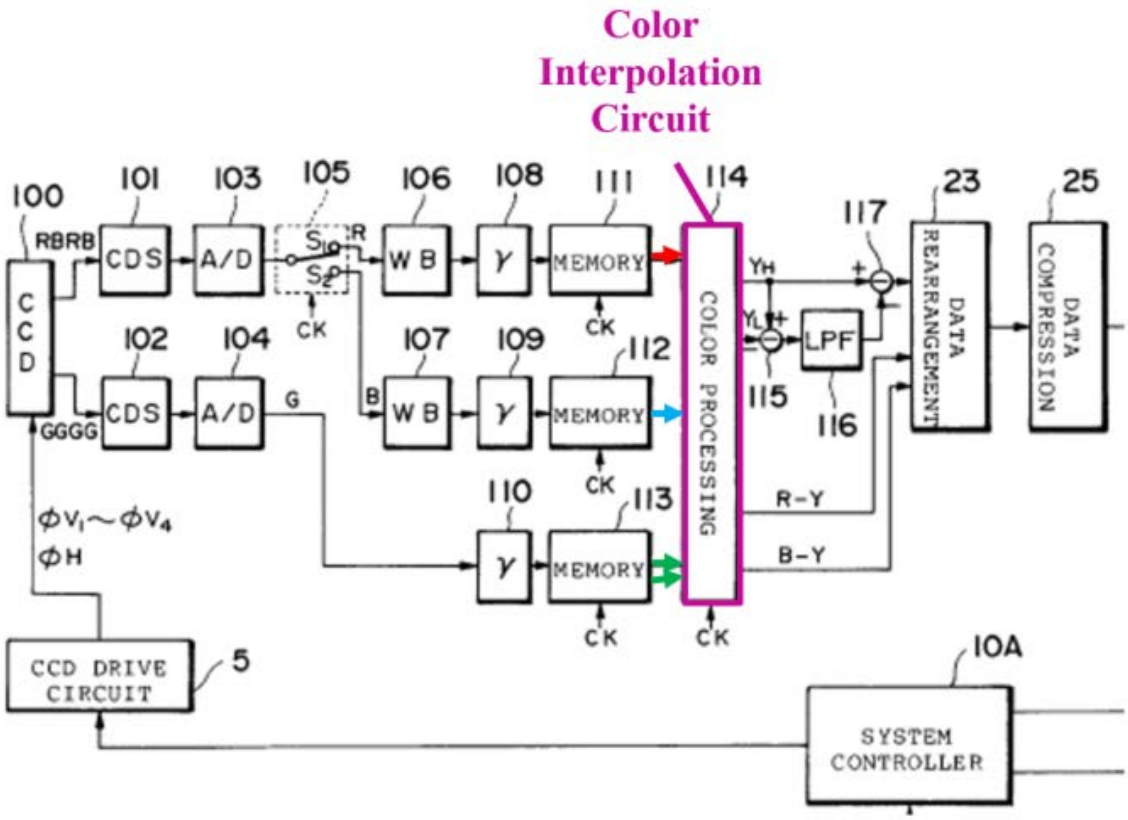
As shown in the annotated excerpt of figure 18 above, the outputs of the red and blue pixels (part of RBRB coming out of the CCD) are "outputted alternately by the first horizontal transfer line 123" and provided to the analog-to-digital converter (A/D) 103, whereas the outputs of the first and second green pixels (part of GGGG coming out of the CCD) are sequentially provided to the analog-to-digital converter (A/D) 104. (Ex. 1006, 25:36-43; Ex. 1002, ¶191.) A POSITA would have understood that the analog-to-digital converters 103 and 104 are "connected to" the outputs of the pixels as they receive and convert the analog signals from those outputs into digital image data. (Ex. 1002, ¶191.) The digital image data generated

by the analog-to-digital converter 103 includes a "first digital signal" corresponding to the red pixel output and a "second digital signal" corresponding to the blue pixel output. (*Id*., ¶192.) The red and blue pixel outputs are sequentially provided from the CCD 100 to A/D 103. The digital image data generated by the analog-to-digital converter 103 includes a "first digital signal" that is output when the red pixel is provided to A/D 103 and a "second digital signal" that is output when the blue pixel output is provided to the A/D 103. (*Id*.) Similarly, the first and second green pixel outputs are sequentially provided to A/D 103. (*Id*., ¶193.) *Inuiya* discloses the G signals are converted into a digital G data, including the "third digital signal" for the "first green pixel," the "fourth digital signal" for the "second green pixel," and other digital signals corresponding to other green pixels. (*Id*.; Ex. 1006, 25:55-59.) Therefore, the analog-to-digital converters 103 and 104 disclose first and second analog-to-digital converters, respectively, as recited in claim 1. (Ex. 1002, ¶194.)

h) Claim 1[h]

Inuiya discloses these limitations. (Ex. 1002, ¶¶195-202.) As discussed above in Sections IX.D.1(f)-(g), the analog-to-digital converters 103 and 104 convert the outputs of red, blue, first green, and second green pixels into the first, second, third, and fourth digital signals, respectively. (*Supra* sections IX.D.1(f)-(g).) *Inuiya* further discloses that these digital signals are processed by white-balance adjustment circuits 106-107 and gamma-correction circuits 108-110 before being

stored in memories 111-113. (Ex. 1006, 25:49-63, FIG. 18; Ex. 1002, ¶195.) The digital pixel data stored in the memories 111-113 is then processed by the color processing block ("color interpolation circuit"), which combines the first, second, third and fourth digital signals to produce luminance data and color difference data. (Ex. 1006, 26:5-19, 27:10-18; Ex. 1002, ¶196.)



(Ex. 1006, FIG. 18 (excerpt, annotated); Ex. 1002, ¶196.)

Inuiya discloses that generation of the luminance data includes combining the digital signals corresponding to the red, blue, and first and second green pixels. (Ex. 1006, FIGs. 27, 29; Ex. 1002, ¶197.) The red, blue, and first/second green pixels

discussed above in sections IX.D.1(b)-(g) are shown in figure 27 below. (*Supra* sections IX.D.1(b)-(g); Ex. 1006, FIG. 27.)

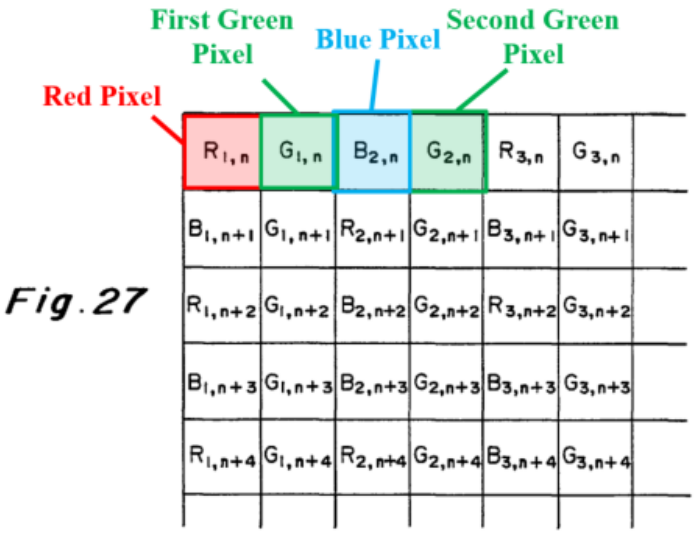
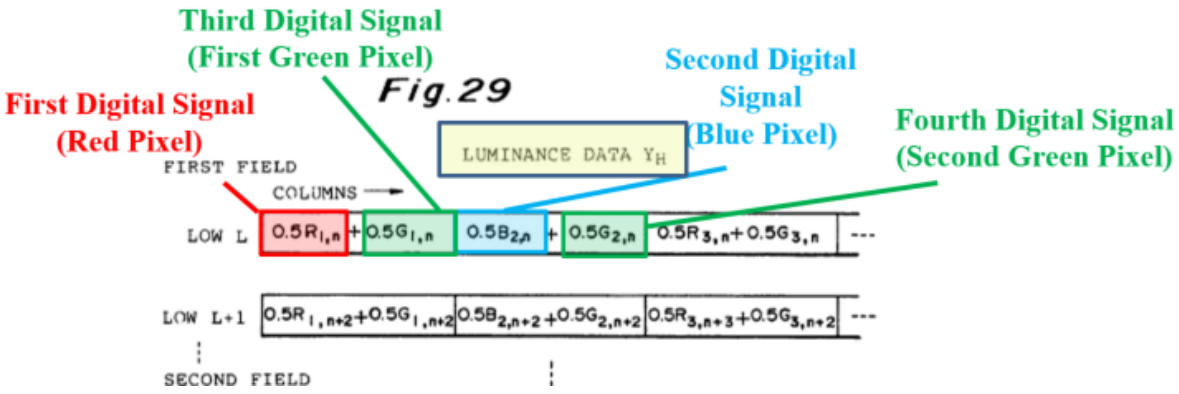


Fig. 27

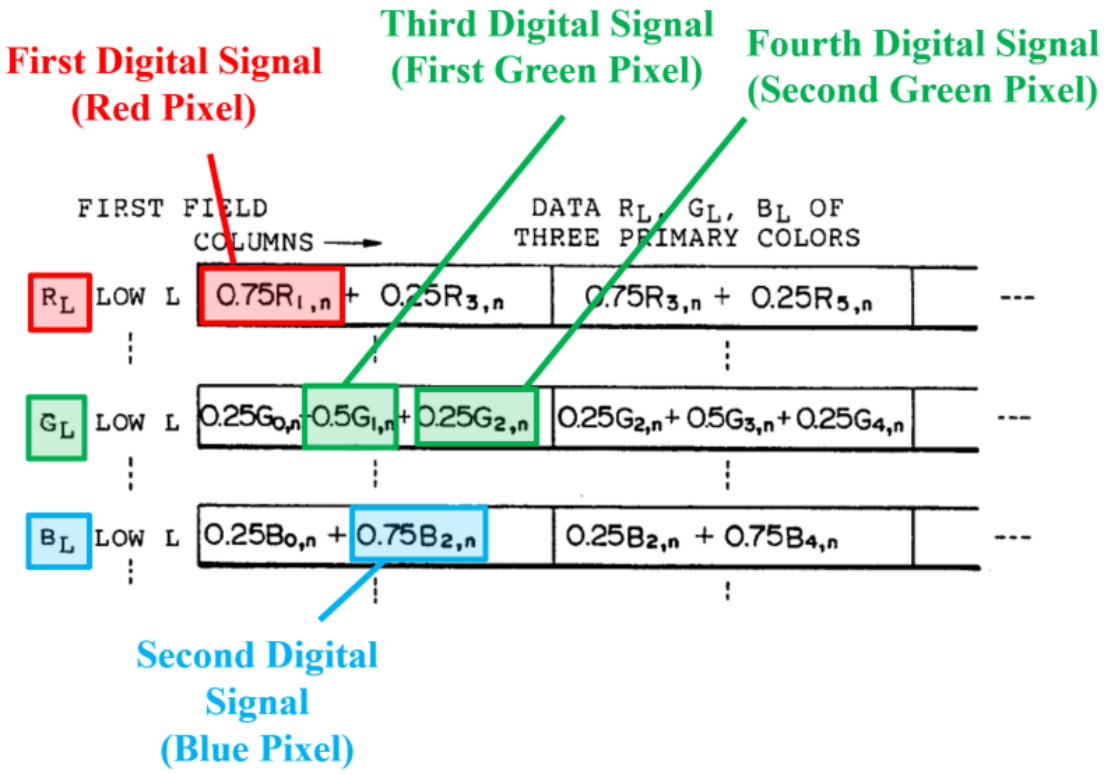
(Ex. 1006, FIG. 27 (annotated); Ex. 1002, ¶198.)

As shown in the annotated excerpt of figure 29 below, the first, second, third, and fourth digital signals are combined by the color processing circuit 114 to generate the luminance data Y_H. (Ex. 1006, FIG. 29; Ex. 1002, ¶199.)



(Ex. 1006, FIG. 29 (annotated); Ex. 1002, ¶199.)

Inuiya further discloses that the pixel outputs for the red, blue, first green, and second green pixels are combined in calculating the luminance data Y_L of the low-frequency components. (Ex. Ex. 1002, ¶200.) Figure 30 of *Inuiya* shows that the outputs for the red, blue, first green, and second green pixels are included in calculating R_L, G_L, and B_L, where, as discussed below, those values are in turn used to calculate the luminance data Y_L:



(Ex. 1006, FIG. 30 (excerpt, annotated); Ex. 1002, ¶200.)

Inuiya discloses:

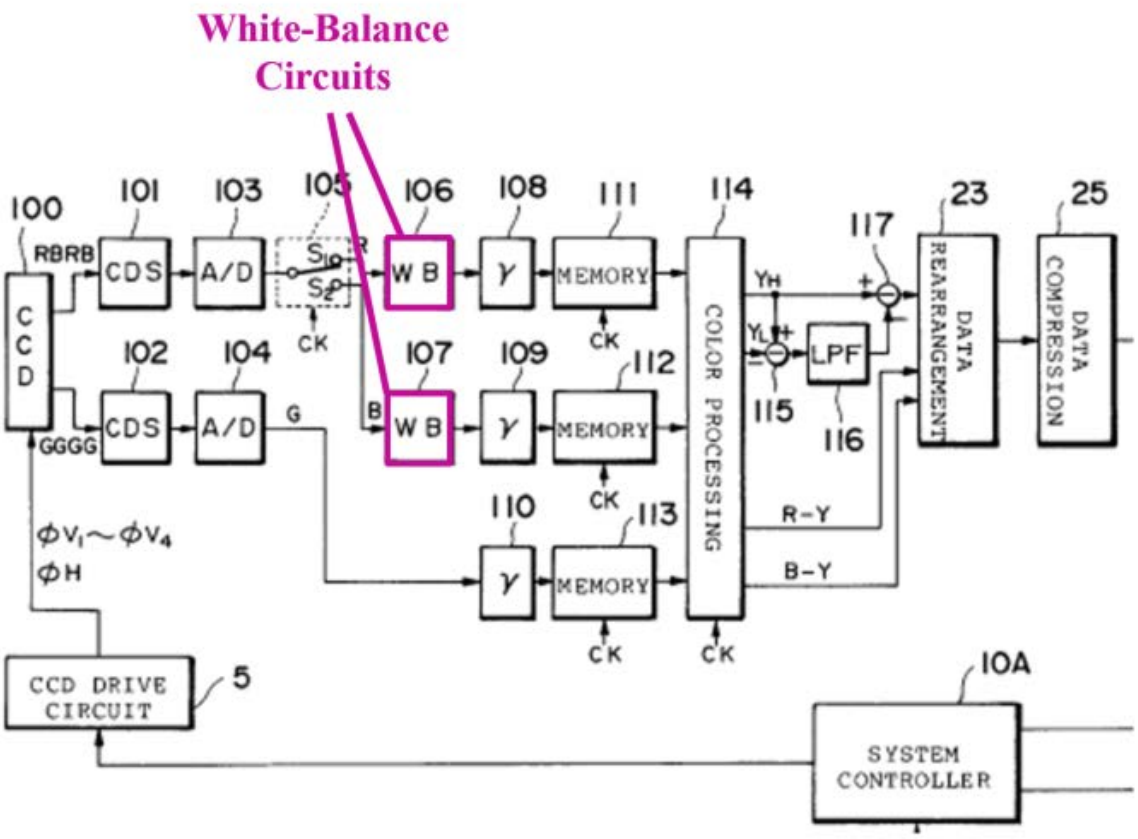
> When the R_L data, G_L data and B_L data is generated for each of the first, second, third and fourth fields, the luminance data Y_L of the low-frequency components is generated, for each of the first, second, third and fourth fields, from the R_L data, G_L data and B_L data in accordance with the following equation:
>
> $$Y_L = 0.3R_L + 0.59G_L + .11B_L \qquad \text{(Eq. (1)}$$

(Ex. 1006, 28:49-57 (equation annotated); Ex. 1002, ¶201.)

As demonstrated above, the digital signals corresponding to the red, blue, first green, and second green pixels are combined to produce both the luminance data Y_H and luminance data Y_L. (Ex. 1002, ¶202.) Therefore, the color processing block 114 constitutes a "color interpolation circuit for combining the first, second, third and fourth digital signal." (*Id*.)

2. Claim 2

Inuiya discloses these limitations. (Ex. 1002, ¶¶203-208.) As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that, after conversion to digital signals, the outputs of the red and blue pixels are provided to white balance adjustment circuits 106, 107 that apply white-balance adjustment to the red and blue pixel data. (Ex. 1006, 25:49-55; Ex. 1002, ¶205.)



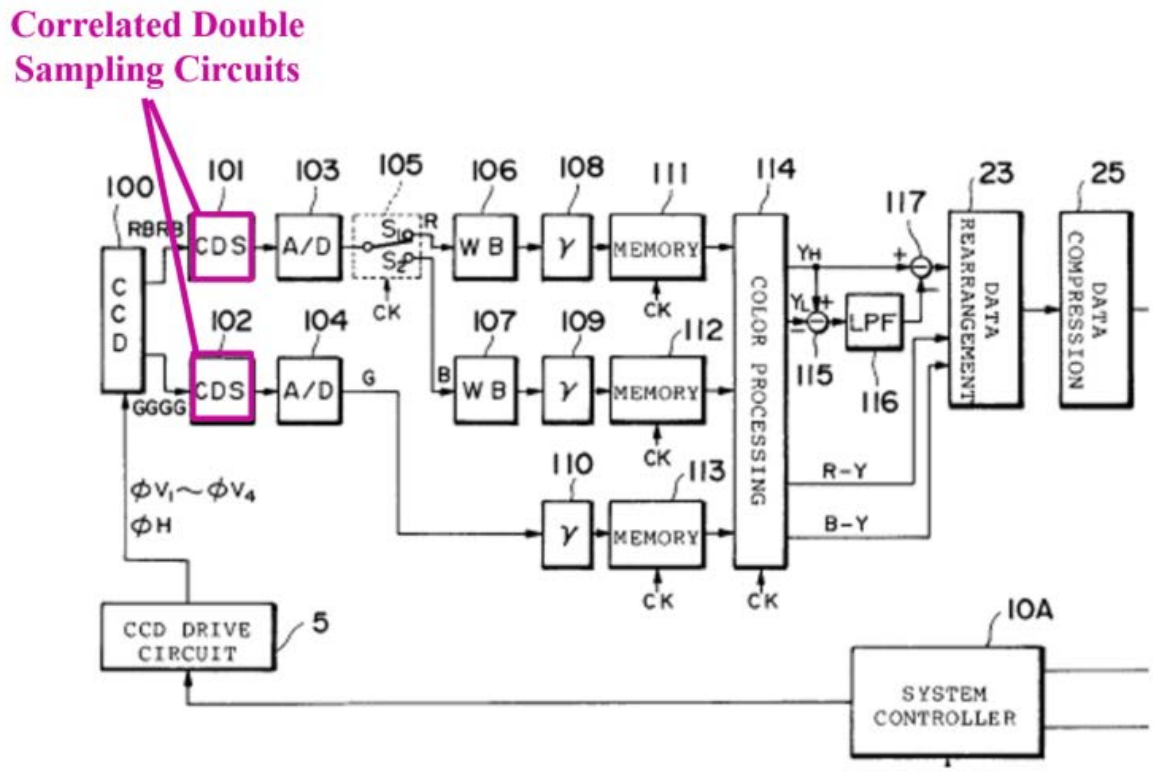
(*Id*., FIG. 18 (excerpt, annotated); Ex. 1002, ¶205.)

A POSITA would have understood that white-balance adjustment involves inserting equalizing gain for one or more of the color components to correct for sensor sensitivity variation across the radiation spectrum. (Ex. 1013, 9:60-10:3; Ex. 1010, 2094 ("To achieve white balance, it is evident from Fig. 4 that the outputs of the blue and green pixels must be amplified with respect to the outputs of the red pixels.").) Therefore, a POSITA would have understood that the white-balance circuits constitute an "error correction circuit" to correct the gain for the blue and

red pixels. (Ex. 1002, ¶¶206-207.) For at least these reasons, *Inuiya* discloses the limitations of claim 2. (*Id*., ¶208.)

3. Claim 3

Inuiya discloses these limitations. (Ex. 1002, ¶¶209-211.) As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that the outputs of pixels are provided to CDS (correlated double sampling) circuits 101-102. (Ex. 1006, 25:36-43, FIG. 18.) A POSITA would have understood that the double sampling performed by the CDS circuits 101-102 reduces fixed pattern noise ("error compensation circuit for correcting a fixed pattern noise offset") in the pixel outputs. (Ex. 1011, 7:34-38; Ex. 1012, 40:17-23; Ex. 1002, ¶210.) Therefore, *Inuiya* discloses the limitations of claim 3. (*Id*., ¶211.)



(Ex. 1006, FIG. 18 (excerpt, annotated); Ex. 1002, ¶210.)

4. Claim 18

a) Claim 18[a]

To the extent the preamble of claim 18 is limiting, *Inuiya* discloses the limitations therein. (Ex. 1002, ¶212.) As discussed above in Section IX.D.1(a), *Inuiya* discloses a solid-state image sensing element, where the operation of such an image sensing element, which includes the capture and processing of pixel data, constitutes an "imaging method." (*Id.*; *Supra* Section IX.D.1(a).)

b) Claim 18[b]

c) Claim 18[c]

Inuiya discloses these limitations. (Ex. 1002, ¶213.) As discussed above in Sections IX.D.1(b)-(c), *Inuiya* discloses a red pixel and a blue pixel, each of which has a corresponding "output." (*Supra* Sections IX.D.1(b)-(c).) As discussed above in Section IX.D.1(f), the outputs of the red and blue pixels are converted from analog signals to first and second digital signals, respectively, by a first analog to digital coverter. (*Supra* Section IX.D.1(f).)

d) Claim 18[d]

e) Claim 18[e]

Inuiya discloses these limitations. (Ex. 1002, ¶214.) As discussed above in Sections IX.D.1(d)-(e), *Inuiya* discloses a first and second green pixel, each of which has a corresponding "output." (*Supra* Sections IX.D.1(d)-(e).) As discussed above in Section IX.D.1(g), the outputs of the first and second green pixels are converted from analog signals to third and fourth digital signals, respectively, by a second analog to digital coverter. (*Supra* Section IX.D.1(g).)

f) Claim 18[f]

Inuiya discloses these limitations for the reasons discussed above in Section IX.D.1(h). (*Supra* Section IX.D.1(h); Ex. 1002, ¶215.)

5. Claims 19-20

Inuiya discloses the limitations of each of claims 19-20 for the reasons discussed above for each of claims 2-3, respectively. (*Supra* Sections IX.D.2-3; Ex. 1002, ¶¶216-217.)

E. Ground 5: Claims 4-5 and 21-22 Are Obvious Over *Inuiya* in View of *Neter*

1. Claim 4

As discussed above in Section IX.B.3, a POSITA would have understood that implementing the components of an imaging device on two chips would have been an obvious combination and/or design choice. (*Supra* section IX.B.3.) *Inuiya*, like *Isogai* and *Neter*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Neter* in Section IX.B.3, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Neter* with a reasonable expectation of success such that *Inuiya's* analog-to-digital converters are on the same chip as the pixel array, while maintaining the color processing circuitry on a second chip. (Ex. 1002, ¶218.)

2. Claim 5

As discussed above in Section IX.B.4, a POSITA would have understood that implementing the components of an imaging device on one chip would have been an obvious combination and/or design choice. (*Supra* section IX.B.4.) *Inuiya*, like

Isogai and *Neter*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Neter* in Section IX.B.4, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Neter* with a reasonable expectation of success such that *Inuiya's* analog-to-digital converters and color processing circuitry are on the same chip as the pixel array. (Ex. 1002, ¶219.)

3. Claims 21-22

The *Inuiya-Neter* combination discloses the limitations of each of claims 21 and 22 for the reasons discussed above for each of claims 4 and 5, respectively. (*Supra* Sections IX.E.1-2; Ex. 1002, ¶220.)

F. Ground 6: Claims 4-5 and 21-22 Are Obvious Over *Inuiya* in View of *Fossum*

1. Claim 4

As discussed above in Section IX.B.3, a POSITA would have understood that implementing the components of an imaging device on two chips would have been an obvious combination and/or design choice. (*Supra* section IX.B.3.) *Inuiya*, like *Isogai* and *Fossum*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Fossum* in Section IX.C.3, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Fossum* with a reasonable expectation of success such that *Inuiya's* analog-to-digital

converters are on the same chip as the pixel array, while maintaining the color processing circuitry on a second chip. (*Supra* Section IX.C.3; Ex. 1002, ¶221.)

2. Claim 5

As discussed above in Section IX.B.4, a POSITA would have understood that implementing the components of an imaging device on one chip would have been an obvious combination and/or design choice. (*Supra* section IX.B.3.) *Inuiya*, like *Isogai* and *Fossum*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Fossum* in Section IX.C.4, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Fossum* with a reasonable expectation of success such that *Inuiya's* analog-to-digital converters and color processing circuitry are on the same chip as the pixel array. (Ex. 1002, ¶222.)

3. Claims 21-22

The *Inuiya-Fossum* combination discloses the limitations of each of claims 21 and 22 for the reasons discussed above for each of claims 4 and 5, respectively. (*Supra* Sections IX.F.1-2; Ex. 1002, ¶223.)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE HERE

The '651 patent will expire on March 28, 2022, which is before the April 1, 2022 target competition date of the co-pending ITC Investigation. (Ex. 1021, 2.) As

a result, the ITC cannot issue a remedy as to the '651 patent, thus making it likely it will be terminated prior to trial. *See Certain Color Intraoral Scanners and Related Hardware and Software*, Inv. No. 337-TA-1091, Initial Determination (Mar. 1, 2019). Therefore, the Board's decision in *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (Sept. 12, 2018) (precedential), is irrelevant here.

But, even if considered, institution is proper under *NHK*, because an evaluation of the six factors under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential), favor institution. As discussed below, while the '651 patent is currently involved in an ITC investigation, Petitioner diligently filed this Petition less than two months after institution of the ITC investigation, four of the ten challenged claims are not asserted in the ITC investigation, the ITC involves different evidentiary standards and burdens, and—most importantly—the ITC cannot invalidate a patent.[6] Accordingly, the Board should institute IPR based on the Petition, which presents strong arguments for unpatentability.

[6] Whether *NHK Spring* and *Fintiv* should apply to an ITC investigation was recently raised in a request for rehearing by the Board and the Precedential Opinion Panel in *Garmin Int'l, Inc. v. Koninklijke Philips N.V.*, IPR2020-00754, Paper 12 (Nov. 19, 2020).

The **first factor (stay)** is neutral, because the ITC favors suspension of remedial orders that conflict with an IPR decision (e.g., issued near the end of an ITC investigation) over staying investigations at the onset. *See In the Matter of Certain Unmanned Aerial Vehicles and Components Thereof*, ITC-337-TA-1133, 2020 WL 5407477, at *1, *20-*22 (ITC Sept. 8, 2020).

The **second factor (proximity of trial)** is neutral, if not slightly for granting institution, because of Petitioner's diligence in filing the Petition. First, Petitioner filed its Petition ***less than two months*** after institution of the ITC investigation.[7] (Ex. 1018, 2.)

Second, the Board's institution decision will likely issue around July 2021, which is before the ITC's initial determination set for December 1, 2021 (Ex. 1023, 3). And, while the investigation hearing is set for August 16-20, 2021 (Ex. 1022, 1; Ex. 1023, 4) and the target completion date is set for April 1, 2022 (Ex. 1021, 2), those dates are "subject to change because of restrictions and uncertainty due to the COVID-19 pandemic" (*id.*, 2; Ex. 1022, 2). Indeed, the ITC has recently delayed a significant number of investigations in which a violation was found. (*See, e.g.*, Ex. 1024.)

[7] PO amended its complaint on October 23, 2020, and further supplemented it in November 2020. (Ex. 1018.)

Third, the hearing before the ALJ is merely the initial step in the ITC's decisional process. *See* 19 C.F.R. § 210.36(a). The ALJ's initial determination is subject to a review by the full Commission, which must issue a final determination. *Id.* §§ 210.43(d), 210.45-46. Additionally, if the Commission finds a violation, it must "transmit" a copy of its final determination and recommended actions (together with the full record) to the President, *see* 19 U.S.C. § 1337(j)(1)(B), and only upon the President's approval or the expiration of the 60-day presidential review period would the ITC's final determination become final (and subject to appeal), *see id.* § 1337(j)(4). Thus, even though the target completion date in the ITC Investigation is set to predate the Board's final written decision, the ultimate completion of the investigation will occur closer to and possibly after the Board's final written decision (per typical Commission extensions).

The **third factor (investment)** weighs in favor of institution. To date, the ITC investigation is in its infancy and thus the Commission and parties have not yet invested substantial resources. (Ex. 1023, 2; Ex. 1017.) While activity in the investigation will subsequently increase at a pace typical of ITC actions, Samsung's diligence in filing this Petition—***less than two months after investigation institution***—weighs against discretionary denial. (Ex. 1018, 2.) *See Philip Morris Prods., S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00919, Paper 9 at 10 (Nov. 16, 2020); *Fintiv*, Paper 11 at 11. Concluding otherwise would mean that this factor

would always weigh against institution when there is a parallel ITC investigation because such investigations always require a rapid investment of resources at the outset.

The **fourth factor (overlap)** weighs strongly in favor of institution. Only claims 1-12 and 18 of the '651 patent remain at issue in the ITC investigation (Ex. 1017; Ex. 1018, 2.), so resolution of the investigation will not resolve the parties' dispute concerning patentability of the ***four*** other claims challenged in the Petition. *See Samsung Elecs. Co. Ltd. v. Dynamics Inc.*, IPR2020-00505, Paper 11 at 13 (Aug. 12, 2020).

Moreover, the ITC investigation does "not render [this] proceeding duplicative or … a waste of the Board's resources," because the ITC involves "differen[t] … evidentiary standards and burdens" and "does not have the authority to invalidate a patent." *Samsung Elecs. Co., Ltd. v. BitMicro, LLC*, IPR2018-01410, Paper 14 at 18 (Jan. 23, 2019); *see also Bio-Tech. Gen. Corp. v. Genentech, Inc.*, 80 F.3d 1553, 1564 (Fed. Cir. 1996) (The ITC cannot "set aside a patent as being invalid [and/or] render it unenforceable."). Indeed, even if the ITC finds any of the challenged claims invalid, PO can still assert those claims in district court. *See Renesas Elecs. Corp. v. Broadcom Corp.*, IPR2019-01040, Paper 9 at 7-8 (Nov. 13, 2019). That PO's predecessor unsuccessfully sued Samsung on invalid patents in the recent past strongly suggests it may do so again here. *See Imperium IP Holdings*

(Cayman) Ltd. v. Samsung Electronics Co., Ltd., 757 Fed. Appx. 974, 980 (Fed. Cir. 2019).

The **sixth factor (other circumstances)** likewise weighs strongly in favor institution. As demonstrated above (*supra* Section IX), the Petition presents strong arguments for unpatentability of the challenged claims. *See Dynamics*, Paper 11 at 14 (finding the "merits of the case weigh in favor" of institution). Thus, institution is consistent with the significant public interest against "leaving bad patents enforceable." *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020). Indeed, this Petition is the ***sole*** challenge to the '651 patent before the Board—a "crucial fact" favoring institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (May 12, 2020). And there is currently no district court litigation to serve as an alternative forum that can issue a binding decision on the validity of the '651 patent.

Accordingly, based on a "holistic view of whether efficiency and integrity of the system are best served," the facts here weigh against exercising discretion under § 314(a) to deny institution. *Dynamics*, Paper No. 11 at 15. While factor 5 (parties) usually weighs against institution, the remaining factors are at least neutral (factors 1 and 2) or favor institution (factors 3, 4, and 6). Plus, the fact that this proceeding is not duplicative or a waste of the Board's resources (factor 4) and the strength of Petitioner's unpatentability positions (factor 6) outweigh other applicable factors,

such as if the ITC investigation concludes before the final written decision is issued in this proceeding (factor 2) or if there were great investment in the ITC investigation (factor 3)—which typically occur when there is a parallel ITC investigation. *See 3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12 at 33-34 (May 26, 2020). Thus, institution here is proper.

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-5 and 19-22 of the ’651 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: January 15, 2021 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,838,651 contains, as measured by the word-processing system used to prepare this paper, 13,856 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: January 15, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on January 15, 2021, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,838,651 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO CA 92691

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)