

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PICTOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 7,323,671

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,323,671**

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Ex. 1008	U.S. Patent No. 6,403,998 to Inoue (“ <i>Inoue</i> ”)
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Ex. 1011	D. Neamen, <i>Semiconductor Physics and Devices – Basic Principles</i> , 3 rd Ed. (2003) (“ <i>Neamen</i> ”)
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I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner” or “Samsung”) requests *inter partes* review of claims 1-26 (“the challenged claims”) of U.S. Patent No. 7,323,671 (“the ’671 patent”) (Ex. 1001), which, according to PTO records, is assigned to Pictos Technologies Inc. (“Patent Owner” or “PO”). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: The ’671 patent is at issue in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission (“the ITC Investigation”).

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), (3) Phillip Citroën (Reg. No. 66,541) (4) Anderson To (*pro hac vice* admission to be requested). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705,

email: PH-Samsung-Pictos-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '671 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-26 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1, 6-8, and 11-13 are unpatentable under pre-AIA 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,688,371 (“*Koizumi*”) (Ex. 1005);

Ground 2: Claims 5, 14, 18-21 and 24-26 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious in view of *Koizumi*;

Ground 3: Claims 2 and 15 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Koizumi* and Japanese Patent Publication No. 2002231889A (“*Yoshimitsu*”) (Ex. 1006);

Ground 4: Claims 3, 6, 16, and 19 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Koizumi* and U.S. Patent No. 6,600,471 (“*Lee*”) (Ex. 1007);

Ground 5: Claims 9 and 22 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Koizumi* and U.S. Patent No. 6,403,998 (“*Inoue*”) (Ex. 1008);

Ground 6: Claims 10 and 23 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Koizumi* and U.S. Patent No. 6,246,043 (“*Merrill*”) (Ex. 1009);

Ground 7: Claims 1, 4, 11 and 12 are unpatentable under pre-AIA 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,110,030 (“*Kochi*”) (Ex. 1010);
and

Ground 8: Claims 14, 17, 24, and 25 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious in view of *Kochi*.

The '671 patent issued January 29, 2008, from U.S. App. No. 11/029,103 filed December 30, 2004. *Yoshimitsu* published August 16, 2002. *Lee* issued July 29, 2003, from U.S. App. No. 09/916,822 filed July 27, 2001. *Inoue* issued June 11, 2002, from U.S. App. No. 09/435,464 filed November 8, 1999. *Merril* issued June 12, 2001, from U.S. App. No. 09/158,758 filed September 22, 1998. Thus, *Yoshimitsu*, *Lee*, *Inoue*, and *Merril* qualify as prior art at least under pre-AIA 35

U.S.C. § 102(b). *Koizumi* issued March 30, 2010, from U.S. App. No. 09/929,037 filed August 15, 2001. *Kochi* issued September 19, 2006, from U.S. App. No. 09/264,719 filed March 9, 1999. Thus, *Koizumi* and *Kochi* qualify as prior art at least under pre-AIA 35 U.S.C. § 102(e). None of these references were considered during prosecution. (*See generally* Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

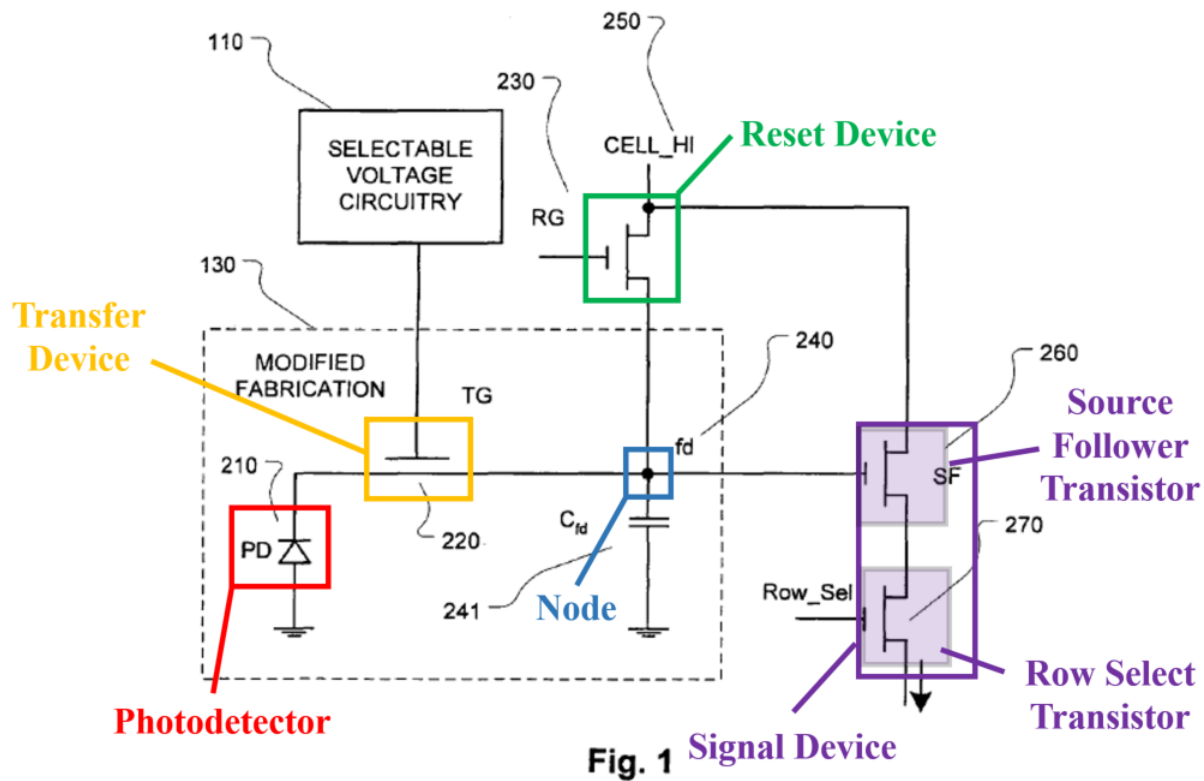
A person of ordinary skill in the art as of the claimed priority date of the '671 patent ("POSITA") would have had a bachelor's degree in a field relating to semiconductor design and manufacturing like physics, electrical engineering, or other related subjects, and two to three years of experience in the design and fabrication of semiconductor devices such as image sensors. More education can supplement practical experience and vice versa. (Ex. 1002, ¶¶20-21.)¹

VII. THE '671 PATENT

The '671 patent relates to an "image sensor integrated circuit" that "includes photodetectors such as photodiodes, nodes such as floating diffusions, and transfer devices such as transfer gates that control a transfer of electrons between a photodetector and a corresponding floating diffusion." (Ex. 1001, 2:13-17.) "The

¹ Petitioner submits the declaration of Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '671 patent. (Ex. 1002, ¶¶1-19; Ex. 1003.)

circuit also includes reset devices such as reset transistors” where “[e]ach floating diffusion node has a corresponding reset device which resets the node.” (*Id.*, 2:17-20.) The circuit also includes row and column circuitry as well as “signal devices such as source follower and row selector transistors.” (*Id.*, 2:20-23.) All of these features, which are highlighted in annotated figure 1 of the ’671 patent below were well-known, standard components of a four-transistor pixel cell that was widely used throughout the industry. (Ex. 1002, ¶¶28-34.)



(Ex. 1001, FIG. 1 (annotated); Ex. 1002, ¶34.)

In addition to these well-known aspects of a widely used 4T pixel cell, the ’671 patent includes selectable voltage circuitry 110 (shown in figure 1 above) that

provides the gate voltage to the transfer device. The “variable voltage circuitry” recited in claim 1 was the only feature identified as new by the Examiner during prosecution. (See Ex. 1004, 151, 177 (Examiner’s Statement of Allowance indicating that the prior art did not disclose or suggest “a voltage selector determining a control voltage of the control signal applied to the plurality of transfer devices”) Notably, during prosecution there were no prior art rejections, and, after a restriction requirement (*id.*, 128-32), the elected pending claims were allowed in the first substantive office action (*id.*, 148).

But, as explained below, all of the features recited in the challenged claims were already known and disclosed in the prior art. (See Ex. 1002, ¶¶35-36, 51-213; ¶¶23-33 (describing the state of the art and citing Exs. 1005, 1007-1008, 1010.) Indeed, with respect to independent claim 1, the “voltage selector” feature that the Examiner relied on in allowing the claims is plainly disclosed in multiple prior art references that also disclose the other limitations recited in the independent claims.

VIII. CLAIM CONSTRUCTION

During IPR, claims are construed according to the “*Phillips* standard,” as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). See 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015). For purposes of

this proceeding, Petitioner believes that no special constructions are necessary for any claim terms to assess whether the challenged claims are unpatentable over the asserted prior art.² (Ex. 1002, ¶37.)

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: Claims 1, 6-8, and 11-13 are Anticipated by *Koizumi*

1. Claim 1

a) An image sensor integrated circuit, comprising:

To the extent the preamble is limiting, *Koizumi* discloses the limitations therein. (Ex. 1002, ¶¶38-42, 51-58.) For instance, *Koizumi* discloses “an image pickup device comprising a plurality of pixels” (Ex. 1005, Abstract) where the “sensor and signal processing can be **formed on one chip**”³ (*id.*, 1:14-18). *Koizumi*’s image pickup apparatus is an “image sensor integrated circuit” as recited in claim 1. (*Id.*, 1:10-25; 4:52-61, 9:22-36, FIGs. 6-7; *infra* Sections IX.A.1(b)-(h).)

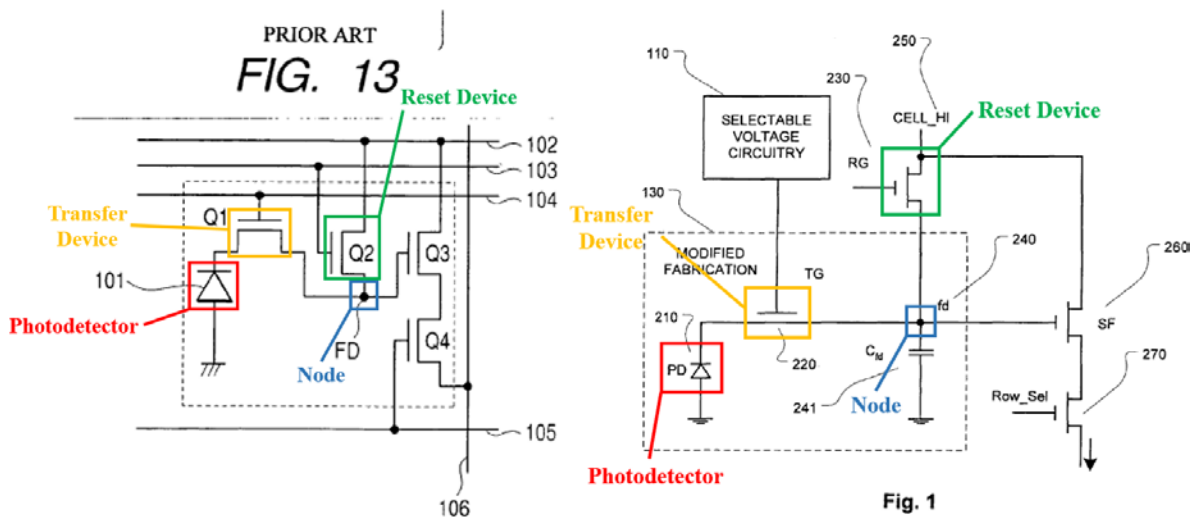
Koizumi further discloses that each pixel in the pixel array of the image pickup device includes “a photodiode, MOS switch, [and] amplification circuit.” (*Id.*, 1:14-16) As shown in annotated Figure 13 below, a pixel in *Koizumi*’s image pickup

² Petitioner reserves all rights to raise claim construction and other arguments in this and other proceedings as relevant and necessary.

³ Emphasis added unless otherwise specified.

device (“image sensor integrated circuit”) includes: “a transfer switch Q1 [to] transfer[] photocharges from a photodiode 101 to a floating diffusion area (FD)”;

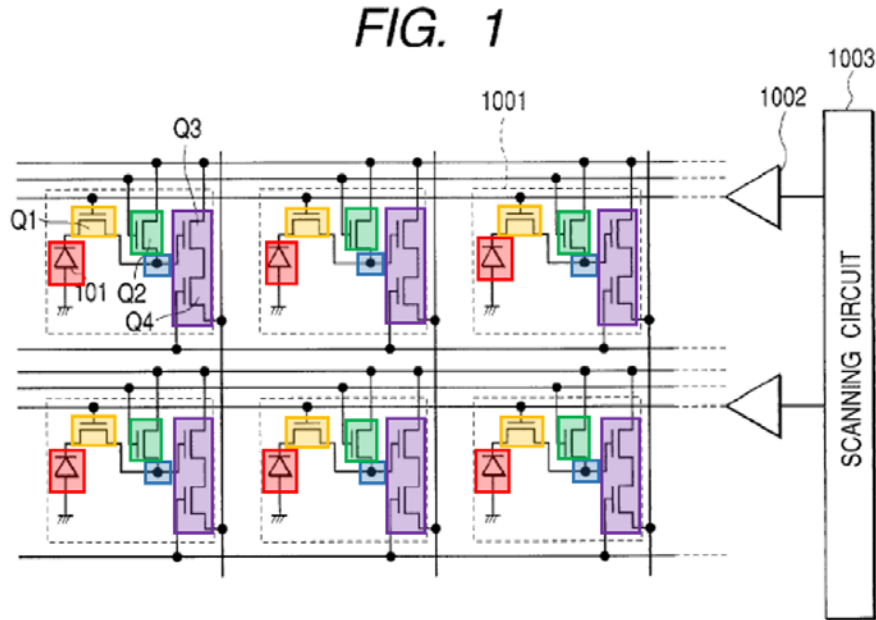
“[a] reset switch Q2 [to] reset[] the floating diffusion area”; “[a]n input MOS transistor Q3...included in a source follower for outputting the voltage in the floating diffusion area”; and “[a] selection switch Q4 [to] select[] a pixel.” (*Id.*, 1:26-32, 5:65-66.) A POSITA would have recognized that *Koizumi*’s pixel shown in figure 13 has a substantially similar circuit topology to the pixel depicted in figure 1 of the ’671 patent. (Ex. 1001, 4:6-20; Ex. 1002, ¶¶52-55.)



(Compare Ex. 1005, FIG. 13 (left, annotated), with Ex. 1001, Fig 1 (right, annotated); Ex. 1002, ¶55.)

Figure 1 of *Koizumi* depicts a portion of the image pickup device and “is a circuit diagram schematically showing the periphery of the drive circuit of a transfer

switch when a plurality of pixels shown in figure [13]⁴ are arrayed.” (Ex. 1005, 6:50-59 (“pixel 1001...has the same structure as that shown in FIG. 13”); *see also id.*, 3:56-4:15.)



(*Id.*, FIG. 1 (annotated); Ex. 1002, ¶56.)

As shown above, *Koizumi*’s image pickup apparatus includes a “gate drive circuit 1002 for operating a transfer switch Q1..., and scanning circuit 1003 for controlling the transfer switches on each row basis.” (Ex. 1005, 6:54-59.) *Koizumi* discloses a number of different embodiments of gate drive circuits used to provide

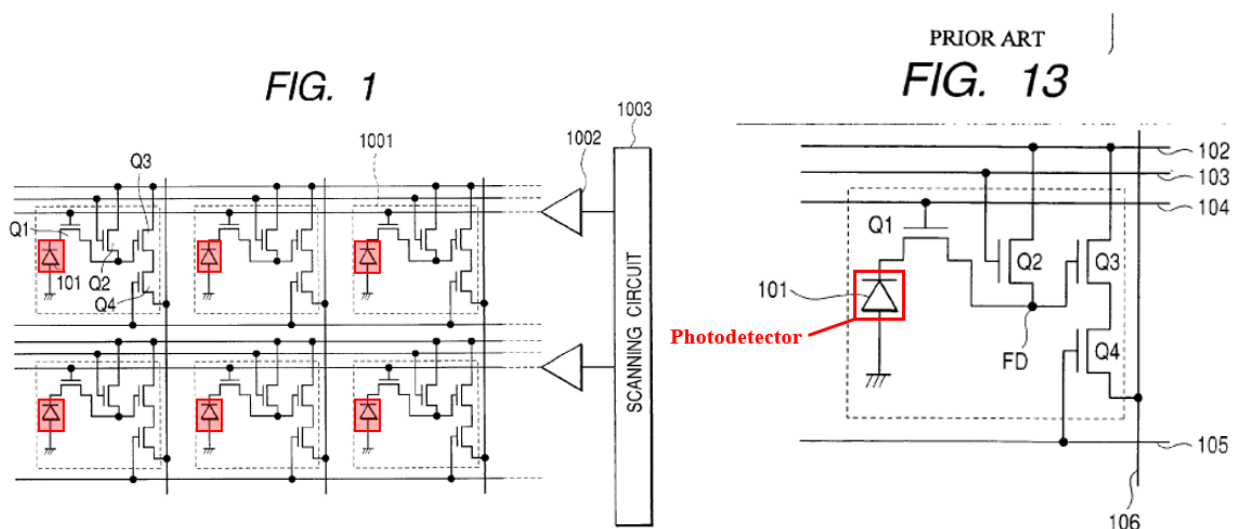
⁴ A POSITA would have understood that *Koizumi* includes a typographical error indicating that figure 12 rather than figure 13 shows the pixel structure. (Ex. 1002, 33 n.2.)

the control voltage to the transfer device Q1 shown above in annotated figure 13 and figure 1. (*Id.*, 5:44-51, FIGs. 2-5; Ex. 1002, ¶¶57-58.)

As discussed above and explained in more detail below, each of the plurality of pixels 1001 includes a photodiode 101 (“photodetector”), corresponding floating diffusion area FD (“node”), transfer switch Q1 (“transfer device”), reset switch Q2 (“reset device”), input MOS transistor Q3, and selection switch Q4 (Q3 and Q4 together form a “signal device”). (*See infra* Sections IX.A.1(b)-(h).)

b) a plurality of photodetectors generating electrons excited by incident photons;

Koizumi discloses this limitation. (Ex. 1002, ¶¶59-61.) For instance, as shown in annotated figures 1 and 13 below, each of the plurality of pixels in *Koizumi*’s image pickup apparatus includes a photodiode 101 (Ex. 1005, 1:26-35, 6:52-56, FIGs. 1, 13), which is a “photodetector” as claimed (Ex. 1001, 2:13-14).

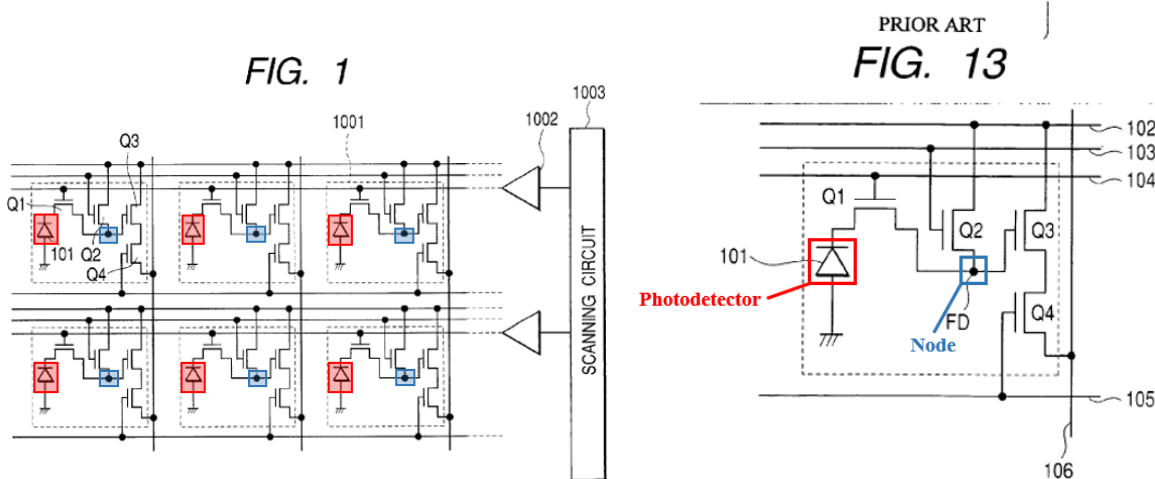


(Ex. 1005, FIGs. 1, 13 (annotated); Ex. 1002, ¶59.) Therefore, *Koizumi*'s image pickup apparatus includes a plurality of pixels, each including a photodiode (“a plurality of photodetectors”). (Ex. 1005, 6:52-54; Ex. 1002, ¶¶59-60.)

It was well known in the art that a photodiode generates electrons when photons of sufficient energy strike (“excite”) the photodiode. (Ex. 1002, ¶61.) Indeed, *Koizumi* explains that “transfer switch Q1 transfers **photocharges** from a photodiode 101 to a floating diffusion area (FD).” (Ex. 1005, 1:27-28.) The understanding that *Koizumi*'s photodiodes generate electrons excited by incident photons is consistent with the disclosure of the '671 patent. (See, e.g., Ex. 1001, claim 12 (“the plurality of photodetectors is a plurality of photodiodes”).)

c) a plurality of nodes, wherein each of the plurality of photodetectors has a corresponding node of the plurality of nodes;

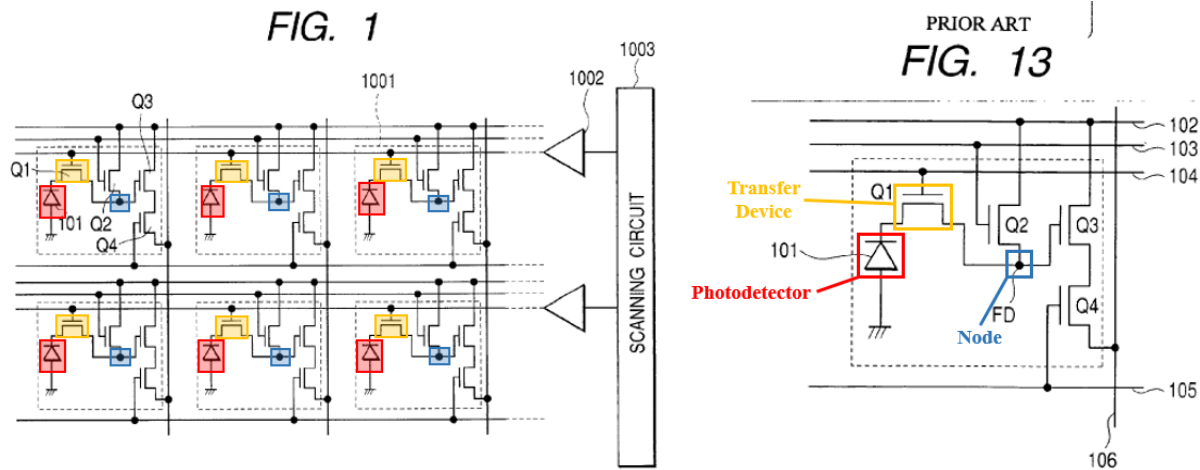
Koizumi discloses this limitation. (Ex. 1002, ¶¶62-63.) As discussed in Section IX.A.1(b) above, each pixel in *Koizumi*'s pixel array includes a photodiode 101 (“photodetector”). (Ex. 1005, 1:25-28, FIG. 13.) As shown in annotated figures 1 and 13 below, each photodiode 101 in *Koizumi*'s pixel array has a corresponding floating diffusion area FD (“plurality of nodes). (*Id.*, 1:26-35, 6:52-56, FIGs. 1, 13; Ex. 1001, 2:19, 7:60, 12:17, ('671 patent referring to “floating diffusion” as a “floating diffusion **node**”).)



(Ex. 1005, FIGs. 1, 13 (annotated); Ex. 1002, ¶¶62.) Because photocharges from each photodiode 101 are transferred to the floating diffusion area FD (Ex. 1005, 1:26-27; 1:51-52; *see infra* Section IX.A.1(d)), each floating diffusion area FD corresponds to the photodiode 101 of its respective pixel. (Ex. 1002, ¶¶62-63.)

- d) a plurality of transfer devices controlling a transfer of the electrons from said each of the plurality of photodetectors to the corresponding node, the transfer depending on a control signal applied to the plurality of transfer devices;

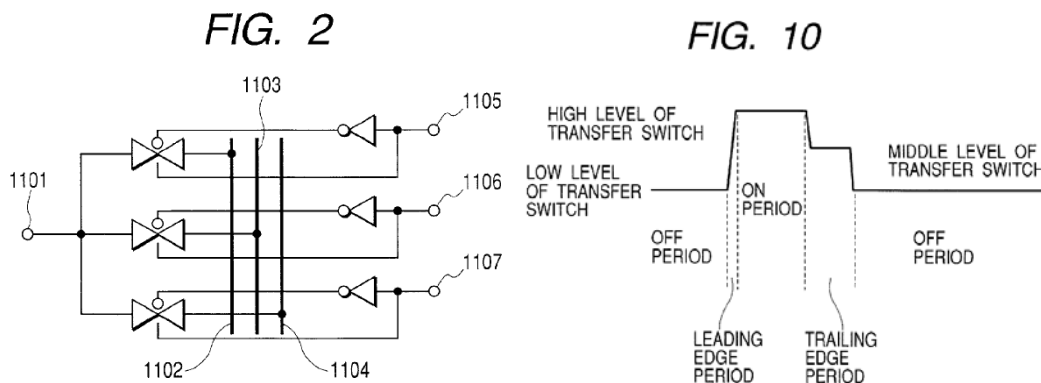
Koizumi discloses this limitation. (Ex. 1002, ¶¶64-69.) As shown in annotated figures 1 and 13 below, each pixel in *Koizumi*'s pixel array includes a transfer switch Q1, which is a "transfer device," as claimed. (Ex. 1005, 1:26-35, 6:52-56, FIGs. 1, 13.)



(Ex. 1005, FIGs. 1, 13 (annotated); Ex. 1002, ¶64.)

Koizumi discloses that the transfer switch Q1 (“transfer device”) shown above in figures 1 and 13 controls the transfer of photo-signal charges (“electrons”) from photodiode 101 to floating diffusion area FD (“node”) depending on the signal applied to control line 104 (“control signal applied to the...transfer device[]”). (Ex. 1005, 1:26-28.) As *Koizumi* explains, “to transfer the photo-signal charges to the floating diffusion area (FD), the transfer switch is turned on and off.” (*Id.*, 1:40-65.)

In the figure 2 embodiment, the state of transfer switch Q1 depends on the signal applied thereto by output terminal 1101 of the gate drive circuit (“control signal applied to the plurality of transfer devices”), which “is connected to the gate of the transfer switch Q1.” (*Id.*, 7:1-7.)



(*Id.*, FIGs. 2, 10.)

For the gate drive circuit shown in figure 2, *Koizumi* discloses that a high-level signal, a middle-level signal, and a low-level signal may be applied to the gate of transfer switch Q1. (*Id.*, 7:1-7.) “More specifically, the high level of the transfer switch is set to 5.0V, the middle level to 3.0V, and the low level to 0.0 V.” (*Id.*, 7:8-10.) As explained in connection with Figure 10, transfer switch Q1 is in an OFF state when the low-level signal (0.0V) is applied, and transfer switch Q1 is in an ON state when the high-level signal (5.0V) is applied. (*Id.*, 6:60-61 (“In this embodiment, a waveform shown in FIG. 10 is formed using a gate drive circuit shown in FIG. 2.”), FIGs. 2, 10; Ex. 1002, ¶¶65-68.)

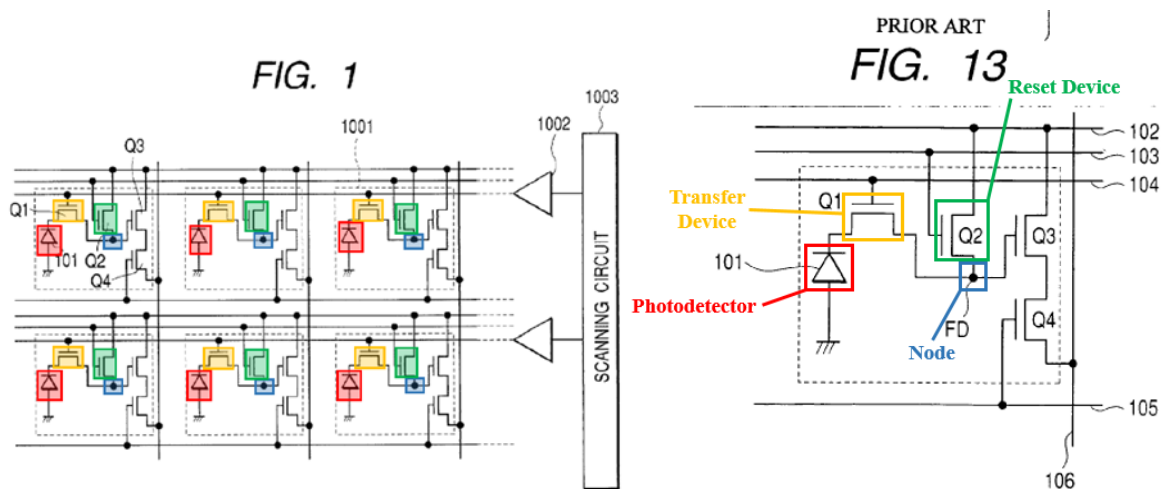
Koizumi further teaches applying the mid-level signal (3.0V) for 0.5 μ sec following the ON period before turning transfer switch Q1 OFF (by applying a low-level signal). (Ex. 1005, 7:8-10, FIG. 10 (showing the transfer switch at the middle level during the “trailing edge period”).) According to *Koizumi*, doing so

beneficially reduces the residual image and suppresses random noises. (*Id.*, 7:10-15; Ex. 1002, ¶68.)

Therefore, *Koizumi* discloses this limitation. (Ex. 1002, ¶69.)

- e) a plurality of reset devices, wherein each of the plurality of nodes has a corresponding reset device of the plurality of reset devices, and said each of the plurality of nodes is reset when the corresponding reset device is active;

Koizumi discloses this limitation. (Ex. 1002, ¶¶70-72.) As shown in annotated figures 1 and 13 below, each pixel in *Koizumi*'s pixel array includes a reset switch Q2 ("plurality of reset devices"). (Ex. 1005, 1:26-35, 6:52-56, FIGs. 1, 13.)



(Ex. 1005, FIGs. 1, 13 (annotated); Ex. 1002, ¶70.)

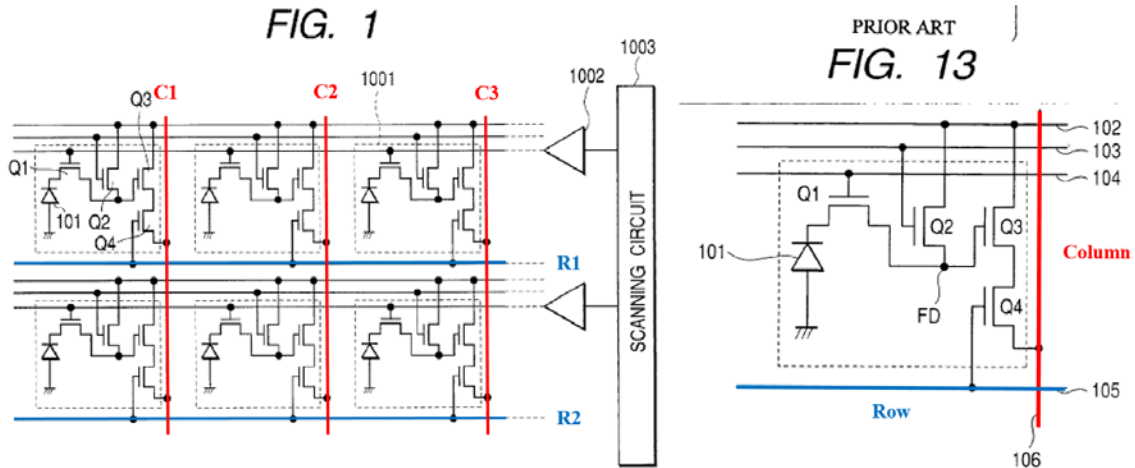
Each "reset switch Q2 resets the [corresponding] floating diffusion area [FD]." (Ex. 1005, 1:28-29.) As shown in annotated figures 1 and 13 above, the gate and source of reset switch Q2 are connected to reset switch control line 103 and

power supply line 102, respectively. (*Id.*, 1:26-39.) A POSITA would have recognized that reset switch Q2 is turned on and off based on the signal applied to the gate of Q2 via reset switch control line 103. (Ex. 1002, ¶¶71-72.) A POSITA further would have recognized that, when reset switch Q2 is in the ON state (“active”), the voltage of the floating diffusion area FD (“node”) is set to a reset voltage V_{res} (“reset”). (*Id.*, ¶72; *see* Ex. 1005, 1:28-29 (“[a] reset switch Q2 resets the floating diffusion area.”), 1:41-55.)

f) row and column circuitry;

Koizumi discloses this limitation. (Ex. 1002, ¶¶73-75.) As shown in annotated figures 1 and 13 below, each pixel of *Koizumi*’s pixel array connects to a selection switch control line 105 used to select a row in the pixel array, and also connects to a signal output line 106 corresponding to the pixel’s column. (Ex. 1005, 1:31-39, 6:54-59, 8:5-6, FIGs. 1, 13.) A POSITA would have understood that additional circuitry in *Koizumi*’s image pickup device performs the row selection that drives the selection switch control line and controls the output of the pixel data provided on the column lines. (Ex. 1002, ¶74.) Such circuitry for accessing the rows and columns of pixels was well-known and widely used. (*Id.*; Ex. 1013, 9:41-60 (“The pixels in each row can be turned on simultaneously by a row select line and the pixels in each column can be selectively output by a column select line using a combination of row and column circuitry, including, e.g., row driver 210, row

address decoder 220, control circuit 250, column driver 260, and column address decoder 270.”); Ex. 1010, 5:66-6:9, 6:21-33 (using a vertical shift register to access different rows).)⁵



(*Id.*, FIGs. 1, 13 (annotated); Ex. 1002, ¶74.)

As *Koizumi* explains, a “selection switch control line 105 for controlling the selection switch Q4 is commonly arranged in the row direction so as to select a row and transfer charges of one row to a line memory at a time.” (Ex. 1005, 1:36-39.) Thus, as shown in annotated figure 1 above and explained in more detail in Section IX.A.1(g) below, a row of pixels is selected by asserting a corresponding selection switch control line 105 (e.g., row R1 or R2 in annotated figure 1 above). Selecting a row causes each pixel in the selected row to transfer charges to a corresponding

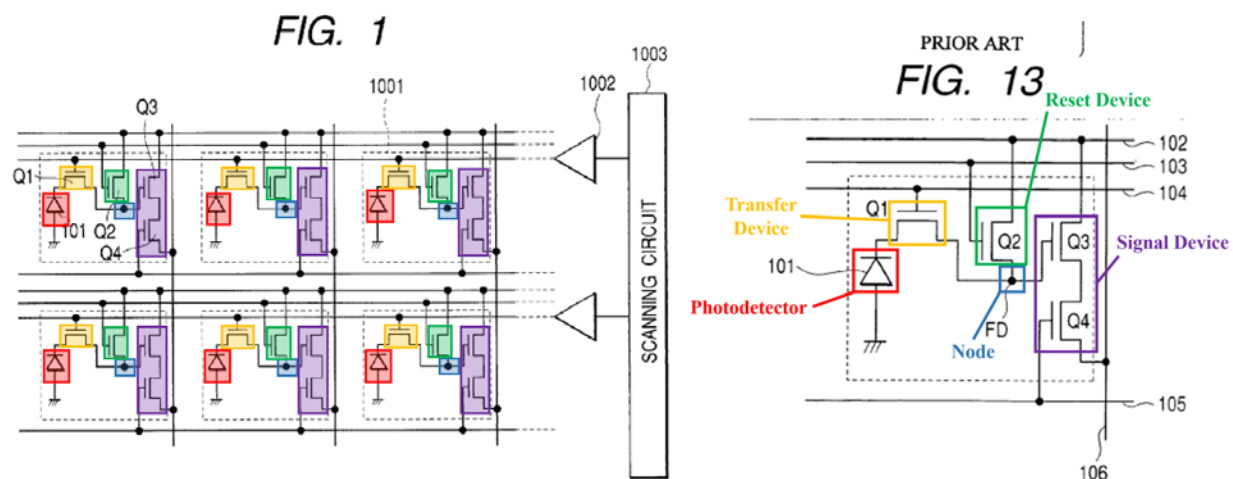
⁵ *Rhodes-674* and *Kochi* demonstrate the knowledge of a POSITA at the relevant time.

signal output line 106 (e.g., columns C1, C2, and C3 in annotated figure 1 above).

The row lines and column lines along with the associated circuitry for driving those lines constitutes “row and column circuitry” as recited in claim 1. (Ex. 1002, ¶75.)

g) a plurality of signal devices coupling the plurality of nodes to the row and column circuitry; and

Koizumi discloses this limitation. (Ex. 1002, ¶¶76-80.) As shown in annotated figures 1 and 13 below, each pixel of *Koizumi*’s pixel array includes an input MOS transistor Q3 and a selection switch Q4 (collectively, a “signal device”). (Ex. 1005, 1:26-35, 6:52-56, FIGs. 1, 13.) Notably, the understanding that the input MOS transistor Q3 and the selection switch Q4 together form a “signal device” for each pixel is consistent with the language of claim 11 of the ’671 patent. (Ex. 1001, claim 11; *see infra* Section IX.A.5.)



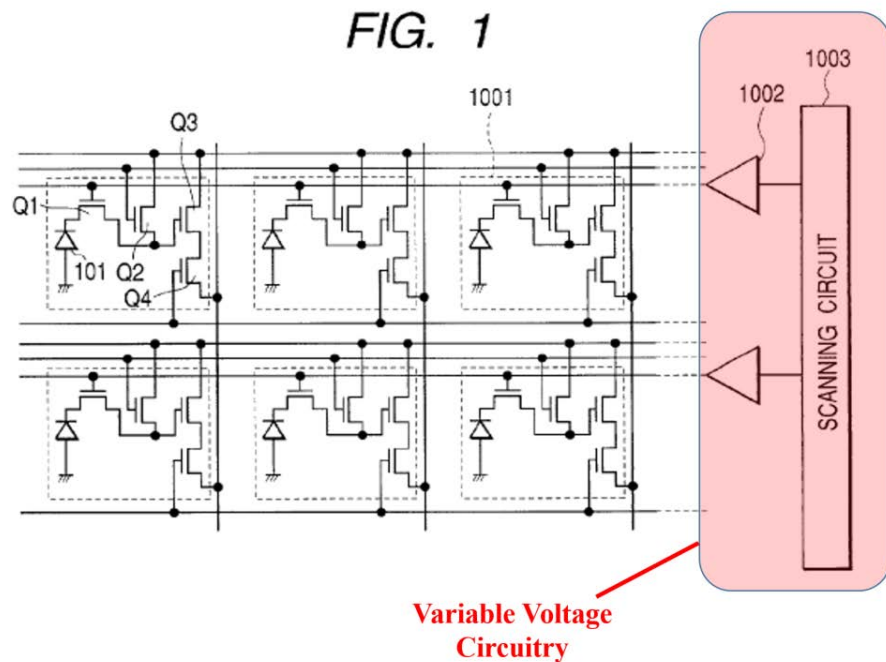
(*Id.*, FIGs. 1, 13 (annotated); Ex. 1002, ¶76.)

As *Koizumi* explains, “input MOS transistor Q3 is included in a source follower for outputting the voltage in the floating diffusion area [FD].” (Ex. 1005, 1:29-32.) As shown in annotated figures 1 and 13 above, the input MOS transistor Q3 and the selection switch Q4 are in a source follower arrangement. (*Id.*; *see also id.*, 1:46-50.) The gate of the selection switch Q4 is coupled to the selection switch control line 105 that is used to select a row in the pixel array, while the drain of Q4 is coupled to the signal output line 106 corresponding to a column in the array. (*Supra* Section IX.A.1(f).) Thus, when the selection switch control line 105 is asserted and selection switch Q4 is turned on, “the voltage in the floating diffusion area [FD] is output to the signal output line 106.” (Ex. 1005, 1:29-32, 1:46-50; Ex. 1002, ¶¶77-80.) Accordingly, floating diffusion node FD is coupled to lines 105 and 106 (“row and column circuitry”) by devices Q3 and Q4 for each of the plurality of pixels in the pixel array (“plurality of signal devices”).

h) variable voltage circuitry including a voltage selector determining a control voltage of the control signal applied to the plurality of transfer devices.

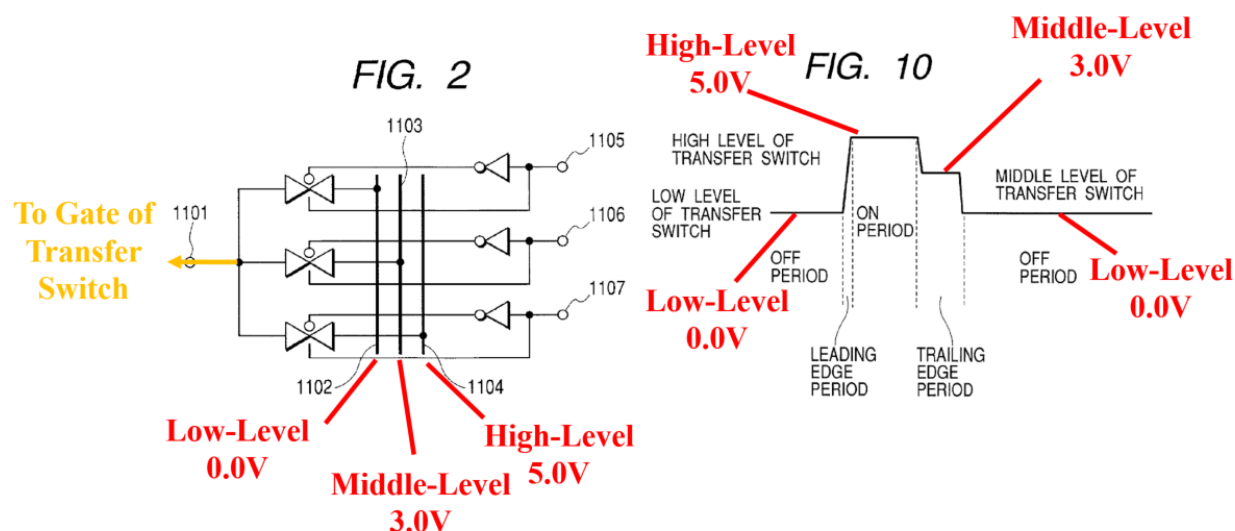
Koizumi discloses this limitation. (Ex. 1002, ¶¶81-85.) *Koizumi* discloses gate drive circuits 1002 and scanning circuit 1003 (collectively, “variable voltage circuitry”) that includes circuitry that determines the voltage applied to the transfer gate Q1 in each of the plurality of pixels (“a voltage selector determining a control

voltage of the control signal applied to the plurality of transfer devices”). (Ex. 1005, 6:54-59, FIG. 1.)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶81.)

As discussed in Section IX.A.1(d), *Koizumi* discloses a gate drive circuit 1002 that is used to provide the control voltage of the transfer gate for each pixel in the pixel array. (*Supra* Section IX.A.1(d).) Specifically, *Koizumi* discloses using the circuit shown in annotated figure 2 below to select between three different voltages in order to apply a signal with a waveform shown in Figure 10 (also below) to transfer switch Q1. (Ex. 1005, 6:60-7:18; *see supra* Section IX.A.1(d).)



(*Id.*, FIGs. 2, 10 (annotated); Ex. 1002, ¶82.)

Koizumi explains that the circuit in figure 2 is used “to output a low level, middle level, and high level, the circuit is designed to input (1,0,0), (0,1,0), and (0,0,1) from the scanning circuit 1003 to input terminals 1105, 1106, and 1107 of the [gate drive] circuit, respectively.” (Ex. 1005, 6:61-66.) A low-level signal (0.0V), middle level signal (3.0V), and high-level signal (5.0V) is selected from a low-level supply line 1102, middle-level supply line 1103, and high level supply line 1104 and provided to the output terminal 1101. (*Id.*, 7:1-5.) “The output terminal 1101 is connected to the gate of the transfer switch Q1 of the pixel 1001 shown in FIG. 1.” (*Id.*, 7:5-7.) *Koizumi* discloses that by applying the middle level signal of 3.0V for 0.5 μ sec during the trailing edge period as shown in figure 10 above, the residual image is reduced and random noise is suppressed. (*Id.*, 7:10-15.) Therefore,

being able to select the middle level voltage in addition to the high and low voltage levels improves the performance of the image sensor. (Ex. 1002, ¶¶83-84.)

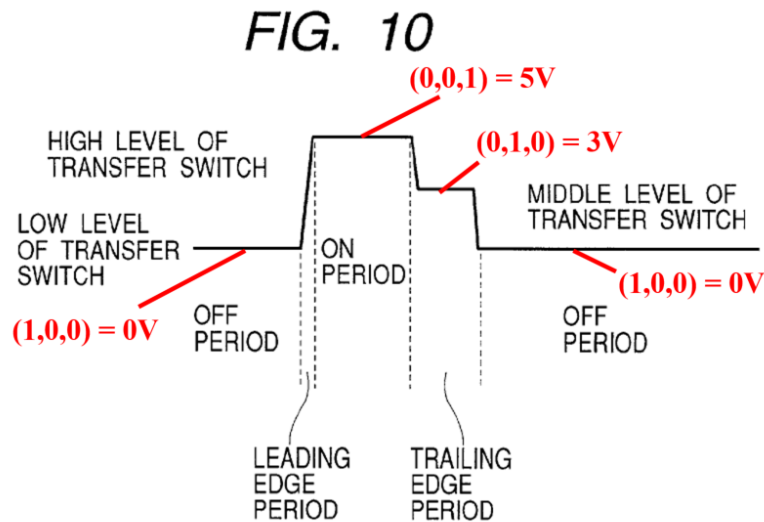
Thus, *Koizumi* discloses that the scanning circuit 1003 and gate drive circuit 1002 (“variable voltage circuitry”) include a voltage selector determining a control voltage of the control signal (e.g., low (0.0V), middle (3.0V), or high (5.0V) level signal) applied to the plurality of transfer switches Q1 (“transfer devices”). (*Id.*, ¶85.)

2. Claim 6

- a) **The circuit of claim 1, wherein the voltage circuitry further comprises a digital to analog converter generating the control signal on the image sensor integrated circuit.**

Koizumi discloses this limitation. (Ex. 1002, ¶¶86-90.) As discussed above in Section IX.A.1(h), gate drive circuit 1002 selects one of a low-level signal (0.0V), a middle-level signal (3.0V), and a high-level signal (5.0V) as the control signal that is applied to the gate of transfer switch Q1 for each of the pixels in the pixel array. (*Id.*, 7:1-7.) A POSITA would have understood that, consistent with *Koizumi*’s description of these signals as specific voltages (0V, 3V, and 5V) and not as logic levels (high, low) or binary bits (0, 1), this resulting control signal generated by the circuitry in figure 2 is an analog signal. (Ex. 1002, ¶¶86-87.) Further, *Koizumi* explains that “to output a low level, middle level, and high level [signal], the circuit [1002] is designed to input (1,0,0), (0,1,0), and (0,0,1) from the scanning circuit 1003

to input terminals 1105, 1106, and 1107.” (Ex. 1005, 6:61-66.) A POSITA would have understood that such inputs are digital signals as they are represented by binary bits corresponding to logic high (“1”) and logic low (“0”) states. (Ex. 1002, ¶88.) Accordingly, gate drive circuit 1002 (“voltage circuitry”) converts digital signal inputs (1,0,0), (0,1,0), and (0,0,1) from scanning circuit 1003 to a control signal that is one of three analog voltages (0V, 3V, or 5V), and thus constitutes “a digital to analog converter generating the control signal on the image sensor integrated circuit,” as claimed. (*Id.*, ¶¶89-90.)



(Ex. 1005, FIG. 10 (annotated); Ex. 1002, ¶89.)

3. Claim 7

- a) The circuit of claim 1, wherein the variable voltage circuitry includes a waveform adjustor.

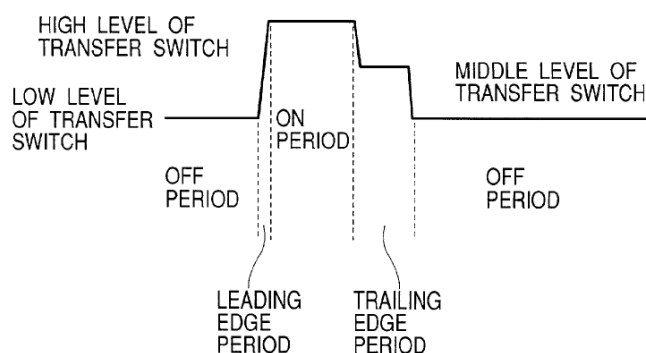
Koizumi discloses this limitation for at least the reasons discussed below in Section IX.A.4. (Ex. 1002, ¶91.)

4. Claim 8

- a) The circuit of claim 1, wherein the variable voltage circuitry includes a waveform adjustor determining a rise time and a fall time of the control signal applied to the plurality of transfer devices.

Koizumi discloses this limitation. (Ex. 1002, ¶¶92-100.) As discussed above in Sections IX.A.1(d) and IX.A.1(h), *Koizumi* discloses gate drive circuit 1002 generates the waveform shown in figure 10 (“waveform adjustor”) that is applied to the gate of transfer switch Q1 for each of the pixels in the pixel array. (*Id.*, 6:60-7:9; *supra* Sections IX.A.1(d), (h).)

FIG. 10



(*Id.*, FIG. 10.) As shown in figure 10, the waveform applied to the gate of transfer switch Q1 has a “leading edge period” (“rise time”) and a “trailing edge period” (“fall time”). (*Id.*, 6:16-18 (“The fall speed means the speed of voltage drop during the trailing edge period.”), FIG. 10.) As *Koizumi* explains in connection with figure 8, a lower fall speed (longer trailing edge period) beneficially reduces residual image.

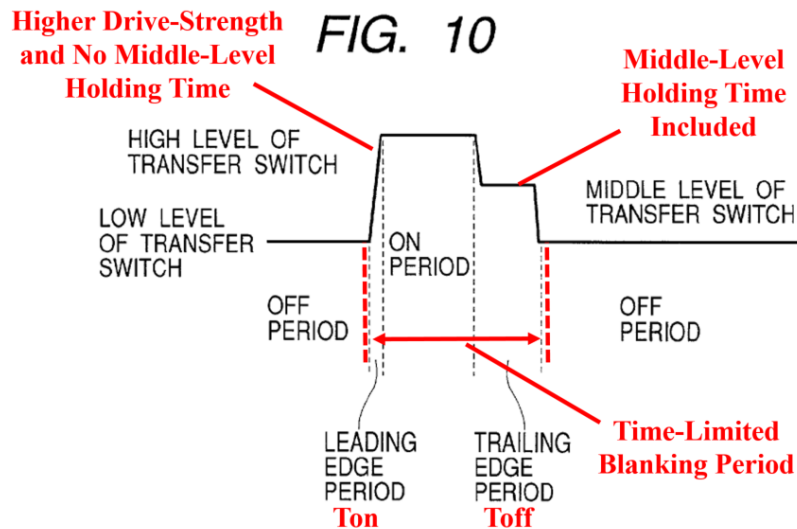
(*Id.*, 6:19-29, FIG. 8 (graph showing relationship between fall speed and residual image).)

Thus, gate drive circuit 1002 prolongs the trailing edge period by applying a middle level signal (e.g., 3.0V) to the gate of transfer switch Q1 for 0.5 μ sec. (*Id.*, 7:8-18.) Accordingly, *Koizumi* discloses that gate drive circuit 1002 (“waveform adjustor”) determines the trailing edge period (“fall time”) of the voltage (“control signal”) applied to transfer switch Q1 of each pixel (“plurality of transfer devices”). (Ex. 1002, ¶¶92-96.)

Koizumi also discloses that the period for charge transfer by the transfer switch is limited, and therefore because the fall-time is delayed (e.g. by application of the middle-level signal during the trailing edge period),⁶ “the rise speed in turning on the transfer switch must be high, as in the prior art.” (Ex. 1005, 8:20-24.) Therefore, *Koizumi* discloses that “the leading edge time T_{on} and trailing edge time T_{off} has a relation $T_{on} < T_{off}$,” which can be accomplished by making the low-high driving force greater than the high-to-low driving force. (*Id.*, 8:24-30.) Therefore, a

⁶ A POSITA would have understood that *Koizumi*’s disclosure of the limited “blanking period” and fall-time being delayed with respect to the trapezoidal waveform in figure 9 also applies to the fall-time being delayed with respect to the addition of the middle-level holding time in figure 10.

POSITA would have recognized that the “leading edge period” (“rise time”) is also determined by the gate drive circuit 1002, which has a greater drive strength for low-high transitions. (Ex. 1002, ¶¶97-99.) In addition, the “leading edge period” (“rise time”) is also determined by the gate drive circuit 1002 **not including** a “middle level [signal] holding time” in the leading edge like that included in the falling edge. (Ex. 1005, FIG. 10; Ex. 1014⁷, 5:59-6:4 (disclosing that for a waveform like that shown in figure 10 of *Koizumi*, an intermediate state (e.g. middle-level holding time) “may also be provided upon transition of signal T from the low level to the high level”, FIG. 9.); Ex. 1002, ¶¶99-100.)



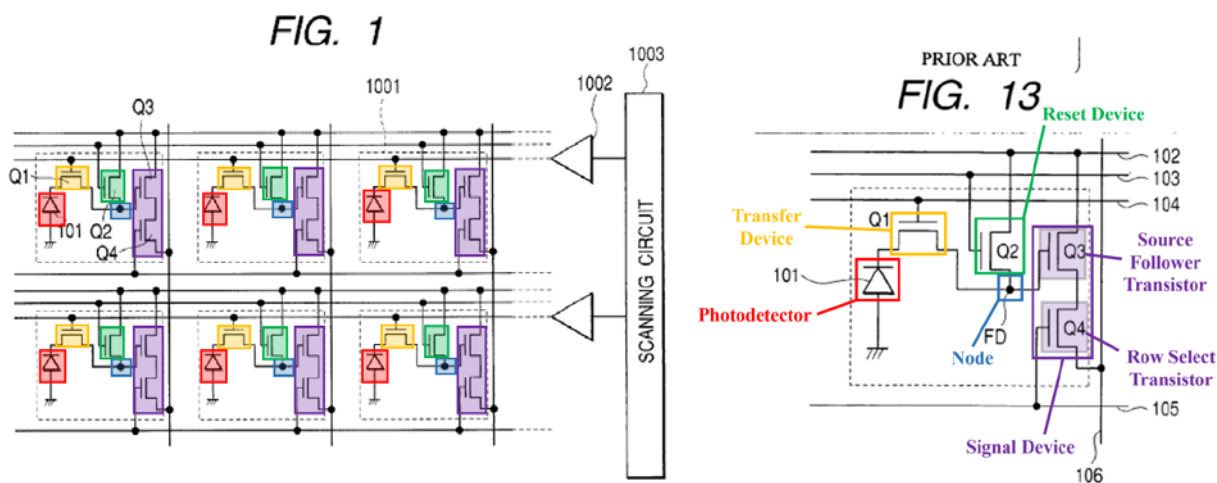
(Ex. 1005, FIG. 10 (annotated); Ex. 1002, ¶¶99.)

⁷ *Cazaux* demonstrates the knowledge of a POSITA at the relevant time.

5. Claim 11

- a) The circuit of claim 1, wherein the plurality of signal devices includes a plurality of row select transistors coupled to the row and column circuitry and a plurality of source follower transistors coupled to the plurality of nodes.

Koizumi discloses this limitation. (Ex. 1002, ¶¶101-102.) As discussed in Section IX.A.1(g), each pixel of *Koizumi*'s pixel array includes an input MOS transistor Q3 and a selection switch Q4 that together form a "signal device" such that the array of pixels includes a "plurality of signal devices." (Ex. 1005, 1:26-35, 6:52-56, FIGs. 1, 13; *supra* Section IX.A.1(g).)



(*Id.*, FIGs. 1, 13 (annotated); Ex. 1002, ¶101.)

As shown in annotated figure 13 above, the gate and drain of selection switch Q4 (“row select transistor”) are respectively coupled to the selection switch control line 105 that performs row selection and signal output line 106 that corresponds to the columns in the pixel array, which are part of the “row and column circuitry” for

the image pickup device. (*Supra* Section IX.A.1(f).) Additionally, the input MOS transistor Q3 is a “source follower transistor” coupled to the floating diffusion node FD (“node”) of each pixel. (Ex. 1005, 1:29-32.) Therefore, each “signal device” in each pixel includes a “row select transistor” (Q4) and a “source follower transistor” (Q3) such that the plurality of pixels in the pixel array includes a “plurality of signal devices [that] includes a plurality of row select transistors coupled to the row and column circuitry and a plurality of source follower transistors coupled to the plurality of nodes” as recited in claim 11. (Ex. 1002, ¶102.) Such an understanding is consistent with the disclosure of the ’671 patent. (Ex. 1001, 4:9-10, FIG. 1.)

6. Claim 12

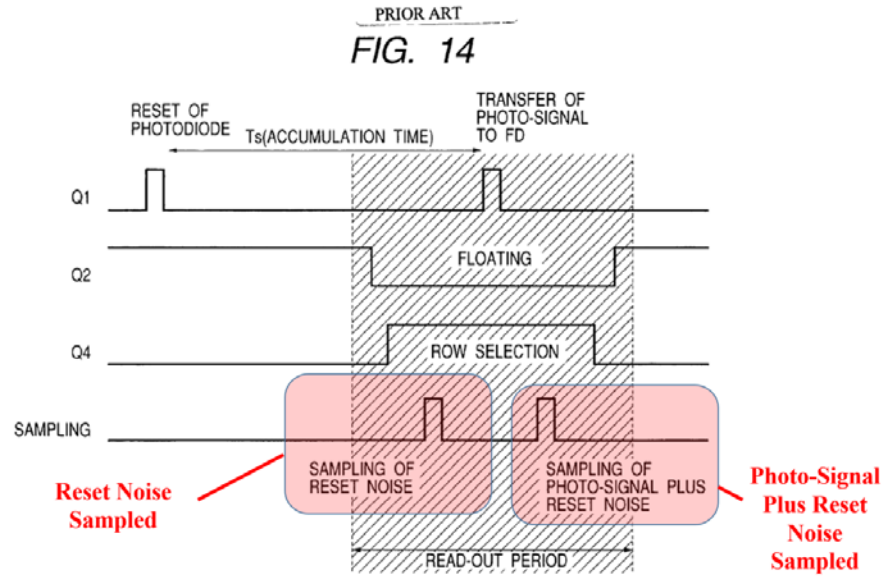
a) The circuit of claim 1, wherein the plurality of photodetectors is a plurality of photodiodes.

Koizumi discloses this limitation. (Ex. 1002, ¶103.) As discussed in Section IX.A.1(b), each pixel in *Koizumi*’s pixel array includes a photodiode 101. (Ex. 1005, 1:25-28, FIG. 13; *supra* Section IX.A.1(b).)

7. **Claim 13**

- a) **The circuit of claim 1, wherein each measurement of the total of the photons is corrected by correlated multiple sampling with a prior measurement of the total of the photons.**

Koizumi discloses this limitation. (Ex. 1002, ¶¶104-109.) For example, *Koizumi* discloses that the read out of a pixel includes double-sampling the charge corresponding to the pixel in order to eliminate reset noise and obtain a high signal to noise (S/N) ratio. (Ex. 1005, 1:41-2:5; Ex. 1002, ¶104.) Specifically, *Koizumi* discloses that, for each read-out operation, after resetting the photodiode 101, the floating diffusion area is set in the floating state, and the selection switch is turned on such that any reset noise present is sampled. (Ex. 1005, 1:41-50, FIG. 14.) A POSITA would have understood that the reset noise corresponds to a “measurement of the total of the photons” as the reset noise is detected in the same manner as charges resulting from photons striking the photodiode. (Ex. 1002, ¶105.) Later, the charges corresponding to the accumulation period of the photodiode (the “photo-signal”) are transferred to the floating diffusion area and a second sampling operation captures the photo-signal plus the reset noise. (Ex. 1005, 1:50-65, FIG. 14.) These sampling events are shown in annotated figure 14 below.



(Ex. 1005, FIG. 14 (annotated); Ex. 1002, ¶105.)

After the second sampling operation, the reset noise sampled in the first sampling operation is subtracted from the photo-signal plus reset noise sampled in the second sampling operation, thereby removing the reset noise from the second sample. (Ex. 1005, 1:66-2:2.) While such multiple-sampling operations to remove reset noise were known in the prior art and disclosed by *Koizumi*, *Koizumi* discloses additional measures to remove other noise in imaging systems. (*Id.*, 2:3-12; Ex. 1002, ¶106-107.) Specifically, *Koizumi* discloses circuits and methods that are used to address “residual image and random noise.” (Ex. 1005, 2:6-7, 2:10-12, 2:27-29, 7:10-13.)

Koizumi discloses that “[i]t is an object of the invention to obtain an image almost free from noise” (*id.*, 3:54-55), and a POSITA would have understood that *Koizumi*’s additional noise reduction measures aimed at residual and random noise

are used in conjunction with the prior art double-sampling that was known to remove reset noise. (Ex. 1002, ¶¶107-108.) The removal of the residual, random, and reset noise is consistent with the objective of “an image almost free from noise.” (*Id.*; Ex. 1005, 3:54-55) Therefore, *Koizumi* discloses reset-noise removal based on a first sampling of the reset noise and a second sampling of the reset noise plus the photo-signal in conjunction with an image pickup device that includes the gate drive circuit discussed above with respect to claim 1. Therefore, for each readout of a pixel (“each measurement of the total of the photons of the pixel”), a first sampling captures reset noise (“prior measurement of the total of the photons”) and a second sampling captures reset noise plus photo-signal (“measurement of the total of the photons”), where the first sampling is subtracted from the second to remove the reset noise (“is corrected by correlated multiple sampling with a prior measurement of the total of the photons”). (Ex. 1002, ¶109.)

B. Ground 2: Claims 5, 14, 18-21, and 24-26 are Obvious in View of *Koizumi*

1. Claim 5

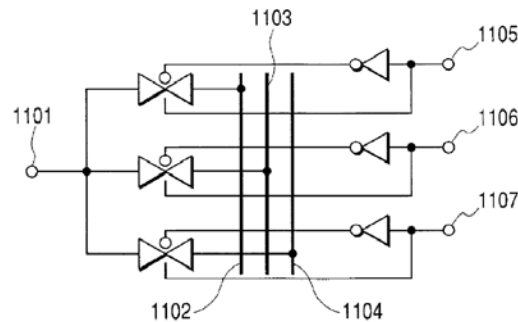
- a) **The circuit of claim 1, wherein the control signal is generated on circuitry separate from the image sensor integrated circuit.**

Koizumi discloses or suggests this limitation to the extent it can be understood. (Ex. 1002, ¶¶110-14.) As discussed in Section IX.A.1(h) above, *Koizumi*'s gate drive circuit 1002 includes a low-level supply line 1102, middle-level supply line 1103, and high-level supply line 1104. (Ex. 1005, 7:1-5). The control signal provided to the gate of transfer devices is selected from these three supply lines, which respectively carry a low (0.0V), middle (3.0V), and high (5.0V) level signal ("control signal"), and output through terminal 1101 of each gate drive circuit. (*Id.*, 6:60-7:9.) While *Koizumi* does not disclose how the voltages on these supply lines are generated, it would have been obvious for a POSITA to generate these voltages external to the image pickup device integrated circuit discussed above in Section IX.A.1. (Ex. 1002, ¶¶110-11.)

Indeed, a POSITA would have been motivated to generate these voltages external to the integrated circuit in order to provide flexibility in configuring these voltages for different applications. (*Id.*, ¶¶111-13.) The example high-level voltage (5V) and low-level voltage (0V) were common supply voltages at the time of the alleged invention. (*Id.*, ¶113.) A POSITA would have understood that such power

supply voltages are typically generated off-chip and would have had a reasonable expectation of success in generating all three of the low, middle, and high voltages off chip as a POSITA would have been familiar with such voltage generation circuitry as it was commonly used to provide supply voltages to integrated circuits. (*Id.*)

FIG. 2



(Ex. 1005, FIG. 2.) Because a POSITA would have found it obvious to generate the supply line voltage that is selected for provision as the gate voltage to the transfer gate (“control signal”) on a different integrated circuit, *Koizumi* discloses or suggests that the “control signal is generated on circuitry separate from the image sensor integrated circuit” as claimed. (Ex. 1002, ¶114.)

2. Claim 14

Claim 14 recites “a computer readable medium containing a description of an image sensor integrated circuit comprising” the limitations of claim 1. (*Compare* Ex. 1001, claim 14 *with* claim 1.) As discussed in Section IX.A.1, *Koizumi* discloses the image sensor integrated circuit of claim 1. A POSITA would have understood that semiconductor integrated circuit design, like the design of image sensors as

disclosed in *Koizumi*, is typically performed using computer aided design tools that result in designs for the integrated circuits that would be understood, in the context of the *Koizumi*, as a “computer readable description of an image sensor integrated circuit.” (Ex. 1002, ¶¶115-16.) Indeed, the creation of such computer-readable designs has been known in the industry for decades, and a typical integrated circuit designer would be aware of such computer-readable descriptions, capable of creating such a computer-readable description, and motivated to create such a computer-readable description as using computer aided design tools greatly simplifies the integrated circuit design and fabrication process. (*Id.*, ¶117.) Accordingly, because the creation of a computer-readable description of *Koizumi*’s image pickup device would have been obvious to a POSITA, *Koizumi* discloses or suggests all of the features of claim 14 for the same reasons discussed above in Section IX.A.1. (*Id.*, ¶118; *supra* Section IX.A.1.)

3. Claim 18

- a) **The computer readable medium of claim 14, wherein the control signal is generated on circuitry separate from the image sensor integrated circuit.**

Koizumi discloses or suggests this limitation for the same reasons discussed above in Sections IX.B.1 and IX.B.2. (Ex. 1002, ¶119.)

4. Claim 19

- a) **The computer readable medium of claim 14, wherein the voltage circuitry further comprises a digital to analog converter generating the control signal on the image sensor integrated circuit.**

Koizumi discloses or suggests this limitation for the same reasons discussed above in Sections IX.A.2 and IX.B.2. (Ex. 1002, ¶120.)

5. Claim 20

- a) **The computer readable medium of claim 14, wherein the variable voltage circuitry includes a waveform adjustor.**

Koizumi discloses or suggests this limitation for the same reasons discussed above in Sections IX.A.4 and IX.B.2. (Ex. 1002, ¶121.)

6. Claim 21

- a) **The computer readable medium of claim 14, wherein the variable voltage circuitry includes a waveform adjustor determining a rise time and a fall time of the control signal applied to the plurality of transfer devices.**

Koizumi discloses or suggests this limitation for the same reasons discussed above in Sections IX.A.4 and IX.B.2. (Ex. 1002, ¶122.)

7. Claim 24

- a) **The computer readable medium of claim 14, wherein the plurality of signal devices includes a plurality of row select transistors coupled to the row and column circuitry and a plurality of source follower transistors coupled to the plurality of nodes.**

Koizumi discloses or suggests this limitation for the same reasons discussed above in Sections IX.A.5 and IX.B.2. (Ex. 1002, ¶123.)

8. Claim 25

- a) **The computer readable medium of claim 14, wherein the plurality of photodetectors is a plurality of photodiodes.**

Koizumi discloses or suggests this limitation for the same reasons discussed above in Sections IX.A.6 and IX.B.2. (Ex. 1002, ¶124.)

9. Claim 26

- a) **The computer readable medium of claim 14, wherein each measurement of the total of the photons is corrected by correlated multiple sampling with a prior measurement of the total of the photons.**

Koizumi discloses or suggests this limitation for the same reasons discussed above in Sections IX.A.7 and IX.B.2. (Ex. 1002, ¶125.)

C. Ground 3: Claims 2 and 15 are Obvious Over *Koizumi* and *Yoshimitsu*

1. Claim 2

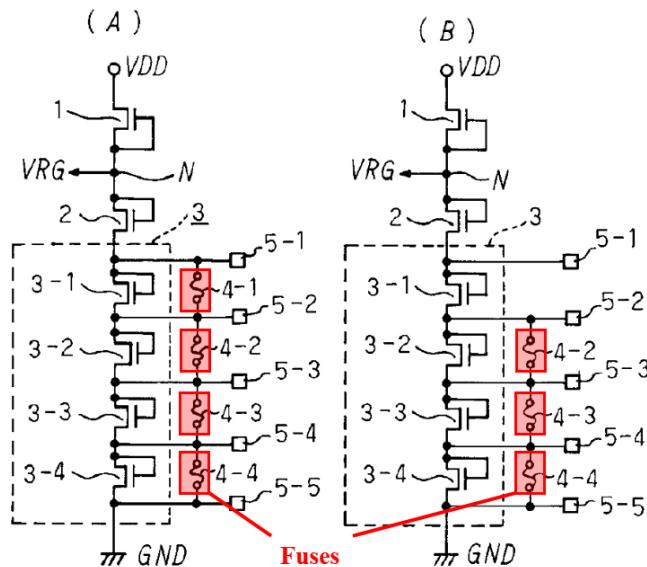
- a) The circuit of claim 1, wherein the voltage selector is controlled by a fuse.**

Koizumi in view of *Yoshimitsu* discloses or suggests this limitation. (Ex. 1002, ¶¶126-38.) As discussed in Section IX.A.1(h), *Koizumi* discloses a gate drive circuit 1002 and a scanning circuit 1003, which collectively constitute the claimed “variable voltage circuitry including a voltage selector” recited in claim 1. (*Supra* Section IX.A.1(h).) While *Koizumi* discloses that low-level (0.0V), middle level (3.0V), and high-level (5.0V) signals are output from the gate drive circuit 1002 shown in figure 2 from supply lines 1102-1104 (Ex. 1005, 7:1-5), *Koizumi* does not explicitly disclose how these different voltages are generated. (Ex. 1002, ¶¶126-27.) *Yoshimitsu*, however, discloses a “bias voltage generating device” for “adjusting the bias voltage [of a solid-state imaging device] over a broad range” that employs fuses to control the voltage generation. (Ex. 1006, Abstract, ¶¶[0012]-[0014], FIG. 1). A POSITA would have found it obvious to combine *Koizumi* and *Yoshimitsu* such that *Koizumi*’s voltage levels are generated by a fuse-based voltage generation circuit like that disclosed by *Yoshimitsu*. (Ex. 1002, ¶128; *id.*, ¶46.) *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

For instance, *Yoshimitsu* discloses that in a solid-state imaging device similar to that disclosed in *Koizumi* (Ex. 1006, ¶¶[0002]-[0004], FIGs. 3-5), “the bias voltage VRG [], which, as shown in FIG. 4, is normally generated by a source-follower bias circuit comprising a drive MOS transistor MD and a charge MOS transistor ML” (*id.*, ¶[0005], FIG. 4). “This type of bias circuit outputs, as a reset bias voltage VRG, the threshold voltage V_{th} of the drive MOS transistor MD subtracted from the power supply voltage VDD ($VDD - V_{th}$).” (*Id.*) *Yoshimitsu* further discloses that “[t]he reset bias voltage VRG undergoes fluctuation and will sometimes malfunction.” (*Id.*, ¶[0006].) Thus, there is a need to change the bias voltage after the circuit is formed. (*Id.*) In a conventional bias circuit as shown in Figure 4, “it is possible to change the threshold voltage [V_{th}] of the MOS transistor MD,” and thus adjusting the output bias voltage VRG, “by adjusting the voltage applied to the gate electrode” of the driving MOS transistor MD. (*Id.*, ¶¶[0007]-[0008].) However, this conventional method of adjusting the bias voltage by applying a “negative potential offset” to the gate of MOS transistor MD can only increase, but not lower, the threshold voltage. (*Id.*, ¶[0009].) Thus, “although the bias voltage VRG can be lowered, it cannot be raised” by such conventional bias circuit, and “the solid-state imaging element becomes defective.” (*Id.*, ¶[0010].)

To solve this problem, *Yoshimitsu* discloses, in connection with Figure 1 (reproduced below), a “bias generating device” including, *inter alia*, a fuse elements

that can be melted or not melted to determine the impedance between the bias voltage output node and the power supply terminal. (*Id.*, ¶¶[0012]-[0014].) To increase the output voltage of the bias generator to match the target value, more fuses can be blown (melted). (*Id.*, ¶[0014].) This way, it “is possible to vary the output value over multiple stages.” (*Id.*)



(*Id.*, FIG. 1 (annotated); Ex. 1002, ¶133.)

In light of *Yoshimitsu*, a POSITA would have been motivated to modify *Koizumi* such that the voltage supplied on at least one of the low-level supply line 1102, middle-level supply line 1103, and high-level supply line 1104 (Ex. 1005, 7:1-5) is generated by a bias generator with fuse elements similar to that taught by *Yoshimitsu*. (Ex. 1002, ¶¶129-35.) A POSITA would have recognized that, for example, the voltage on the middle-level supply line 1103 could be generated using such a fuse-based voltage generator in order to allow that voltage to be adjusted in

order to better align with the goal of noise reduction as discussed by *Koizumi* with respect to the embodiment corresponding to figures 2 and 10. (*Id.*, ¶136.) Such a modification discloses a “voltage selector...controlled by a fuse,” as claimed.

A POSITA would have looked to *Yoshimitsu* to improve *Koizumi*’s apparatus because both *Yoshimitsu* and *Koizumi* are directed toward solid state imaging devices. (*Id.*, ¶137; Ex. 1005, 1:10-13; Ex. 1006, ¶¶[0002]-[0004], FIGs. 3-5.) Indeed, since *Koizumi* does not explicitly disclose how the bias voltages in supply lines 1102-1104 are generated, a POSITA would have been motivated to look for bias voltage generators such as those taught by *Yoshimitsu*. (Ex. 1002, ¶137.) Having read *Yoshimitsu*, a POSITA would have recognized the advantages of *Yoshimitsu*’s bias generator over conventional devices, as taught by *Yoshimitsu* and discussed above. (*Id.*; Ex. 1006, ¶¶[0005]-[0014].) A POSITA would have had a reasonable expectation of success in modifying *Koizumi* in view of *Yoshimitsu* because such a modification would have been nothing more than combining known elements in accordance with well-known principles of integrated circuit design and fabrication. (Ex. 1002, ¶138.)

2. Claim 15

- a) **The computer readable medium of claim 14, wherein the voltage selector is controlled by a fuse.**

Koizumi in view of *Yoshimitsu* discloses or suggests this limitation for the same reasons discussed above in Sections IX.C.1 and IX.B.2. (Ex. 1002, ¶139.)

D. Ground 4: Claims 3, 6, 16, and 19 are Obvious Over *Koizumi* and *Lee*⁸

1. Claim 3

- a) The circuit of claim 1, wherein the voltage selector is controlled by a register.**

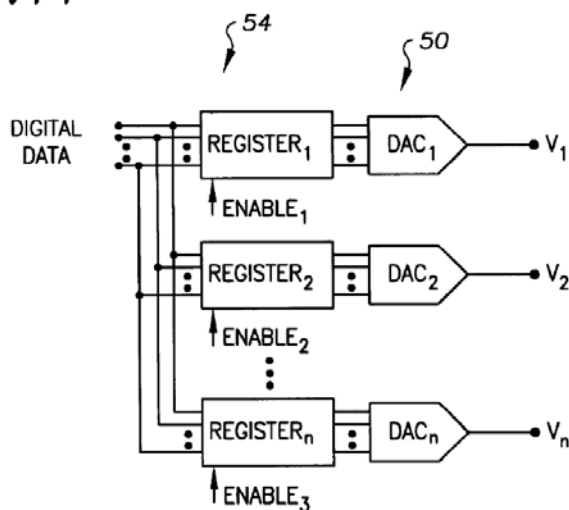
Koizumi in view of *Lee* discloses or suggests this limitation. (Ex. 1002, ¶¶140-47.) As discussed in Section IX.A.1(h), *Koizumi* discloses a gate drive circuit 1002 and a scanning circuit 1003, which collectively constitute “variable voltage circuitry including a voltage selector” as recited in claim 1. (*Supra* Section IX.A.1(h).) *Koizumi*’s gate drive circuit 1002 selects the control voltage from the low-level signal, middle-level signal, and high-level signal that are provided on supply lines 1102-1104. (Ex. 1005, 7:1-7.) *Koizumi* further discloses that “the high level of the transfer switch is set to 5.0 V, the middle level to 3.0 V, and the low level to 0.0 V.” (*Id.*, 7:8-10.) *Koizumi* does not explicitly disclose how these different voltage levels are “set” or generated. (Ex. 1002, ¶141.) *Lee*, however, discloses a register-based voltage generation circuit for generating control voltages in an imaging system including a MOS pixel array (Ex. 1007, Abstract, 12:9-25, FIG. 11; Ex. 1002, ¶¶47-48), and a POSITA would have found it obvious to combine

⁸ Petitioner does not repeat the language of claims 6 and 19, which are provided above in Grounds 1 and 2.

Koizumi and *Lee* such that *Koizumi*'s voltage levels are generated by a register-based voltage generation circuit like that disclosed by *Lee*. (Ex. 1002, ¶142.)

For instance, *Lee* discloses, in connection with Figure 11 (reproduced below), “digital-to-analog converters (DAC’s)...to generate” any number of independent control voltage levels. (Ex. 1007, 12:9-12.) *Lee* explains that “a number, n , of DACs 50 are employed to generate n independent control voltage levels.” (*Id.*, 12:12-14.) For each prescribed voltage level, a corresponding digital voltage value is stored in one of n **digital registers 54**, and “the output of the corresponding DAC is set at the corresponding voltage determined by the data in the **register**.” (*Id.*, 12:14-20.) Accordingly, the digital registers are enabled by an enable signal, thereby causing the corresponding DAC to output the prescribed voltage level, as determined by the data in the register. (*Id.*, 12:9-25.)

FIG. 11



(*Id.*, FIG. 11.) *Lee* discloses that this configuration beneficially allows for more flexibility in setting control voltages “because the DAC’s can be programmed to produce different charge control voltages.” (*Id.*, 12:21-25.)

In light of *Lee*’s disclosures, a POSITA would have been motivated to implement *Koizumi*’s gate drive circuit 1002 to include one or more registers and corresponding DACs, as taught by *Lee*, to generate one or more of the low, middle, and high voltage levels on supply lines 1102-1104. (Ex. 1002, ¶¶143-46.) A POSITA would have appreciated that such a modification would have beneficially increased the device’s flexibility in generating control voltages, because the registers “can be programmed to produce different charge control voltages.” (*Id.*, ¶146; Ex. 1007, 12:21-25.) Such flexibility is beneficial to, and compatible with, *Koizumi*’s description of these voltages as being “set,” which a POSITA would have understood to indicate that they are configurable. (Ex. 1002, ¶146.)

A POSITA would have looked to *Lee* to improve *Koizumi*’s device because both *Lee* and *Koizumi* are directed toward imaging systems including MOS pixel arrays (Ex. 1005, Abstract; Ex. 1007, Abstract), and *Koizumi* does not indicate how the supply voltages 1102-1104 are generated. (Ex. 1002, ¶147.) A POSITA would have had a reasonable expectation of success modifying *Koizumi* in view of *Lee* because such a modification would have been nothing more than combining known elements in accordance with well-known principles of integrated circuit design. (*Id.*)

Such a modification would have resulted in voltage control circuitry including a “voltage selector...controlled by a register, as claimed.” (*Id.*)

2. Claim 6

As discussed above in Section IX.A.2, *Koizumi* discloses this feature. (*Supra* Section IX.A.2) To the extent Pictos argues or the Board finds that *Koizumi* does not explicitly disclose this limitation, *Koizumi* in view of *Lee* discloses or suggests this limitation. (Ex. 1002, ¶¶148-49.) As discussed in Section IX.D.1, a POSITA would have been motivated by *Lee* to modify *Koizumi*’s device to use at least one register and corresponding digital-to-analog converter, as taught by *Lee*, to generate a low, middle, and/or high level control signal. (*Id.*, ¶149.)

3. Claim 16

- a) **The computer readable medium of claim 14, wherein the voltage selector is controlled by a register.**

Koizumi in view of *Lee* discloses or suggests this limitation for the same reasons discussed above in Sections IX.D.1 and IX.B.2. (Ex. 1002, ¶150.)

4. Claim 19

Koizumi in view of *Lee* discloses or suggests this limitation for the same reasons discussed above in Sections IX.D.2 and IX.B.2. (Ex. 1002, ¶151.)

E. Ground 5: Claims 9 and 22 are Obvious Over *Koizumi* and *Inoue*

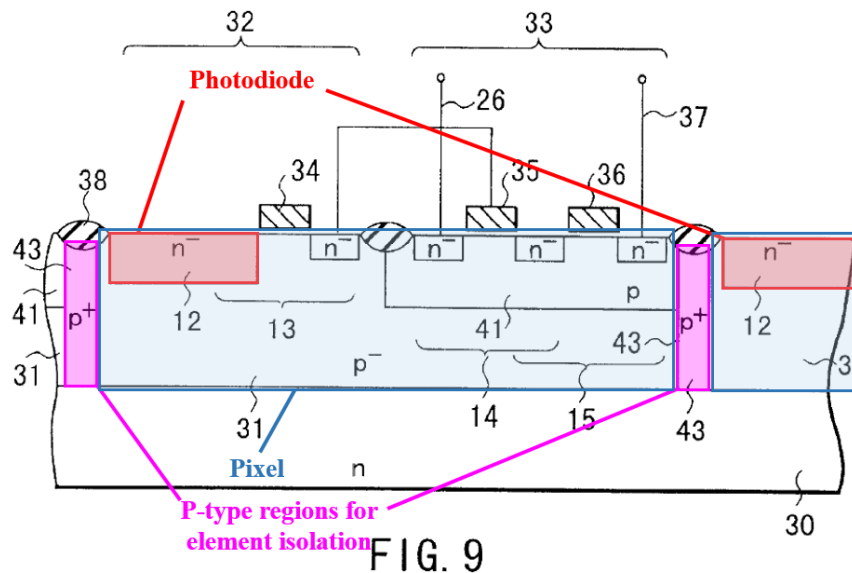
1. Claim 9

- a) The circuit of claim 1, further comprising: a plurality of p-type regions isolating neighboring photodetectors from each other.**

Koizumi in view of *Inoue* discloses or suggests this limitation. (Ex. 1002, ¶¶152-59.) As discussed in Section IX.A.1, *Koizumi* discloses the circuit of claim 1. (*Supra* Section IX.A.1.) To the extent *Koizumi* does not disclose “a plurality of p-type regions isolating neighboring photodetectors from each other,” such a feature would have been obvious in view of *Inoue*. (Ex. 1002, ¶152.)

Inoue discloses a MOS type solid-state image sensor “having an image pickup area formed at a semiconductor substrate and comprising a two-dimensional array of row and column unit cells.” (Ex. 1008, Abstract; 1:5-20.) *Inoue* discloses certain problems with MOS type solid-state image sensor. For instance, “blooming” and “color mixing” may result “from the leaking of overflowed elections into the adjacent pixel,” or “from signal leaking from a deeper area in the substrate.” (*Id.*, 1:63-2:3.) To solve these problems, *Inoue* discloses a MOS type solid-state image sensor which comprises an n type semiconductor substrate, and “at least one first p well area provided in a surface portion of the n type semiconductor substrate, and a plurality of second p well areas selectively provided at a surface portion of the first p well area.” (*Id.*, 2:47-60.)

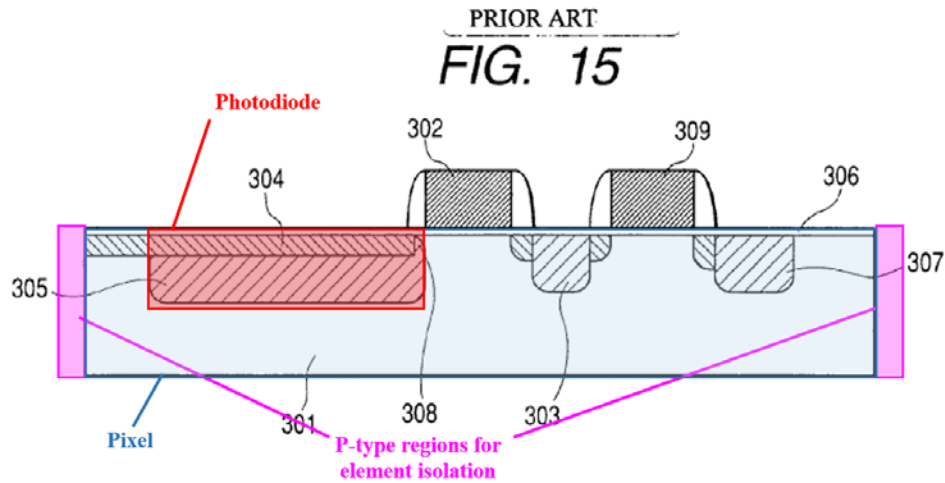
Among other things, *Inoue* discloses, in connection with Figure 9 (reproduced below, “a p⁺ type area 43 for element isolation...formed beneath a field oxide film 38 corresponding to a pixel-to-pixel area.” (*Id.*, 9:28-33.) The p⁺ type area 43 has a higher impurity concentration, and is formed deeper than second p well area 41. (*Id.*, 9:33-35.) This “decreas[es] the leakage of a signal between pix[els],” and thus prevents “color mixing.” (*Id.*, 9:35-39.)



(*Id.*, FIG. 9 (annotated); Ex. 1002, ¶155.) Thus, *Inoue* discloses “a plurality of p-type regions isolating neighboring photodetectors from each other,” as claimed. (Ex. 1002, ¶¶153-55, *id.*, ¶49.)

In light of *Inoue's* disclosures, a POSITA would have found it obvious to modify *Koizumi's* image pickup device to include p type areas with a higher impurity

concentration than *Koizumi*'s p-well 301 to provide increased isolation between pixels. (Ex. 1008, 9:33-35; Ex. 1002, ¶156.)



(Ex. 1005, FIG. 15 (showing a cross-section of *Koizumi*'s pixel, as modified by *Inoue*); Ex. 1002, ¶156.) A POSITA would have been motivated to do so because, as disclosed by *Inoue*, such a modification would have beneficially “decreas[ed] the leakage of a signal between pix[els],” and thus prevented “color mixing” in a pixel array like that disclosed in *Koizumi*. (Ex. 1008, 9:35-39; Ex. 1002, ¶157.)

A POSITA would have looked to *Inoue* to improve *Koizumi*'s device because both *Inoue* and *Koizumi* are directed toward imaging systems including MOS pixel arrays that include photodiodes disposed within p-wells. (Ex. 1005, Abstract; Ex. 1008, Abstract; Ex. 1002, ¶158.) Including p-type regions for pixel isolation like that disclosed in *Inoue* in *Koizumi*'s device would have merely been the use of a known technique (using p-type regions to isolate pixels from one another) applied

to a similar device (the image pickup device of *Koizumi* that includes a pixel array) ready for improvement to achieve the expected and desired result of decreased leakage between pixels and less color mixing. *KSR*, 550 U.S. at 415-21. (Ex. 1002, ¶158.) Including such p-type isolation regions in *Koizumi*'s image pickup device would have been straightforward for a POSITA given such a person's knowledge and *Inoue*'s disclosure as to how to implement such isolation regions in a pixel array like that disclosed in *Koizumi*. (*Id.*)

Such a modification would have resulted in "a plurality of p-type regions isolating neighboring photodetectors from each other," as claimed.

2. Claim 22

- a) The computer readable medium of claim 14, further comprising: a plurality of p-type regions isolating neighboring photodetectors from each other.**

Koizumi in view of *Inoue* discloses or suggests this limitation for the same reasons discussed above in Sections IX.E.1 and IX.B.2. (Ex. 1002, ¶160.)

F. Ground 6: Claims 10 and 23 are Obvious Over *Koizumi* and *Merrill*

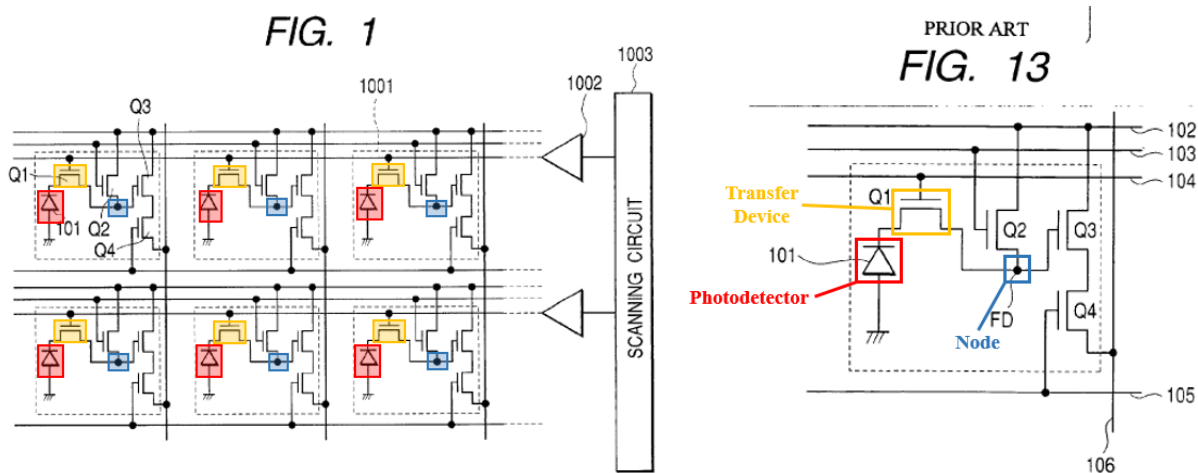
1. Claim 10

Koizumi in view of *Merrill* discloses or suggests the limitations of claim 10.

(Ex. 1002, ¶¶161-77.)

- a) **The circuit of claim 1, wherein each of the plurality of transfer devices includes a first terminal, a second terminal, a body connecting the first terminal and the second terminal, a control terminal controlling the transfer of the electrons between the first terminal and the second terminal through the body, and**

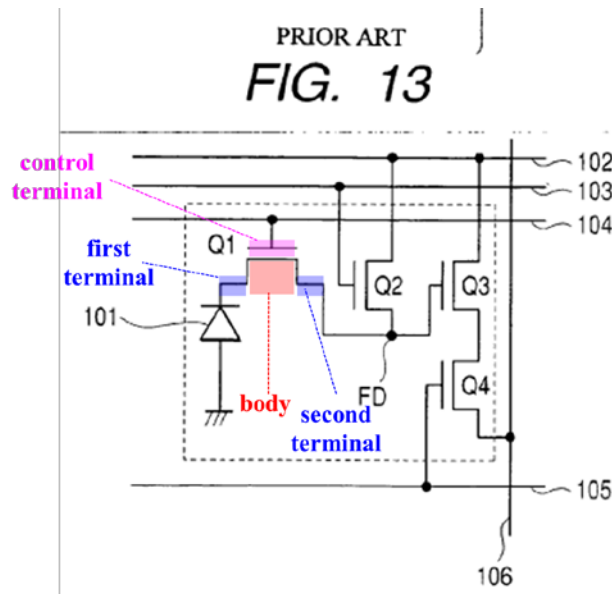
Koizumi discloses this limitation. (Ex. 1002, ¶¶162-64.) As discussed in Section IX.A.1(d), *Koizumi* discloses an image pickup device that includes transfer switch Q1 (“transfer device”) as shown in Figures 1 and 13 below. (Ex. 1005, 1:26-35, 6:52-59, FIGs. 1, 13.)



(Ex. 1005, FIGs. 1, 13 (annotated); Ex. 1002, ¶162.)

Transfer switch Q1 is a MOS transistor. (Ex. 1005, 1:14-18 (“An APS includes for each pixel...MOS switch”), 1:26.) Thus, a POSITA would have

understood that transfer switch Q1 includes a source terminal (“first terminal”), a drain terminal (“second terminal”), a channel (“body”) that connects the source and drain terminals, and a gate terminal (“control terminal”) as shown in annotated Figure 13 below. (Ex. 1002, ¶163; Ex. 1005, FIG. 13, 2:38-46 (disclosing “channel” of a MOS transistor), 2:54 (“gate” of a transfer switch), 7:64-65 (“source” and “drain” of a MOS transistor), Ex. 1011,⁹ FIG. 11.35 (disclosing a MOS transistor including a channel that connects source and drain terminals, and a gate terminal), 483-85.)



(Ex. 1005, FIG. 13 (annotated); Ex. 1002, ¶163.)

A POSITA would have understood that when a sufficiently large bias is applied (known as the threshold voltage) to the gate (“control terminal”), charge

⁹ *Neamen* demonstrates the knowledge of a POSITA at the relevant time.

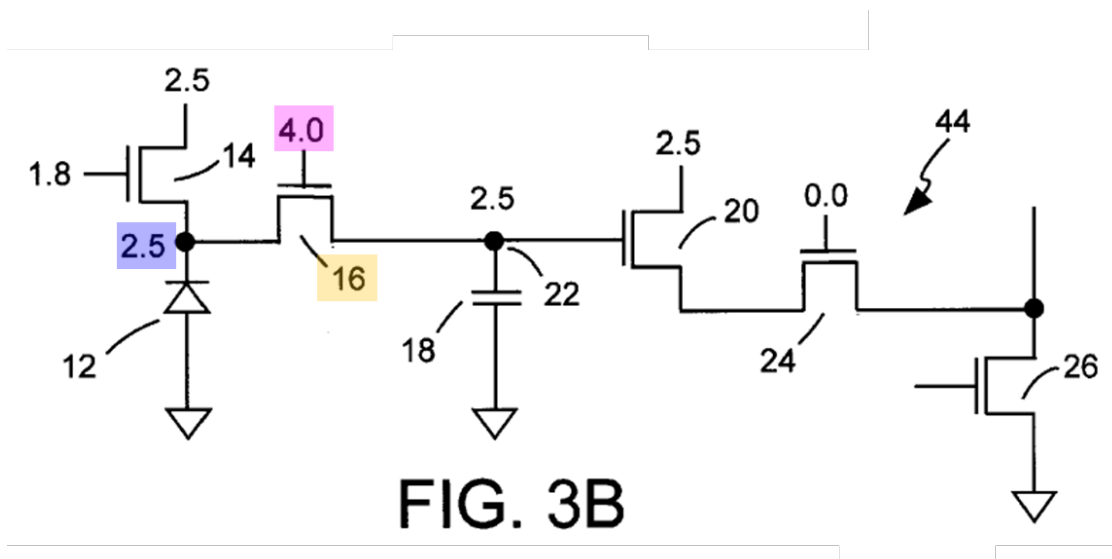
carriers (“electrons”) could flow from the source to the drain through the channel. (Ex. 1002, ¶164; Ex. 1005, 1:26-28 (“a transfer switch Q1 transfers photocharges from a photodiode 101 to a floating diffusion area (FD)”), 3:12 (“threshold voltage” of a transfer switch); Ex. 1011, 483-485 (disclosing that when a sufficiently large gate voltage is applied, an electron inversion layer is formed, which establishes a channel that connects the source and drain terminals).) Indeed, as shown in Figures 17A-D, *Koizumi* discloses that a transfer switch can be “turned on and off” to control the transfer of signal charges from the photodiode to the floating diffusion area, where, as shown in Figure 13, the photodiode is connected to the source and the floating diffusion area is connected to the drain. (Ex. 1005, 3:20-37.) Accordingly, *Koizumi* discloses this limitation. (Ex. 1002, ¶164.)

- b) a dielectric between the control terminal and the body, the dielectric satisfying a lifetime specification of the image sensor integrated circuit when the control signal is applied with the channel formed, the dielectric failing the lifetime specification of the image sensor integrated circuit if the control signal is applied with at least one of the first terminal and the second terminal at a ground voltage of the image sensor integrated circuit.**

Koizumi in view of *Merrill* discloses or suggests these limitations to the extent they can be understood. (Ex. 1002, ¶¶165-77.) Given that transfer switch Q1 of *Koizumi* is a MOS transistor, a POSITA would have understood that it includes a dielectric layer (e.g., oxide or insulator) between the gate (“control terminal”) and

the channel (“body”). (*Id.*, ¶167.) While *Koizumi* does not expressly disclose “dielectric satisfying a lifetime specification of the image sensor integrated circuit...,” a POSITA would have found it obvious to implement such features in view of *Merrill*, to the extent these features can be understood. (*Id.*; *id.*, ¶50.)

Merrill discloses monitoring the voltage drop applied across a gate dielectric to ensure that the transfer transistor may properly operate throughout the expected lifetime of the device. (*Id.*, ¶168.) For example, *Merrill* discloses monitoring “voltage between the gates and the source or drain...for stress in the gate dielectric” of a transfer transistor. (Ex. 1009, 5:9-15.) *Merrill* discloses that, to “transfer the voltage level of 2.5 volts to the storage node 22,” it applies a 4.0 V bias to the gate and a 2.5 V bias to the drain of transfer transistor 16 as shown in Figure 3B. (*Id.*, 5:16-26, 5:36-41.)

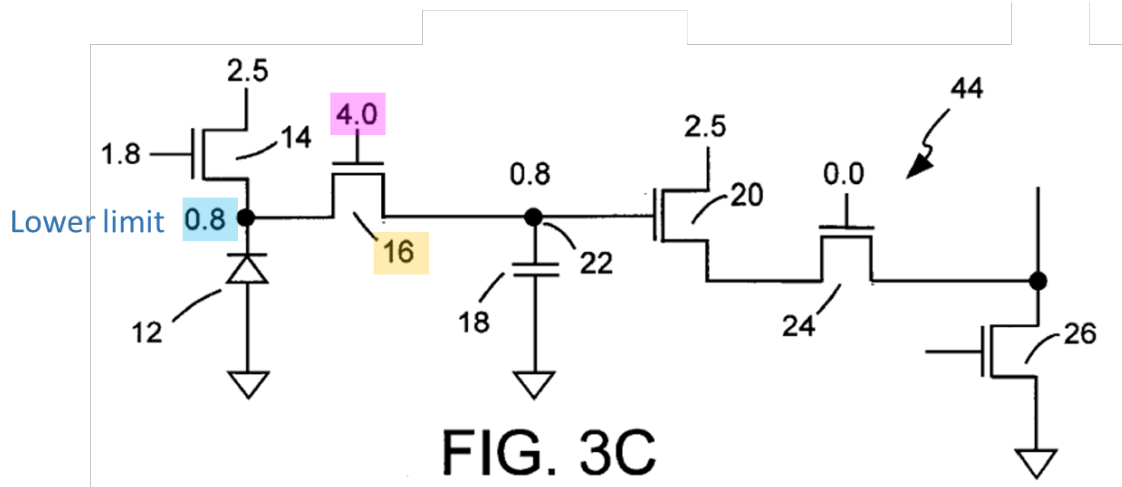


(*Id.*, FIG. 3B (annotated); Ex. 1002, ¶169.) According to *Merrill*, “the maximum operating voltage” across gate dielectric is 2.75 V. (Ex. 1009, 5:4-9 (“MOS transistors that are greater than the nominal operating voltage of 2.5 volts need to be monitored for an excessive electric field represented by a voltage greater than 2.75 volts across the gate dielectric.”), 5:32-35, 5:58-60.) Thus, as a POSITA would have understood, under the gate-drain bias scenario as depicted in Figure 3B above, the voltage drop across the gate dielectric for transistor 16 is 1.5 V, which is less than the maximum operating voltage of 2.75 V and is within the constraints developed for the transistor’s operating lifetime. (Ex. 1002, ¶¶168-71; Ex. 1009, 6:6-10.)

Furthermore, given that, under the FIG. 3B bias scenario, a gate bias (“control signal”) is applied across the gate dielectric of transfer transistor 16 to allow transferring of signal charges through transistor 16, a POSITA would have understood that a channel is formed between the source and drain terminals of transistor 16 under this bias scenario. (Ex. 1002, ¶172; Ex. 1011, 483-85.) Thus, *Merrill* discloses “the dielectric satisfying a lifetime specification of the image sensor integrated circuit when the control signal is applied with the channel formed.” (Ex. 1002, ¶172.)

Additionally, *Merrill* discloses that, when a gate bias of 4.0 V is applied to transfer transistor 16, the **lower limit** of the photodiode cathode voltage, i.e., the drain voltage of the transistor 16, is **0.8 V** in order to meet the operating lifetime

constraints. (Ex. 1009, 5:41-43, 5:48-6:18 (disclosing that while the 3.2 V drop exceeds normal operating condition, it can be tolerated for several reasons, including meeting the operating lifetime constraints).)



(*Id.*, FIG. 3C (annotated); Ex. 1002, ¶173.)

Given that, to satisfy the operating lifetime constraints, the lower limit of the drain voltage is 0.8 V, a POSITA would have understood that an even lower drain voltage, including 0 V (i.e., a ground voltage), would have been outside the limit and thus would not have met the operating lifetime constraints for the gate dielectric. (Ex. 1002, ¶173-74.) Thus, *Merrill* discloses “the dielectric failing the lifetime specification of the image sensor integrated circuit if the control signal is applied with at least one of the first terminal and the second terminal at a ground voltage of the image sensor integrated circuit.” (*Id.*)

While *Koizumi* discloses biasing transfer switch Q1 to facilitate charge transfer, it does not expressly disclose setting a limit on the voltage drop across the

gate dielectric to ensure that the transistor would operate properly throughout its projected lifetime. (*Id.*, ¶175.) As such, a POSITA would have looked to other references, like *Merrill*, that disclose such information. (*Id.*; see generally Ex. 1009.) Having read *Merrill*, a POSITA would have found it obvious to implement a limit on the voltage drop across the gate dielectric by, e.g., setting a lower limit on the drain bias. (Ex. 1002, ¶175.)

A POSITA would have been motivated to implement *Merrill*'s teachings in *Koizumi* because it would have ensured that *Koizumi*'s transfer gate would continue to operate throughout its projected lifetime by avoiding an excessive voltage drop across the gate dielectric. (*Id.*, ¶176.) Indeed, such an excessive voltage drop would have led to high electric field that stresses the gate dielectric, leading to “catastrophic breakdown” of the gate dielectric. (Ex. 1012¹⁰, 448 (“Thin oxide films undergo catastrophic breakdown when stressed by high electric fields.”); Ex. 1002, ¶176.) Furthermore, a POSITA would have understood that setting such voltage limit would have ensured the applied voltages do not overstress the gate dielectric and would have allowed the device to sustain “sufficiently long lifetime under normal operating conditions.” (*Id.*; Ex. 1012, 422 (“The oxide film [of a MOSFET gate oxide] must exhibit a sufficiently long lifetime under normal operating conditions....”).)

¹⁰ *Wolf-V3* demonstrates the knowledge of a POSITA at the relevant time.

Accordingly, a POSITA would have found it beneficial to implement voltage limits, like those disclosed in *Merrill*, for *Koizumi*'s transfer devices. (Ex. 1002, ¶176.)

A POSITA would have looked to *Merrill* to improve *Koizumi* because both *Koizumi* and *Merrill* are directed to CMOS imaging pixel technology that includes a transfer gate to transfer pixel charges. Moreover, a POSITA would have had a reasonable expectation of success in implementing *Merrill*'s voltage limits in *Koizumi*'s image pickup device as gate dielectric breakdown was a known issue in CMOS systems. (Ex. 1015¹¹, 5:38-6:22 (disclosing dielectric breakdown will occur for a sufficiently large gate voltage when the source or drain of the transistor is at ground).) As such, a POSITA would have been aware of the issue and techniques for avoiding it, such as those disclosed by *Merrill*. (Ex. 1002, ¶177.) Furthermore, including voltage operating limitations like that disclosed in *Merrill* in the device of *Koizumi* would have merely been the application of a known technique (setting a voltage operating limit for transfer transistors) to a similar device (the transfer transistor in *Koizumi*) ready for improvement to achieve the expected and desired result of preventing gate dielectric breakdown to ensure an adequate operating lifetime. *KSR*, 550 U.S. at 415-21. (Ex. 1002, ¶177.)

¹¹ *Wang* demonstrates the knowledge of a POSITA at the relevant time.

2. Claim 23

- a) The computer readable medium of claim 14, wherein each of the plurality of transfer devices includes a first terminal, a second terminal, a body connecting the first terminal and the second terminal, a control terminal controlling the transfer of the electrons between the first terminal and the second terminal through the body, and a dielectric between the control terminal and the body, the dielectric satisfying a lifetime specification of the image sensor integrated circuit when the control signal is applied with the channel formed, the dielectric failing the lifetime specification of the image sensor integrated circuit if the control signal is applied with at least one of the first terminal and the second terminal at a ground voltage of the image sensor integrated circuit.

Koizumi in view of *Merrill* discloses or suggests this limitation for the same reasons discussed above in Sections IX.F.1 and IX.B.2. (Ex. 1002, ¶178.)

G. Ground 7: Claims 1, 4, and 11-12 are Anticipated by *Kochi*¹²

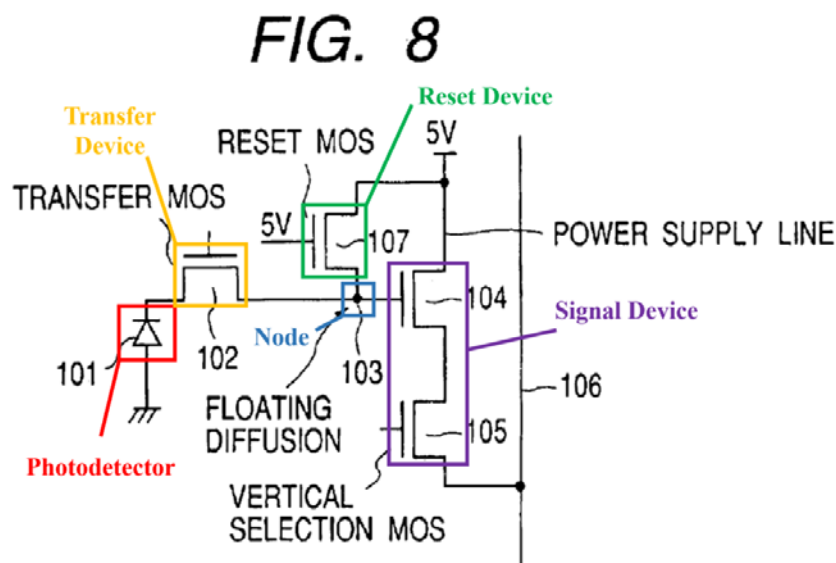
1. Claim 1

a) 1(a)

To the extent the preamble is limiting, *Kochi* discloses the limitations therein. (Ex. 1002, ¶¶179-84; *id.*, ¶¶43-45.) For instance, *Kochi* discloses a “solid state image pickup apparatus,” which, as shown in annotated figures 8 and 9 below, comprises all of the elements recited in claim 1. (Ex. 1010, Abstract, 4:64-5:8.) For

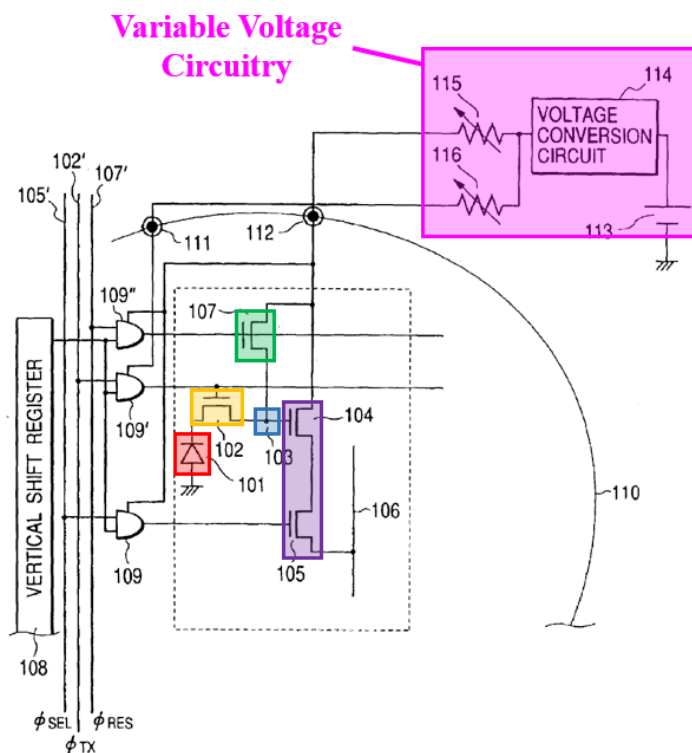
¹² Petitioner does not repeat the language of claims 1 and 11-12, which are provided above in Ground 1.

instance, *Kochi* discloses, in connection with figure 8, “an equivalent circuit corresponding to a pixel” that includes photodiode 101, transfer switch 102 (“transfer device”), floating diffusion area 103 (“node”), resetting MOS transistor 107 (“reset device”), as well as a source follower MOS transistor 104 and a vertical selecting MOS transistor 105 (collectively, “signal device”). (*Id.*, 4:63-5:8.)



(*Id.*, FIG. 8 (annotated); Ex. 1002, ¶¶180-81.) *Kochi* further discloses, in connection with figure 9, “a **solid state image pickup apparatus 110** for converting incident light into an electrical signal for output to the exterior and a **voltage supply unit** for driving the solid state image pickup apparatus 110.” (Ex. 1010, 5:58-62.) *Kochi* explains that the image pickup apparatus 110 and the voltage supply unit shown in figure 9 are “formed on [the] same semiconductor chip” (*id.*), which constitutes an “image sensor integrated circuit” as recited in the preamble of claim 1.

FIG. 9



(*Id.*, FIG. 9 (annotated); Ex. 1002, ¶182.) *Kochi* explains that “the circuit in a broken-lined frame is same as that shown in FIG. 8.” (Ex. 1010, 5:66-67.) In addition, apparatus 110 includes “a voltage supply unit 113 such as a battery, a voltage conversion circuit 114 for converting the voltage of the voltage supply unit 114 into a desired voltage, variable resistors 115, 116, a power supply voltage input terminal 112 for entering a voltage for driving the solid state image pickup apparatus, and an input terminal 111 for entering a voltage for driving the transferring MOS transistor 102” (collectively, “variable voltage circuitry”). (*Id.*, 6:10-16.) While figure 9 only shows the vertical shift register 103 and one pixel, *Kochi* makes clear

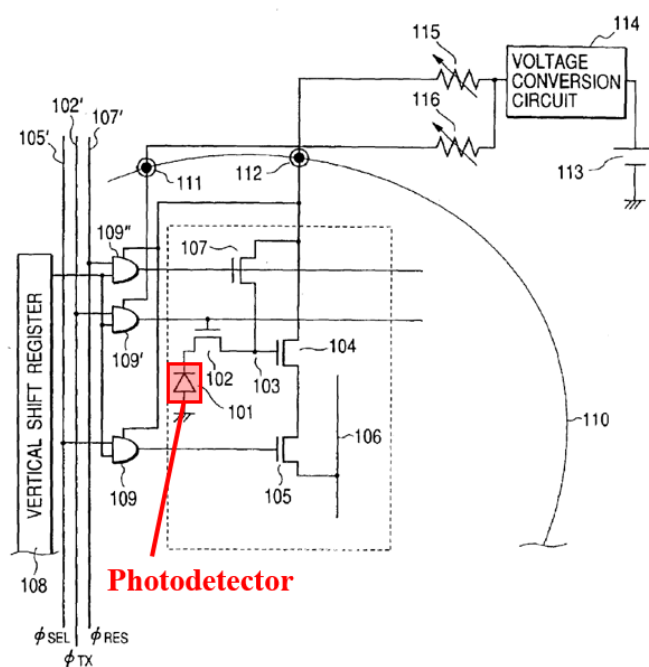
that apparatus 110 includes other pixels and a horizontal shift register. (*Id.*, 5:63-65; Ex. 1002, ¶183.)

Accordingly, *Kochi* discloses an “image sensor integrated circuit,” as claimed.
(*Id.*, ¶184; *infra* Section IX.G(b)-(h).)

b) 1(b)

Kochi discloses this limitation. (Ex. 1002, ¶¶185-86.) As discussed above, while figure 9 only shows one example pixel, apparatus 110 includes a plurality of pixels. (Ex. 1010, 5:63-65.) As shown in annotated figure 9 below, each pixel includes a photodiode 101 (*Id.*, 4:65-66, 5:66-67, FIGs. 8-9), which is a “photodetector” as claimed (“plurality of photodetectors”). (Ex. 1001, 2:13-14.)

FIG. 9

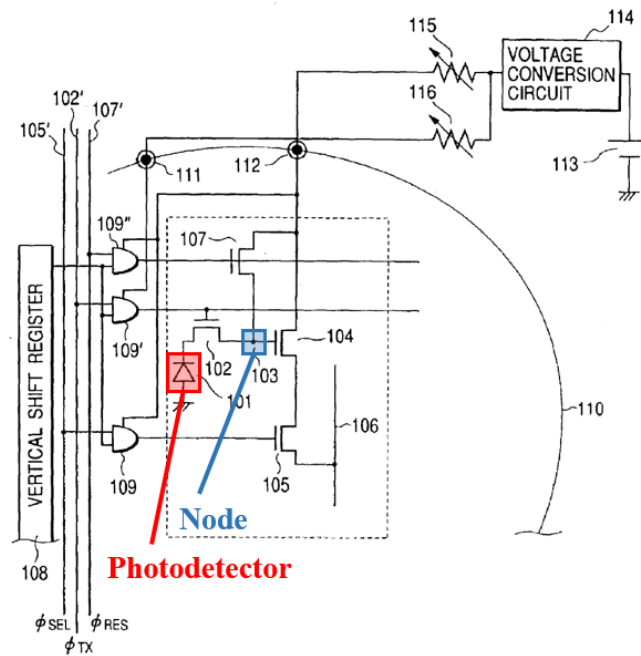


(Ex. 1010, FIG. 9 (annotated); Ex. 1002, ¶185.) *Kochi* explains that each “photodiode 101 accumulates a photo-induced charge which is transferred by a transfer switch 102” (“generating electrons excited by incident photons”). (Ex. 1010, 4:65-66; *see also id.*, 4:40-43; Ex. 1002, ¶186.)

c) 1(c)

Kochi discloses this limitation. (Ex. 1002, ¶187.) *Kochi* explains that “photodiode 101 accumulates a photo-induced charge which is transferred by a transfer switch 102, and the transferred photo-induced charge is **temporarily stored in a floating diffusion area 103.**” (Ex. 1010, 4:65-5:3.) As shown in annotated figure 9 below, each pixel includes such a floating diffusion area 103 (“plurality of nodes”), which is a “corresponding node” to photodiode 101 (“photodetector”) for that pixel of the plurality of pixels (“wherein each of the plurality of photodetectors has a corresponding node of the plurality of nodes”). (*Id.*, 4:65-5:8.)

FIG. 9

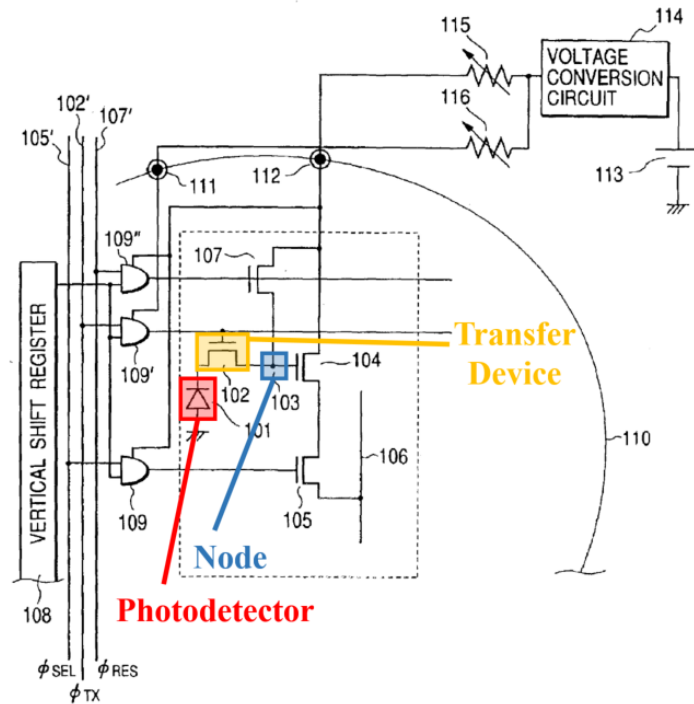


(*Id.*, FIG. 9 (annotated); Ex. 1002, ¶187.)

d) 1(d)

Kochi discloses this limitation. (Ex. 1002, ¶¶188-90.) As shown in annotated figure 9 below, each pixel of the plurality of pixels includes a transfer switch 102 (“a plurality of transfer devices”). (Ex. 1010, 4:65-5:8.)

FIG. 9



(*Id.*, FIG. 9 (annotated); Ex. 1002, ¶188.) As *Kochi* explains, when transfer switch 102 is turned off, “a photo-induced charge is accumulated in the photodiode...according to the amount of incident light.” (Ex. 1010, 4:40-43.) When transfer switch 102 is turned on, “the photo-induced charge is transferred from the photodiode...to the floating diffusion area.” (*Id.*, 4:43-58, FIGs. 6A-B.) The on/off state of transfer switch 102 is controlled by the voltage provided to the input terminal 111, which “driv[es] the transferring MOS transistor 102.” (*Id.*, 6:10-16.) The terminal 111 provides a voltage to the AND gate 109', which, in turn, drives the gate of the transfer device 102 such that the voltage applied to the gate of the transfer device 102 is determined by the voltage on terminal 111. (*Id.*, 6:2-4 (disclosing

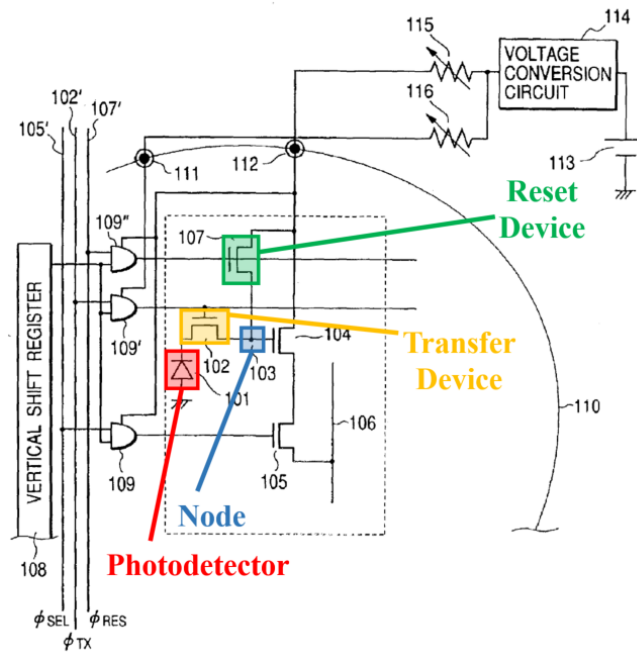
AND gate 109 “having two input/output terminals and an **electric power source terminal for driving the AND circuit.**”), 6:4-7 (“[O]nce high voltage is applied to both two input terminals, **a voltage value of the electric power source voltage for driving of the AND circuit is output from the output terminal.**”); 6:21-24 (“AND circuit 109 outputs the voltage value input from the terminal 112”).)

Thus, *Kochi* discloses a plurality of pixels, each including a transfer switch 102 (“plurality of transfer devices”) “controlling the transfer of the electrons from [photodiode 101] to the corresponding [floating diffusion area 103], the transfer depending on a control signal applied to [transfer switch 102]” via input terminal 111. (Ex. 1002, ¶¶188-90.)

e) 1(e)

Kochi discloses this limitation. (Ex. 1002, ¶¶191-93.) As shown in annotated figure 9 below, each pixel of the plurality of pixels includes a resetting MOS transistor 107 (“plurality of reset devices”). (Ex. 1010, 5:4-8.)

FIG. 9



(*Id.*, FIG. 9 (annotated); Ex. 1002, ¶191.) *Kochi* discloses that “floating diffusion area 103 is connected to a power source through a **resetting MOS transistor 107**, and, in the resetting operation by the application of a voltage of 5V to the gate thereof, the floating diffusion area 103 is reset to a potential of $5V - V_{th}$.” (Ex. 1010, 5:4-8; *see also id.*, 4:43-44 (“The floating diffusion area 11 is **reset by turning on the reset gate 12.**”).)

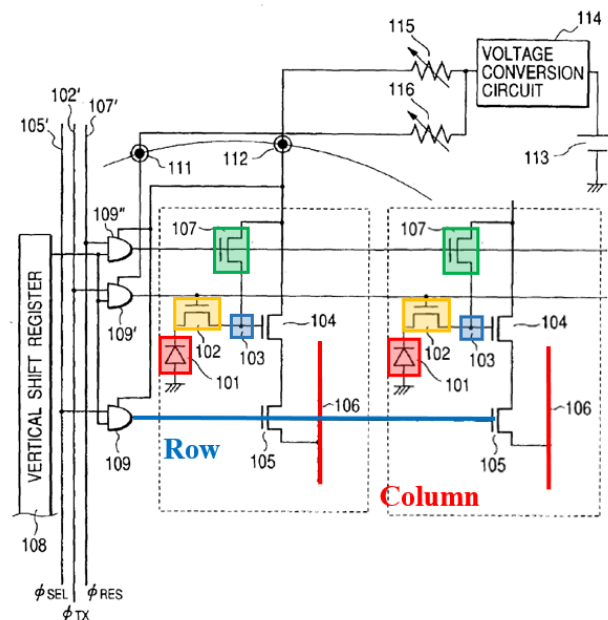
Thus, *Kochi* discloses a plurality of pixels, each including a resetting MOS transistor 107 connecting floating diffusion area 103 to a power source, wherein the floating diffusion area 103 is reset to a potential of $5V - V_{TH}$ when resetting MOS transistor 107 is turned on (“a plurality of reset devices, wherein each of the plurality

of nodes has a corresponding reset device of the plurality of reset devices, and said each of the plurality of nodes is reset when the corresponding reset device is active”). (Ex. 1002, ¶¶191-93.)

f) 1(f)

Kochi discloses this limitation. (Ex. 1002, ¶¶194-97.) For instance, as shown in a demonstrative based on figure 9 below, *Kochi*'s apparatus includes vertical shift register 108 coupled to, *inter alia*, AND circuit 109 that corresponds to a row of pixels and an output line 106 that corresponds to a column of pixels ("row and column circuitry"). (Ex. 1010, 5:4-8.)

FIG. 9



(*Id.*, FIG. 9 (annotated); Ex. 1002, ¶194.) *Kochi* discloses that “the transferred photo-induced charge...stored in a floating diffusion area 103, amplified by a source

follower MOS transistor 104 and is **read out by a vertical selecting MOS transistor 105 to an output line 106.**” (Ex. 1010, 4:65-5:3.)

Each vertical selecting MOS transistor 105 is coupled to an AND gate 109 “having two input/output terminals and an electric power source terminal for driving the AND circuit.” (*Id.*, 6:2-4.) “Once high voltage is applied to both two input terminals, a voltage value of the electric power source voltage for driving of the AND circuit is output from the output terminal.” (*Id.*, 6:4-7.) Signal line 105’ supplies pulse ϕ_{sel} to turn on and off vertical selecting MOS transistor 105. (*Id.*, 6:14-20.) Thus, when “a pulse is applied from the vertical shift register 108” and pulse ϕ_{sel} is applied from signal line 105’, “AND circuit 109 outputs the voltage value input from the terminal 112,” turning on vertical selecting MOS transistor 105 (*id.*, 6:20-29), thereby reading out the transferred photo-induced charge stored in a floating diffusion area 103 to output line 106 (*id.*, 4:65-5:3). (*Id.*, 4:65-5:8, 6:20-29; Ex. 1002, ¶¶195-96.)

As shown in demonstrative above, the output from AND circuit 109 is applied to all pixels in the same row, which causes each pixel to readout the amplified photo-induced charge stored in floating diffusion area 103 to a respective output line 106 corresponding to the column of the pixel. (Ex. 1002, ¶197; *infra* Section IX.G.1(g).)

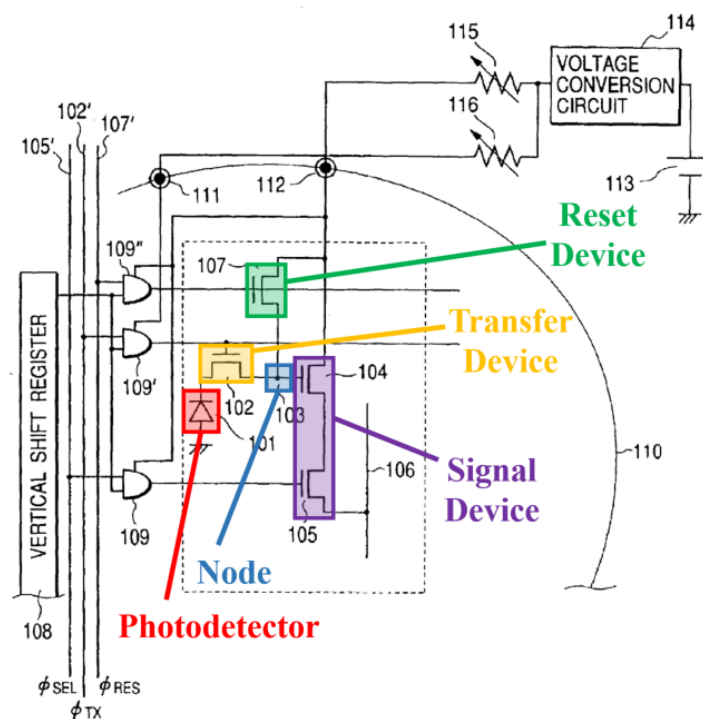
Indeed, the accessing of pixels in such a manner using the associated row and column circuitry was well known in the art. (Ex. 1014¹³, 9:41-60; Ex. 1002, ¶197.)

g) 1(g)

Kochi discloses this limitation. (Ex. 1002, ¶¶198-99.) As discussed above, figure 9 only shows one of the plurality of pixels that are included in apparatus 110. (*Id.*, 5:63-65.) As shown in annotated figure 9 below, each pixel includes a source follower MOS transistor 104 and vertical selecting MOS transistor 105 (collectively, “signal device”). (Ex. 1010, 4:65-5:3.) The understanding that source follower MOS transistor 104 and vertical selecting MOS transistor 105 together form a single “signal device” for each pixel is consistent with the language of claim 11 of the ’671 patent. (Ex. 1001, claim 11; *infra* Section IX.G.3.)

¹³ *Rhodes-647* demonstrates the knowledge of a POSITA at the relevant time.

FIG. 9



(Ex. 1010, FIG. 9 (annotated); Ex. 1002, ¶¶198.) For each of the plurality of pixels, the vertical selecting MOS transistor 105 is coupled to AND circuit 109 which selects the row of pixels, coupled to the output line 106 that corresponds to the column for the pixel, (*supra* Section IX.G.1(f)), and also coupled to the source follower MOS transistor 104, which in turn is coupled to floating diffusion area 103 (“node”) (“a plurality of signal devices coupling the plurality of nodes to the row and column circuitry”). (Ex. 1010, FIG. 9.) *Kochi* explains that “the transferred photo-induced charge...stored in a floating diffusion area 103, amplified by a source

follower MOS transistor 104 and is **read out by a vertical selecting MOS transistor 105 to an output line 106.**” (*Id.*, 4:65-5:3; Ex. 1002, ¶¶198-99.)

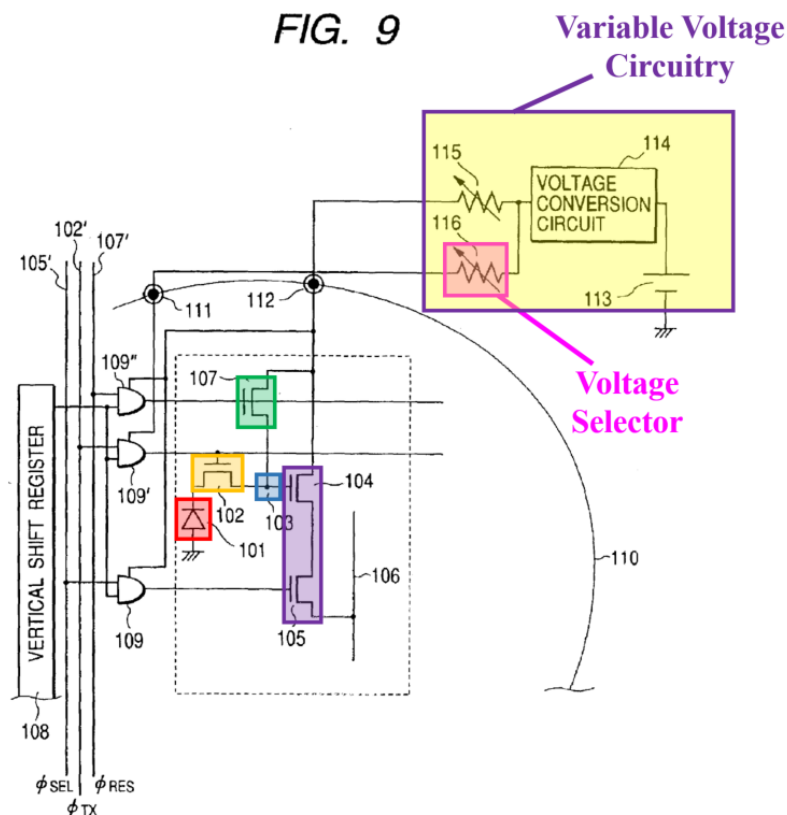
h) 1(h)

Kochi discloses this limitation. (Ex. 1002, ¶¶200-202.) For instance, as shown in Figure 9 (reproduced below), *Kochi*’s apparatus 110 includes a voltage supply unit 113, a voltage conversion circuit 114, and variable resistors 115, 116 (collectively, “variable voltage circuitry”):

[A] voltage supply unit 113 such as a battery, a voltage conversion circuit 114 for converting the voltage of the voltage supply unit 114 into a desired voltage, variable resistors 115, 116, a power supply voltage input terminal 112 for entering a voltage for driving the solid state image pickup apparatus, and an input terminal 111 for entering a voltage for driving the transferring MOS transistor 102.

(Ex. 1010, 6:9-16.)

FIG. 9



(*Id.*, FIG. 9 (annotated); Ex. 1002, ¶200.) As *Kochi* explains, voltage conversion circuit 114 “convert[s] the voltage of the voltage supply unit 114 into a desired voltage.” (Ex. 1010, 6:9-16.) *Kochi* further explains that “the voltage at the input terminal 111 can be made different, by the variable resistor 116.” (*Id.*, 6:39-41.) Thus, the voltage at input terminal 111 (“voltage of the control signal”) applied to transfer switch 102 is determined by voltage conversion circuit 114 and variable resistor 116 (“voltage selector”). (*Id.*, 6:14-16 (“[I]nput terminal 111 for entering a voltage for driving the transferring MOS transistor 102.”); *supra* Section IX.G.1(d).)

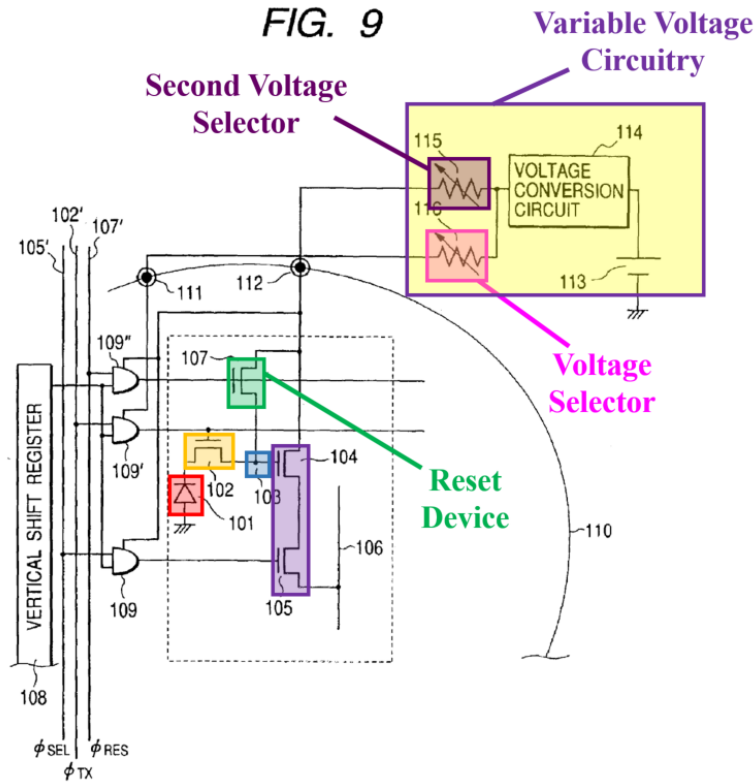
Accordingly, *Kochi* discloses a voltage supply unit 113, a voltage conversion circuit 114, and variable resistors 115, 116, (collectively, “variable voltage

circuitry”), wherein variable resistor 116 (“voltage selector”) determines the voltage at input terminal 111 (“control voltage of the control signal”) applied to transferring MOS transistor 102 (transfer device”). (Ex. 1002, ¶¶200-202.)

2. Claim 4

- a) The circuit of claim 1, wherein the variable voltage circuitry includes a second voltage selector determining a second control voltage of a second control signal applied to the plurality of reset devices.**

Kochi discloses this limitation. (Ex. 1002, ¶¶203-205.) As discussed above in Section IX.G.1(h), *Kochi* discloses the claimed “variable voltage circuitry” that includes the variable resistor 116 (“voltage selector”) for determining the voltage at input terminal 111 applied to transfer switch 102 (“control voltage of the control signal applied to the plurality of transfer devices”). (*Supra* Section IX.G.1(h).) As shown in annotated figure 9 below, *Kochi*’s apparatus 110 further includes variable resistor 115 (“second voltage selector”) for determining the voltage at the power supply voltage input terminal 112 (“second control voltage of a second control signal”) that is applied to, *inter alia*, the resetting MOS transistor 107 for each pixel (“plurality of reset devices”).



(Ex. 1010, FIG. 9 (annotated); Ex. 1002, ¶203.) The voltage at power supply voltage input terminal 112 is determined by voltage conversion circuit 114 and variable resistor 115 (“second voltage selector”), and applied to, *inter alia*, resetting MOS transistor 107. (Ex. 1010, 6:10-15, FIG. 9.) As *Kochi* explains, “[a]s the voltage at the input terminal 111 can be made different, by the variable resistor 116, from the voltage at the power supply voltage input terminal 112...the pulse voltage for driving the transferring MOS transistor 102 can be adjusted independently from the pulse voltage for driving the resetting MOS transistor 107.” (*Id.*, 6:38-46.)

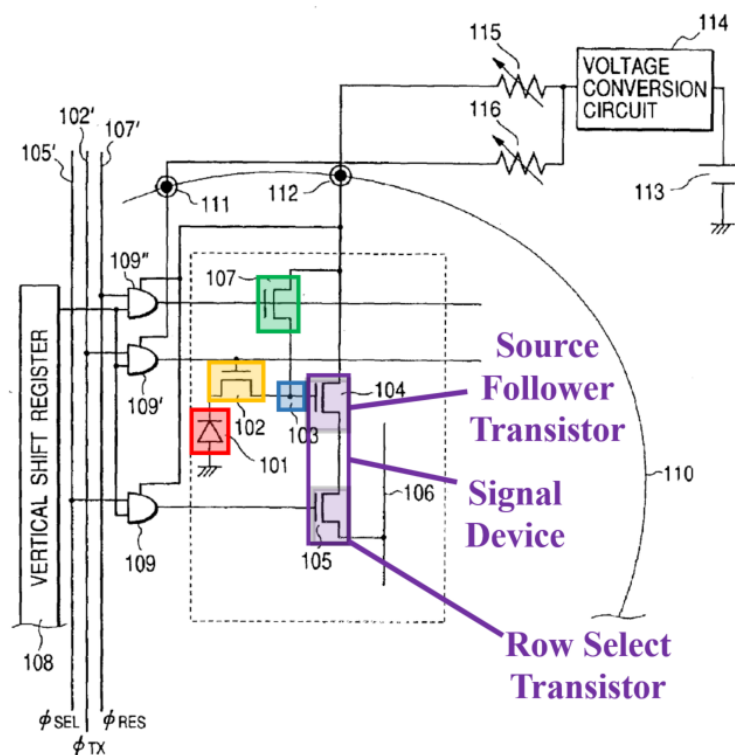
Thus, *Kochi* discloses a second variable resistor 115 (“second voltage selector”) determining the voltage at power supply voltage input terminal 112 (“a

second control voltage of a second control signal”) applied to resetting MOS transistor 107 (“reset device”). (Ex. 1002, ¶¶203-205; *supra* Section IX.F.1(h).)

3. Claim 11

Kochi discloses this limitation. (Ex. 1002, ¶¶206-207.) As discussed in Section IX.G.1(g), each pixel of *Kochi*'s apparatus 110 includes source follower MOS transistor 104 and vertical selecting MOS transistor 105 (collectively, "signal device"). (Ex. 1010, 4:65-5:3; *supra* Section IX.G.1(g).)

FIG. 9



(Ex. 1010, FIG. 9 (annotated); Ex. 1002, ¶206.)

As shown in annotated figure 9 above, each vertical selecting MOS transistor 105 (“row select transistor”) is coupled to AND circuit 109 and output line 106, which are part of the “row and column circuitry” for the image pickup device. (Ex. 1010, 4:65-5:3, FIG. 9; *supra* Section IX.G.1(f).) Additionally, each source follower MOS transistor 104 is coupled to the floating diffusion area 103 (“node”) for the corresponding pixel. (Ex. 1010, 4:65-5:3, FIG. 9.) Therefore, the apparatus 110, which includes a plurality of pixels with each having a corresponding signal device, includes “a plurality of row select transistors coupled to the row and column circuitry and a plurality of source follower transistors coupled to the plurality of nodes” as recited in claim 11. (Ex. 1002, ¶207.)

4. Claim 12

Kochi discloses this limitation. (Ex. 1002, ¶208.) As discussed in Section IX.G.1(b), each pixel in *Kochi*’s apparatus 110 includes photodiode 101. (Ex. 1010, 4:65-66.)

H. Ground 8: Claims 14, 17, 24, and 25 are Obvious in View of *Kochi*¹⁴

1. Claim 14

As discussed above in Section IX.B.2, claim 14 recites “a computer readable medium containing a description of an image sensor integrated circuit comprising” the limitations of claim 1. As further discussed above in Section IX.B.2, the creation of a “computer-readable description of an image sensor integrated circuit,” such as the integrated circuit disclosed in *Kochi*, was well known in the art and obvious to a POSITA. (Ex. 1002, ¶209; *supra* Section IX.B.2.) As discussed in Section IX.G.1, *Kochi* discloses an image sensor integrated circuit as recited in claim 1. Accordingly, *Kochi* discloses or suggests all of the features of claim 14 for the same reasons discussed above in Sections IX.B.2 and IX.G.1. (Ex. 1002, ¶¶209-210; *supra* Sections IX.B.2 and IX.G.1.)

¹⁴ Petitioner does not repeat the language of claims 24-25, which are provided above in Ground 2.

2. Claim 17

- a) **The computer readable medium of claim 14, wherein the variable voltage circuitry includes a second voltage selector determining a second control voltage of a second control signal applied to the plurality of reset devices.**

Kochi discloses or suggests this limitation for the same reasons discussed above in Sections IX.G.2 and IX.H.1. (Ex. 1002, ¶211.)

3. Claim 24

Kochi discloses or suggests these limitations for the same reasons discussed above in Sections IX.G.3 and IX.H.1. (Ex. 1002, ¶212.)

4. Claim 25

Kochi discloses or suggests this limitation for the same reasons discussed above in Sections IX.G.4 and IX.H.1. (Ex. 1002, ¶213.)

X. INSTITUTION IS APPROPRIATE HERE

The Board's decision in *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (Sept. 12, 2018) (precedential), does not apply here, because an evaluation of the six factors under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential), favor institution. As discussed below, while the '671 patent is involved in an ITC investigation, Petitioner diligently filed this Petition less than two months after institution of the ITC investigation, the ITC involves different evidentiary standards and burdens, and—most importantly—the ITC cannot invalidate a patent.¹⁵ Accordingly, the Board should institute IPR based on the Petition, which presents strong arguments for unpatentability.

The **first factor (stay)** is neutral, because the ITC favors suspension of remedial orders that conflict with an IPR decision (e.g., issued near the end of an ITC investigation) over staying investigations at the onset. *See In the Matter of Certain Unmanned Aerial Vehicles and Components Thereof*, ITC-337-TA-1133, 2020 WL 5407477, at *1, *20-*22 (ITC Sept. 8, 2020).

¹⁵ Whether *NHK Spring* and *Fintiv* should apply to an ITC investigation was recently raised in a request for rehearing by the Board and the Precedential Opinion Panel in *Garmin Int'l, Inc. v. Koninklijke Philips N.V.*, IPR2020-00754, Paper 12 (Nov. 19, 2020).

The **second factor (proximity of trial)** is neutral, if not slightly for granting institution, because of Petitioner’s diligence in filing the Petition. First, Petitioner filed its Petition *less than two months* after institution of the ITC investigation.¹⁶ (Ex. 1018, 2.)

Second, the Board’s institution decision will likely issue around July 2021, which is before the ITC’s initial determination set for December 1, 2021 (Ex. 1023, 3). And, while the investigation hearing is set for August 16-20, 2021 (Ex. 1022, 1; Ex. 1023, 4) and the target completion date is set for April 1, 2022 (Ex. 1021, 2), those dates are “subject to change because of restrictions and uncertainty due to the COVID-19 pandemic” (*id.*, 2; Ex. 1022, 2). Indeed, the ITC has recently delayed a significant number of investigations in which a violation was found. (*See, e.g.*, Ex. 1024.)

Third, the hearing before the ALJ is merely the initial step in the ITC’s decisional process. *See* 19 C.F.R. § 210.36(a). The ALJ’s initial determination is subject to a review by the full Commission, which must issue a final determination. *Id.* §§ 210.43(d), 210.45-46. Additionally, if the Commission finds a violation, it must “transmit” a copy of its final determination and recommended actions (together

¹⁶ PO amended its complaint on October 23, 2020, and further supplemented it in November 2020. (Ex. 1018.)

with the full record) to the President, *see* 19 U.S.C. § 1337(j)(1)(B), and only upon the President's approval or the expiration of the 60-day presidential review period would the ITC's final determination become final (and subject to appeal), *see id.* § 1337(j)(4). Thus, even though the target completion date in the ITC Investigation is set to predate the Board's final written decision, the ultimate completion of the investigation will occur closer to and possibly after the Board's final written decision (per typical Commission extensions).

The **third factor (investment)** weighs in favor of institution. To date, the ITC investigation is in its infancy and thus the Commission and parties have not yet invested substantial resources. (Ex. 1023, 2; Ex. 1017.) While activity in the investigation will subsequently increase at a pace typical of ITC actions, Samsung's diligence in filing this Petition—*less than two months after investigation institution*—weighs against discretionary denial. (Ex. 1018, 2.) *See Philip Morris Prods., S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00919, Paper 9 at 10 (Nov. 16, 2020); *Fintiv*, Paper 11 at 11. Concluding otherwise would mean that this factor would always weigh against institution when there is a parallel ITC investigation because such investigations always require a rapid investment of resources at the outset.

The **fourth factor (overlap)** weighs strongly in favor of institution. The ITC investigation does “not render [this] proceeding duplicative or...a waste of the Board’s resources,” because the ITC involves “differen[t]...evidentiary standards and burdens” and “does not have the authority to invalidate a patent.” *Samsung Elecs. Co., Ltd. v. BitMicro, LLC*, IPR2018-01410, Paper 14 at 18 (Jan. 23, 2019); *see also Bio-Tech. Gen. Corp. v. Genentech, Inc.*, 80 F.3d 1553, 1564 (Fed. Cir. 1996) (The ITC cannot “set aside a patent as being invalid [and/or] render it unenforceable.”). Indeed, even if the ITC finds any of the challenged claims invalid, PO can still assert those claims in district court. *See Renesas Elecs. Corp. v. Broadcom Corp.*, IPR2019-01040, Paper 9 at 7-8 (Nov. 13, 2019). That PO’s predecessor unsuccessfully sued Samsung on invalid patents in the recent past strongly suggests it may do so again here. *See Imperium IP Holdings (Cayman) Ltd. v. Samsung Electronics Co., Ltd.*, 757 Fed. Appx. 974, 980 (Fed. Cir. 2019).

The **sixth factor (other circumstances)** likewise weighs strongly in favor of institution. As demonstrated above (*supra* Section IX), the Petition presents strong arguments for unpatentability of the challenged claims. *See Dynamics*, Paper 11 at 14 (finding the “merits of the case weigh in favor” of institution). Thus, institution is consistent with the significant public interest against “leaving bad patents enforceable.” *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020). Indeed, this Petition is the *sole* challenge to the ’671 patent before the Board—a

“crucial fact” favoring institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (May 12, 2020). And there is currently no district court litigation to serve as an alternative forum that can issue a binding decision on the validity of the ’671 patent.

Accordingly, based on a “holistic view of whether efficiency and integrity of the system are best served,” the facts here weigh against exercising discretion under § 314(a) to deny institution. *Dynamics*, Paper No. 11 at 15. While factor 5 (parties) usually weighs against institution, the remaining factors are at least neutral (factors 1 and 2) or favor institution (factors 3, 4, and 6). Plus, the fact that this proceeding is not duplicative or a waste of the Board’s resources (factor 4) and the strength of Petitioner’s unpatentability positions (factor 6) outweigh other applicable factors, such as if the ITC investigation concludes before the final written decision is issued in this proceeding (factor 2) or if there were great investment in the ITC investigation (factor 3)—which typically occur when there is a parallel ITC investigation. *See 3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12 at 33-34 (May 26, 2020). Thus, institution here is proper.

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-26 of the '671 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: January 19, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,323,671 contains, as measured by the word-processing system used to prepare this paper, 13,939 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: January 19, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on January 19, 2021, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,323,671 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)