UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL CORPORATION,
WESTERN DIGITAL TECHNOLOGIES, INC., AND SANDISK, LLC

Petitioners

v.

Martin Kuster

Patent Owner.

Inter Partes Review No. IPR2020-01391

U.S. Patent No. 8,693,206

PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 8,693,206 PURSUANT TO 35 U.S.C. §§ 311-319, 37 C.F.R. § 42

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Petitioners Western Digital Corporation ("WDC"), Western Digital Technologies, Inc. ("WDT") and SanDisk, LLC ("SanDisk") ("Petitioners") respectfully request *inter partes* review ("IPR") in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.* of claims 1-19 of U.S. Patent No. 8,693,206 ("the '206") ("Challenged Claims").

I. INTRODUCTION

The '206 claims well-known prior art mechanical designs for connectors on "external storage devices" such as USB flash drives. The '206 purports to have innovated USB connectors compatible with both the USB 2.0 and USB 3.0 protocols. But the USB 3.0 standard, which issued years earlier, mandates that USB 3.0 connectors be backward-compatible with USB 2.0 and describes in detail the connector design necessary to support both protocols.

The '206's alleged "innovation," involves nothing more than providing the two tiers of connector contacts required by the USB 3.0 standard, and arranging them exactly as taught by the standard and a host of other prior art references.

The '206 does not teach anything new about the device's dimensions, electronics, or manufacturing. The '206 claims lack any inventive features. This is underscored by He (Ex. 1011), Chen (Ex. 1010) and Hsiao (Ex. 1009)[1], prior art

[1] The Exhibit List is attached as Appendix B.

references disclosing USB drives having connectors identical to those claimed in the ’206, in addition to the other references cited herein.

Petitioners respectfully request that IPR be instituted and the Challenged Claims be canceled as unpatentable.

II. MANDATORY NOTICES (37 C.F.R. § 42.8(b))

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioners WDC, WDT and SanDisk are the real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The ’206 was the subject of a civil action in *Kuster v. Western Digital Corporation,* Case No. 3:20-cv-01089, filed in the U.S. District Court for the Northern District of Texas, Dallas Division, which was dismissed by Patent Owner. The ’206 is the subject of a civil action in *Kuster v. Western Digital Technologies, Inc.*, Case No. 6:20-cv-00563 ADA, filed June 24, 2020 and currently pending in the U.S. District Court for the Western District of Texas (Waco) (“the Litigation”).

Petitioners are filing concurrently herewith an IPR Petition – IPR 2020-01410 – for U.S. Patent No. 8,705,243, the parent of the ’206.

C. Lead and Backup Counsel (37 C.F.R. § 42.8(b)(3))

Petitioners provide the following designation of counsel:

Lead Counsel	Backup Counsel
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D. Service Information (37 C.F.R. § 42.8(b)(4))

Please address all correspondence and service to lead counsel and back-up counsel at the addresses listed above. Petitioners consent to electronic service by email to EricaWilson@walterswilson.com, Eric@walterswilson.com.

III. IPR REQUIREMENTS (37 C.F.R. § 42.104)

A. Standing (37 C.F.R. § 42.104(a))

Petitioners certify: (1) the '206 is available for IPR; and (2) Petitioners are not barred or estopped from requesting IPR of the Challenged Claims. The '206 issued April 8, 2014, and this Petition is being filed within one year of service of Complaints against Petitioners alleging infringement of the '206 (*see* Section II.B.) and is not barred under 35 U.S.C. § 315(b).

B. Challenge Under 37 C.F.R. § 42.104(b)

Petitioners request IPR of the Challenged Claims on the grounds listed below. [2]

Ground	Claims	Basis[3]
1. He-Cheng	1-5, 8-11, 13-15, 18-19	35 U.S.C. § 103
2. He-Cheng-Hiller	6-7, 16-17	35 U.S.C. § 103
3. He-Sun	1-11, 13-19	35 U.S.C. § 103
4. Hsiao	11-12	35 U.S.C. § 102
5. Hsiao	11-12	35 U.S.C. § 103
6. Hsiao-Sun	11-12	35 U.S.C. § 103
7. Chen-Cheng	11-12, 14-15, 18	35 U.S.C. § 103
8. Chen-Cheng-Hiller	16, 17	35 U.S.C. § 103

[2] For some claims Petitioner relies on alternative grounds of invalidity since some art is § 102(e) prior art and potentially could be antedated.

[3] The '206 is a pre-AIA patent; all references to the United States Code are to pre-AIA versions.

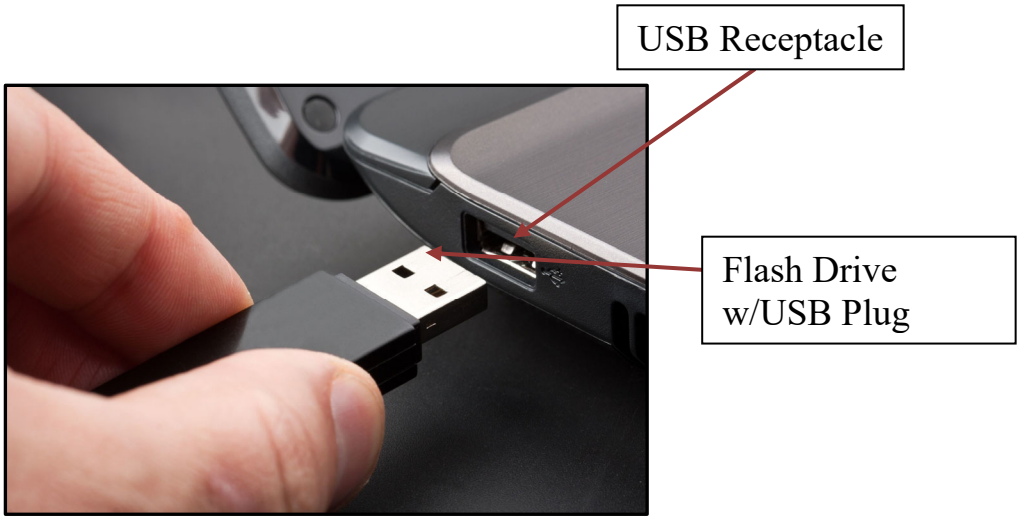
9. Chen-Cheng-Wan	19	35 U.S.C. § 103

IV. STATE OF THE ART

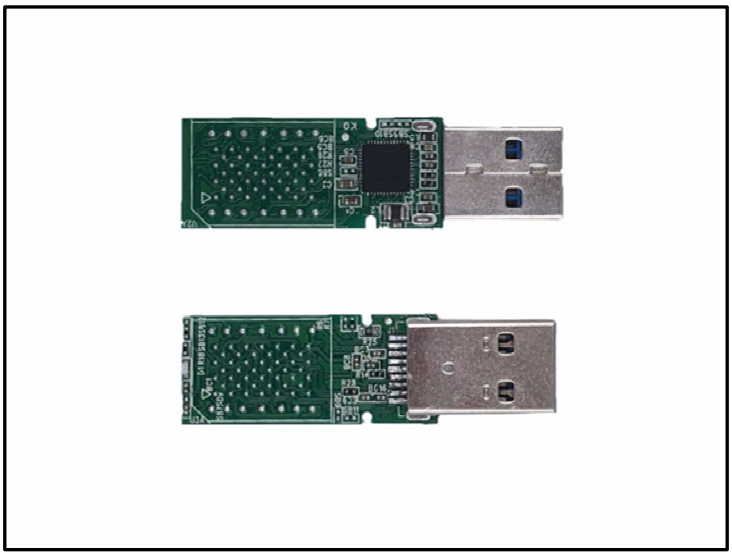
The '206 is directed to connectors for "external storage device[s]," such as Universal Serial Bus ("USB") flash drives (termed "USB sticks") having multiple interfaces, thus allowing them to be connected to more than one type of receptacle—e.g., USB 2.0 and USB 3.0 receptacles. Ex. 1001, 1:23-24, 1:28-33, 1:65-2:2, 2:30-32, 4:21-23.

A. USB Flash Drives

USB flash drives are data storage devices having USB connection interfaces. Their primary components are memory for data storage, a controller communicating with memory to manage read/write operations and ensure compliance with the USB protocol, and a plug that allows the device to be connected to a USB receptacle on a host device such as a laptop.



The memory, controller and plug connector are mounted on a substrate such as a printed circuit board ("PCB") as exemplified below:

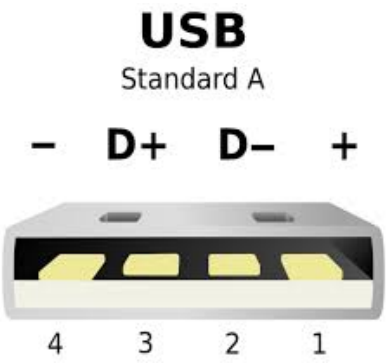


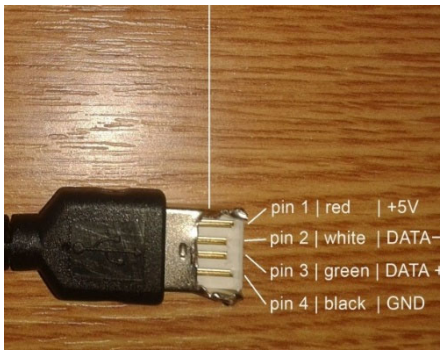
Ex. 1005, ¶¶ 49-52.

B. USB 2.0 and 3.0 Standards

The USB standard governs the design of USB connections. USB standards (termed "Specifications") are issued by the USB Implementers Forum ("USB-IF") which promulgated the USB 2.0 and USB 3.0 Specifications in 2000 and 2008, respectively. Ex. 1001, 1:38-45; Ex. 1019, ¶¶ 1-10.

Flash drive USB 2.0 connectors commonly conform to USB Standard-A, and have four non-resilient metal contacts that transfer power, ground and serial differential data D+ and D- signals. These contacts (often called "fingers") are embedded in an insulative housing or directly on a PCB or other substrate.



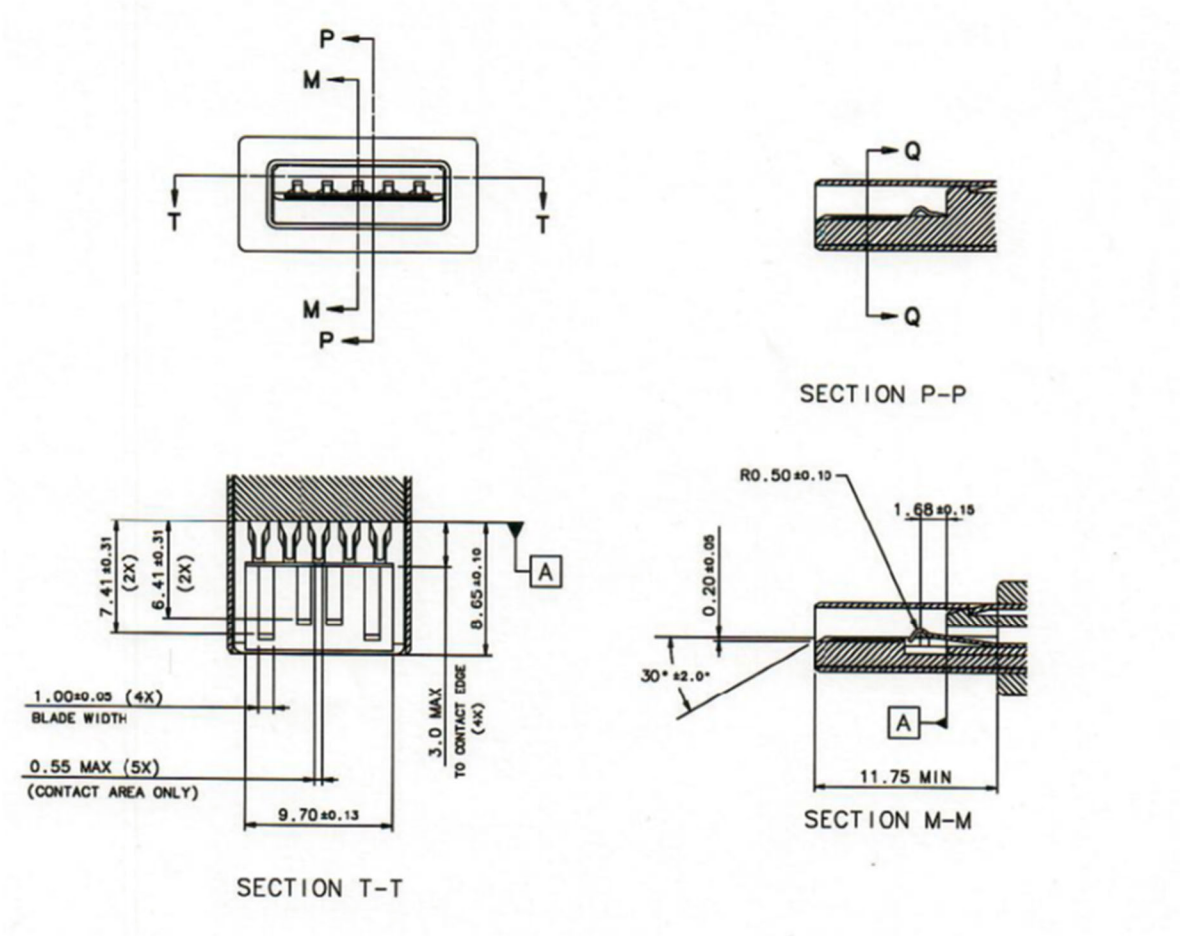


Ex. 1005, ¶¶ 59-61.

USB 2.0 supports three bus speeds, and USB 3.0 supports a fourth, faster bus speed termed "SuperSpeed." Ex. 1001, 1:36-53. The USB 3.0 Specification defines a dual-bus architecture with two physical buses—the USB 2.0 bus and the USB 3.0 SuperSpeed bus—operating in parallel. Ex. 1008, Section 3.1, Fig. 3-1; Ex. 1005, ¶ 62.

The USB 3.0 Specification identifies backward compatibility as a "key design area[]" (Ex. 1008, Section 1.6), and requires USB 3.0 devices to be backward compatible with USB 2.0. *Id.* at 3-1. A USB 3.0 Standard-A compliant plug must fit both USB 2.0 and USB 3.0 receptacles. *Id.*, Section 5.2.1.1 and Table 5-1; Ex. 1005, ¶¶ 63-64.

Accordingly, USB 3.0 Standard-A plugs have the same form factor and the same four metal contacts as USB 2.0 Standard-A plugs. Ex. 1008, Section 5.3.1.1. To support SuperSpeed, the USB 3.0 Specification adds five resilient contacts—two signal pairs (denoted StdA_SSTX-, StdA_SSTX+ and StdA_SSRX-, StdA_SSRX+) and a grounding contact. *Id.* at 5-14; *id*, Section 5.3.1.2 and Table 5-2. The contacts are arranged in a two-tier configuration with the "SuperSpeed" contacts sitting behind USB 2.0 contacts with a portion of the SuperSpeed contacts above the USB 2.0 contacts. *Id.* at 5-4, Section 5.3.1; *see also id.*, Fig. 5-2 (showing two-tier contact arrangement) (excerpt below):



See Ex. 1005, ¶¶ 65-68.

C. Chip-on-Board ("COB") Technology

Prior art flash drives commonly used COB technology to mount components such as controllers and memory on a substrate because it permits miniaturization of the flash drive. With COB, components such as memory dies are wired and bonded to a substrate (*e.g.,* a PCB), without first being encapsulated by electronic packaging. Ex. 1005, ¶ 72.

V. THE ’206 PATENT

The ’206 is directed to connectors for “external storage device[s]” such as “USB sticks” having multiple interfaces, thus allowing them to be connected to more than one type of receptacle—e.g., USB 2.0 and USB 3.0 receptacles. Ex. 1001, 1:23-24, 1:28-33, 1:65-2:2; 2:30-32, 4:21-23; Appendix A.[4]

The ’206 focuses on the connector’s mechanical interface, adopting the same two-tier contact arrangement as the USB 3.0 Standard-A Plug Specification. Appendix A, claims 1, 10 and 11.

The claimed storage devices include substrates having a “connection” surface and a “component” surface opposite the connection surface. Appendix A, claims 1[b], 10[b], 11[b]. The substrate may be a PCB “used to mechanically support and electrically connect the other components of the device **10**.” Ex. 1001, 4:32-35.

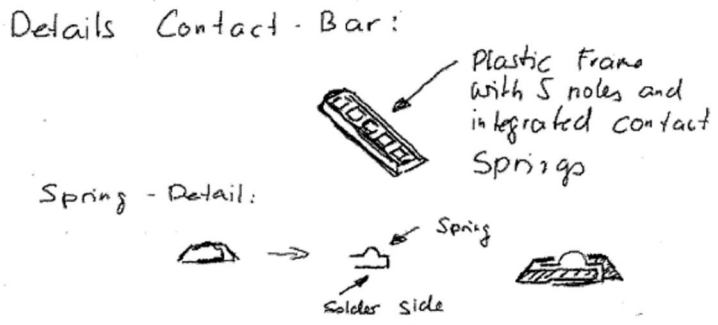
The ’206 calls one set of contacts “connection fingers,” which as depicted in the ’206, are the same as USB 2.0 contacts. *See, e.g.,* Ex. 1001, 4:62-66 (“connection fingers **20** may be configured to electrically couple” to USB 2.0 wires

[4] Appendix A hereto lists the ’206 claims. Elements of independent claims 1, 10 and 11 are labeled with letters for ease of reference.

of a "corresponding USB 2.0 connector"), Figs. 7-8 (item 20). The claims vary in the location of the connection fingers. *See* Appendix A.

The claims require a "contact bar" (comprising a second set of contacts) mounted on the substrate's "connection surface." The contact bar has portions of extensions (claims 1-10) or "portions that are electrically coupled with the substrate" (claims 11-19), that are a greater distance from the substrate surface than the connection fingers. Appendix A, claims 1, 10, 11, elements [e]-[f].

Provisional application 61/438,139, incorporated by reference into the '206 (Ex. 1001, 1:6-14), depicts a "Contact bar" as a "Plastic Frame with 5 holes and integrated contact springs:"



Ex. 1002 at 12.

At least one "memory die stack" is mounted on the substrate. Appendix A, 1[c], 10[c], 11[c]. The "stack" may have only one memory die. Ex. 1001, 3:19-32, 3:39-45, Figs. 16-19, 22-23 (depicting memory die stacks "having a single

die"), 8:36-38 (POSITA "will understand that the memory die stack **18** may include 1, 2, 4, or any suitable number of dies **64**").

The '206's dependent claims 3, 5-7 and 14-17 contain limitations regarding the placement of memory die stacks and the number of dies per stack. *See* Appendix A. A controller configured to access the memory is mounted on the substrate. Appendix A, claims 1[d], 10[d], 11[d].

See Ex. 1005, ¶¶ 73-83.

VI. THE '206 PROSECUTION HISTORY

The '206 issued April 8, 2014 from U.S. Patent Application No. 13/757,505, filed February 1, 2013 as a continuation of U.S. Patent Application No. 13/362,431 ("'431 Application"), filed January 31, 2012. The '431 Application claims priority to U.S. Provisional Applications Nos. 61/438,139 ("'139 Provisional") filed January 31, 2011 (Ex. 1002) and 61/442,379 ("'379 Provisional") filed February 14, 2011 (Ex. 1003) (collectively, "Provisionals"). Ex. 1001, face page, 1:6-14.

The Examiner found the as-filed claims were subject to a restriction/election requirement; he identified two claim groups and twenty species that he categorized by referencing figures in the application. Ex. 1004 at 113-18. Applicant provisionally elected to pursue "Group II" claims wherein "connection fingers" are "mounted on or embedded within the substrate," conditionally elected the Figure

35 species, and identified claims Applicant contended were generic to species identified by the Examiner. *Id.* at 101-104.

On July 16, 2013, the Examiner rejected the elected claims. He made no prior art rejections, but *inter alia* (1) made provisional double-patenting rejections over claims of the '431 Application; (2) rejected claims using the term "mounted on or embedded" as indefinite, finding it unclear "if the recited limitation is required (and) or is optional (or)"; and (3) rejected as indefinite claims referencing USB standards. *Id.* at 82-89.

On October 16, 2013, Applicant filed a Terminal Disclaimer with respect to the '431 Application, amended the claims to replace the phrase "mounted on or embedded within" with "embedded to be exposed upon," and amended claims to reference the USB 2.0 and USB 3.0 standards in effect as of January 31, 2011. *Id.* at 56-70.

On November 14, 2013, the Examiner issued a Notice of Allowance ("11-14-13 NOA"). *Id.* at 32-43. In his reasons for allowance, the Examiner focused on the connector arrangement claimed in the independent claims. *Id*. at 40-42.

Over two months later, on February 5, 2014, Applicant submitted a Supplemental Information Disclosure Statement ("SIDS") listing *inter alia* U.S. Patent No. 8,480,435 ("Hsiao") (Ex. 1009). *Id.* at 25-31. On February 14, 2014, Applicant paid the issue fee and requested the Examiner consider the SIDS and

issue a Supplemental NOA. *Id.* at 15-24. On March 10, 2014, the Examiner issued a Supplemental NOA stating simply that he had considered the references cited in the SIDS and "Claims 12-30 were still found allowable." *Id.* at 10-12. The '206 issued shortly thereafter.

VII. PETITIONERS' MAIN REFERENCES WERE NOT BEFORE THE EXAMINER

Petitioner relies on prior art combinations of (1) He (Ex. 1011) and Cheng (Ex. 1012) or He and Sun (Ex. 1014) and (2) Chen (Ex. 1010) and Cheng (Ex. 1012) or Chen and Sun to challenge the independent claims in this petition. This art was not before the Examiner during prosecution nor was the same or substantially the same art.

Petitioner also relies on Hsiao (Ex. 1009) and Hsiao and Sun to show that claims 11 and 12 are invalid. Applicant's eleventh-hour citation of Hsiao – months after the Examiner issued the 11-14-2013 NOA – should not dissuade the Board from instituting IPR. The Petition relies primarily on art that was not before the Examiner. Moreover, the Office materially erred by "overlooking specific teachings" of Hsiao that "impact patentability of" claims 11 and 12—*i.e.,* Figures 9-10 and accompanying disclosure in Hsiao's specification. *Advanced Bionics, LLC v. Med-El Elektromedizinische Gerate GMBH*, IPR2019-01469, Paper 6 at 7-9, n.9 (PTAB Feb. 13, 2020) (Precedential) (establishing § 325(d) analysis

"framework"); *see also Mylan Pharm., Inc. v. Merck Sharp & Dohme Corp.*, IPR2020-00040, Paper 21 at 17-20 (PTAB May 12, 2020) (refusing to decline to institute IPR under § 325(d) where Examiner "simply overlooked" relevant teachings of cited prior art); *Medacta USA, Inc., v. RSB Spine, LLC*, IPR2020-00264, Paper 24 at 18 (PTAB May 22, 2020) (same).

The Board considers "*Becton* factors" (c), (e) and (f) in assessing whether a petitioner has shown "material error." *Advanced Bionics,* IPR2019-01469, Paper 6 at 9-10, n. 10 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG,* IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017)). Analysis of these factors here shows the Office materially erred.

The Examiner provided no evaluation of Hsiao (or any art of record), made no rejections based on Hsiao, and, indeed, made no prior art rejections whatsoever. *See Becton* factor (c). Applicant disclosed Hsiao to the Office in a SIDS months after prosecution on the merits was completed and the 11-14-13 NOA issued. The Examiner's Supplemental NOA provides no explanation for the allowance of claims 11 and 12 over Hsiao. *See* Section VI.

As Sections XI.D and XI.E show, the Examiner's conclusion was erroneous. *See Becton* factor (e). Figures 9-10 of Hsiao and associated text teach a USB COB flash memory device having both USB 2.0 and USB 3.0 interfaces and a connector that is identical to that of claims 11 and 12. Hsiao discloses every feature the

Examiner stated in the 11-14-13 NOA was missing from the prior art of record. (Hsiao was not of record at the time.) *See* Ex. 1004 at 42; Section XI.D (explaining how Hsiao teaches these features); Ex. 1005, ¶¶ 90-92.

The Petition contains additional evidence not considered by the Examiner including the expert declaration of Dr. Baker (Ex. 1005), who explains in detail how Hsiao, alone or in combination with Sun (Ex. 1014), invalidates claims 11-12. *See Becton* factor (f).

Petitioner also provides Patent Owner's infringement contentions filed in the Litigation showing how Patent Owner applies the claims to the accused devices. Ex. 1016. These contentions underscore Hsiao's relevance because Hsiao's USB flash drive and connector design (Hsiao, Figs. 9-10) mimic that which Patent Owner now alleges infringes claims 11 and 12.

Significantly, the '206 claims are each shown to be invalid in view of art not previously before the Examiner. The Board should institute IPR.

VIII. THE BOARD SHOULD NOT DECLINE REVIEW UNDER SECTION 314(A)

Consideration of the *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (Precedential) factors favor institution here.

1. Factor 1: Potential For A Stay in District Court Is Neutral

Petitioner WDT intends to move for a stay of the Litigation if the Board institutes IPR. This factor is neutral because the district court's decision on WDT's motion will come after institution, and is "based on a variety of circumstances and facts beyond [the Board's] control and to which the Board is not privy." *See Sand Revolution II, LLC v. Continental Intermodal Group—Trucking, LLC*, IPR2019-01393, Paper 24 at 7 (PTAB Jun. 16, 2020) (Informative).

2. Factor 2: Lack Of A Trial Date Favors Institution

No trial date has been set in the Litigation, WDT has not yet answered and a case management conference has not been held. Even if the trial date is set before the Board issues its institution decision, trial dates in the Western District of Texas where the Litigation is pending are uncertain due to the COVID-19 pandemic. *See* Ex. 1020.

In contrast, the Board can adhere to the one-year statutory deadline prescribed by 35 U.S.C. § 316(a)(11), having converted to remote oral hearings early in the pandemic. *See Sand Revolution*, IPR2019-01393, Paper 24 at 9; Ex. 1021.

3. Factor 3: District Court's Minimal Investment In The Merits Of The Litigation Favors Institution

Petitioners filed this petition less than two months after Patent Owner filed the Litigation Complaint, and before Petitioner WDT filed its responsive pleading. The district court has invested no time in the merits of the Litigation. *See* Section II.B; *Apple Inc. v. Seven Networks, LLC*, IPR2020-00156, Paper No. 10 at 11 (PTAB Jun. 15, 2020) (finding diligence in filing petition where petition was filed four months before the § 315(b) statutory bar date).

4. Factor 4: Minimal Overlap Between Issues In This Proceeding And The Litigation Favors Institution

Petitioner WDT has not served invalidity contentions in the Litigation. However, the invalidity positions in the Litigation will be vastly different from the grounds submitted in this petition. The USB 3.0 Specification (Ex. 1008) issued several years before the priority date, and many companies had products on the market before the '206 priority dates. Consequently, Petitioner WDT has identified and expects to rely upon a significant amount of system art in the Litigation. Further, Petitioners will stipulate that they will not pursue invalidity on the same grounds in the Litigation if the Board institutes trial in this proceeding. *See Fintiv*, IPR2020-00019, Paper No. 11 at 12-13 (use of different prior art in IPR petition than in district court favors institution).

Lastly, the Petition challenges claims 1-19, but Patent Owner's Litigation Complaint only alleges infringement of claims 11-12 and 18-19. Ex. 1022. Accordingly, the Board will resolve claims which the district court will not address, while the opposite is not true. *See Seven Networks*, IPR2020-00156, Paper 10 at 17 (fact that the Board will resolve claims that the district court will not address weighs in favor of institution).

5. Factor 5 Is Neutral

Only Patent Owner and Petitioner WDT are parties both in this proceeding and the Litigation; Petitioners WDC and SanDisk are not. However, given the corporate relationship between Petitioners, this factor is neutral.

6. Factor 6: Additional Factors Favor Institution.

Petitioners' Grounds are strong (*see* Section XI), further favoring institution. *Fintiv*, IPR2020-00019, Paper 11 at 14–15 (Where merits "seem particularly strong on the preliminary record, this fact has favored institution.").

IX. CLAIM CONSTRUCTION AND LEVEL OF ORDINARY SKILL IN THE ART

A. Claim Construction

Petitioners submit that all terms should be given their plain meaning as understood by POSITA in view of the intrinsic evidence, but reserve the right to respond to any constructions that may later be offered by Patent Owner or adopted

by the Board. Petitioner is not waiving any arguments concerning indefiniteness or claim scope that may be raised in the Litigation.

Petitioners offer the following constructions of selected terms:

1. "Mounted on" Means "Securely Attached, Affixed or Fastened To"

The term "mounted on," used in all the claims, refers to a physical object that is "mounted on" another physical object. "Mounted on" has no specialized meaning in the art and the '206 ascribes no specialized meaning to it. Ex. 1005, ¶¶ 99-102.

The Federal Circuit has held that the "ordinary meaning" of "mounted on" is "securely attached, affixed, or fastened to." *Asyst Techs. v. Emtrak, Inc.*, 402 F.3d 1188, 1193 (Fed. Cir. 2005); *see also Felix v. Am. Honda Motor Co*., 562 F.3d 1167, 1177-78 (Fed. Cir. 2009) ("mounted on" is "securely affixed or fastened to"). Here, "mounted on" should be afforded its ordinary meaning of "securely attached, affixed or fastened to." *See* Ex. 1005, ¶ 103.

"Mounted on" as used in the claim phrase "a contact bar mounted on the connection surface of the substrate" does not require that the contact bar be mounted *entirely* on the substrate's connection surface. *See Netlist, Inc. v. Diablo Techs., Inc.*, 701 F. App'x 1001, 1004 (Fed. Cir. 2017) ("Nothing in the claim

language or specification requires the 'entire circuit' to be mounted on the memory module.")

2. "Embedded to Be Exposed Upon"

Section VI explains that during prosecution, in response to the Examiner's indefiniteness rejection, Applicant amended "mounted on or embedded within" to read "embedded to be exposed upon."

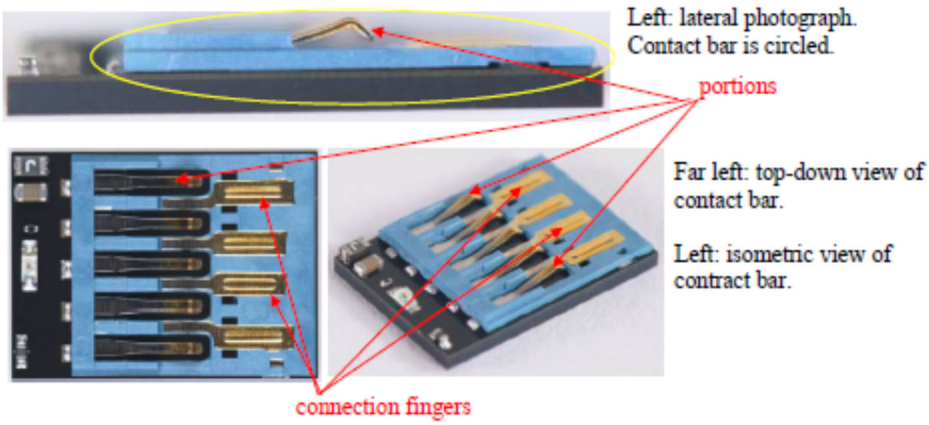
"Embedded" has no specialized meaning in the art or in the '206. Ex. 1005, ¶ 106. The term should be afforded its ordinary dictionary definition of "set firmly into a mass or material." *See* https://www.merriam-webster.com/dictionary/embedded; *see also* https://ahdictionary.com/word/search.html?q=embedded ("embed" means "to fix firmly in a surrounding mass: *embed a post in concrete*." *See also* Ex. 1005, ¶¶ 104-107.

3. Memory Die Stack

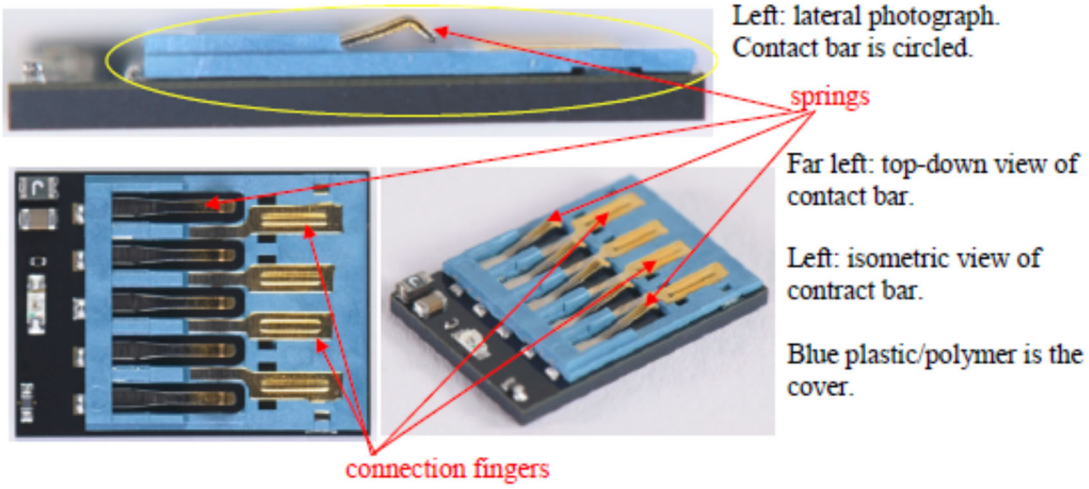
The '206 claims all require a "memory die stack," mounted on the claimed substrate. As Section V explains, the "stack" may have only one memory die. *See* Ex. 1005, ¶ 108.

4. Patent Owner's Litigation Complaint Shows Patent Owner's Construction of "Portions," "Connection Fingers," "Contact Bar," "Contact Bar Cover" and First and Second Distances

Patent Owner's Litigation Complaint (excerpts below) show Patent Owner's construction of "portions," "connection fingers," "contact bar," "contact bar cover," and first and second distances.

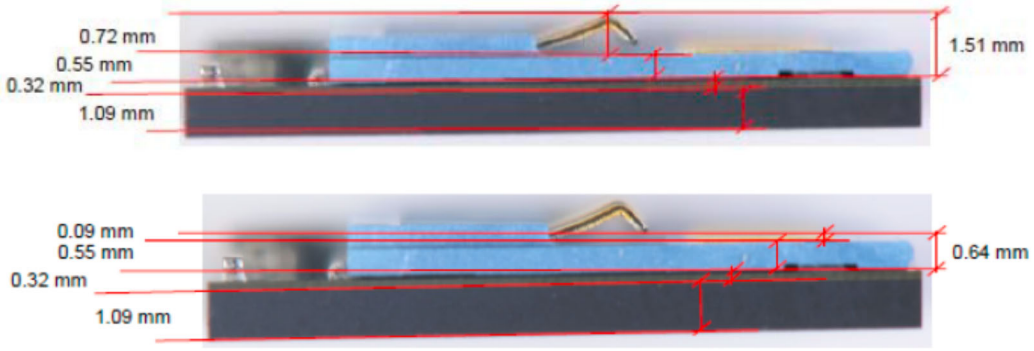


Ex. 1016 at 14.



Id. at 7.

The portions and connection fingers are identified above.
This row of the chart shows the rleative distances recited in the claims.
Each portion is located approximately 1.51 mm from the connection surface.
Each connection finger is located approximately 0.64 mm from the connection surface.



Id. at 15. *See* Ex. 1005, ¶¶ 109-110.

B. Persons of Ordinary Skill in the Art

The '206 is directed to a simple mechanical modification of external storage device connectors. For purposes of this IPR, POSITA would have had (1) a Bachelor's degree in EE, CompE, or ME, and (2) at least one year of experience with USB and other computer interface protocols. Ex. 1005 ¶¶ 43-48.

X. PRIOR ART OVERVIEW

A. Effective Filing Date

Claim 12 of the '206 is not entitled to the filing date of either of the Provisionals because neither Provisional provides written description support under 35 U.S.C. § 112 for at least claim 12's limitation "the plurality of connection fingers are embedded to be exposed upon the cover of the contact bar." Both

Provisionals teach that the claimed "connection fingers" are on the substrate itself. Ex. 1002 at 8, 12-13; Ex. 1003. *See* Ex. 1005, ¶¶ 93-97.

Accordingly, the effective filing date for claim 12 can be no earlier than the '431 Application's filing date—January 31, 2012.

This is not an issue for this Petition, however, because Petitioners' cited prior art is also prior art to the Provisionals, whose earliest filing date is January 31, 2011.

B. Prior Art Bases

The following are prior art under at least 35 U.S.C. § 102(b) because each was published over one year before January 31, 2011:

- USB 2.0 Specification, published April 27, 2000 (Ex. 1007). *See* Ex. 1019, ¶¶ 1-7;
- USB 3.0 Specification, published November 12, 2008 (Ex. 1008). *See* Ex. 1019, ¶¶ 1-4, 8-10;
- U.S. Patent 7,625,243 ("Chen"), published December 1, 2009 (Ex. 1010);
- U.S. Patent Application Publication 2009/0098773 ("Cheng"), published April 16, 2009 (Ex. 1012);
- U.S. Patent Application Publication 2008/0150111 ("Hiller"), published June 26, 2008 (Ex. 1013);

- U.S. Patent 7,563,140 ("Wan"), published July 21, 2009 (Ex. 1015).

The following are prior art under 35 U.S.C. § 102(e) as of their filing dates:

- U.S. Patent 7,909,654 ("He"), filed June 2, 2010 (Ex. 1011);
- U.S. Patent 8,480,435 ("Hsiao"), filed November 23, 2010 (Ex. 1009).

Sun (Ex. 1014) is a World Intellectual Property Organization publication of a Patent Cooperation Treaty application ("PCT") under 35 U.S.C. § 351(a). The PCT was filed July 30, 2010 in English, designated the U.S., and was published in English as WO 2011/160321. Ex. 1014, face page. Accordingly, Sun is prior art under 35 U.S.C. § 102(e) as of its PCT filing date, July 30, 2010. *See also* MPEP § 2136.

Prior art references cited herein or in Dr. Baker's Declaration (Ex. 1005) but not applied to the claims are supplied to provide information regarding the state of the art as of January 31, 2011.

C. He (Ex. 1011)

He, entitled "Plug Connector having An Improved Shell," discloses a USB plug connector—which He states "could be a USB flash disk" (Ex. 1011, 3:50-51)—compatible with USB 2.0 and 3.0 receptacles. *Id.*, 1:35-43, 3:9-12.

The plug connector's substrate (PCB **1**) has a base portion **10**, and a tongue portion **11**, and "opposed upper and lower surfaces." *Id.*, 1:27-29; *see also id.,*

2:16-25. The PCB has contacting pads **13** "formed by golden fingers of the PCB **1**" that are "adapted for USB 2.0 protocol." *Id.*, 2:34-35, 3:9-10.

He's plug connector also has resilient contacts **2,** including "two pairs of differential contacts and a grounding contact" for the USB 3.0 interface. *Id.*, 3:7-12. The resilient contacts **2** are assembled to insulator **3** to form a "contact module" that is mounted on PCB **1** by soldering tail portions **23** of resilient contacts **2** to soldering pads **12** on PCB **1**. *Id.*, 2:57-65, Figs. 3-4.

The resilient contacts **2** have portions **21** that extend above the PCB surface and are thus a greater height above the PCB's surface than the "golden fingers" formed on the PCB surface. *Id.*, 2:48-55, Figs. 3, 6 (annotated)[5]:

[5] The coloring on figures reproduced herein was added.

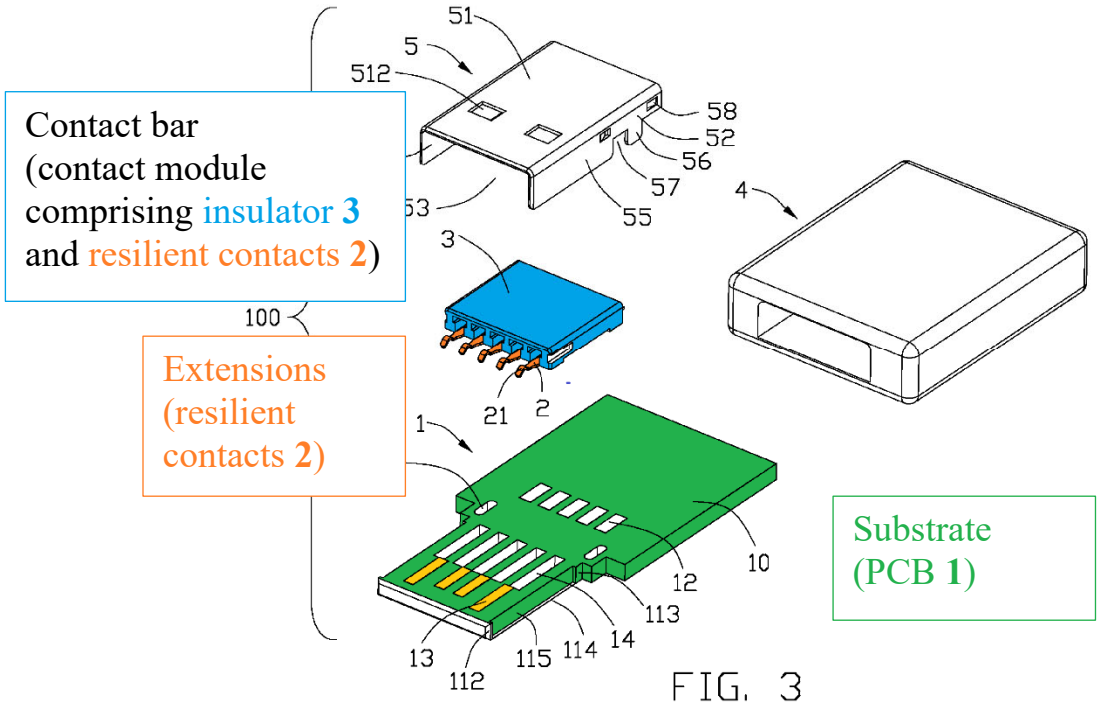


FIG. 3

Contact bar (contact module comprising insulator **3** and resilient contacts **2**)

Extensions (resilient contacts **2**)

Substrate (PCB **1**)

Connection fingers 13

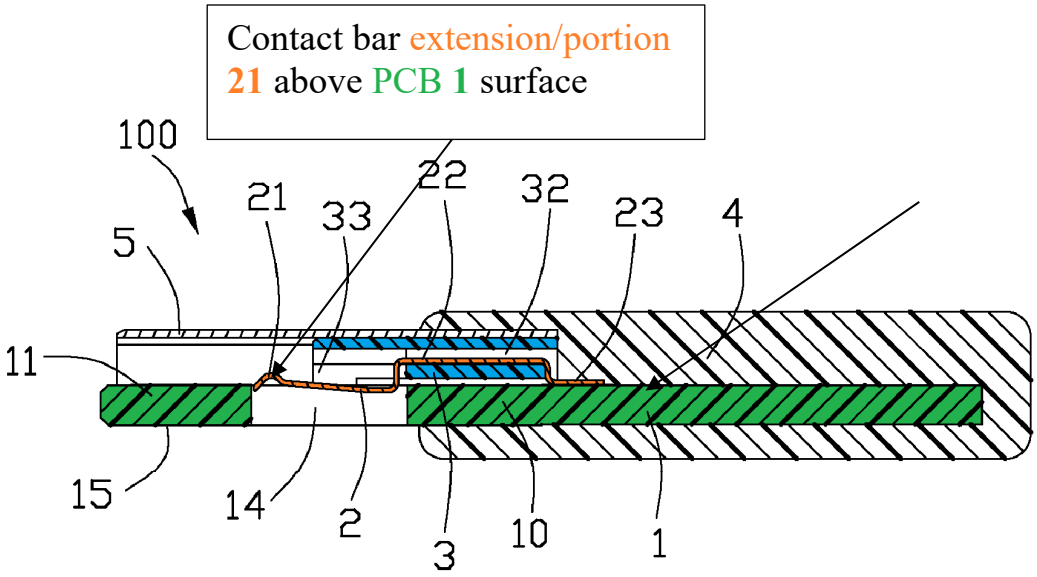


FIG. 6

See Ex. 1005, ¶¶ 133-136.

D. Hsiao (Ex. 1009)

Hsiao, entitled "USB Connector," teaches COB flash memory devices having both USB 2.0 and 3.0 interfaces. Ex. 1009, 1:36-39, 6:51-55, 7:30-38. In Figures 9-10, Hsiao discloses an external storage device wherein: (1) a contact bar having a cover (connector main body **320**) and terminals **323** is mounted on the connection surface of COB substrate **310,** and (2) connection fingers (terminals **322**) are embedded to be exposed upon the contact bar cover (connector main body **320**). *Id.*, 6:38-55, 7:4-38, Figs. 9-10 (annotated):

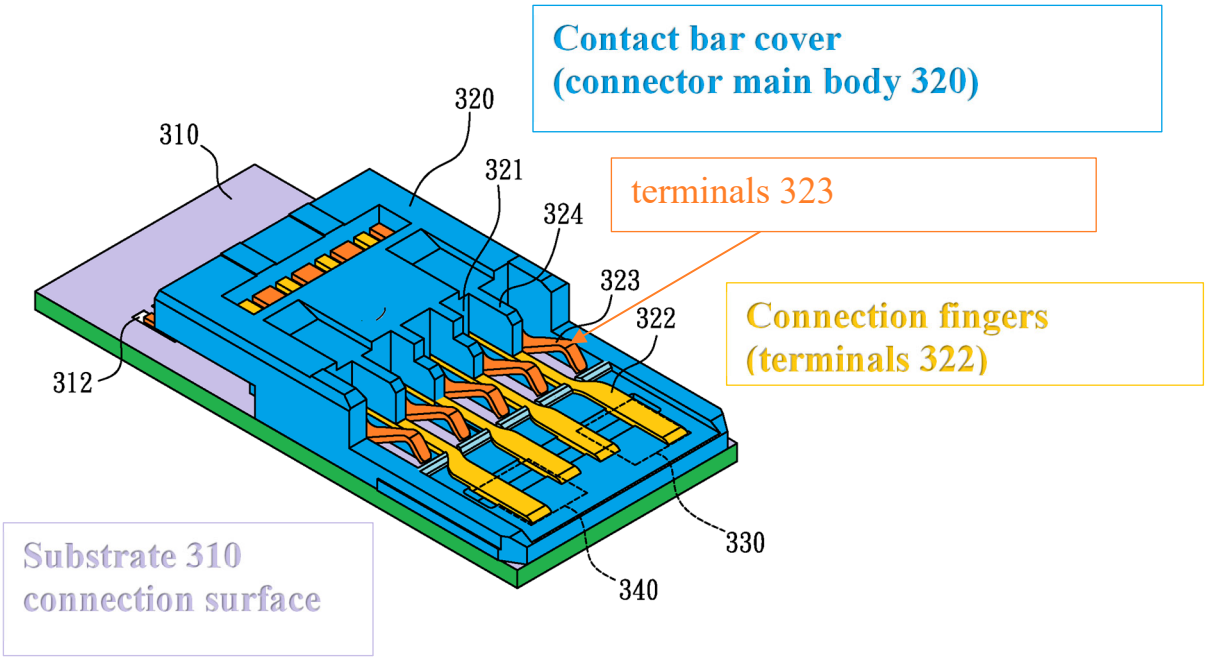


FIG. 10

Substrate **310**'s "connection surface" includes contact pads **311** (for USB 2.0 connections) and **312** (for USB 3.0 connections). *Id.*, 6:47-51, 6:59-7:3, Figs. 9, 10. Terminals **322** (USB 2.0 interface) and **323** (USB 3.0 interface) are "integrally

formed" with connector main body **320,** which "is made of insulation material" such as "plastic." *Id.*, 7:4-5, 7:39-42, 7:47-51. The terminals' "tails" are "welded" to contact pads **311** and **312**. *Id.*, 7:42-47.

USB controller **330** and flash memory **340** are installed on substrate **310** "through a means of [COB] package," which Hsiao states "is a conventional art." *Id.*, 7:34-36. Hsiao teaches that the disclosed USB connector "has a smaller volume and lower production cost compared to conventional USB connectors." *Id.*, 7:52-54.

See Ex. 1005, ¶¶ 111-118.

E. Chen (Ex. 1010)

Chen, entitled "Extension to Version 2.0 Universal Serial Bus Connector With Improved Contact Arrangement," discloses a connector plug having a USB 2.0 interface and a "non-USB 2.0" interface. Ex. 1010, Abstract. The plug has the same two-tier contact arrangement claimed in the '206 installed in insulative housing **10**.

"[P]lug contacts **13** include four plug conductive contacts [**131-134]** and a plurality of additional plug contacts **137**" "located behind the conductive contacts." Ex. 1010, 6:31-34, 6:46-49. The housing **10** includes passageways **123** for receiving the contacts (*id.*, 6:28-41), thereby making a contact bar.

Contacts **131-134** carry USB 2.0 signals. *Id.*, 7:59-64. "[E]ach comprises a plug contact portion **16**" that "is flat and nonelastic." *Id.*, 6:50-53, 6:57-58. When contacts **131-134** "are inserted into corresponding passageways **123**," this flat, non-elastic contact portion **16**, "is substantially coplanar with the supporting surface **121** as shown in FIGS. **3-4**." *Id.*, 6:58-62, Figs. 3-4.

"[P]lug contacts **137** include two pairs of differential plug contacts **138**" "for transferring/receiving high-speed signals" and "grounding plug contact **139**." *Id.*, 7:15-19, Fig. 2. These contacts each have "an elastic contact portion" designated **1381** and **1391**, respectively. *Id.*, 7:21-30. "[E]ach contact portion **1381**, **1391** is cantileveredly received in the passageways **123** and protruding upwardly beyond the supporting surface **121** so that the contact portion **1381**, **1391** is elastic and deformable when engaging with corresponding contacts of the extension to USB receptacle **200**." *Id.*, 7:43-48, Figs. 2-3 (annotated):

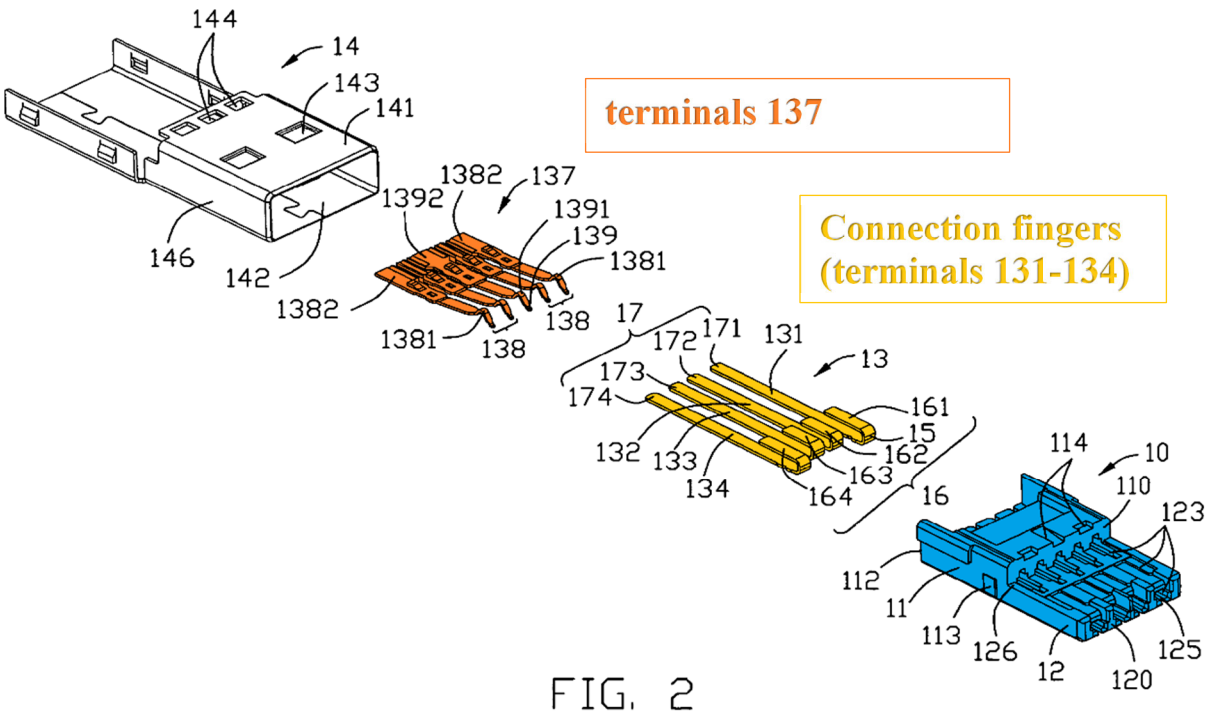


FIG. 2

Contact bar comprising **housing 10**, terminals **137** and **embedded connection fingers**

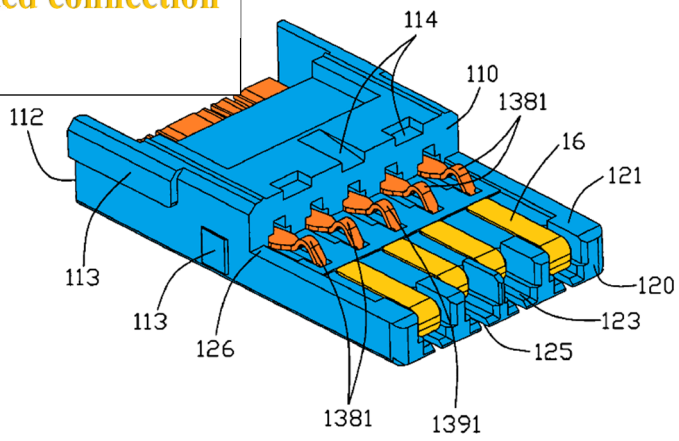


FIG. 3

Housing **10** has base and tongue portions **11, 12** that are "integrally injecting [sic: injection] molded" as one piece. *Id.*, 5:49-52, 6:12-14. The plug tongue

portion **12** has substantially the same dimensions as a standard USB 2.0 plug, and plug contacts **137** each have portions **1381** or **1391** that are a greater height above the substrate surface than the fingers. *Id.*, 7:55-57, Fig. 4 (annotated) (black arrows show first height, red arrows showing second height):

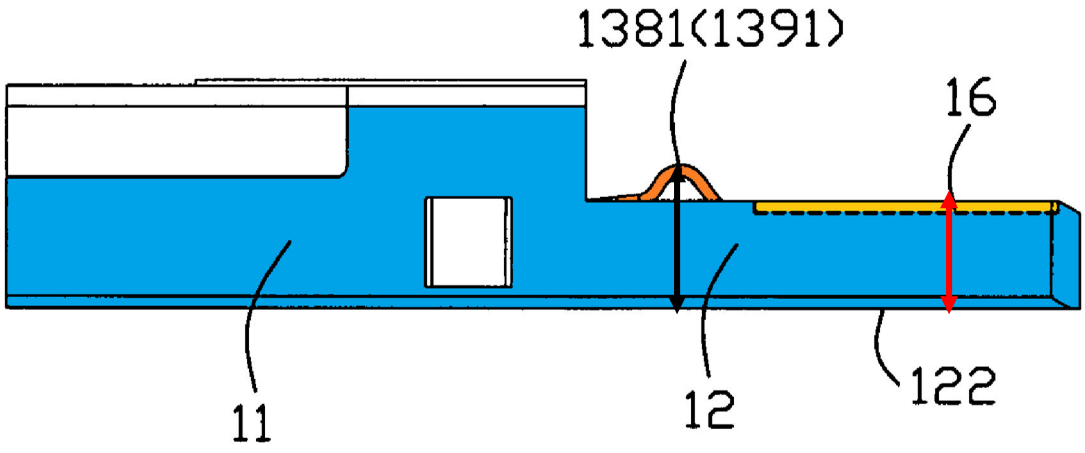


FIG. 4

Chen discloses an embodiment in which "the extension to USB is a memory device," that includes a PCB with a memory unit. *Id.*, 11:43-12:22. The USB plug has the configuration described above and is physically and electrically connected to the PCB. *Id.*; *see also id.*, claim 3.

See Ex. 1005, ¶¶ 119-132.

F. Cheng (Ex. 1012)

Cheng, entitled "Space Minimized Flash Drive," discloses USB flash drives in which memory is mounted on both sides of the flash drive's PCB. *See* Ex. 1012, [**0029-30**], [**0035-36**], Figs. 2, 6.

Cheng teaches that mounting flash memory on both PCB surfaces permits miniaturization of a flash memory device while providing for greater memory capacity. Ex. 1012, [**0010**], [**0030**].

See Ex. 1005, ¶¶ 142-145.

G. Hiller (Ex. 1013)

Hiller, entitled "Memory Device," discloses that a "conventional approach" to memory die stacking includes stacking "same-sized dies with overhanging designs." Ex. 1013, [**0003**]. Hiller discloses "a memory device comprising at least one memory stack of stacked memory dies which are staggered with respect to each other." *Id.*, [**0004**]; Figs. 8-9, 18:

FIG 8

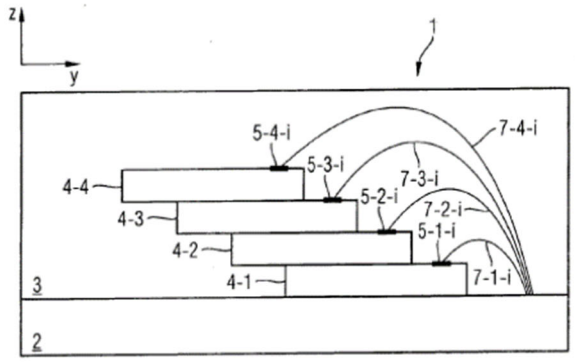


FIG 9

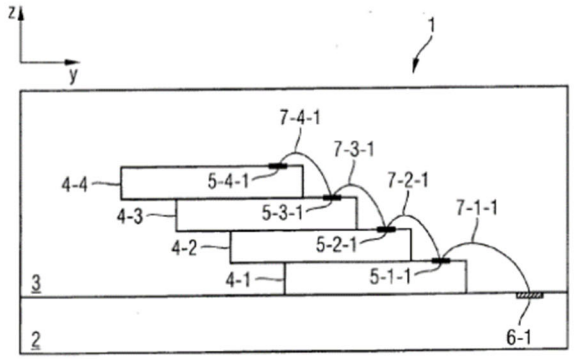
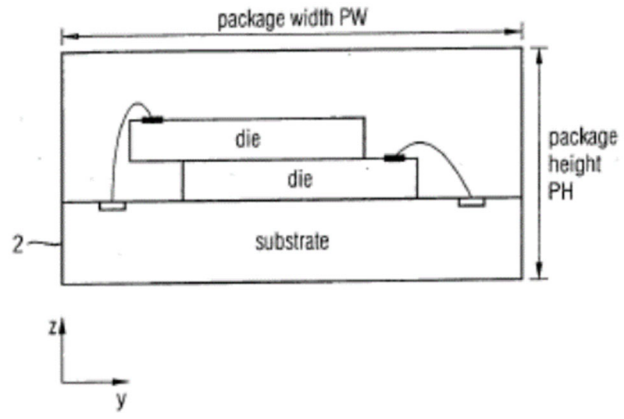


FIG 18



See Ex. 1005, ¶¶ 146-148.

H. Sun (Ex. 1014)

Sun, entitled "Data Storage Device," discloses USB "data storage device[s]" in which flash memory assemblies comprise "4 stacked flash memory dies." Ex. 1014, Abstract. These memory assemblies are mounted on either surface of the storage device's substrate or on both surfaces. *Id.* at 12-14. Sun teaches an advantage of multichannel stacked flash memory is providing "high data storage capability at high data transfer rates while maintaining a compact construction due to the high-rise stacked architecture." *Id.* at 2. Ex. 1005, ¶ 149.

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

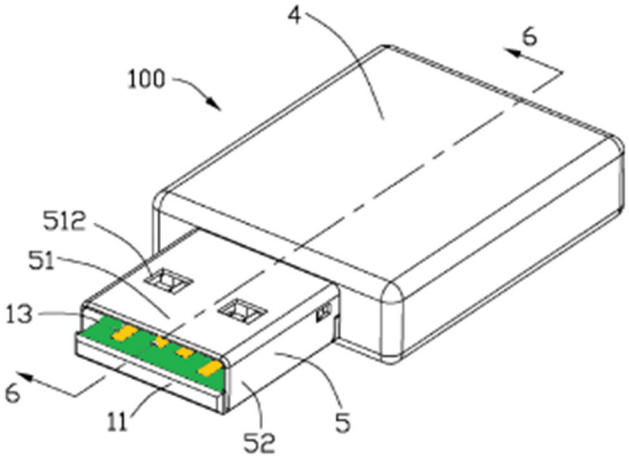
A. Ground 1: Claims 1-5, 8-11, 13-15, and 18-19 Are Obvious Over He And Cheng

As shown below, He and Cheng combined render claims 1-5, 8-11, 13-15 and 18-19 obvious. Ex. 1005, ¶ 153.

1. Claim 1

[a] An external storage device comprising:

He discloses a "USB flash disk" which POSITA would have known is synonymous with "USB flash drive," and is an external storage device. Ex. 1011, 1:35-43 (disclosing as "another aspect of the present invention, an USB flash disk"); 3:50-51 ("[T]he plug connector could be a USB flash disk"), Figs 1, 3:


4
6
100
512
51
13
6
11
52
5

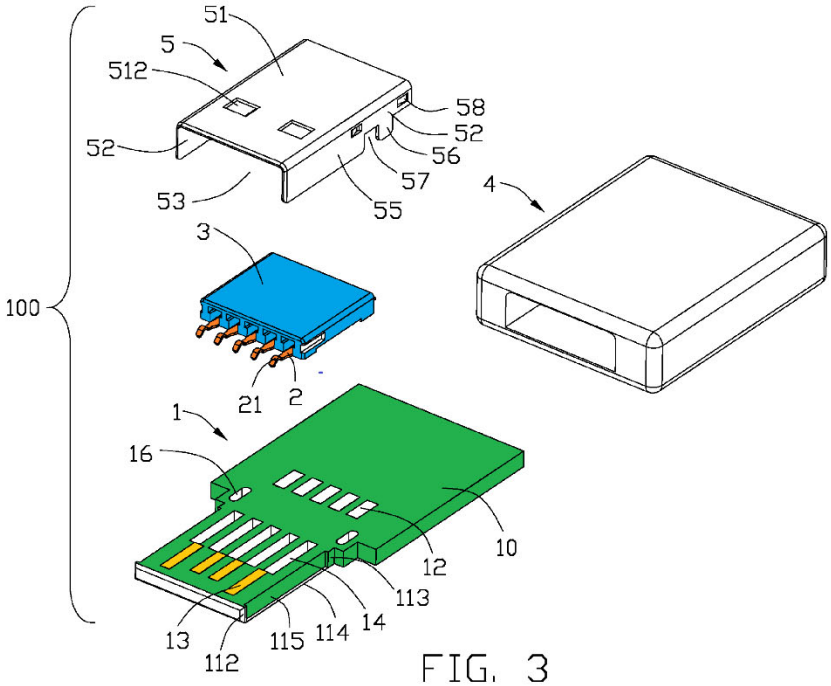

51
5
512
58
52
52
56
57
53
55
4
3
100
21
2
1
16
10
12
113
14
13
112
115
114

FIG. 3

See Ex. 1005, ¶¶ 154-155.

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

The substrate is PCB **1** which has two opposite surfaces. *See* Ex. 1011, 1:27-31 ("[A] plug connector for mating with a receptacle connector comprises a PCB having opposed upper and lower surfaces"); 2:16-20 ("Referring to FIGS. **1-3**, [a] plug connector **100** according to the present [sic: invention] is adapted for mating with a receptacle connector (not shown) and comprises a printed circuit board (named as PCB hereinafter) **1** . . .."

The "connection" surface is the surface on which "golden fingers" (for USB 2.0 signals) are formed. *Id.*, 2:28-35 ("The tongue portion **11** has a plurality of metal contacting pads **13** formed on an upper surface thereof . . .. The contacting pads **13** are formed by golden fingers of the PCB **1** . . .."), 3:9-10 ("The metal contacting pads **13** are adapted for USB 2.0 protocol."). The component surface is the opposite PCB surface. *Id.*, 2:35-37 ("tongue portion **11** has a lower surface opposite to the upper surface")

See Ex. 1005, ¶¶ 156-159.

[c] at least one memory die stack mounted on one of the connection surface and the component surface of the substrate;

He discloses "a USB flash disk" (Ex. 1011, 1:35-43, 3:50-51, Fig. 1), but does not expressly disclose a memory die stack mounted on PCB **1**. However, the very definition of a USB ***flash*** disk is that it includes flash memory; POSITA would have known that memory mounted on the PCB is necessarily present in a USB flash disk. Absent flash memory, it would not be a "USB flash disk." Ex. 1005, ¶¶ 160-161.

Indeed, Cheng (Ex. 1012) teaches that "a conventional flash drive" has "a USB connector" and "a rectangular body where a plurality of components such as flash memory devices, controllers, and passive components are disposed on a printed circuit board enclosed by the rectangular body." *Id.*, [**0004**]. POSITA would have known that flash memory necessarily includes at least one memory die. Ex. 1005, ¶¶ 162-163.

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

He does not expressly disclose that the "USB flash disk" has a controller mounted on the PCB. POSITA, however, would have known that this controller is necessarily present in a USB flash disk. POSITA would have understood a USB controller is required to provide a USB standard compatible interface between the USB bus and flash memory. The USB controller manages read/write operations

between flash memory and the USB bus, ensuring that communications follow the USB standard. Ex. 1005, ¶¶ 164-165.

Moreover, Cheng discloses that "conventional flash drive[s]" have "controllers" that are "disposed on a printed circuit board." Ex. 1012, [**0004**]. Cheng teaches that the controller is "electrically connected" to memory and the USB connector, and thus configured to access memory. Ex. 1012, [**0023**], [**0027**]-[**0029**].

It would have been obvious to POSITA to mount a controller on He's PCB as is "conventional" in USB flash drives. POSITA would have been motivated to do so to provide a USB standard compatible interface between the USB bus and the flash memory. Ex. 1005, ¶¶ 166-167.

[e] a contact bar mounted on the connection surface of the substrate, the contact bar comprising a plurality of extensions, each of the plurality of extensions including a portion that is located at a first distance relative to the connection surface of the substrate;

The contact bar is resilient contacts **2** ("plurality of extensions") assembled to insulator **3**, which He calls a "contact module." Ex. 1011, 2:48-60 ("[E]ach resilient contact **2** has . . . a connecting portion **22** . . . assembled to a plurality of cavities **32** of the insulator **3,** therefore, ***the resilient contact 2 and the insulator 3 are formed as a contact module*** together for being assembled to the PCB **1** . . .")

(emphasis added), 3:15-17 ("the resilient contact **2** could be insert molded into the insulator **3** so as to form as a contact module together for being assembled to the PCB **1**"), Figs. 3-6.

The contact bar (contact module) is mounted on the substrate's (PCB **1**) connection surface by soldering tail portions **23** of the extensions (resilient contacts **2**) to "soldering pads **12** securely." *Id.*, 2:60-62, 2:48-49 ("each resilient contact **2** has a tail portion **23** for being soldered on the soldering pad **12**"), Figs. 3-4 (annotated):

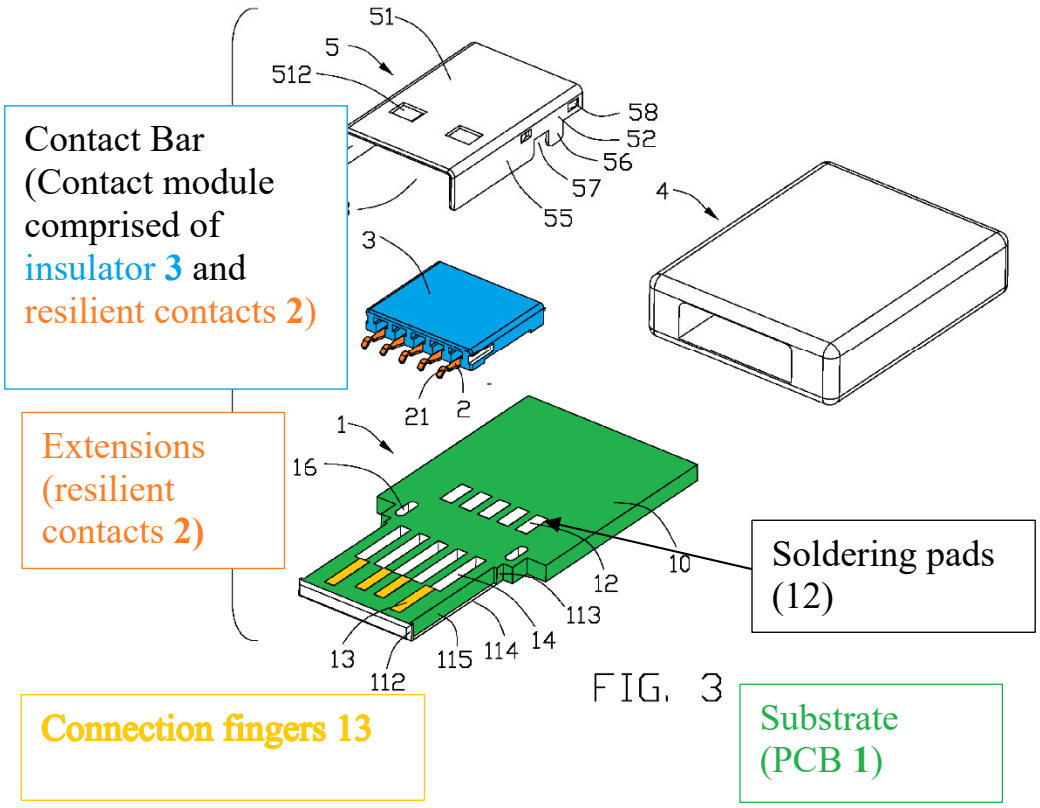


FIG. 3

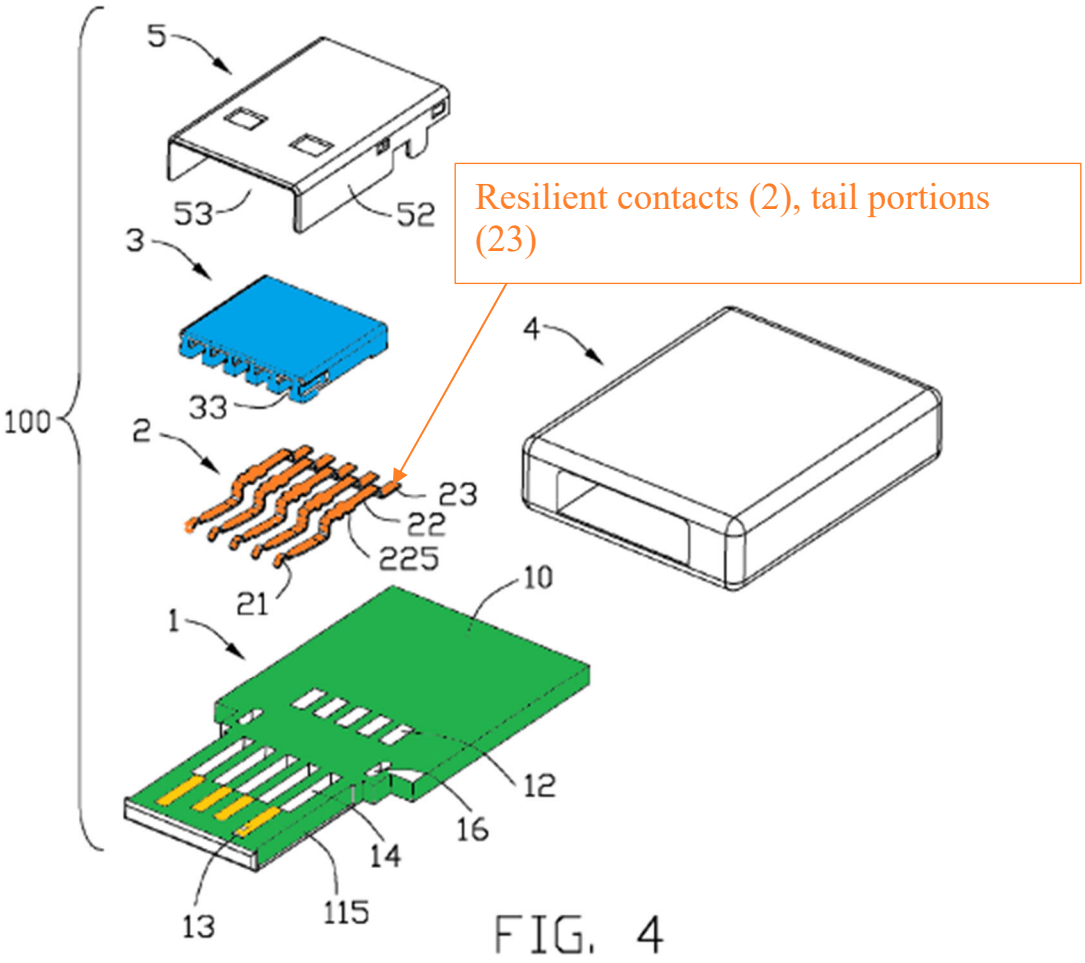


FIG. 4

Each resilient contact **2** has "a resilient contacting portion **21** being movably received in the passageway **14** for mating with the receptacle connector." Ex. 1011, 2:48-51. The first distance is the height of contacting portions **21** above the substrate (PCB **1**) surface. *See id.*, Fig. 6:

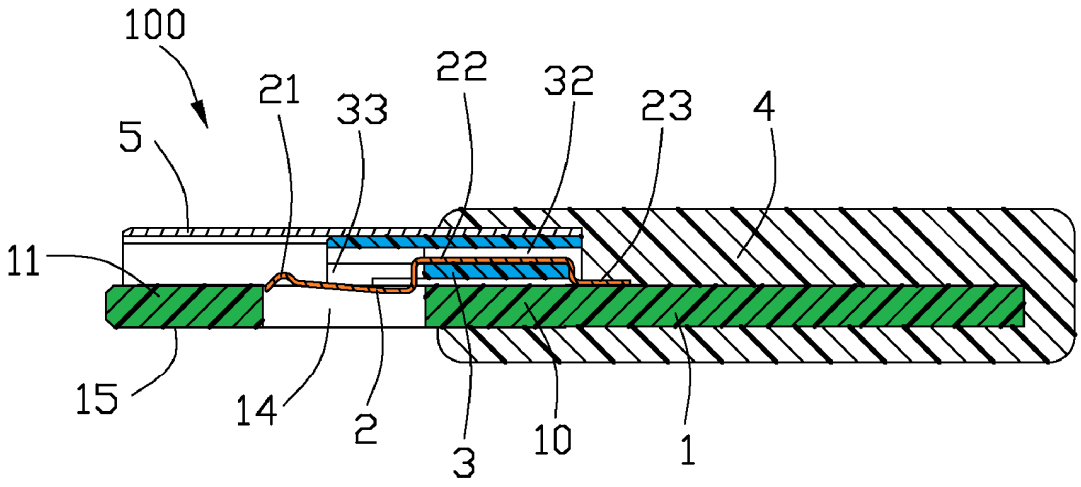


FIG. 6

See Ex. 1005, ¶¶ 168-171.

[f] a plurality of connection fingers embedded to be exposed upon the connection surface of the substrate at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

The "plurality of connection fingers embedded to be exposed upon" the substrates "connection surface" are "contacting pads **13** [f]ormed by golden fingers of the PCB **1**." Ex. 1011, 2:34-35, *see also id.*, 3:12-15 ("The metal contacting pads **13** and the contacting portions **21** are located on the upper surface of the tongue portion **11** and are arranged in two rows along a front-to-back direction.")

The second distance is the golden fingers' height above the surface of PCB **1**. Figure 4 shows that these fingers are flat and rectangular in shape, and as Figure 6 shows the second distance is necessarily less than the first distance. *Id.*, Figs. 4, 6. *See* Ex. 1005, ¶¶ 172-174.

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of extensions of the contact bar.

He discloses that the connection fingers (contacting pads **13**) "are adapted for USB 2.0 protocol," and "contacting pads **13** and resilient contacts **2** are "adapted for USB 3.0 protocol." Ex. 1011, 3:9-12. Thus, a first interface (USB 2.0) comprises the plurality of connection fingers, and a second interface (USB

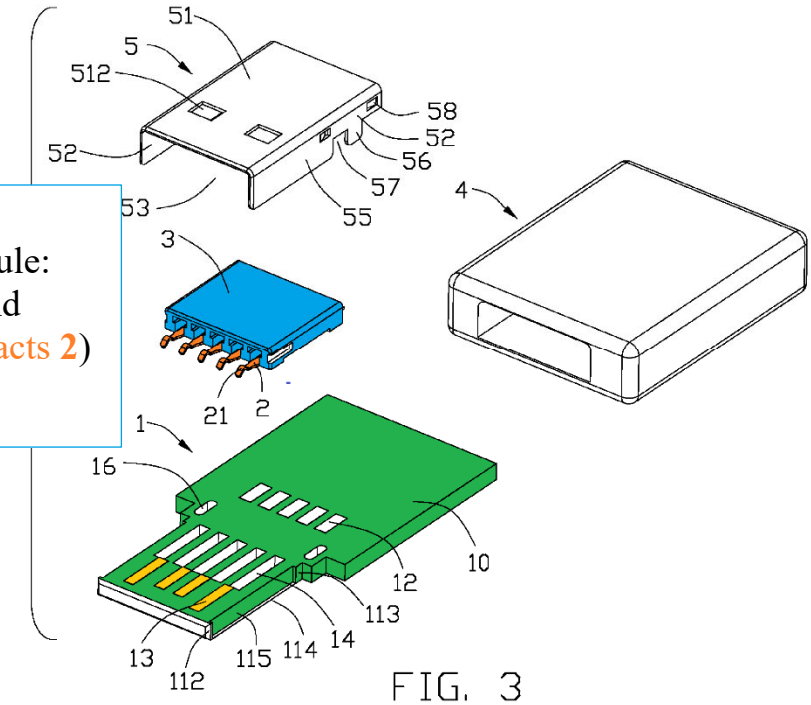
3.0) comprises the plurality of contact bar extensions (resilient contacts **2**). *See* Ex. 1005, ¶¶ 175-176.

2. Claims 2, 4 and 8

Claims 2, 4 and 8 depend from claim 1. As explained, He and Cheng combined disclose the elements of claim 1 and render it obvious. As shown below, He discloses the additional elements of claims 2, 4 and 8; He and Cheng combined thus render these claims obvious. Ex. 1005, ¶ 177.

a) Claim 2

Claim 2 requires that the contact bar "further comprises a cover." *See* Appendix A. Section XI.A.1(element [e]) explains the "contact bar" comprises insulator **3** with resilient contacts **2** installed. The "cover" is insulator **3** shown in Figures 3-4 (annotated):



Contact Bar (contact module: insulator 3 and resilient contacts 2)

FIG. 3

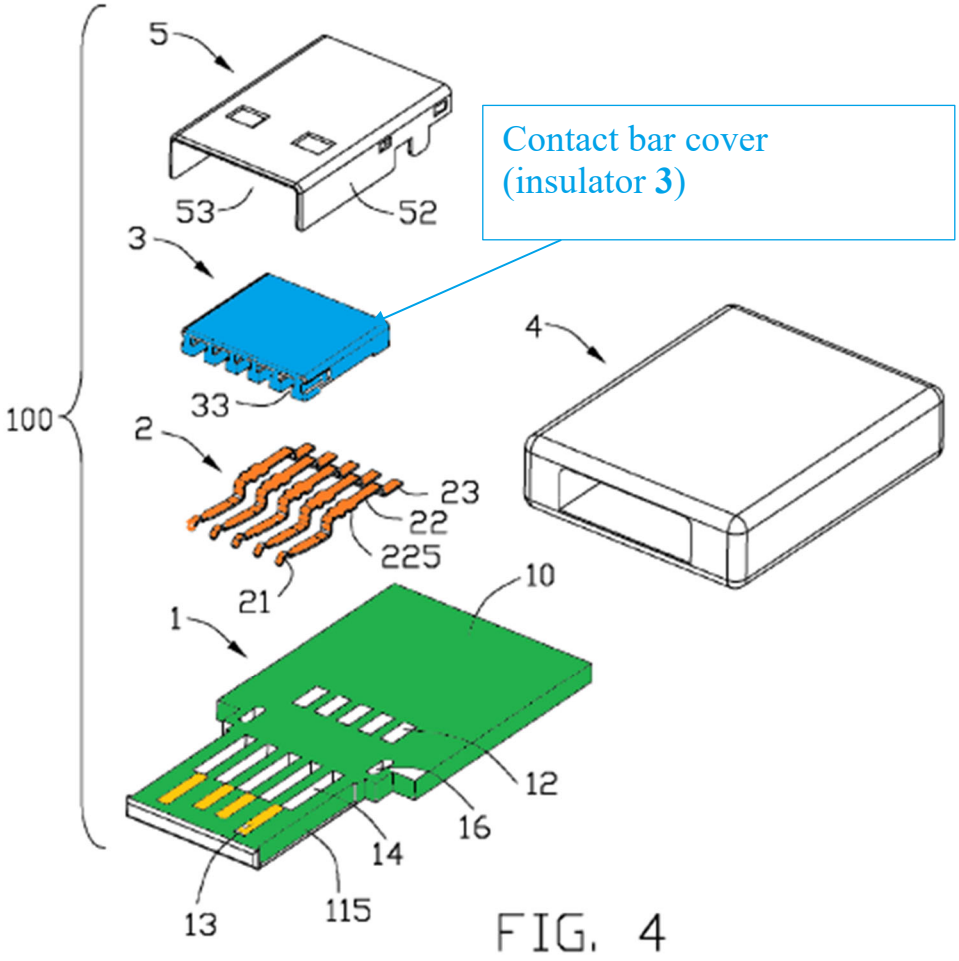


FIG. 4

See Ex. 1005, ¶¶ 178-179

b) Claim 4

Claim 4 requires that the "each extension includes a projection, the projection configured to be located at the first distance in an uncompressed position." Appendix A.

Section XI.A.1(element [e]) explains that the claimed "extensions" are resilient contacts **2**. These contacts include a "contacting portion **21**" designed to be "deflected by the receptacle connector" "in the height direction" when the plug is mated with a receptacle. Ex. 1011, 2:48-3:4 ("[E]ach resilient contact **2** has . . . a resilient contacting portion **21**. . . . the resilient contacting portions **21** are deflected by the receptacle connector . . .. The insulator **3** has a plurality of grooves **33** communicating with the cavities **32** and collaborating with the passageway **14** together to offer spaces for the contacting portions **21** deflecting in the height direction"), Fig. 6 (annotated):

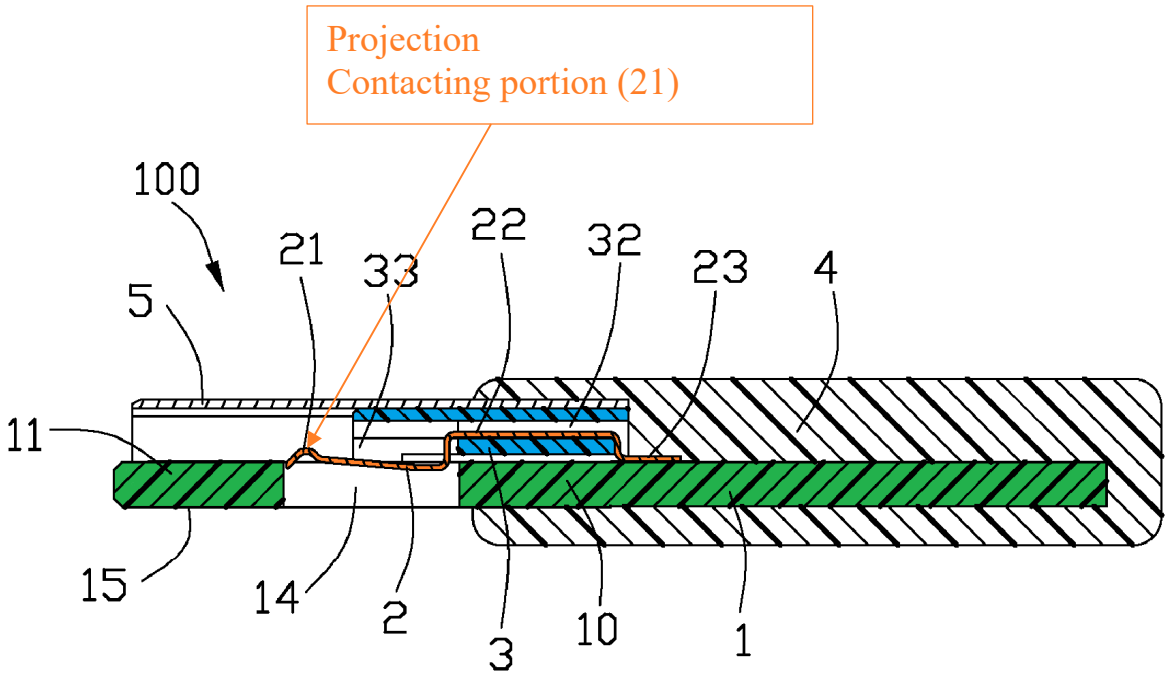

Projection
Contacting portion (21)
100
21
33
22
32
23
4
5
11
15
14
2
3
10
1

FIG. 6

Contacting portion **21** is the extension projection. The first distance is the height of contacting portion **21** above PCB **1**, and contacting portion **21** is located at this position when it is not being deflected (*i.e.*, when uncompressed). Ex. 1005, ¶¶ 180-182.

c) Claim 8

Claim 8 requires "the substrate comprises a printed circuit board." Appendix A. He discloses this limitation, stating that the USB flash disk substrate is a printed circuit board (PCB **1**). Ex. 1010, 2:16-19 ("plug connector **100**" "comprises an printed circuit board (named as PCB hereinafter) **1**"), 3:50-51 ("the plug connector could be a USB flash disk"). *See* Ex. 1005, ¶¶ 183-184.

3. Claim 10

He and Cheng combined render claim 10 obvious. Independent claim 10 duplicates the elements of claim 1 and adds element 10[h] requiring "the external storage device is configured to support Universal Serial Bus ("USB") 2.0 and USB 3.0 standards in effect as of Jan. 31, 2011."[6] *Compare* Appendix A, claim 1 *with* claim 10.

[6] The USB 2.0 and 3.0 specifications, published in 2000 and 2008, respectively (Ex. 1007 and 1008) were "in effect" on January 31, 2011. Ex. 1019, ¶¶ 1-10.

Section XI.A.1 explains that He and Cheng combined disclose claim 1's elements and render it obvious. He also teaches claim 10's additional element, stating "[t]he metal contacting pads **13** are adapted for USB 2.0 protocol. The metal contacting pads **13** and the resilient contacts **2** are adapted for USB 3.0 protocol." Ex. 1011, 3:9-12. *See* Ex. 1005, ¶¶ 185-187.

4. Claim 11

He and Cheng combined teach the elements of claim 11 and render it obvious. Claim 11 duplicates claim 1, elements [a]-[d]. *Compare* Appendix A, claim 1 *with* claim 11. Section XI.A.1 explains that He and Cheng combined teach each of these elements. He also teaches elements 11[e]-[g]. Ex. 1005, ¶ 188.

[e] a contact bar mounted on the connection surface of the substrate, the contact bar including a plurality of portions that are electrically coupled with the substrate and located at a first distance relative to the connection surface of the substrate;

Section XI.A.1(element [e]) explains that He's contact bar is resilient contacts **2** assembled to insulator **3**, called a "contact module." *See also* Ex. 1011, 2:59-61, 3:15-17. The contact bar (contact module) is mounted on the substrate's (PCB **1**) connection surface by soldering tail portions **23** of resilient contacts **2** to PCB **1**'s soldering pads **12.** Ex. 1011, 2:48-49, 2:60-62. He teaches that tail

portions **23** "will electrically connect to the soldering pads **12** reliably." *Id.*, 2:62-65.

Each resilient contact **2** has "a resilient contacting portion **21** being movably received in the passageway **14** for mating with the receptacle connector, and a connecting portion **22** connecting the contacting portion **21** and the tail portion **23**." *Id.*, 2:48-53.

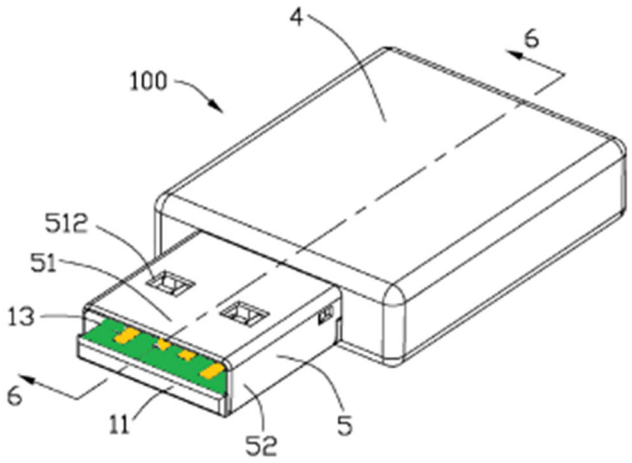
Contacting portions **21** constitute the claimed "plurality of portions that are electrically coupled with the substrate." They are "electrically coupled" to the substrate via their connection to tail portions **23** which are electrically connected to PCB **1**'s soldering pads **12**. The first distance is the height of contacting portions **21** above PCB **1**. *See* Section XI.A.1(element [e]);

See Ex. 1005, ¶¶ 189-192.

[f] a plurality of connection fingers electrically coupled with the substrate, the plurality of connection fingers located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

He discloses this limitation, stating that tongue portion **11** of PCB **1** "has a plurality of metal contacting pads **13** formed on an upper surface thereof" that "are formed by golden fingers of the PCB **1**." Ex. 1011, 2:28-35. Metal contacting pads **13** constitute "connection fingers electrically coupled with the substrate."

The second distance is the height of the metal contacting pads **13** above PCB **1**'s surface. These contacts, depicted as flat and rectangular, are embedded in PCB **1**. As Figure 6 (a cross-sectional view of the plug connector taken along line **6-6** of Figure 1) shows, the second distance is less than the first distance. *Id.*, 1:66-67, Figs. 1, 6 (annotated):



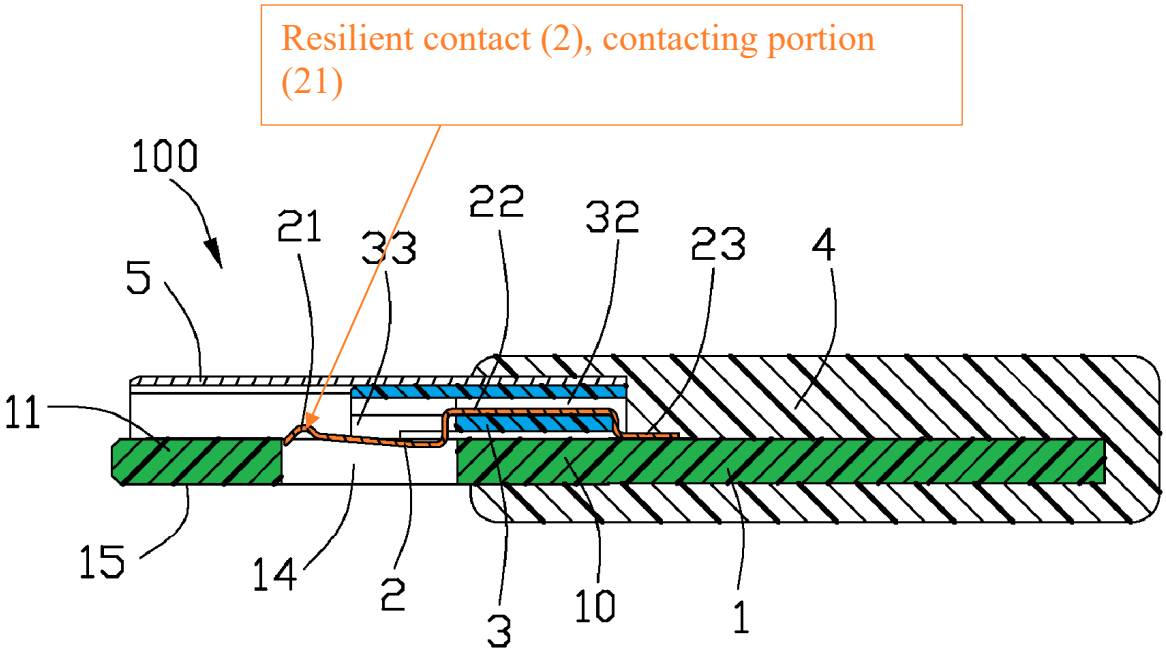

Resilient contact (2), contacting portion (21)
100
21
33
22
32
23
4
5
11
15
14
2
3
10
1

FIG. 6

As shown, the contacting portion **21** of resilient contacts **2** extends above PCB **1**'s surface, while the metal contacting pads **13** are embedded in PCB **1**'s surface. The second distance is therefore less than the first distance. *Id.*

See Ex. 1005, ¶¶ 193-196.

Claim 11[g] requires that a first interface comprises the connection fingers and a second interface comprises the contact bar "portions." Appendix A, 11[g]. He discloses that the connection fingers (contacting pads **13**) "are adapted for USB 2.0 protocol," and "contacting pads **13** and resilient contacts **2** (which include contact bar portions **21)** are "adapted for USB 3.0 protocol." Ex. 1011, 3:9-12; Ex. 1005, ¶ 197.

5. Claims 13 and 19

Claims 13 and 19 depend from claim 11. As discussed, He and Cheng combined teach all the limitations of claim 11 and render it obvious. As discussed below, He teaches the additional elements of claims 13 and 19. Thus, He and Cheng combined render claims 13 and 19 obvious. Ex. 1005, ¶ 198.

a) Claim 13

Claim 13 requires that the "connection fingers are embedded to be exposed upon the substrate." *See* Appendix A. Section XI.A.4(element[f]) explains that He's connection fingers (metal contacting pads **13**) are embedded to be exposed upon the substrate (PCB **1**). *See* Ex. 1005, ¶ 199.

b) Claim 19

Claim 19 requires that "the external storage device is configured to support Universal Serial Bus ("USB") 2.0 and USB 3.0 standards in effect as of Jan. 31, 2011." Appendix A. As discussed with respect to claim 10, He teaches this limitation. *See* Section XI.A.3; Ex. 1005, ¶ 200.

6. Claims 3, 5, 9, 14-15 and 18

Claims 3, 5 and 9 depend from claim 1 and claims 14-15 and 18 depend from claim 11. *See* Appendix A. Sections XI.A.1 and XI.A.4 explain that He and Cheng combined teach the elements of claims 1 and 11 and render them obvious. He and/or Cheng also disclose the additional elements of claims 3, 5, 9, 14-15, 18 and render them obvious. Ex. 1005, ¶ 201.

a) Claims 9 and 18

Claims 9 and 18 require that the first and second distances each comprise heights above the connection surface, and the second height is less than the first. *See* Appendix A.

Section XI.A.1 and XI.A.4, (elements [e]-[f]) explain that the first distance is the height of contacting portion **21** of resilient contacts **2** above PCB **1**'**s** connection surface, the second distance is the height of metal contacting pads **13** above that surface, and, the second height is less than the first. *See* Sections XI.1.A and XI.A.4 (elements [e]-[f]); Ex. 1005, ¶¶ 202-204.

7. Claims 3, 5 and 14-15

Claims 3, 5, 14-15 are all directed to the placement of memory die stacks on the substrate's surface(s). Claims 3 and 14 require that "the at least one memory die stack" and the "contact bar" are mounted on the same substrate surface. Claims 5 and 15 require that at least one memory die stack is mounted on each substrate surface. *See* Appendix A.

As Section XI.A.1 explains, He discloses a "USB flash disk," which POSITA would have understood has flash memory, but does not disclose which PCB surface(s) the flash memory is mounted on. It was well-known to POSITA that memory and the USB connections could be mounted on the same surface, and POSITA would have been motivated to do so where POSITA desired to create a slimmer device. Ex. 1005, ¶¶ 205-206. POSITA would have been motivated to mount memory on both substrate surfaces to increase memory capacity without substantially increase the device's length. *Id.*, ¶ 206.

Additionally, Cheng discloses USB flash drives in which a plurality of memory die stacks (flash memories **150**, **130**) are mounted on opposite surfaces (**111A, 111B)** of the substrate (PCB **110**). Ex. 1012, **[0030]**, Fig. 2 (annotated) :

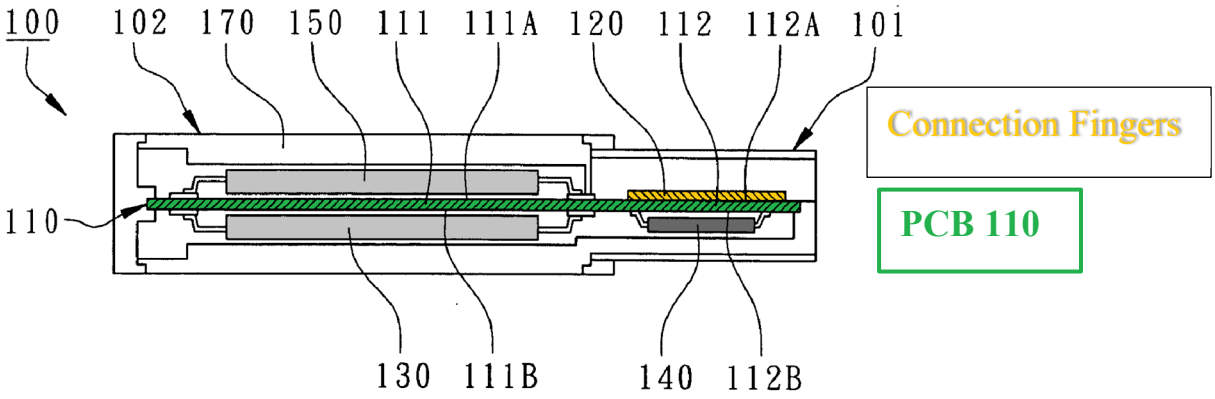


FIG. 2

Memory die stack
130, 150

Cheng also shows an embodiment where flash memories **250** and **230** are mounted on opposite surfaces (**211A** and **211B**) of the substrate (PCB **210**) "using COB processes and are electrically connected to the printed circuit board through wire bonding." *Id.*, [**0035-36**], Fig. 6:

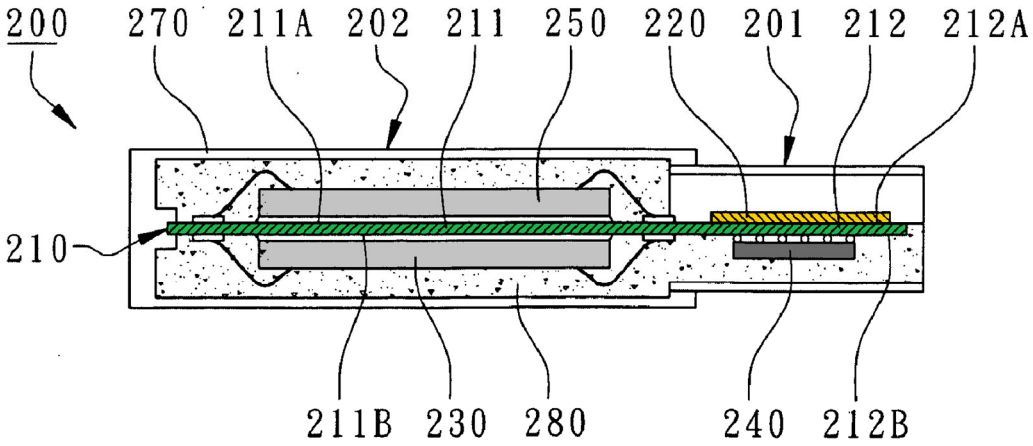


FIG. 6

Cheng thus discloses at least one memory die stack mounted on the same substrate surface as the contact bar as required by claims 3 and 14, and at least one memory die stack mounted on both substrate surfaces as required by claims 5 and 15. Cheng explains that mounting flash memory on both PCB surfaces permits miniaturization of a flash memory device while providing for "higher memory capacities." *Id.*, [**0010**], [**0030**]. POSITA would have been motivated to utilize Cheng's memory layout (including at least one memory die stack mounted on the PCB's connection surface) in He's USB flash disk in order to increase memory capacity without substantially increasing the device's length. *See* Ex. 1005, ¶¶ 207-209.

B. Ground 2: Claims 6-7 and 16-17 are Obvious Over He and Cheng and Further in View of Hiller

Claims 6 and 16 depend from claims 5 and 15, respectively, and require that the "plurality of memory die stacks" each comprises a "plurality of dies." Claims 7 and 17 depend from claims 6 and 16, respectively and require that the "plurality of dies" in a least two memory dies stacks are stacked in an overlapping arrangement. *See* Appendix A.

Section XI.A.7 explains that He and Cheng combined teach the elements of claims 5 and 15, and render them obvious. Section XI.A.7 explains that Cheng

discloses mounting a memory die stack on both PCB surfaces but does not disclose stacks having a plurality of dies.

Hiller (Ex. 1013) discloses memory die stacks having multiple dies and describes a "conventional approach" to memory die stacking that includes stacking "same-sized dies with overhanging designs." *Id.*, **[0003]**. Hiller also discloses "a memory device comprising at least one memory stack of stacked memory dies which are staggered with respect to each other." *Id.*, **[0004]**; Figs. 8-9, 18:

FIG 8

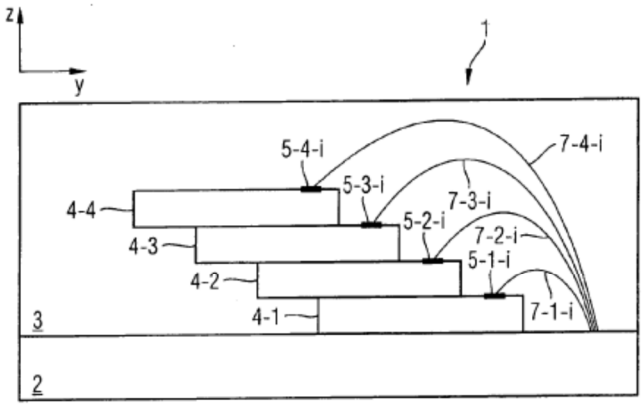


FIG 9

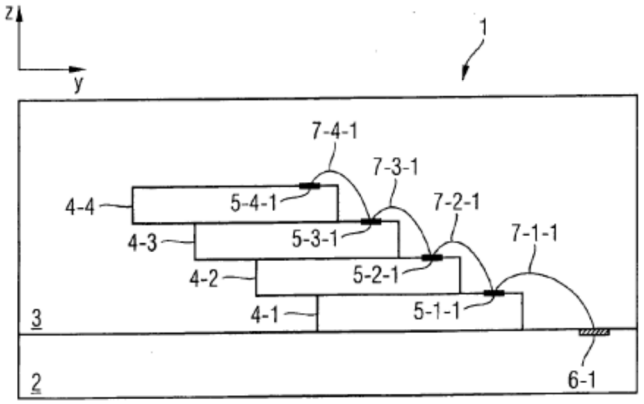
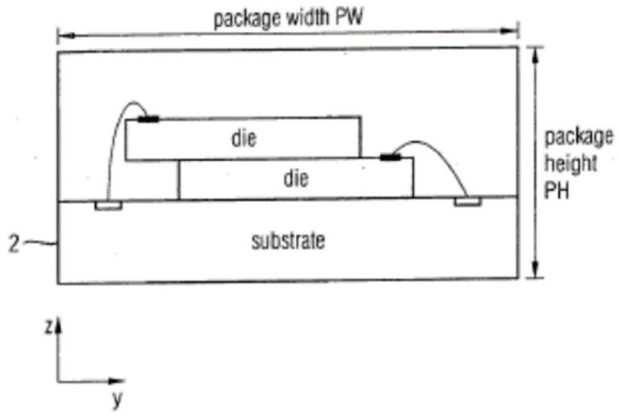


FIG 18



It would have been obvious to POSITA to utilize this conventional approach to memory die stacking in He's device, and POSITA would have been motivated to do so because using stacks having multiple dies allows for a memory device with greater storage capacity contained in a smaller space. Moreover, the overlapping arrangement facilitates wire bonding of the dies to the PCB while minimizing the need to increase the PCB length. Claims 6-7 and 16-17 are therefore obvious over He and Cheng and further in view of Hiller. Ex. 1005, ¶¶ 210-213.

C. Ground 3: Claims 1-11 and 13-19 Are Obvious over He and Sun

1. Claims 1-2, 4, 8-11, 13 and 18-19

Claims 1-2, 4, 8-11, 13 and 18-19 are obvious over He in view of Sun. Ex. 1005, ¶ 214. Section XI.A explains that He discloses a "USB flash disk" (which POSITA would have understood is synonymous with USB flash drive) that has a

connector with both USB 2.0 and USB 3.0 interfaces. Section XI.A also explains that He discloses the elements of claims 1-2, 4, 8-11, 13 and 18-19, but does not explicitly state that the USB flash disk has at least one memory die stack and a controller configured to access that memory.

Sun discloses USB 2.0/3.0 compatible flash drives having at least one memory die stack and a controller configured to access that memory. Sun discloses that these flash drives have (1) "flash memory assembl[ies]" and (2) a "USB 3.0 Controller" (**582**) that includes "NAND controller **510** arranged to cooperate with the flash memory assembly" to effectuate data transfer to and from the memory, and a main controller **530** connected between the NAND Controller and USB 2.0 and 3.0 physical layer interfaces ("PHY"). Ex.1014 at 11-12, Fig. 9:

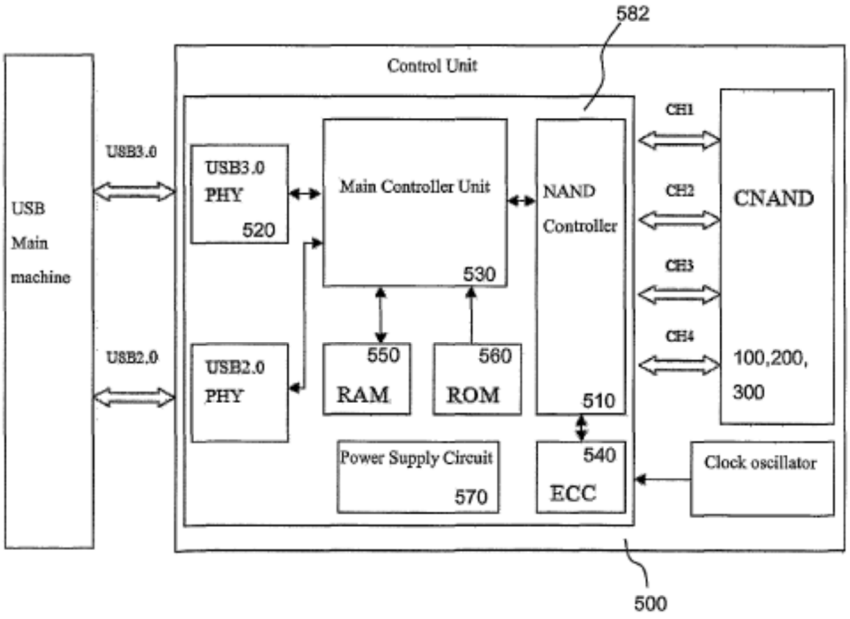


FIG. 9

It would have been obvious to POSITA to include flash memory and a USB controller in He's USB flash disk and configure the controller to access memory in order to effectuate data transfer to and from memory in compliance with the USB specifications as taught by Sun. Ex. 1005, ¶¶ 214-216.

2. Claims 3, 5-7, 14-17

Claims 3, 5-7 depend from claim 1 and claims 14-17 depend from claim 11, and all are directed to the placement of memory die stacks on the substrate. Claims 3 and 14 require that at least one memory die stack is mounted on the same substrate surface as the contact bar. Claims 5 and 15 require at least one memory die stack is mounted on each substrate surface. Claims 6 and 16 require that the memory die stacks of claims 5 and 15, respectively have "a plurality of dies," and claims 7 and 17 require that the dies in at least two memory die stacks of claims 6 and 16 "are stacked in an overlapping arrangement." *See* Appendix A.

Sun discloses three flash memory assemblies, each of which has four stacked dies. *See* Ex. 1014 at 6 ("flash memory assembly 100 of Figures 2, and 2A" "comprises a stack of 4 flash memory dies"), *id.* at 9 ("stack assembly 200 of Figures 3 and 3A has a structure substantially identical to that of Figures 2 and 2A"), *id.* at 9-10 ("structure and connection of the flash memory dies and PCB" for stack assembly 300 of Figs. 8, 8A "identical to that of Figure 2"), *id.* at 10-11 ("the exemplary stack comprises 4 dies"); Figs. 2-2A, 3-3A, 8-8A:

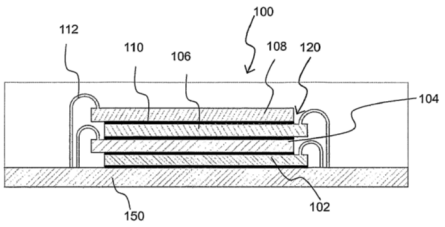


FIG. 2

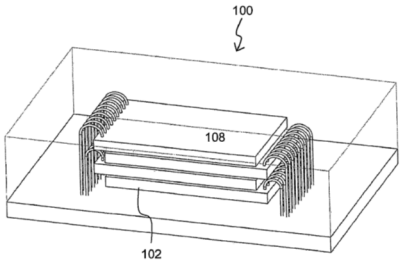


FIG. 2A

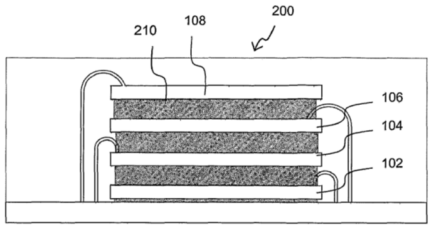


FIG. 3

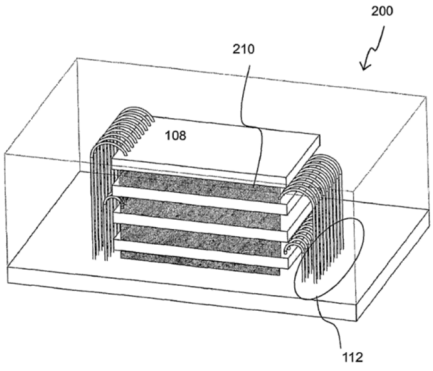


FIG. 3A

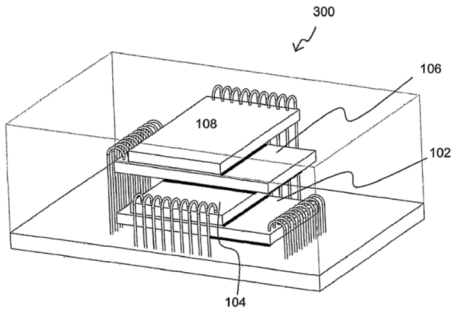


FIG. 8A

Sun discloses that the memory die stack can be mounted on the same surface as "USB connector **590.**" *Id.* at 12-13 (Figs. 10-10B show "the circuit components of the flash drive of Figure 9 are mounted on a printed circuit board (PCB) **580**"), Figs. 10-10A:

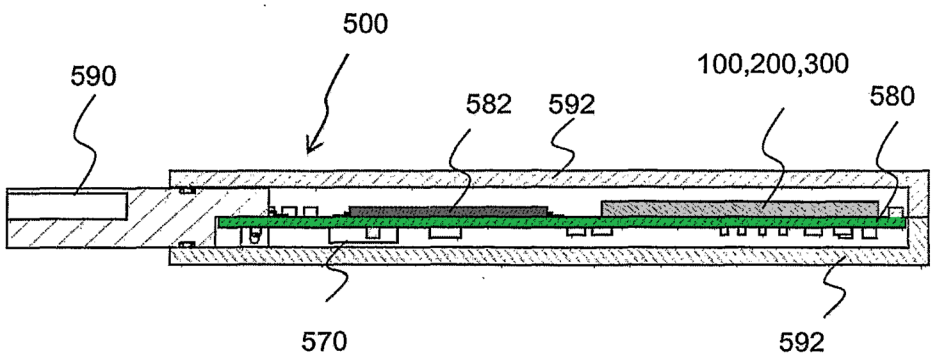


FIG. 10

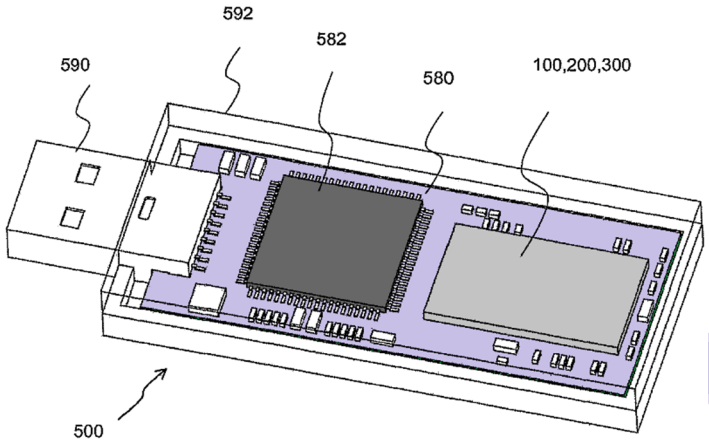


FIG. 10A

Connector 590

IC 582

Memory die stack 100, 200, 300

Sun also discloses memory die stacks mounted on ***both*** PCB surfaces:

> [M]ore than one flash memory stack could be included in each flash drive. [S]tacked flash memory assemblies could be mounted on both sides of the PCB, . . . thereby substantially enhancing the storage capacity of the flash drive . . .

Id. at 14-15.

Sun discloses that the dies in each stack are stacked in an overlapping arrangement:

> As shown more particularly in Figures 2 and 2A, the dies are organized such that the contact portion of one die is on one lateral end, while that of an adjacent die is on the direct opposite lateral end. This zigzag stacking facilitates a more balanced and symmetrical stacking to facilitate a more stable structure and enables more dies to be stackable in a stack to further increases storage capacity. In addition, this stacking arrangement also provides a more space efficient arrangement for the bonding wire to negotiate when extending from the die to the PCB.

Ex. 1014 at 9, Fig. 2, Fig. 8A.

See Ex. 1005, ¶¶ 217-220.

It would have been obvious to POSITA to combine He with Sun to create external storage devices having the memory die stack arrangements claimed in claims 3, 5-7 and 14-17. *Id.*, ¶ 221. POSITA would have been motivated to do so and have a reasonable expectation of success for the following reasons.

For external storage devices, POSITA had (and has) finite choices regarding which substrate surface(s) to mount a memory die stack on. Memory could be mounted on (1) the same surface as the USB connector, (2) the opposite surface, or (3) both surfaces. Where a designer requires a slimmer device, the designer may choose to mount the memory on the same surface as other components and the

USB connector. Where the designer requires increased memory capacity without substantially increasing the device's length, the designer may choose to mount a memory die stack on both substrate surfaces, rather than placing the stacks side-by-side on the same surface. *Id.*, ¶ 222.

POSITA would have been motivated to mount memory on the "connection" surface (on which the contact bar is mounted) of He's flash memory device as required by claims 3 and 14, and disclosed in Sun, Figs. 10-10C, where POSITA desired to minimize device thickness. *Id.*, ¶ 223.

POSITA would have been motivated to mount memory on both surfaces of He's flash memory device as required by claims 5 and 15 and disclosed in Sun (Ex. 1014 at 14-15) where POSITA desired to increase memory capacity without substantially increasing the overall length of He's device. Ex. 1005, ¶ 224.

The number of dies to include in a memory die stack, and the arrangement of those dies, is a function of the desired size and memory capacity of the device. Where greater memory capacity is required, a designer could include more dies in the stack, stacking them in a way that best meets the desired size requirements for the device. *Id.*, ¶ 225.

POSITA would have been motivated to include a plurality of memory dies in the memory die stacks of He's device as required by claims 6 and 16, and disclosed in Sun, in order to increase memory capacity without substantially

increasing the length of He's device. As Sun teaches, "the footprint of the flash memory assembly" having multiple dies "is about the same as that of a single flash memory die." Ex. 1014 at 13. *See* Ex. 1005, ¶ 226.

POSITA would have been motivated to stack the dies in an "overlapping arrangement" as required by claims 7 and 17 and taught by Sun in order to facilitate wire bonding of the dies to the substrate and aid in miniaturization of the device. *Id.*, ¶ 227.

D. Ground 4: Claims 11-12 Are Anticipated by Hsiao

As shown below, Hsiao discloses every element of claims 11-12 and thus anticipates these claims. *Id.*, ¶ 228.

1. Claim 11

[a] An external storage device comprising:

Hsiao teaches an external storage device—*i.e.,* a USB COB flash memory device. Ex. 1009, 7:30-36 ("[S]ubstrate **310** of the USB connector" is "installed with a USB controller **330** and at least one flash memory **340** respectively coupled to the plural first contact pads **311** and the plural second contact pads **312**; the USB controller **330** and the flash memory **340** are installed on the substrate **310** through a means of Chip-On-Board package, said means is a conventional art . . .."), Figs. 9-10:

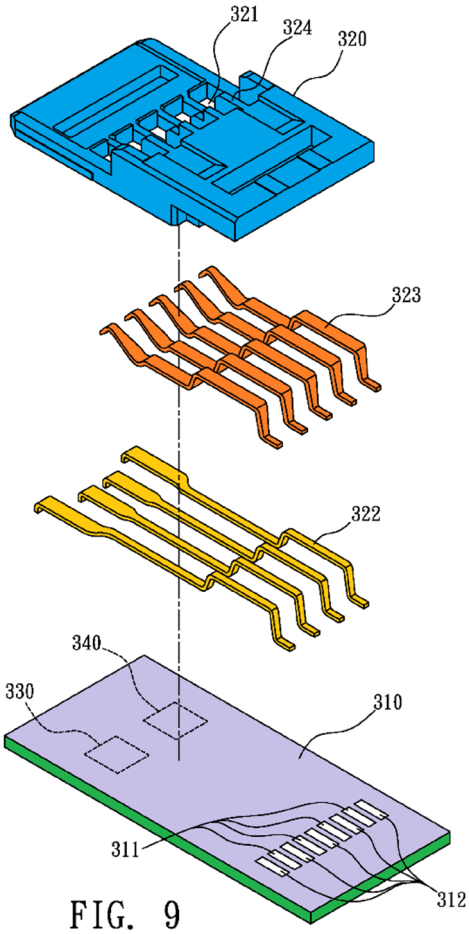


FIG. 9

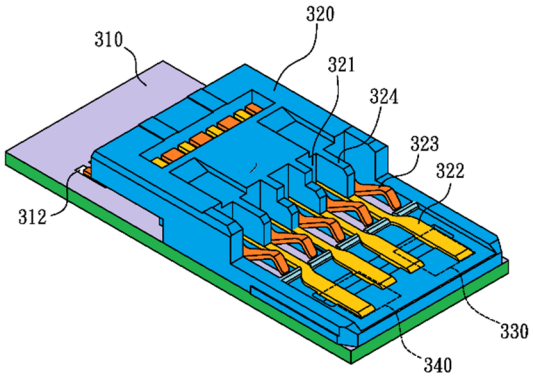


FIG. 10

Ex. 1005, ¶¶ 229-230.

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

The substrate is "Chip on Board (COB) substrate" **310**. Ex. 1009, 6:51-55. The "connection" surface is the surface where contact pads **311** and **312** are installed, and the "component" surface is the opposite surface. *Id.*, 6:47-7:3:

> [P]lural first contact pads **311** is e.g. but not limited to four, so as to assemble a USB2.0 connector, ...
>
> [C]ontact pads **312** . . . transmit StdA_SSRX−, StdA_SSRX+, GND_DRAIN, StdA_SSTX− and StdA_SSTX+ signals of USB3.0 specification.

The dotted lines for memory **340** and controller **330** (*see id.*, Figs. 9-10) indicate they are mounted on the opposite substrate surface from the "contact pads"—*i.e.,* the "component" surface. Ex. 1005, ¶¶ 231-233.

> *[c] at least one memory die stack mounted on one of the connection surface and the component surface of the substrate*;

Hsiao teaches at least one memory die stack mounted on the substrate, stating: "***[S]ubstrate 310 of the USB connector of the present invention is further installed with*** a USB controller **330** and ***at least one flash memory 340*** respectively coupled to the plural first contact pads **311** and the plural second contact pads **312** . . .." Ex. 1009, 7:30-36 (emphasis added). POSITA would have known that flash memory **340** necessarily has at least one memory die. Ex. 1005, ¶¶ 234-235. As explained, the memory is mounted on substrate **310**'s "component" surface.

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

The claimed controller is "USB controller **330**." The controller is configured to access the memory. Both the controller and memory are connected to contact pads **311** and **312.** Ex. 1009, 7:30-36. Moreover, POSITA would have known that the purpose of a USB controller is to provide a USB standard compatible interface between the USB bus and the flash memory. The USB controller manages read and write operations between the flash memory and the USB bus to ensure that communications between the flash memory and USB bus follow the USB standard. Ex. 1005, ¶¶ 236-237.

[e] a contact bar mounted on the connection surface of the substrate, the contact bar including a plurality of portions that are electrically coupled with the substrate and located at a first distance relative to the connection surface of the substrate;

Hsiao discloses a contact bar—*i.e.,* connector main body **320** with second terminals **323** installed. Ex. 1009, 7:39-42, Figs. 9-10. Terminals **323** are "integrally formed" with connector main body **320** along with terminals **322**; connector main body **320** is then mounted on the substrate's connection surface. *Id.*, 7:39-47 ("As shown in FIG. **10**, when being manufactured, firstly the plural

first terminals **322** and the plural second terminals **323** are arranged with a staggering means, then is integrally formed with the connector main body 320; then the connector main body **320** is disposed on the substrate **310**, and the other ends of the plural first terminals **322** and the plural second terminals **323** are respectively welded on the plural first contact pads **311** and the plural second contact pads **312** with a means of surface mount technology (SMT).")

A portion of terminals **323** is "upwardly bended then downwardly bended after being exposed outside the opening slots **321**." *Id.*, 7:27-29. The first distance is the height of the "upwardly bended" portion of terminals **323** above substrate **310.** These "portions" are electrically coupled with the substrate because the other end of terminals **323** is "welded" to substrate **310**'s second contact pads **312**. Ex. 1009, 7:39-47, Fig. 10 (annotated):

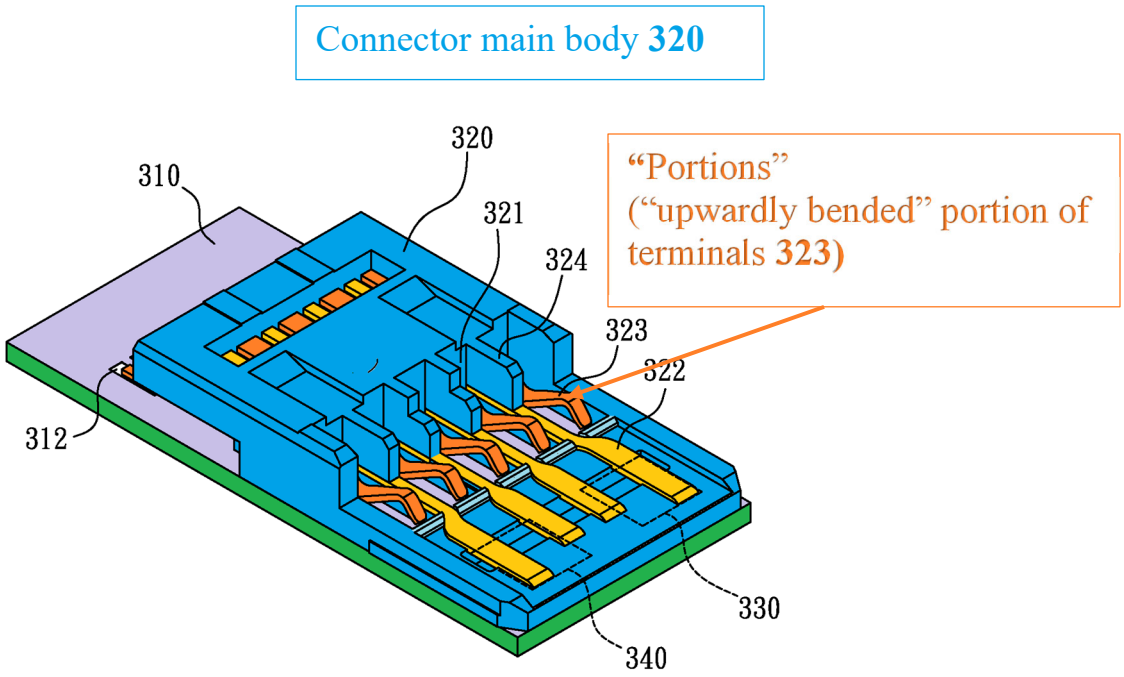


FIG. 10

See Ex. 1005, ¶¶ 238-241.

[f] a plurality of connection fingers electrically coupled with the substrate, the plurality of connection fingers located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

Hsiao's discloses a "plurality of connection fingers" (terminals **322)** which, as discussed with respect to element 11[e], are "electrically coupled" with substrate **310** by welding one end of terminals **322** to contact pads **311**. Ex. 1009, 7:39-47.

These terminals are "installed below the plural slot columns **324** and exposed outside the slot columns **324** then forwardly extended." *Id.*, 7:10-13.

The second distance is the height of the "forwardly extended" portion of terminals **322** above substrate **310**. As Figure 10 shows, this part of terminals **322** are flat and do not have an "upwardly bended" portion as do terminals **323**. Accordingly, the second distance is less than the first distance.

See Ex. 1005, ¶¶ 242-244.

Moreover, Hsiao's flash drive is configured to support the USB 2.0 and 3.0 protocols (*id.*, 7:47-50) and is a USB 3.0 Standard-A connector. *Id.*, 6:67-7:3 (explaining contact pads **312** transmit "StdA" signals). Thus, it must include the USB 3.0 Specification's two-tier contact arrangement for Standard-A connectors in which USB 3.0 SuperSpeed contacts (terminals **323** in Hsiao) are arranged in a row behind the USB 2.0 contacts (terminals **322** in Hsiao) and a portion of the USB 3.0 SuperSpeed terminals sit above (in the vertical direction) the USB 2.0 contacts. *See* Section IV.B; Ex. 1005, ¶ 245.

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of portions of the contact bar.

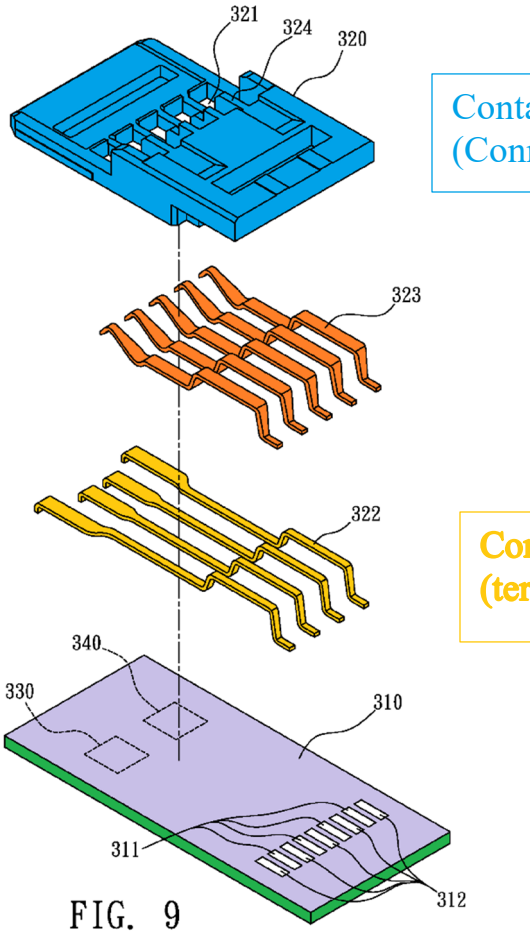
Hsiao teaches this element. *See, e.g.,* Ex. 1001, 7:47-54 ("the four first terminals **322** [connection fingers] of the USB connector are assembled as a

USB2.0 connector, the five second terminals **323** ["portions"] of the USB connector are assembled as a USB3.0 connector"). *See* Ex. 1005, ¶ 247.

2. Claim 12

Claim 12 depends from claim 11. Section XI.D.1 explains how Hsiao anticipates claim 11. Hsiao also discloses the additional element of claim 12—"the contact bar comprises a cover and wherein the plurality of connection fingers are embedded to be exposed upon the cover of the contact bar" (Appendix A)—and thus anticipates it.

Hsiao's contact bar cover is connector main body **320** and "connection fingers" (terminals **322**) "are embedded to be exposed upon" the contact bar cover. Ex. 1009, Figs. 9-10 (annotated):



Contact bar cover
(Connector main body **320**)

Connection fingers
(terminals 322)

FIG. 9

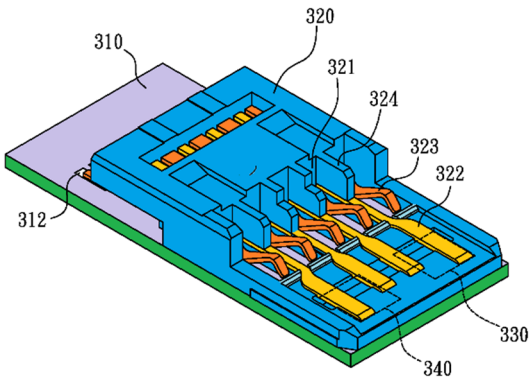


FIG. 10

See Ex. 1005, ¶¶ 248-250.

Terminals **322** are "installed below the plural slot columns **324**" of connector main body **320**, "and exposed outside the slot columns **324** then forwardly extended." Ex. 1009, 7:10-13, Fig. 10. These contacts are "integrally formed" with connector main body **320** before it is mounted on substrate **310** and are thus embedded in the contact bar cover. *Id.*, 7:39-47.

This "embedding" occurs in two places. First, the terminals are embedded in the contact bar cover when they are installed below the slot columns **324** of connector main body **320**, and held in the openings in the horizontal lip shown in Ex. 1009, Fig. 10.

Second, POSITA would have understood that the "forwardly extended" contact portion of terminals **322** would be embedded in the front section of connector main body **320** to facilitate proper mating with and ensure compatibility with the USB 2.0 standard receptacle into which this connector is inserted. POSITA would have understood the front portion of the terminals **322** (which bend downward) would be fixed, as shown, to secure the contacts and prevent them from bending upward or moving laterally. Ex. 1009, Figs. 9-10 (annotated):

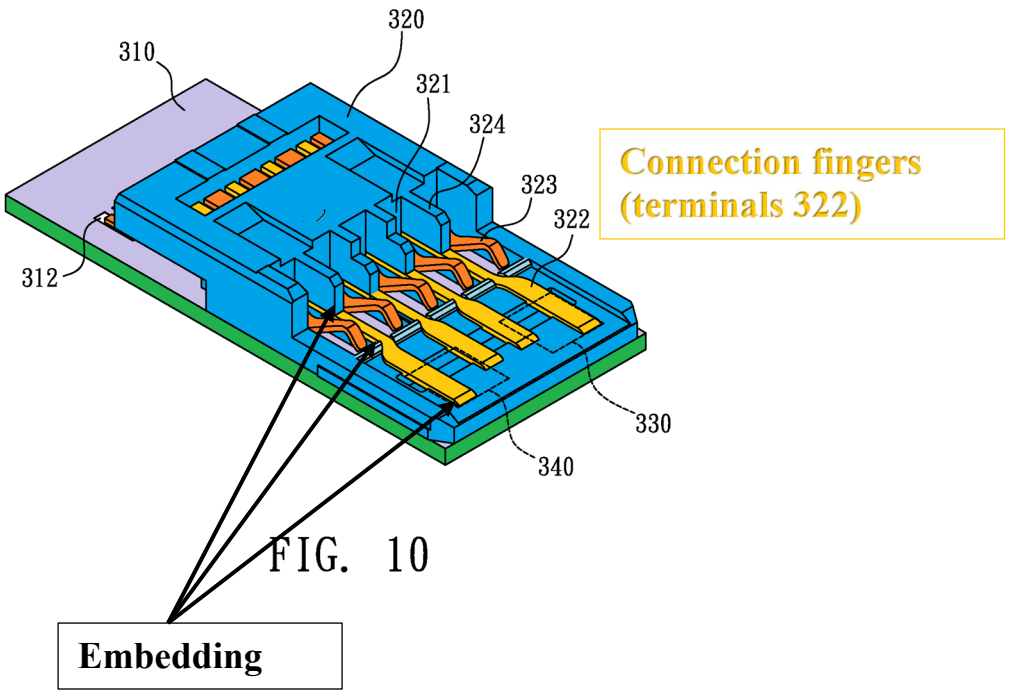


FIG. 10

See Ex. 1005, ¶¶ 251-253.

E. Ground 5: Claim 12 Is Obvious Over Hsiao

As Section XI.D explains, claim 12 is anticipated by Hsiao. To the extent, however, the Board concludes that: (1) the limitation requiring the connection fingers to be embedded to be exposed upon the contact bar cover (*see* XI.D.2) requires the *entire* "forwardly extended" portion of terminals **322** to be embedded in the front portion of the contact bar cover (connector main body **320**), and (2) Hsiao does not explicitly disclose this, Hsiao renders claim 12 obvious.

It would have been obvious to POSITA that the entire "forwardly extended" contact portion of terminals **322** could be embedded in the front portion of connector main body **320**. POSITA would have been motivated to do so to

increase the mechanical strength of the USB 2.0 interface, inhibit lateral movement and upward bending of the contacts, and facilitate mating with a USB 2.0 standard receptacle. POSITA would have had a reasonable expectation of success as embedding USB 2.0 contacts in insulative material in a USB 2.0 plug was commonplace and routine. *See* Ex. 1005, ¶ 254.

F. Ground 6: Claims 11-12 Are Obvious Over Hsiao and Sun

1. Claims 11-12

As Sections XI.D and XI.E explain, Hsiao anticipates and/or renders obvious claims 11-12. To the extent the Board determines that Hsiao does not expressly disclose that Hsiao's "controller" is "configured to access memory," Sun discloses this limitation. Hsiao and Sun combined thus render claims 11-12 obvious.

Sun discloses a USB 2.0/3.0 compatible flash drive having a "USB 3.0 Controller" (control unit **582**). Ex. 1014 at 11-12, Fig. 9. The controller includes "NAND Controller **510**" which "cooperate[s] with the flash memory" to effectuate data transfer to and from the memory, and "Main Controller **530**" connected between the NAND Controller and the USB 2.0 and 3.0 physical layer interfaces ("PHY"). *Id.*

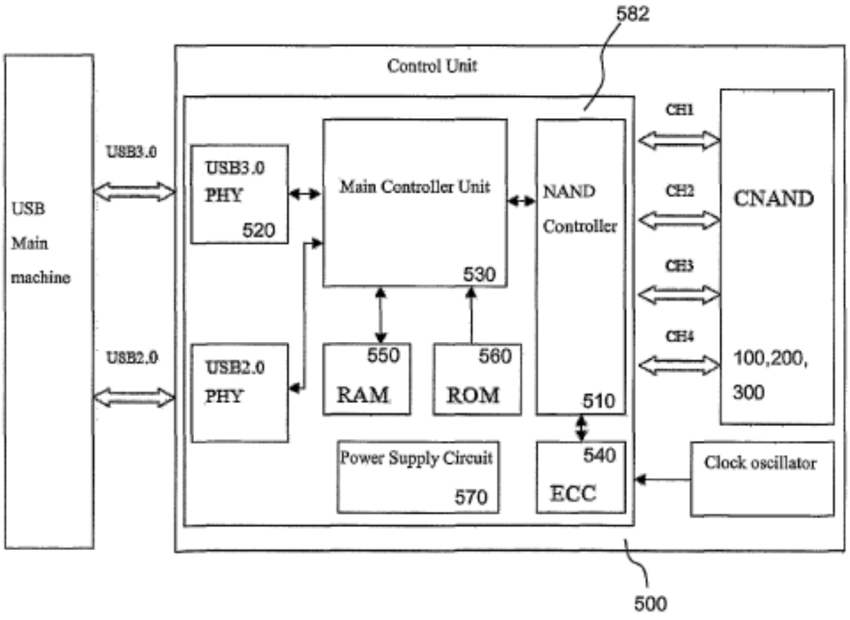


FIG. 9

It would have been obvious to POSITA to configure Hsiao's USB controller **330** to access Hsiao's flash memory **340** in order to effect data transfer to and from memory in compliance with the USB specifications as taught by Sun.

See Ex. 1005, ¶¶ 255-257.

G. Ground 7: Claims 11-12, 14-15 and 18 Are Obvious Over Chen and Cheng

As shown below, Chen and Cheng combined teach all the elements of claims 11-12, 14-15 and 18 and render those claims obvious. Ex. 1005, ¶ 258.

1. Claim 11

[a] An external storage device comprising:

Chen discloses an "external storage device," *i.e.,* memory device **300**. Ex. 1010, Fig. 13, 11:43-48 ("A second embodiment of the present invention is

disclosed in FIG. 13. In this embodiment, the extension to USB is a memory device **300**. The memory device **300** includes an outer case **36** enclosing a printed circuit board with a memory unit (not shown) and an interface **31** electrically connecting with the printed circuit board.")

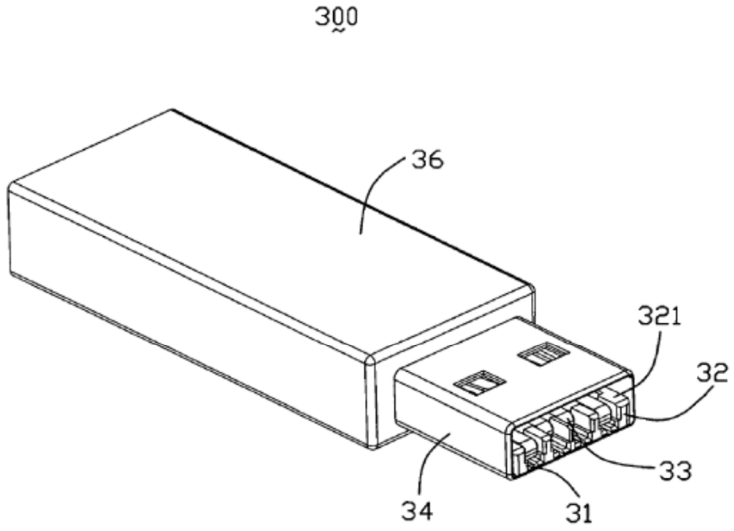


FIG. 13

POSITA would have understood Figure 13 to depict a USB memory device which is an external storage device. *See* Ex. 1005, ¶¶ 259-261.

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

The substrate is the PCB described above, and necessarily has two opposite surfaces. In memory device **300** "tail portions" of the connector plug contacts **33** are "physically and electrically connected to the printed circuit board." Ex. 1010,

11:55-58. The PCB's "connection surface" is the surface to which these "tail portions" are physically and electrically connected. The "component surface" is the opposite PCB surface. Ex. 1005, ¶¶ 262-263.

Moreover, Cheng discloses "a space-minimized flash drive to effectively reduce" the flash drive's length "to miniaturize the flash drive without greatly increasing the manufacturing costs during mass production." Ex. 1012, **[0006].** Cheng's flash drive includes a PCB with two opposite surfaces in which memory is mounted on both surfaces to increase the device's memory capacity without increasing its length. *Id.*, [**0010**], **[0030]**, **[0035]**. It would have been obvious to POSITA to combine Chen and Cheng to create a storage device wherein the PCB has two opposite surfaces, and mount components on both PCB surfaces rather than side-by-side on one surface in order to reduce the device's overall length. Ex. 1005, ¶ 264.

[c]at least one memory die stack mounted on one of the connection surface and the component surface of the substrate;

Chen discloses that memory device **300** includes "a printed circuit board with a memory unit (not shown)." Ex. 1010, 11:45-47. POSITA would have known that this "memory unit" necessarily includes at least one memory die. Ex. 1005, ¶¶ 265-266.

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

Chen does not expressly disclose that memory device **300** includes a controller. Chen, however, teaches that portable USB memory devices require controllers. *See* Ex. 1010, 2:12-18, 2:28-30 ("***peripheral[s], like a portable memory device***," with "type-A USB connector" **500** include "four conductive contacts 53" that "carry the USB signals generated or received ***by a controller chip in the peripherals.***") (emphasis added).

Section X.E explains that Chen discloses a connector plug having two interfaces—a USB 2.0 interface and a "non-USB 2.0" interface. POSITA would have known that memory device **300** has a controller that accesses memory. POSITA would have known that the purpose of a controller is to provide a compatible interface for both protocols between the buses and memory. The controller manages read/write operations between memory and the USB 2.0 and non-USB 2.0 buses to ensure that communications between memory and the buses follow the USB 2.0 protocol and/or the non-USB 2.0 protocol. Ex. 1005, ¶¶ 267-269.

Moreover, Cheng discloses "conventional flash drive[s]" not only have "USB connector[s]" but also "controllers." Ex. 1012, **[0004]**. Cheng discloses a

USB flash drive wherein the controller is mounted on PCB **110** and "electrically connected" to memory and the USB connector, and thus configured to access memory. *Id.*, **[0023], [0029]**. It would have been obvious to POSITA to include a controller in Chen's memory device **300** mounted on the PCB as Cheng teaches. POSITA would have been motivated to do so to provide a compatible interface between the USB 2.0 bus (and the non-USB 2.0 bus) and memory, and have a way to manage read/write operations to and from memory. *See* Ex. 1005, ¶ 270-271.

[e] a contact bar mounted on the connection surface of the substrate, the contact bar including a plurality of portions that are electrically coupled with the substrate and located at a first distance relative to the connection surface of the substrate;

Chen discloses "an extension to USB plug **100**" depicted in Figs. 1-5. Ex. 1010, 5:47-49. In Chen's second embodiment – memory device **300** – the connector is the same as extension to USB plug **100**. Chen states "interface **31** includes a tongue portion **32**, a plurality of contacts **33** supported on a supporting surface **321** of the tongue portion **32**. The tongue portion **32** and the contacts **33** are both with an arrangement same to [that] of the extension to USB plug **100** shown in FIG. 1 which is compatible to [that] of the standard USB connector." *Id.*, 11:43-54; *see also id.*, 11:65-12:22 (describing contacts), claim 3 (claiming memory device). Memory device **300** can mate with either a standard USB

receptacle or the extension to USB receptacle **200** shown in Figure 6 (*id.*, 11:62-65) which requires memory device **300**'s plug to have the same configuration as USB plug **100** extension. Ex. 1005, ¶¶ 272-273.

Chen discloses the claimed contact bar and describes it with reference to figures 2-3 (annotated):

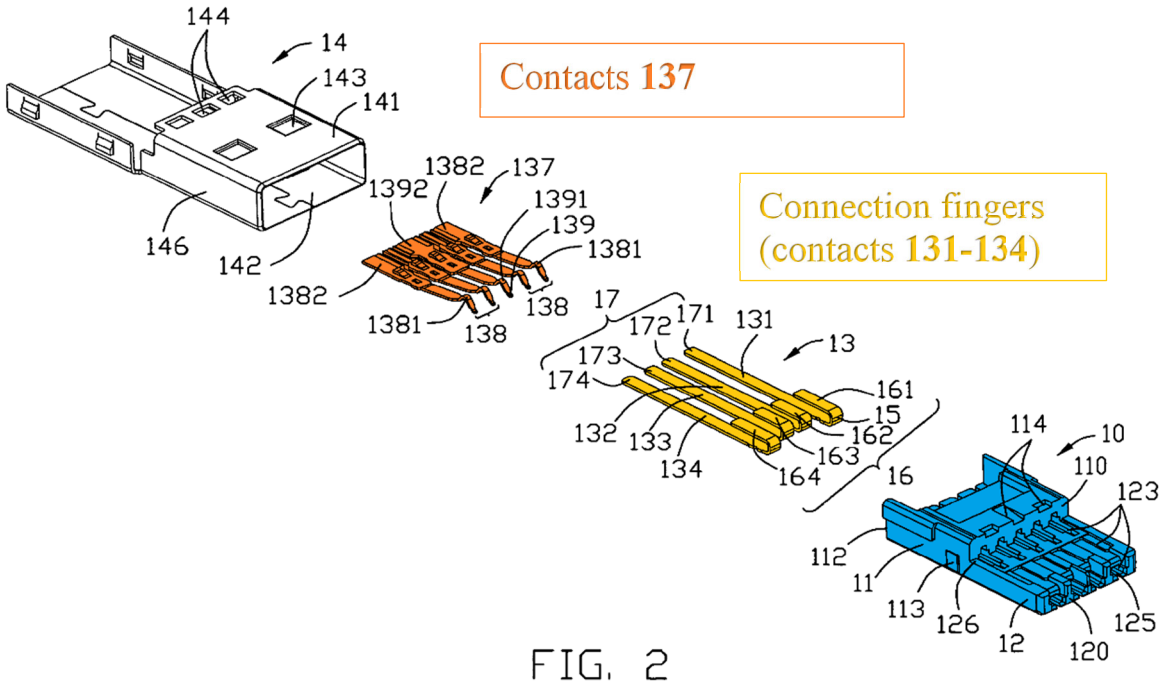


FIG. 2

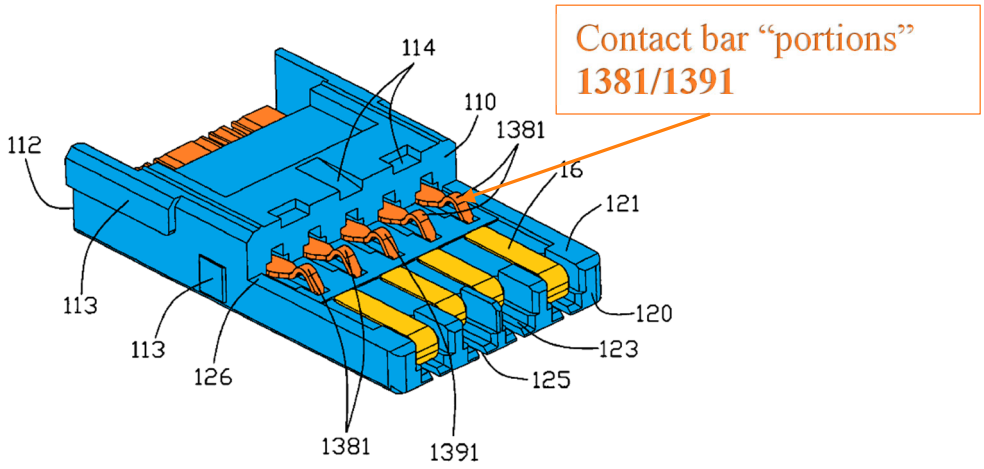


FIG. 3

See Ex. 1005, ¶ 274.

The contact bar including "a plurality of portions that are electrically coupled with the substrate" is housing **10**, with additional contacts **137** installed in passageways **123**. The claimed "portions" are contact portions **1381/1391.** *Id.*, ¶ 275.

"[C]ontacts **13** include four plug conductive contacts designated [**131-134**] and a plurality of additional plug contacts **137**." Ex. 1010, 6:31-34; *see also id.*, 11:66-12:22 (discussing contacts in disclosed embodiments), claim 3. "[C]ontacts **137** include two pairs of differential plug contacts **138** and a grounding plug contact **139**." *Id.*, 7:15-17; *see also id.*, 12:18-22, Fig. 2, claim 3. These contacts have "elastic contact portion[s]" (**1381/1391**). *Id.*, 7:21-22, 7:27-30, Fig. 3.

The housing **10** has "passageways **123** for receiving the additional plug contacts **137**" that "are located behind the passageways **123** for receiving the four plug conductive contacts [**131-134**] along the front-to-rear direction." *Id.*, 6:37-41.

"[E]ach contact portion **1381**, **1391** is cantileveredly received in the passageways **123** and protruding upwardly beyond the supporting surface **121** so that the contact portion **1381**, **1391** is elastic and deformable when engaging with corresponding contacts of the extension to USB receptacle **200**." *Id.*, 7:43-48, Figs. 3-4.

In memory device **300** the contact bar is mounted on the PCB by "physically and electrically" connecting the terminals' "tail portions" to the PCB. Ex. 1010, 11:55-58. Thus, contacts **137** (and portions **1381/1391** of contacts **137**) are "electrically coupled with the substrate." The first distance is the height of contact portions **1381**, **1391** above the PCB surface on which the contact bar is mounted.

See Ex. 1005, ¶¶ 276-279.

[f] a plurality of connection fingers electrically coupled with the substrate, the plurality of connection fingers located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

Chen discloses "connection fingers" as contacts **131-134** which "are substantially of the same configuration" and include "a plug contact portion **16**" that is "flat and non-elastic." Ex. 1010, 6:50-58, Figs. 2-3.

The connection fingers are "electrically coupled with the substrate." *Id.*, 11:55-58 (the contacts' "tail portions" are "physically and electrically connected" to the PCB).

Housing **10** has "[a] plurality of plug contact receiving passageways **123** [that] are recessed in the supporting surface **121** of the plug tongue portion **12**." Ex. 1010, 6:28-30. The passageways are for receiving "the four conductive contacts [**131-134**]." *Id.*, 6:34-37. When these contacts "are inserted into corresponding passageways **123**, each plug contact portion **16** thereof is substantially coplanar with the supporting surface **121** as shown in FIGS. **3-4**." 6:58-62, Figs. 3-4.

The second distance is the height of plug contact portion **16** above the PCB surface. Since plug contact portion **16** is "substantially coplanar with the supporting surface **121**" (*id.*, 6:60-62) and contact bar portions **1381/1391** "protrud[e] upwardly beyond the supporting surface **121**," (*id.*, 7:45-46), the second distance is necessarily less than the first distance. *See id.*, Fig. 4 (annotated) (black arrows show first distance, red arrows show second distance):

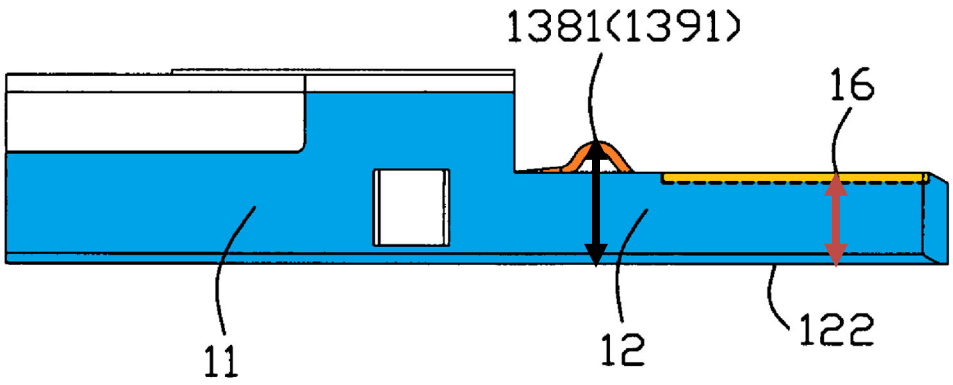


FIG. 4

See Ex. 1005, ¶¶ 280-284.

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of portions of the contact bar.

Chen discloses the plurality of connection fingers (contacts **131-134**), are "for USB protocol to transmit USB signals. In detail, the four conductive contacts [**131-134**] are for power (VBUS) signal, -data signal, +data signal and grounding, respectively." Ex. 1010, 7:59-64, 12:5-9. The contact bar "portions" (**1381/1391** of contacts **137**) are "for a non-USB protocol." *Id.*, 12:14-19; Ex. 1005, ¶¶ 285-287.

2. Claims 12, 14-15 and 18

Claims 12, 14-15 and 18 depend from claim 11. *See* Appendix A. Section XI.G.1 explains that Chen and Cheng combined disclose the elements of claim 11 and render it obvious. As explained below, Chen and Cheng combined also

disclose the additional elements of claims 12, 14-15 and 18, and render them obvious. Ex. 1005, ¶ 288.

a) Claim 12

Claim 12 requires the external storage device's "contact bar comprises a cover," and the "connection fingers are embedded to be exposed upon" the contact bar cover. Appendix A. Chen discloses this limitation.

The contact bar cover is insulative housing **10** in which "[a] plurality of plug contact receiving passageways **123** are recessed in the supporting surface **121** of the plug tongue portion **12**." Ex. 1010, 6:28-30. The passageways are for receiving "the four conductive contacts [**131-134**]." *Id.*, 6:34-37. When these contacts "are inserted into corresponding passageways **123**, each plug contact portion **16** thereof is substantially coplanar with the supporting surface **121** as shown in FIGS. **3-4**." *Id.*, 6:58-62, Fig. 3 (annotated):

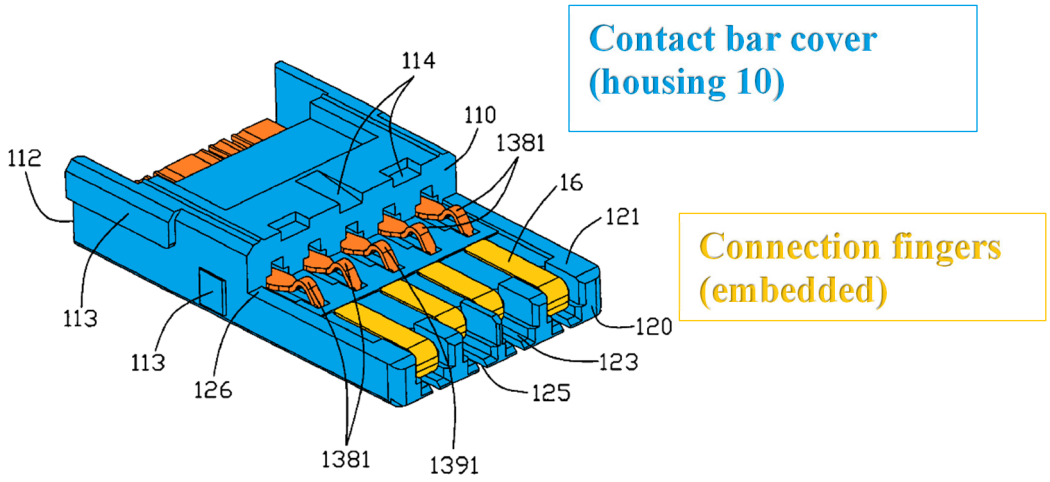


FIG. 3

They are thus embedded to be exposed upon the contact bar cover.

See Ex. 1005, ¶¶ 289-291.

b) Claims 14-15

Claims 14 and 15 require that at least one memory die stack is mounted on the same substrate surface as the contact bar (claim 14) or at least one memory die stack is mounted on both substrate surfaces (claim 15). Appendix A.

Chen's memory device **300** includes "an printed circuit board with a memory unit (not shown)" (Ex. 1010, 11:45-47), however, Chen does not state which PCB surface the "memory unit" is mounted on. It would have been obvious to POSITA to mount the memory die stack on the same surface as the contact bar, where POSITA was most concerned with minimizing the device's thickness. Ex. 1005, ¶¶ 292-293.

Moreover, section XI.A.7 explains that Cheng discloses memory die stacks mounted on both PCB surfaces, thus meeting the requirements of both claims 14 and 15. Cheng explains that mounting flash memory on both PCB surfaces permits miniaturization of a flash memory device by keeping device length smaller while providing for "higher memory capacities." Ex. 1012, [**0010**], [**0030**]; *see also* Section XI.A.7. POSITA would have been motivated to utilize Cheng's memory layout, which includes at least one memory die stack mounted on both PCB surfaces (and thus the same surface as the contact bar) in Chen's memory device **300** in order to increase memory capacity without substantially increasing device length. *See* Ex. 1005, ¶ 294.

3. Claim 18

Claim 18 requires the first and second distances each comprise heights above the substrate's connection surface, and the second height is less than the first. Appendix A. Section XI.G (elements [e]-[f]) explain that in Chen, the first distance is the height of contact bar portions **1381**, **1391** above the PCB surface on which the contact bar is mounted, and the second distance is the height of plug contact portion **16** of terminals **131-134** above that surface. As Figure 4 shows, the second height is less than the first height.

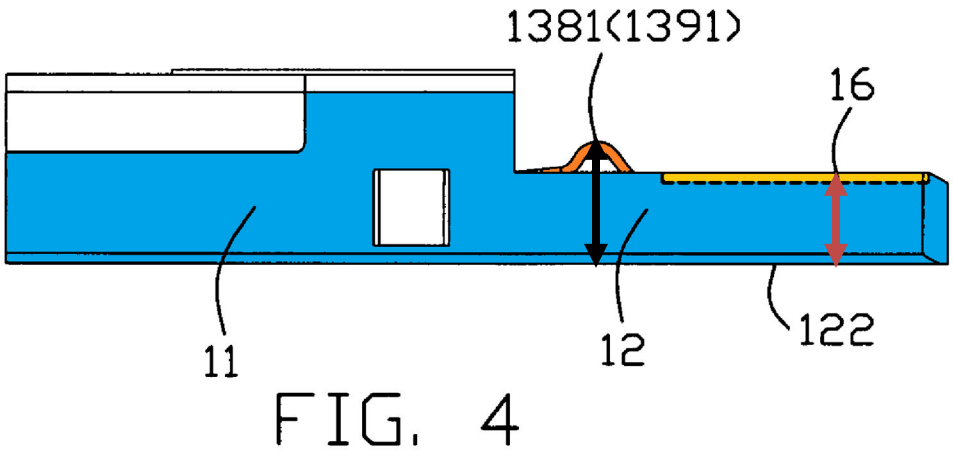


FIG. 4

Ex. 1010, Fig. 4 (annotated) (black arrow shows first distance, red arrow shows second distance). *See* Ex. 1005, ¶ 295.

H. Ground 8: Claims 16 and 17 Are Obvious Over Chen and Cheng and Further in View of Hiller

Claim 16 depends from claim 15 and claim 17 depends from claim 16. Claim 16 requires that "each of the plurality of memory die stacks" recited in claim 15, has "a plurality of memory dies," and claim 17 requires that the plurality of memory dies for at least two memory die stacks are "stacked in an overlapping arrangement." Appendix A.

Section XI.G.2.b explains that Chen and Cheng combined teach the elements of claim 15 and render it obvious. Cheng discloses mounting a memory die stack on both PCB surfaces but does not expressly disclose that the stacks include a "plurality of dies."

Section XI.B explains that Hiller (Ex. 1013) discloses memory die stacks using multiple dies and describes a "conventional approach" to memory die stacking that includes stacking "same-sized dies with overhanging designs." Ex. 1013, **[0003]**. Hiller also discloses "a memory device comprising at least one memory stack of stacked memory dies which are staggered with respect to each other." *Id.*, **[0004]**; Figs. 8-9, 18:

FIG 8

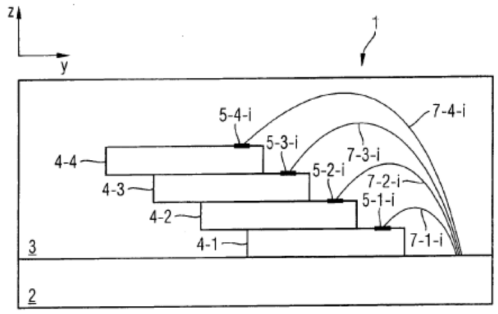


FIG 9

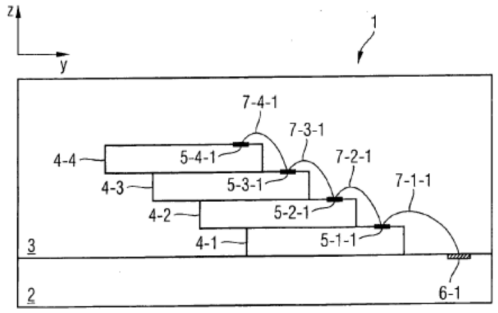
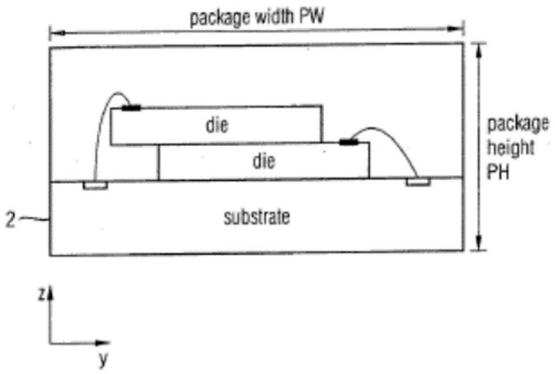


FIG 18



It would have been obvious to POSITA to utilize this conventional approach to memory die stacking in Chen's device, and POSITA would have been motivated to do so because using stacks having multiple dies allows for a memory device with greater storage capacity contained in a smaller space. Moreover, the overlapping arrangement facilitates wire bonding of the dies to the PCB while minimizing the need to increase the PCB length. Ex. 1005, ¶¶ 296-299. Claims 16 and 17 therefore are obvious over Chen and Cheng in view of Hiller. *Id.*

I. Ground 9: Claim 19 is Obvious Over Chen and Cheng and Further in View of Wan

Claim 19 depends from claim 11 and requires that "the external storage device is configured to support Universal Serial Bus ("USB") 2.0 and USB 3.0 standards in effect as of Jan. 31, 2011." Appendix A. Section XI.G.1 explains that Chen and Cheng combined teach the elements of claim 11, and render it obvious. Wan "provide[s] a plug connector that complies with USB 2.0 and 3.0

Specifications." Ex. 1015, 1:47-49. Wan's plug connector has the same two-tier contact arrangement disclosed in Chen, and Wan explains that the first contacts **12** "comply with a USB 2.0 specification" and the second contacts **22** "comply with a USB 3.0 specification." *Id.*, 2:40-41, 3:38-39, Figs. 2, 4:

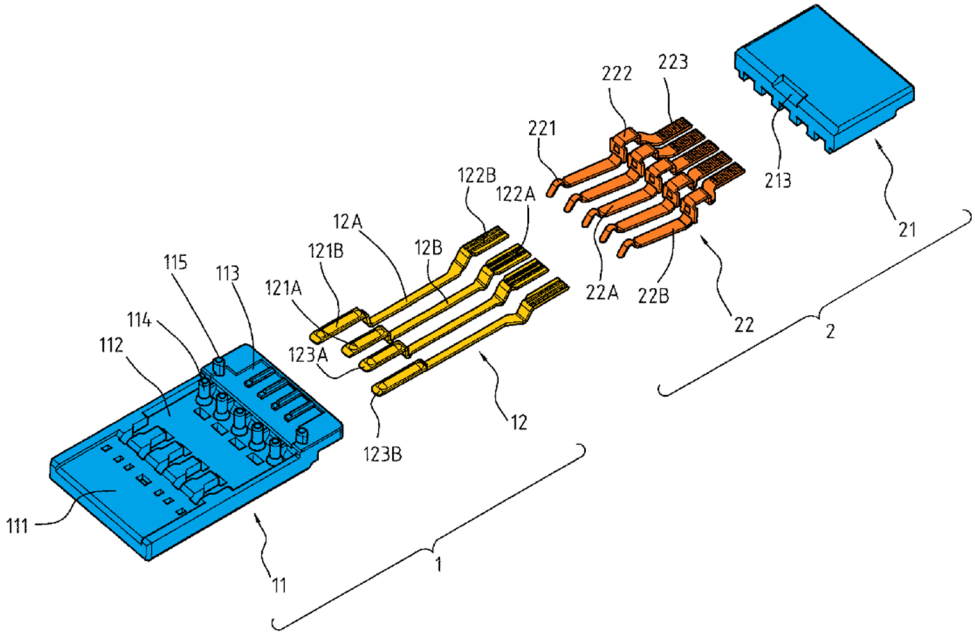


Fig. 2

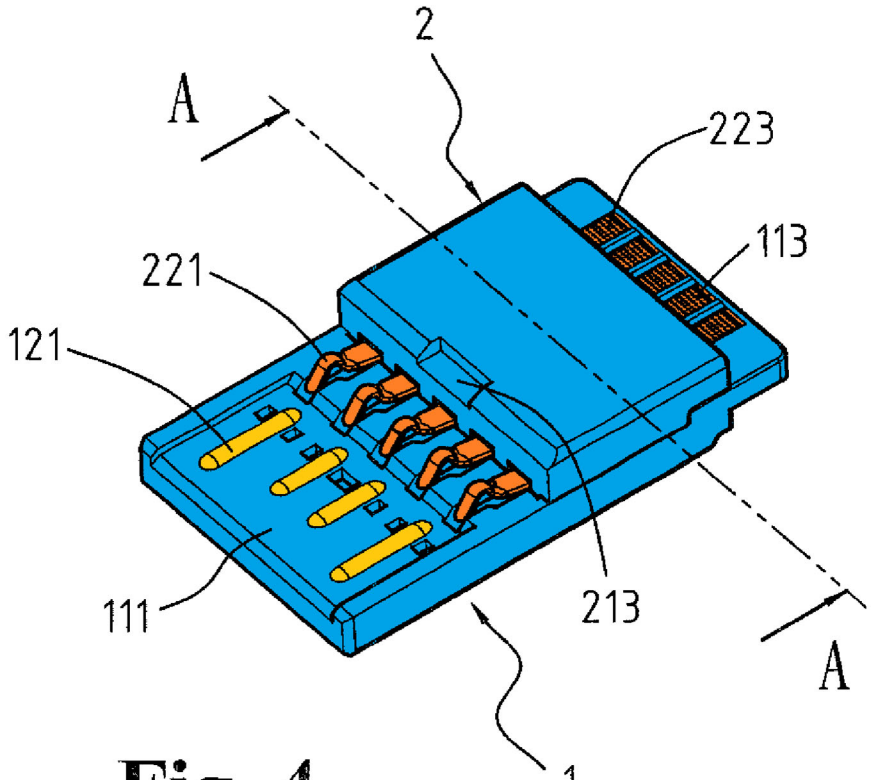


Fig. 4

Chen, Cheng and Wan combined teach the elements of claim 19 and render it obvious. It would have been obvious to POSITA in view of Wan's disclosure to configure Chen's memory device **300** to support USB 2.0 and 3.0 standards. POSITA would have been motivated to do so to meet market demand for a faster device (one that implements USB 3.0's SuperSpeed protocol) but that retains the USB 2.0 plug's smaller form factor, and POSITA would have had a reasonable expectation of success in doing so. Ex. 1005, ¶¶ 300-302.

Chen's memory device **300** has a plug with two sets of contacts supporting two interfaces, one of which (conductive contacts **131-134**) is for USB 2.0 signals. *See* Section XI.G.1(element [g]); Ex. 1010, 5:37-41 ("standard USB" refers to USB 2.0), *id*., 12:5-9 (contacts **131-134** compatible with "standard USB" receptacle).

Additional "contacts **137** include two pairs of differential plug contacts **138**" for "transferring/receiving high-speed signals" (Ex. 1010, 7:15-21), and support a second "non-USB protocol." *Id.*, 12:14-17. POSITA would have understood "non-USB protocol" to refer to a "non-USB **2.0**" protocol because (1) as of Chen's filing date, June 13, 2007, the USB 3.0 standard had not issued, (2) Chen discloses that "standard USB" refers to USB 2.0, and (3) Chen's Abstract states that the "differential contacts are adapted for non-USB 2.0 protocol." *See* Ex. 1005, ¶¶ 303-304; *see also* Ex. 1019, ¶¶ 1-10.

Chen teaches that the purpose of his two-tier contact arrangement is to support the USB 2.0 protocol while providing an additional set of contacts necessary to support another higher speed bus architecture, stating "[t]o provide a kind of connector with a small size and a high transmission rate for portability and high data transmitting efficiency is much desirable." Ex. 1010, 3:10-12. POSITA would have been familiar with the USB 3.0 Specification and understood that it provides a dual-bus architecture operating in parallel—one to support USB 2.0 and

one to support USB 3.0 SuperSpeed which is significantly faster than USB 2.0. *See* Section IV.B. POSITA would also have understood that Chen's second contacts **137** are exactly those required to support SuperSpeed in Standard-A plugs and Chen's arrangement of contact sets **131-134** and **137** is identical to that specified in the USB 3.0 Specification for supporting the dual-bus architecture. Accordingly, claim 19 is obvious over Chen and Cheng and further in view of Wan. Ex. 1005, ¶¶ 305-306.

XII. CONCLUSION

Petitioner requests *Inter Partes* Review of the Challenged Claims pursuant to Grounds 1-9.

XIII. PAYMENT OF FEES – 37 C.F.R. § 42.15(a)

The director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 502587 for this Petition and further authorizes payment for any additional fees to be charged to this Deposit Account.

DATED this 4th day of August, 2020.

Respectfully submitted,

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APPENDIX A

U.S. Patent No. 8,693,206 Claim Listing

1. [a] An external storage device comprising:

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

[c] at least one memory die stack mounted on one of the connection surface and the component surface of the substrate;

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

[e] a contact bar mounted on the connection surface of the substrate, the contact bar comprising a plurality of extensions, each of the plurality of extensions including a portion that is located at a first distance relative to the connection surface of the substrate;

[f] a plurality of connection fingers embedded to be exposed upon the connection surface of the substrate at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of extensions of the contact bar.

2. The external storage device of claim 1, wherein the contact bar further comprises a cover.

3. The external storage device claim 1, wherein the at least one memory die stack and the contact bar are mounted on the same surface of the substrate.

4. The external storage device of claim 1, wherein each extension includes a projection, the projection configured to be located at the first distance in an uncompressed position.

5. The external storage device of claim 1, further comprising a plurality of memory die stacks, wherein at least one of the plurality of memory die stacks is mounted on the connection surface of the substrate, and at least one of the plurality of memory die stacks is mounted on the component surface of the substrate.

6. The external storage device of claim 5, wherein each of the plurality of memory die stacks comprises a plurality of dies.

7. The external storage device of claim 6, wherein the plurality of dies of at least two of the plurality of memory die stacks are stacked in an overlapping arrangement.

8. The external storage device of claim 1, wherein the substrate comprises a printed circuit board.

9. The external storage device of claim 1, wherein the first distance comprises a first height above the connection surface, and the second distance comprises a second height above the connection surface, wherein the second height is less than the first height.

10. [a] An external storage device comprising:

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

[c] at least one memory die stack mounted on one of the connection surface and the component surface of the substrate;

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

[e] a contact bar mounted on the connection surface of the substrate, the contact bar comprising a plurality of extensions, each of the plurality of extensions including a portion that is located at a first distance relative to the connection surface of the substrate;

[f] a plurality of connection fingers embedded to be exposed upon the connection surface of the substrate at a second distance relative to the

connection surface of the substrate, the second distance being less than the first distance; and

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of extensions of the contact bar; and

[h] wherein the external storage device is configured to support Universal Serial Bus ("USB") 2.0 and USB 3.0 standards in effect as of Jan. 31, 2011.

11. [a] An external storage device comprising:

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

[c] at least one memory die stack mounted on one of the connection surface and the component surface of the substrate;

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

[e] a contact bar mounted on the connection surface of the substrate, the contact bar including a plurality of portions that are electrically coupled with the substrate and located at a first distance relative to the connection surface of the substrate;

[f] a plurality of connection fingers electrically coupled with the substrate, the plurality of connection fingers located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of portions of the contact bar.

12. The external storage device of claim 11, wherein the contact bar comprises a cover and wherein the plurality of connection fingers are embedded to be exposed upon the cover of the contact bar.

13. The external storage device of claim 11, wherein the plurality of connection fingers are embedded to be exposed upon the substrate.

14. The external storage device claim 11, wherein the at least one memory die stack and the contact bar are mounted on the same surface of the substrate.

15. The external storage device of claim 11, further comprising a plurality of memory die stacks, wherein at least one of the plurality of memory die stacks is mounted on the connection surface of the substrate, and at least one of the plurality of memory die stacks is mounted on the component surface of the substrate.

16. The external storage device of claim 15, wherein each of the plurality of memory die stacks comprises a plurality of dies.

17. The external storage device of claim 16, wherein the plurality of dies of at least two of the plurality of memory die stacks are stacked in an overlapping arrangement.

18. The external storage device of claim 11, wherein the first distance comprises a first height above the connection surface, and the second distance comprises a second height above the connection surface, wherein the second height is less than the first height.

19. The external storage device of claim 11, wherein the external storage device is configured to support Universal Serial Bus ("USB") 2.0 and USB 3.0 standards in effect as of Jan. 31, 2011.

APPENDIX B

EXHIBIT LIST

Exhibit #	Reference
1001	U.S. Patent No. 8,693,206 (“’206”)
1002	Provisional Application No. 61/438,139
1003	Provisional Application No. 61/442,379
1004	’206 Prosecution History (as downloaded from USPTO Public Pair)
1005	Declaration of R. Jacob Baker, Ph.D., P.E.
1006	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
1007	USB 2.0 Specification
1008	USB 3.0 Specification
1009	U.S. Patent 8,480,435 (“Hsiao”)
1010	U.S. Patent 7,625,243 (“Chen”)
1011	U.S. Patent 7,909,654 (“He”)
1012	U.S. Patent Application Publication 2009/0098773 (“Cheng”)
1013	U.S. Patent Application Publication 2008/0150111 (“Hiller”)
1014	WIPO Publication WO 2011/160321 (“Sun”) (also published as US Patent Application Publication 2012/0203954).

1015	U.S. Patent 7,563,140 ("Wan")
1016	Exhibits C and D to Complaint filed in *Kuster v. Western Digital Technologies, Inc.*, Case No. 6:20-cv-00563 ADA (W.D.Tex.)
1017	U.S. Patent Application Publication 2008/0093720 ("Hiew")
1018	U.S. Patent Application Publication 2005/0070138 ("Chiou")
1019	Declaration of Jeffrey L. Ravencraft
1020	Supp. Order re Court Operations During COVID-19 Pandemic (W.D.Tex. Jul. 2, 2020)
1021	USPTO update on in-person meetings available at https://www.uspto.gov/about-us/news-updates/uspto-update-person-meetings (last downloaded 7/25/2020)
1022	Complaint (without Exhibits) filed in *Kuster v. Western Digital Technologies, Inc.*, Case No. 6:20-cv-00563 ADA (W.D.Tex.)

CERTIFICATION OF WORD COUNT UNDER 37 C.F.R. § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition For *Inter Partes* Review Of U.S. Patent No. 8,693,206 totals 13,962 excluding the table of contents, table of authorities, mandatory notices under § 42.8, Appendix A (claim listing) and Appendix B (exhibit list), Certificate of Service and this Certification of Word Count.

This word count was made by using the built-in word count function tool in the Microsoft Word software used to prepare the document.

DATED this 4th day of August, 2020.

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. §§ 42.6 and 42.105, that a complete copy of the attached PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,693,206, including all Exhibits and related documents, was served on August 4, 2020, via overnight carrier upon the Patent Owner by serving the correspondence address of record with the USPTO as follows:

Kilpatrick Townsend & Stockton LLP
Mailstop: IP Docketing – 22
1100 Peachtree Street
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and is being served via overnight carrier and email on August 4, 2020 upon counsel of record for the Patent Owner in the litigation pending before the U.S. District Court for the Western District of Texas (Waco) entitled *Kuster v. Western Digital Technologies, Inc.,* 6:20-cv-00563 ADA as follows:

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DATED this 4th day of August, 2020.

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