UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CREE, INC.
Petitioner

v.

DOCUMENT SECURITY SYSTEMS, INC.
Patent Owner

Case IPR2020-_____
U.S. Patent No. 6,784,460

PETITION FOR *INTER PARTES* REVIEW OF U. S. PATENT NO. 6,784,460 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *ET SEQ.*

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1005	U.S. Patent No. 6,784,463 ("Camras")
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I. MANDATORY NOTICES (37 C.F.R. § 42.8)

A. Real Party-In-Interest

The real party in interest is Cree, Inc.

B. Related Matters

The following matter is related: *Document Security Systems, Inc. v. Cree, Inc.*, No. 2-19-cv-08141 (C.D. Cal.).

C. Lead and Back-Up Counsel

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II. INTRODUCTION

This Petition establishes a reasonable likelihood that at least one of claims 1-8 of U.S. Patent No. 6,784,460 ("the '460 patent") is unpatentable. Petitioner requests that the Board institute *inter partes* review.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW PETITION

A. Certification of Standing

Petitioner certifies that the '460 patent is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting *inter Partes* review on the grounds identified herein.

B. Fee

The Director is authorized to charge any fees specified by 37 C.F.R. § 42.15(a) to Deposit Accout No. 17-0055.

C. Proof of Service

Proof of service of this Petition is provided in Attachment A.

IV. IDENTIFICATION OF CHALLENGED CLAIMS (37 C.F.R. § 42.104(B))

All claims are asserted to be obvious under 35 U.S.C. §103. The references relied upon for each ground are as follows:

- Ground 1: Claims 1-7 are rendered obvious by ***Slater***.
- Ground 2: Claims 1-7 are rendered obvious by ***Slater*** in view of ***Steigerwald***.

- Ground 3: Claims 1-7 are rendered obvious by ***Slater*** in view of ***Steigerwald*** and ***Haitz***.

- Ground 4: Claims 1-8 are rendered obvious by Applicant's Admitted Prior Art ("***AAPA***") in view of ***Camras***

- Ground 5: Claims 1-7 are rendered obvious by ***AAPA*** in view of ***Steigerwald and Haitz.***

V. OVERVIEW OF THE ’460 PATENT

The '460 patent, entitled "Chip Shaping For Flip-Chip Light Emitting Diode" has a priority date of October 10, 2002. Ex. 1001, col. 1. The '460 patent describes a method of fabricating a semiconductor flip-chip light emitting diode ("LED") to improve light extraction. Ex. 1001, 1:7-10; 39-41. "Flip-chip" refers to a packaging technique where a device is fabricated by depositing layers on a substrate, which is then inverted, such that the substrate is above the active semiconductor layers. Ex. 1012, ¶48. The '460 patent states that prior art flip-chip LEDs were fabricated on and emited light through substrates having a "cuboidal shape (e.g., a rectangular prism)", as in FIG. 1. Ex.1001, 1:13-19.

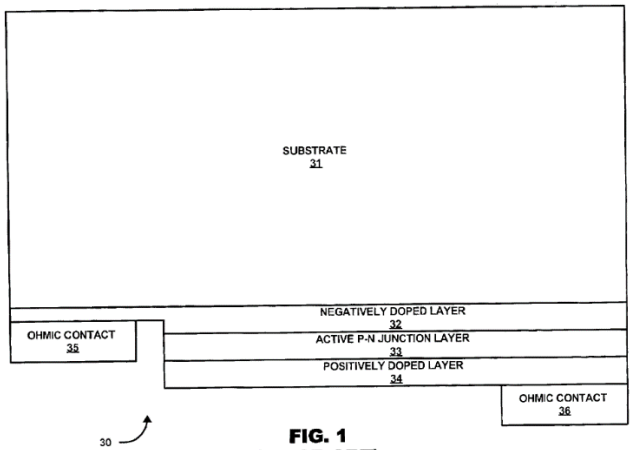


FIG. 1
(PRIOR ART)

FIG. 2 shows the drawback of a cuboidal substrate. Because of the difference between the optical index of refraction of the substrate and the surrounding environment, light emitted from an active p-n junction layer at angles within "trap cones" is trapped within the substrate by total internal reflection ("TIR"). See Ex. 1001, 1:22-38; Ex. 1012, ¶29.

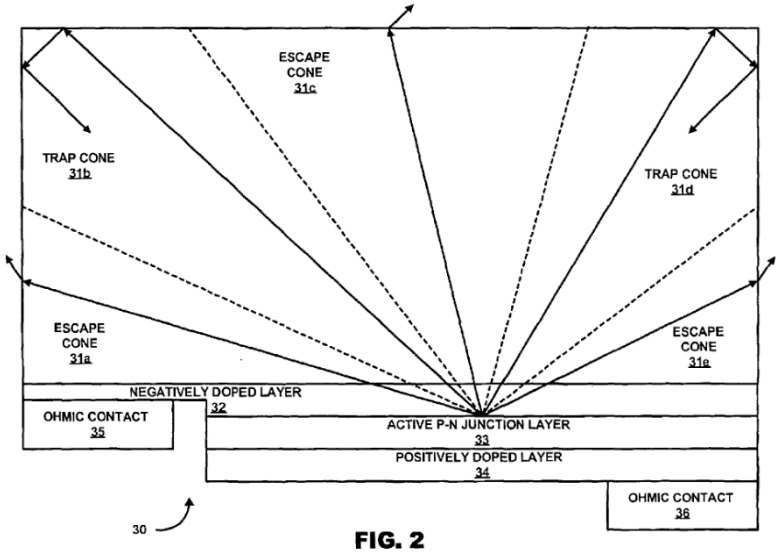


FIG. 2
(PRIOR ART)

The '460 patent addresses this problem by providing substrates having a

pyramidal shape. Ex. 1001, 2:22-23; 3:1-2. Such shapes (see FIGs. below), enable light to escape the substrate that would otherwise be trapped by TIR, because more light intersects the walls of the substrate at angles that are less than the "critical angle", i.e., the angle of TIR. See *Id*., 2:26-35; 3:5-15 and Ex. 1012, ¶¶30, 39-40.

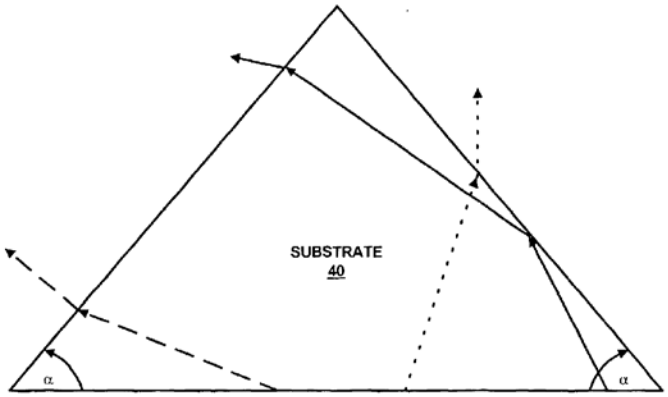


FIG. 3

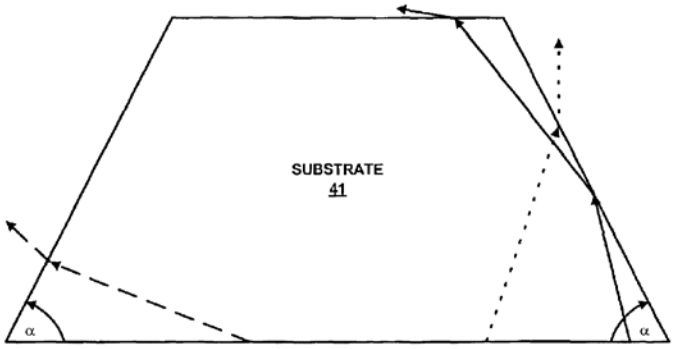


FIG. 9

The '460 patent has 8 claims. Claims 1, 6 and 8 are independent.

The chart below illustrates the repeated language and differences between independent claims 1, 6 and 8.

1[p] A semiconductor light-emitting diode of flip-chip design, comprising:	**6[p]** [Same as **[1[p]**]	**8[p]** [Same as **[1[p]**]
1[a] a light-emitting region including a negatively doped layer, a positively doped layer, and an active p-n junction layer between said negatively doped layer and said positively doped layer;	**6[a]** a light-emitting region including a first doped layer, a second doped layer, and an active p-n junction layer between said first doped layer and said second doped layer;	**8[a]** [Same as 6**[a]**]
1[b] a transparent substrate overlying said light-light emitting region,	**6[b]** and a first transparent substrate adjacent said first doped layer,	**8[b]** [Same as **6[b]**]
1[c] said substrate having a pyramidal shape so that said substrate has a cross-	**6[c]** said first transparent substrate having a pyramidal shape that said	**8[c]** [Same as **6[c]**]

sectional area that decreases with distance from said junction	substrate has a cross-sectional area that decreases with distance from said junction	
1[d] and wherein lateral extent of said substrate is bound by lateral extent of a doped layer nearest to the transnarent substrate;	**6[d]** [Same as 1**[d]**]	**8[d]** and wherein lateral extent of said substrate is bound by lateral extent of said <u>first doped layer</u>;
1[e] and ohmic contacts for forward biasing said junction layer so that at least most of the light is emitted from the junction layer into the surrounding environment is emitted through said substrate.	**6[e]** [Same as **[1[e]**]	**8[e]** [Same as **[1[e]**]
		8[f] and wherein an upper portion of said first doped

		layer has a pyramidal shape.

The differences between dependent claims 2 and [7] are shown below:

2 and [7]. The semiconductor light emitting diode of claim 1, wherein said substrate [first transparent substrate] has a side surface and a bottom surface, and wherein a slope angle of said side surface relative to said bottom surface is within a range of [1]10-80 degrees.

VI. RELEVANT PROSECUTION HISTORY

As originally filed, claim 1 read

A semiconductor light emitting diode of flip-chip design, comprising:

a light emitting region including

a negatively doped layer

a positively doped layer; and

an active p-n junction layer between said negatively doped layer and said positively doped layer; and

a first transparent substrate overlying said light emitting region, said first transparent substrate having a pyramidal shape.

Id. at 142.

In a first Office Action, the Examiner rejected all claims over ***Krames*** (Ex.

1007), which describes an LED having an inverse pyramidal substrate (12 in FIG. 2, below). Ex. 1002 at 80-86.

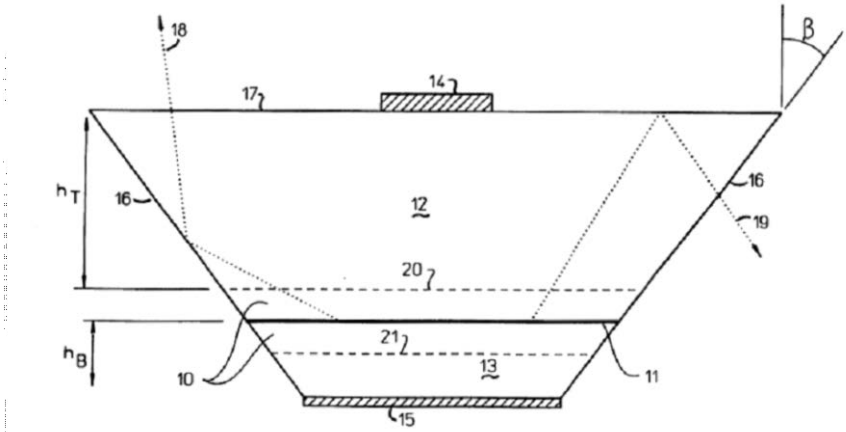


Figure 2

Applicant amended then independent claims 1 and 14 to distinguish over ***Krames***:

1. (currently amended) A semiconductor ~~light~~ light-emitting diode of flip-chip design, comprising:

a ~~light~~ light-emitting region including

a negatively doped layer

a positively doped layer; and

an active p-n junction layer between said negatively doped layer and said positively doped layer; ~~and~~

a ~~first~~ transparent substrate overlying said light emitting region, said ~~first transparent~~ substrate having a pyramidal shape so that said substrate has a cross-sectional area that decreases with distance from said junction; and

ohmic contacts for forward biasing said junction layer so that at least most of the

light is emitted from said junction layer into a surrounding environment is emitted through said substrate.

Ex. 1002 at 66. Applicant argued that the addition of the "ohmic contacts" limitation distinguished ***Krames***, where

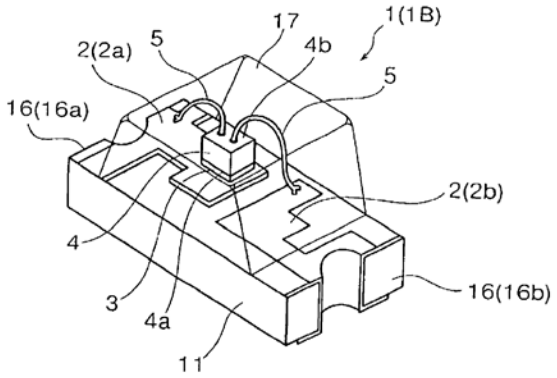
> Most of the light generated at an active region appears to exit through window 12, which widens with distance from the active region 11. Window 13 narrows with distance from the action region, but an ohmic contact 15 occludes light from exiting the distal surface, while a corresponding contact 14 only occludes a fraction of the area of distal surface 17 of top window 12. Thus, very little, if any, of the light exiting Krames LED exits window 13.

Id., at 69.

Thus, Applicant amended the claims to require ohmic contacts that enable more light to be emitted from the pyramidal substrate into the surrounding environment than from other surfaces.

The Examiner rejected all independent claims over ***Fujiwara*** (Ex. 1009), which shows an LED packaged with a "light emanating mold" 17 in FIG. 5, below, having no occlusive contacts on its outside surface . Ex. 1002 at 53-59.

FIG.5



In response, Applicant added to all independent claims: "wherein lateral extent of said substrate is bound by lateral extent of said light-emitting region." *Id*. at 31-33. An Examiner's Amendment changed "bound by lateral extent of said light-emitting region" to "bound by lateral extent of a doped layer nearest to the transparent substrate" for the claims that became 1 and 6, and a similar change was made to claim 17, which became claim 8. *Id*. at 16-18.

The "bound" limitation does not have textual support in the specification, but Applicant stated, that "bound" was "repeat[ly] illustrated in the Figures of the present patent application." Ex. 1002 at 35. Applicant also stated, "[a]s we discussed during the interview, this structure [the "bound" limitation] results from the fabrication process used to deposit the substrate above the light emitting region of the diode". *Id*. at 35-36.

Applicant distinguished ***Fujiwara***, in part by arguing that the lateral extent of ***Fujiwara's*** "mold" 17 was not "bound by lateral extent of said light-emitting region" as

required by the amended claims, because "Fujuwara's [sic] Figure 5 illustrates a mold 17 that completely surrounds and engulfs its 'luminous element 4' on all sides and even below the bottom plane of the 'luminous element 4'". Ex. 1002 at 36.

VII. CLAIM CONSTRUCTION

Claim terms should be given the ordinary meaning that the terms would have to a person of ordinary skill in the art on the earliest effective filing date, in view of the specification and file history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005); 37 C.F.R. § 42.100(b).

For all claim terms except those specifically identified below, Petitioner applies the plain and ordinary meaning and contends that no further construction is necessary to resolve the question of patentability. See, e.g., A*urobindo Pharma USA, Inc. v. Andrx Corp. et al.*, IPR2017-01648, Paper 34 at 11 (PTAB Dec. 28, 2018) ("We address the construction of only certain claim terms raised by the parties, and we do so only to the extent necessary to determine whether Petitioner has demonstrated unpatentability by a preponderance of the evidence.").

Petitioner does not waive any argument in any litigation that claim terms in the '460 patent are indefinite or otherwise invalid, or its right to raise additional issues of claim construction in any litigation.

A. "ohmic contacts … so that at least most of the light is emitted from the junction layer into the surrounding environment is emitted through said substrate" (claims 1, 6 and 8)

1. "[S]o that at least most" recites an intended result, and has no patentable weight.

The phrase "ohmic contacts…so that at least most of the light is emitted from the junction layer into the surrounding environment is emitted through said substrate" ("the 'most' recitation") states an intended result of the preceding structural elements, namely, the presence of the ohmic contacts, and has no patentable weight. The recitation does not recite a structural limitation for the claim independent of the ohmic contacts.

"[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett–Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990) (emphasis in original). "[T]he patentability of apparatus or composition claims depends on the claimed structure, not on the use or purpose of that structure." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 809 (Fed. Cir. 2002). Here, the "so that" clause merely describes the effect of the preceding structural limitations, and a "clause that merely states the result of the limitations in the claim adds nothing to the patentability or substance of the claim." *Texas Instruments Inc. v. U.S. Int'l Trade Comm'n*, 988 F.2d 1165, 1172 (Fed. Cir. 1993). In a case where an apparatus claim recites an intended result of some structure, that recitation is inherently disclosed by any prior art having the same structure. See *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

2. If limiting, the recitation only requires that the ohmic contacts occlude the substrate less than other device surfaces.

If limiting, the recitation should be read to require arrangement of ohmic contacts such that they block light from the substrate less than they block light from other device surfaces.

The claim language itself ties the "most" recitation to the previously recited ohmic contacts, so if the recitation imposes any structural limitation, it is on the ohmic contacts.

The file history clarifies how the recitation and the ohmic contacts are linked. The "most" recitation was added in prosecution, at the same time as the ohmic contacts limitation, to distinguish over FIG. 2 of ***Krames*** (below).

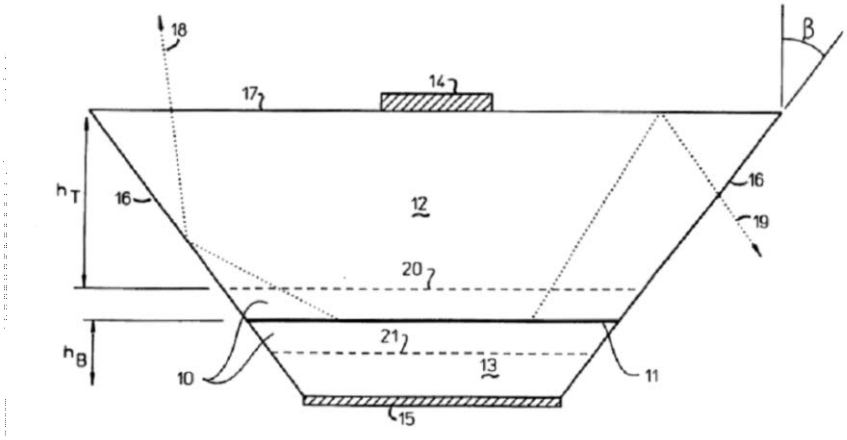


Figure 2

Applicant distinguished ***Krames*** by pointing out that its truncated pyramidal window 13 was occluded by contact 15, while its inverse pyramidal window 12 was less occluded by contact 14. Ex. 1002 at 69. Thus, the file history suggests that, at most, the recitation means that the ohmic contacts must be arranged such that they block less

light from being emitted from the pyramidal substrate into the surrounding environment than from other surfaces of the device.

This is consistent with the specification, where all embodiments are pictured having ohmic contacts on the bottom of the device, where they do not block light from being emitted from the substrate but do block light from being emitted from other device surfaces. See, Ex. 1001, FIG. 16, below. The '460 patent's specification contains no textual support for the "most" recitation. Thus, the only support for the "most" recitation is the Figures, which simply show ohmic contacts on the bottom of the device.

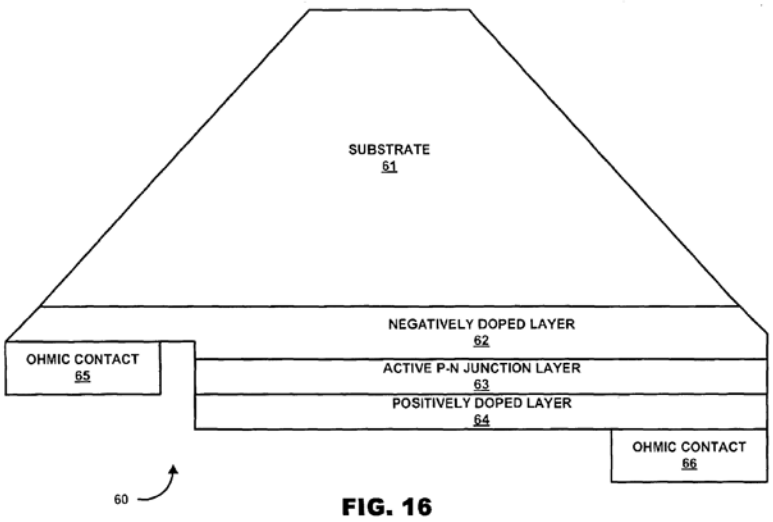


FIG. 16

VIII. DEFINITION OF THE POSA

M.P.E.P. §2141.03 sets forth the elements to be considered in determining the qualifications of the POSA. In view of the type of problems encountered in the art and

the prior art solutions to those problems, the person of ordinary skill in the art ("POSA") for the '460 patent would have had a B.S. in electrical engineering or a related field, and four years' experience designing LED packages. Ex. 1012, ¶¶23-26. This description is approximate, and a higher level of education or skill might make up for less experience, and vice-versa. *Id*.

IX. SUMMARY OF THE SCOPE AND CONTENT OF THE PRIOR ART

A. Applicant's Admitted Prior Art ("*AAPA*")

The '460 patent admits that the basic structure of a flip-chip semiconductor LED (i.e., elements 1,6[p, a, b, d and e]) was known in the art. Ex. 1001, 1:13-38 and Figs. 1 (below) and 2:

> FIG. 1 illustrates a known LED **30** of flip-chip design, where the LED **30** includes a transparent substrate **31** having a cuboidal shape (e.g., a rectangular prism), a negatively doped layer **32**, an active p-n junction layer **33**, and a positively doped layer **34**. A pair of ohmic contacts **35** and **36** are employed to forward bias LED **30** whereby light is generated and emitted from the active p-n junction layer **33** into the substrate **31**.

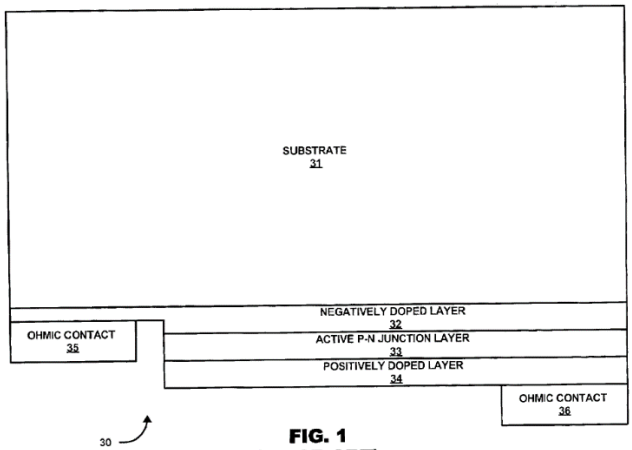


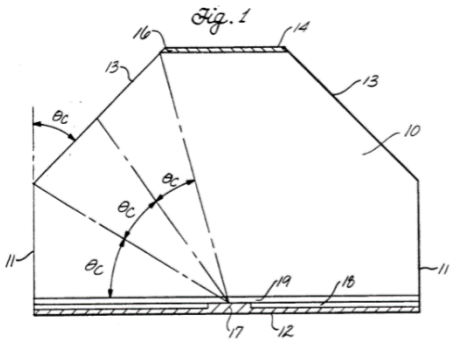
FIG. 1
(PRIOR ART)

AAPA is available as prior art in IPR proceedings. *One World Techs., Inc. v. Chamberlain Grp., Inc.*, No. IPR2017-00126, 2019 WL 1504032, at *9 (P.T.A.B. Apr. 4, 2019).

B. Haitz

U.S. Patent No. 5,087,949 to ***Haitz*** (Ex. 1008) is entitled "Light-Emitting Diode With Diagonal Faces". ***Haitz*** issued on February 11, 1992. ***Haitz*** constitutes prior art under 35 U.S.C. §102(b).

Haitz discloses a semiconductor LED where the device-environment interface is formed by a thick n-layer, ("body" 10, in FIG. 1, right). ***Haitz*** recognizes the same problem with light trapping by TIR in this layer that the '460 patent recognizes in its substrate:

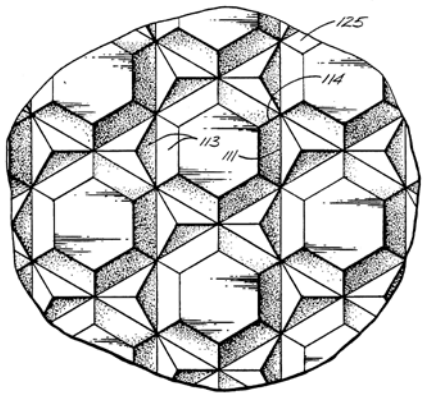


"Extracting light from an LED is not easy

because of the high index of refraction of the semiconductor material which may be in the range of from about 2.9 to 4.0…" Ex. 1008, 1:36-39. ***Haitz*** notes that, ideally, this interface would be hemispherical: "so that light from a small p-n junction in its center is normal to the surface regardless of the ray direction." *Id*., 2:37-41. Hemispheres, however, are "extremely high in price because of the complex processing required". *Id*., 2:41-43 and 49-51.

Haitz's solution is to ***approximate*** a dome or hemisphere using a truncated pyramid, which is pictured in FIGs. 1 and 3 (right). See Ex. 1008, 2:60-3:3; 5:43-64. This shape "is a better approximation of a hemisphere than the rectangular parallelopipid of a conventional LED." See *Id*., 5:43-53. ***Haitz*** notes that a truncated pyramidal shape improves extraction, even for an extended light emitting p-n junction layer. See *Id*., 4:49-62. ***Haitz*** also notes that LEDs are easily given a pyramidal top layer with a beveled dicing saw as part of the dicing process: "[f]abrication of a LED with beveled edges is a straightforward adaption of conventional manufacturing techniques for semiconductors." *Id*., 5:4-6 and see 5:14-34.

Fig. 3

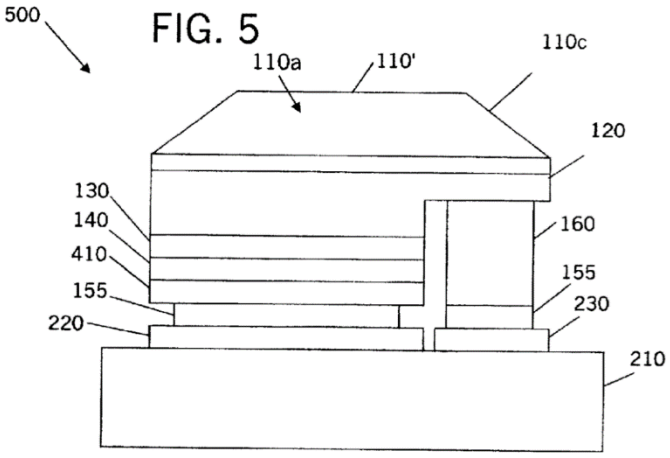


C. Slater

US Patent 6,791,119 to ***Slater*** (Ex. 1003) is entitled "Light Emitting Diodes Including Modifications for Light Extraction." ***Slater*** was filed January 25, 2002 and

claims priority to Provisional Application No. 60/307,235 (Ex 1011), filed on July 23, 2001 ("***Slater Provisional***"), which is incorporated by reference into ***Slater***. Ex. 1003, 1:8-16. The ***Slater Provisional*** supports the disclosures of ***Slater*** relied on herein. See Ex. 1011, pgs. 14:1-15:8; 16:1-17:2; 26:3- 29:5 and FIGs. 2, 5, 17A and 17B. Additionally, the ***Slater Provisional*** supports at least one issued claim of ***Slater***, for example, issued claim 18, which is supported by FIGs. 17A and 18, and the accompanying description. Accordingly, ***Slater*** constitutes prior art under 35 U.S.C. §102(e) having an effective filing date of at least July 23, 2001 and no later than January 25, 2002. See MPEP § 2136.03(III).

Slater discloses in FIG. 5 a flip-chip LED where the substrate has been given a truncated pyramidal shape, which enhances "light extraction from the LED by beveling or slanting at least some of the sidewall 110c of the substrate 110'" to reduce reflection within the substrate. *Id*., 11:52-57. ***Slater*** explicitly teaches that flip-chip structures may be used with "substrate geometries including cubic, triangular, pyramidal, truncated pyramidal and/or hemispherical with reduced area first faces." *Id*., 21:40-45.



D. Camras

US Patent 6,784,463 to ***Camras*** (Ex. 1005) is entitled “III-Phosphide and III-

Arsenide Flip Chip Light-Emitting Devices." ***Camras*** was filed March 11, 2002 and constitutes prior art under 35 U.S.C. §102(e).

Camras discloses a semiconductor, flip-chip LED. Ex. 1005, 2:52-65. In FIG. 7A, ***Camras*** shows a substrate 117 having a truncated pyramidal shape, overlying a first doped layer 114, which also has a truncated pyramidal shape. *Id*., 12:8-31.

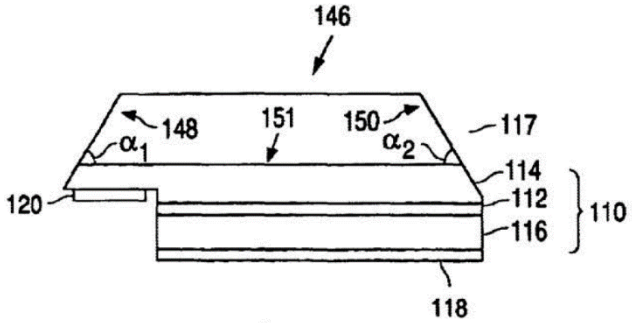


FIG. 7A

Camras recognizes that such a substrate "may approximate the shape of, for example, a dome or a hemisphere." *Id*., 12:19-22. This shape ensures that "more of the light emitted by active region 112 is incident on interfaces between the superstrate and the external environment at angles close to normal incidence than is the case for a superstrate having a cubic or rectangular prism shape…" *Id*, 12:22-27. ***Camras*** teaches that the truncated pyramidal substrate can be formed by the conventional wafer dicing process. *Id*., 12:13-15.

E. Steigerwald

US Patent 6,573,537 to ***Steigerwald*** (Ex. 1004) was filed on March 29, 2001, issued on June 3, 2002 and constitutes prior art under 35 U.S.C. §102(e). ***Steigerwald*** discloses discloses a flip-chip LED (See Ex. 1004, 3:66- 4:4, FIG. 6b (below)) having the same basic structure that has been discussed. Ex. 1004, 9:63-66.

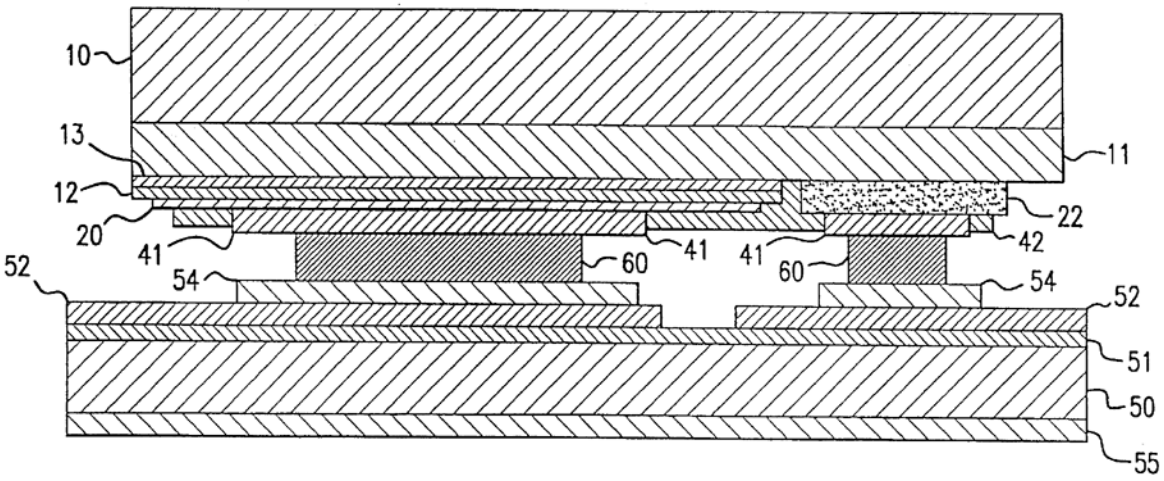


FIG.6(b)

Steigerwald analyzes the behavior of a typical device in connection with FIG. 13(c) (below), with a substrate that is index matched to its epitaxial region. See Ex. 1004, 14:1-15. In this device, "Virtually all light generated from the active region is coupled into the superstrate and has a high probability for escape through one of the five exposed superstrate surfaces." *Id*., 14:15-18. Thus, ***Steigerwald*** teaches that, even in devices with cuboidal substrates, most of the emitted light is emitted through the substrate.

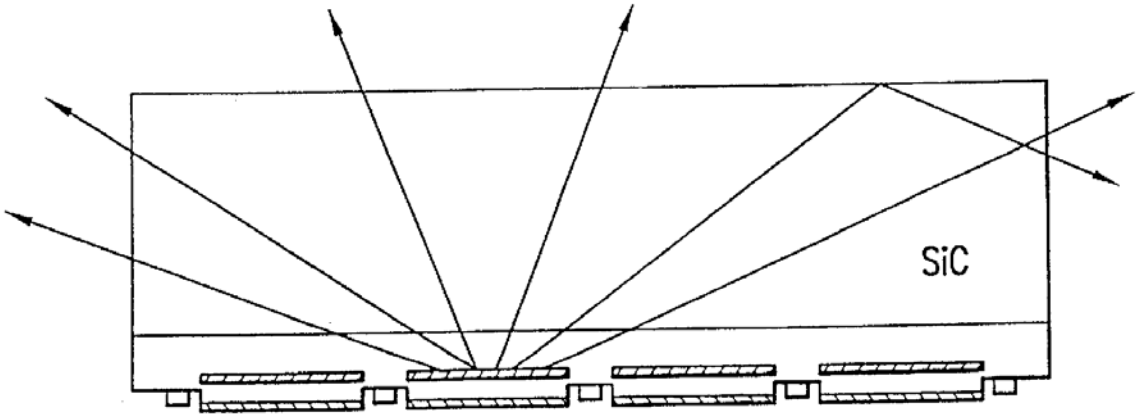


FIG. 13(c)

X. PRECISE REASONS FOR THE RELIEF REQUESTED

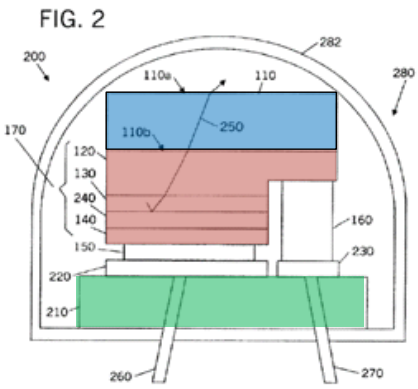
A. Ground 1: Claims 1-7 are obvious over *Slater*.

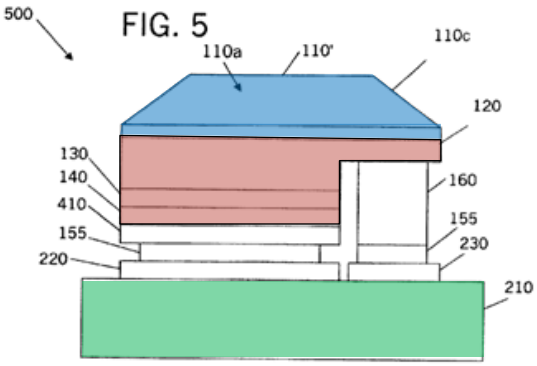
1,6[p]: ***A semiconductor light-emitting diode of flip-chip design, comprising***

Slater's FIG. 5. shows a semiconductor LED. Ex. 1003, 11:51-52: "LEDs … are illustrated in FIG. 5". The LED of FIG. 5 has layers 120, 130, 140 (red, below), described for FIG. 1[1], which : "preferably comprise gallium nitride-based semiconductor layers…" *Id*., 7:36-42. The FIG. 5 LED is a flip-chip. In reference to FIG. 2, ***Slater*** discloses a "flip-chip or upside-down packing

[1] See *Id*., 6:60-61 ("Like numbers refer to like elements throughout."); 37 C.F.R. § 1.84(p)(4).

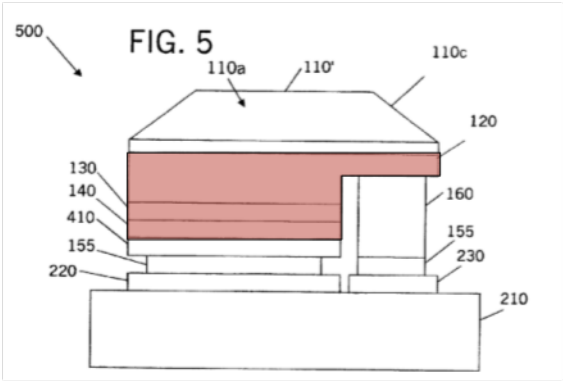
configuration [that] places the silicon carbide substrate 110 up, away from the mounting substrate 210, and places the diode region 170 down, adjacent to the mounting substrate 210." *Id*., 10:26-30; ; Ex. 1012, ¶¶78-79, 121. The FIG. 5 LED shows the same packaging configuration described as "flip-chip" with respect to FIG. 2 (below) where mounting support 210 (green) is below the diode region (120, 130 and 140) (red) and substrate 110' (blue) (*Id*, 11:55 ("substrate 110'")) is above the diode region.





1[a], {6[a]}: ***a light-emitting region including a negatively doped layer {first doped layer}, a positively doped layer {second doped layer}, and an active p-n junction layer between said negatively doped {first doped} layer and said positively doped {second doped} layer;***

FIG. 5 shows these layers 120, 130, 140 (red, below), described for FIG. 1: "[t]he diode region 170 including the n-type layer 120, the active region 130, and/or the p-type layer 140 …" *Id*., 7:36-41. Active region 130 is between n-type layer 120 and p-type layer 140. "The active region 130 may comprise a light emitting layer…" ***Id.***, 7:58-60. The n-type and p-type layers are negatively and positively doped, respectively: "Preferably, the n-type gallium nitride layer 120 comprises silicon-doped gallium nitride, while the p-type gallium nitride layer 130 comprises magnesium-doped gallium nitride." *Id*., 7:60-63. The POSA would recognize the reference to "p-type gallium nitride layer ***130***" to be an obvious drafting error[2], and would understand this reference to be "p-type gallium nitride layer ***140***", because ***Slater*** correctly describes layer 130 as the "active region" and layer 140 as the "p-type layer" throughout the remainder of the reference. See, e.g., *Id*., 7:33-41; 10:38-46; Ex. 1012 at ¶¶122-123.



Active region 130 constitutes an interface between n-layer 120 and p-layer 140, and so, is an active p-n junction layer between those two layers. Ex. 1003, 2:50-53 ("layers of p-type and n-type material [] define a p-n junction therebetween…"); Ex.

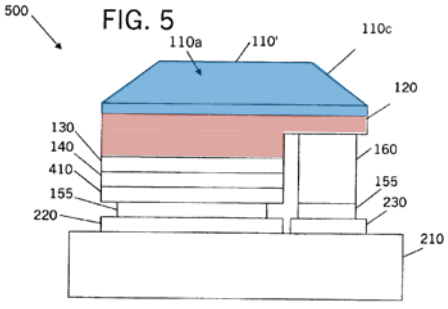
[2] See *In re Yale*, 434 F.2d 666, 668–69 (C.C.P.A. 1970) (finding that a POSA would mentally correct obvious specification errors).

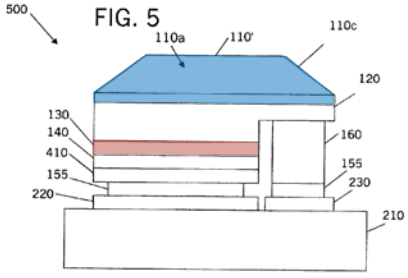
1012, ¶124.

1[b], {6[b]} : *a {first} transparent substrate overlying {adjacent} said light-light emitting region {first doped layer},*

110' of FIG. 5 is a transparent substrate. ***Slater*** discloses that the substrates of FIGs. 1-6, including 110' of FIG. 5, may be transparent silicon carbide. See Ex. 1033, 12:20-22; 7:21-31 ("silicon carbide substrate 110…that is transparent to optical radiation"); 8:13-16; 11:66-12:1 ("[t]he substrate comprises single crystal, transparent silicon carbide…"). ***Slater*** discloses that other transparent substrates, like sapphire, areusable for all embodiments. *Id*., 7:6-10 ("embodiments…may…employ[] any combination of a substrate that is non-absorbing or transparent" and index matched LED layers); 13-19 (referring to sapphire as such a substrate).

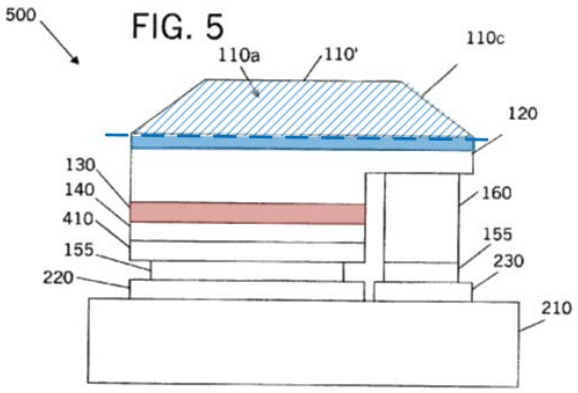
FIG. 5 shows substrate 110' (Ex. 1003, 11:55) (blue, below) overlying (i.e., on top of) light emitting region 130 (red, below right) (*Id*., 7:57-59), and adjacent to first doped layer 120 (red, below left). See *Id*., 7:60-63.





1[c], {6[c]}: ***said {first transparent} substrate having a truncated pyramidal shape so that said substrate has a cross-sectional area that decreases with distance from said junction***

Substrate 110' has a truncated pyramidal shape with a cross sectional area that decreases with distance from junction layer 130. The POSA would understand substrate 110' to be beveled around its entire perimeter because that is depicted in FIG. 5 below. Additionally, ***Slater*** describes "beveling or slanting at least some of the sidewall [singular] 110c of the substrate 110'". Ex. 1003, 11:52-55. The POSA would understand "sidewall" to refer to the entire perimeter sidewall being beveled above the dotted line at right. Ex. 1012, ¶127. The purpose of the bevel is to reduce the angle of incidence of light on sidewall 110c to reduce TIR. Ex. 1003, 11:52-58 ("Since the incident angle of light striking the beveled sidewall 110c is generally closer to the normal than it otherwise might be, less light may be reflected back onto the substrate"). In view of this teaching, the POSA would understand that sidewall 110c was beveled on all sides, so that TIR was reduced on all sides. Ex. 1012, ¶128.



At a minimum, it would have been obvious to give substrate 110' a truncated pyramidal shape. Ex. 1012, ¶¶129-136. ***Slater*** discloses truncated pyramidal substrates in connection with FIGs. 17A and 17B: "flip chip mounting…structures … may be used with other substrate geometries including cubic, triangular, pyramidal,

truncated pyramidal and/or hemispherical, with reduced area first faces". Ex. 1003, 21:41-45. ***Slater*** describes these substrate geometries as enhancements usable to modify previously described substrates, like FIG. 5's 110', to increase extraction efficiency:

> Embodiments of the invention that were described in FIGS. 1-6 above provide modifications of the silicon carbide substrate, to embody means for extracting at least some of the light …Other embodiments of the invention now will be described where various geometric modifications are made to the substrate, to provide other embodiments of means for extracting at least some of the light from the substrate, to allow increased extraction efficiency…These enhancements may be used with…substrates…as was described in connection with FIGS. 1-6, above.

See Ex. 1003, 12:20-39. ***Slater*** teaches that these substrate geometries, described in reference to FIG. 17A, are compatible with flip-chip LEDs such those of FIG 5. See *Id*., 19:33-35.

Slater motivates the enhancement. ***Slater*** teaches that "improved light extraction" can be achieved by "modifications of the…substrate…for extracting at least some of the light…" Ex. 1003, 12:19-22. One such substrate modification is the beveled sidewall 110c of FIG. 5, which enhances light extraction. *Id*., 11:52-60. Other modifications include the "pyramidal" and "truncated pyramidal" substrates as described in reference to FIGs. 17A and 17B. *Id*., 21:41-44. In view of these teachings, the POSA would have been motivated to bevel not just the portions of side wall 110c that are shown in FIG. 5, in cross section, but the entire perimeter of the substrate, resulting in a truncated pyramid, since this would reduce TIR from all

sidewall surfaces. Ex. 1012, ¶¶129-131.

The proposed modification would have been a simple substitution of a known element (a truncated pyramidal substrate) for the substrate 110' of FIG. 5 to obtain predictable result - the extraction of more light from the substrate. Ex. 1012, ¶131. Viewed another way, the proposed modification would have been simply beveling the unseen sides of sidewall 110c in the same manner as the visible sides of sidewall 110c to obtain increased light extraction. *Id*.

If the term "pyramidal" requires disclosure of the sidewall portions (if extended) converging to a common vertex[3], it would have been obvious for the POSA to modify FIG. 5 of ***Slater*** to so provide.

First, the POSA would have been motivated to bevel the entire perimeter of the device of FIG. 5 at the same angle. The POSA would have been motivated to select an angle for the beveled side wall 110' that provided increased light extraction, as ***Slater*** teaches with regard to the FIG. 5 embodiment. Ex. 1012, ¶132. It would have been obvious to use that same angle on all sides to achieve increased light extraction, around the entire perimeter of the device. Using the same angle on all sides allows the same beveling process be used on all the portions of the sidewall, thereby reducing the need for additional manufacturing steps. *Id*.

Second, the POSA would have recognized that the perimeter of the FIG. 5

[3] See Ex. 1002 at 36.

device was square, or alternatively, it would have been obvious to make it square, because ***Slater*** teaches that "LED chips generally have square perimeters for reasons of packing density within a wafer." Ex. 1003, 14:11-13; Ex. 1012, ¶133. A square substrate with four perimeter sidewall portions beveled back at the same angle would have sidewall portions that would be four truncated triangular planes, all inclined toward the center of the device, and all converging toward a common vertex. *Id*.

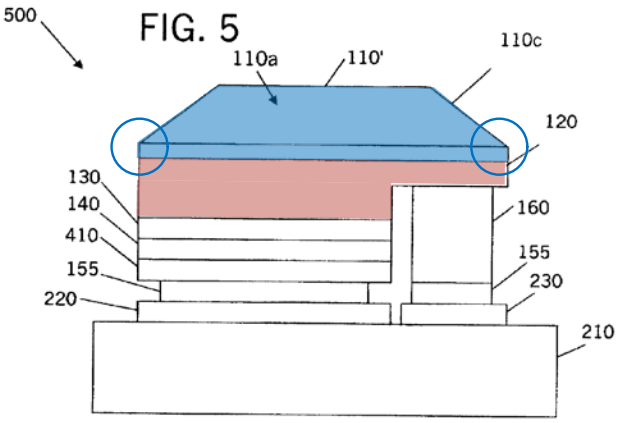
The POSA would have been further motivated to use a centered, pyramidal shape to produce an LED die with an axially symmetric light emission pattern. Ex. 1012, ¶134-136. In many applications, LEDs are packaged with rotationally symmetric primary optics, i.e., domes or hemispheres. *Id*., ¶135-136. The POSA would have understood that a substrate with an axially symmetric light emission pattern packaged with a rotationally symmetric primary optic results in an axially symmetric emission pattern from the packaged LED. *Id*. Such an axially symmetric light emission pattern would be advantageous in many applications, such as flashlights. Additionally, packaged LEDs are commonly incorporated with secondary optics in the end product. *Id*. A packaged LED with an axially symmetric emission pattern is more easily incorporated with secondary optics because the packaged LED need not be aligned in any particular rotational orientation relative to the secondary optic. *Id*. This can also enable a simpler secondary optic design. *Id*.

If the claim requires that the pyramidal shape extend all the way to first doped layer, it would have been obvious to incorporate this feature. The POSA would have

understood that increasing the beveled portion of substrate 110' would further reduce TIR, thereby increasing light extraction. Ex. 1012, ¶¶137-139.

1,6[d]: ***and wherein lateral extent of said substrate is bound by lateral extent of a doped layer nearest to the transparent substrate; and***

The lateral extent of substrate 110' is bound by, i.e., does not extend further than, the lateral extent of the n-doped layer 120, as shown below.

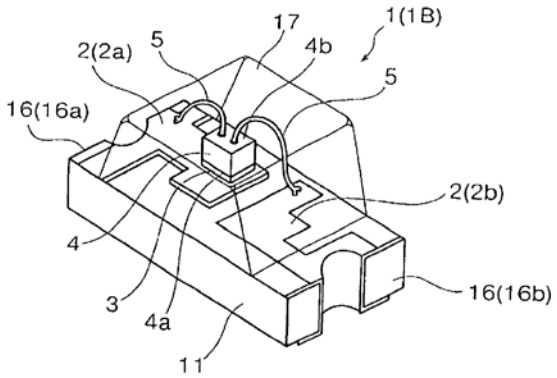


The POSA would understand FIG. 5 to show substrate 110' being bound by the lateral extent of layer 120 all around its perimeter. Ex. 1012, ¶¶140-143. The '460 patent's Applicant admitted that cross-sectional drawings like FIG. 5 provided sufficient support for the bound limitation. See Section VI, above. Accordingly, the cross-sectional drawing of ***Slater's*** FIG. 5, which shows the same sort of lateral bounding, discloses the limitation. See *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, IPR2017-01561, 2018 WL 6584977 at *12-15(P.T.A.B., Dec. 12,

2008) (comparing cross sectional drawings and stating "[w]e find that Kawai Figure 12 shows a contact hole with straight sidewalls in the same manner as Patent Owner contends the '188 patent shows contact holes with straight sidewalls.")

Additionally, ***Slater's*** devices are fabricated by the same formation-and-dice process that the '460 patent's Applicant said causes the "bound" element. As set forth above, the Applicant added the "bound" element to distinguish over ***Fujiwara,*** which disclosed a mold (right), which "completely surrounds and engulfs" the LED. Applicant stated that the "bound" substrate of the claims, by contrast, "results from the fabrication process used to deposit the substrate above the light emitting region of the diode". Ex. 1002 at 35-36. Consistent with this disclosure, the POSA would understand that the "bound" element would result from forming the epitaxial layers on the substrate at the wafer level, then dicing the substrate into die, such that the edges of both the substrate and the epitaxial layers were defined by the same perimeter cuts. Ex. 1012, ¶¶142-143.

FIG.5

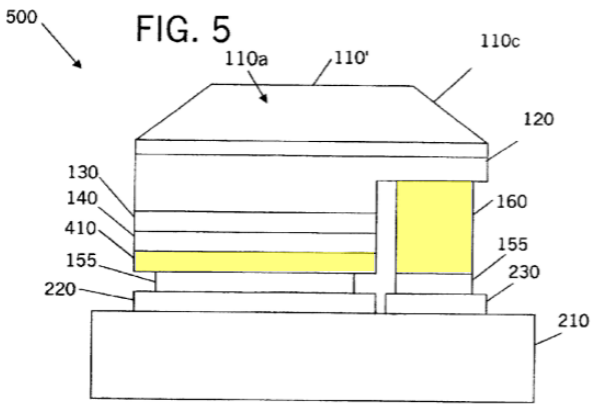


This is the same process taught by ***Slater***. ***Slater*** teaches fabricating LEDs by depositing epitaxial layers on a substrate, and then dicing the wafer. Ex. 1003, 8:58-65; 22:45-63 ("a diode region is formed on a silicon carbide substrate…dicing is performed to separate individual LED chips…"); FIG. 19. Thus, ***Slater*** teaches the

epitaxial layers covering the substrate before dicing, such that, when the chips are diced from the wafer, a single saw cut, and/or a cleavage line, defines the edges of both the substrate and the epitaxial layers, such that the substrate does not extend beyond the edges of the epitaxial layers. Ex. 1012, ¶143.

1,6[e]: ***ohmic contacts for forward biasing said junction layer so that at least most of the light is emitted from the junction layer into the surrounding environment is emitted through said substrate.***

Slater discloses a p-layer "ohmic and reflective region 410", which contains a "thin transparent ohmic contact 412" (Ex. 1003, 11:22-40), and an n-layer ohmic contact 160 (11:49; 8:3-7), both of which are depicted in FIG. 5 (yellow, right). The n- and p-layer ohmic contacts 410 and 160, respectively, are for forward biasing the junction layer 130. See, *Id*., 7:25-31 (referring to "applying a voltage across the diode region, for example, across ohmic contacts 150 and 160"); Ex. 1012, ¶144. Region 410 includes ohmic contact 412 (Ex. 1003, 11:25) and would be understood to take the place of anode ohmic contact 150 in FIG. 1. *Id*., 7:32-37; Ex. 1012, ¶144.



Slater teaches the "most" recitation under any construction.

First, if limiting, the "most" recitation only requires contacts being arranged to occlude the substrate less than other surfaces. ***Slater's*** FIG. 5 shows ohmic contact 160 and "ohmic and reflective region 410" on the bottom of the device, precisely where the

contacts are located in the '460 patent (See, e.g., FIG. 16, above), and as a result, they block light emitted downward, and do not occlude substrate 110'. Ex. 1012, ¶¶146-149. Ohmic contact 160 would be understood as opaque or reflective, and therefore occlusive. Ex. 1012, ¶147. Contact 410 includes "a reflector 414", which "preferably comprises aluminum and/or silver" and which "contacts the thin transparent ohmic contact 412 over the entire surface area of the thin transparent ohmic contact 412", and thus is also occlusive. See Ex. 1003, 11:26-39; Ex. 1012, ¶148. Thus, in FIG. 5, the bottom contacts 160 and 410 occlude the bottom of device, and there are no occlusive contacts on the substrate.

Second, ***Slater*** discloses emitting most of the light through the substrate and explains how that occurs. ***Slater*** notes that, when the substrate is index matched to the epitaxial layers "very little internal reflection may occur at a boundary between gallium nitride and silicon carbide. Consequently, it may be difficult to prevent light generated in a gallium nitride-based layer from passing into a silicon carbide substrate". See Ex. 1003, 8:66 - 9:20 and 7:4-19 ("embodiments of the invention may be employed with any combination of a substrate that is…transparent…and an index matched… epitaxial layer"). ***Slater*** teaches that, as a result of this effect, flip-chips like FIG. 5 are the most efficient architectures for light extraction: "embodiments of the present invention can encourage light generated in diode region 170 to enter the substrate 110, where it can be ***most efficiently*** extracted." See *Id.*, 10:1-14 (emphasis added); 12:3-4 ("[]External efficiency of the diode can be enhanced due to increased light extraction from the

substrate."); Ex. 1012, ¶150.

Slater also teaches the use of reflectors below the light emitting layer 130 to force light into the substrate: "In some embodiments of the invention, the diode includes a reflector that reflects light generated in the diode region back into the substrate for subsequent extraction from the device…" Ex. 1003, 12:4-13. FIG. 2 shows such a reflector, 240, below the active layer 130, reflecting initially downwardly emitted ray 250 into substrate 110 and out into the surrounding environment. Ex., 1003, 10:35-41; 10:63-11:3. Similar to FIG. 2, FIG. 5's "ohmic and reflective region" 410 has a reflector 414 (*Id*., 11:22-25), which extends across the entire downward side of active area 130, and which would reflect light back into substrate 110' and out into the surrounding environment. Ex. 1012, ¶151.

FIG. 2

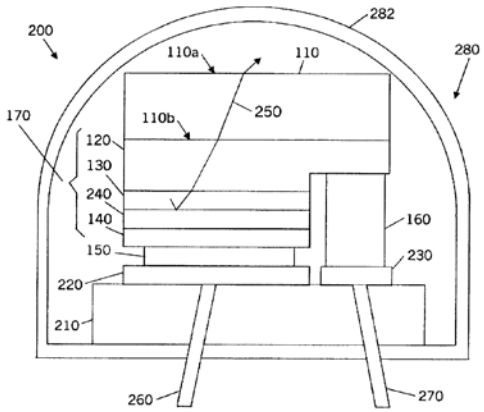
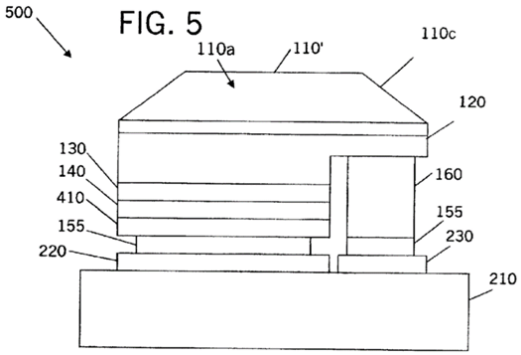


FIG. 5



Thus, ***Slater*** includes every feature for increasing light extraction through the substrate taught by the '460 patent (i.e., an index matched, pyramidal substrate and non-occluding contacts), but also additional features that the POSA would have been motivated to use to modify the LED of FIG. 5 to further ensure that most of the light is emitted through the substrate where it can be "most efficiently extracted" Ex. 1003,

10:1-14; Ex. 1012, ¶153. For these reasons, if the '460 patent teaches a configuration that supports the "at least most" recitation, then ***Slater*** at least makes obvious such a configuration.

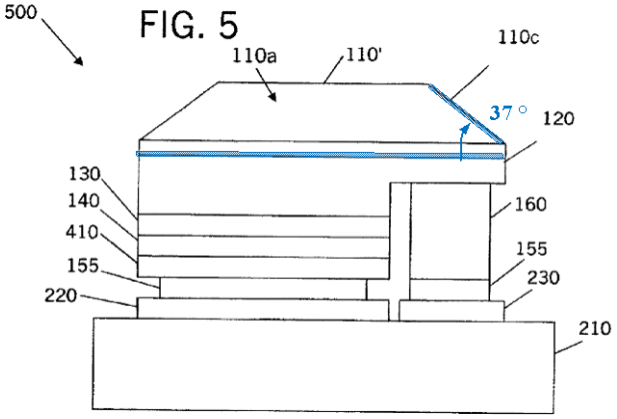
Third, even without ***Slater's*** explicit teaching that light is "most efficiently" extracted through its substrate, the "most" recitation is inherently present in ***Slater's*** FIG. 5. As explained in the Karlicek declaration (See Section IX), the diode region emits light isotropically, i.e., with equal power in all angles into a sphere. Ex. 1012, ¶¶154-155. Upwardly emitted light passes, mostly without reflection, into the substrate because its material is index matched with the epitaxial layerater. Ex. 1003, 11:64-12:18; 12:34-39; Ex. 1012, ¶155. Downwardly emitted light is reflected back up toward the diode region by ohmic and reflective region 410, where it also passes into the substrate, just like ray 250 in FIG. 2. Ex. 1003, 11:21-42; 12:4-13 and Ex. 1012, ¶155. Only a miniscule fraction of the light is emitted laterally, though the epitaxial layers, because the thickness of the substrate would be understood to be 10 to 30 times the thickness of the entire active region. See Ex. 1012, ¶156; Ex. 1003, 6:59-60 ("[i]n the drawings, the thickness of layers and regions are exaggerated for clarity."). This means that the angular subtense of the edges of the active layers is very small as compared to other surfaces of the device, and only a small of light can leak out through those edges. Ex. 1012, ¶155.

Thus, ***Slater*** 's FIG. 5 would be understood to force light into the substrate, and to minimize most other paths into the environment, necessarily resulting in most of the

light being emitted through the substrate. Ex. 1012, ¶157. Light that is in the substrate will either be emitted through one of its top or side faces, or will be reflected by TIR back down, where it will either be absorbed in the active region, or re-reflected back up by the reflective contact, with only very small fraction leaking out the epitaxial layers. *Id*. Accordingly, even the cuboidal embodiment of ***Slater's*** FIG. 2, if built to typical dimensions, would emit most its light through the substrate. *Id*. The device of FIG. 5, including a TIR reducing pyramidal substrate, results in even more light being emitted through the substrate. *Id*.

2,{7}: *The semiconductor light emitting diode of claim 1{6}, wherein said substrate [first transparent substrate] has a side surface and a bottom surface, and wherein a slope angle of said side surface relative to said bottom surface is within a range of {1}10-80 degrees.*

Slater's depicted substrate 110' has a side surface 110c, and a bottom surface (adjacent to n-layer 120) (both blue, right), with a relative slope angle of 37˚ degrees[4]. Ex. 1003, 11:51-63; Ex. 1012, ¶158.



[4] ***Slater's*** drawing, like ***Camras'*** below, would reasonably suggest a slope within the claimed range, because that is what is drawn. See *In re Asianian*, 590 F.2d 911, 914 (CCPA 1979).

Even without ***Slater's*** explicit disclosure, it would have been obvious for the POSA to try angles within the claimed ranges. ***Slater*** teaches that the sidewall should be beveled to decrease the incidence angle of light striking the sidewall. Ex. 1003, 11:52-58. The POSA would understand that for very small bevel angles (e.g., less than 10˚), the sidewall would remain substantially vertical (approximating a cuboidal substrate), and for very large angles (e.g., above 80˚), the sidewall would be essentially horizontal (also approximating a cuboidal substrate, but a very thin one). Ex. 1012, ¶159. Thus, to achieve the taught improvement, it would have been obvious for the POSA to choose among the finite range of angles near the middle of the range, which would have a reasonable probability of increasing extraction, especially in light of the 37˚ angled sidewall shown in FIG. 5 . *Id*.

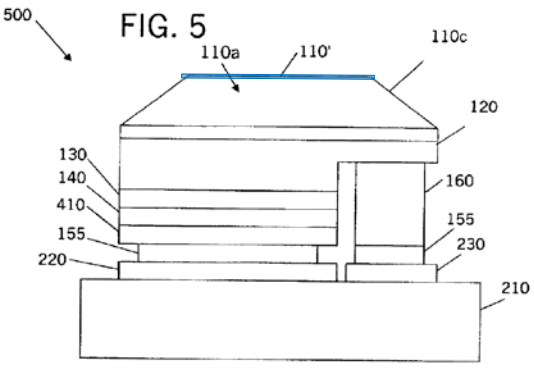
3: ***The semiconductor light emitting diode of claim 1, wherein said substrate is composed of electricity non-conductive material***.

Slater discloses sapphire substrates. Ex. 1003, 7:6-17 (identifying "sapphire (Al2O3)" as a usable substrate); 17:40-50 ("embodiments according to the present invention can be used to improve sapphire-based nitride LEDs… "); 12:35-39 ("These enhancements may be used with silicon carbide substrates, as was described in connection with FIGS. 1-6 above, but also may be used with conventional substrates comprising… sapphire."). Sapphire is non-conductive. *Id*., 17:50-53, and see Ex. 1001, 2:43-45. The POSA would have been motivated to select a sapphire substrate because at the time of the alleged invention, sapphire was a cheap and common

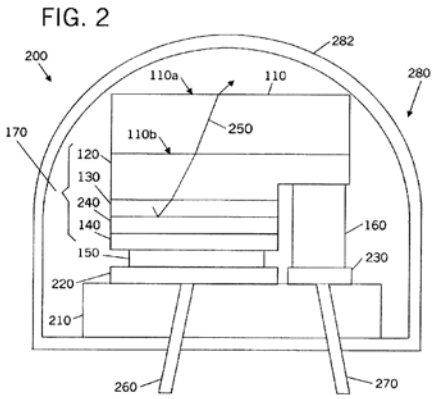
substrate used for LEDs, and was compatible with flip-chip GaN devices having contacts on the same side. Ex. 1012, ¶160-161. A device with a GaN diode and a sapphire substrate would still meet the "most" recitation. *Id*. at ¶162.

> **4:** ***The semiconductor light emitting diode of claim 1, wherein said substrate has a truncated pyramidal shape so as to define a flat top surface through which at least some of said light is emitted into said surrounding environment.***

Slater's FIG. 5 substrate 110' has a truncated pyramidal shape with a flat top surface (blue, right).

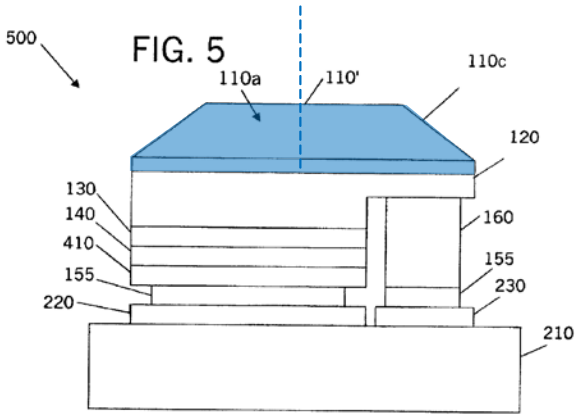


If FIG. 5 does not already disclose a truncated pyramidal substrate, it would have been obvious to modify the FIG. 5 embodiment to incorporate ***Slater's*** explicit teaching of a "truncated pyramidal" substrate usable to modify substrates like 110' to enhance light extraction. Ex. 1003, 21:41-45, 1[c], above and Ex. 1012, ¶¶164, 127-139. In the resulting device, some light would be emitted more or less vertically, and would escape the flat top surface. Ex. 1012, ¶165. ***Slater*** shows this in FIG. 2 (right), where ray 250 is escaping though a portion of a flat top surface 110a, which would be retained in the device of FIG. 5. *Id*.



5: ***The semiconductor light emitting diode of claim 4, wherein said top surface has a center coinciding with a center longitudinal axis of said substrate.***

The top surface of substrate 110' has a center that coincides with a center longitudinal axis of the substrate.



Moreover, for the reasons set forth above for element 1[c], it would have been obvious to make substrate 110' a *centered*, truncated pyramid, since the POSA would have selected a bevel angle for improved light extraction and used that angle around the perimeter of the device to simplify manufacturing, and further, in order to produce a device with an axially symmetric light emission pattern . Ex. 1012, ¶¶167, 127-139.

B. Ground 2: Claims 1-7 are obvious over *Slater* in view of *Steigerwald*.

As set forth in Ground 1, ***Slater's*** teachings, alone, render obvious claims 1-7, including the "most" recitation of elements 1, 6[e]. If ***Slater*** does not disclose this recitation, it is explicitly disclosed in ***Steigerwald***. ***Steigerwald*** demonstrates that a device according to ***Slater's*** teachings emits most of its light through the substrate and suggests further light extraction features, which would have been obvious to add to the device to achieve the "most" recitation.

Steigerwald, like ***Slater***, discloses a flip-chip LED (See Ex. 1004, 3:66- 4:4,

FIG. 6(b)) having an active region 13 between n-type layer 11 and p-type layer 12. *Id*., 9:63-66. Above the epitaxial layers is a transparent "superstrate" 10, which the POSA would understand as a substrate. *Id*., 9:66 - 10:2 ("superstrate 10 can be the growth substrate for deposition of the III-nitride layers"); Ex. 1012, ¶83. The substrate can be sapphire or silicon carbide. Ex. 1004, 10:2-4. The device includes high reflectivity p- and n- electrodes, to increase extraction:

> The device is inverted so that light may be taken out through the transparent superstrate 10 as well as the sidewalls and provides good extraction efficiency by using highly reflective, thick p- and n-electrode metallizations 20, 22. The reflectivities of the p- and n-electrodes are such that their absorption at the LED emission wavelength is less than 25% per pass, as described above.

Id., 10:13-20. The highly reflective contacts 20, 22 are ohmic. *Id*., 3:66-4:1 ("[t]he present invention is an inverted III-nitride light emitting device (LED) with highly reflective ohmic contacts.") and see 4:10-12.

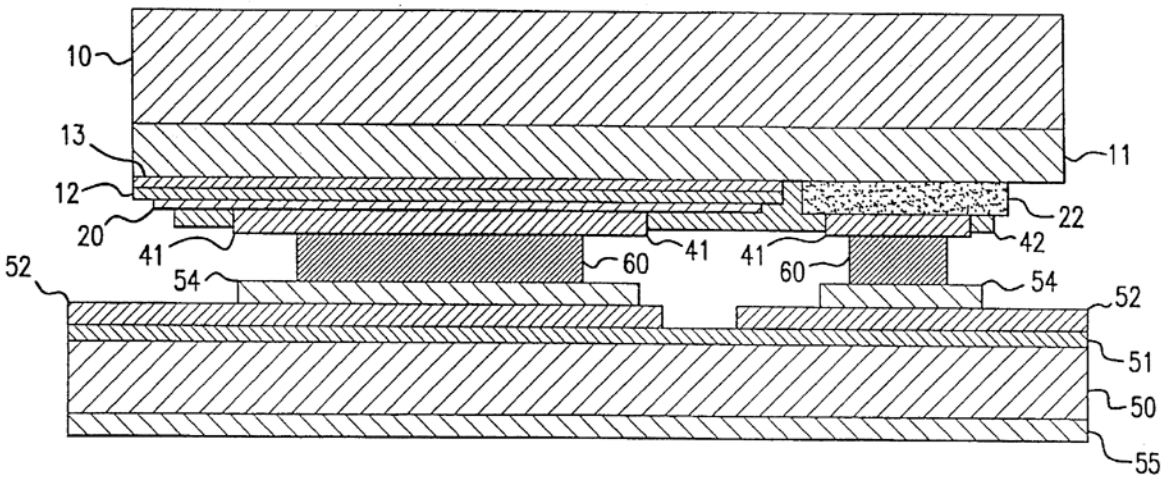


FIG.6(b)

Steigerwald notes that for an index matched substrate, as in ***Slater***, the majority emitted light will be emitted through the substrate. See Ex 1004, 14:1-20. Specifically, ***Steigerwald*** states that when an index matched substrate is used (e.g, SiC over GaN, as in FIG. 13(c), below), "there is very little probability for total internal reflection and consequently no waveguide is formed within the III-nitride layers. ***Virtually all light generated from the active region is coupled into the superstrate and has a high probability for escape through one of the five exposed superstrate surfaces.***" *Id*., 14:13-18 (emphasis added).

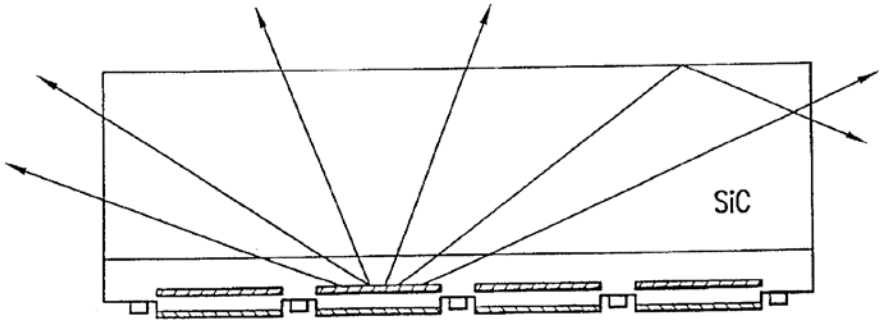


FIG.13(c)

Steigerwald would suggest to the POSA that devices like ***Slater's***, which include an indexed matched substrate and a reflective p-contact, would also result in most of the emitted light being emitted through the substrate. Ex. 1012, ¶¶168-170 and Section IX. Indeed, the POSA would recognize this, even for devices like ***Slater's*** FIG. 2, which have a cuboidal substrate like FIG. 13(c) of ***Steigerwald***, above. *Id*.. ¶170. The POSA would also recognize that by beveling the edges of ***Slater's*** substrate even more

light would be extracted through the substrate, i.e., the "high probability" referred to by ***Steigerwald***, above, would increase even further. *Id*., ¶171.

Further, if not already present, the POSA would have been motivated to incorporate ***Steigerwald's*** light extracting features, i.e., an index matched substrate, and reflective n- and p- contacts, with the combined teachings of ***Slater***, resulting in a device where most of the emitted light is emitted through the substrate. Ex. 1012, ¶172. This modification would have been motived by both ***Slater*** and ***Steigerwald's*** interest in increasing light extraction and overall efficiency. *Id*. The combination would have been a use of familiar elements (***Steigerwald's*** reflective contacts and index matching), according to known methods (e.g., placing the contacts on the bottom side of a flip-chip device), to achieve predictable results (increased light extraction). *Id*.

Additionally, ***Steigerwald*** teaches that flip-chip devices having reflective contacts will emit most of the light through the substrate, *even for non-indexed matched substrates.* See Ex. 1004, 13:45-67. In a conventional device of this sort, because of the index mismatch, "a large portion of the light generated from the active region [is] totally-internally-reflected at the sapphire/III-nitride interface…and is guided laterally along the device towards the sides of the die." *Id*., 13:49-55. ***Steigerwald*** teaches that the majority of this waveguided light is absorbed before it escapes through the sides of the epitaxial layers: "because of the many loss mechanisms present in the III-nitride epi layers and electrodes, most of the waveguided

light is lost before escaping the device." *Id*., 13:55-58. Thus, for even for an index mismatched device, where light is trapped in the epitaxial layers, but most of that is absorbed, the majority of the light escaping into the environment is still emitted through the substrate. Ex. 1012, ¶173.

Steigerwald also teaches a method to further increase extraction through a non-index matched substrate: "[l]ight extraction of the LED can be increased by providing a textured surface at one of the interfaces of the III-nitride heterostructure", which may be "random or ordered". *Id*., 13:45-47. The texturing, shown in FIG. 13(b), below, serves "to scatter light out of the III-nitride layers". See *Id*., 13:49-60.

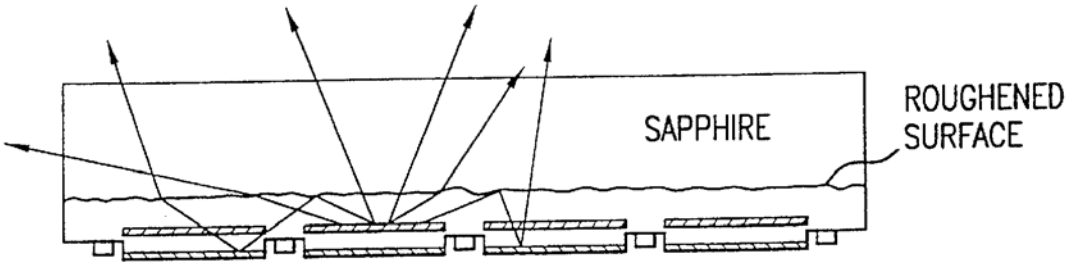


FIG.13(b)

In view of ***Steigerwald***, the POSA would understand that in devices like Slater's FIG. 5, but where the substrate was a lower index material, most of the emitted light would still be emitted through the substrate. Ex. 1012, ¶176. Additionally, the POSA would have been motivated to include ***Steigerwald's*** teaching of texturing the epi/substrate interface for lower index substrates to further extraction efficiency. *Id*. Such a combination would be motivated by both references' interest in increasing

efficiency by extracting light through the substrate, and would have been the use of familiar elements (a textured surface), according to known methods (locating the textured surface at the epi-substrate interface) to achieve predictable results (increased light extraction). *Id*.

Thus, if ***Slater*** does not disclose the "most" recitation, a POSA would have been motivated by the teachings of ***Steigerwald*** to modify ***Slater*** with the "most" recitation to increase the light extraction efficiency of FIG. 5 of ***Slater***.

C. Ground 3: Claims 1-7 are obvious over Slater in view of *Haitz* and *Steigerwald*.

If ***Slater's*** teachings do not disclose a pyramidal substrate, bound by the nearest doped layer on all sides, it would have been obvious to modify the structure of FIG. 5 of ***Slater*** to incorporate those elements from ***Haitz***. For the reasons set forth in Ground 2, ***Steigerwald*** shows how such a device meets the "most" recitation and also includes further light extraction elements that would have been obvious to add to the combination of ***Slater*** and ***Haitz.***

As set forth in Ground 1, ***Slater*** alone renders obvious all the elements of claims 1-7, particularly elements 1,6[p, a, b] and 3. ***Slater*** and ***Steigerwald*** further render obvious elements 1,6[e].

1[c], 6[c]:

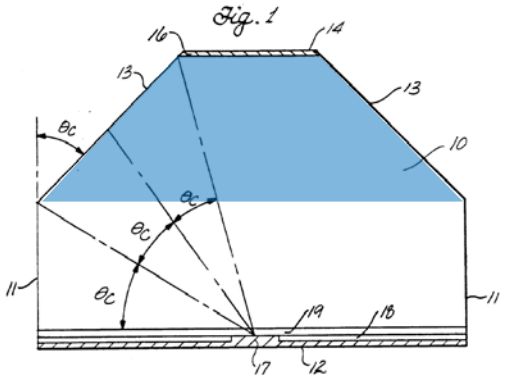
If ***Slater*** alone does not render obvious "a substrate having a pyramidal shape" with decreasing cross sectional area from the junction, it would have been obvious to

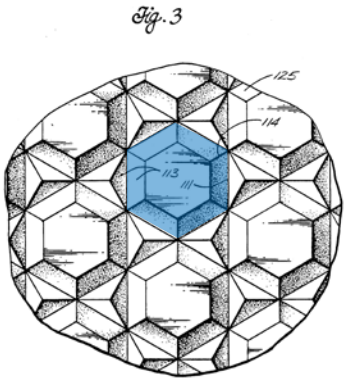
add such a substrate in view of ***Haitz.***

Haitz discloses an LED having a thick n-type "body", which is its uppermost layer, and which has a truncated pyramidal shape:

> In practice of this invention the LED has a rectangular base with four side faces 11 perpendicular to the back face 12 of the LED. In a typical embodiment the base is square. The base is surmounted by a truncated rectangular pyramid having four diagonal faces 13 and a front face 14 parallel to the back face.

Ex. 1008, 3:31-34; 2:60-67; 5:54-64 (describing pyramidal bodies having hexagonal bases). Exemplary pyramidal bodies are pictured in FIGs. 1 and 3, below.





Haitz's bodies have a centered, truncated, pyramidal shape with decreasing cross sectional area from the junction. Ex. 1012, ¶¶178-181. ***Haitz*** states that all faces 13 are sloped at the same angle. Ex. 1008, 3:65-67 ("…each diagonal face of the truncated pyramid is tilted relative to the side face of the base at an angle in the order of twice the critical angle for total internal reflection, θ_c."). The bases of ***Haitz's*** devices are regular polygons like squares or hexagons, so the bases of the angled faces have the same length. See Ex. 1008 FIG. 3, 3:34, 5:50-53; Ex. 1012, ¶181. As a result,

Haitz's faces are truncated triangles, which if extended, would terminate at a common vertex. Ex. 1012, ¶181. Furthermore, ***Haitz's*** truncated pyramidal bodies are *centered*, truncated pyramids, approximating a hemisphere or dome. *Id*., 5:50-52 ("The square LED with beveled edges hereinabove described is a better approximation of a hemisphere than the rectangular parallelopid of a conventional LED"); 5:54-59 (describing hexagonal, centered truncated pyramids as "[a] still better approximation of a hemispherical external shape"); Ex. 1012, ¶180.

It would have been obvious in view of ***Haitz*** to make ***Slater's*** substrate 110' a centered, truncated pyramid. Ex. 1012, ¶184-187. ***Slater's*** primary concern is light extraction. Ex. 1003, 5:3:34-38. ***Slater*** also recognizes that TIR within the substrate reduced efficiency and that beveling the sidewall would help. *Id*., 11:52-60. ***Haitz*** recognizes this same problem, where TIR occurs at the interface between a thick, cuboidal, doped layer and the environment:

> Extracting light from an LED is not easy because of the high index of refraction of the semiconductor material… only rays that impinge on the chip surface at an angle equal to or less than θ_c will be refracted through the surface. All rays impinging at angles greater than θ_c will experience total internal reflection.

See Ex. 1008, 1:36-50 and 2:3-10 (describing the light trapping problem in cuboidal layers). ***Haitz*** teaches that the ideal surface for light extraction is a hemisphere, but that these are difficult to fabricate:

> Taken to its ultimate or optimal configuration for light extraction, a LED would have a surface of a hemisphere so that light from a small p-n

> junction in its center is normal to the surface regardless of the ray direction. Such hemispherical LEDs have been built and are highly efficient, but extremely high in price because of the complex processing required.

Ex. 1008, 2:37-43. ***Haitz*** teaches that such shapes are easily formed during the wafer dicing process: "Fabrication of a LED with beveled edges is a straightforward adaption of conventional manufacturing techniques for semiconductors." *Id*., 5:4-5 and 5-31 (describing various techniques for producing beveled LEDs during dicing). ***Haitz*** also teaches that such a shape has good light extraction gains, even for extended light emitting regions like ***Slater's***. See *Id*., 4:49-61 (referring to a 2x efficiency gain and "good results" with a 45˚ pyramid angle when the "p-n junction extends all the way across the back face of the LED").

Thus, ***Slater*** describes one method of shaping the top layer of an LED - beveling its sidewall. ***Haitz*** teaches that a good shape for light extraction is an approximate hemisphere, which can be easily fabricated with conventional wafer dicing methods. In view of ***Haitz's*** teaching, the POSA would have been motivated to bevel ***Slater's*** substrate into a centered, truncated, pyramidal shape, because such a shape would approximate a hemisphere, which increases light extraction by reducing the amount of light subject to TIR, while being easily fabricated using conventional techniques. Ex. 1012, ¶184.

The POSA would have understood that ***Haitz's*** teachings were compatible with

and could be used to improve ***Slater***. Ex. 1012, ¶185. The thick n-layer of ***Haitz*** is equivalent to the substrate of ***Slater***. Both the thick n-layer of ***Haitz*** and the substrate of ***Slater*** (FIG. 5) are thick structures overlying the light emission region and serve as light emission surfaces. As taught in both references, TIR light trapping may occur between the light emission surface and the surrounding environment based on the index of refraction differences between the light emission surface and the surrounding environment. *Id.* ***Slater*** describes its applicability to GaP and GaAs based devices and substrates, and ***Haitz*** directly discusses those materials and others for the thick n-layer. See Ex. 1003, 7:13-19; Ex. 1008, 3:29-31. As a result, both ***Slater*** and ***Haitz*** are facing the same TIR problem caused by the same or analogous index of refraction differences between the light emission surface and the surrounding environment. Ex. 1012, ¶185. Both references address the problem by beveling the side walls of the LED chip. *Id*. A POSA would be motivated to modify ***Slater*** according to the teachings of ***Haitz*** to produce a centered, truncated, pyramidal substrate to improve light extraction using efficient and established manufacturing techniques. *Id*., ¶185-186. Also, as set forth in X.A.1[c], the resulting shape would also have the advantage of generating an axially symmetric light emission pattern, which the POSA would have found been advantageous in certain applications. *Id*., ¶187.

If the claim requires that the substrate's pyramidal shape extends all the way to the nearest doped layer, it would have obvious to add this feature. As set forth above, the POSA would recognize that this feature further reduces TIR that might occur at a

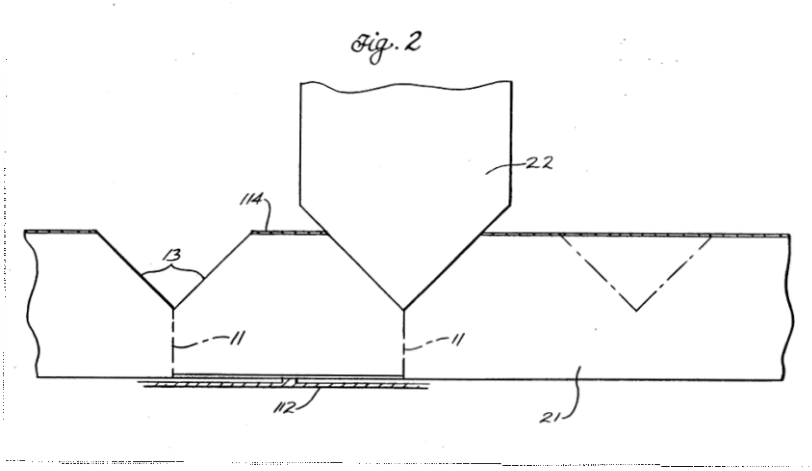
vertical sidewall surface, e.g., 11 in ***Haitz***. Ex. 1012, ¶194-197. ***Haitz*** teaches that this can be done easily and predictably simply by changing the depth of the beveled dicing saw used to bevel the top layer or by simply cutting through the device in one pass to shap and singulate the LED device.. *Id*., ¶194-195.

1,6[d]:

If ***Slater*** alone does not render obvious the lateral extent of the substrate being bound by the lateral extent of the nearest doped layer over its entire perimeter, it would have been obvious to include this element in view of ***Haitz***.

Haitz teaches that the edges of cuboidal devices are circumscribed by planar cuts that go through all the layers of the device. Ex. 1008, 1:66-2:2 (referring to "a scribe and break technique… where the side faces are smooth crystallographic planes intersecting the front and back surfaces"). ***Haitz*** teaches that the same is true for its pyramidal devices, which can be fabricated using a "V-shaped" dicing saw to form angled faces 13 in LEDs on a wafer by "sawing arrays of parallel V-shaped grooves in orthogonal directions". Ex. 1008, 5:14-23, and FIG. 2 (below). This process defines the pyramidal shape around the entire perimeter of ***Haitz's*** square "body". *Id*., 3:34-37; Ex. 1012, ¶¶190-191 and Section X. After this is done, "the individual LEDs may be separated from each other by cleaving from the bottom of the groove, or a second pass may be made with a conventional dicing saw aligned with the bottom of the groove". Ex. 1003, *5:*23-27. The result of either of these processes is a vertical cut from the base of the pyramidal portion of ***Haitz's*** body down through the epitaxial layers (shown

as edge 11, in FIG. 2, below), on all four sides. Ex. 1012, ¶¶190-191. ***Haitz*** also teaches that the beveled dicing saw can be used to shape and signulate the LED chip in one pass. Ex. 1008, 5:28-34; Ex. 1012, ¶¶190, 195. These techniques cause the lateral extent of body 10 to be bound by the lateral extent of the epitaxial region on all sides. Ex. 1012, ¶191.



The POSA would have been motivated to use this process to form pyramidal substrates in the devices of ***Slater***, since the process ***Haitz*** describes could efficiently bevel the substrate of FIG. 5 of ***Slater*** as part of the dicing process, thereby reducing process steps and, as ***Haitz*** teaches, could be achieved with a "straightforward adaptation of conventional manufacturing techniques." Ex. 1008, 5:4-6; Ex. 1012, ¶192. The POSA would understand that this process could be easily applied to ***Slater*** with predictable results, since ***Slater*** already discloses the use of a dicing saw to generate similar shapes. See Ex. 1005, 12:66-13:10; Ex. 1012, ¶193.

2 and 7:

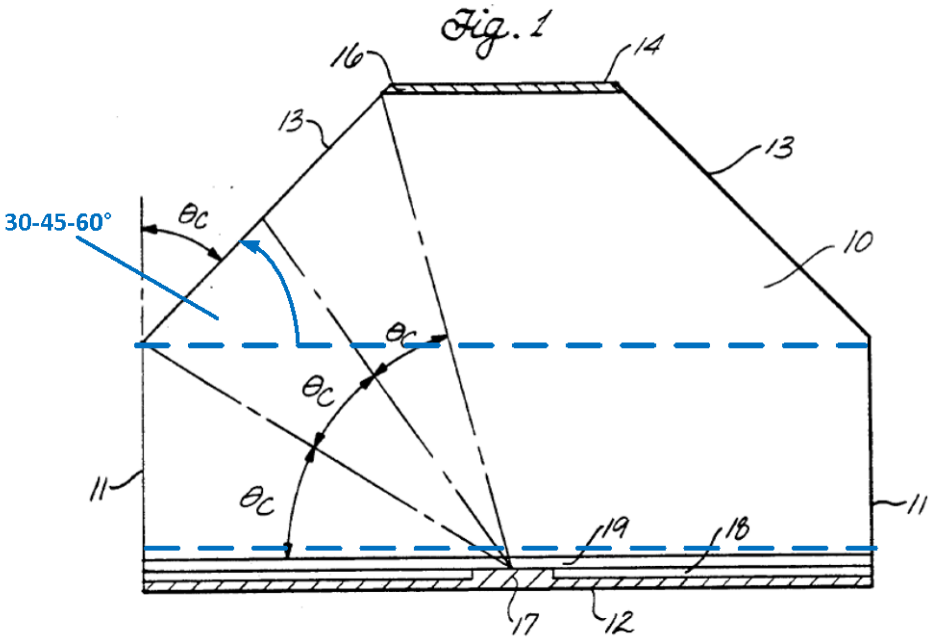
If ***Slater*** alone does not render obvious the claimed angular ranges, they are

rendered obvious by ***Haitz***.

Haitz teaches that its truncated pyramidal body has angular faces inclined at 90-θ_c with respect to its bottom surface, as shown in marked up FIG. 1 below. ***Haitz*** also states,

> Thus, in an exemplary embodiment …the diagonal faces extend at an angle of 45° relative to the side faces. Tests of light-emitting diodes with diagonal faces in the range of from 30° to 60° from the side faces show improvements in light extraction efficiency of from one and one-half to two times the light output of a conventional LED of similar dimensions without the diagonal faces.

Ex. 1008, 4:62 - 5:3. Thus, ***Haitz*** teaches that its side surfaces may have a slope angle of between 30° to 60° with respect to the horizontal, as marked below. Ex. 1012, ¶199-200. The POSA would be motivated to select a slope angle within this range for FIG. 5 of ***Slater*** based on ***Haitz's*** teaching that this angle results in improvements in extraction efficiency relative to conventional cuboidal LEDs, even for extended sources. Ex. 1008, 4:53-61 (describing 30° to 60° as "appropriate" with "good results" at 45°); 4:66-5:3; Ex. 1012, ¶¶199-201. A POSA would be motivated to look to ***Haitz*** for selecting the bevel angle for the substrate 110' of ***Haitz*** because ***Slater*** and ***Haitz*** disclose light extraction from LEDs of the same materials, among others as discussed above. Ex. 1012, ¶201.



4 and 5:

If ***Slater*** does not render obvious a centered, truncated pyramidal substrate with a flat top surface, the POSA would have been motivated to incorporate this teaching from ***Haitz***, because, as set forth in X.C.1[c], above, this shape approximates a hemisphere and is efficiently fabricated. Ex. 1012, ¶¶202, 205. Additionally, as discussed in X.A.1[c], the POSA would have been motivated to use a centered, truncated pyramidal substrate to increase light extraction without the need for additional manufacturing steps and further to generate an axially symmetrical light emission pattern. *Id*.

As ***Slater's*** FIG. 2 shows, in the resulting device of the modified FIG. 5, light emitted vertically would escape the flat, top surface. Ex. 1012, ¶203-204. The POSA would omit ***Haitz's*** top side contact 14 from the combination, because it would block

light from being emitted from the substrate, which runs counter to ***Slater's*** interest in increasing extraction. *Id*., ¶203. It would also serve no function in ***Slater's*** design, where the electrical contacts are on the bottom of the device. *Id*.

D. Ground 4: Claims 1-8 are obvious over *AAPA* in view of *Camras*

In describing "Related Art" (Ex. 1001, 1:13-41, FIGs. 1 and 2), the '460 patent admits that almost every feature of the claimed LED was known in the prior art. Specifically, the ***AAPA*** admits that the following elements, pictured in FIG. 1, below, were known:

- A semiconductor LED of flip-chip design (**1[p], 6[p], 8[p]**): "An LED is a semiconductor chip or die that emits light when a forward current flows through the LED. FIG. 1 illustrates a known LED **30** of flip-chip design…" Ex. 1001, 1:13-15, FIG. 1.

- A light emitting region with n, p, and a junction layer in between (**1[a], 6[a], 8[a]**): "a negatively doped layer 32, an active p-n junction layer 33, and a positively doped layer 33…whereby light is generated and emitted from the active p-n junction layer…" *Id*., 1:17-22.

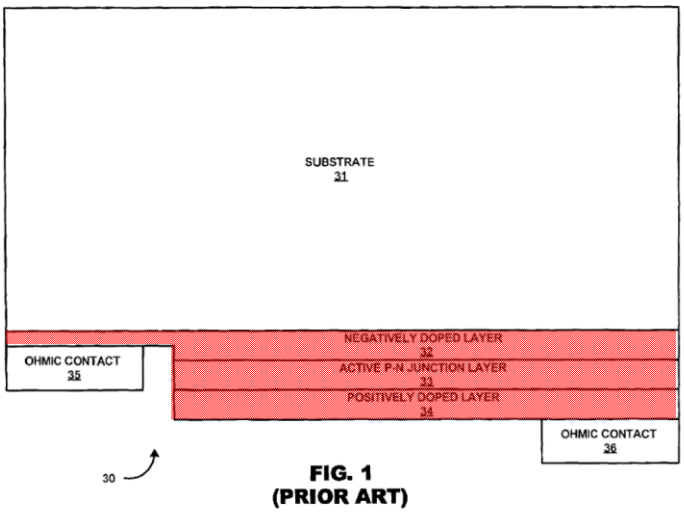


FIG. 1
(PRIOR ART)

- A transparent substrate over and adjacent the LED layers (**1[b], 6[b], 8[b]**): "LED **30** includes a transparent substrate **31**". *Id.*, 1:16.

- The lateral extent of the substrate being bound by the lateral extent of the LED layers (**1[d], 6[d], 8[d]**): FIG. 1.

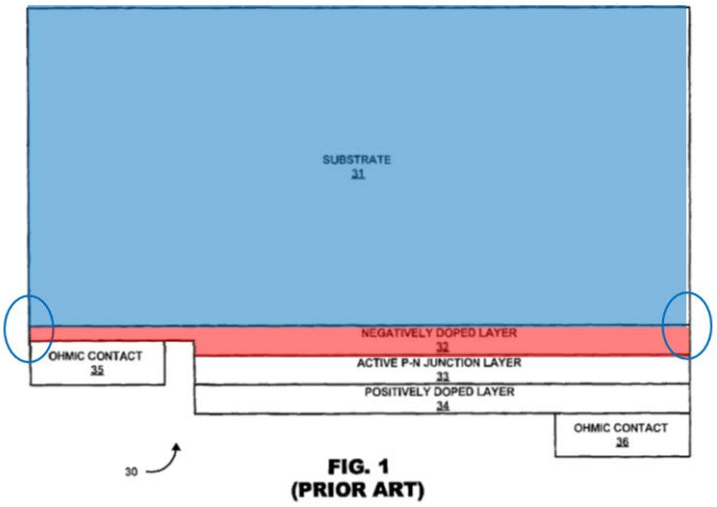


FIG. 1
(PRIOR ART)

- Ohmic contacts for forward biasing the junction layer, and placed to not obscure the substrate. (**1[e], 6[e], 8[e]**): "ohmic contacts 35 and 36 are employed to forward bias LED 30". *Id.*, 1:19-21.

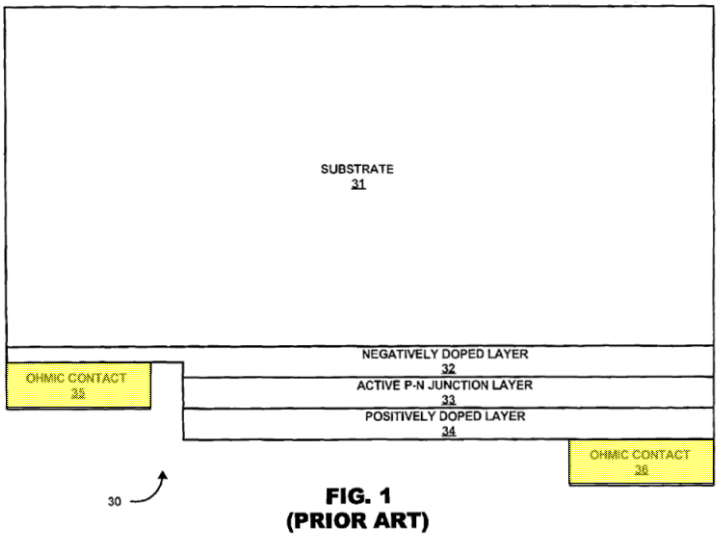


FIG. 1
(PRIOR ART)

The only claim elements *not* admitted to be prior art in the '460 patent are the elements relating to the pyramidal substrate (E.g., 1[c], and the dependent claims), but ***Camras*** teaches these, and it would have been obvious to modify the cuboidal ***AAPA*** substrate according to ***Camras'*** teachings to increase light extraction.

1[c], 6[c], 8[c]:

Camras, like the ***AAPA***, discloses a flip-chip, semiconductor LED having the typical diode structure and a transparent substrate. See Ex. 1005, 2:52-53; 63-65; 4:13-54. In connection with FIG. 7A, ***Camras*** discloses a substrate having a centered, truncated pyramidal shape, with a cross-sectional area that decreases with distance from the nearest doped layer 114, chosen to approximate a dome or hemisphere:

> In the embodiment illustrated in Fig. 7A, for example, light-emitting device 146 includes superstrate 117 having surfaces 148 and 150 which form acute angles… with a top surface 151 of stack 110.…The shapes of the superstrates in light-emitting devices 146 and 152 may approximate the shape of, for example, a dome or a hemisphere.

Ex. 1005, 12:10-13; 12:19-22. While ***Camras*** calls substrate 117 a "superstrate", the POSA would understand it as a substrate because the diode stack 110 may be grown on it. Ex. 1012, ¶¶71, 211-212; Ex. 1005:11:41-43 ("In another method of fabricating light-emitting devices such as those disclosed above, stack 110 is grown on superstrate 117 rather than on host substrate 140.") Because substrate 117 is chosen to approximate a dome, the POSA would understand that its angled surfaces are formed on all sides, and the angles of the sidewalls would be equal, and inclined toward a central point, (as

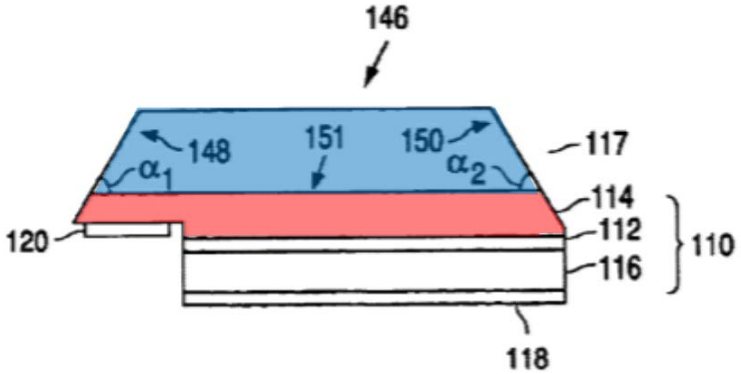


FIG. 7A

pictured in annotated FIG. 7A, right), since this configuration would approximate a dome or hemisphere. Ex. 1012, ¶212-215. As seen, the cross sectional area of substrate 117 decreases with distance from nearest doped layer 114.

The POSA would also understand substrate 117 to have a square base, or at least for this feature to be obvious, because the POSA would understand that the FIG. 7A device is essentially ***Camras'*** square FIG. 2 device but with a beveled, instead of a cuboidal, substrate. See Figures, below; Ex. 1012, ¶¶214, 75. The two devices have very similar cross sections, and ***Camras*** describes the FIG. 7A device immediately after discussing the light trapping disadvantage of the FIG. 2 device. *Id*., Ex. 1005, 11:66-12:31. Additionally, a square device with a square substrate would be consistent with ***Camras'*** teaching that the substrate 117 is intended to approximate a dome or hemisphere. Ex. 1012, ¶214.

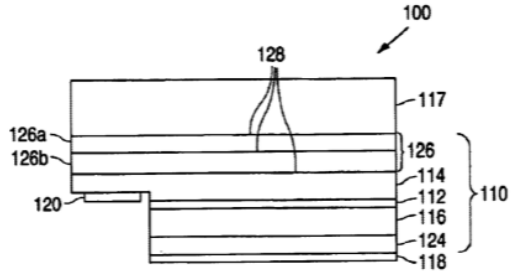


FIG. 2A

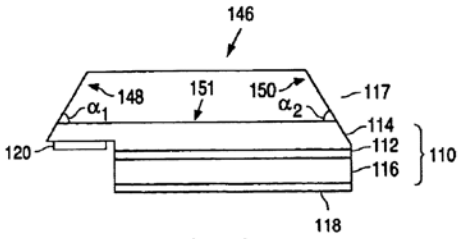


FIG. 7A

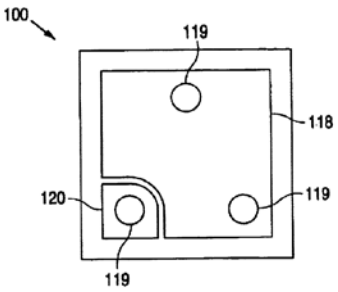


FIG. 2B

Because substrate 117 has equal angled facets arranged around a square perimeter that are inclined inward, those facets are truncated triangles which, if extended, would converge to a common vertex. Ex. 1012, ¶215.

It would have been obvious to replace the cuboidal substrate 31 of the ***AAPA*** with ***Camras'*** centered, truncated, pyramidal substrate 117, in order to improve light extraction. Ex. 1012, ¶¶216-219. ***Camras*** recognizes that light may be trapped by TIR in cuboidal substrates. Referring to FIG. 2A (above), ***Camras*** states, "some of the light emitted by active region 112 may be trapped in light-emitting device 100 by total internal reflection at interfaces between, for example, superstrate 117 and air…" Ex. 1005, 12:1-5. Thus, the POSA would have understood that the cuboidal substrate 31 of the ***AAPA***, like FIG. 2 of ***Camras***, was ready for improvement. ***Camras*** states that its dome-like substrate improves extraction over cuboidal substrates:

> Hence, in these embodiments more of the light emitted by active region **112** is incident on interfaces between the superstrate and the external environment at angles close to normal incidence than is the case for a superstrate having a cubic or rectangular prism shape as in FIG. **1**. Consequently, light may be extracted more efficiently from light-emitting devices **146** and **152** than from light-emitting device **100** since the fraction of emitted light trapped in devices **146** and **152** by total internal reflection may be reduced compared to that for device **100**.

Ex. 1005, 12:22-31 and 12:8-10. Thus, replacement of the ***AAPA's*** cuboidal substrate with ***Camras'*** truncated pyramidal substrate would have been the application of a known modification (beveling the substrate), to a known device (the cuboidal substrate of the ***AAPA***), which was ready for improvement, to yield predictable results (decreased light trapping). Ex. 1012, ¶218.

Moreover, the POSA would have been motivated to keep ***Camras'*** centered, truncated pyramid in the combination. ***Camras*** teaches that the substrate's bevel angles can be varied to optimize extraction efficiency. Ex. 1005, 12:51-56. The POSA would have been motivated to choose one optimal angle to use around the entire perimeter, in order to optimize overall efficiency without the need for additional manufacturing steps. Ex. 1012, ¶219. Additionally, for the reasons discussed above, a centered, truncated pyramid would advantageously create an axial symmetric emission pattern, which would compatible with rotationally symmetric optics like domes or hemispheres. *Id*., ¶220.

If the claim element requires the substrate's pyramidal shape to extend to the nearest doped layer, ***Camras*** discloses this element, and it would have been obvious to include in the combination to reduce TIR light trapping. Ex. 1012, ¶221.

1[d], 6[d], 8[d]:

If the ***AAPA*** does not disclose the "bound" element, ***Camras*** does, and it would have been obvious to combine ***Camras'*** teaching with the ***AAPA*** to gain manufacturing

efficiency advantages taught by ***Camras***.

FIG. 7A of ***Camras*** shows substrate 117 being bound by the lateral extent of nearest doped layer, or first doped layer, 114, marked below.

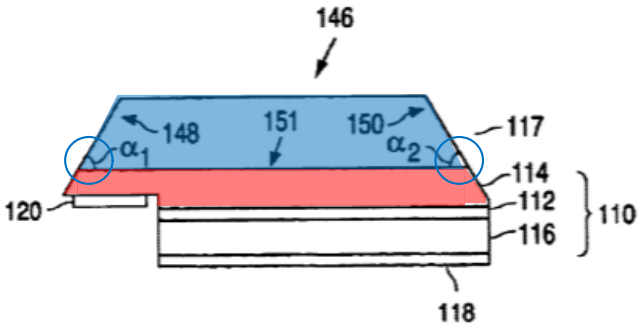


FIG. 7A

As set forth above, the only support for the bound limitation in the '460 patent is in cross-sectional Figures. Thus, ***Camras's*** cross-section (and indeed, the cross-section of FIG. 1 of the ***AAPA***) provides the same extent of disclosure for the "bound" element that the '460 patent provides, and therefore, discloses the element.

Moreover, teachings from ***Camras*** motivate including the bound element in the combination. ***Camras*** states that the angled surfaces of the FIG. 7A embodiment "may be formed, for example, by dicing a wafer into separate devices with a beveled or angled saw blade." Ex. 1005, 12:13-15. The POSA would have been motivated to adopt this method of shaping the substrate during the dicing process, because it would have been an efficient method by which to shape the substrate while signulating the wafer, thereby reducing process steps. Ex. 1012, ¶¶225-227. This process would result in the substrate being bound by nearest doped layer 114, around its perimeter, because,

during the dicing process described above, the same angled blade that formed angled surfaces 148, 150 at the perimeter of substrate 117 would also form individual LED devices by either sawing and cleaving or sawing through the active layer stack 110. Ex. 1012, ¶227. Applicant relied on this observation during prosecution to distinguish ***Fujiwara's*** mold, which "completely surrounds and engulfs" the LED (because it is added after dicing) from the "bound" substrate of the claims, which "results from the fabrication process used to deposit the substrate above the light emitting region of the diode". Ex. 1002 at 35-36; Ex. 1012, ¶225.

1[e], 6[e], 8[e]:

The combination of ***AAPA***'s ohmic contacts and ***Camras'*** pyramidal substrate discloses or makes obvious the "most" recitation .

First, if limiting, as discussed above, the "most' recitation only requires locating contacts so that less of the substrate is occluded than any other surface. The ***AAPA*** places contacts 35, 36 on the bottom of the device, just as the contacts are placed in the purportedly inventive embodiments of the '460 patent. Ex. 1001, FIG. 1. Indeed, ***Camras***, unlike the '460 patent, explicitly teaches that such contact placement forces most of the emitted light into the substrate where it can be extracted:

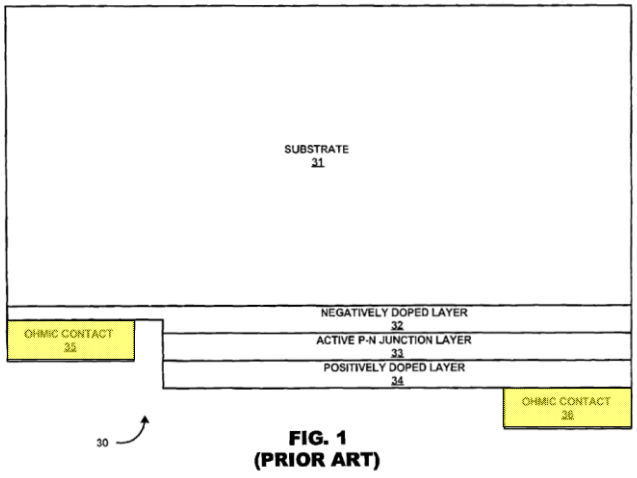


FIG. 1
(PRIOR ART)

> Since contacts **118** and **120** (FIGS. 2A-2B, **3**A-**3**C) are both disposed on the bottom of stack **110**, in embodiments in which contacts **118** and **120** are opaque (e.g., reflective), ***a larger fraction of light emitted by active region 112 exits the stack through its top side into superstrate 117 than through its bottom side.***

Ex. 1005, 9:25-30 (emphasis added); 9:66 - 10:3 (stating that bottom side contacts "do not block light emitted by active region 112 from exiting device 100 through superstrate 117***")***. The POSA would understand these teachings to apply to the FIG. 7A's bottom side contacts. Ex. 1012, ¶¶229-230.

Second, ***Camras*** teaches other features, not present in the '460 patent, that enhance light extraction through the substrate. ***Camras*** discloses *reflective* bottom side contacts, which reflect downwardly emitted light back into the substrate for extraction: "In some embodiments, contact **118** is highly reflective to light emitted by active region **112** and consequently reflects such light incident on it from active region **112** back toward substantially transparent superstrate **117**." *Id*., 6:35-38. Additionally, ***Camras*** teaches *ohmic* contacts, which the POSA would be motivated to use for the ohmic contacts of the ***AAPA***. Ex. 1005, 6: 38-48 (incorporating by reference EX 1006, 3:54-4:45; Ex. 1012, ¶231. Also, ***Camras*** teaches a reflective layer 124 (pictured with FIG. 2A), arranged "between active region 112 and contact 118 to reflect a portion of light emitted by active region 112 toward substantially transparent superstrate 117." See, Ex. 1005, 8-24.

Camras also teaches an index matched substrate to suppress TIR at the epitaxial-substrate boundary. Ex. 1005, 5:47-59 ("Forming superstrate 117 from a high

refractive index material to more closely match the index of stack 110 typically increases the efficiency with which light emitted by active region 112 is coupled from stack 110 into superstrate 117.").

Additionally, ***Camras*** teaches that the substrate's surfaces may be textured to facilitate extraction: "light extraction efficiency of the light-emitting device is improved by the inclusion of one or more interfaces that are roughened or textured to scatter light out of the device." Ex. 1005, 13:1-10.

The POSA would have been motivated to incorporate some or all of the light extracting features of ***Camras*** discussed above in order to further ***Camras'*** goal of achieving "light-emitting devices with improved light extraction and brightness". Ex. 1005, 4:11-12; Ex. 1012, ¶¶231-234. Such a device would have every light extraction feature taught in the '460 patent, and more, so that most of the light is emitted through the substrate. Ex. 1012, ¶235. As ***Camras*** demonstrates, the use of such elements was well within the skill of the POSA, and they could be easily and predictably applied to improve the ***AAPA*** device in the same manner in which they are used in ***Camras***. Ex. 1012, ¶234.

Third, the recitation is inherently present in the ***AAPA*** supplemented with ***Camras'*** teaching of reflectors on the bottom of the device and an indexed matched substrate. As is discussed in X.A.1[e], index matching the epitaxial layers to the substrate while placing reflectors below the diode region, prevents much light from exiting the device anywhere other than through the substrate. Ex. 1012, ¶¶236-237.

The POSA would recognize that in both ***Camras*** and the ***AAPA***, the substrate would be 10 to 30 times the thickness of the entire active region, and so only a tiny fraction of light would escape out the edge of the active region Ex. 1012, ¶¶236-237; Ex. 1005, 4:5 ("dimensions in the figures are not necessarily to scale."). Thus, in the proposed combination, light is forced into the substrate, and other paths into the environment are minimized, which necessarily results in most of the emitted light being emitted through the substrate. Ex. 1012, ¶¶236-237. This is true, even for cuboidal devices like ***Camras'*** FIG. 2A. *Id*., ¶237. The device of the combination, including a pyramidal substrate, would result in even more light emitted through the substrate. *Id*.

8[f]: ***and wherein an upper portion of said first doped layer has a pyramidal shape.***

Camras discloses an upper portion of first doped layer, 114 (Ex. 1005, 4:29-32), which has a pyramidal shape. The POSA would understand that layer 114 would be beveled, as shown, by the same perimeter saw cuts that shaped substrate 117 into a pyramidal shape during the dicing process. Ex. 1012, ¶238.

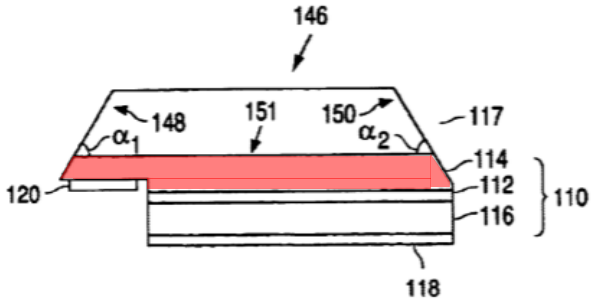


FIG. 7A

The POSA would have been motivated to include the pyramidal upper layer in

the combination to increase the amount of light extracted from the layer by reducing total internal reflection at its edges. Ex. 1012, ¶239. Additionally, the POSA would recognize that the first doped layer could efficiently be given a pyramidal shape by the same perimeter sawing process used to form ***Camras'*** substrate 117 into a pyramidal shape, simply by adjusting the depth of the saw cut, singlulating the LED chip with the angled saw in one pass. *Id.*, ¶238.

2 and 7:

As shown in FIG. 7A, substrate 117 has a bottom surface 151 (blue), which makes an angle with side surfaces 148, 150 of 60˚ degrees. Ex. 1012, ¶240. Moreover, ***Camras*** states that the bevel angle may vary to optimize light extraction efficiency. Ex. 1005, 12:51-56 ("The extraction efficiency of the light-emitting devices shown in FIGS. 7A-7D may be optimized, for example, by varying the thickness of superstrate **117** and by varying the bevel angles (e.g., α_1, α_2, β_1, β_2, γ_1, and γ_2) of the surfaces of superstrate **117…**"). For the reasons discussed above in X.A.2, it would have been obvious to try angles falling within the range of 10˚ to 80˚ to appreciably reduce the angle of incidence of light striking surfaces 148 and 150. Ex. 1012, ¶241.

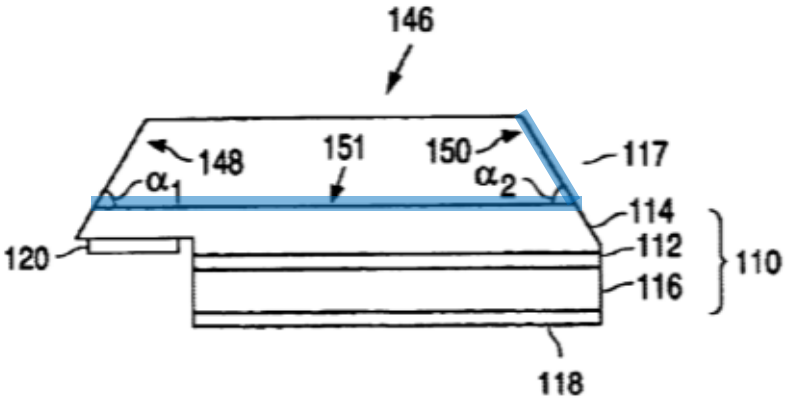


FIG. 7A

3:

The AAPA suggests that its substrate 31 can be non-conductive because of its contact placement. Ex. 1012, ¶242.

Moreover, in describing the flip-chip embodiment of FIG 2, ***Camras*** provides "[S]ubstrate 117 has no electrical function…. [S]uperstrate 117 may be formed from a substantially non-conducting or highly resistive material." Ex. 1005, 4:55-61, and 30-32. This teaching applies to FIG. 7A, which is also a flip-chip configuration, and the POSA would understand that FIG. 7A's substrate 117 has no electrode, need not carry current, and may therefore be non-conductive. Ex. 1012, ¶242.

Camras also discloses that its substrate may be non-conductive sapphire. Ex. 1005, 5:9-10. The POSA, at the time of the filing date of the '460 patent, would have been motivated to select sapphire in cases where cost was a concern because it was cheap and the most common substrate for GaN devices. Ex. 1012, ¶243.

4:

Camras's FIG. 7A substrate 117is a truncated, pyramidal shape. See X.D.1[c], above. ***Camras'*** substrate has a flat top surface (blue, below), through which at least some light would be emitted in the combination, since the light emitting layer 33 of the ***AAPA***, would emit at least some light vertically. Ex. 1012, ¶244.

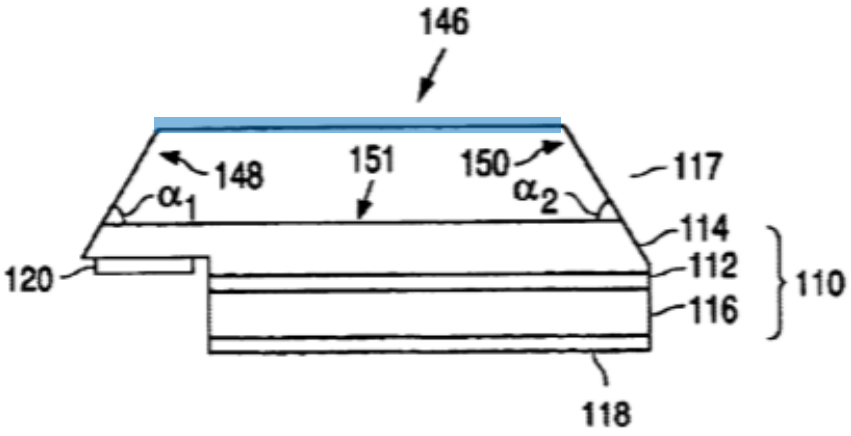


FIG. 7A

AAPA FIG. 2 (below) shows an example of such vertically emitted light, which is transmitted through a central portion of a flat top surface. This portion of substrate 31 would remain flat in the combination, since keeping a flat central portion of the top surface helps to approximate a hemisphere, which is ***Camras'*** intent. Ex. 1012, ¶245.

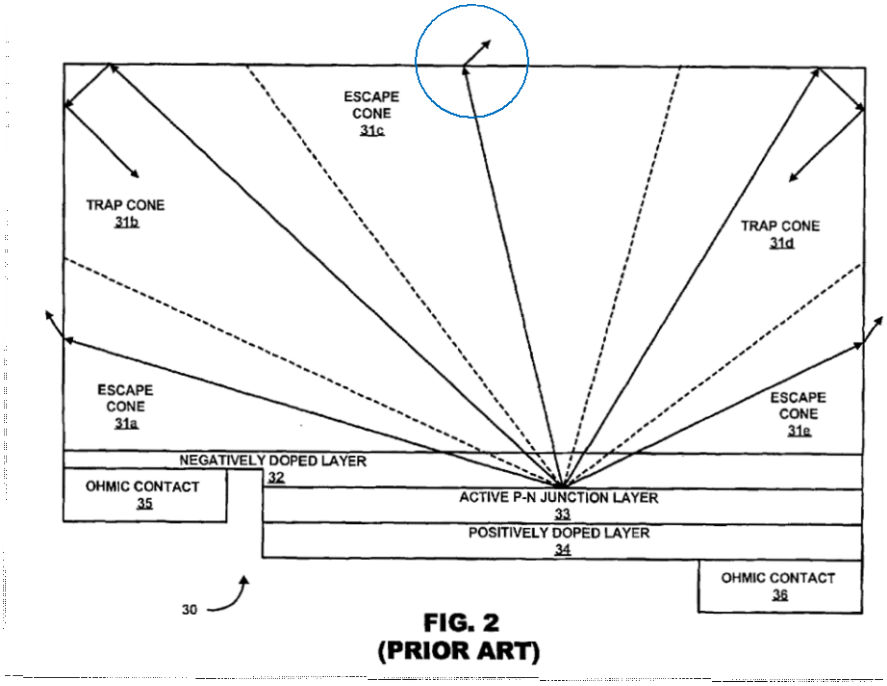


FIG. 2
(PRIOR ART)

5:

Camras' substrate 117 has a top surface 146 that has a center coinciding with a longitudinal axis of the substrate, as shown. It would have been obvious to retain the centered top surface in the combination since ***Camras*** teaches that a substrate approximating a dome or hemisphere is advantageous, and such a shape would have a centered, flat top surface. See Ex. 1005, 12:19-27; Ex. 1012, ¶246 . Additionally, this feature results from selecting the same bevel angle around the perimeter of the device, which the POSA would do to increase light extraction while reducing the need for additional manufacturing steps. See Ex. 1005, 12:18-19; Ex. 1012,¶246. Also, a centered, truncated pyramidal substrate would generate a symmetrical light emission pattern, which the POSA would recognize as advantageous, *Id*. at ¶246.

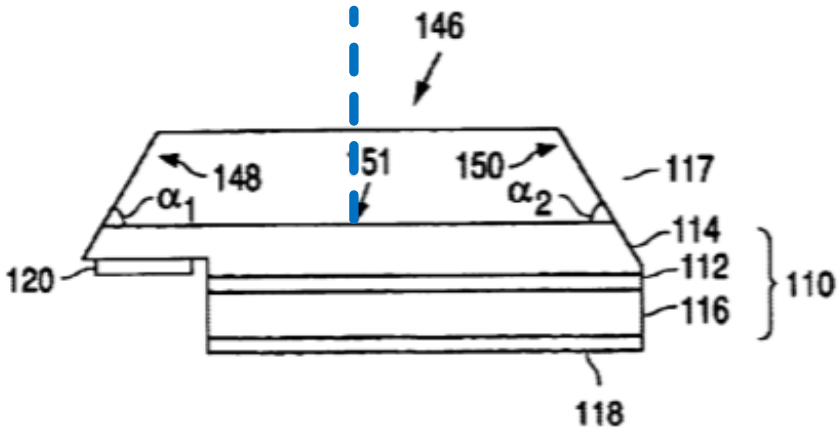


FIG. 7A

E. Ground 5: Claims 1-7 are obvious over *AAPA* in view of *Haitz* and *Steigerwald*

As discussed above, the ***AAPA*** discloses elements, 1,6[p], 1,6[a], 1,6[b] and the ohmic contacts of 1,6[e]. ***Haitz*** discloses the pyramidal substrate limitations.

Steigerwald discloses a non-conductive substrate, the "most" recitation and shows how the combined teachings of the references result in the "most" recitation. For the reasons below, it would have been obvious to combine teachings from ***Haitz*** and ***Steigerwald*** into the ***AAPA*** device.

1[c], 6[c]:

As discussed in X.C.1[c], ***Haitz*** discloses an LED having a thick n-type "body", which is its uppermost layer, and which has a centered, truncated, pyramidal shape, with facets arranged around a square LED, chosen to approximate a hemisphere or dome. It would have been obvious in view of ***Haitz*** to use this shape for the ***AAPA*** substrate 31. ***Haitz*** teaches that light may be trapped by TIR in a cuboidal structure like ***AAPA*** substrate 31:

> In such a rectangular body reflected rays never change their angle of incidence. In other words, rays emitted in a direction outside of the six escape cones will always remain outside of the escape cones no matter how many reflections they experience. Such rays keep bouncing around within the LED until they eventually are absorbed.

Ex. 1008, 2:4-10 and 1:36-50 (describing TIR light trapping within an LED). The POSA would have understood that this problem would also be present in the cuboidal substrate 31 of the ***AAPA***. Ex. 1012, ¶¶249-251. As discussed in X.C.1[c], ***Haitz*** teaches that this problem can be addressed by modifying the uppermost LED layer into a centered, truncated pyramid, which is an approximation of a hemisphere, which improves extraction, even for an extended p-n junction region like that pictured

in the ***AAPA***. Ex. 1008, 3:34-37; 3:65-68; 5:43-53; 4:53-5:3; Ex. 1012, ¶¶249-251. ***Haitz*** also teaches that a square device is advantageous because "the square LED with beveled edges…is a better approximation of a hemisphere than the rectangular parallelopipid of a conventional LED". Ex. 1008, 5:50-53; Ex. 1012, ¶250. Thus, as in X.C.1[c], the POSA would have understood that the ***AAPA*** device was ready for improvement with the teachings of ***Haitz***. Ex. 1012, ¶252.

The POSA would have understood that ***Haitz's*** improvement could be readily and predictably applied to the ***AAPA***. ***Haitz's*** thick n-layer is made from common, high index substrate materials that were known at the time of filing of the '460 patent and overlap with the substrates described in the '460 patent. Ex. 1008, 3:29-31 (discussing a GaP substrate); Ex. 1001, 2:36-45 (discussing a GaP substrate); Ex. 1012, ¶251. Furthermore, ***Haitz*** describes the same phenomena described in the ***AAPA*** where light is trapped by TIR within the LED die due to the index of refraction difference between the light emission surface and the surrounding environment. A POSA would understand that the solution proposed in ***Haitz*** to shape the light emission surface in the form of a centered truncated pyramid with decreasing cross sectional area from the junction would reduce the amount of light subject to TIR and thereby increase light emission. Ex. 1012, ¶251.

Additionally, the POSA would have been encouraged by ***Haitz's*** teaching that modifying cuboidal layers like the ***AAPA's*** is easily done while dicing with arrays of parallel cuts with a v-shaped dicing saw - a "straightforward adaptation of conventional

manufacturing techniques for semiconductors". See Ex. 1008, 5:4-34; Ex. 1012, ¶253. As discussed in X.C.1[c], the POSA would have been further motivated to select this shape to generate an axially symmetrical light emission pattern.

Thus, modification of the ***AAPA's*** cuboidal substrate with ***Haitz's*** teaching of a truncated pyramidal top layer would have been the application of a known modification (beveling a top layer), to a known device (the cuboidal substrate of the ***AAPA***), which was ready for improvement, to yield predictable result (decreased light trapping). Ex. 1012, ¶252.

For the reasons set forth above in section X.d, it would have been obvious to extend the pyramidal shape of the substrate down to the nearest doped layer, in view of the teachings of ***Haitz***. Ex. 1012, ¶254.

1[d], 6[d]:

If the ***AAPA*** does not disclose the "bound" element, ***Haitz*** does, and, it would have been obvious to include it in view of ***Haitz***, for the reasons discussed in X.C.1[d], specifically, because it would result from the efficient shaping and dicing method suggested by ***Haitz***. Ex. 1012, ¶255.

1[e], 6[e]:

As discussed in X.D.1[e], the **AAPA** discloses the "most" recitation by locating ohmic contacts on the bottom side of the device, where they leave substrate 31 unoccluded.

As discussed in X.B, if the "most" recitation requires more, ***Steigerwald*** discloses the recitation by teaching bottom side, reflective contacts, an index matched substrate and other light extraction features, which would have been obvious to include with the combined device of the ***AAPA*** and ***Haitz***. As discussed, incorporating these features results in "[v]irtually all light generated from the active region is coupled into the superstrate and has a high probability for escape through one of the five exposed superstrate surfaces", which means that most of the emitted light will be emitted through the substrate. Ex. 1004, 14:13-18; Ex. 1012, ¶¶257, 259. ***Steigerwald*** also teaches that most of the light for devices with non-index matched substrates will also be emitted through the substrate, and the use of a textured interface between the epitaxial region and the substrate to couple more light into a non-index matched substrate . Ex. 1004, 13:49-67; Ex. 1012, ¶257.

The POSA would have been motivated to incorporate ***Steigerwald's*** light extracting features into the combination in order to improve extraction efficiency, which is an interest of both ***Steigerwald*** and ***Haitz***. See Ex. 1004, 4:1-4 (touting the "increased extraction efficiency" of flip-chip LEDs); Ex. 1008, 2:52-53 ("It is… desirable to provide means for improving the efficiency of light extraction from an LED."); 1012, ¶258.

2 and 7:

As set forth in Ground 3, above, ***Haitz*** discloses truncated pyramidal LED surfaces having side wall bevel angles between 30° to 60°. The POSA would be

motivated to select angles within this range based on ***Haitz's*** teaching that this angle results in improvements in extraction efficiency relative to conventional cuboidal LEDs. Ex. 1008, 4:53-5:3 (describing 30° to 60° as "appropriate" with "good results" at 45˚; Ex. 1012, ¶260.

3:

Steigerwald discloses a non-conductive, sapphire substrate with a textured interface to reduce waveguiding, in connection with FIG. 13b. See X.B, above; Ex. 1004, FIG. 1; 13:55-67; 3:48-49; 10:2-3. As discussed in X.D.3, the POSA would have selected a sapphire substrate for reasons of cost and availability for GaN devices, and ***Steigerwald*** makes clear that this could be done while still producing a device where most of the emitted light was emitted through the substrate. Ex. 1012, ¶261.

4 - 5.

As discussed in X.C.1[c], 4-5 and X.E.1[c], ***Haitz*** teaches a centered, truncated, pyramidal top layer, with a flat top surface, which would have been obvious to use for the substrate 31 of the ***AAPA*** because it approximates a hemisphere and is easy to fabricate. The resulting shape would have a centered, flat top surface through which some light was emitted, as is shown in FIG. 2 of the ***AAPA***, which shows a ray being emitted through a flat, top portion of substrate 31 which would reman flat in the combination. Ex. 1012, ¶¶262-263. The POSA would omit ***Haitz's*** top contact from the combination, because it would block light from being emitted from the substrate, which runs counter to *Haitz's* interest in increasing extraction, and is unnecessary in the

AAPA device. *Id*., ¶262.

XI. CONCLUSION

For the foregoing reasons, all claims of the '460 patent are unpatentable. Petitioner respectfully requests cancellation of these claims.

Dated: February 11, 2020.

Respectfully submitted,

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CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on the 11th day of February, 2020, a complete copy of the Petition for *Inter Partes* Review of U.S. Patent No. 6,784,460, including all exhibits and other documents filed together with the Petition, were served via Priority Mail Express or by another means at least as fast and reliable, on the patent owner at the correspondence address of record for the patent:

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Petition complies with the word count limitation of 37 C.F.R. § 42.24(a)(1)(i) because the Petition contains 13990 words, including annotations added to figures and excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a)(1).

Date: February 11, 2020

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