UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES, INC.
Petitioner

v.

KONDA TECHNOLOGIES INC.
Patent Owner

Patent No. 10,003,553

PETITION FOR POST GRANT REVIEW
OF U.S. PATENT NO. 10,003,553

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I. INTRODUCTION

Flex Logix Technologies, Inc. ("Petitioner") requests post grant review ("PGR") of claims 1-7, 9-15, and 17-19 ("the challenged claims") of U.S. Patent No. 10,003,553 ("the '553 patent") (Ex. 1001), which, according to PTO records, is assigned to Konda Technologies, Inc. ("Patent Owner" or "PO"). For the reasons below, the challenged claims should be found unpatentable and canceled.

The '553 patent purports to be part of a family of applications based on U.S. Provisional Patent Application 61/531,615 ("the '615 provisional application") filed September 7, 2011. Prior to filing the '615 provisional application to which the '553 patent purports to claim priority, PO filed numerous patent applications concerning similar subject matter, and many of those earlier-filed applications are listed as related applications in the '553 patent. (Ex. 1001, 1:8-2:62.) During prosecution of applications claiming priority to the '615 provisional application, those earlier filed applications were relied on by the PTO for claim rejections.

In addressing those previous rejections based on its own earlier-filed subject matter, PO argued that the rejected claims included "rings" that were not disclosed in the earlier-filed applications. As demonstrated below, the claims of the '553 patent do not include any "rings," and the challenged claims of the '553 patent are anticipated or rendered obvious by PO's earlier-filed applications.

Similarly, during prosecution of an earlier-filed related application, PO added limitations to pending claims to overcome rejections based on *Wong*. However, the claims of the '553 patent do not include the features PO previously added in order to overcome *Wong*, and, as demonstrated in a concurrently filed petition, *Wong* anticipates the challenged claims of the '553 patent.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Parties-in-Interest

Petitioner identifies Flex Logix Technologies, Inc. as the real party-in-interest.

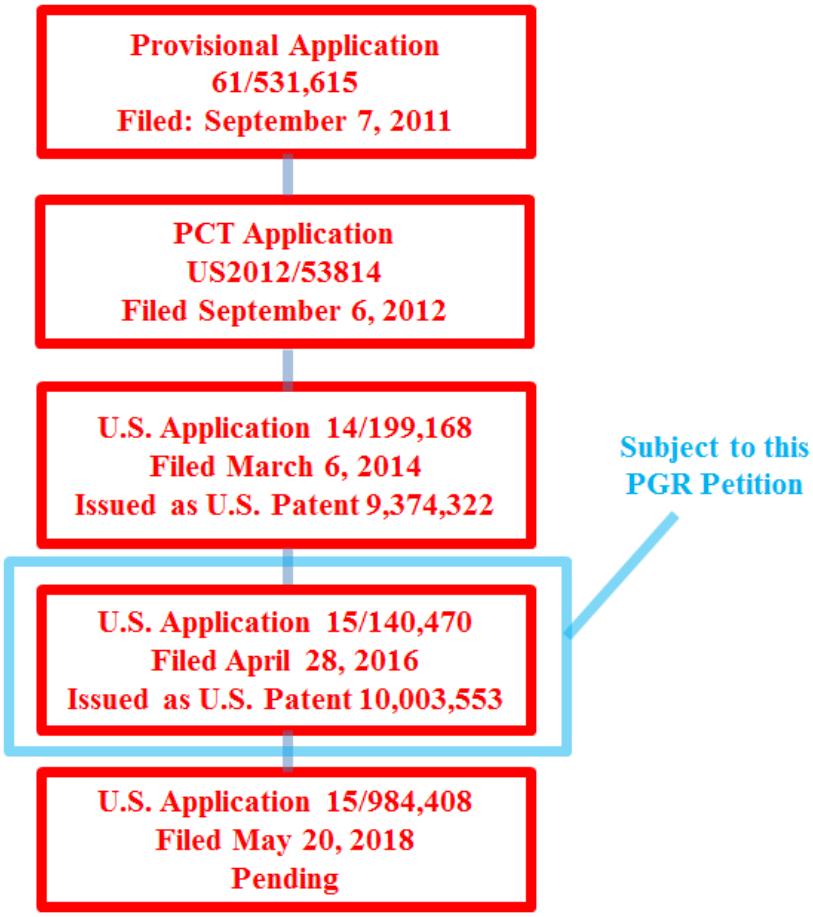
B. Related Matters

1. Lawsuit(s)

PO has asserted the '553 patent against Petitioner in *Konda Technologies Inc. v. Flex Logix Technologies, Inc.*, No. 5:18-cv-07581-LHK (N.D. Cal.). PO has also asserted U.S. Patent Nos. 8,269,523 ("the '523 patent"), 8,898,611 ("the '611 patent"), 9,529,958 ("the '958 patent"), and 10,050,904 ("the '904 patent") in the foregoing district court litigation.

2. Related Applications

The '553 patent is related to several patents and/or patent applications, as shown in the purported priority chain below:



3. Concurrently filed petitions

Petitioner is concurrently filing two other petitions for PGR of certain claims of the ’553 patent.

C. Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Quadeer A. Ahmed (Reg. No. 60,835). Service information is Paul

Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-FlexLogix-Konda-PGR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. TIME FOR FILING UNDER 37 C.F.R. § 42.202

The '553 patent issued on June 19, 2018, and this Petition is being timely filed no later than the date that is nine months after the date of the grant of the '553 patent.

V. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.204(a)

Petitioner certifies that the '553 patent is available for PGR and Petitioner is not barred or estopped from requesting PGR on the grounds identified herein.

As discussed below in Section IX, the '553 patent is eligible for PGR because it has at least one claim that is not entitled to a pre-AIA filing date.

VI. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

A. Claims for Which Review is Requested

Petitioner respectfully requests review of claims 1-7, 9-15, and 17-19 ("challenged claims") of the '553 patent, and cancellation of these claims as

unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following grounds:

Ground 1: Claims 1-7, 9-15, and 17-19 are unpatentable under AIA 35 U.S.C. § 102(a)(1) as being anticipated by Published PCT Application No. WO 2008/109756 ("*Konda '756 PCT*") (Ex. 1009).

Ground 2: Claims 1-7, 9-15, and 17-19 are unpatentable under AIA 35 U.S.C. § 103 as obvious over *Konda '756 PCT* in view of U.S. Patent No. 6,940,308 to Wong ("*Wong*") (Ex. 1008).

The earliest possible priority date for the '553 patent is September 7, 2011, which corresponds to the filing date of the '615 provisional application. (Ex. 1007, 90). *Konda '756 PCT* published September 12, 2008, and *Wong* issued on September 6, 2005. Thus, *Konda '756 PCT* and *Wong* are prior art at least under AIA U.S.C. § 102(a)(1) with respect to the '553 patent.

Konda '756 PCT was not considered by the Patent Office during prosecution. *Wong* was considered by the Patent Office during prosecution. However, Petitioner presents *Wong* in a new light never considered by the Office. For example, the prosecution history of the '553 patent does not include

substantive discussion of *Wong* or any other prior art reference relating to patentability of the '553 patent claims. Indeed, there were no claim rejections based on any prior art. Here, Petitioner presents testimony from R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '553 patent (Ex. 1002, ¶¶3-13, 18; Ex. 1003), who confirms that the relevant teachings of *Konda '756 PCT* and *Wong* disclose or suggest what is claimed by challenged claims 1-7, 9-15, and 17-19 of the '553 patent. (*See* Ex. 1002, ¶¶86-187; *see also infra* Section XIII.)

As such, any consideration of *Wong* by the Patent Office during prosecution of the '553 patent should not preclude the Board from considering and adopting the ground in this petition.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '553 patent would have had a master's degree in electrical engineering or a similar field, and at least two to three years of experience with integrated circuits and networks. (Ex. 1002, ¶18.) More education can supplement practical experience and vice versa. (*Id*.)

VIII. BACKGROUND

The ’553 patent generally relates to switching networks that can be used to route signals between logic blocks included on an integrated circuit device such as an FPGA. (Ex. 1002, ¶¶20-50.)

A. The ’553 Patent

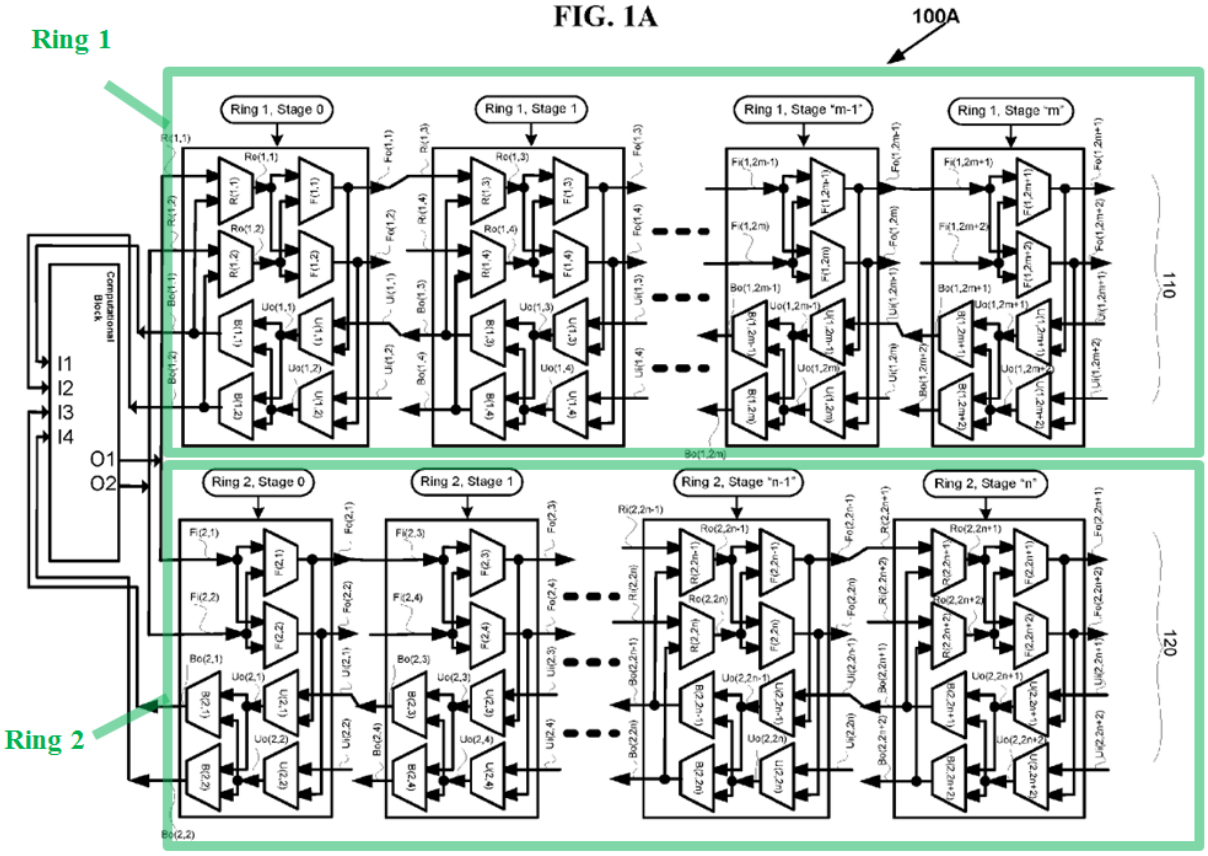
The ’553 patent, which matured from the U.S. Application No. 15/140,470 (“the ’470 application”), acknowledges that multi-stage hierarchical networks were known and used in many applications at the time of the alleged invention, such as in “FPGA routing of hardware designs.” (Ex. 1001, 2:66-3:1, 4:47-48.) The ’553 patent states that known VLSI (very large scale integration) layouts for integrated circuits with such networks, such as the Benes network disclosed by *Wong* (Ex. 1008) are “inefficient and complicated.” (*Id.*, 3:2-4, 3:30-36.) For instance, the ’553 patent contends that prior art network layouts “require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the signal which effect the maximum clock speed of operation.” (*Id.,* 3:43-48; Ex. 1002, ¶¶31-32 (citing Ex. 1040).)

The ’553 patent alleges to disclose “[s]ignificantly optimized multi-stage networks, useful in wide target applications” where the “optimized multi-stage

networks in each block *employ several rings* of stages of switches with inlet and outlet links." (Ex. 1001, 3:58-67 (emphasis added).) As discussed below, PO touted this concept of "rings" in the '553 patent family as an important distinction over PO's earlier patent applications, and, not surprisingly, the claims in the applications to which the '553 patent claims priority (and the originally filed claims in the '470 application itself) all include the "ring" concept. However, these "rings"—which (i) the '553 patent describes as an important aspect of the alleged optimizations to the prior art multi-stage hierarchical networks, and (ii) PO touted as an important distinction over PO's other applications—are not recited in the claims of the '553 patent. (Ex. 1002, ¶¶33-38.)

First, the '553 patent's disclosure emphasizes "rings." Each of figures 1-15 of the '553 patent illustrates, describes, or relates to the use of "rings" in a "multi-stage hierarchical network." (Ex. 1002, ¶33 (citing Ex. 1001, 4:42-6:22, FIGs. 1-15, 8:56-9:3, 33:26-48).) Annotated figure 1 of the '553 patent below shows two such "rings":

FIG. 1A



(Ex. 1001, FIG.1 (annotated); Ex. 1002, ¶38.) Similarly, the figures that depict example "stages" in the '553 patent are described as illustrating portions of a "ring." (Ex. 1001, 4:56-5:3, 5:32-6:6, FIGs. 2A-2E, 9A-11C.)

Second, during prosecution of U.S. Application No. 14/199,168 ("the '168 application"), which issued as U.S. Patent No. 9,374,322 ("the '322 patent") (*see supra* Section II.B.2), PO explicitly defined "rings" and argued that the inclusion of such rings was a "key difference[]" with respect to PO's earlier alleged inventions disclosed in U.S. Patent No. 8,898,611 ("the '611 patent").

> *Current application discloses stages in rings where forward connecting links are feedback into backward connecting links through one or more multiplexers and also backward connecting links are feedback into forward connecting links through one or more multiplexers,* where US Patent No. 8,898,611 discloses folded and butterfly fat tree networks where in each stage only forward connecting links are feedback into backward connecting links . . . *This is one of the key differences in the current invention*. . .

(Ex. 1005, 97-98 (emphases added).)

> The ring concept disclosed in the current application is not a true ring, the term ring is used in the current invention since in each stage backward connecting links are feedback to forward connecting links and vice versa as opposed to only a U-turn in original multi-stage networks.

(*Id.,* 101; *see also* Ex. 1001, 2:33-38; Ex. 1002, ¶¶39-42.)

The claims of the ’322 patent all include this “ring” concept. (Ex. 1035, 47:42-51:3.) Similarly, all of the claims of PCT Application No. PCT/US12/53814 (“the ’814 PCT application”) to which the ’168 application claims priority also

include this "ring" concept. (Ex. 1006, 79-82 (1:3-4:23).)[1].) Indeed, the originally filed claims in the '470 application also include "rings" (Ex. 1004, 286-292) and further include specific limitations consistent with the definition PO provided for a "ring" during prosecution of the '168 application. (*Id*., 287 (82:13-18)[2]; Ex. 1002, ¶¶39-41.)

But in contrast to the originally filed claims in the '470 application, the issued claims in the '322 patent, and the claims in the 814 PCT application, new claims 21-40 that were added by amendment during prosecution of the '470 application and that issued as claims 1-20 in the '553 patent **do not** include "rings." (Ex. 1004, 77-84.)[3] In other words, issued claims 1-20 of the '553 patent

[1] The '814 PCT application as filed had errors in pagination such that the section that includes the claims restarts the pagination at page 1. Therefore, citations to the '814 PCT application include both a page number for the exhibit as well as the page and line numbers printed on the page identified within the exhibit.

[2] When appropriate, citations to the as-filed '470 application include page and line numbers corresponding to the application.

[3] While the Examiner noted in an Interview Summary that the newly presented claims would be reviewed for their compliance with 35 U.S.C. § 112, the claims

are missing a feature that is not only highlighted in the specification as an alleged fundamental point of novelty, but was in fact touted by PO as a "key difference[]" between the disclosure of the '553 patent family and another patent family belonging to PO. (Ex. 1002, ¶42.)

B. Material Incorporated by Reference in the '553 Patent

The '553 patent attempts to incorporate by reference a list of more than 20 patents and patent applications. (Ex. 1001, 1:8-2:62; Ex. 1002, ¶37.) However, the incorporations by reference of these patents and applications provide no "detailed particularity [regarding] what specific material" they incorporate and do not "clearly indicate where that material is found" in the patents and applications. *Cook Biotech Inc. v. Acell, Inc.*, 460 F. 3d 1365, 1376 (Fed. Cir. 2006); *see also Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018) ("To incorporate material by reference, the host document must identify with detailed particularity what specific material it incorporates and clearly indicate where that material is found in the various documents.") (internal citations and quotation

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were subsequently allowed without any further rejections. (Ex. 1004, 51, 25-32.) The issued claims, however, do not comply with the requirements of 35 U.S.C. § 112, as demonstrated in the concurrently filed PGR petition.

marks omitted). Indeed, even when material is properly incorporated, "[i]t is not sufficient for purposes of the written description requirement of § 112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to the modifications that the inventor might have envisioned, but failed to disclose." *D Three Enters., LLC v. Sunmodo Corp.*, 890 F.3d 1042, 1050 (Fed. Cir. 2018) (internal citation omitted).

The '553 patent simply identifies several patents and patent applications and states that the material is incorporated in its entirety without specifying any particular portions of the documents as being relevant. (Ex. 1001, 1:8-2:62) *Cook Biotech Inc.*, 460 F. 3d at 1376; *see also Nautilus, Inc. v. Icon Health & Fitness Inc.*, IPR2017-01408, 2018 WL 6318050, at *20 (PTAB Dec. 3, 2018) (allowing incorporation by reference where the incorporating language provided detail regarding what was disclosed in the incorporated by reference). Moreover, many, if not all, of those incorporated patents and applications also incorporate by reference other patents and applications. (*See, e.g.*, Ex. 1007, 5-6; Ex. 1006, 1-3 (1:5-3:6).) Without providing sufficient particularity such that a POSITA would recognize what is being incorporated by reference, the material incorporated by reference cannot be relied upon to determine the scope of the claims or to remedy

defects in the '553 patent, such as lack of written description of the claimed subject matter under 35 U.S.C. §112.[4]

Indeed, any such reliance would impermissibly require a POSITA to look at the different embodiments disclosed in the various patents and make unspecified combinations of elements without any guidance as to what should be combined or how such combinations should be accomplished. *D Three Enters., LLC*, 890 F.3d at 1050. Patentees' attempts to show written description support by relying on an unspecified combination of teachings from incorporated material and the disclosure of the patent have repeatedly been rejected. *Nautilus, Inc.*, IPR2017-01408, 2018 WL 6318050 at *20-23 (rejecting PO's attempt to combine teachings from incorporated reference with disclosure of patent-at-issue in an effort to show

[4] Elsewhere in the specification, the '553 patent describes certain prior art multi-stage networks disclosed in U.S. patents that were previously incorporated by reference. (Ex. 1001, 7:32-8:19.) But that portion of the specification simply notes that the alleged "optimization" techniques disclosed in the '553 patent may be implemented in certain prior art multi-stage networks, i.e., it does not rely on any concepts disclosed in the referenced U.S. patents for purposes of supporting the disclosure of the '553 patent. (*Id.*, 7:32-37.)

written description support for disputed claim limitation, noting that "obviousness is not the standard for written description"); *Purdue Pharma L.P. v. Recro Tech., LLC*, 694 F. App'x 794, 797 (Fed. Cir. 2017) (affirming Board's finding that claims lack written description support and stating that "[t]o the extent that Purdue contends that a person of skill in the art would isolate and combine aspects from various embodiments in the specifications (including patents incorporated by reference involving a different drug) to obtain the claimed invention [for written description support], Purdue relies upon the wrong test."); *see also Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997); *Ariad Pharms., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc); *Trans Video Elecs., Ltd. v. Sony Elecs., Inc.*, 822 F. Supp. 2d 1020, 1027 (N.D. Cal. 2011).

Therefore, in light of the lack of particularity provided by the limited description of the material incorporated by reference in the '553 patent, the patents and patent applications incorporated therein should not be considered in determining whether the claims comply with the requirements of 35 U.S.C. § 112. Moreover, even if considered, the material incorporated by reference cannot cure the deficiencies identified herein. (*See, e.g.*, *infra* Section IX.)

IX. PGR ELIGIBILITY

The PGR provisions of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA") apply to patents subject to the first inventor to file provisions of the AIA, i.e., patents having at least one claim with an effective filing date on or after March 16, 2013. *Grunenthal GmbH v. Antecip Bioventures II LLC*, PGR2018-00001, Paper 17 at 9-10 (May 1, 2018). A claim in a U.S. application is entitled to the benefit of the filing date of an earlier filed U.S. or PCT application if the subject matter of the claim is disclosed in the earlier filed application in accordance with the written description requirement. *PowerOasis, Inc. v. T-Mobile USA, Inc*., 522 F.3d 1299, 1306 (Fed. Cir. 2008) (subject matter disclosed for first time in a continuation application does not receive benefit of the parent's filing date); *see also In re Gosteli*, 872 F.2d 1008, 1010–11 (Fed. Cir. 1989).

To comply with the written description requirement, the specification or earlier-filed application "must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed." *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed Cir. 2005); *see also Lockwood*, 107 F.3d at 1572; *Allergan, Inc. v. Sandoz Inc*., 796

F.3d 1293, 1308-09 (Fed. Cir. 2015). "The test requires an objective inquiry in to the four corners of the specification from the perspective" of a POSITA. *Ariad*, 598 F.3d at 1351. Whether the added subject matter is an obvious variant of the disclosed subject matter is irrelevant. *Lockwood*, 107 F.3d at 1572.

The chart above in Section II.B.2 shows that the '553 patent relates to two applications filed prior to March 16, 2013, namely the '615 provisional application (Ex. 1007) and the '814 PCT application (Ex. 1006). The '553 patent is eligible for PGR because it has at least one claim that is not entitled to the filing date of either the '615 provisional application or the '814 PCT application ("the two pre-AIA applications"). In particular, at least claims 1, 2, 4, 9, 11, 12, and 14 of the '553 patent include subject matter that is not disclosed in the two pre-AIA applications. *PowerOasis, Inc.*, 522 F.3d at 1306; *In re Gosteli*, 872 F.2d at 1010–11. (Ex. 1002, ¶¶52-75.)

Claims 1, 2, 4, 9, 11, 12, and 14 are not entitled to a pre-March 16, 2013 filing date as discussed below, thereby confirming PGR eligibility. (Ex. 1002, ¶52.)

A. The Two Pre-AIA Applications Do Not Support Switches Configurable By a Flip Flop (Claim 9)

Claim 9 of the '553 patent, which depends from claim 1, recites "each switch configurable by an SRAM Cell or a Flash Cell or *a flip-flop*." (Ex. 1001, 50:31-32 (emphasis added).) A "flip-flop" is never mentioned in the two pre-AIA applications. (*See generally* Exs. 1006-1007.)

The disclosure of the '814 PCT application (including the claims) is limited to describing switches as being configurable by an SRAM Cell or a Flash Cell. (Ex. 1002, ¶53.) For example, the '814 PCT application indicates that in the context of "programmable integrated circuit embodiments," switches or crosspoints that determine how inlet links and outlet links are connected can be controlled by a "programmable cell." (Ex. 1006, 75 (75:4-10).) Specifically, the '814 PCT application discloses:

> In volatile programmable integrated circuit embodiments the programmable cell may be an *SRAM (Static Random Address Memory) cell.* In non-volatile programmable integrated circuit embodiments the programmable cell may be a *Flash memory cell.*

(*Id*., 75 (75:23-26) (emphases added).)

> In other embodiments all the *d* * *d* switches described in the current invention are also implemented using muxes

> of different sizes controlled by *SRAM cells* or *flash cells* etc.

(*Id*., 76 (76:4-6) (emphasis added); Ex. 1002, ¶53.)

Thus, the '814 PCT application does not disclose the "flip-flop" feature recited in claim 9. (Ex. 1002, ¶54.)

The '615 provisional application does not include any disclosure relating to a "flip-flop" and does not even describe configuring switches using SRAM and Flash cells. (*See generally* Ex. 1007; Ex. 1002, ¶54.)

Thus, neither of the two pre-AIA applications conveys to a POSITA that the named inventor had possession of the features claimed at the relevant time. Neither mentions a "flip-flop" in any respect, let alone in the context of controlling a switch as recited in issued claim 9.[5] Indeed, the first appearance of the term

[5] While the two pre-AIA applications generally purport to incorporate a number of additional patents/patent applications by reference, neither pre-AIA application includes any explanation regarding the relevance of the incorporated material. Thus, as discussed above, Patent Owner cannot rely on such incorporated material in an effort to make up for the lack of disclosure in the as-filed application disclosures. (*Supra* Section VIII.B.) In any event, none of the material

"flip-flop" was in a new claim 29 (which issued as claim 9) added January 8, 2018 during prosecution of the '470 application. (Ex. 1004, 63, 69 ("2018 January 08"), 80.) Therefore, claim 9 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the '470 application.[6] (Ex. 1002, ¶¶55-56.)

B. The Two Pre-AIA Applications Do Not Support Claims 1, 2, 4, 11, 12, and 14

Claim 4 of the '553 patent depends from claim 2, which in turn depends from claim 1. Similarly, claim 14 depends from claim 12, which in turn depends from claim 11. Each of claims 1, 2, 4, 11, 12, and 14 is not supported by the two pre-AIA applications, as discussed below. (Ex. 1002, ¶¶57-75.)

Claim 1 of the '553 patent recites in part:

> forward connecting links comprising … zero or more *cross links connected from a switch in a stage in a*

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incorporated by reference supports the claimed "flip-flop" features. (Ex. 1002, ¶55, n.6.)

[6] The '168 application, which is a post-AIA application, includes essentially the same disclosure as the '814 PCT application. (Ex. 1002, ¶55.) Thus, the '168 application also does not disclose the "flip-flop" feature. (*Id*.)

> *subnetwork to a switch in the same numbered stage in one or more other subnetworks* …
>
> backward connecting links comprising … zero or more *cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks*

(Ex. 1001, 49:27-40 (emphases added).)

To the extent the claims can be understood, claim 1 includes forward and backward connecting links that include *cross links* between switches connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks. (*Id.*) Claim 2 adds that those *cross links* are implemented as vertical links only, or horizontal links only, or both vertical links and horizontal links. (Ex. 1001, 49:41-45.) Claim 4 further limits the *cross links* that are horizontal links to either being of "substantially of equal length in the entire two-dimensional grid of rows and columns" or being "of a *hop length h*" "*where "h ≥ 0*." (*Id.*, 49:60-50:2.) Claim 4 also limits the cross links that are vertical links to either being of "substantially of equal length in the entire two-dimensional grid of rows and columns" or being "of a *hop length v*" "*where "v ≥ 0*." (*Id.*; Ex. 1002, ¶¶57-58.)

As set forth below, there is no disclosure of "forward connecting links" or "backward connecting links" that are "cross links" "connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks" in the two pre-AIA applications, let alone disclosure of any such links that have the additional features recited in claims 2 and 4. (Ex. 1002, ¶59.)

1. Claim 1

The first appearance of a "*cross link*" "connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks" was on January 8, 2018 when claim 21 (which eventually issued as claim 1) was added during prosecution of the '470 application. (Ex. 1004, 69 ("2018 January 08"), 77-78; *see also id.*, 61-62; Ex. 1001, 48:62-49:40.) But the two pre-AIA applications do not provide written description support for the "cross links" features of claim 1. (Ex. 1002, ¶¶60-61.)

For example, outside of the Abstract[7] and the material incorporated by reference[8] in the specification of the '814 PCT application, the only mention of "cross links" in the specification is in the "Summary of the Invention":

[7] The Abstract's referral to networks that "employ shuffle exchange links where outlet links of cross links from switches in a stage of a ring in one sub-integrated

> The optimized multi-stage networks with their VLSI layouts employ shuffle exchange links where outlet links of *cross links from switches in a stage* of a ring in one sub-integrated circuit block *are connected to either inlet links of switches in the another stage* of a ring in another sub-integrated circuit block *or inlet links of switches in the another stage* of a ring in the same sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice-versa.

(Ex. 1006, 5 (5:3-8) (emphases added); Ex. 1002, ¶62.)

This isolated reference to "cross links" is limited to "cross links" connected "from switches in a stage" to switches in "*another* stage."[9] The same is true with

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circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block" is substantively the same as that contained in the cited portion. (Ex. 1006, Abstract, 5:3-8.)

[8] *See supra* n.5.

[9] To the extent that PO argues that "another stage" should be understood broadly such that it encompasses "a same stage" or "a different stage," such an argument would be inconsistent with the use of the "same" and "another" terms in the '553 patent and its family. For example, the '814 PCT application states "another stage

respect to the "cross links" recited in the claims of the '814 PCT application, i.e., they recite "cross links connecting from a switch in a stage ... to a switch in *another stage*," where the cross links in the '814 PCT application are included in forward and backward connecting links that connect "from switches in lower stage to switches in the *immediate succeeding higher stage*" and "from switches in higher stage to switches in the *immediate preceding lower stage*," respectively. (Ex. 1006, 80 (2:4-13) (emphasis added).) Thus, the '814 PCT application does not describe any "cross link" that is "connected from a switch in a stage in a

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of a ring *in the same or another* sub-integrated circuit block" (Ex. 1006, 83 (1:14-15) (emphasis added)), thereby making clear that "another" is used to mean "a different" and not "the same or a different." The '814 PCT application further states the cross links "are connected to either inlet links of switches in the another stage of a ring *in another sub-integrated circuit block or* inlet links of switches in the another stage of a ring *in the same sub-integrated circuit block*." (*Id*., 5 (5:3-8) (emphases added).) Therefore, PO explicitly distinguishes between "same" and "another" in the context of the sub-integrated circuit blocks in the '553 patent and its family. (Ex. 1002, ¶63.)

subnetwork to a switch in the *same numbered stage* in one or more other subnetworks" as recited in claim 1. (Ex. 1002, ¶64.)

Outside of the material incorporated by reference,[10] the '615 provisional application does not include any disclosure relating to a "cross link." (*See generally* Ex. 1007; Ex. 1002, ¶65.)

Accordingly, claim 1 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the '470 application.[11] (Ex. 1002, ¶65.)

2. Claim 2

Claim 2 depends from claim 1 and recites "*said cross links* between switches of stages in any two said subnetworks are connected as either vertical links only, or horizontal links only, or both vertical links and horizontal links." (Ex. 1001, 49:41-45.) The first appearance of the above-noted features of claim 2 in conjunction with the "cross links" of claim 1 was in newly added claim 22 (which issued as claim 2) submitted January 8, 2018 during prosecution of the '470

[10] *See supra* n.5.

[11] The '168 application also does not disclose the "same numbered stage" feature of claim 1. (Ex. 1002, ¶64; *see also supra* n.6.)

application. (Ex. 1004, 69 ("2018 January 08"), 79; *see also id.*, 62; Ex. 1001, 49:41-45; Ex. 1002, ¶67.)

As discussed above, no "cross links" having the characteristics recited in claim 1 are disclosed in the two pre-AIA applications. (*See supra* Section IX.B.1.) Thus, assuming the recitation of "said cross links" in claim 2 modifies the "zero or more cross links" recited in claim 1, it logically follows that these pre-AIA applications cannot support such "cross links" as further modified by claim 2. Therefore, claim 2 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the '470 application.[12] (Ex. 1002, ¶66.)

3. Claim 4

a) The "Substantially of Equal Length" Feature Is Not Supported

Claim 4 depends from claim 2 and recites "said horizontal links between switches in two said stages are *substantially of equal length* and said vertical links between switches in two said stages are *substantially of equal length* in the entire two-dimensional grid of rows and columns." (Ex. 1001, 49:60-65.) The first

[12] The '168 application also does not disclose the features of claim 2. (Ex. 1002, ¶66; *see also supra* n.6.)

appearance of the above-noted features of claim 4 in conjunction with the above-discussed features of claims 1 and 2 was in newly added claim 24 (which issued as claim 4) submitted January 8, 2018 during prosecution of the '470 application. (Ex. 1004, 69 ("2018 January 08"), 78; *see also id.*, 62; Ex. 1001, 49:60-50:2; Ex. 1002, ¶68.)

As discussed above, no "cross links" as recited in claim 1 or as further characterized by claim 2 are disclosed in the two pre-AIA applications. (*See supra* Sections IX.B.1-2.) Thus, assuming the recitation of "said horizontal links" and "said vertical links" in claim 4 further modifies the horizontal and vertical links recited in claim 2, which in turn modify the "zero or more cross links" recited in claim 1, it logically follows that these pre-AIA applications cannot support such "cross links" as further modified by claim 4. Therefore, claim 4 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the '470 application.[13] (Ex. 1002, ¶69.)

[13] The '168 application does not disclose the features of claim 4. (Ex. 1002, ¶69; *see also supra* n.6.)

b) The "Hop Length" Features Are Not Supported

Claim 4 also recites "said horizontal links between switches in two said stages are substantially of a *hop length h* and said vertical links between switches in two said stages are substantially of a *hop length v* where $h \geq 0$ *and* $v \geq 0$." (Ex. 1001, 49:60-50:2.) As is the case for the other features recited in claim 4, assuming this feature regarding "hop length" further modifies the "cross links" as recited in claim 1 and further characterized by claim 2, no such cross links are disclosed in the two pre-AIA applications. (Ex. 1002, ¶70; *see supra* Section IX.B.1.)

Moreover, as discussed below, the claimed ranges of hop length "$h \geq 0$ *and* $v \geq 0$" are not supported by the two pre-AIA applications *in any context*. Indeed, prior to the filing of claim 24 during prosecution of the '470 application, there was no recitation of a hop length of "0" and only hop lengths ≥ 1 were previously described or claimed. (Ex. 1002, ¶71.)

The first appearance of a horizontal or vertical "hop length" "≥ 0" in relation to any link was in claim 24 (now claim 4) submitted January 8th, 2018 during prosecution of the '470 application. (Ex. 1004, 69 ("2018 January 08"), 79; Ex. 1001, 49:60-50:2.) But the specification of the '470 application explicitly states that each of the horizontal and vertical hop lengths is a positive number, therefore

making a hop length of 0, which is included in the claimed ranges, outside the scope of the disclosure of the '470 application. (Ex. 1004, 253 (48:14-18) ("'Vx' denotes an external vertical hop wire … with 'x' vertical hop length, where 'x' is a positive integer."), 256 (51:10-14) ("'Hx' denotes an external horizontal hop wire … with 'x' horizontal hop length where 'x' is a positive integer."); 259 (54:6-8) ("In general the hop length of an external vertical hop wire can be *any positive number*. Similarly, the hop length of an external horizontal hop wire can be *any positive number*.") (emphases added).) Zero is not a positive number and therefore is not included in the disclosed ranges of hop-length. (Ex. 1002, ¶72.)

The same description of hop lengths being limited to positive numbers is present in the '814 PCT application (Ex. 1006, 47 (47:1-5), 49 (49:26-30), 52 (52:23-25)) and the '615 provisional application (Ex. 1007, 35 (31:9-13), 38 (34:5-9), 41 (37:3-5)). None of the applications as filed, including the '470 application itself, mentions a "hop length" of "0," let alone such a hop length in the context of the "cross links" set forth in claim 1. (Ex. 1002, ¶73.)

Accordingly, claim 4 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the '470 application.[14, 15] (Ex. 1002, ¶74.)

[14] *See supra* n.5.

4. Claims 11, 12, and 14

Claims 11, 12, and 14 recites features analogous to those discussed above with respect to claims 1, 2, and 4, respectively. For example, just like claim 1, claim 11 recites "zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks." (Ex. 1001, 51:14-17, 51:25-28; *see also id.*, 49:30-33, 49:37-40.) Similarly, like claim 2, claim 12 recites that "zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks." (*Id.*, 51:32-36; *see also id.*, 49:41-45.) And claim 14, like claim 4, recites cross links that are horizontal links are of "substantially of equal length in the entire two-dimensional grid of rows and columns" or being "of a *hop length h*" "*where "h ≥ 0.*" (*Id.*, 51:51-52:7; *see also id.*, 49:60-50:2.) Claim 14, like claim 4, also recites that cross links that are vertical links are of "substantially of equal length in the entire two-dimensional grid of rows and columns" or being "of a *hop length v*" "*where "v ≥ 0.*" (*Id.*, 51:51-52:7; *see also id.*, 49:60-50:2; Ex. 1002, ¶75.) Thus, for at least the same

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[15] The '168 application does not disclose the features of claim 4. (Ex. 1002, ¶73; *see also supra* n.6.)

reasons discussed above, neither of the two pre-AIA applications conveys to a POSITA that the named inventor had possession of the above-noted features set forth in claims 11, 12, and 14 at the relevant time.[16] Accordingly, claims 11, 12, and 14 are not entitled to an effective filing date earlier than the April 28, 2016 filing date of the '470 application.[17] (*Supra* Sections IX.B.1-3; Ex. 1002, ¶75.)

C. AIA Applicability

As discussed above, at least claims 1, 2, 4, 9, 11, 12, and 14 of the '553 patent include subject matter that is not disclosed by a pre-March-16-2013 application. As such, the '553 patent is eligible for PGR. Further, because at least claims 1, 2, 4, 9, 11, 12, and 14 are not entitled to a priority date prior to March 16, 2013, every claim of the '553 patent is subject to the first-to-file provisions of § 102(a). *See MPEP* at § 2159.02.

X. CLAIM CONSTRUCTION

In a post grant review, claims are construed in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in

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[16] *See supra* n.5.

[17] The '168 application does not disclose the features of claims 11, 12, and 14. (Ex. 1002, ¶75; *see also supra* n.6.)

the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.200(b). In particular, claim terms are generally given their "ordinary and customary meaning," that is, "the meaning that the term would have to a POSITA in question at the time of the invention, i.e., as the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*). In the case that "the specification . . . reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess . . . the inventor's lexicography governs." *Id.* at 1316 (internal citation omitted).

The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems*, Inc., IPR2015-00633, Paper 11 at 16 (August 14, 2015). Petitioner submits that for purposes of this proceeding, no term requires construction. (Ex. 1002, ¶51.)

XI. EARLIEST EFFECTIVE FILING DATE OF THE '553 PATENT

As discussed above, the two pre-AIA applications and the post-AIA '168 application do not provide adequate written description support for at least the "*same numbered stage*" feature in independent claims 1 and 11. (*Supra* Sections IX.B.1, IX.B.4.) Claims 2-10 and 12-20 depend from independent claims 1 and

11, and consequently are also not supported by the two pre-AIA applications and the post-AIA '168 application.

Thus, for purposes of this proceeding, the challenged claims are not entitled to an effective filing date any earlier than the April 28, 2016 filing date of the '470 application.

XII. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: *Konda '756 PCT* Anticipates Claims 1-7, 9-15, and 17-19

Konda '756 PCT (Ex. 1009) was published September 12, 2008. *Konda '756 PCT*, which is titled "Fully Connected Generalized Multi-Stage Networks," is generally directed to a multi-stage network for nonblocking connections. (Ex. 1009, Title, 5:10-6:6.) *Konda '756 PCT* incorporates by reference, among other applications, U.S. Provisional Patent Application 60/984,724 ("the '724 provisional application"). (Ex. 1009, 2:18-21.) The '724 provisional application as filed became publically available as of the date of *Konda '756 PCT* publication, i.e., September 12, 2008. *See* 37 C.F.R. § 1.14(a)(1)(vi) ("Unpublished pending applications (including provisional applications) that are *incorporated by reference* or otherwise identified. A copy of the application as originally filed of an *unpublished pending application may be provided to any person*, upon written request and payment of the appropriate fee, *if the application is incorporated by*

reference or otherwise identified in a U.S. patent, a statutory invention registration, a U.S. patent application publication, *an international publication of an international application under PCT Article 21(2) . . . .*" (emphasis added))[18]; *Ex Parte Xiaoming Bao & Stephen M. Allen*, Appeal No. 2016-006293, 2017 WL 1397726, at *4 (PTAB Mar. 28, 2017) ("When Kovalic [an international application] published in July 2009, the Kovalic Provisional published as well.") (citing *Ex Parte Yamaguchi*, 88 U.S.P.Q.2d 1606, 2008 WL 4233306, at *6 (B.P.A.I. Aug. 29, 2008) (precedential opinion) ("[W]hile provisional applications are not themselves published under 35 U.S.C. § 122(b)(2)(A)(iii), the corresponding regular utility application that claims priority to a provisional application under § 119(e) is generally published (with certain exceptions) after 18

[18] In litigation PO contends that the '724 provisional application "did not become available to the public as of the [September 12, 2008] publication date" of the '756 PCT application because "Dr. Konda never gave permission to anyone." (Ex. 1036, 7-8.) Petitioner submits that PO misreads 37 C.F.R. § 1.14(a)(1)(vi) and that such permission would only be required for "access to the paper file" of the '724 provisional application, whereas the application itself was publicly available as of September 12, 2008.

months. *Upon such publication, not only is the regular utility application laid open to the public, but its corresponding provisional application is likewise made available to the public*." (emphasis added) (footnote omitted) (citation omitted))).

Moreover, because the '724 provisional application is incorporated by reference in *Konda '756 PCT*, the contents of the '724 provisional application were effectively contained in *Konda '756 PCT* itself when it was published. *See MPEP* at § 2163.07(b) ("Instead of repeating some information contained in another document, an application may attempt to incorporate the content of another document or part thereof by reference to the document in the text of the specification. The information incorporated is as much a part of the application as filed as if the text was repeated in the application, and should be treated as part of the text of the application as filed.")

As discussed below, the '724 provisional application, which is part of *Konda '756 PCT*, discloses the features of claims 1-7, 9-15, and 17-19.[19]

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[19] Petitioner's analysis of *Konda '756 PCT* with respect to the challenged claims focuses solely on the disclosure of the '724 provisional application incorporated therein. In other words, the analysis does not involve combining disclosure in the

1. Claim 1

Konda '756 PCT discloses each and every feature of claim 1. (Ex. 1002, ¶¶87-134.)

a) "A network implemented in a non-transitory medium comprising"

To the extent the preamble is limiting, *Konda '756 PCT*, by way of its incorporation of the '724 provisional application, discloses a network implemented in a non-transitory medium. (Ex. 1002, ¶¶88-91.) For example, the '724 provisional application discloses that "[t]he present invention is concerned with the VLSI layouts of arbitrarily large switching networks for broadcast, unicast, and multicast connections." (Ex. 1010,[20] 6:18-19.) The '724 provisional application further discloses that the VLSI layouts of networks are included "on a semiconductor chip" such as a Field Programmable Gate Array (FPGA), and a POSITA would have understood such a semiconductor chip to be a non-transitory

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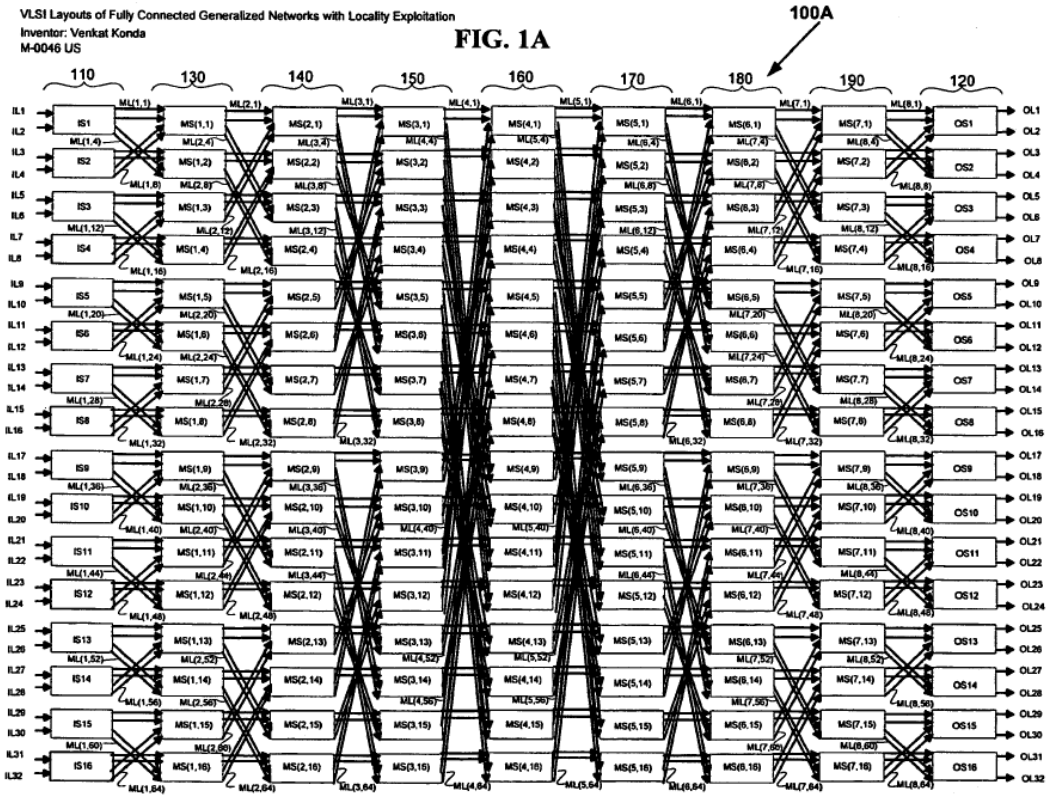
'724 provisional application with other disclosure within *Konda '756 PCT*. (*See infra* Sections XII.A-B.)

[20] Petitioner cites to the disclosure of the '724 provisional application (Ex. 1010), which was incorporated by reference and thus included in *Konda '756 PCT*.

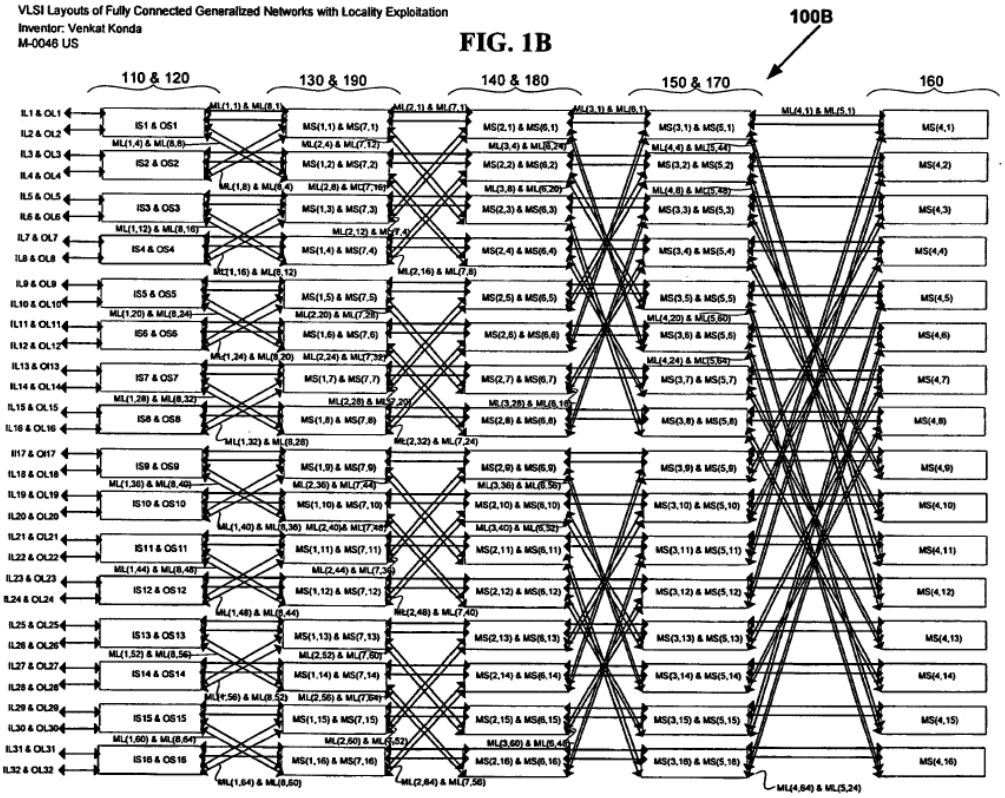
medium. (*Id.*, 7:1-9.) Therefore, *Konda '756 PCT* discloses a network implemented as part of a semiconductor chip ("network implemented in a non-transitory medium"). (Ex. 1002, ¶88.)

Figure 1A of the '724 provisional application illustrates an "exemplary generalized multi-link multi-stage network . . . with nine stages of one hundred forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configuration logic blocks." (Ex. 1010, 9:10-14.)



(Ex. 1010, FIG. 1A; Ex. 1002, ¶89.)

The ’724 provisional application discloses that connections are set up “between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190.” (Ex. 1010, 9:13-15.) The ’724 provisional application further discloses that figure 1B, replicated below, is a folded version of the network shown in figure 1A. (*Id.*, 2:17-18, 15:15-16.)



(Ex. 1010, FIG. 1B; Ex. 1002, ¶90.)

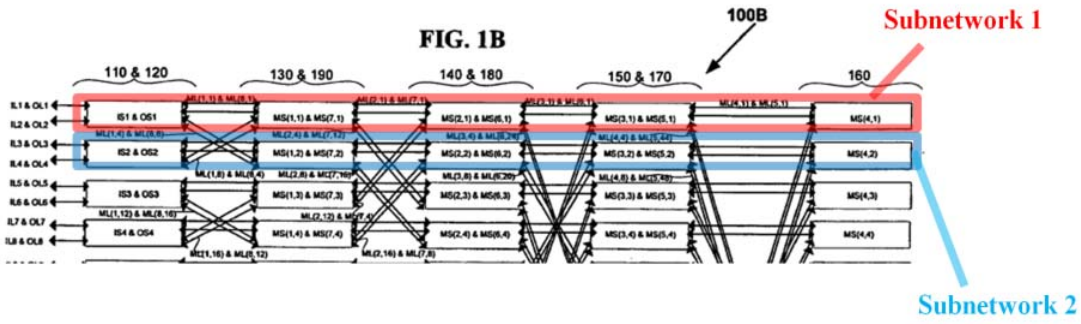
Accordingly, a POSITA would have readily understood that much of the description regarding the network of figure 1A in the ’724 provisional application is also applicable to figure 1B of the ’724 provisional application as it is simply a

folded version of the network in figure 1A. (Ex. 1010, 15:15-22.) The network shown in figure 1B of the '724 provisional application, which can be included on a FPGA integrated circuit, is "a network implemented in a non-transitory medium," as claimed. (*Id.*, 7:1-9; Ex. 1002, ¶91.)

b) "a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links, and"

(1) a plurality of subnetworks

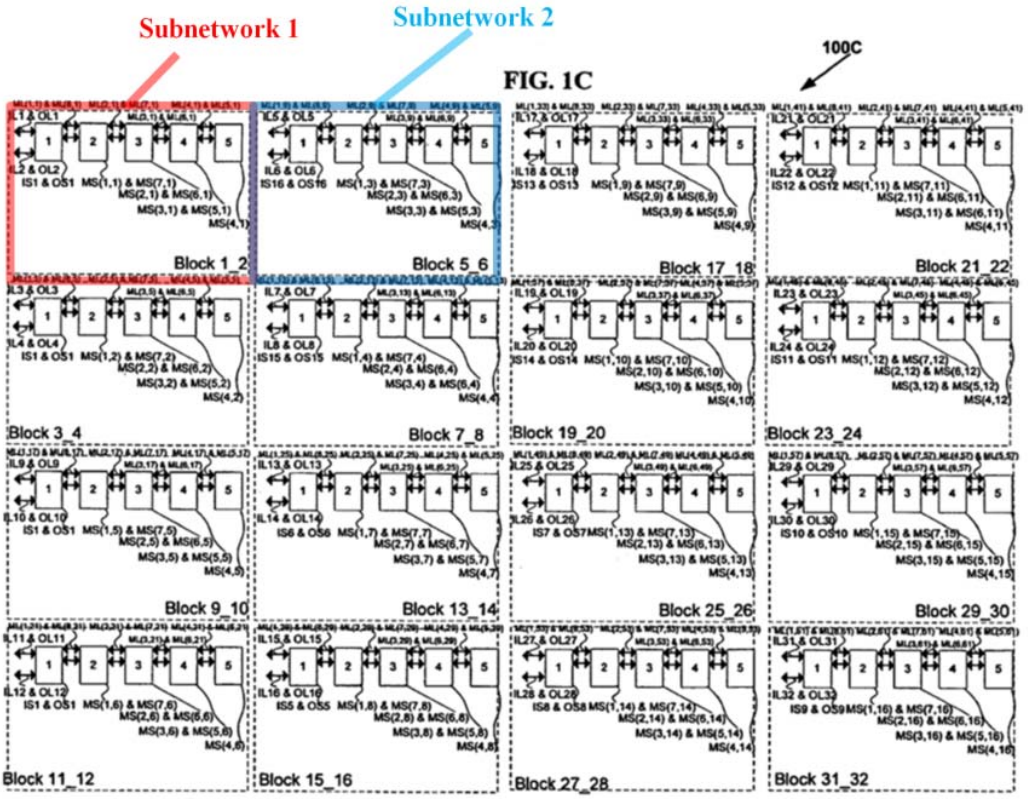
Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses a plurality of subnetworks. (Ex. 1002, ¶¶92-94.) The '724 provisional application discloses that the network shown in figure 1B includes a plurality of subnetworks.



(Ex 1010, FIG. 1B (excerpt, annotated to show a plurality of subnetworks); Ex. 1002, ¶92.)

According to the '724 provisional application, the layout shown in figure 1C below includes 16 blocks, where "[e]ach block implements all the switches in one

row of the network 100B of FIG. 1B, one of the key aspects of the current invention." (Ex. 1010, 17:15-20.)



(*Id.*, FIG. 1C (annotated to show a plurality of subnetworks); Ex. 1002, ¶93.)

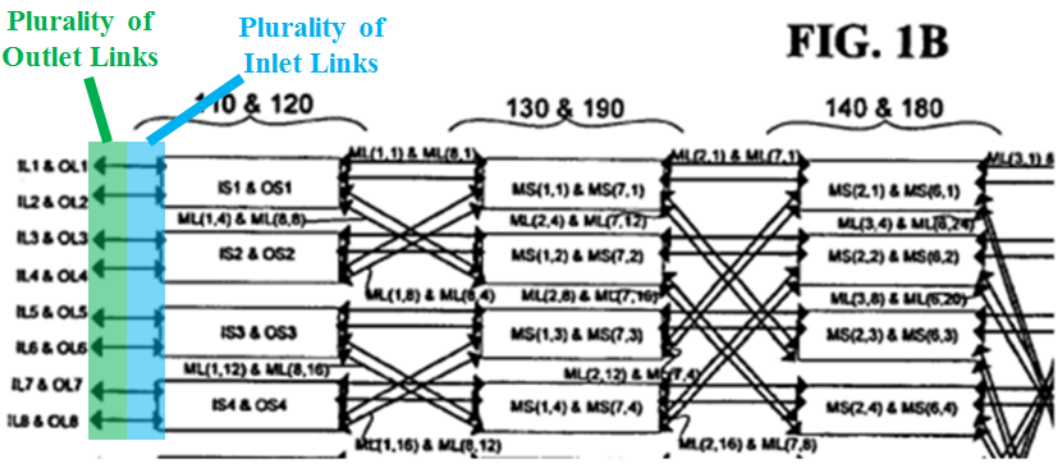
Therefore, each of the "blocks" shown in figure 1C of the '724 provisional application corresponds to a row of switches in one row of the network illustrated in figure 1B. (Ex. 1010, 17:15-20.) Each row of switches corresponds to a portion of the network and would have been understood to constitute a "subnetwork." (Ex. 1002, ¶94.) Because the network in figure 1B includes 16 rows of switches, it includes 16 subnetworks, each of which is illustrated as a "block" in figure 1C.

(Ex. 1010, FIGs. 1B, 1C.) Therefore, the '724 provisional application discloses that the network of figure 1B includes a plurality of subnetworks. (Ex. 1002, ¶94.)

(2) a plurality of inlet links and a plurality of outlet links

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses a plurality of inlet links and a plurality of outlet links. (Ex. 1002, ¶¶95-104.) For example, the excerpt of figure 1B of the '724 provisional application below show inlet links (IL1, IL2, … IL8) and outlet links (OL1, OL2, … OL8), where, for example, the inlet links IL1 and IL2 are connected to the inputs of switch IS1 & OS1, and outlet links OL1 and OL2 are connected to the outputs of switch IS1 & OS1. (Ex. 1010, 15:15-22, 28:20-35, FIG. 1B; Ex. 1002, ¶95.)

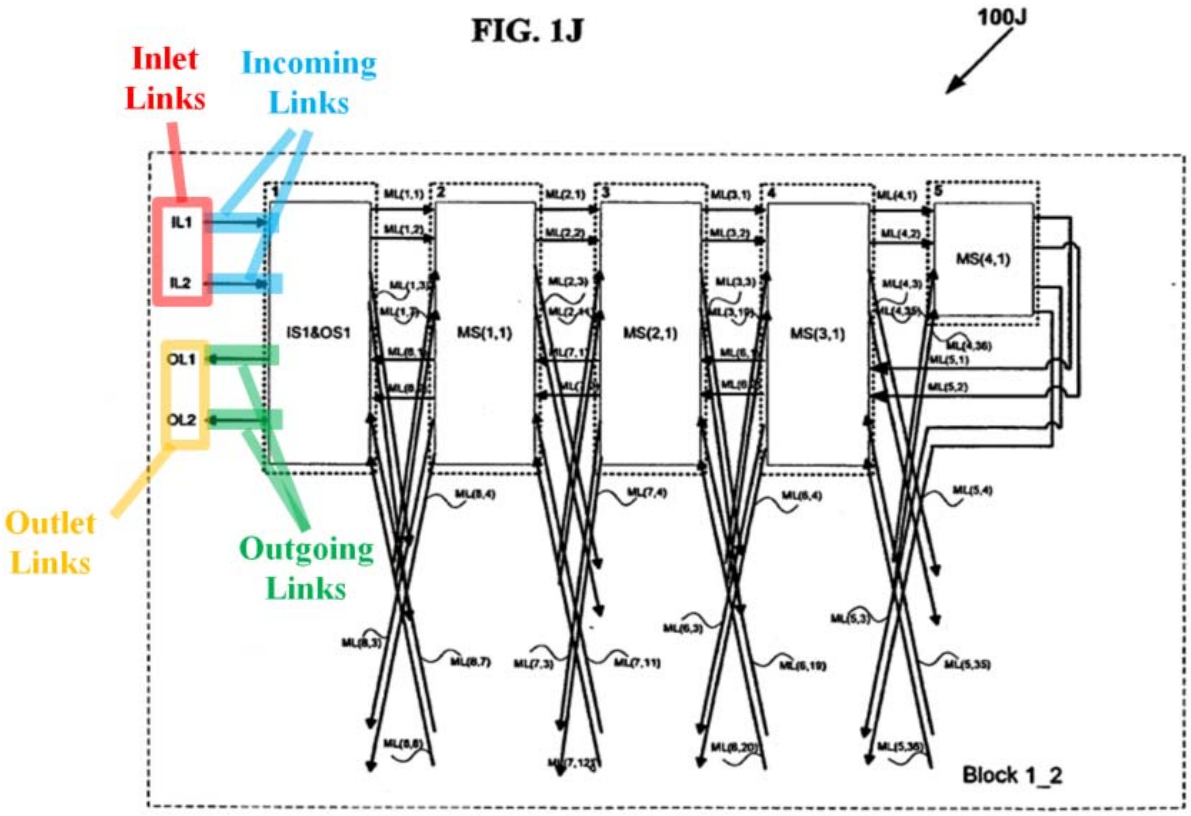
In particular, the '724 provisional application discloses that the subnetworks include inputs ("plurality of inlet links") (highlighted in blue below) that are coupled to inputs of the switches in the first stage of the network. The '724 provisional application also discloses that the subnetworks include outputs ("plurality of outlet links") (highlighted in green below) that are coupled to outputs of the switches in the first stage of the network. (Ex. 1002, ¶96.)



(Ex. 1010, FIG. 1B (excerpt, annotated to show inlet links and outlet links); Ex. 1002, ¶96.)

A POSITA would have understood that each double-ended arrow represents two links, which is evident from comparing figures 1A and 1B as the labeling of each double-ended arrow includes two labels in figure 1B (one for each link) whereas the single-ended arrows in figure 1A only have one label. (Ex. 1010, 1A, 1B; Ex. 1002, ¶97.) Moreover, the '724 provisional confirms that each of the double-ended arrow links can be implemented as "two different tracks" (i.e., different "links"." (Ex. 1002, ¶¶97-98.) Such an understanding is confirmed by annotated figure 1J below, which shows the inlet links (red) connected to the incoming links (blue) of the switch IS1&OS1 in the subnetwork corresponding to the top row of figure 1B (block 1_2) as well as the outlet links (orange) connected

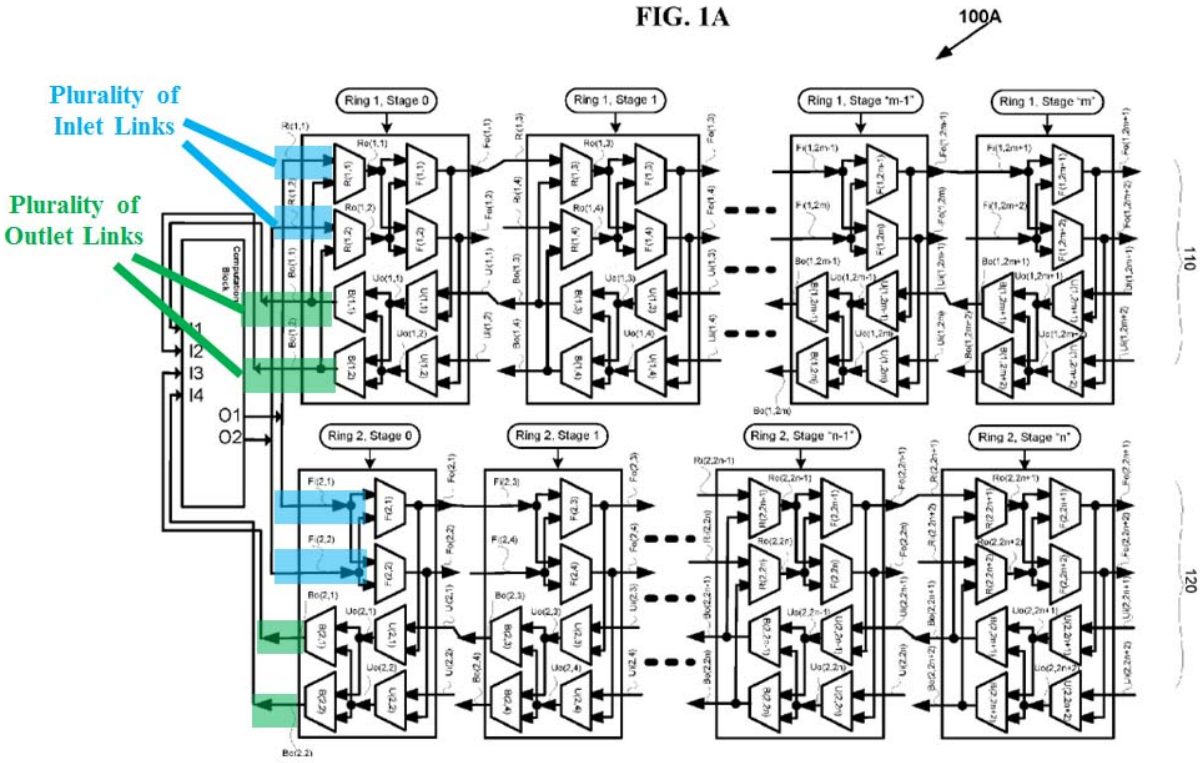
to the outgoing links (green) of the switch IS1&OS1, which is the top-left switch shown above in the annotated excerpt of figure 1B. (Ex. 1010, 28:14-26, 29:4-10; Ex. 1002, ¶97.)



(Ex. 1010, FIG. 1J (annotated); Ex. 1002, ¶97.)

Indeed, the inlet links and outlet links shown above for the '724 provisional application are consistent with the disclosure of the '553 patent, which discloses that the outlet links correspond to the outputs of the blocks and the inlet links correspond to the inputs of the blocks. (Ex. 1001, 9:4-26, FIG. 1A; Ex. 1002, ¶99.)

FIG. 1A

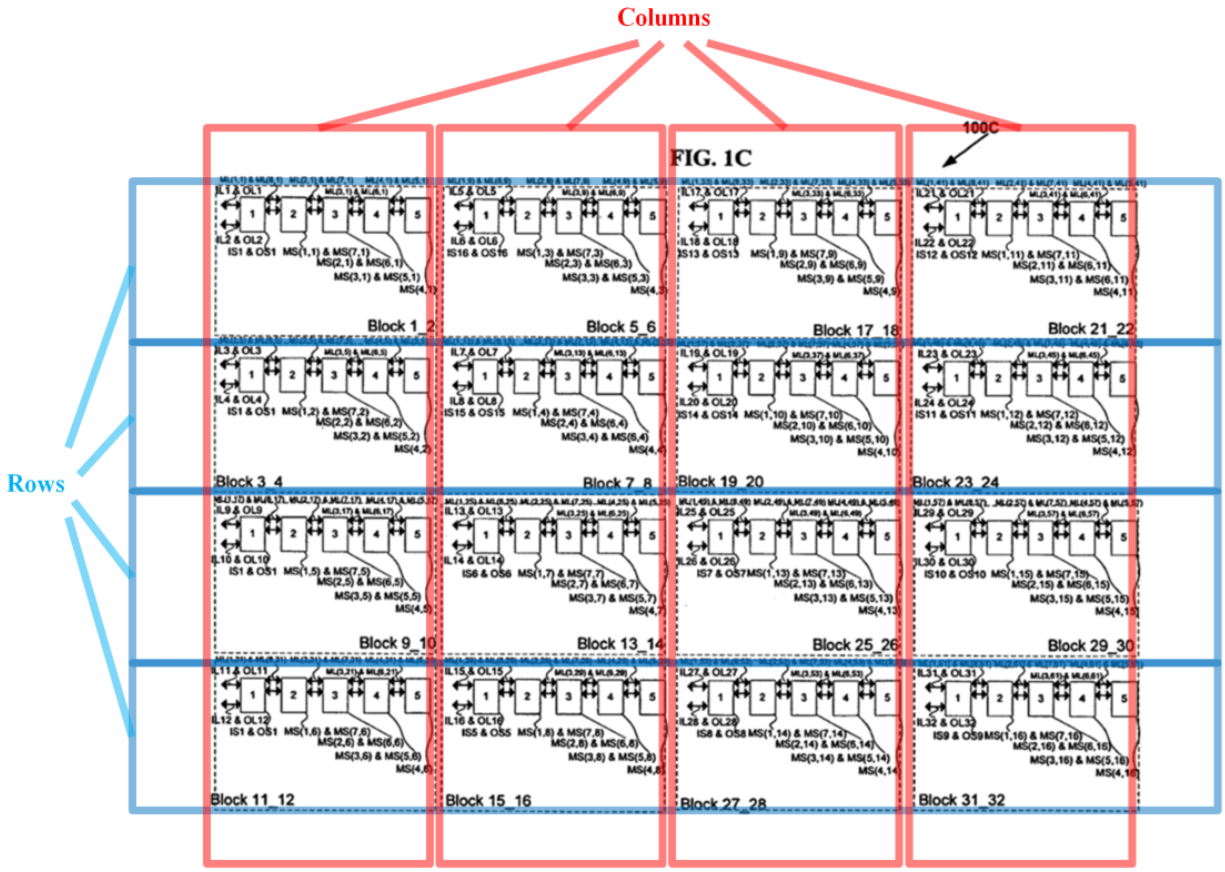


(Ex. 1001, FIG. 1A (annotated to show inlet links (blue) and outlet links (green); Ex. 1002, ¶99.)

c) "said plurality of subnetworks arranged in a two-dimensional grid of rows and columns; and"

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses said plurality of subnetworks arranged in a two-dimensional grid of rows and columns. (Ex. 1002, ¶¶103-104.) For example, figure 1C of the '724 provisional application, which is a layout of the network shown in figure 1B,

shows the "plurality of subnetworks arranged in a two-dimensional grid of rows and columns." (Ex. 1010, 2:22-24, FIG. 1C; Ex. 1002, ¶103.)



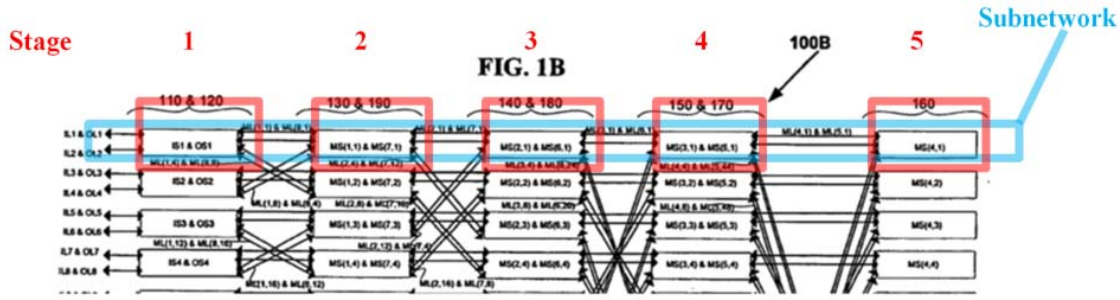
(Ex. 1010, FIG. 1C; Ex. 1002, ¶103.)

The '724 provisional application explicitly describes the subnetworks or "blocks" in figure 1C as being in rows and columns. (Ex. 1010, 20:19-22 ("Similarly the bandwidth provided between Block 1_2 and block 7_8 is also 2's BW since corresponding rows (formed by Block 1_2 and Block 5_6; and by Block

3_4 and Block 7_8) and columns (formed by Block 1_2 and Block 3_4; and by Block 5_6 and Block 7_8) offer 2's BW."); Ex. 1002, ¶104.)

d) "each subnetwork comprising y stages, where y ≥ 1; and"

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses each subnetwork comprising y stages, where y ≥ 1. (Ex. 1002, ¶105.) For example, in figure 1B the '724 provisional application, each subnetwork includes 5 stages, and therefore *Konda '756 PCT* discloses "each subnetwork comprising y stages, where y ≥ 1." The '724 provisional application states that figure 1B is a diagram of the "equivalent symmetrical folded" network shown in figure 1A with five stages. (Ex. 1010, 2:17-19.) The annotated excerpt of figure 1B of the '724 provisional application below shows each of the stages in the subnetwork corresponding to the top row of the network.



(*Id*., FIG. 1B (excerpt, annotated); Ex. 1002, ¶105.)

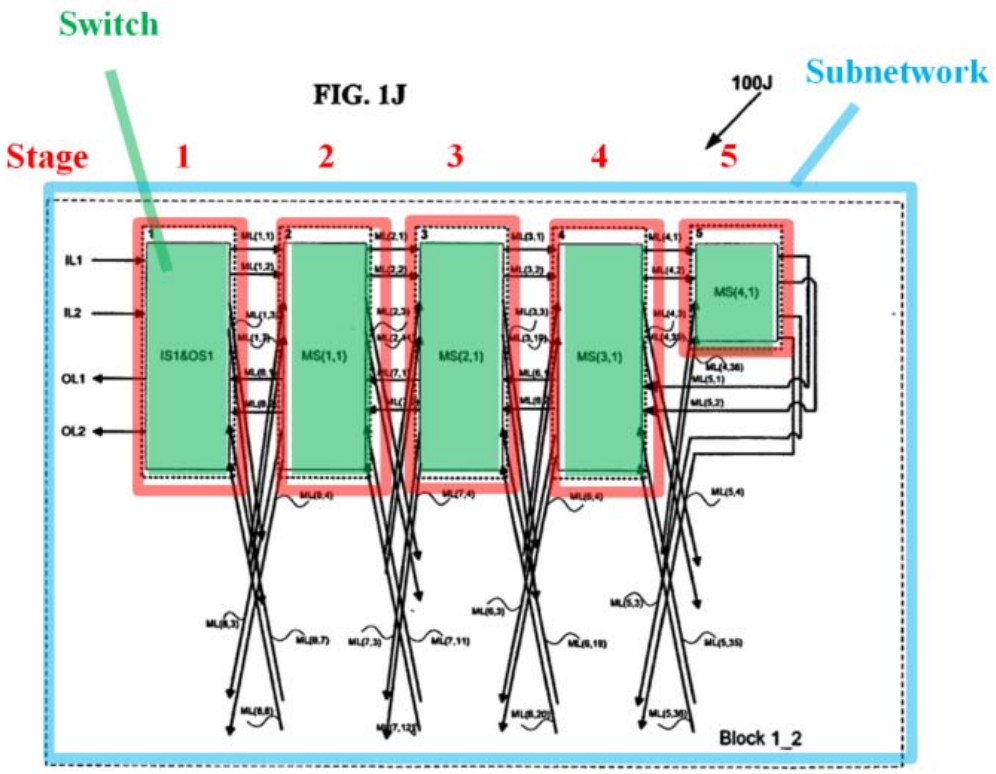
e) "each stage comprising a switch of size d_i x d_o, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size d_i x d_o having d_i incoming links and d_o outgoing links; and"

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses this claim element. (Ex. 1002, ¶¶106-110.) As an initial matter, a POSITA would have understood this claim element to require that each stage includes a switch that has at least two incoming links and at least two outgoing links (e.g., at least a 2x2 switch with at least two inputs and two outputs). This is because in the relevant art of integrated circuits, "a switch of size d_i x d_o" in the context of "where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size d_i x d_o having d_i incoming links and d_o outgoing links" would have informed a POSITA about the input/output configuration of the switch, and not the actual area (i.e., physical size) of the switch. (*Id*., ¶106.) As explained below, the '724 provisional application discloses that each stage of the network illustrated in figure 1B includes a switch that is at least a 2x2 switch. Therefore, *Konda '756 PCT* discloses this claim element.

For example, the '724 provisional application states with respect to the network of figure 1A, which is folded to produce the network of figure 1B, that figure 1A has "nine stages of one hundred and forty four switches." (Ex. 1010, 9:10-12.) The '724 provisional application further states with respect to figure 1A

that "input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16" and that all the middle stages consist of sixteen, four by four switches. (*Id.*, 9:15-24; Ex. 1002, ¶107.)

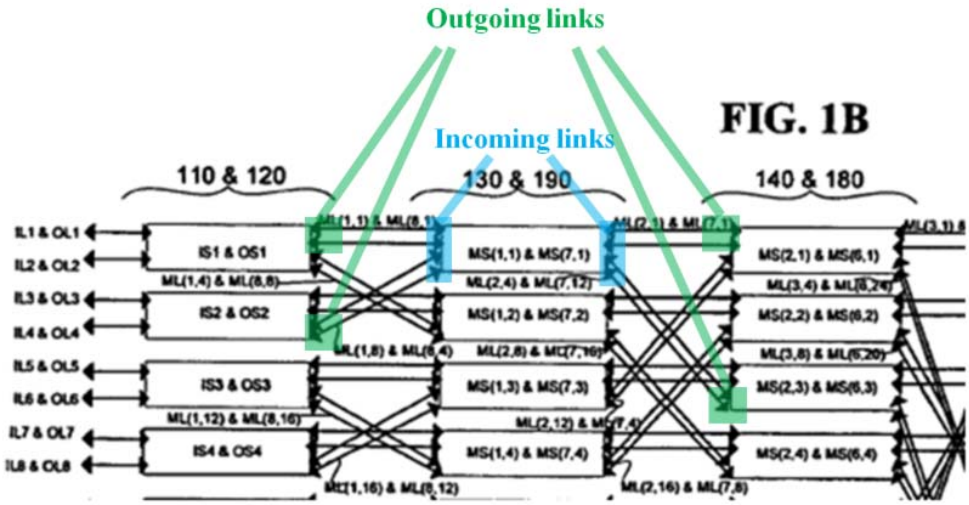
Moreover, *Konda '756 PCT* discloses other variations on the embodiment shown in figure 1B where the sets of switches described with respect to figure 1A are combined to form larger 8x8 and 6x6 switches that are used to implement the switches for the different stages in the network. (Ex. 1010, 28:14-26, 29:4-10.) For example, the '724 provisional application discloses that the switches for the stages in figure 1B can be combined switches as shown in annotated figure 1J below, where the combined input and output switches (e.g. IS1&OS1 corresponding to stage 1) form a 6x6 switch and the middle switches (e.g. MS1,1) are each implemented as an 8x8 switch. (*Id.*; *see also id.*, 29:20-28; Ex. 1002, ¶108.)



(Ex. 1010, FIG. 1J (annotated); Ex. 1002, ¶108.)

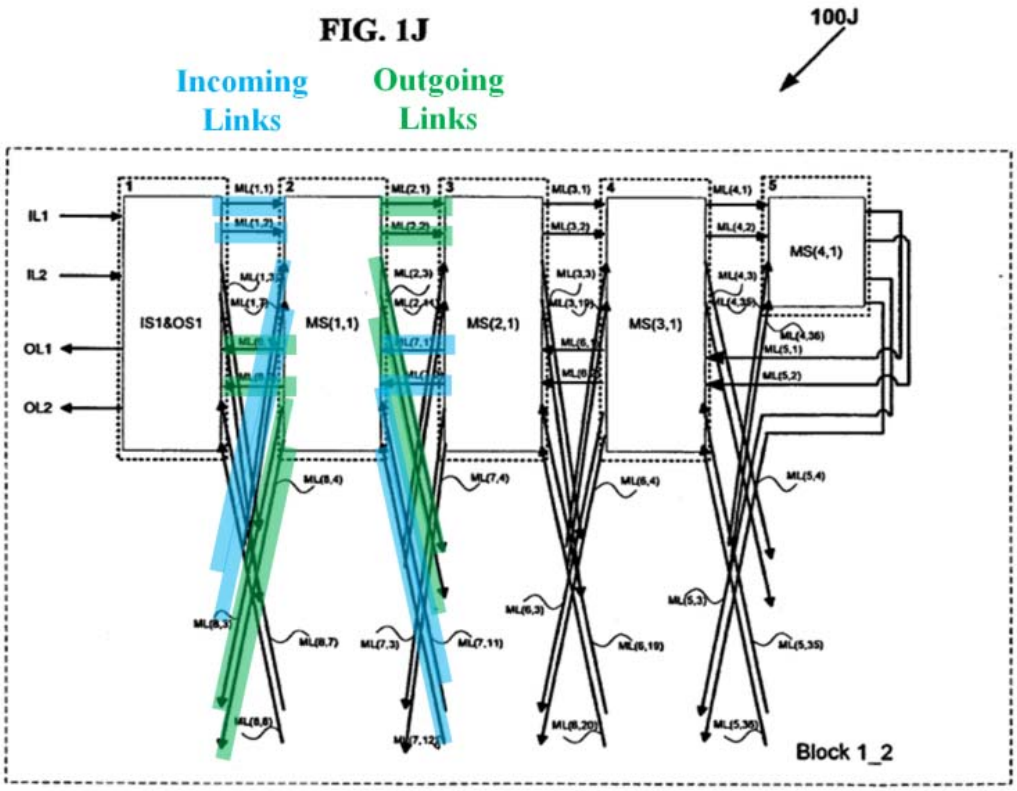
For at least these reasons, *Konda '756 PCT* discloses "each stage comprising a switch of size d_i x d_o, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size d_i x d_o having d_i incoming links and d_o outgoing links." (Ex. 1002, ¶109.)

As shown in the annotated excerpt of figure 1B below, the switch for each stage includes incoming links (blue) corresponding to arrows going into the switch and outgoing links (green) corresponding to arrows going away from the switch. As noted above with respect to claim feature 1[b](2), each double-ended arrow represents two links. (*See supra* Section XII.A.1(b)(2); Ex. 1002, ¶110.)



(Ex. 1010, FIG. 1B (excerpt annotated to show incoming links (blue) and outgoing links (green) for stage 2); Ex. 1002, ¶110.)

The same links highlighted in the annotated excerpt of figure 1B above are also depicted in figure 1J and are highlighted in annotated figure 1J below. In annotated figure 1J below, the incoming links are highlighted in blue and the outgoing links are highlighted in green for the switch MS(1,1) included in stage 2 of the subnetwork corresponding to block 1_2.

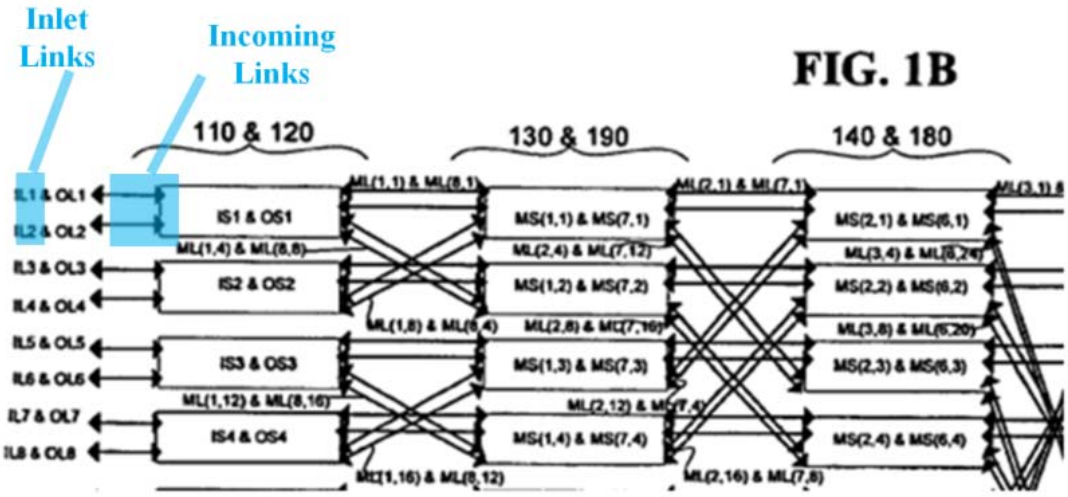


(Ex. 1010, 1J (annotated); Ex. 1002, ¶110.)

f) "Said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork; and"

To the extent this claim element can be understood by a POSITA, *Konda '756 PCT*, by way of its incorporation of the '724 provisional application, discloses this claim element. (Ex. 1002, ¶¶111-116.) For example, in the '724 provisional application, the inlet links correspond to the inputs to the subnetworks

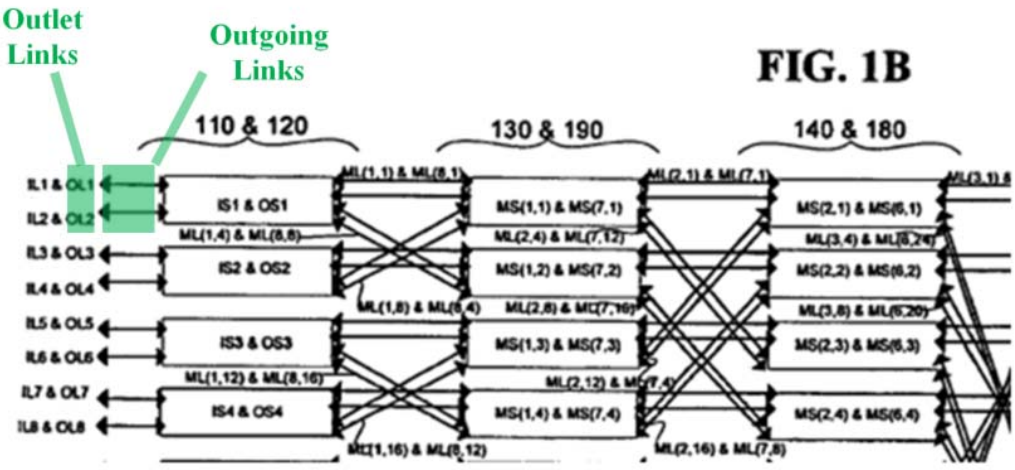
and the outlet links correspond to the outputs of the subnetworks. (*Id*., ¶¶111-112; *see supra* Section XII.A.1(b)(2).) As shown in the annotated excerpts of figure 1B below, the labeled incoming links and outgoing links corresponding to the first stage of the network also correspond to the inlet links and outlet links of the subnetworks. (Ex. 1010, FIGs. 1B, 1J.) For example, as depicted in the annotated excerpt of figure 1B below, the inlet links IL1 and IL2 are each connected to one of the incoming links of one of the switches in stage 1 of the subnetwork corresponding to the top row. (Ex. 1010, 10:11-14, 15:15-22, 29:20-23, FIGs. 1B, 1J.)



(*Id*., FIG. 1B (excerpt, annotated); Ex. 1002, ¶113.)

Similarly, as depicted in the annotated excerpt of figure 1B below, the outlet links OL1 and OL2 are each connected to one of the outgoing links of one of the

switches in stage 1 of the subnetwork corresponding to the top row. (Ex. 1010, 10:11-14, 15:15-22, 29:20-23, FIGs. 1B, 1J; Ex. 1002, ¶114.)



(Ex. 1010, FIG. 1B (excerpt, annotated); Ex. 1002, ¶¶114-116 (also explaining that figure 1J confirms this understanding of *Konda '756 PCT*.)

As demonstrated above, in the embodiment shown in figure 1B of the '724 provisional application, each inlet link in the plurality of inlet links is coupled to an incoming link of a switch in the first stage of a subnetwork, and each outlet link in the plurality of outlet links is coupled to an outgoing link of a switch in the first stage of a subnetwork. (Ex. 1002, ¶¶111-116.) Therefore, to the extent this claim feature can be understood, *Konda '756 PCT* discloses "said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork." (*Id*.)

g) "each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said inlet links and may or may not be comprising the same number of said outlet links; each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said stages; each stage may or may not be comprising the same number of switches; and each switch in each stage may or may not be of the same size, each multiplexer in each stage may or may not be of the same size and"

Konda '756 PCT discloses this claim element. (Ex 1002, ¶¶117-122.) As an initial matter, this entire claim element does not further limit claim 1 because it simply recites several optional features. *MPHJ Tech. Invs., LLC v. Ricoh Ams. Corp.*, 847 F.3d 1363, 1379 (Fed. Cir. 2017) ("As a matter of linguistic precision, optional elements do not narrow the claim because they can always be omitted."), citing to *In re Johnston*, 435 F.3d 1381, 1384 (Fed. Cir. 2006). As discussed separately below, since each subpart of claim element 1[g] imposes an optional "may or may not be" element onto the network components such as number of inlet/outlet links, number of stages, number of switches, etc., *Konda '756 PCT* discloses claim element 1[g] regardless of the optional features imposed thereon. (Ex. 1002, ¶¶117-122.)

(1) each subnetwork of the plurality of subnetworks *may or may not be comprising* the same number of said inlet links and *may or may not be comprising* the same number of said outlet links;

For instance, *Konda '756 PCT* discloses claim element 1[g](1) as long as it discloses that each subnetwork of the plurality of subnetworks has some inlet links and some outlet links, since the claim does not require that each of the subnetworks have the "same number" of inlet and/or outlet links. (Ex. 1002, ¶118.) And since it has already been shown above that each subnetwork includes inlet and outlet links, *Konda '756 PCT* discloses this claim element. (*Supra* Section XII.A.1(b)(2).)

(2) each subnetwork of the plurality of subnetworks *may or may not be comprising* the same number of said stages;

Similarly, *Konda '756 PCT* discloses claim element 1[g](2) as long as it discloses that each subnetwork has a stage, since the claim does not require that each subnetwork have the "same number" of stages. (Ex. 1002, ¶119.) And since it has already been shown above that each subnetwork includes a stage, *Konda '756 PCT* discloses this claim element. (*Supra* Section XII.A.1(d).)

(3) each stage *may or may not be comprising* the same number of switches; and

Similarly, *Konda '756 PCT* discloses claim element 1[g](3) as long as it discloses that each stage has a switch, since the claim does not require that each stage have the "same number" of switches. (Ex. 1002, ¶120.) And since it has already been shown above that each stage includes a switch, *Konda '756 PCT* discloses this claim element. (*Supra* Section XII.A.1(e).)

(4) each switch in each stage *may or may not be* of the same size,

Similarly, *Konda '756 PCT* discloses claim element 1[g](4) as long as it discloses a switch in each stage, since the claim does not require that each switch have the "same size." (Ex. 1002, ¶121.) And since it has already been shown above that *Konda '756 PCT* discloses a switch in each stage, *Konda '756 PCT* discloses this claim element. (*Supra* Section XII.A.1(e).)

(5) each multiplexer in each stage *may or may not be* of the same size.

With respect to claim element 1[g](5), there is no antecedent basis for "each multiplexer." To the extent the claim element can be understood, this claim feature does not require each stage to include a multiplexer because nowhere in claim 1 is it specified that each stage includes any multiplexers. Because claim 1 does not require each stage to include a multiplexer, *Konda '756 PCT* discloses this claim

feature whether or not it discloses each stage includes a multiplexer. For example, if there are no multiplexers in the stages, then "each multiplexer in each stage may or may not be of the same size" is true as no multiplexers are present and therefore the further condition applied to those non-existent multiplexers ("may or may not be of the same size") is also true. If there are multiplexers in each stage, then they are either "of the same size" or they are not, and the additional condition is also satisfied. For at least these reasons, *Konda '756 PCT* discloses claim element 1[g](5). (Ex. 1002, ¶122.)

> **h) "Said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork; and"**

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses this claim element. (Ex. 1002, ¶¶123-130.) As an initial matter, a POSITA would have understood this claim element to mean that the incoming and outgoing links (together) for each switch include a plurality of

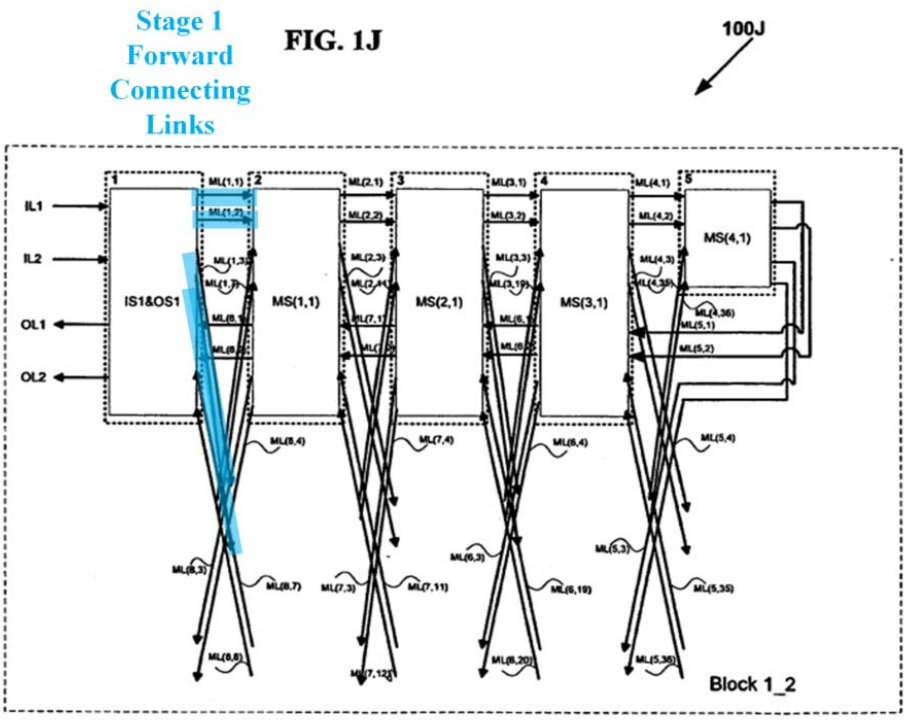
forward connecting links and a plurality of backward connecting links.[21] In other words, if a switch has one incoming link that is a forward connecting link and one outgoing link that is a forward connecting link, the claim feature of the incoming and outgoing links for the switch including a plurality of forward connecting links would be satisfied. (Ex. 1002, ¶123.) Similarly, if the switch has one incoming link that is a backward connecting link and one outgoing link that is a backward connecting link, the links for that switch would have been understood by a POSITA to include a plurality of backward connecting links. (*Id.*)

Such an interpretation of the claim is consistent with other portions of claim 1 and the recitations in independent claim 11. For example, claim elements 1[i]-1[j] recite what is included in the forward connecting links separately from what is included in the backward connecting links. (*See infra* Sections XII.A.1(i)-(j).) Similarly claim 11 separately recites "said incoming links comprising . . ." and "said outgoing links comprising . . ." (*See infra* Sections XII.A.10(h)-(i).) Thus, claim elements 1[i]-1[j] and claim 11 confirm that the incoming and outgoing links in claim 11 are being further characterized *individually*. In contrast, the subject

[21] The claim terms "forward connecting links" and "backward connecting links" are not used in the '553 patent outside of the claims.

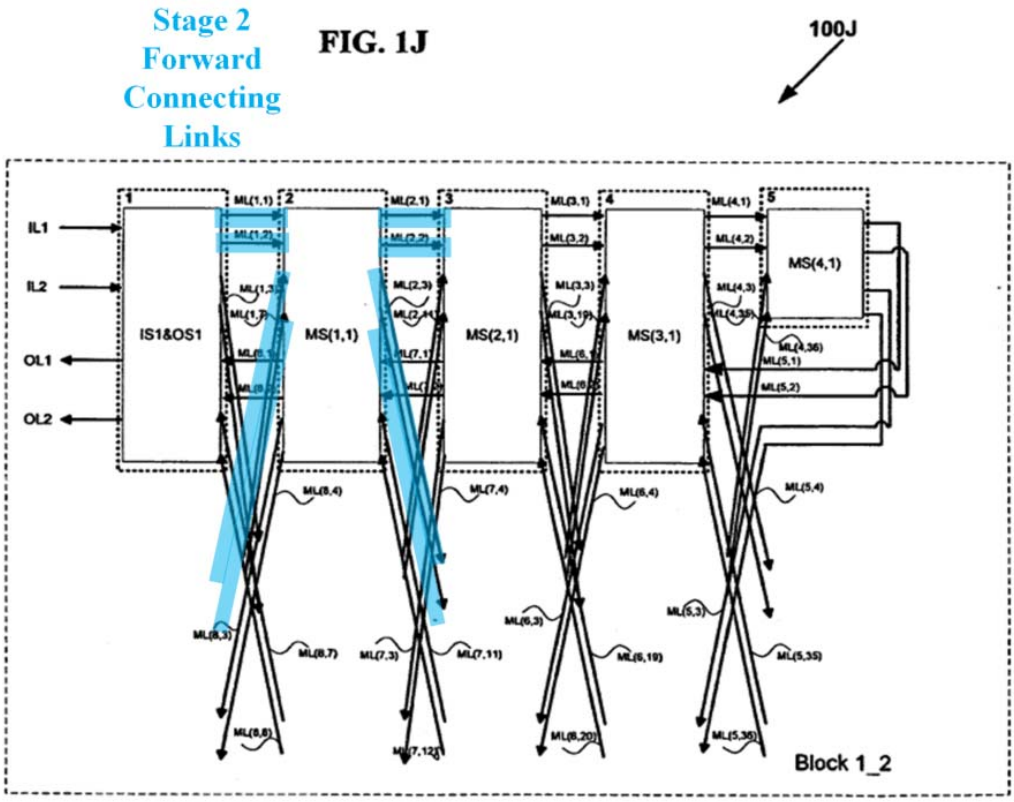
claim element 1[h] indicates the "incoming and outgoing links in each switch in each stage" taken together include a plurality of forward connecting links and a plurality of backward connecting links. (Ex. 1002, ¶124.)

Konda '756 PCT discloses the forward and backward connecting links as recited in claim element 1[h]. For example, as illustrated in figure 1J of the '724 provisional application, which depicts one of the subnetworks (block 1_2) included in the network of figure 1B, the incoming links and outgoing links for each switch of each stage include a plurality of forward connecting links.

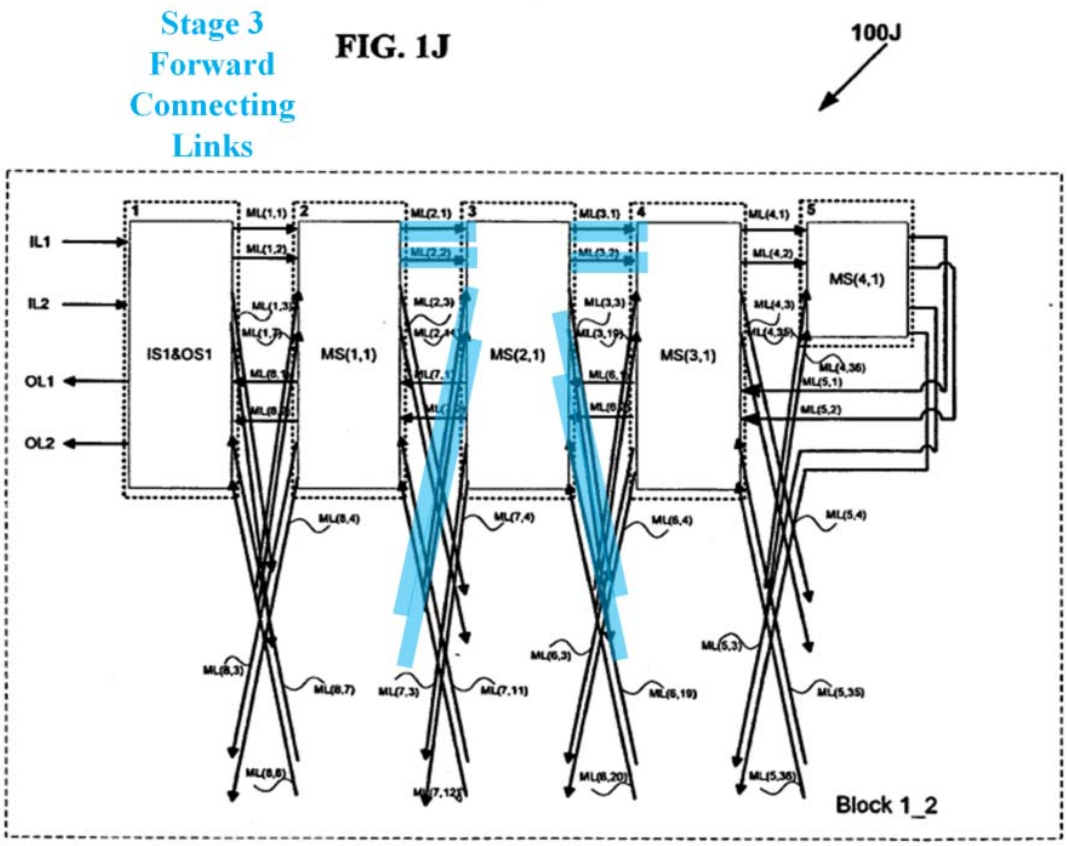


(Ex. 1010, FIG. 1J (annotated to show forward connecting links (blue) for stage 1 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶125.)

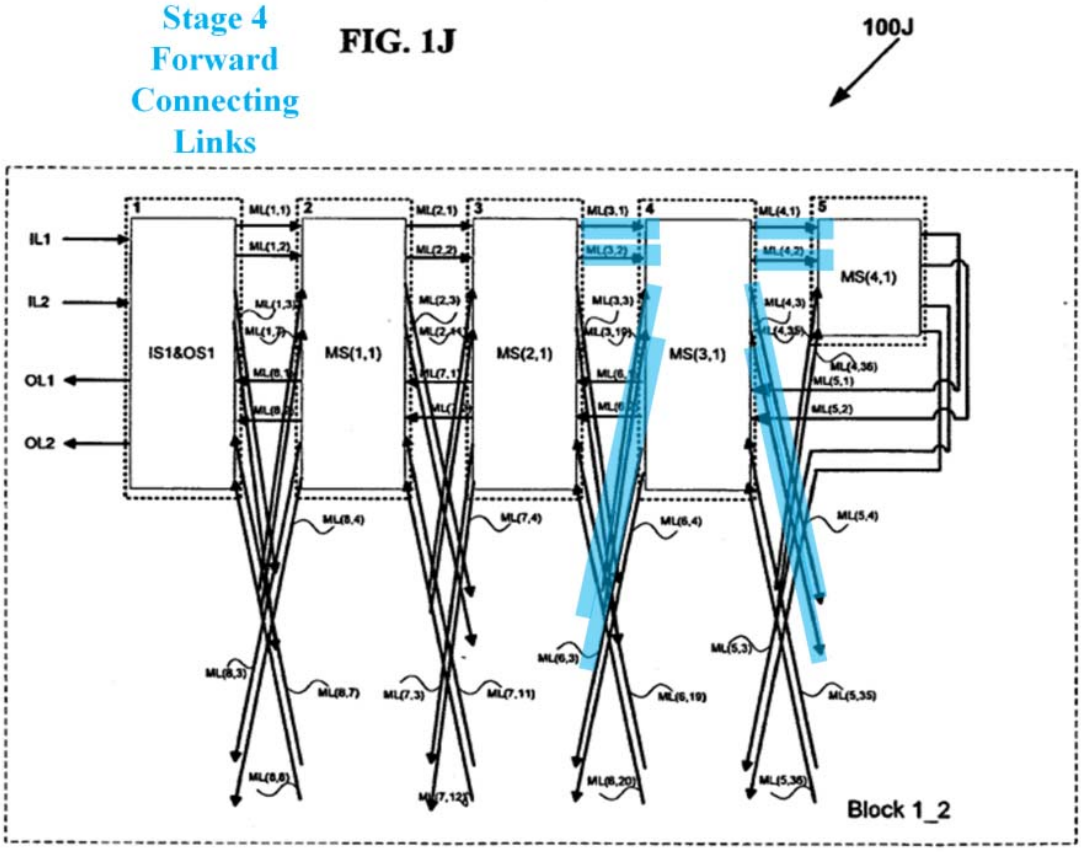
The forward connecting links shown in annotated figure 1J above are connected from a switch in stage 1 ("a stage") to switches in stage 2 in the same subnetwork (i.e., in the same row) or stage 2 in another subnetwork (i.e., in another row) ("another stage in same said subnetwork or another said subnetwork"). Similar annotated versions of figure 1J showing the forward connecting links for stages 2-5 are provided below.



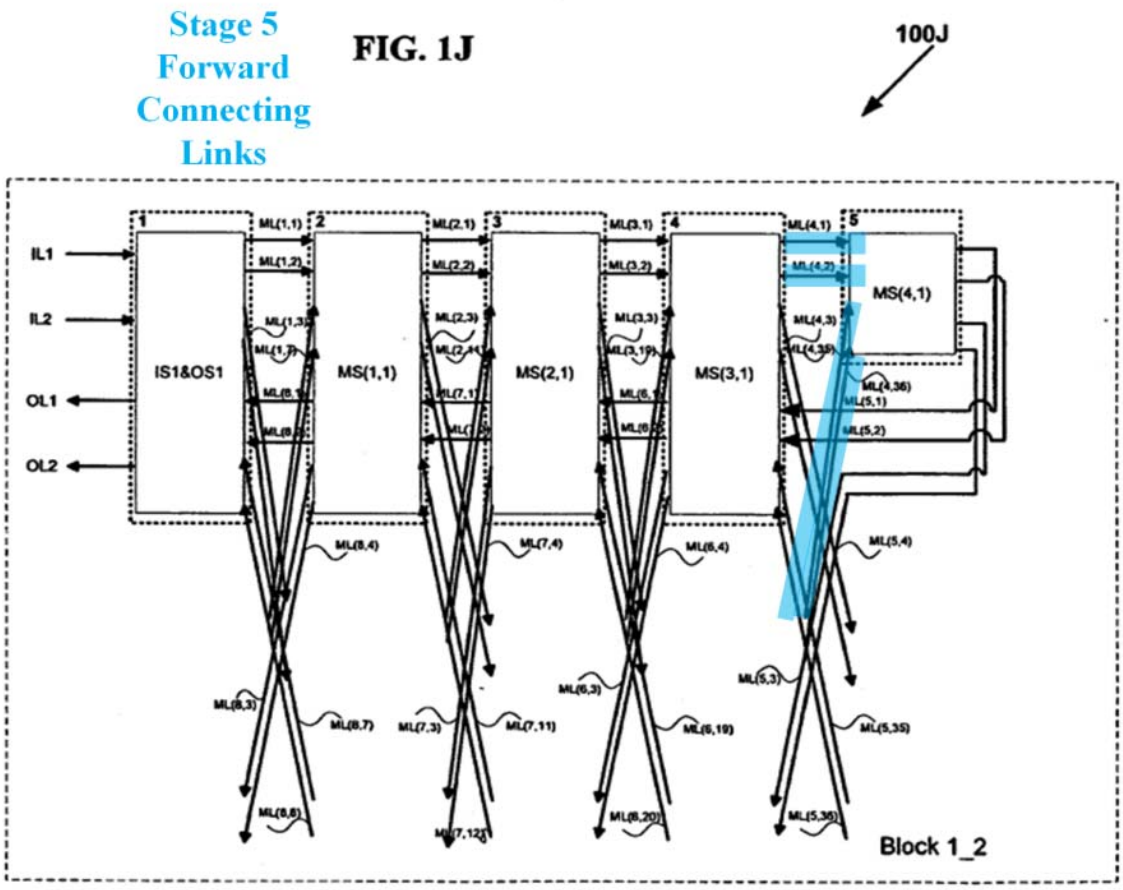
(Ex. 1010, FIG. 1J (annotated to show forward connecting links (blue) for stage 2 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶126.)



(Ex. 1010, FIG. 1J (annotated to show forward connecting links (blue) for stage 3 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶126.)



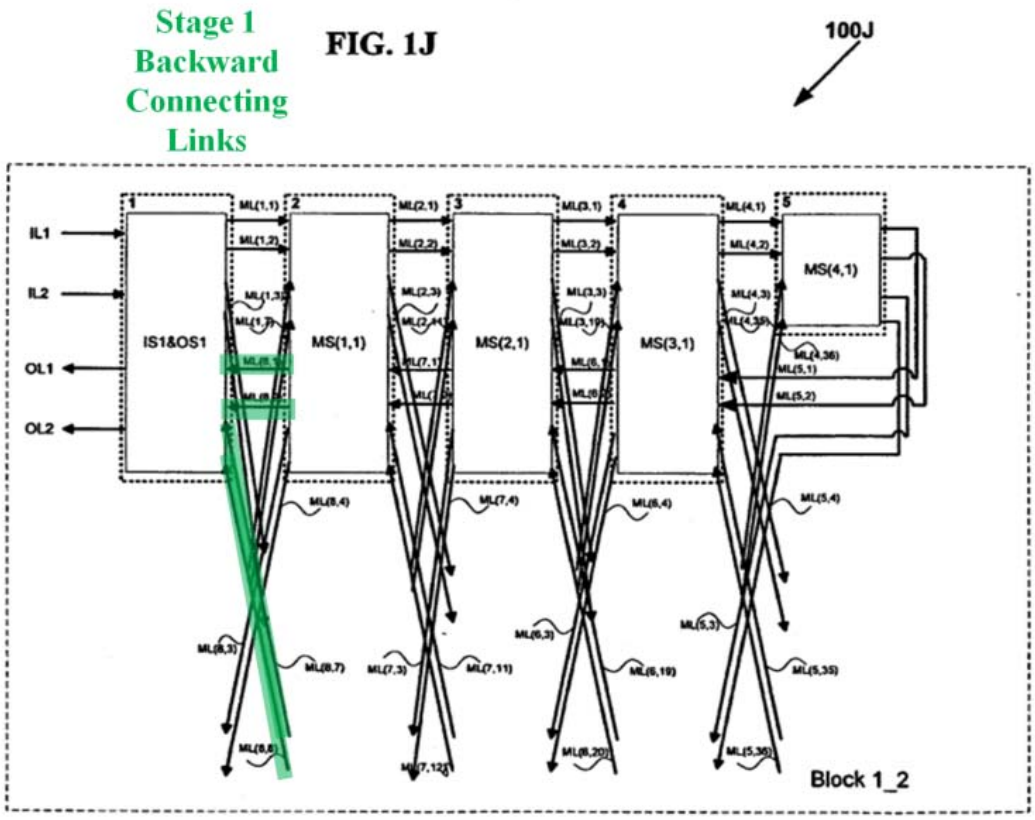
(Ex. 1010, FIG. 1J (annotated to show forward connecting links (blue) for stage 4 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶126.)



(Ex. 1010, FIG. 1J (annotated to show forward connecting links (blue) for stage 5 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶126)[22]

[22] While the annotated versions of figure 1J above highlight the forward connecting links for the switches in the stages of the top-most subnetwork in figure 1B, figure 1B itself shows that each of the switches in each of the stages in each of the

Konda '756 PCT also discloses the backward connecting links as recited in claim element 1[h]. For example, as illustrated in figure 1J of the '724 provisional application, which depicts one of the subnetworks (block 1_2) included in the network of figure 1B, the incoming links and outgoing links for each switch of each stage include a plurality of backward connecting links.



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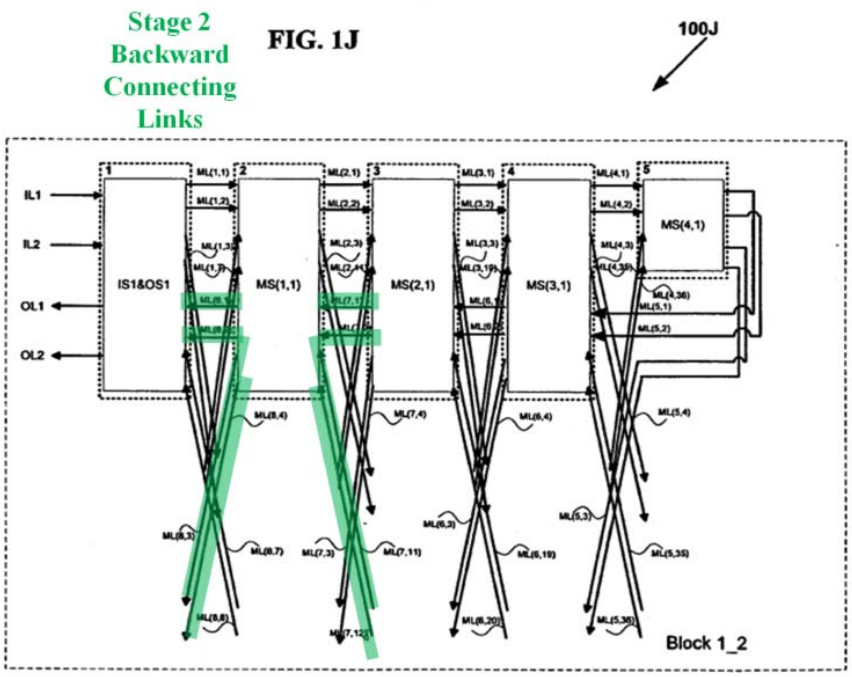
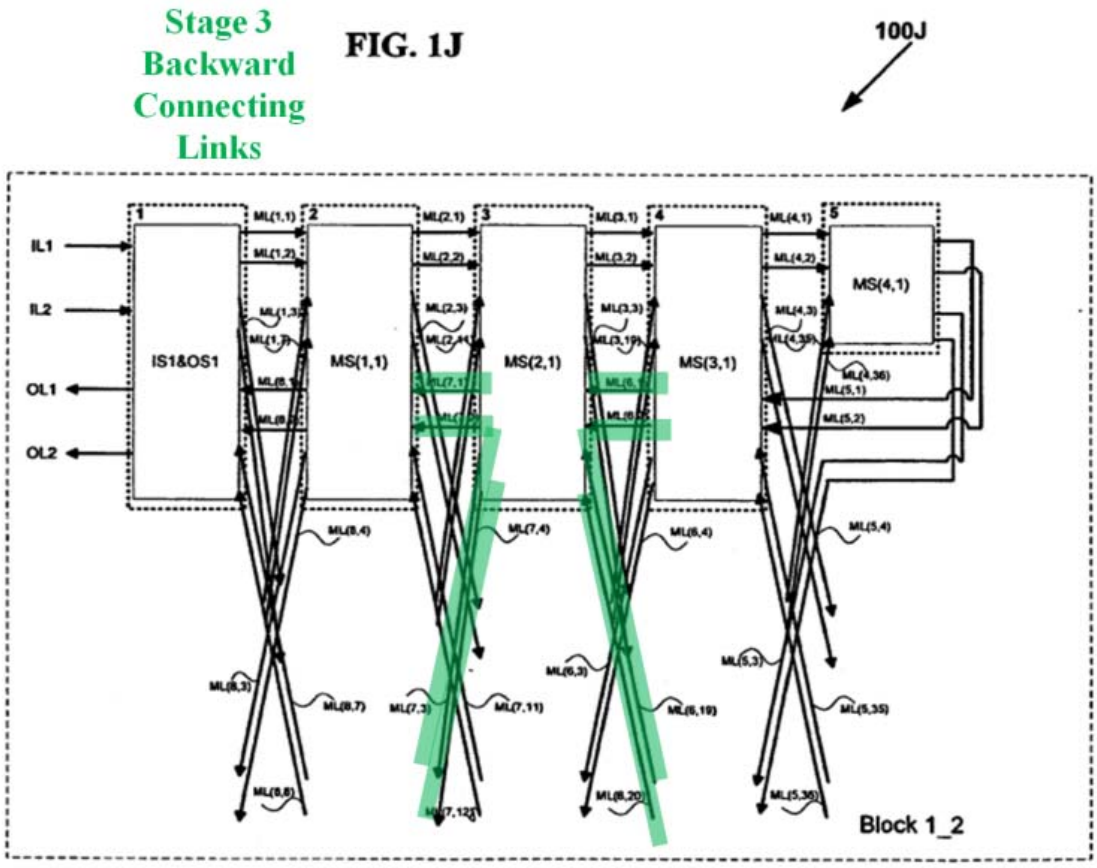
subnetworks illustrated includes a plurality of forward connecting links. (Ex. 1010, FIGs. 1B, 1J; Ex. 1002, ¶127.)

(Ex. 1010, FIG. 1J (annotated to show backward connecting links (green) for stage 1 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶128.)

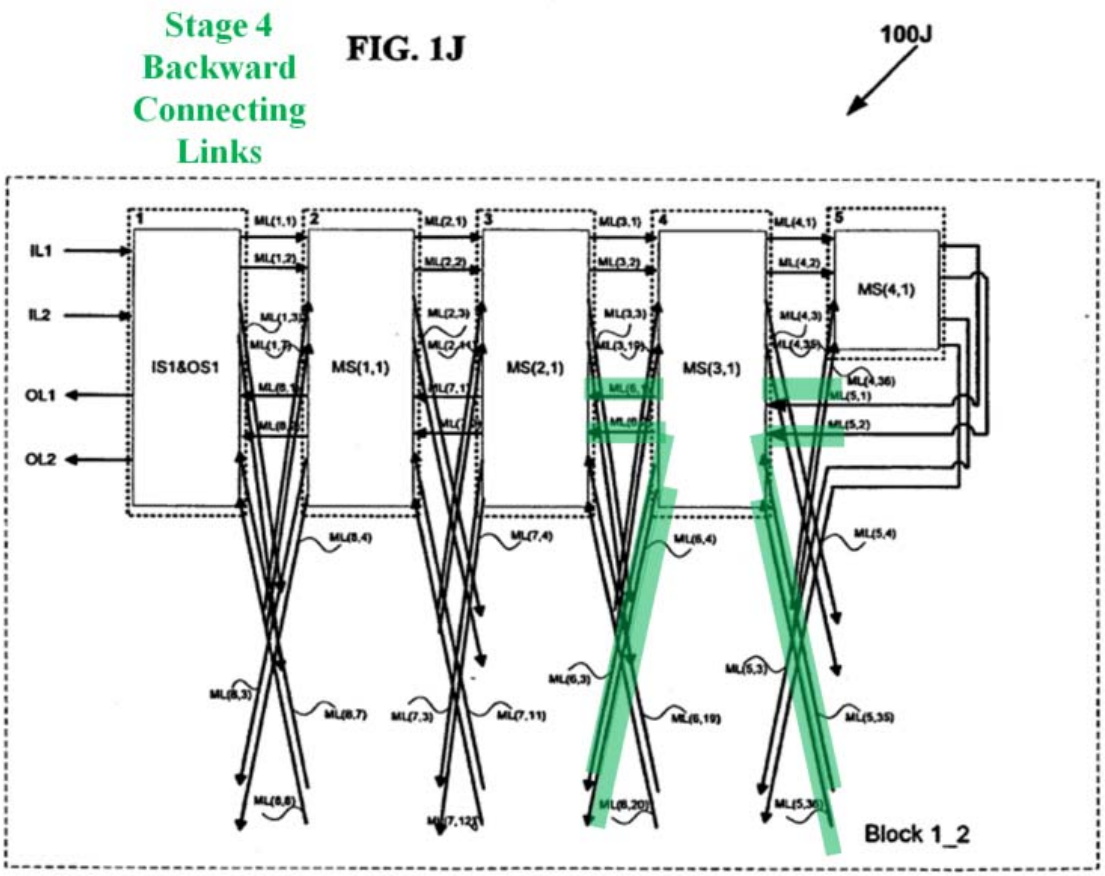
Each of the backward connecting links shown in annotated figure 1J above is connected from a switch in stage 2 ("a stage") to a switch in stage 1 ("another stage in same said subnetwork or another said subnetwork"). Similar annotated versions of figure 1J showing the backward connecting links for stages 2-5 are provided below.



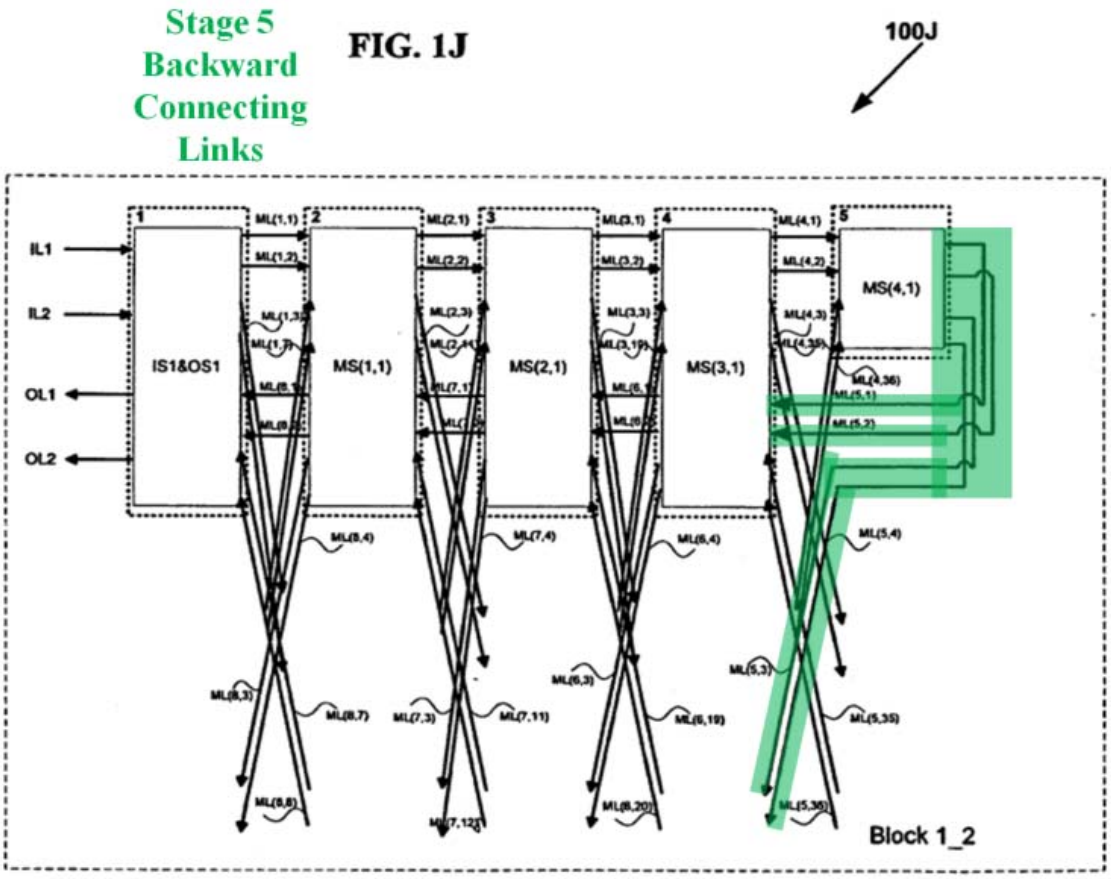
(Ex. 1010, FIG. 1J (annotated to show backward connecting links (green) for stage 2 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶129.)



(Ex. 1010, FIG. 1J (annotated to show backward connecting links (green) for stage 3 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶129.)



(Ex. 1010, FIG. 1J (annotated to show backward connecting links (green) for stage 4 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶129.)



(Ex. 1010, FIG. 1J (annotated to show backward connecting links (green) for stage 5 of the subnetwork corresponding to the top row of FIG. 1B); Ex. 1002, ¶129.)[23]

[23] While the annotated versions of figure 1J above highlight the backward connecting links for the switches in the stages of the top-most subnetwork in figure 1B, figure 1B itself shows that each of the switches in each of the stages in each of the subnetworks illustrated includes a plurality of backward connecting links. (Ex. 1010, FIGs. 1B, 1J; Ex. 1002, ¶130.)

i) "Said forward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks, and"

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses this claim element. (Ex. 1002, ¶¶131-132.) As an initial matter, this claim element does not further limit claim 1 because it simply recites several optional features. *MPHJ Tech. Invs., LLC*, 847 F.3d at 1379; *In re Johnston*, 435 F.3d at 1384. For example, claim 1 requires "*zero or more* cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks."[24] Since each subpart of claim element 1[i] imposes an optional "zero or more" feature onto the network

[24] For convenience, "cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in on or more other subnetworks" are referred to as "same-stage" cross links. In addition to same-stage cross links, claim 11 also recites "cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks," which are referred to as "inter-stage cross links."

components (e.g. forward connecting links including "zero or more" straight links and cross links), *Konda '756 PCT* discloses claim element 1[i] regardless of the optional features imposed thereon. (Ex. 1002, ¶¶131-132.) In other words, because *Konda '756 PCT* discloses forward connecting links as discussed above (*supra* Section XII.A.1(h)), *Konda '756 PCT* discloses claim element 1[i] because *Konda '756 PCT* discloses that the forward connecting links include "zero or more" cross links and straight links.[25] (Ex. 1002, ¶¶131-132.)

j) "Said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks."

Konda '756 PCT, by way of its incorporation of the '724 provisional

[25] To the extent they can be understood, dependent claims 2, 4, 5-7, and 9 attempt to further limit the "zero or more cross links" recited in claim 1. Because claim 1 requires "zero or more" cross links, *Konda '756 PCT* discloses the features of claims 2, 4, 5-7, and 9 by virtue of disclosing the claimed forward and backward connecting links which include the "zero or more" cross links with the additional features of claims 2, 4, 5-7, and 9.

application, discloses this claim element. (Ex. 1002, ¶¶133-134.) Like claim element 1[i], this claim element does not further limit claim 1 because it simply recites several optional features. (*See supra* Section XII.A.1(i).) Since each subpart of claim element 1[j] imposes an optional "zero or more" feature onto the network components (e.g. backward connecting links including "zero or more" straight links and cross links), *Konda '756 PCT* discloses claim element 1[j] regardless of the optional features imposed thereon. (Ex. 1002, ¶¶133-134.) In other words, because *Konda '756 PCT* discloses backward connecting links as discussed above (*supra* Section XII.A.1(h)), *Konda '756 PCT* discloses claim element 1[j] because *Konda '756 PCT* discloses that the backward connecting links include "zero or more" cross links and straight links. (Ex. 1002, ¶¶133-134.)

2. Claim 2

a) "The network implemented in a non-transitory medium of claim 1, wherein said cross links between switches of stages in any two said subnetworks are connected as either vertical links only, or horizontal links only, or both vertical links and horizontal links."

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses this claim element. (Ex. 1002, ¶135.) While claim 2 is unclear regarding the antecedent basis of "said cross links," it is assumed that the cross links recited in claim 2 are included in the "zero or more cross links" of the forward connecting links and the "zero or more cross links" of the backward connecting links of claim 1. Since claim 2 requires "zero or more" cross links with the recited characteristics, *Konda '756 PCT* discloses the features of claim 2 whether or not *Konda '756 PCT* includes any cross links having the characteristics recited in claim 2.

3. Claim 3

a) "The network implemented in a non-transitory medium of claim 2, wherein each subnetwork with its said stages is replicated in either said rows or said columns of the two-dimensional grid, or

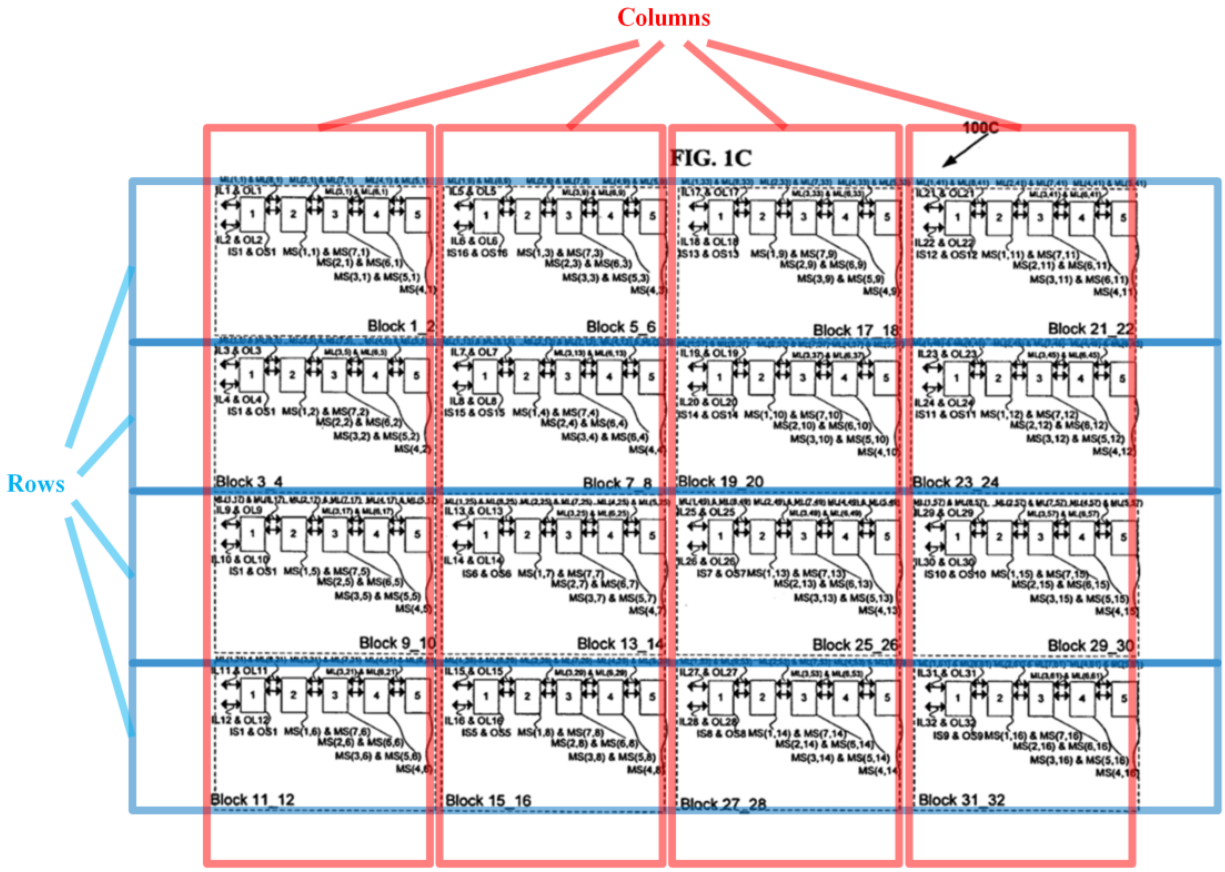
each subnetwork with said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid, or

each subnetwork with both its said stages, and said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid."

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses claim element 3[a]. (Ex. 1002, ¶¶136-138.) Claim element 3[a] recites three possible configurations of each subnetwork separated by the two "or" conjunctions. "When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Brown v. 3M*, 265 F.3d 1349, 1351 (Fed. Cir. 2001). Thus, to disclose claim element 3[a], the prior art must disclose at least one of the three possible configurations recited. *Konda '756 PCT* discloses at least the first optional configuration, i.e., *Konda '756 PCT* discloses "each subnetwork with its said

stages is replicated in either said rows or said columns of the two-dimensional grid." (Ex. 1002, ¶¶136-137.)

For example, figure 1C of the '724 provisional application shows the layout of the blocks ("subnetworks") corresponding to the network shown in figure 1B of the '724 provisional application. (Ex. 1010, 2:22-24, FIGs. 1B, 1C.) With respect to the first configuration recited in claim element 3[a], as shown in figure 1C of the '724 provisional application, each subnetwork is replicated in both the rows and columns of figure 1C, where the network of figure 1C includes four rows and four columns. (Ex. 1002, ¶137.)



(Ex. 1010, FIG. 1C (annotated to show subnetworks in rows and columns); Ex. 1002, ¶137.)

4. Claim 4

a) "The network implemented in a non-transitory medium of claim 2, wherein said horizontal links between switches in two said stages are substantially of equal length and said vertical links between switches in two said stages are substantially of equal length in the entire two-dimensional grid of rows and columns, or

said horizontal links between switches in two said stages are substantially of a hop length h and said vertical links between switches in two said stages are substantially of a hop length v where $h \geq 0$ and $v \geq 0$."

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses this claim element. (Ex. 1002, ¶¶139-140.) Claim element 4[a] recites two possible configurations of the horizontal and vertical links separated by the two "or" conjunctions. Thus, to disclose claim element 4[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at 1351. Moreover, the "vertical links" and "horizontal links" recited in claim element 4[a] further modify the "zero or more cross links" of claim 1 by way of claim 2. (Ex. 1002, ¶139.)

Since claim 4 requires "zero or more" cross links with the recited characteristics, *Konda '756 PCT* discloses the features of claim 4 whether or not *Konda '756 PCT* includes any cross links having the characteristics recited in claim 4. (*Id*., ¶¶139-140.)

5. Claim 5

a) "The network implemented in a non-transitory medium of claim 1, wherein said incoming cross links and said outgoing cross links are connected through only one multiplexer at each switch."

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses this claim element. (Ex. 1002, ¶141.) While there is no antecedent basis for "said incoming cross links" and "said outgoing cross links" as recited in claim 5, *Konda '756 PCT* discloses the features of claim 5 to the extent the "said incoming cross links" and "said outgoing cross links" are interpreted as further limiting the "zero or more" same-stage cross links in the forward and backward connecting links of claim 1. Since claim 5 requires "zero or more" cross links with the recited characteristics, *Konda '756 PCT* discloses the features of claim 5 whether or not *Konda '756 PCT* includes any cross links having the characteristics recited in claim 5. (*Id*.)

6. Claim 6

a) "The network implemented in a non-transitory medium of claim 1, wherein said one or more cross links are connected between switches in two said stages that are not same numbered."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶142.) While there is no antecedent basis for "said one or more cross links," *Konda '756 PCT* discloses the features of claim 6 to the extent the "said one or more cross links" are

interpreted as further limiting the "zero or more" same-stage cross links in the forward and backward connecting links of claim 1. Since claim 6 requires "zero or more" cross links with the recited characteristics, *Konda '756 PCT* discloses the features of claim 6 whether or not *Konda '756 PCT* includes any cross links having the characteristics recited in claim 6. (*Id*.)

7. Claim 7

a) "The network implemented in a non-transitory medium of claim 6, wherein said one or more cross links are connected between at least one same numbered stage in all said subnetworks, or said one or more cross links are connected between at least one set of two not same numbered stages in all said subnetworks."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶143.) While there is no antecedent basis in claim 1 for "said one or more cross links" as recited in claim 7, *Konda '756 PCT* discloses the features of claim 7 to the extent the "said one or more cross links" are interpreted as further limiting the "zero or more" same-stage cross links in the forward and backward connecting links of claims 1 and 6. Since claim 7 requires "zero or more" cross links with the recited characteristics, *Konda '756 PCT* discloses the features of claim 7 whether or not *Konda '756 PCT* includes any cross links having the characteristics recited in claim 7. (*Id*.)

8. Claim 9

a) "The network implemented in a non-transitory medium of claim 1, wherein said cross links are implemented in two or more metal layers, *or*

each switch is configurable by an SRAM cell or a Flash Cell or a flip-flop, *or*

said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers are either inverting or non-inverting buffers, *or*

some of said stages in a subnetwork comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ and each such switch having $d_i + m$ incoming links and $d_o + n$ outgoing links, *or*

one or more of said stages in a said subnetwork comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶¶144-147.) Claim element 9[a] modifies the network of claim 1 by way of five possible configurations separated by the four "or" conjunctions. Thus, to disclose claim element 9[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at 1351. As discussed below, *Konda '756 PCT* discloses at least three of the configurations set forth in claim 9. (Ex. 1002, ¶¶144-147.)

With respect to "said cross links are implemented in two or more metal layers," claim 9 is unclear regarding the antecedent basis of "said cross links." It is

assumed that "said cross links" recited in claim 9 are included in the "zero or more cross links" of the forward connecting links and the "zero or more cross links" of the backward connecting links of claim 1. Whether or not the embodiment shown in figure 1B of the '724 provisional application includes any cross links as recited in claim 1 and further characterized by claim 9, that embodiment still discloses "zero or more" cross links that are implemented in two or more metal layers as recited in claim 9. (*Id*., ¶145.)

Moreover, *Konda '756 PCT* also discloses, by way of its incorporation of the '724 provisional application, "some of said stages in a subnetwork comprising a switch of size $(d_i +m)x(d_o +n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ and each such switch having $d_i + m$ incoming links and $d_o + n$ outgoing links." It is assumed that this phrase simply requires that some of the stages include a switch that is 2x2 or greater in size such that the switch has at least 2 incoming links and 2 outgoing links. As discussed above with respect to claim element 1[e], such a switch is included in each of the stages of the network shown in figure 1B of the '724 provisional application. (*Supra* Section XII.A.1(e).) Therefore, *Konda '756 PCT* discloses the features of claim 9 for this additional reason. (Ex. 1002, ¶146.)

Furthermore, *Konda '756 PCT*, by way of its incorporation of the '724 provisional application, also discloses "each switch is configurable by an SRAM

cell or a Flash Cell or a flip-flop." For instance, the '724 provisional application discloses that "[i]n all the embodiments disclosed in the current invention, all the switches in some embodiments may be implemented as active switches consisting of cross points using SRAM cells or Flash memory cells." (Ex. 1010, 61:19-21.) Therefore, the switches shown in the figure 1B embodiment of the '724 provisional application may be implemented using cross points with SRAM or Flash memory cells controlling the switches. (Ex. 1002, ¶147.)

9. Claim 10

a) "The network implemented in a non-transitory medium of claim 1, wherein said switches of size d_i x d_o are either fully populated or partially populated, *or*

said plurality of subnetworks are implemented in a single dimension, *or*

said plurality of subnetworks are either implemented in three or more dimensions or implemented in a 3D integrated circuit device."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶¶148-149.) Claim element 10[a] modifies the network of claim 1 by way of three possible configurations separated by the two "or" conjunctions. Thus, to disclose claim element 10[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at 1351.

Konda '756 PCT, by way of its incorporation of the '724 provisional application, discloses at least one of these configurations. For example, i.e., the '724 provisional application discloses that "said plurality of subnetworks are either implemented in three or more dimensions or implemented in a 3D integrated circuit device" as set forth in claim 10. (Ex. 1002, ¶148.) For instance, the '724 provisional states that "the switches may be implemented as in 3D-FPGAs." (Ex. 1010, 61:19-24; Ex. 1002, ¶148.) Because an FPGA is an integrated circuit device, implementing the switches of the network of figure 1B as in a 3D-FPGA discloses implementing the plurality of subnetworks in a "3D integrated circuit device" as recited in claim 10. (Ex. 1002, ¶149.)

10. Claim 11

a) "A network implemented in a non-transitory medium comprising"

The preamble of claim 11 recites features that track those of the preamble of claim 1. Thus, to the extent the preamble is limiting, *Konda '756 PCT* discloses the features of the preamble for at least the reasons presented above for claim element 1[a]. (*Supra* Section XII.A.1(a); Ex. 1002, ¶150.)

b) "a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links"

Claim element 11[b] recites features that track those of claim element 1[b]. *Konda '756 PCT* discloses this feature for at least the reasons presented above for element 1[b]. (*Supra* Section XII.A.1(b); Ex. 1002, ¶151.)

c) "said plurality of subnetworks arranged in a two-dimensional grid of rows and columns"

Claim element 11[c] recites features that track those of claim element 1[c]. *Konda '756 PCT* discloses this feature for at least the reasons presented above for element 1[c]. (*Supra* Section XII.A.1(c); Ex. 1002, ¶152.)

d) "each subnetwork comprising y stages, where $y \geq 1$; and"

Claim element 11[d] recites features that track those of claim element 1[d]. *Konda '756 PCT* discloses this feature for at least the reasons presented above for element 1[d]. (*Supra* Section XII.A.1(d); Ex. 1002, ¶153.)

e) "each stage comprising a switch of size d_i x d_o, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size d_i x d_o having d_i incoming links and d_o outgoing links; and"

Claim element 11[e] recites features that track those of claim element 1[e]. *Konda '756 PCT* discloses this feature for at least the reasons presented above for element 1[e]. (*Supra* Section XII.A.1(e); Ex. 1002, ¶154.)

f) "Said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork; and"

Claim element 11[f] recites features that track those of claim element 1[f]. *Konda '756 PCT* discloses this feature for at least the reasons presented above for element 1[f]. (*Supra* Section XII.A.1(f); Ex. 1002, ¶155.)

g) "each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said inlet links and may or may not be comprising the same number of said outlet links; each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said stages; each stage may or may not be comprising the same number of switches; and each switch in each stage may or may not be of the same size, each multiplexer in each stage may or may not be of the same size and"

Claim element 11[g] recites features that track those of claim element 1[g]. *Konda '756 PCT* discloses this feature for at least the reasons presented above for element 1[g]. (*Supra* Section XII.A.1(g); Ex. 1002, ¶156.)

h) "Said incoming links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks, and"

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶¶157-158.) As an initial matter, this claim element does not further limit claim 11, as it simply recites several optional features. *MPHJ Tech. Invs., LLC*, 847 F.3d at 1379; *In re Johnston*, 435 F.3d at 1384. Since each subpart of claim element 11[h] imposes an optional "zero or more" feature onto the network components such as the incoming links including "zero or more" straight links and two types of "zero or more" cross links, *Konda '756 PCT* discloses claim element 11[h] regardless of the optional features imposed thereon. (Ex. 1002, ¶¶157-158.) In other words, because *Konda '756 PCT* discloses incoming links as discussed above (*supra* Section XII.A.10(e)), *Konda '756 PCT* discloses claim element 11[h] because *Konda '756 PCT* discloses that the incoming links include "zero or more" straight links and

"zero or more" of each of the different types of cross links recited.[26] (Ex. 1002, ¶¶157-158.)

> **i) "Said outgoing links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks."**

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶¶159-160.) As an initial matter, this claim element does not further limit claim 11, as it simply recites several optional features. *MPHJ Tech. Invs., LLC*, 847 F.3d at 1379; *In re Johnston*, 435 F.3d at 1384. Since each subpart of claim element 11[i] imposes an optional "zero or more" feature onto the network components such as the outgoing

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[26] To the extent they can be understood, dependent claims 12, 14, 15, and 19 attempt to further limit the "zero or more cross links" recited in claim 11. Because claim 11 requires "zero or more" cross links, *Konda '756 PCT* discloses the features of claims 12, 14, 15, and 19 because *Konda '756 PCT* discloses "zero or more" cross links with the features added by those claims.

links including "zero or more" straight links and two types of "zero or more" cross links, *Konda '756 PCT* discloses claim element 11[i] regardless of the optional features imposed thereon. (Ex. 1002, ¶¶159-160.) In other words, because *Konda '756 PCT* discloses outgoing links as discussed above (*supra* Section XII.A.10(e)), *Konda '756 PCT* discloses claim element 11[i] because *Konda '756 PCT* discloses that the incoming links include "zero or more" straight links and "zero or more" of each of the different types of cross links recited. (Ex. 1002, ¶¶159-160.)

11. Claim 12

a) "The network implemented in a non-transitory medium of claim 11, wherein said cross links between switches of stages in any two said subnetworks are connected as either vertical links only, or horizontal links only, or both vertical links and horizontal links."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶161.) While claim 12 is unclear regarding the antecedent basis of "said cross links," it is assumed that the cross links recited in claim 12 are included in the two types of "zero or more cross links" of the incoming links and the two types of "zero or more cross links" of the outgoing links of claim 11.

Because claim 12 requires "zero or more" cross links with the recited characteristic, *Konda '756 PCT* discloses the features of claim 12 whether or not *Konda '756 PCT* includes any cross links having the characteristics recited in

claim 12. Indeed, even assuming that *Konda '756 PCT* discloses some cross links as recited in claim 11, but those cross links do not have the characteristics recited in claim 12, *Konda '756 PCT* would still disclose "zero" cross links as recited in claim 12. (*Id*.)

12. Claim 13

a) "The network implemented in a non-transitory medium of claim 12, wherein each subnetwork with its said stages is replicated in either said rows or said columns of the two-dimensional grid, or each subnetwork with said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid, or each subnetwork with both its said stages, and said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid."

Claim 13 recites features that track those of claim 3. *Konda '756 PCT* discloses this feature for at least the reasons presented above for claim 3. (*Supra* Section XII.A.3; Ex. 1002, ¶162.)

13. Claim 14

a) "The network implemented in a non-transitory medium of claim 12, wherein said horizontal links between switches in two said stages are substantially of equal length and said vertical links between switches in two said stages are substantially of equal length in the entire two-dimensional grid of rows and columns, or

said horizontal links between switches in two said stages are substantially of a hop length h and said vertical links between switches in two said stages are substantially of a hop length v where h ≥ 0 and v ≥ 0."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶163.) Claim element 14[a] recites two possible configurations of the horizontal and vertical links separated by the two "or" conjunctions. Thus, to disclose claim element 14[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at 1351. Moreover, the "vertical links" and "horizontal links" recited in claim element 14[a] further modify the two types of "zero or more cross links" of the incoming links and the two types of "zero or more cross links" of the outgoing links of claim 11 by way of claim 12. (Ex. 1002, ¶163.) Because claim 14 requires "zero or more" same-stage or inter-stage cross links with the recited characteristics, in order to disclose this claim element *Konda '756 PCT* is not required to disclose any cross links at all, let alone any cross links having the

requirements added by claims 12 and 14. (*Supra* Section XII.A.11; Ex. 1002, ¶163.)

14. Claim 15

a) "The network implemented in a non-transitory medium of claim 12, wherein said one or more cross links are connected between at least one same numbered stage in all said subnetworks or said one or more cross links are connected between at least one set of two not same numbered stages in all said subnetworks."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶164.) While there is no antecedent basis for "said one or more cross links" as recited in claim 15, *Konda '756 PCT* discloses the features of claim 15 to the extent the "said one or more cross links" is interpreted as further limiting the "zero or more" same-stage or inter-stage cross links in the incoming and outgoing links of claim 11. Because claim 15 requires "zero or more" same-stage or inter-stage cross links with the recited characteristics, *Konda '756 PCT* discloses the features of claim 15 whether or not *Konda '756 PCT* includes any cross links having the characteristics recited in claim 15. Indeed, even assuming that *Konda '756 PCT* discloses some cross links as recited in claim 11, but those cross links do not have the characteristics recited in claims 12 and 15, *Konda '756 PCT* still discloses "zero" cross links as recited in claim 15. (Ex. 1002, ¶164.)

15. Claim 17

a) "The network implemented in a non-transitory medium of claim 11, wherein some of said stages in a subnetwork comprising a switch of size (d_i + m) x (d_0 + n), where $d_i \geq 2$, $d_o \geq 2$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ and each such switch having d_i + m incoming links and d_o + n outgoing links, or

one or more of said stages in a said subnetwork comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers."

Claim 17 recites features similar to those set forth in claim 9. *Konda '756 PCT* discloses this claim element for at least the reasons presented above for claim 9. (*Supra* Section XII.A.8; Ex. 1002, ¶165.)

16. Claim 18

a) "The network implemented in a non-transitory medium of claim 11, wherein said switches of size d_i x d_o are either fully populated or partially populated, or

said plurality of subnetworks are implemented in a single dimension, or

said plurality of subnetworks are either implemented in three or more dimensions or implemented in a 3D integrated circuit device."

Claim 18 recites features that track those of claim 10. *Konda '756 PCT* discloses this claim element for at least the reasons presented above for claim 10. (*Supra* Section XII.A.9; Ex. 1002, ¶166.)

17. Claim 19

a) "The network implemented in a non-transitory medium of claim 11, wherein said one or more cross links are connected between at least one same numbered stage in all said subnetworks, and said same numbered stage may be any stage including the final stage."

Konda '756 PCT discloses this claim element. (Ex. 1002, ¶167.) While there is no antecedent basis for "said one or more cross links" as recited in claim 19, *Konda '756 PCT* discloses the features of claim 19 to the extent the "said one or more cross links" is interpreted as further limiting the "zero or more" same-stage or inter-stage cross links in the incoming and outgoing links of claim 11. For instance, in order to disclose the features of claim 19, *Konda '756 PCT* need not disclose any cross links having the requirements added by claim 19. As long as *Konda '756 PCT* discloses "zero or more" cross links with the added characteristics of claim 19, *Konda '756 PCT* discloses the claimed cross links. In other words, even assuming that *Konda '756 PCT* discloses some cross links as recited in claim 11, but those cross links do not have the characteristics recited in claim 19, *Konda '756 PCT* still discloses "zero" cross links as recited in claim 19. (*Id*.)

B. Ground 2: *Konda '756 PCT* In View of *Wong* Renders Claims 1-7, 9-15, and 17-19 Obvious

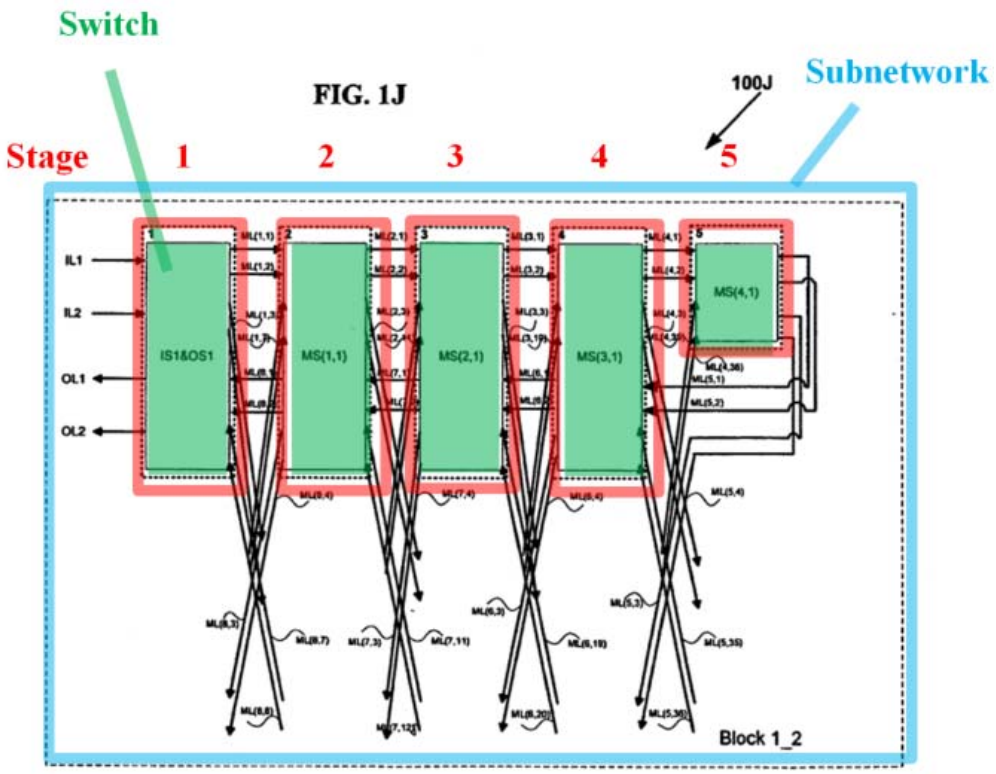
1. Claim 1

As demonstrated above in Section XII.A, *Konda '756 PCT* discloses all of the features of claim 1. For example, as discussed above, the network of figure 1B of the '724 provisional application as incorporated by reference in *Konda '756 PCT* discloses "each multiplexer in each stage may or may not be of the same size," as recited in claim element 1[g](5), because nowhere in claim 1 is it specified that each stage includes any multiplexers at all. (*Supra* Section XII.A.1[g](5).)

However, to the extent that PO argues or the Board finds that claim element 1[g](5) requires each stage or any stages of the network to include a multiplexer, it would have been obvious in view of *Wong* to implement the switches in the stages of figure 1B of the '724 provisional application using multiplexers that "may or may not be of the same size." (Ex. 1002, ¶¶168-185.) As discussed below, in view of *Wong*, a POSITA would have found it obvious to include a multiplexer in each stage of the network disclosed in figure 1B the '724 provisional application in order to provide operational switches that enable the interconnections between the switches in the stages of the network. (*Id.*)

In general, obviousness entails an inquiry that is "expansive and flexible" and takes into account "the inferences and creative steps that a person of ordinary skill in the art would employ" when presented with the teachings of the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-18 (2007). Under this flexible approach, it can be important to identify "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements" in the way claimed. *Takeda Chemical Industries, Ltd. v. Alphapharm Pty., Ltd.*, 492 F.3d 1350, 1356–57 (Fed. Cir. 2007). Such reason may be found "explicitly or implicitly in market forces; design incentives; the interrelated teachings of multiple patents; any need or problem known in the field of endeavor at the time of invention and addressed by the patent; and the background knowledge, creativity, and common sense of the person of ordinary skill." *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1371 (Fed. Cir. 2018) (internal quotations and citations omitted); *see also KSR*, 550 U.S. at 419-20. Moreover, "'if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.'" *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (quoting *KSR*, 550 U.S. at 417).

Under the law of obviousness, including the above principles, the combination of *Wong* with *'756 Konda PCT* would have been obvious to a POSITA. As discussed above, *'756 Konda PCT* discloses switches included in the stages of the subnetworks shown in figure 1B of the '724 provisional application. (*See supra* Section XII.A.1(e).) For example, the '724 provisional application states that the network of figure 1A, which is folded to produce the network of figure 1B, has "nine stages of one hundred and forty four switches." (Ex. 1010, 9:10-12.) The '724 provisional application further states with respect to figure 1A that "input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of sixteen, four by two switches OS1-OS16" and that all the middle stages consist of sixteen, four by four switches. (*Id.*, 9:15-24; Ex. 1002, ¶172.) Moreover, the '724 provisional application discloses that the switches for the stages in figure 1B can be combined switches as shown in figure 1J below, where the combined input and output switches (e.g. IS1&OS1 corresponding to stage 1) is a 6x6 switch and the middle switches (e.g. MS1,1) are each implemented as an 8x8 switch. (Ex. 1010, 29:4-28; Ex. 1002, ¶172.) Therefore the network shown in figure 1B of the '724 provisional application includes one or more switches in each of the stages. (Ex. 1002, ¶172.)



(Ex. 1010, FIG. 1J (annotated); Ex. 1002, ¶172.)

But *Konda '756 PCT* does not provide specifics as to how the above-identified switches are implemented. (Ex. 1002, ¶173.) Therefore, a POSITA would have looked to references that provide further details regarding circuitry used for implementing switches. (*Id.*) A POSITA would have accordingly looked to *Wong* and combined the teachings of *Wong* with *Konda '756 PCT* because *Wong* discloses a well-known implementation of switches used in networks similar to those described in *Konda '756 PCT*. In view of *Wong*, a POSITA would have combined the teachings of the two references such that the switches in *'756 Konda PCT* would be implemented using multiplexers as disclosed in *Wong*. (*Id.*)

Wong, like *Konda '756 PCT*, relates to an interconnection network architecture which provides an interconnection network that can be used in FPGAs. (Ex. 1008, Abstract; Ex. 1010, 6:18-19, 7:1-9; Ex. 1002, ¶174.) An example layout of an FPGA that includes *Wong's* interconnection network architecture is shown in figure 13A below. (Ex. 1008, FIG. 13A, 13:12-16.) The FPGA layout in figure 13A includes switches 82 (annotated in green) and associated logic cells 81 (annotated in red). (*Id*.)

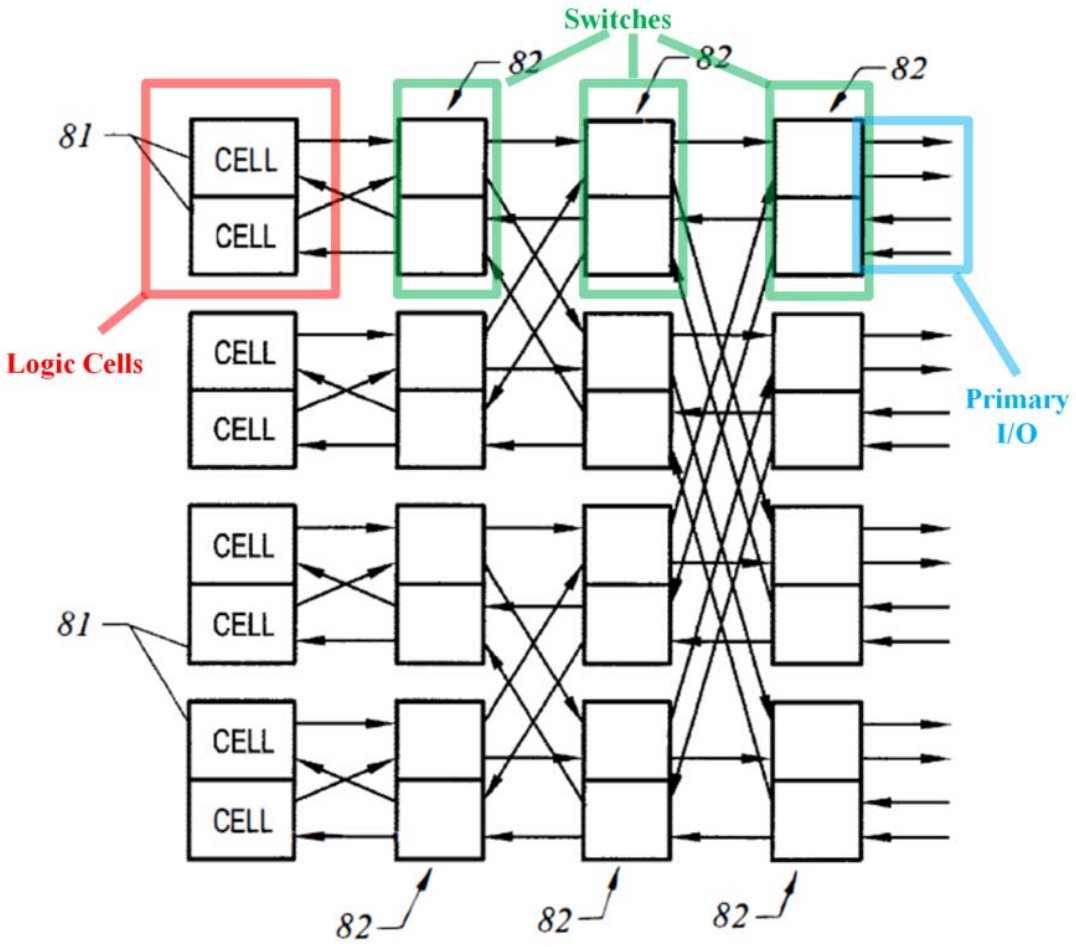


FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶174.)

Like *Konda '756 PCT*, the networks used in the FPGAs disclosed in *Wong* utilize links between switches in successive stages in the same row of switches (annotated in blue below) as well as links between switches in successive stages in different rows (annotated in green below).

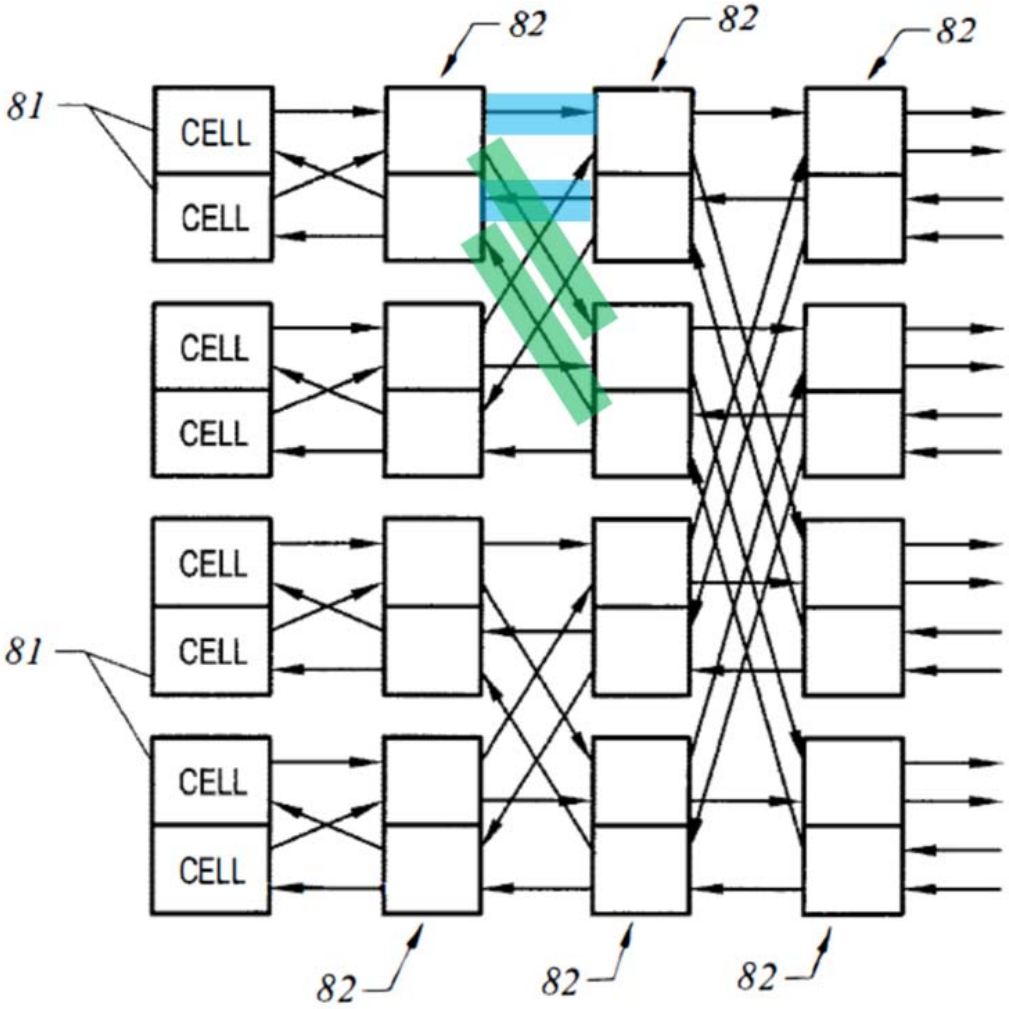


FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶175.)

A POSITA would have understood that the 4x4 switches 82 shown in figure 13A can be made up of sets of 2x2 switches such as those shown in figures 2A-C of *Wong* or can be a combined switch such as that shown in figure 7 of *Wong*. (Ex. 1002, ¶¶176-177; Ex. 1008, 5:4-6 ("The building block of the described Benes network is the 2x2 (2 input, 2 output) switch 20, having operations illustrated in FIGS. 2A and 2B."); *see also id*., 5:26-29.) For example, figure 2C shows an example 2x2 switch implementation, and figure 7 shows an example 4x4 switch implementation. (Ex. 1008, 2:29-30, FIGs. 2C, 7; Ex. 1002, ¶¶178-179.)

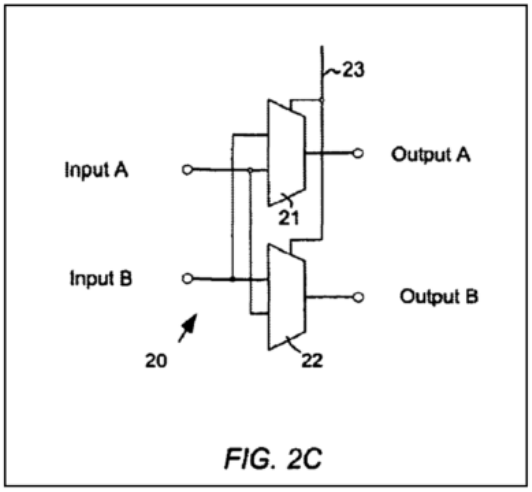


FIG. 2C

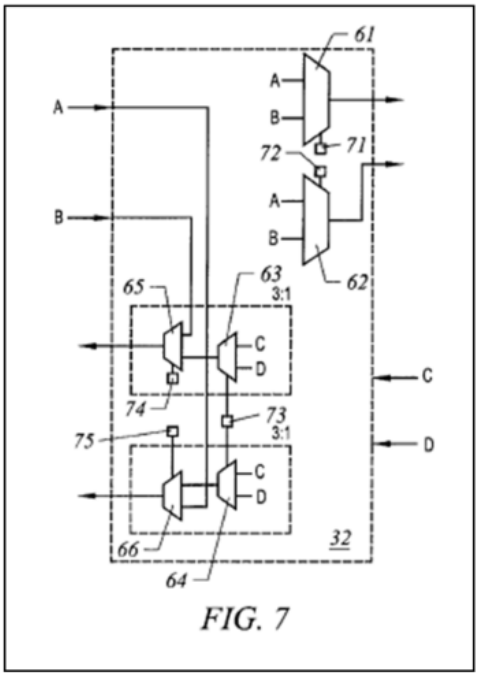


FIG. 7

(Ex. 1008, FIGs. 2C, 7.)

With respect to the switch shown in figure 2, *Wong* discloses:

> The switching itself can be implemented with two 2:1 multiplexers or MUX's as shown by FIG. 2C. The switch 20 has two MUXs 21 and 22 having two input nodes which are each connected to one of the input terminals, input A or input B, of the switch 20. The output node of the MUX 21 forms the output terminal, output A, and the output node of the MUX 22 forms the output terminal, output B, of the switch 20. Both MUXs 21 and 22 are connected to a control line 23 which carries the configuration or control bit. The entire switch cell only requires 18 transistors in a CMOS (Complementary Metal-Oxide-Semiconductor) implementation of an integrated circuit.

(Ex. 1008, 5:14-25.)

According to *Wong*, figure 7 illustrates a combined switch that includes four inputs and four outputs and supports "corner turning" where an input on the left side of the switch (A or B) is fed back to an output on the left side of the switch. (Ex. 1008, 7:22-8:9, FIG. 7.) Such corner turning is supported by the combined switch shown in figure 7, which includes many multiplexers. (*Id.,* 8:10-34, FIG. 7; Ex. 1002, ¶180.)

Therefore, *Wong* discloses implementing each switch in each stage using multiplexers. Specifically, *Wong* discloses networks such as that illustrated in figure 13A, where each stage includes a switch 82, and where each switch can be constructed using multiplexers such as is shown in figures 2 and 7 of *Wong*. (Ex.1008, 2:29-30, 2:56-57, 5:14-29, 8:12-34, 13:19-22, FIGs. 2C, 7, 13A; Ex. 1002, ¶181.)

Based on the teachings of *Wong*, a POSITA would have been motivated to implement the switches shown in figure 1B of *Konda '756 PCT* using multiplexers. (Ex. 1002, ¶182.) A POSITA would have looked to *Wong* because, *inter alia*, like *Konda '756 PCT*, *Wong* is related to hierarchical interconnection networks used in FPGAs that include a plurality of stages that includes switches. (Ex. 1008, 1:59-2:22; Ex. 1010, 2:17-19, 9:10-14, 15:15-16, FIG. 1B; Ex. 1002, ¶182.)

Having looked to *Wong*, a POSITA would have found it obvious to combine the teachings of *Wong* with *Konda '756 PCT* to use multiplexers (like in *Wong*) to construct the switches of *Konda '756 PCT*'s network, including the network shown in figure 1B of the '724 provisional application. (Ex. 1002, ¶¶182-183.) A POSITA would have been motivated to combine the teachings of these two references in the above manner because *Konda '756 PCT* does not disclose the

particular implementation of the switches included in its network, while *Wong* provides details on how to implement switches such as those used in *Konda '756 PCT*'s network. (*Id*.) Indeed, *Wong* discloses that "[t]he entire switch cell *only requires 18 transistors* in a CMOS (Complementary Metal-Oxide-Semiconductor) implementation of an integrated circuit" (Ex. 1008, 5:22-26), thereby providing an efficient and well-known implementation of switches in networks that can be used in, for example, FPGAs. Such a modification of *Konda '756 PCT* would have been within the capabilities of one of ordinary skill because *Wong* discloses how such switches can be constructed using multiplexers. (Ex. 1002, ¶183.) Indeed, using multiplexers in the switches shown in figure 1B of *Konda '756 PCT* would have been straightforward for a person of ordinary skill given such person's knowledge of basic circuit concepts of multiplexers and switches. (*Id*.)

A POSITA would have recognized that the proposed modification would have involved a combination of known prior art elements, according to known methods, to yield predictable results (e.g., a switch that works as described in *Konda '756 PCT* that includes a multiplexer like in *Wong*). (*Id*., ¶184.) *See KSR*, at 416 (2007). A POSITA would have reasonably expected success in making such a modification without negatively affecting the operation of *Konda '756 PCT*'s network. (Ex. 1002, ¶184.)

Moreover, POSITA would have recognized that such an implementation would have been a common-sense and predictable choice among known options (e.g., implementing the switch as a multiplexer) given the disclosures of *Konda '756 PCT*, *Wong*, and the knowledge of a POSITA at the time of the alleged invention. (*Id*.) A POSITA would have had the capability and knowledge to take into account any modifications and issues when incorporating *Wong*'s features with those of *Konda '756 PCT* to ensure *Konda '756 PCT's* network operated properly in accordance with the objectives described by *Konda '756 PCT*. (*Id.*)

Therefore, *Konda '756 PCT* in combination with *Wong* discloses or suggests "each multiplexer in each stage may or may not be of the same size" as recited in claim 1. Furthermore, *Konda '756 PCT* in combination with *Wong* discloses or suggests the remaining features of claim 1 for the reasons discussed above for claim 1 in Ground 1, with the only modification to the analysis for claim 1 being the inclusion of a multiplexer in the switches based on *Wong*. (*Supra* Section XII.A.1; Ex. 1002, ¶185.)

2. Claim 11

Konda '756 PCT in combination with *Wong* discloses or suggests the features of claim 11 for reasons similar to those discussed above in Section XII.A.10; Ex. 1002, ¶186.) Specifically, *Konda '756 PCT* if view of *Wong*

discloses the features of claim 11 as discussed above in Section XII.A.10 with respect to *Konda '756 PCT*, where it would have been obvious to implement the switches in the stages of the network in in figure 1B of the '724 provisional application as incorporated by reference in *Konda '756 PCT* using multiplexers as disclosed in *Wong* for the same reasons discussed above in Section XII.B.1. Furthermore, *Konda '756 PCT* in combination with *Wong* discloses or suggests the remaining features of claim 11 for the reasons discussed above for claim 11 in Ground 1, with the only modification to the analysis for claim 11 being the inclusion of a multiplexer in the switches based on *Wong*. (*Supra* Section XII.A.10; Ex. 1002, ¶186.)

3. Claims 2-7, 9-10, 12-15, and 17-19

Konda '756 PCT in combination with *Wong* discloses or suggests the features of these claims for reasons similar to those discussed in Sections XII.A.2-9, XII.A.11-17. (*See supra* Sections XII.A.2-9, XII.A.11-17; Ex. 1002, ¶187.) The same analysis presented above for these claims in Ground 1 is also applicable for the *Konda '756 PCT-Wong* combination discussed above in Sections XII.B.1-2. (*See supra* Sections XII.B.1-2; Ex. 1002, ¶187.) The combination of *Wong* with *Konda '756 PCT* does not affect the analysis for these claims in Sections XII.A.2-9, XII.A.11-17.

XIII. THE BOARD SHOULD INSTITUTE THIS PETITION

Petitioner is filing two additional PGR petitions challenging claims of the '553 patent concurrently with the filing of this petition. One of the other petitions concerns § 112 issues, including indefiniteness, written description support, and enablement. The other prior art petition includes a single ground with *Wong* as the primary reference and does not utilize the primary reference at issue here (*Konda '756 PCT*).[27] The prior art petitions are being filed out of an abundance of caution because of the statutory estoppel provisions.

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[27] To extent Patent Owner contends that the disclosure of *Konda '756 PCT* is cumulative to other subject matter that was considered by the Patent Office during prosecution, Petitioner presents that disclosure in a new light. For example, the prosecution history of the '553 patent does not include substantive discussion of *Konda '756 PCT* or any other prior art reference relating to patentability of the '553 patent claims. Indeed, there were no claim rejections based on any prior art. Here, Petitioner presents testimony from Dr. Baker confirming that the relevant teachings of *Konda '756 PCT* disclose what is claimed by challenged claims 1-7, 9-15, and 17-19 of the '553 patent. (*See* Ex. 1002, ¶¶86-167.) Therefore, any consideration of disclosure similar to that of *Konda '756 PCT* by the Patent Office

The unpatentability grounds presented in the Petition differ substantially from those raised in the concurrently-filed petitions. Accordingly, the Board should institute review based on the substantially different grounds presented in this petition. Indeed, institution of the three petitions is particularly justified given that the Board generally discourages follow-on petitions. *See General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper No. 19 at 9 (Sept. 6, 2017). Finally, Petitioner has narrowed the grounds presented in each of the petitions to achieve the goal of "just, speedy, and inexpensive resolution" consistent with 37 C.F.R. § 42.1(b).[28]

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during prosecution of the '553 patent should not preclude the Board from considering and adopting the grounds in this petition.

[28] PO continues to prosecute patent applications in the same family as the '553 patent that, while no longer reciting the "rings" feature, include unsupported claim terms and optional features. (*See, e.g.*, Ex. 1037, 4-24.) Such claims, which include features similar to those recited in the '553 patent claims, are indefinite on their face, and the minimal substantive limitations, to the extent they can be understood, are plainly disclosed in the prior art, including PO's own earlier-published patents and applications.

XIV. CONCLUSION

For the reasons given above, Petitioner requests institution of PGR for claims 1-7, 9-15, and 17-19 of the '553 patent, and a finding that the claims are unpatentable based on the above grounds.

Respectfully submitted,

Dated: March 18, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,003,553 contains, as measured by the word processing system used to prepare this paper, 18,594 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: March 18, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 18, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,003,553 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent electronically to Patent Owner's litigation counsel listed below:

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