

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES, INC.
Petitioner

v.

KONDA TECHNOLOGIES INC.
Patent Owner

Patent No. 10,003,553

**PETITION FOR POST GRANT REVIEW
OF U.S. PATENT NO. 10,003,553**

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Ex. 1026	File History of U.S. Provisional Application No. 60/940,394
Ex. 1027	U.S. Pat. No. 8,898,611
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Ex. 1034	File History of U.S. Application No. 12/601,275
Ex. 1035	U.S. Patent No. 9,374,322
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Ex. 1037	RESERVED
Ex. 1038	RESERVED
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Ex. 1040	U.S. Patent No. 3,358,269

I. INTRODUCTION

Flex Logix Technologies, Inc. (“Petitioner”) requests post grant review (“PGR”) of claims 1-7, 9-15, and 17-19 (“the challenged claims”) of U.S. Patent No. 10,003,553 (“the ’553 patent”) (Ex. 1001), which, according to PTO records, is assigned to Konda Technologies, Inc. (“Patent Owner” or “PO”). For the reasons below, the challenged claims should be found unpatentable and canceled.

The ’553 patent purports to be part of a family of applications based on U.S. Provisional Patent Application 61/531,615 (“the ’615 provisional application”) filed September 7, 2011. Prior to filing the ’615 provisional application to which the ’553 purports to claim priority, PO filed numerous patent applications concerning similar subject matter, and many of those earlier-filed applications are listed as related applications in the ’553 patent. (Ex. 1001, 1:8-2:62.) During prosecution of applications claiming priority to the ’615 provisional application, those earlier filed applications were relied on by the PTO for claim rejections.

In addressing those previous rejections based on its own earlier-filed subject matter, PO argued that the rejected claims included “rings” that were not disclosed in the earlier-filed applications. The claims of the ’553 patent do not include any “rings,” and as demonstrated in another concurrently-filed PGR petition, the challenged claims of the ’553 patent are anticipated or rendered obvious by PO’s

earlier-filed applications.

Similarly, during prosecution of an earlier-filed related application, PO added limitations to pending claims to overcome rejections based on *Wong*. However, the claims of the '553 patent do not include the features PO previously added in order to overcome *Wong*, and, as demonstrated below, *Wong* anticipates the challenged claims of the '553 patent.¹

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Parties-in-Interest

Petitioner identifies Flex Logix Technologies, Inc. as the real party-in-interest.

¹ Petitioner is also concurrently filing an additional petition for PGR of the '553 patent demonstrating that all the claims of the '553 patent are indefinite and fail to comply with the written description and enablement requirements under 35 U.S.C. § 112. However, to the extent the claims can be understood, the instant petition and another concurrently-filed prior art petition demonstrate that the claims are also unpatentable over the prior art. The additional prior art petitions are being filed out of an abundance of caution because of the statutory estoppel provisions.

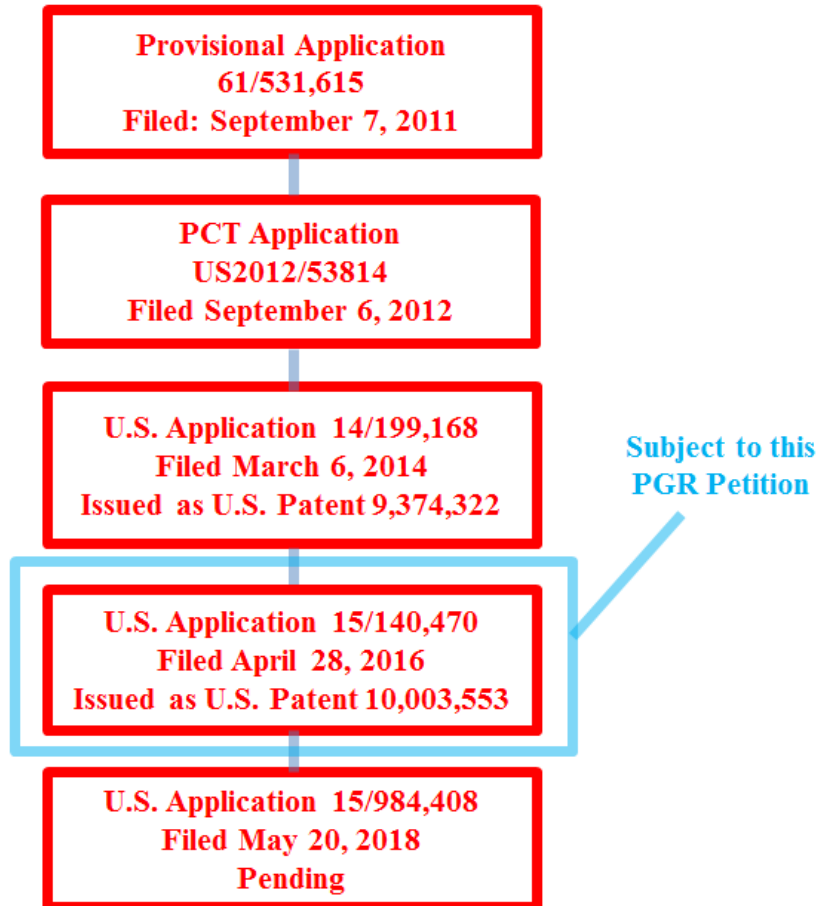
B. Related Matters

1. Lawsuit(s)

PO has asserted the '553 patent against Petitioner in *Konda Technologies Inc. v. Flex Logix Technologies, Inc.*, No. 5:18-cv-07581-LHK (N.D. Cal.). PO has also asserted U.S. Patent Nos. 8,269,523 (“the '523 patent”), 8,898,611 (“the '611 patent”), 9,529,958 (“the '958 patent”), and 10,050,904 (“the '904 patent”) in the foregoing district court litigation.

2. Related Applications

The '553 patent is related to several patents and/or patent applications, as shown in the purported priority chain below:



3. Concurrently filed petitions

Petitioner is concurrently filing two other petitions for PGR of certain claims of the '553 patent.

C. Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Quadeer A. Ahmed (Reg. No. 60,835). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700,

Fax: 202.551.1705, email: PH-FlexLogix-Konda-PGR@paulhastings.com.

Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. TIME FOR FILING UNDER 37 C.F.R. § 42.202

The '553 patent issued on June 19, 2018, and this Petition is being timely filed no later than the date that is nine months after the date of the grant of the '553 patent.

V. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.204(a)

Petitioner certifies that the '553 patent is available for PGR and Petitioner is not barred or estopped from requesting PGR on the ground identified herein.

As discussed below in Section IX, the '553 patent is eligible for PGR because it has at least one claim that is not entitled to a pre-AIA filing date.

VI. PRECISE RELIEF REQUESTED AND GROUND RAISED

A. Claims for Which Review is Requested

Petitioner respectfully requests review of claims 1-7, 9-15, and 17-19 (“challenged claims”) of the '553 patent, and cancellation of these claims as unpatentable.

B. Statutory Ground of Challenge

The challenged claims should be canceled as unpatentable on the following ground:

Ground 1: Claims 1-7, 9-15, and 17-19 are unpatentable under AIA 35 U.S.C. § 102(a)(1) as being anticipated by U.S. Patent No. 6,940,308 to Wong (“*Wong*”) (Ex. 1008).

The earliest possible priority date for the ’553 patent is September 7, 2011, which corresponds to the filing date of the ’615 provisional application (Ex. 1007, 90). *Wong* issued on September 6, 2005. Thus, *Wong* is prior art at least under AIA 35 U.S.C. § 102(a)(1) with respect to the ’553 patent.

Wong was considered by the Patent Office during prosecution, but Petitioner presents *Wong* in a new light never considered by the Office. (*See infra* Section XII.) For example, the prosecution history of the ’553 patent does not include substantive discussion of *Wong* relating to patentability of the ’553 patent claims, and *Wong* was not the basis for any claim rejections. (*See generally* Ex. 1004.) Here, Petitioner presents testimony from R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the ’553 patent (Ex. 1002, ¶¶3-13, 18; Ex. 1003), who confirms that the relevant teachings of *Wong* disclose what is claimed by challenged claims 1-7, 9-15, and 17-19 of the ’553 patent. (*See* Ex. 1002, ¶¶82-

221.)

Notably, a different Examiner relied upon *Wong* to reject claims in another patent application assigned to PO, namely U.S. Patent Application No. 12/601,275 (“the ’275 application”), which eventually issued as U.S. Patent No. 8,269,523 (“the ’523 patent”). (*See* Ex. 1034, 76-103.) In response to the rejection, which concerned numerous features also recited in the claims of the ’553 patent (*id.*, 78-79), PO presented arguments that mischaracterize the disclosure of *Wong* (*id.*, 48-50). (Ex. 1002, ¶¶83-87.) Moreover, PO amended the claims to include limitations that are not present in the claims of the ’553 patent (Ex. 1035, 53-54), where the Examiner listed those features in the reasons for allowance of the amended claims in the ’275 application (*id.*, 14). (Ex. 1002, ¶¶88-90.)

As such, consideration of *Wong* by the Patent Office during prosecution of the ’553 patent should not preclude the Board from considering and adopting the ground in this petition.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’553 patent would have had a master’s degree in electrical engineering or a similar field, and at least two to three years of experience with

integrated circuits and networks. (Ex. 1002, ¶18.) More education can supplement practical experience and vice versa. (*Id.*)

VIII. BACKGROUND

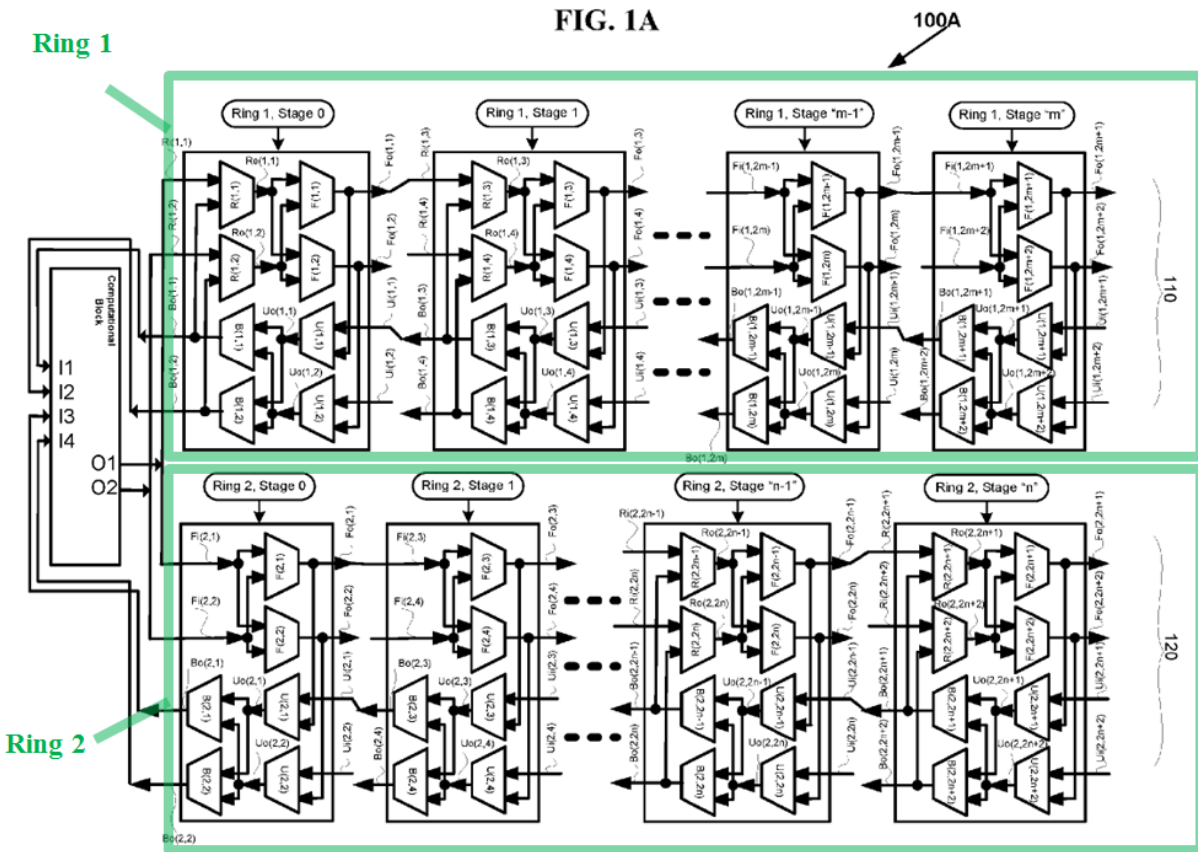
The '553 patent generally relates to switching networks that can be used to route signals between logic blocks included on an integrated circuit device such as an FPGA. (Ex. 1002, ¶¶20-50.)

A. The '553 Patent

The '553 patent, which matured from the U.S. Application No. 15/140,470 (“the '470 application”), acknowledges that multi-stage hierarchical networks were known and used in many applications at the time of the alleged invention, such as in “FPGA routing of hardware designs.” (Ex. 1001, 2:66-3:1, 4:47-48.) The '553 patent states that known VLSI (very large scale integration) layouts for integrated circuits with such networks, such as the Benes network disclosed by *Wong* (Ex. 1008), are “inefficient and complicated.” (*Id.*, 3:2-4, 3:30-36.) For instance, the '553 patent contends that prior art network layouts “require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the signal which effect the maximum clock speed of operation.” (*Id.*, 3:43-48; Ex. 1002, ¶¶31-32 (citing Ex. 1040).)

The '553 patent alleges to disclose “[s]ignificantly optimized multi-stage networks, useful in wide target applications” where the “optimized multi-stage networks in each block *employ several rings* of stages of switches with inlet and outlet links.” (Ex. 1001, 3:58-67 (emphasis added).) As discussed below, PO touted this concept of “rings” in the '553 patent family as an important distinction over PO’s earlier patent applications, and, not surprisingly, the claims in the applications to which the '553 patent claims priority (and the originally filed claims in the '470 application itself) all include the “ring” concept. However, these “rings”—which (i) the '553 patent describes as an important aspect of the alleged optimizations to the prior art multi-stage hierarchical networks, and (ii) PO touted as an important distinction over PO’s other applications—are not recited in the claims of the '553 patent. (Ex. 1002, ¶¶33-38.)

First, the '553 patent’s disclosure emphasizes “rings.” Each of figures 1-15 of the '553 patent illustrates, describes, or relates to the use of “rings” in a “multi-stage hierarchical network.” (Ex. 1002, ¶33 (citing Ex. 1001, 4:42-6:22, FIGs. 1-15, 8:56-9:3, 33:26-48).) Annotated Figure 1 of the '553 patent below shows two such “rings”:



(Ex. 1001, FIG.1 (annotated); Ex. 1002, ¶38.) Similarly, the figures that depict example “stages” in the ’553 patent are described as illustrating portions of a “ring.” (Ex. 1001, 4:56-5:3, 5:32-6:6, FIGs. 2A-2E, 9A-11C.)

Second, during prosecution of U.S. Application No. 14/199,168 (“the ’168 application”), which issued as U.S. Patent No. 9,374,322 (“the ’322 patent”) (*see supra* Section II.B.2), PO explicitly defined “rings” and argued that the inclusion of such rings was a “key difference[]” with respect to PO’s earlier alleged inventions disclosed in U.S. Patent No. 8,898,611 (“the ’611 patent”).

Current application discloses stages in rings where forward connecting links are feedback into backward connecting links through one or more multiplexers and also backward connecting links are feedback into forward connecting links through one or more multiplexers, where US Patent No. 8,898,611 discloses folded and butterfly fat tree networks where in each stage only forward connecting links are feedback into backward connecting links. . . . This is one of the key differences in the current invention which allows the total number of stages to be made small to route the same hardware circuit benchmark.

(Ex. 1005, 97-98 (emphases added).)

The ring concept disclosed in the current application is not a true ring, the term ring is used in the current invention since in each stage backward connecting links are feedback to forward connecting links and vice versa as opposed to only a U-turn in original multi-stage networks.

(*Id.*, 101; *see also* Ex. 1001, 2:33-38; Ex. 1002, ¶¶39-42.)

The claims of the '322 patent all include this “ring” concept. (Ex. 1035, 47:42-51:3.) Similarly, all of the claims of PCT Application No. PCT/US12/53814 (“the '814 PCT application”) to which the '168 application claims priority also

include this “ring” concept. (Ex. 1006, 79-82 (1:3-4:23).)²) Indeed, the originally filed claims in the ’470 application also include “rings” (Ex. 1004, 286-292) and further include specific limitations consistent with the definition PO provided for a “ring” during prosecution of the ’168 application. (*Id.*, 287 (82:13-18)³; Ex. 1002, ¶¶39-41.)

But in contrast to the originally filed claims in the ’470 application, the issued claims in the ’322 patent, and the claims in the 814 PCT application, new claims 21-40 that were added by amendment during prosecution of the ’470 application and that issued as claims 1-20 in the ’553 patent **do not** include “rings.” (Ex. 1004, 77-84.)⁴ In other words, issued claims 1-20 of the ’553 patent

² The ’814 PCT application as filed had errors in pagination such that the section that includes the claims restarts the pagination at page 1. Therefore, citations to the ’814 PCT application include both a page number for the exhibit as well as the page and line numbers printed on the page identified within the exhibit.

³ When appropriate, citations to the as-filed ’470 application include page and line numbers corresponding to the application.

⁴ While the Examiner noted in an Interview Summary that the newly presented claims would be reviewed for their compliance with 35 U.S.C. § 112, the claims

are missing a feature that is not only highlighted in the specification as an alleged fundamental point of novelty, but was in fact touted by PO as a “key difference[]” between the disclosure of the ’553 patent family and another patent family belonging to PO. (Ex. 1002, ¶42.)

B. Material Incorporated by Reference in the ’553 Patent

The ’553 patent attempts to incorporate by reference a list of more than 20 patents and patent applications. (Ex. 1001, 1:8-2:62; Ex. 1002, ¶37 (citing Exs. 1011-1034).) However, the incorporations by reference of these patents and applications provide no “detailed particularity [regarding] what specific material” they incorporate and do not “clearly indicate where that material is found” in the patents and applications. *Cook Biotech Inc. v. Acell, Inc.*, 460 F. 3d 1365, 1376 (Fed. Cir. 2006); *see also Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018) (“To incorporate material by reference, the host document must identify with detailed particularity what specific material it incorporates and clearly indicate where that material is found in the various documents.”) (internal

were subsequently allowed without any further rejections. (Ex. 1004, 51, 25-32.) The issued claims, however, do not comply with the requirements of 35 U.S.C. § 112, as demonstrated in the concurrently filed PGR petition.

citations and quotation marks omitted). Indeed, even when material is properly incorporated, “[i]t is not sufficient for purposes of the written description requirement of § 112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to the modifications that the inventor might have envisioned, but failed to disclose.” *D Three Enters., LLC v. Sunmodo Corp.*, 890 F.3d 1042, 1050 (Fed. Cir. 2018) (internal citation omitted).

The ’553 patent simply identifies several patents and patent applications and states that the material is incorporated in its entirety without specifying any particular portions of the documents as being relevant. (Ex. 1001, 1:8-2:62) *Cook Biotech Inc.*, 460 F. 3d at 1376; *see also Nautilus, Inc. v. Icon Health & Fitness Inc.*, IPR2017-01408, 2018 WL 6318050, at *20 (PTAB Dec. 3, 2018) (allowing incorporation by reference where the incorporating language provided detail regarding what was disclosed in the incorporated by reference). Moreover, many, if not all, of those incorporated patents and applications also incorporate by reference other patents and applications. (*See, e.g.*, Ex. 1007, 5-6; Ex. 1006, 1-3 (1:5-3:6).) Without providing sufficient particularity such that a POSITA would recognize what is being incorporated by reference, the material incorporated by

reference cannot be relied upon to remedy defects in the '553 patent, such as lack of written description of the claimed subject matter under 35 U.S.C. §112.⁵

Indeed, any such reliance would impermissibly require a POSITA to look at the different embodiments disclosed in the various patents and make unspecified combinations of elements without any guidance as to what should be combined or how such combinations should be accomplished. *D Three Enters., LLC*, 890 F.3d at 1050. Patentees' attempts to show written description support by relying on an unspecified combination of teachings from incorporated material and the disclosure of the patent have repeatedly been rejected. *Nautilus, Inc.*, IPR2017-01408, 2018 WL 6318050 at *20-23 (rejecting PO's attempt to combine teachings from incorporated reference with disclosure of patent-at-issue in an effort to show

⁵ Elsewhere in the specification, the '553 patent describes certain prior art multi-stage networks disclosed in U.S. patents that were previously incorporated by reference. (Ex. 1001, 7:32-8:19.) But that portion of the specification simply notes that the alleged "optimization" techniques disclosed in the '553 patent may be implemented in certain prior art multi-stage networks, i.e., it does not rely on any concepts disclosed in the referenced U.S. patents for purposes of supporting the disclosure of the '553 patent. (*Id.*, 7:32-37.)

written description support for disputed claim limitation, noting that “obviousness is not the standard for written description”); *Purdue Pharma L.P. v. Recro Tech., LLC*, 694 F. App’x 794, 797 (Fed. Cir. 2017) (affirming Board’s finding that claims lack written description support and stating that “[t]o the extent that Purdue contends that a person of skill in the art would isolate and combine aspects from various embodiments in the specifications (including patents incorporated by reference involving a different drug) to obtain the claimed invention [for written description support], Purdue relies upon the wrong test.”); *see also Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) (“It is not sufficient for purposes of the written description requirement of § 112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to modifications that the inventor might have envisioned, but failed to disclose.”); *Ariad Pharms., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc); *Trans Video Elecs., Ltd. v. Sony Elecs., Inc.*, 822 F. Supp. 2d 1020, 1027 (N.D. Cal. 2011).

Therefore, in light of the lack of particularity provided by the limited description of the material incorporated by reference in the ’553 patent, the patents and patent applications incorporated therein should not be considered in determining whether the claims comply with the requirements of 35 U.S.C. § 112.

Moreover, even if considered, the material incorporated by reference cannot cure the deficiencies identified herein. (*See, e.g., infra* Section IX.)

IX. PGR ELIGIBILITY

The PGR provisions of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”) apply to patents subject to the first inventor to file provisions of the AIA, i.e., patents having at least one claim with an effective filing date on or after March 16, 2013. *Grunenthal GmbH v. Antecip Bioventures II LLC*, PGR2018-00001, Paper 17 at 9-10 (May 1, 2018). A claim in a U.S. application is entitled to the benefit of the filing date of an earlier filed U.S. or PCT application if the subject matter of the claim is disclosed in the earlier filed application in accordance with the written description requirement. *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1306 (Fed. Cir. 2008) (subject matter disclosed for first time in a continuation application does not receive benefit of the parent’s filing date); *see also In re Gosteli*, 872 F.2d 1008, 1010–11 (Fed. Cir. 1989).

To comply with the written description requirement, the specification or earlier-filed application “must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed.”

LizardTech, Inc. v. Earth Resource Mapping, Inc., 424 F.3d 1336, 1345 (Fed Cir. 2005); *see also Lockwood*, 107 F.3d at 1572; *Allergan, Inc. v. Sandoz Inc.*, 796 F.3d 1293, 1308-09 (Fed. Cir. 2015). “The test requires an objective inquiry into the four corners of the specification from the perspective” of a POSITA. *Ariad*, 598 F.3d at 1351. Whether the added subject matter is an obvious variant of the disclosed subject matter is irrelevant. *Lockwood*, 107 F.3d at 1572.

The chart above in Section II.B.2 shows that the ’553 patent relates to two applications filed prior to March 16, 2013, namely the ’615 provisional application (Ex. 1007) and the ’814 PCT application (Ex. 1006). The ’553 patent is eligible for PGR because it has at least one claim that is not entitled to the filing date of either the ’615 provisional application or the ’814 PCT application (“the two pre-AIA applications”). In particular, at least claims 1, 2, 4, 9, 11, 12, and 14 of the ’553 patent include subject matter that is not disclosed in the two pre-AIA applications. *PowerOasis, Inc.*, 522 F.3d at 1306; *In re Gosteli*, 872 F.2d at 1010–11. (Ex. 1002, ¶¶52-75.)

Claims 1, 2, 4, 9, 11, 12, and 14 are not entitled to a pre-March 16, 2013 filing date as discussed below, thereby confirming PGR eligibility. (Ex. 1002, ¶52.)

A. The Two Pre-AIA Applications Do Not Support Switches Configurable By a Flip Flop (Claim 9)

Claim 9 of the '553 patent, which depends from claim 1, recites “each switch configurable by an SRAM Cell or a Flash Cell or *a flip-flop*.” (Ex. 1001, 50:31-32 (emphasis added).) A “flip-flop” is never mentioned in the two pre-AIA applications. (*See generally* Exs. 1006-1007.)

The disclosure of the '814 PCT application (including the claims) is limited to describing switches as being configurable by an SRAM Cell or a Flash Cell. (Ex. 1002, ¶53.) For example, the '814 PCT application indicates that in the context of “programmable integrated circuit embodiments,” switches or crosspoints that determine how inlet links and outlet links are connected can be controlled by a “programmable cell.” (Ex. 1006, 75 (75:4-10).) Specifically, the '814 PCT application discloses:

In volatile programmable integrated circuit embodiments the programmable cell may be an *SRAM (Static Random Address Memory) cell*. In non-volatile programmable integrated circuit embodiments the programmable cell may be a *Flash memory cell*.

(*Id.*, 75 (75:23-26) (emphases added).)

In other embodiments all the $d * d$ switches described in the current invention are also implemented using muxes

of different sizes controlled by *SRAM cells* or *flash cells*
etc.

(*Id.*, 76 (76:4-6) (emphasis added); Ex. 1002, ¶53.)

Thus, the '814 PCT application does not disclose the “flip-flop” feature recited in claim 9. (Ex. 1002, ¶54.)

The '615 provisional application does not include any disclosure relating to a “flip-flop” and does not even describe configuring switches using SRAM and Flash cells. (*See generally*, Ex. 1007; Ex. 1002, ¶54.)

Thus, neither of the two pre-AIA applications conveys to a POSITA that the named inventor had possession of the features claimed at the relevant time. Neither mentions a “flip-flop” in any respect, let alone in the context of controlling a switch as recited in issued claim 9.⁶ Indeed, the first appearance of the term

⁶ While the two pre-AIA applications generally purport to incorporate a number of additional patents/patent applications by reference, neither pre-AIA application includes any explanation regarding the relevance of the incorporated material. Thus, as discussed above, Patent Owner cannot rely on such incorporated material in an effort to make up for the lack of disclosure in the as-filed application disclosures. (*Supra* Section VIII.B.) In any event, none of the material

“flip-flop” was in a new claim 29 (which issued as claim 9) added January 8, 2018 during prosecution of the ’470 application. (Ex. 1004, 63, 69 (“2018 January 08”), 80.) Therefore, claim 9 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the ’470 application.⁷ (Ex. 1002, ¶¶55-56.)

B. The Two Pre-AIA Applications Do Not Support Claims 1, 2, 4, 11, 12, and 14

Claim 4 of the ’553 patent depends from claim 2, which in turn depends from claim 1. Similarly, claim 14 depends from claim 12, which in turn depends from claim 11. Each of claims 1, 2, 4, 11, 12, and 14 is not supported by the two pre-AIA applications, as discussed below. (Ex. 1002, ¶¶57-75.)

incorporated by reference supports the claimed “flip-flop” features. (Ex. 1002, ¶55, n.6.)

⁷ The ’168 application, which is a post-AIA application, includes essentially the same disclosure as the ’814 PCT application and the ’470 application. (Ex. 1002, ¶55.) Thus, the ’168 application also does not disclose the “flip-flop” feature. (*Id.*)

Claim 1 of the '553 patent recites in part:

forward connecting links comprising ... zero or more
*cross links connected from a switch in a stage in a
subnetwork to a switch in the same numbered stage in
one or more other subnetworks ...*

backward connecting links comprising ... zero or more
*cross links connected from a switch in a stage in a
subnetwork to a switch in the same numbered stage in
one or more other subnetworks*

(Ex. 1001, 49:27-40 (emphases added).)

To the extent the claims can be understood, claim 1 includes forward and backward connecting links that include *cross links* between switches connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks. (*Id.*) Claim 2 adds that those *cross links* are implemented as vertical links only, or horizontal links only, or both vertical links and horizontal links. (Ex. 1001, 49:41-45.) Claim 4 further limits the *cross links* that are horizontal links to either being of “substantially of equal length in the entire two-dimensional grid of rows and columns” or being “of a *hop length h*” “where $h \geq 0$.” (*Id.*, 49:60-50:2.) Claim 4 also limits the cross links that are vertical links to either being of “substantially of equal length in the entire two-

dimensional grid of rows and columns” or being “of a *hop length v*” “where “ $v \geq 0$.” (*Id.*; Ex. 1002, ¶¶57-58.)

As set forth below, there is no disclosure of “forward connecting links” or “backward connecting links” that are “cross links” “connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks” in the two pre-AIA applications, let alone disclosure of any such links that have the additional features recited in claims 2 and 4. (Ex. 1002, ¶59.)

1. Claim 1

The first appearance of a “*cross link*” “connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks” was on January 8, 2018 when claim 21 (which eventually issued as claim 1) was added during prosecution of the ’470 application. (Ex. 1004, 69 (“2018 January 08”), 77-78; *see also id.*, 61-62; Ex. 1001, 48:62-49:40.) But the two pre-AIA applications do not provide written description support for the “cross links” features of claim 1. (Ex. 1002, ¶¶60-61.)

For example, outside of the Abstract⁸ and the material incorporated by reference⁹ in the specification of the '814 PCT application, the only mention of “cross links” in the specification is in the “Summary of the Invention”:

The optimized multi-stage networks with their VLSI layouts employ shuffle exchange links where outlet links of *cross links from switches in a stage* of a ring in one sub-integrated circuit block *are connected to either inlet links of switches in the another stage* of a ring in another sub-integrated circuit block *or inlet links of switches in the another stage* of a ring in the same sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice-versa.

(Ex. 1006, 5 (5:3-8) (emphases added); Ex. 1002, ¶62.)

⁸ The Abstract’s referral to networks that “employ shuffle exchange links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block” is substantively the same as that contained in the cited portion. (Ex. 1006, Abstract, 5:3-8.)

⁹ See *supra* n.6.

This isolated reference to “cross links” is limited to “cross links” connected “from switches in a stage” to switches in “*another* stage.”¹⁰ The same is true with respect to the “cross links” recited in the claims of the ’814 PCT application, i.e., they recite “cross links connecting from a switch in a stage ... to a switch in *another stage*,” where the cross links in the ’814 PCT application are included in

¹⁰ To the extent that PO argues that “another stage” should be understood broadly such that it encompasses “a same stage” or “a different stage,” such an argument would be inconsistent with the use of the “same” and “another” terms in the ’553 patent and its family. For example, the ’814 PCT application states “another stage of a ring *in the same or another* sub-integrated circuit block” (Ex. 1006, 83 (1:14-15) (emphasis added)), thereby making clear that “another” is used to mean “a different” and not “the same or a different.” The ’814 PCT application further states the cross links “are connected to either inlet links of switches in the another stage of a ring *in another sub-integrated circuit block or* inlet links of switches in the another stage of a ring *in the same sub-integrated circuit block*.” (*Id.*, 5 (5:3-8) (emphases added).) Therefore, PO explicitly distinguishes between “same” and “another” in the context of the sub-integrated circuit blocks in the ’553 patent and its family. (Ex. 1002, ¶63.)

forward and backward connecting links that connect “from switches in lower stage to switches in the *immediate succeeding higher stage*” and “from switches in higher stage to switches in the *immediate preceding lower stage*,” respectively. (Ex. 1006, 80 (2:4-13) (emphasis added).) Thus, the ’814 PCT application does not describe any “cross link” that is “connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks” as recited in claim 1. (Ex. 1002, ¶64.)

Outside of the material incorporated by reference,¹¹ the ’615 provisional application does not include any disclosure relating to a “cross link.” (*See generally* Ex. 1007; Ex. 1002, ¶65.)

Accordingly, claim 1 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the ’470 application.¹² (Ex. 1002, ¶65.)

2. Claim 2

Claim 2 depends from claim 1 and recites “*said cross links* between switches of stages in any two said subnetworks are connected as either vertical links only, or

¹¹ *See supra* n.6.

¹² The ’168 application also does not disclose the “same numbered stage” feature of claim 1. (Ex. 1002, ¶64; *see also supra* n.7.)

horizontal links only, or both vertical links and horizontal links.” (Ex. 1001, 49:41-45.) The first appearance of the above-noted features of claim 2 in conjunction with the “cross links” of claim 1 was in newly added claim 22 (which issued as claim 2) submitted January 8, 2018 during prosecution of the ’470 application. (Ex. 1004, 69 (“2018 January 08”), 79; *see also id.*, 62; Ex. 1001, 49:41-45; Ex. 1002, ¶67.)

As discussed above, no “cross links” having the characteristics recited in claim 1 are disclosed in the two pre-AIA applications. (*See supra* Section IX.B.1.) Thus, assuming the recitation of “said cross links” in claim 2 modifies the “zero or more cross links” recited in claim 1, it logically follows that these pre-AIA applications cannot support such “cross links” as further modified by claim 2. Therefore, claim 2 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the ’470 application.¹³ (Ex. 1002, ¶66.)

¹³ The ’168 application also does not disclose the features of claim 2. (Ex. 1002, ¶66; *see also supra* n.7.)

3. Claim 4

a) The “Substantially of Equal Length” Feature Is Not Supported

Claim 4 depends from claim 2 and recites “said horizontal links between switches in two said stages are *substantially of equal length* and said vertical links between switches in two said stages are *substantially of equal length* in the entire two-dimensional grid of rows and columns.” (Ex. 1001, 49:60-65.) The first appearance of the above-noted features of claim 4 in conjunction with the above-discussed features of claims 1 and 2 was in newly added claim 24 (which issued as claim 4) submitted January 8, 2018 during prosecution of the ’470 application. (Ex. 1004, 69 (“2018 January 08”), 78; *see also id.*, 62; Ex. 1001, 49:60-50:2; Ex. 1002, ¶68.)

As discussed above, no “cross links” as recited in claim 1 or as further limited by claim 2 are disclosed in the two pre-AIA applications. (*See supra* Sections IX.B.1-2.) Thus, assuming the recitation of “said horizontal links” and “said vertical links” in claim 4 further modifies the horizontal and vertical links recited in claim 2, which in turn modify the “zero or more cross links” recited in claim 1, it logically follows that these pre-AIA applications cannot support such “cross links” as further modified by claim 4. Therefore, claim 4 is not entitled to

an effective filing date earlier than the April 28, 2016 filing date of the '470 application.¹⁴ (Ex. 1002, ¶69.)

b) The “Hop Length” Features Are Not Supported

Claim 4 also recites “said horizontal links between switches in two said stages are substantially of a *hop length h* and said vertical links between switches in two said stages are substantially of a *hop length v* where $h \geq 0$ and $v \geq 0$.” (Ex. 1001, 49:60-50:2.) As is the case for the other features recited in claim 4, assuming this feature regarding “hop length” further modifies the “cross links” as recited in claim 1 and further limited by claim 2, no such cross links are disclosed in the two pre-AIA applications. (Ex. 1002, ¶70; *see supra* Section IX.B.1.)

Moreover, as discussed below, the claimed ranges of hop length “ $h \geq 0$ and $v \geq 0$ ” are not supported by the two pre-AIA applications *in any context*. Indeed, prior to the filing of claim 24 during prosecution of the '470 application, there was no recitation of a hop length of “0” and only hop lengths ≥ 1 were previously described or claimed. (Ex. 1002, ¶71.)

¹⁴ The '168 application does not disclose the features of claim 4. (Ex. 1002, ¶69; *see also supra* n.7.)

The first appearance of a horizontal or vertical “hop length” “ ≥ 0 ” in relation to any link was in claim 24 (now claim 4) submitted January 8th, 2018 during prosecution of the ’470 application. (Ex. 1004, 69 (“2018 January 08”), 79; Ex. 1001, 49:60-50:2.) But the specification of the ’470 application explicitly states that each of the horizontal and vertical hop lengths is a positive number, therefore making a hop length of 0, which is included in the claimed ranges, outside the scope of the disclosure of the ’470 application. (Ex. 1004, 253 (48:14-18) (“‘Vx’ denotes an external vertical hop wire ... with ‘x’ vertical hop length, where ‘x’ is a positive integer.”), 256 (51:10-14) (“‘Hx’ denotes an external horizontal hop wire ... with ‘x’ horizontal hop length where ‘x’ is a positive integer.”); 259 (54:6-8) (“In general the hop length of an external vertical hop wire can be *any positive number*. Similarly, the hop length of an external horizontal hop wire can be *any positive number*.”) (emphases added).) Zero is not a positive number and therefore is not included in the disclosed ranges of hop-length. (Ex. 1002, ¶72.)

The same description of hop lengths being limited to positive numbers is present in the ’814 PCT application (Ex. 1006, 47 (47:1-5), 49 (49:26-30), 52 (52:23-25)) and the ’615 provisional application (Ex. 1007, 35 (31:9-13), 38 (34:5-9), 41 (37:3-5)). None of the applications as filed, including the ’470 application

itself, mentions a “hop length” of “0,” let alone such a hop length in the context of the “cross links” set forth in claim 1. (Ex. 1002, ¶73.)

Accordingly, claim 4 is not entitled to an effective filing date earlier than the April 28, 2016 filing date of the ’470 application.^{15, 16} (Ex. 1002, ¶74.)

4. Claims 11, 12, and 14

Claims 11, 12, and 14 recites features analogous to those discussed above with respect to claims 1, 2, and 4, respectively. For example, just like claim 1, claim 11 recites “zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks.” (Ex. 1001, 51:14-17, 51:25-28; *see also id.*, 49:30-33, 49:37-40.) Similarly, like claim 2, claim 12 recites that “zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks.” (*Id.*, 51:32-36; *see also id.*, 49:41-45.) And claim 14, like claim 4, recites cross links that are horizontal links are of “substantially of equal length in the entire two-dimensional grid of rows and

¹⁵ *See supra* n.6.

¹⁶ The ’168 application does not disclose the features of claim 4. (Ex. 1002, ¶73; *see also supra* n.7.)

columns” or being “of a *hop length h*” “where “ $h \geq 0$.” (*Id.*, 51:51-52:7; *see also id.*, 49:60-50:2.) Claim 14, like claim 4, also recites that cross links that are vertical links are of “substantially of equal length in the entire two-dimensional grid of rows and columns” or being “of a *hop length v*” “where “ $v \geq 0$.” (*Id.*, 51:51-52:7; *see also id.*, 49:60-50:2; Ex. 1002, ¶75.) Thus, for at least the same reasons discussed above, neither of the two pre-AIA applications conveys to a POSITA that the inventor had possession of the above-noted features set forth in claims 11, 12, and 14 at the relevant time.¹⁷ Accordingly, claims 11, 12, and 14 are not entitled to an effective filing date earlier than the April 28, 2016 filing date of the ’470 application.¹⁸ (*Supra* Sections IX.B.1-3; Ex. 1002, ¶75.)

C. AIA Applicability

As discussed above, at least claims 1, 2, 4, 9, 11, 12, and 14 of the ’553 patent include subject matter that is not disclosed by a pre-March-16-2013 application. As such, the ’553 patent is eligible for PGR. Further, because at least claims 1, 2, 4, 9, 11, 12, and 14 are not entitled to a priority date prior to March 16,

¹⁷ *See supra* n.6.

¹⁸ The ’168 application does not disclose the features of claims 11, 12, and 14. (Ex. 1002, ¶75; *see also supra* n.7.)

2013, every claim of the '553 patent is subject to the first-to-file provisions of § 102(a). *See MPEP* at § 2159.02.

X. CLAIM CONSTRUCTION

In a post grant review, claims are construed in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.200(b). In particular, claim terms are generally given their “ordinary and customary meaning,” that is, “the meaning that the term would have to a POSITA in question at the time of the invention, i.e., as the effective filing date of the patent application.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*). In the case that “the specification . . . reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess the inventor’s lexicography governs.” *Id.* at 1316 (internal citation omitted).

The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper 11 at 16 (August 14, 2015). Petitioner submits that for purposes of this proceeding, no term requires construction. (Ex. 1002, ¶51.)

XI. EARLIEST EFFECTIVE FILING DATE OF THE '553 PATENT

As discussed above, the two pre-AIA applications and the post-AIA '168 application do not provide adequate written description support for at least the “*same numbered stage*” feature in independent claims 1 and 11. (*Supra* Sections IX.B.1, IX.B.4.) Claims 2-10 and 12-20 depend from independent claims 1 and 11, and consequently are also not supported by the two pre-AIA applications and the post-AIA '168 application.

Thus, for purposes of this proceeding, the challenged claims are not entitled to an effective filing date any earlier than the April 28, 2016 filing date of the '470 application.

XII. DETAILED EXPLANATION OF THE GROUND

A. Ground 1: *Wong* Anticipates Claims 1-7, 9-15, and 17-19

Wong discloses the features of claims 1-7, 9-15, and 17-19.

1. Claim 1

Wong discloses each and every feature of claim 1. (Ex. 1002, ¶¶92-176.)

a) “A network implemented in a non-transitory medium comprising”

To the extent the preamble is limiting, *Wong* discloses a network implemented in a non-transitory medium. (Ex. 1002, ¶¶92-100.) For example, *Wong* discloses a programmable network (“network”) implemented in a Field

Programmable Gate Array (FPGA) integrated circuit (“non-transitory medium”). (Ex. 1008, 1:14-17, 1:59-61, 4:12-16.) (Ex. 1002, ¶¶92; *see also id.*, ¶¶76-81.)

In particular, *Wong* discloses that “[t]he present invention relates to integrated circuit interconnections and, in particular, to the interconnection architecture of FPGA (Field Programmable Gate Array) integrated circuits.” (Ex. 1008, 1:14-17.) *Wong* further discloses that “FPGAs are integrated circuits whose functionalities are designated by the users of the FPGA” where the “user programs the FPGA (hence the term, ‘field programmable’) to perform the functions desired by the user.” (*Id.*, 1:18-21; Ex. 1002, ¶¶92-94.)

Wong’s programmable networks include a plurality of programmable switches that are arranged in hierarchical levels. (Ex. 1008, 1:61-64, 2:7-8.) Figure 4A of *Wong* shows an 8x8 Benes network that is made up of a plurality of switches 20. (*Id.*, 2:41-43, 5:4-6.)

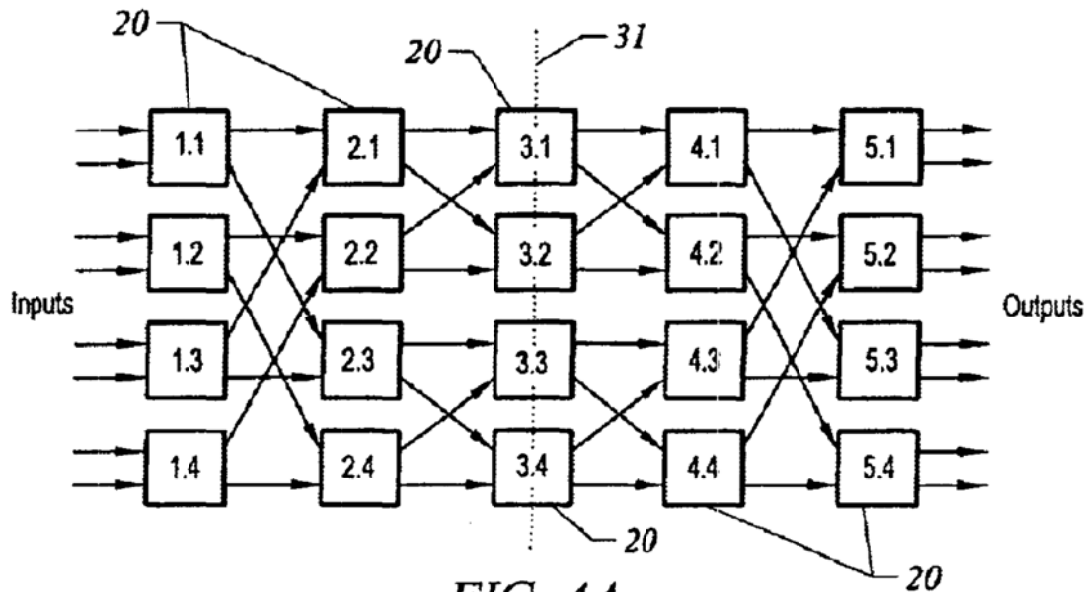


FIG. 4A

(*Id.*, FIG. 4A; Ex. 1002, ¶95.)

The 8x8 network shown in figure 4A can be folded in the middle (along dotted line 31 shown in figure 4A) to produce a folded Benes network, examples of which are shown in figures 4B and 4C. (Ex. 1008, 2:41-46, 6:58-67; Ex. 1002, ¶96.)

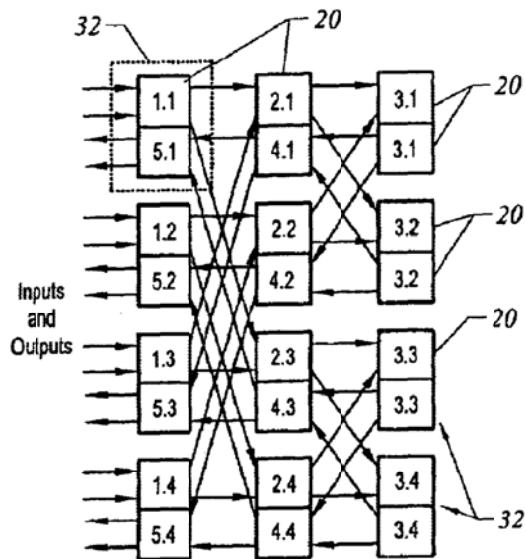


FIG. 4B

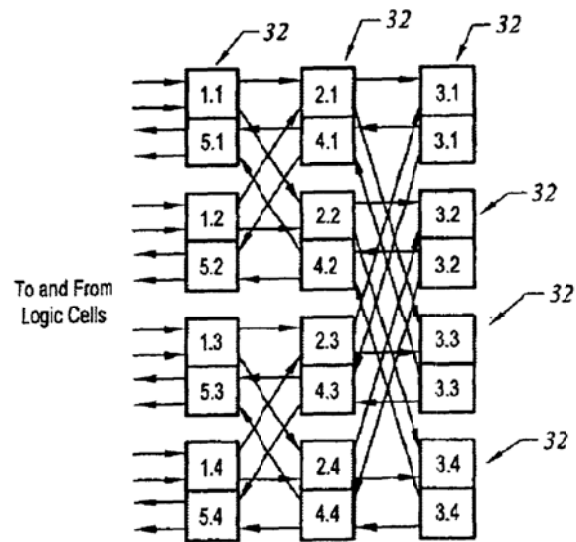


FIG. 4C

(Ex. 1008, FIGs. 4B (left), 4C (right, where the interconnections have been inverted by level); Ex. 1002, ¶96.)

Figures 13A and 13B of *Wong* build on the disclosure corresponding to figure 4C and illustrate exemplary floorplan layouts of FPGAs that use the Benes network topology such as that shown in figure 4C. (Ex. 1008, 3:7-10, FIGs. 13A-13B.) For example, referring to Figure 13A, *Wong* discloses that “[w]ith the previous illustrations of the Benes interconnect network and columns of logic cells added, the layout is nearly completed.” (*Id.*, 13:19-22; Ex. 1002, ¶97.)

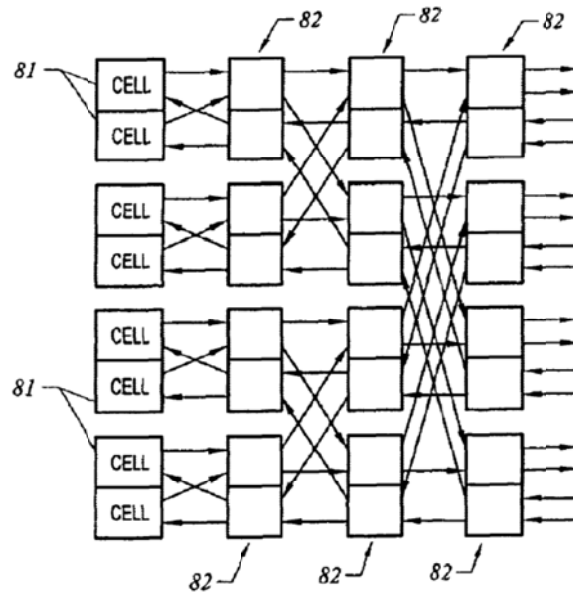


FIG. 13A

(Ex. 1008, FIG. 13A.)

Figure 13B shows a multi-column embodiment that includes two instantiations of the layout shown in figure 13A. (*Id.*, 3:7-10; 13:36-38.)

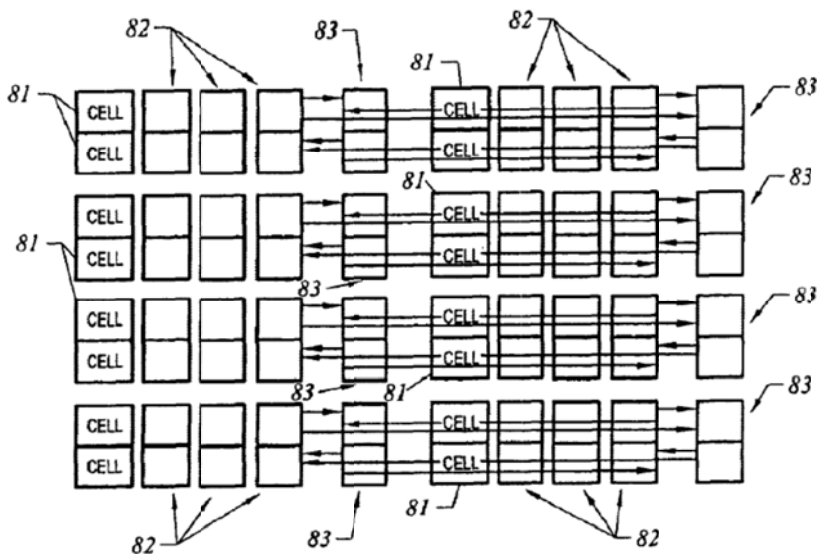


FIG. 13B

(*Id.*, FIG. 13B; Ex. 1002, ¶98.)

In figures 13A and 13B, logic cells 81 are included in the FPGA along with switch cells 82 and 83. (Ex. 1008, 13:22-23, 13:36-38.) An annotated version of Figure 13A below demonstrates one example of the interconnection between the logic cells 81 and the network made up of switches 82.

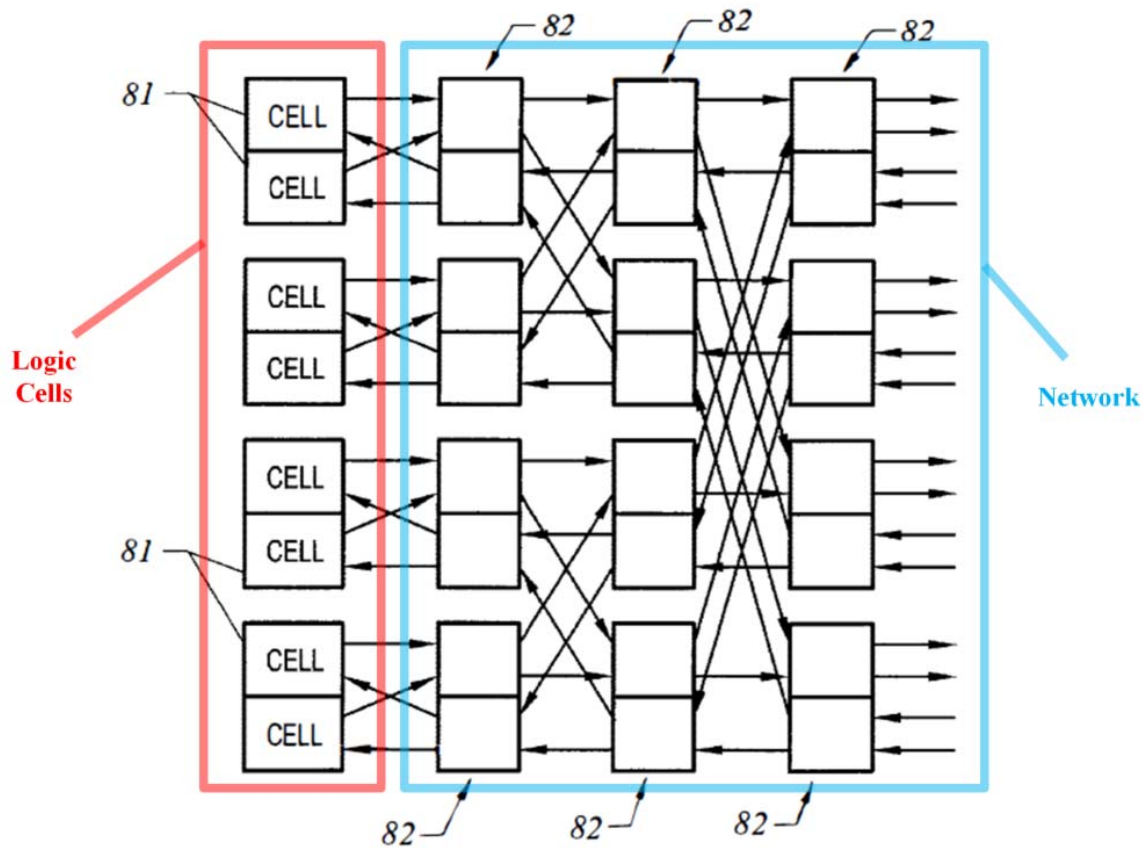
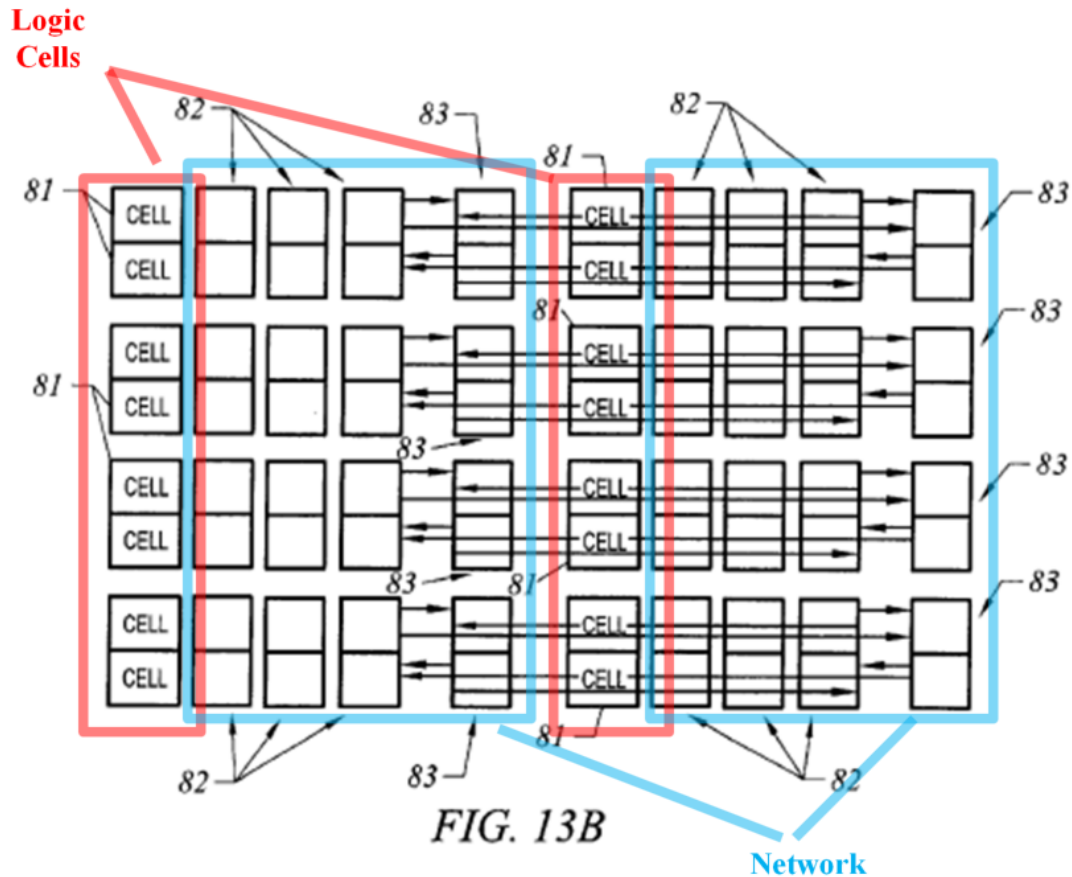


FIG. 13A

(*Id.*, FIG. 13A (annotated); Ex. 1002, ¶99.)

Similarly, an annotated version of Figure 13B of *Wong* below illustrates the interconnection between the logic cells 81 and the network that includes switches 82 and 83.



(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶100.)

Thus, *Wong* discloses a programmable network (“network”) implemented in an FPGA integrated circuit (“non-transitory medium”).

b) “a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links,”

(1) a plurality of subnetworks

Wong discloses a plurality of subnetworks. (Ex. 1002, ¶¶101-102.) For example, *Wong* discloses that the network shown in figure 13A below includes a plurality of rows of switches 82 (“subnetworks”). Similarly, figure 13B of *Wong* includes a plurality of subnetworks. As shown below, each subnetwork in figure 13A includes a row of switches 82, while each subnetwork in figure 13B includes one more switch 83 in addition to the switches 82.

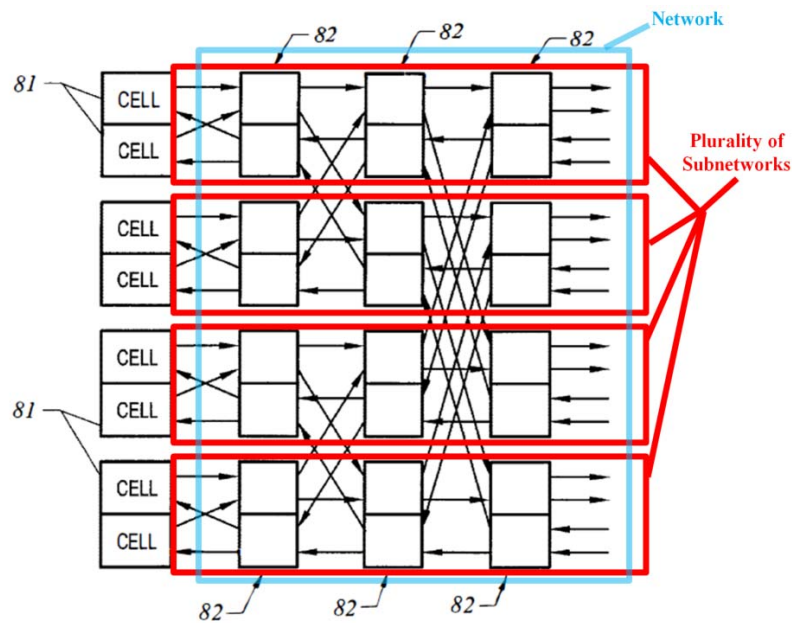
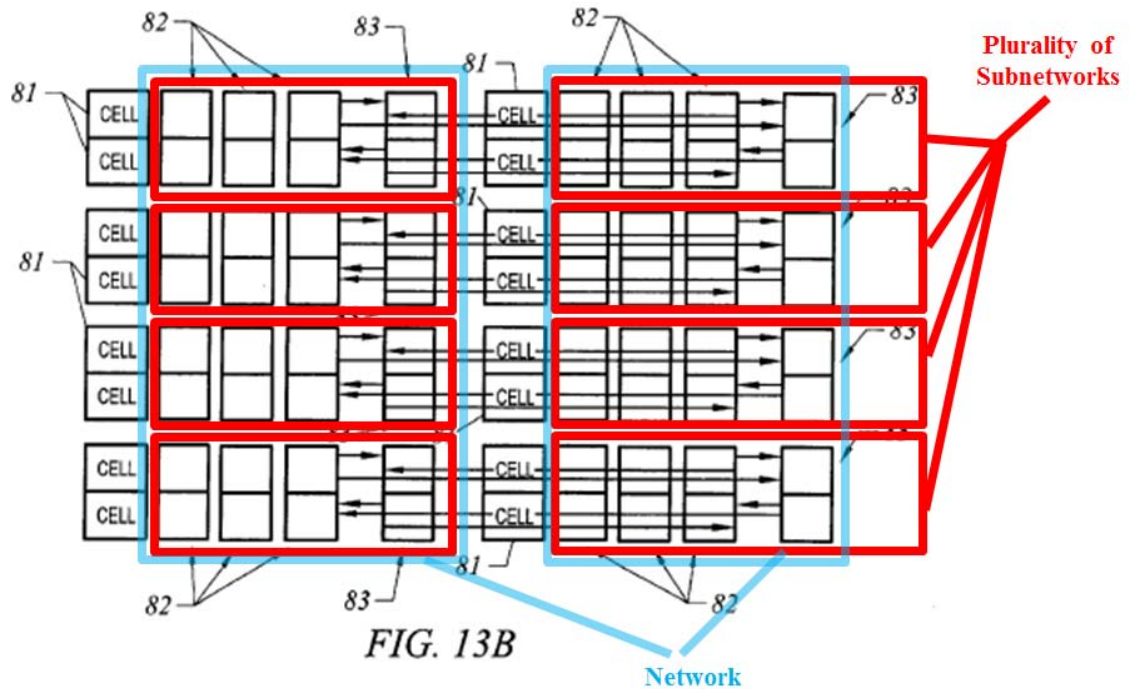


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show a plurality of subnetworks); Ex. 1002, ¶101.)



(Ex. 1008, FIG. 13B (annotated to show plurality of subnetworks); Ex. 1002, ¶102.)

(2) a plurality of inlet links and a plurality of outlet links

Wong discloses a plurality of inlet links and a plurality of outlet links. (Ex. 1002, ¶¶103-109.) For example, as shown below in an annotated version of figure 13A, *Wong* discloses that its above-noted subnetworks include inputs (“plurality of inlet links”) (highlighted in blue) that are coupled to inputs of the switches 82 in the first stage of the network and outputs (“plurality of outlet links”) (highlighted

in green) that are coupled to outputs of the switches 82 in the first stage of the network.

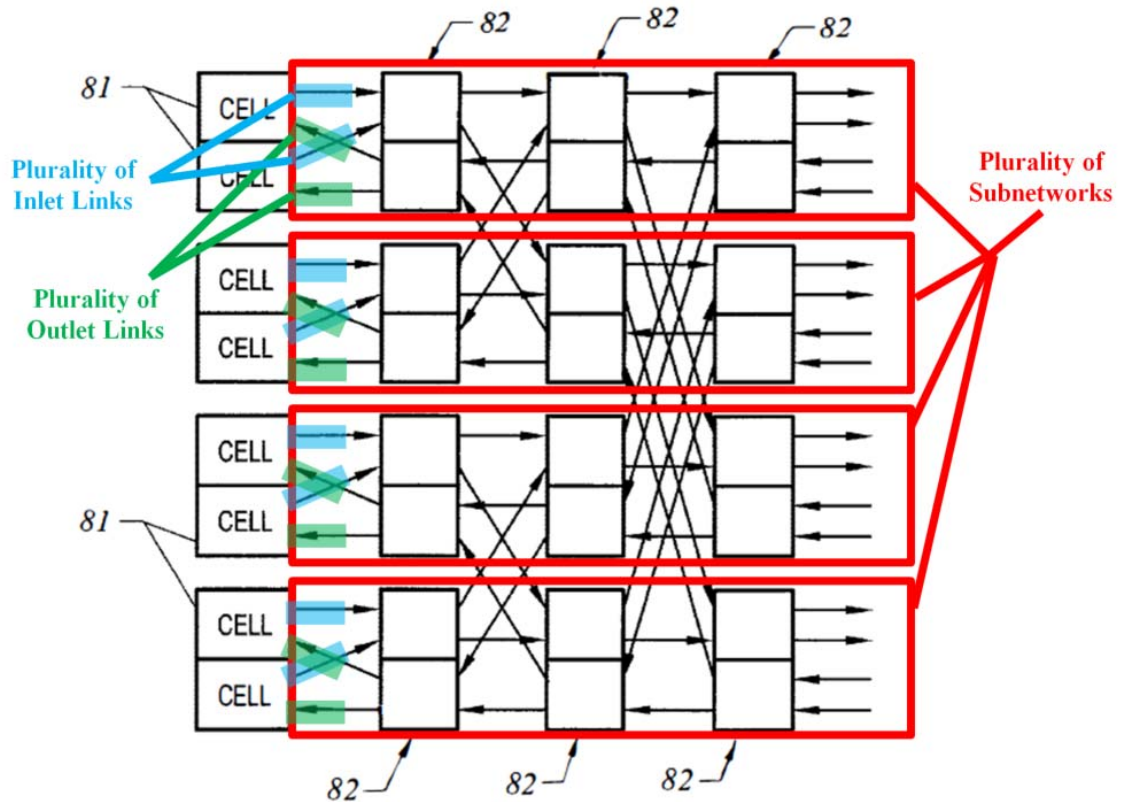


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show inlet links (blue) and outlet links (green));

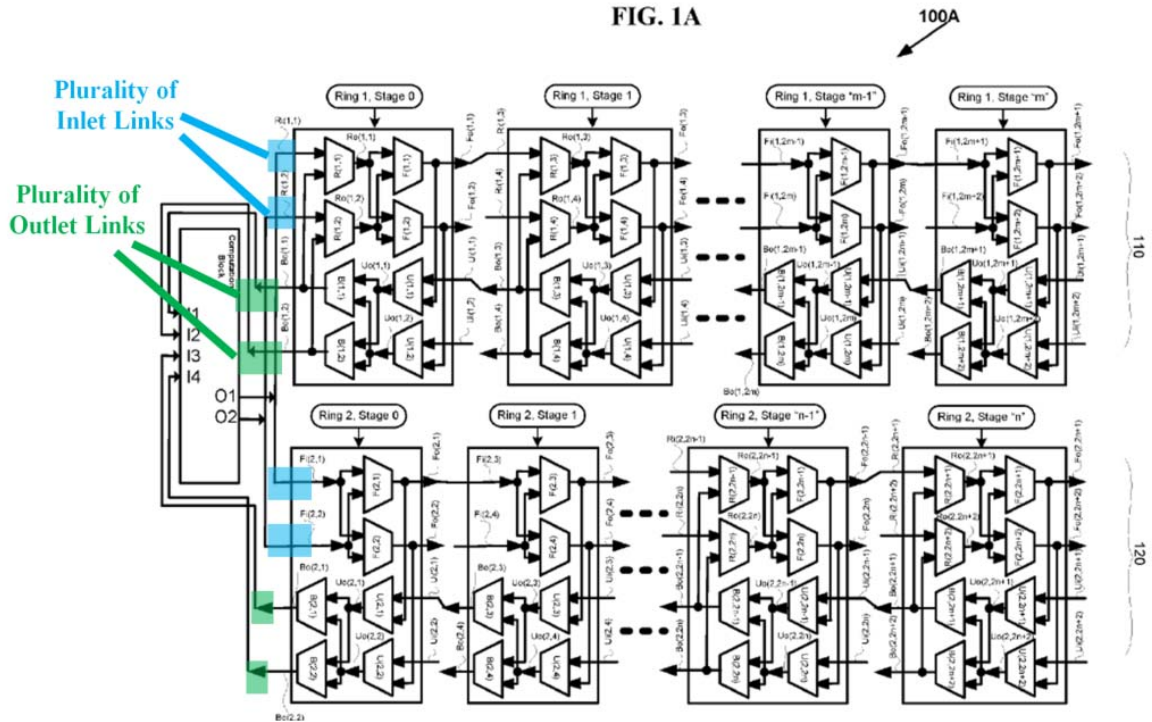
Ex. 1002, ¶103.)¹⁹

¹⁹ The embodiment of figure 13B of *Wong* includes two instantiations of the network shown in figure 13A of *Wong* and therefore includes the same inlet links

Indeed, the inlet links and outlet links in *Wong* are consistent with the disclosure of the '553 patent, which discloses that the outlet links correspond to the outputs of the rings and the inlet links correspond to the inputs of the rings. (Ex. 1001, 9:4-26, FIG. 1A.) Notably, as discussed below with respect to claim element 1[f], the inlet links and outlet links are connected to one or more of said incoming links of a switch in the network, and therefore the highlighted arrows shown in the diagrams of the '553 patent and *Wong* represent both the inlet links of the subnetwork and the incoming links of the switch. (*See infra* Section XII.A.1(f).)

and outlet links shown above with respect to figure 13A. (Ex. 1008, 13:36-38; Ex. 1002, ¶104.)

FIG. 1A



(Ex. 1008, FIG. 1A (annotated to show inlet links (blue) and outlet links (green);
Ex. 1002, ¶104.)

c) “said plurality of subnetworks arranged in a two-dimensional grid of rows and columns; and”

Wong discloses the plurality of subnetworks arranged in a two-dimensional grid of rows and columns. (Ex. 1002, ¶¶110-116.) For example, figures 13A and 13B of *Wong* disclose the “plurality of subnetworks” identified above with respect to claim element 1[b](1), where the plurality of subnetworks are arranged in rows and columns. (*Supra* Section XII.A.1(b)(1); Ex. 1008, FIGs. 13A-13B.)

Figure 13A of *Wong* shows the subnetworks and logic cells arranged in four rows in one column.

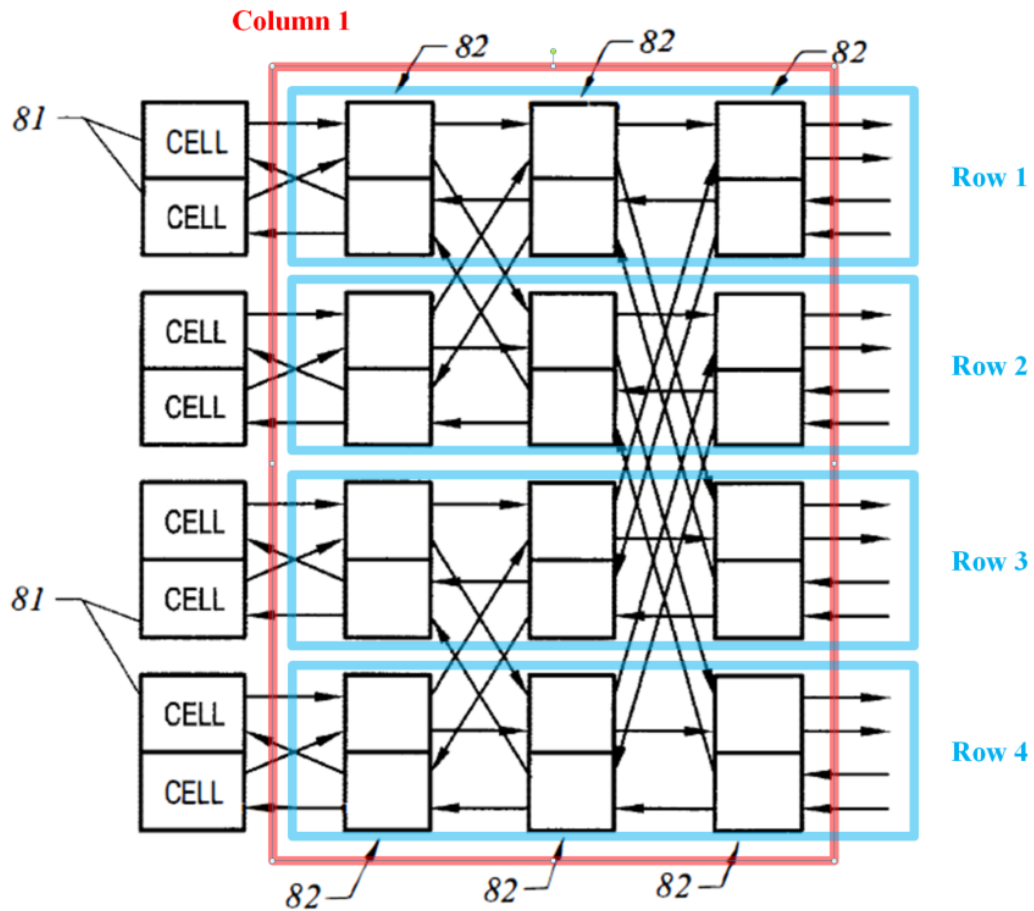


FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶110.)

While the claim recites “a two-dimensional grid of rows and columns,” a POSITA would have understood the claim to encompass a two-dimensional grid where the subnetworks are only laid out in a single dimension (e.g., one row or one column). (Ex. 1002, ¶111.) Such an understanding is supported by claim 10,

which depends from claim 1 and recites “said plurality of subnetworks are implemented in a single dimension.” (Ex. 1001, 50:49-50.) A POSITA would recognize in light of claim 10 that the scope of claim 1 would broadly encompass a two-dimensional grid where the subnetworks are laid out in a single dimension (e.g., one row or one column). (Ex. 1002, ¶111.) Therefore, Figure 13A, which shows subnetworks in multiple rows in a single column, discloses the subject claim element. (*Id.*)

Moreover, *Wong*’s Figure 13B embodiment discloses subnetworks arranged in multiple rows and multiple columns.

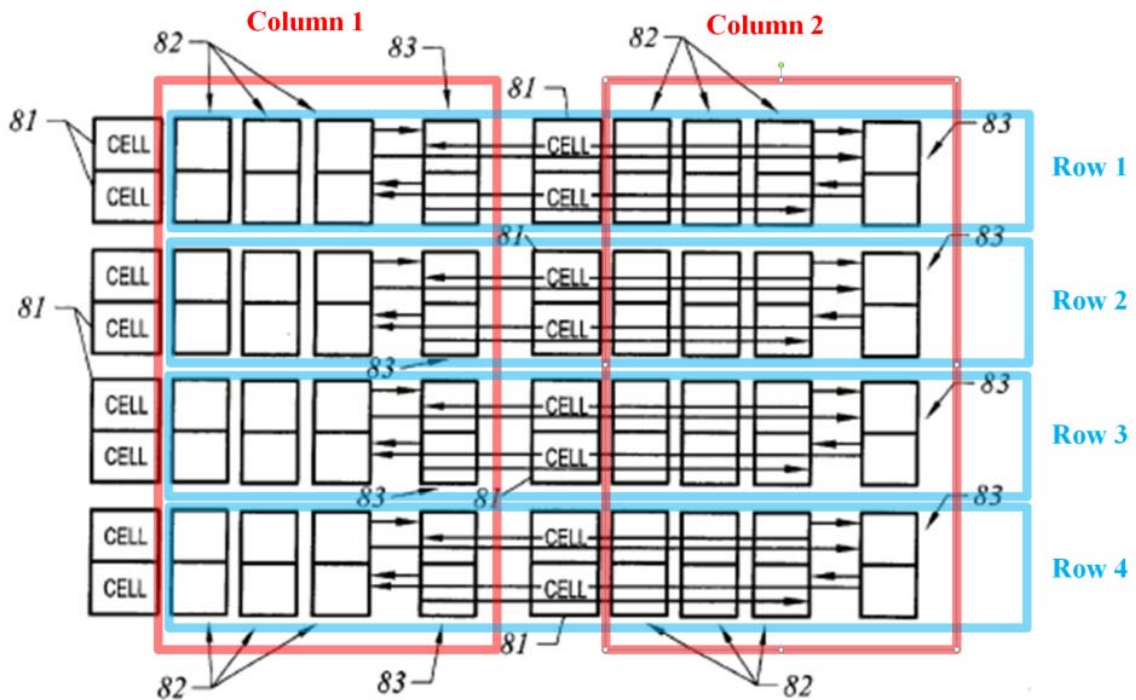


FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶112.)

As shown, Figure 13B discloses an embodiment with subnetworks arranged in four rows and two columns. (Ex. 1008, 13:36-38; *see also id.*, 3:7-10; Ex. 1002, ¶113.) *Wong* also discloses further expansion of the network in both the column and row directions. (Ex. 1002, ¶114 (citing Ex. 1008, 13:38-40, 13:44-46).)

To the extent Patent Owner argues that that the “two-dimensional grid of rows and columns” corresponds to a physical layout of the subnetworks on an integrated circuit, *Wong*’s subnetworks in figures 13A-13B satisfy such a

requirement as they correspond to the physical arrangement of the subnetworks on the integrated circuit. (Ex. 1008, 13:13-16, 13:19-22; Ex. 1002, ¶¶115-116.)

d) “each subnetwork comprising $y \geq 1$ stages, where $y \geq 1$; and”

Wong discloses each subnetwork comprising y stages, where $y \geq 1$. (Ex. 1002, ¶¶117-119.) For example, figures 13A and 13B of *Wong* disclose that each of the “plurality of subnetworks” identified above with respect to claim element 1[b](1) includes three or four stages (i.e., $y \geq 1$). (*Supra* Section XII.A.1(b)(1); Ex. 1008, FIGs. 13A-13B; Ex. 1002, ¶¶117-118.)

For example, in Figure 13A of *Wong*, each subnetwork includes three stages (each switch 82 corresponds to a “stage”).

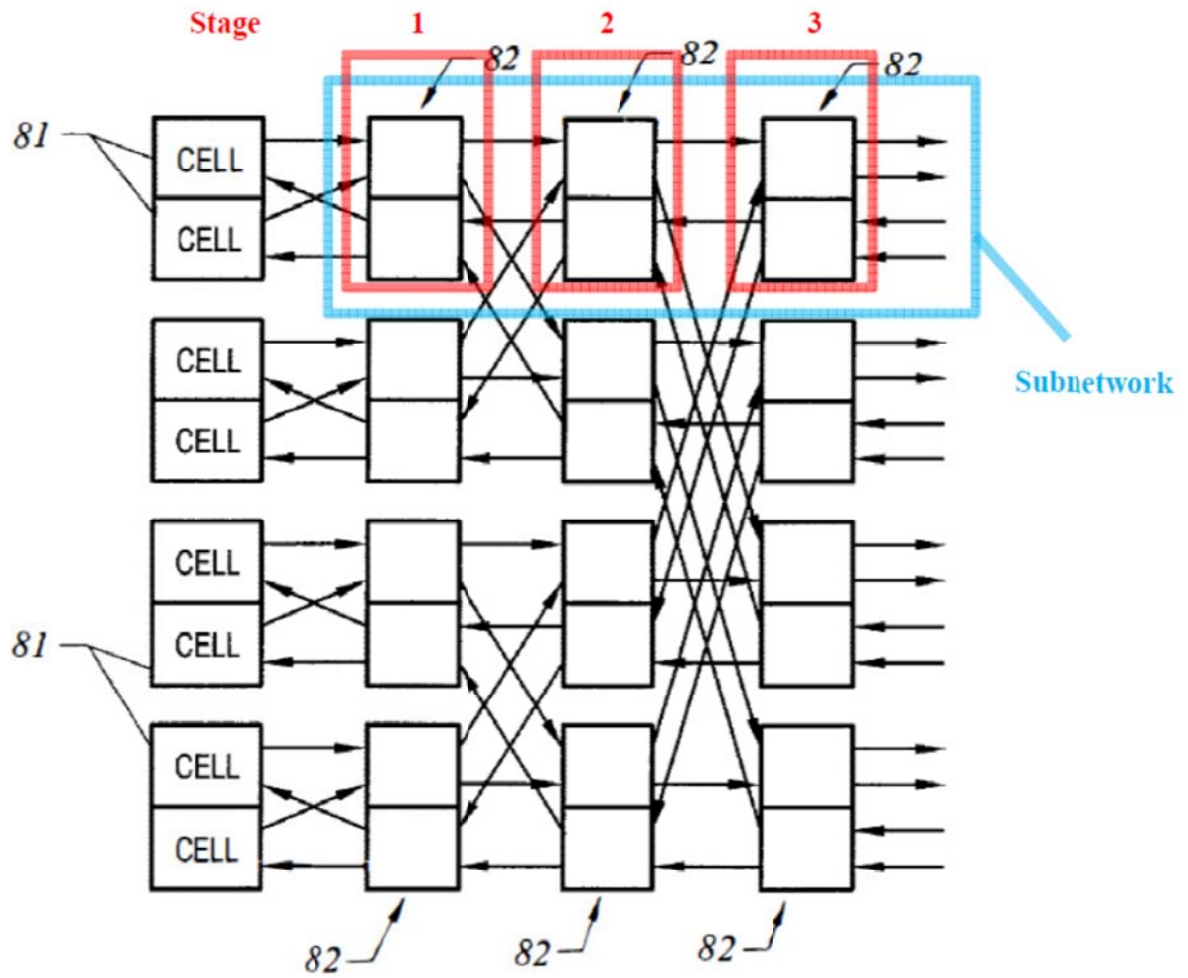


FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶117.)

Similarly, as shown in Figure 13B, each subnetwork includes four stages.

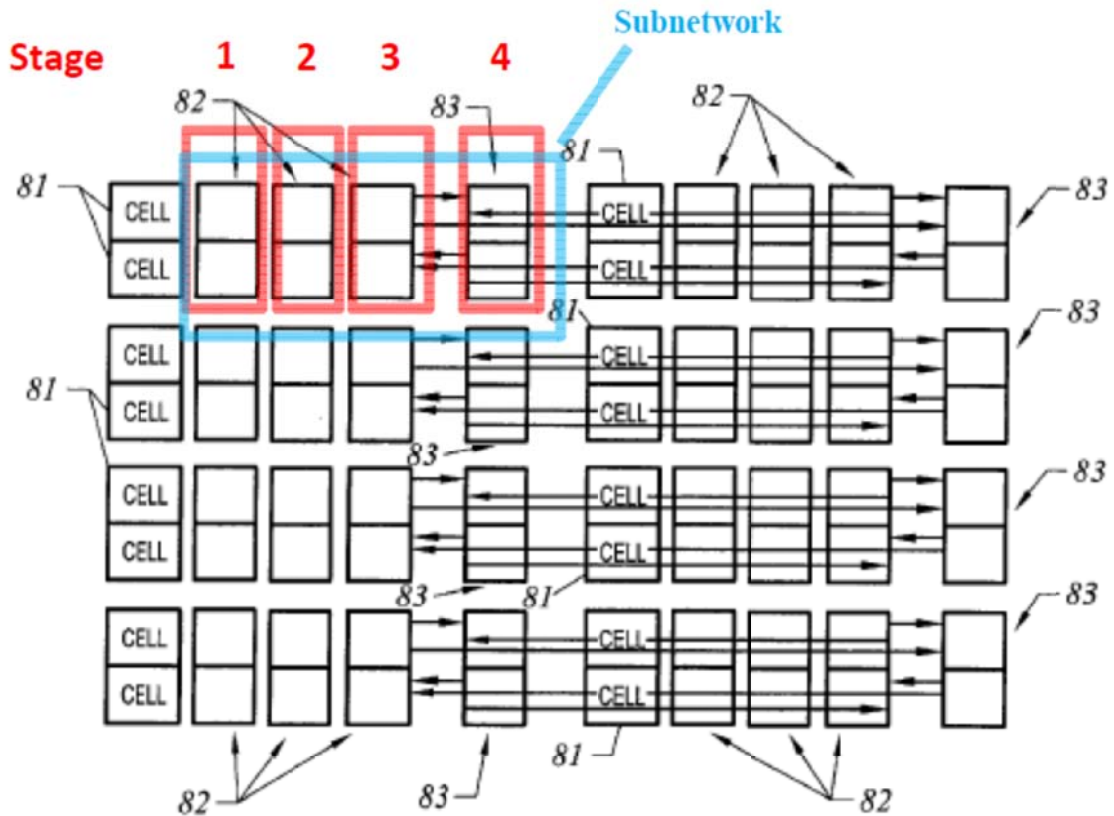
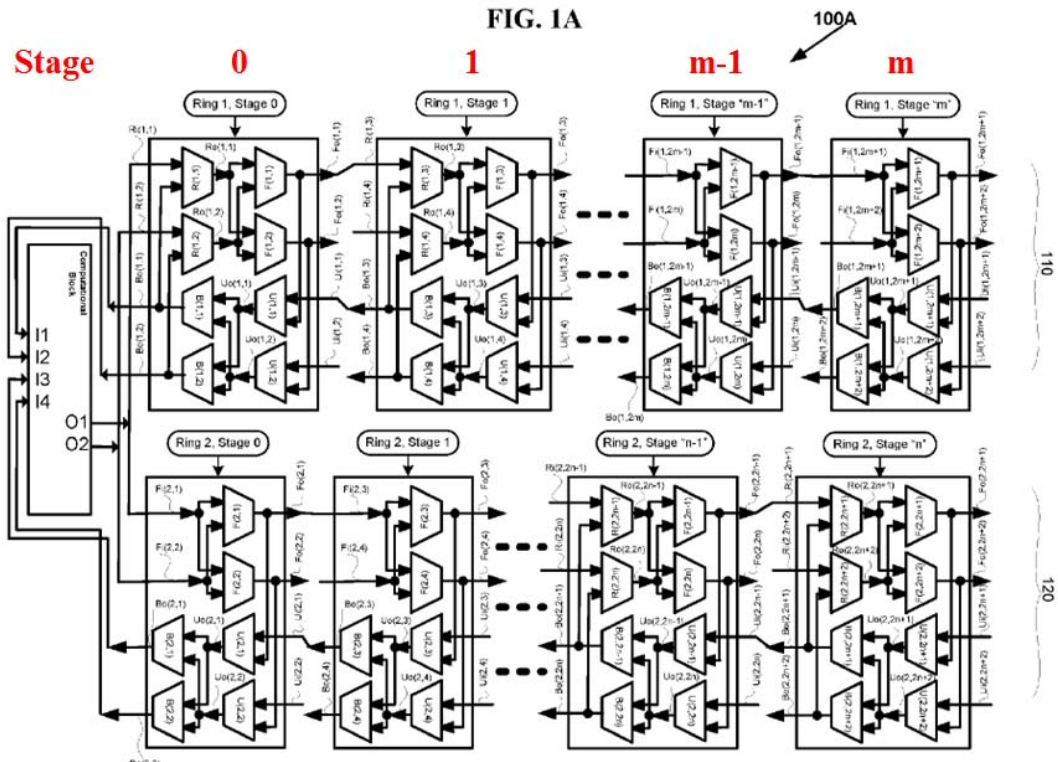


FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶118.)

Indeed, *Wong*'s disclosure of the subnetworks including a plurality of stages is consistent with the disclosure of the '553 patent, which discloses a "partial multi-stage hierarchical network" where each ring (e.g., rings 110 and 120) consists of $m+1$ or $n+1$ stages, where "m" and "n" are positive integers. (Ex. 1001, 8:57-9:3; Ex. 1002, ¶119.)



(Ex. 1001, FIG. 1A (annotated); Ex. 1002, ¶119.)

- e) “each stage comprising a switch of size $d_i \times d_o$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_o$ having d_i incoming links and d_o outgoing links; and”

Wong discloses this claim element. (Ex. 1002, ¶¶120-128.) As an initial matter, a POSITA would have understood this claim element to require that each stage includes a switch that has at least two incoming links and at least two outgoing links (e.g., at least a 2x2 switch with at least two inputs and two outputs). (Ex. 1002, ¶¶120-121.) This is because in the relevant art of integrated circuits, “a switch of size $d_i \times d_o$ ” in the context of “where $d_i \geq 2$ and $d_o \geq 2$ and each switch of

size $d_i \times d_o$ having d_i incoming links and d_o outgoing links” would have informed a POSITA about the input/output configuration of the switch, and not the actual area (i.e. physical size) of the switch. (*Id.*) As explained below, in the embodiments shown in figures 13A and 13B of *Wong*, each stage includes a switch that is 2x2 or larger, and therefore, *Wong* discloses this claim element.

First, as discussed above and illustrated below, each stage of *Wong*’s subnetworks of figures 13A-13B includes a switch (e.g., switch 82 or 83). (*Supra* Sections XII.A.1(b)(1),(d).)

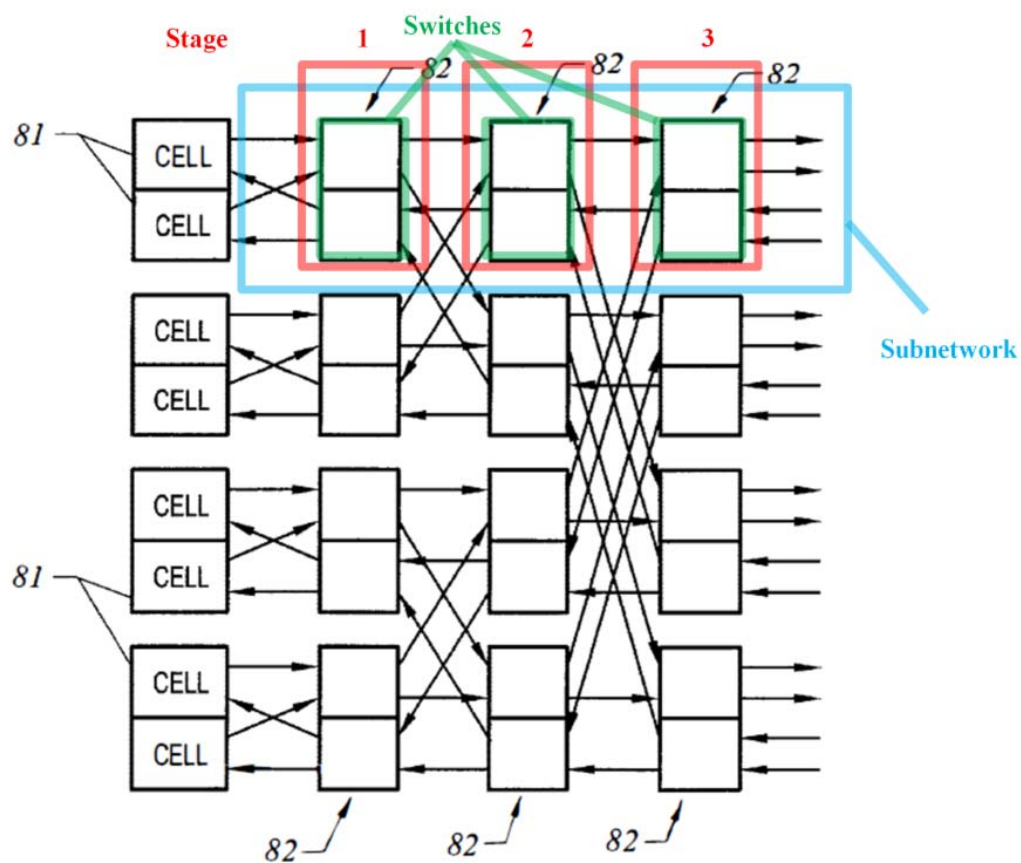


FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶122.)

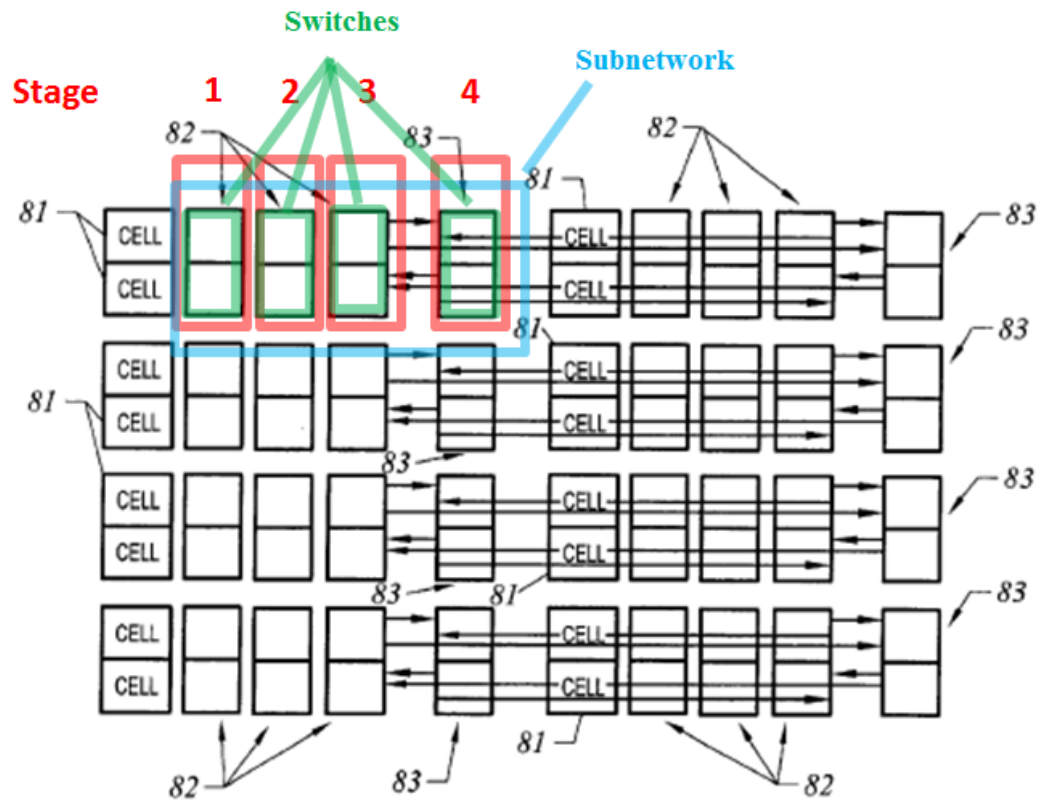


FIG. 13B

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶123.)

Each of the switches 82, 83 shown in figures 13A and 13B of *Wong* is at least a 2x2 switch that has at least 2 inputs and 2 outputs. (Ex. 1002, ¶124.) For instance, as shown in the annotated versions of figure 13A of *Wong* below, each switch cell 82 in each of stages 1-3 includes four inputs (“ d_i incoming links”) and four outputs (“ d_o outgoing links”).

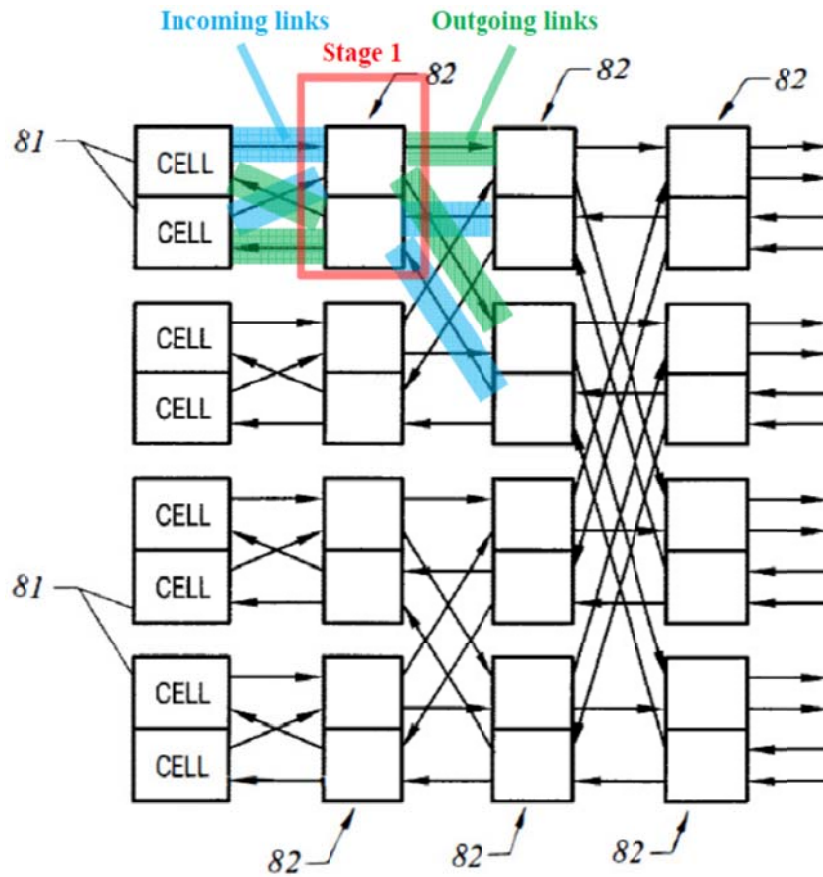


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show incoming links (blue) and outgoing links (green) for stage 1); Ex. 1002, ¶125.)

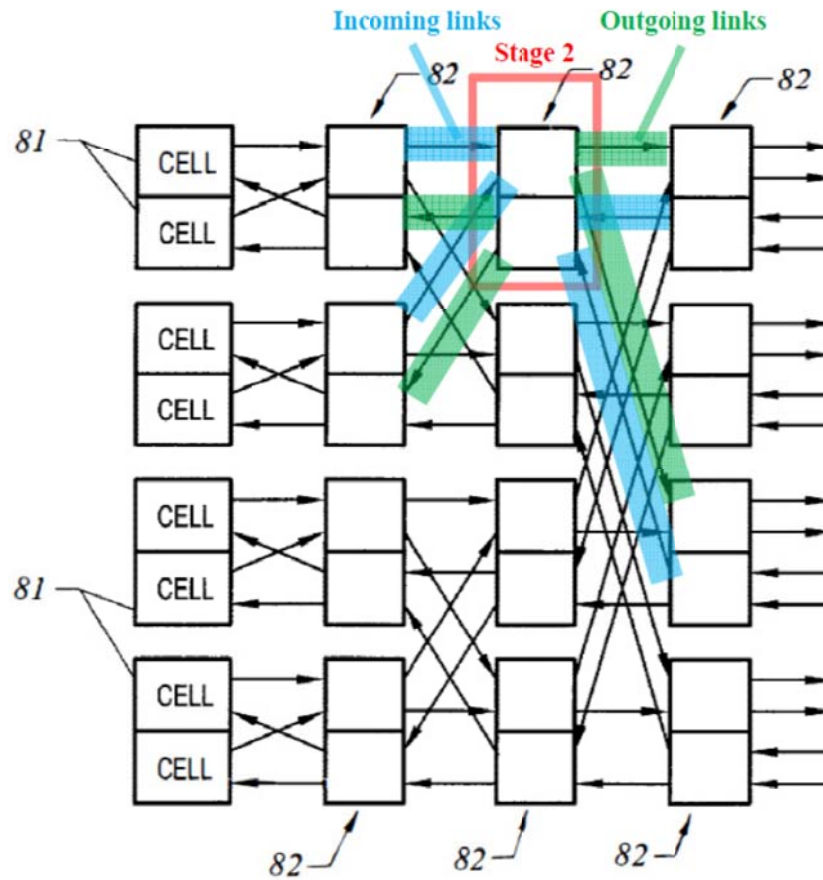


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show incoming links (blue) and outgoing links (green) for stage 2); Ex. 1002, ¶125.)

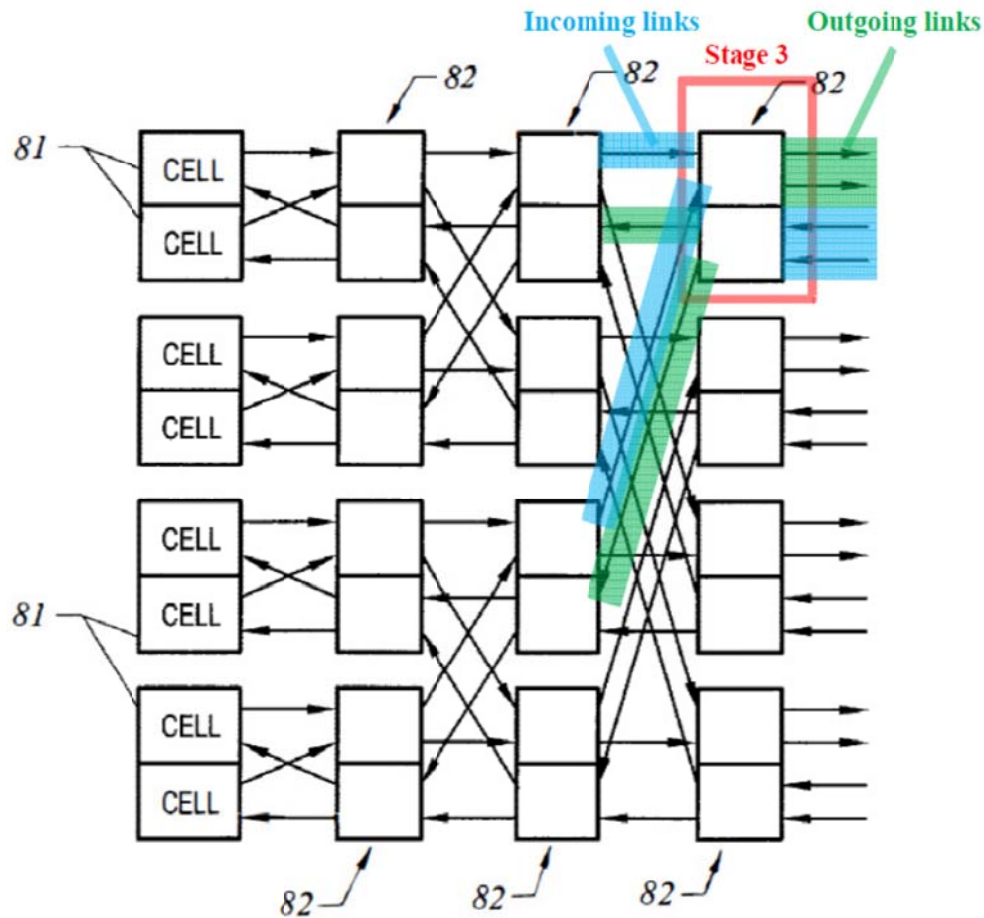
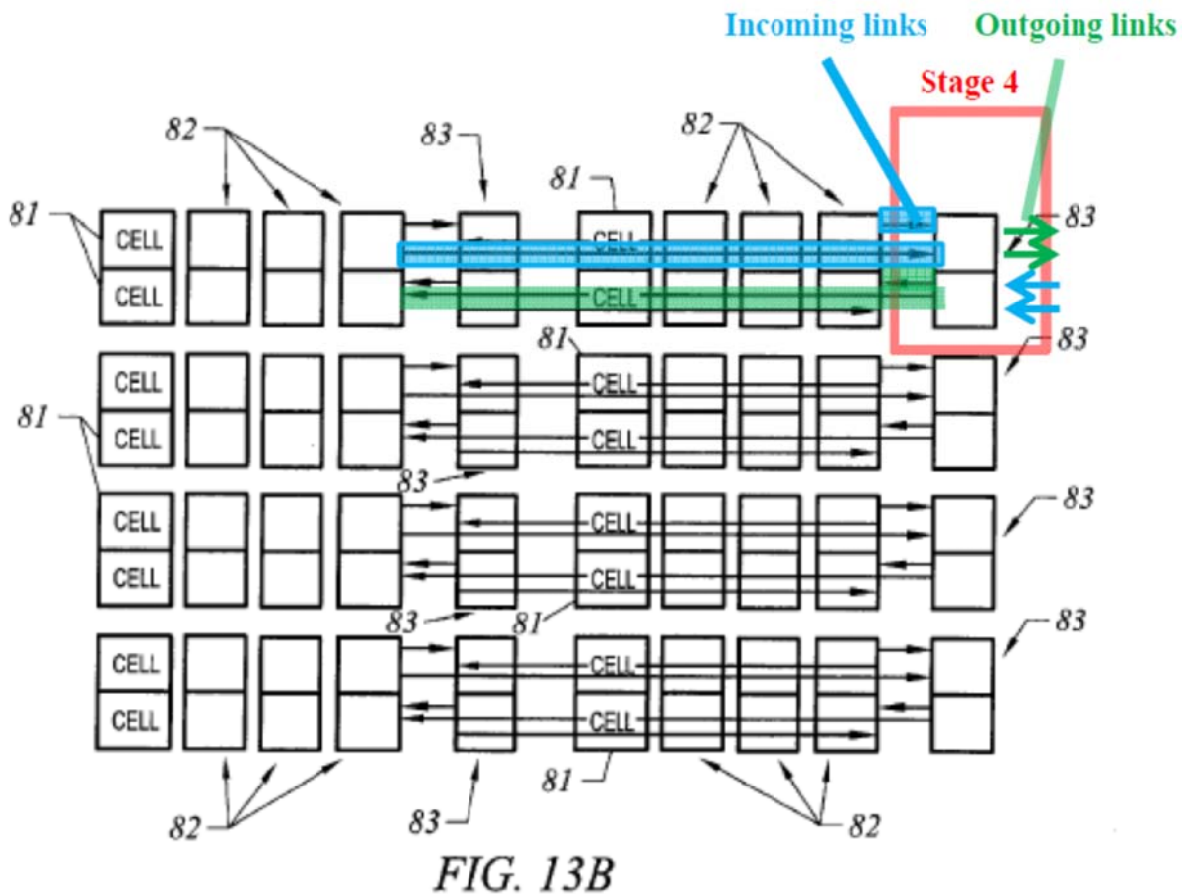


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show incoming links (blue) and outgoing links (green) for stage 3); Ex. 1002, ¶125.)

Similarly, each switch in each of stages 1-4 of the subnetworks shown in figure 13B has four incoming links and four outgoing links as figure 13B includes two instantiations of figure 13A with the addition of another stage of switches 83. (Ex. 1008, 3:7-10; 13:36-38; Ex. 1002, ¶126.)



(Ex. 1008, FIG. 13B (annotated to show incoming links (blue) and outgoing links (green) for stage 4); Ex. 1002, ¶126.)²⁰

²⁰ The annotations add the incoming links and outgoing links corresponding to the primary I/O of the FPGA in Figure 13B (shown as blue and green arrows to the right of switch 83). (Ex. 1008, 13:42-43.) As such, switches 83 are also 4x4 switches that have four incoming links and four outgoing links. (Ex. 1002, ¶127.)

Furthermore, a POSITA would have understood that the 4x4 switches shown in figures 13A and 13B can be made up of sets of 2x2 switches such as those shown in figures 2A and 2B of *Wong* or can be a combined switch such as that shown in figure 7. (Ex. 1008, 5:4-6 (“The building block of the described Benes network is the 2x2 (2 input, 2 output) switch 20, having operations illustrated in FIGS. 2A and 2B.”); 5:4-6, 5:26-29, 7:6-8, 8:10-15, 8:65-9:3, 13:19-22, 13:33-36.)

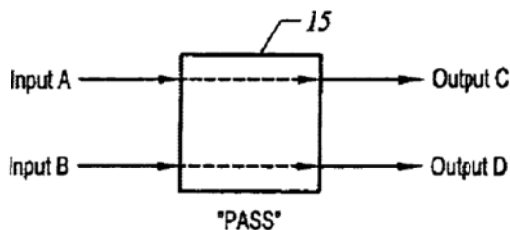


FIG. 2A

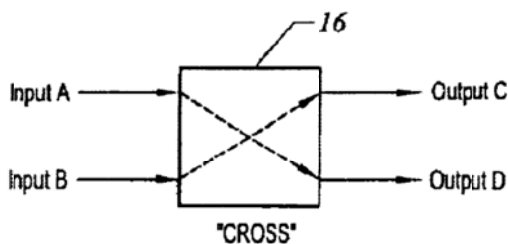


FIG. 2B

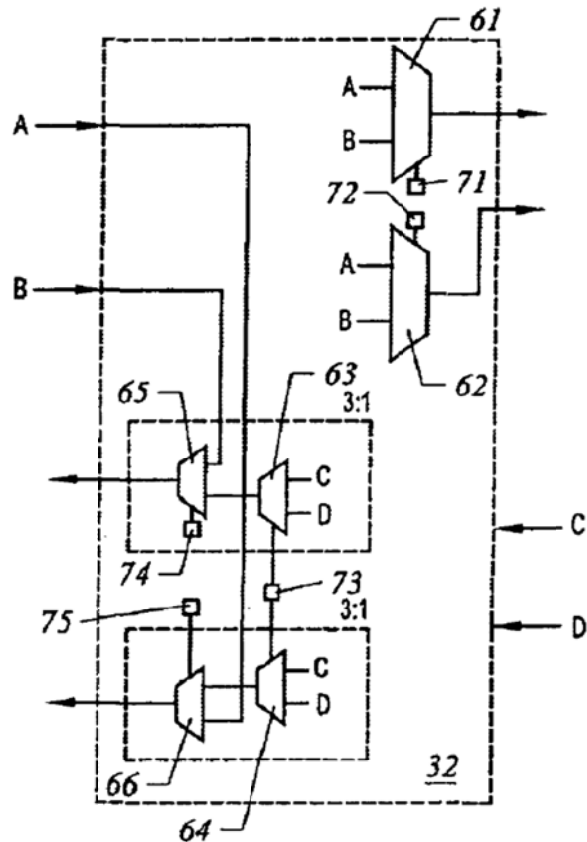


FIG. 7

(*Id.*, FIGs. 2A, 2B, 7; Ex. 1002, ¶128.)

- f) **“Said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork; and”**

To the extent this claim element can be understood by a POSITA, *Wong* discloses the claim element. (Ex. 1002, ¶¶129-137.) For example, as discussed above, the inlet links correspond to the inputs to the subnetworks and the outlet links correspond to the outputs of the subnetworks in figures 13A-13B of *Wong*. (*Supra* Section XII.A.1(b)(2).)

As shown in annotated Figure 13A of *Wong* below, the inlet links corresponding to the inputs of the subnetworks are each connected to a corresponding incoming link of a switch 82 in the first stage of a subnetwork.

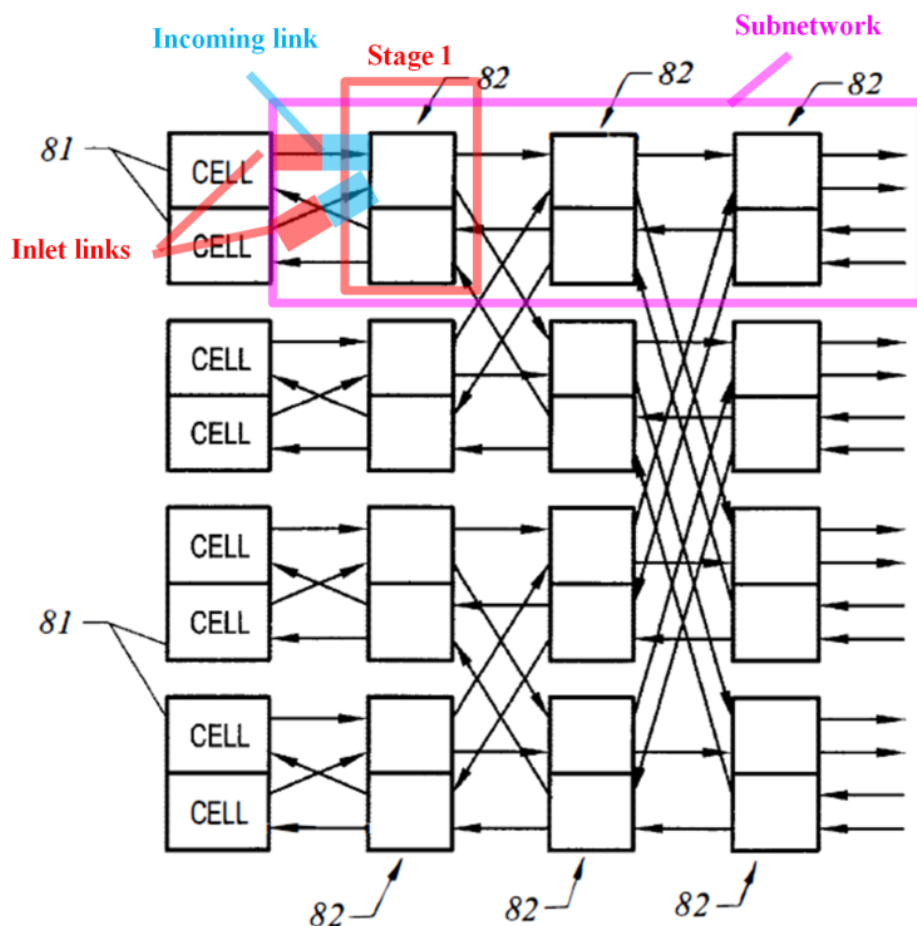


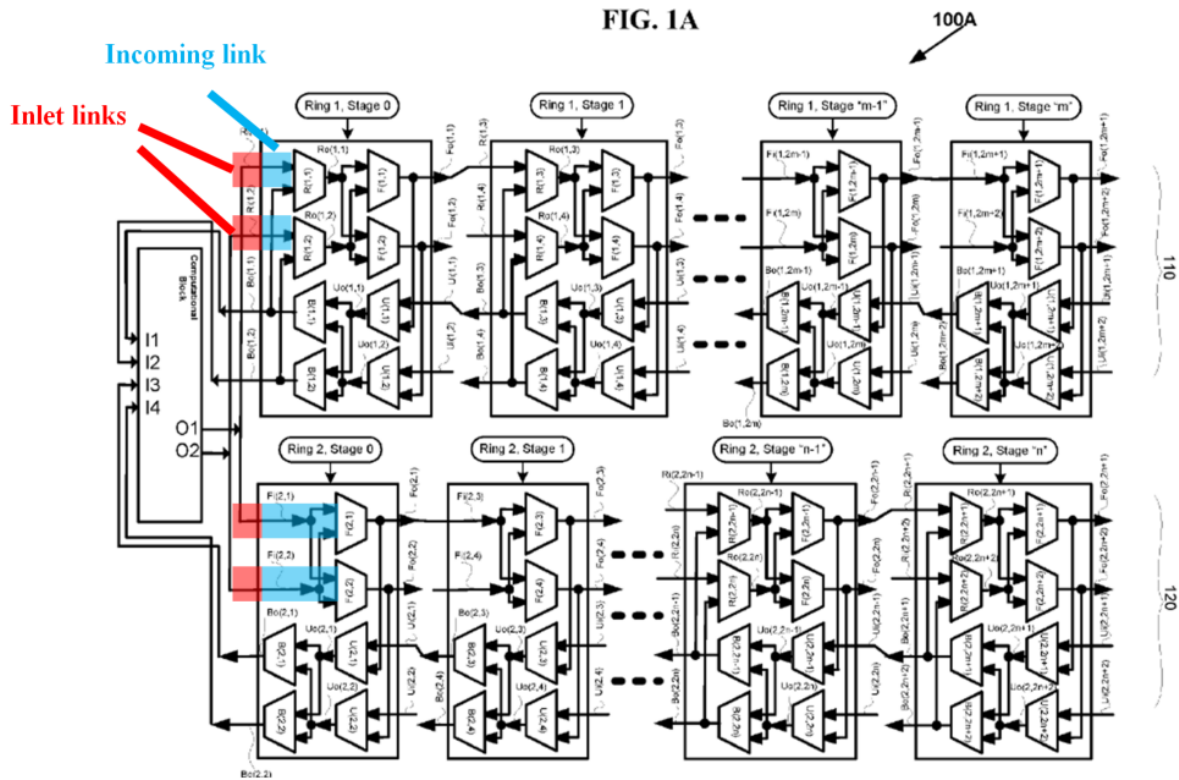
FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶130.)

As shown in annotated figure 1A of the '553 patent below, the “inlet links” connected to the “incoming links” highlighted in figure 13A of *Wong* above are

consistent with the “inlet links” connected to the “incoming links” disclosed by the ’553 patent. (Ex.1002, ¶131.)²¹

²¹ To the extent Patent Owner argues or the Board determines that the inlet links and outlet links are not included in the subnetworks, which is inconsistent with claim element 1[g](1), *Wong* provides the same disclosure as would be relied upon to support the inlet links and outlet links outside of the subnetwork in the ’553 patent. For example, if Patent Owner argues that the “inlet links” correspond to the outputs (O1 and O2) of the computational block and the “outlet links” correspond to the inputs (I1-I4) shown on the left side of figure 1A of the ’553 patent, *Wong* discloses the logic cells 81 have similar outputs and inputs that would constitute inlet links and outlet links. (Ex.1002, ¶136-137.)



(Ex. 1001, FIG. 1A (annotated); Ex. 1002, ¶131.)

Similarly, as shown in figure 13A of *Wong*, the outlet links corresponding to the outputs of the subnetworks are each connected to a corresponding outgoing link of a switch in the first stage of a subnetwork of the network.

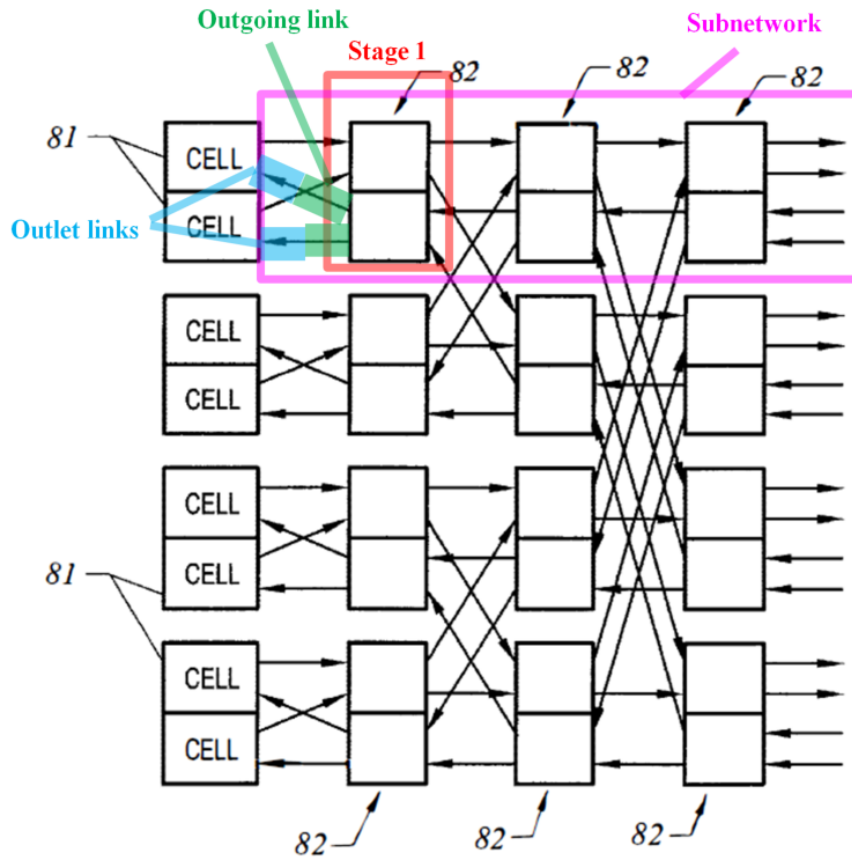
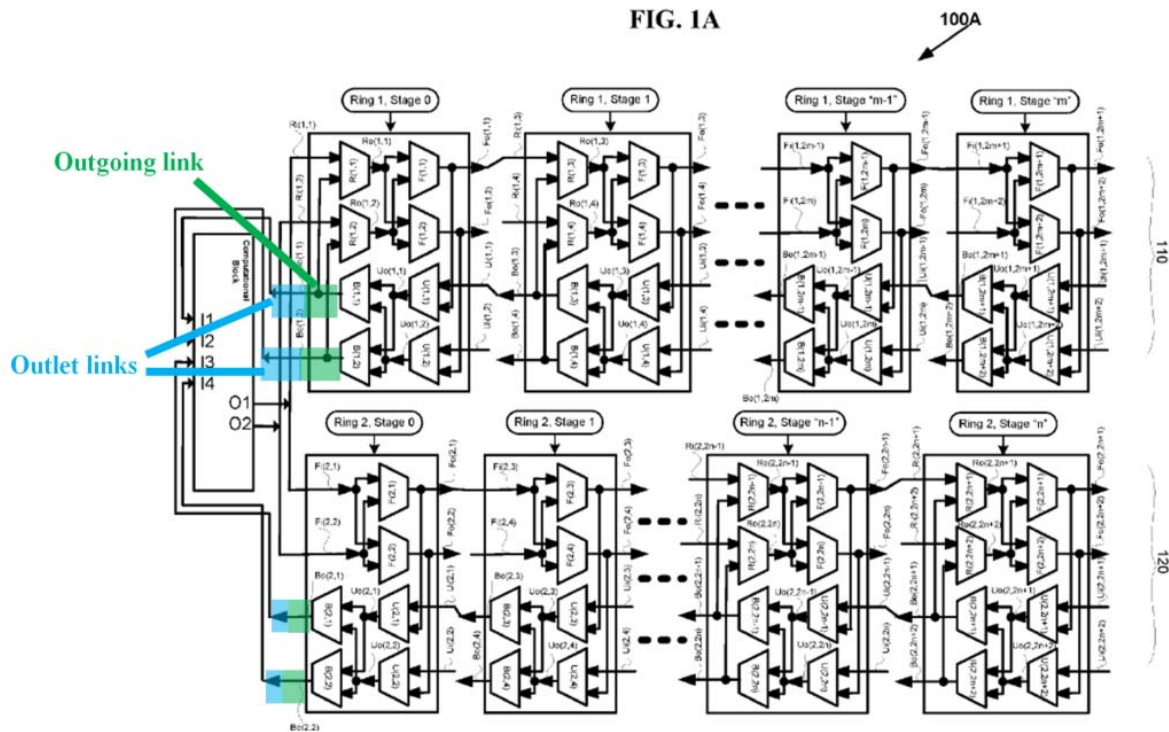


FIG. 13A

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶132.)

As shown in annotated figure 1A of the '553 patent below, the “outlet links” connected to the “outgoing links” highlighted in figure 13A of *Wong* above are consistent with the “outlet links” connected to the “outgoing links” disclosed by the '553 patent. (Ex.1002, ¶133.)



(Ex. 1001, FIG. 1A (annotated); Ex. 1002, ¶133.)

While not explicitly shown in figure 13B, a POSITA would have understood that the connections between the logic cells and first-stage switches of the subnetworks are also present since figure 13B includes two instantiations of the circuitry and connections shown in figure 13A. (Ex. 1008, 13:36-38; Ex. 1002, ¶134.)

As demonstrated above, in the embodiments shown in figure 13A and 13B of *Wong*, each inlet link in the plurality of inlet links is coupled to an incoming link of a switch in the first stage of a subnetwork, and each outlet link in the plurality of

outlet links is coupled to an outgoing link of a switch in the first stage of a subnetwork. (Ex. 1002, ¶135.) Therefore, to the extent this claim feature can be understood, *Wong* discloses “said inlet links connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork.” (*Id.*)

- g) **“each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said inlet links and may or may not be comprising the same number of said outlet links; each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said stages; each stage may or may not be comprising the same number of switches; and each switch in each stage may or may not be of the same size, each multiplexer in each stage may or may not be of the same size and”**

Wong discloses this claim element. (Ex 1002, ¶¶138-151.) As an initial matter, this entire claim element does not further limit claim 1 because it simply recites several optional features. *MPHJ Tech. Invs., LLC v. Ricoh Ams. Corp.*, 847 F.3d 1363, 1379 (Fed. Cir. 2017) (“As a matter of linguistic precision, optional elements do not narrow the claim because they can always be omitted.”) (citing *In re Johnston*, 435 F.3d 1381, 1384 (Fed. Cir. 2006)). As discussed separately below, since each subpart of claim element 1[g] imposes an optional “may or may

not be” feature onto the network components such as number of inlet/outlet links, number of stages, number of switches, etc., *Wong* discloses this claim element regardless of the optional features imposed thereon. (Ex. 1002, ¶¶138-151.)

- (1) each subnetwork of the plurality of subnetworks *may or may not be comprising* the same number of said inlet links and *may or may not be comprising* the same number of said outlet links;**

Wong discloses claim element 1[g](1) as long as it discloses that each subnetwork of the plurality of subnetworks has some inlet links and some outlet links, since the claim does not require that each of the subnetworks have the “same number” of inlet and/or outlet links. (Ex. 1002, ¶139.) And since it has already been shown above that each subnetwork includes inlet and outlet links, *Wong* discloses this claim element. (*Supra* Section XII.A.1(b)(2).) Indeed, *Wong* discloses that its subnetworks in figures 13A-13B include the same number of inlet and outlet links. (Ex. 1002, ¶140.)

- (2) each subnetwork of the plurality of subnetworks *may or may not be comprising* the same number of said stages;**

Similarly, *Wong* discloses claim element 1[g](2) as long as it discloses that each subnetwork has a stage, since the claim does not require that each subnetwork have the “same number” of stages. (Ex. 1002, ¶141.) And since it has already

been shown above that each subnetwork includes a stage, *Wong* discloses this claim element. (*Supra* Section XII.A.1(d).) Indeed, *Wong* discloses that its subnetworks in figures 13A-13B include the same number of stages. (Ex. 1002, ¶¶142-143.)

(3) each stage *may or may not be comprising the same number of switches; and*

Similarly, *Wong* discloses claim element 1[g](3) as long as it discloses that each stage has a switch, since the claim does not require that each stage have the “same number” of switches. (Ex. 1002, ¶144.) And since it has already been shown above that each stage includes a switch, *Wong* discloses this claim element. (*Supra* Sections XII.A.1(d)-(e).) Indeed, *Wong* discloses that each stage in figures 13A-13B includes the same number of switches. (Ex. 1002, ¶¶145-146.)

(4) each switch in each stage *may or may not be of the same size,*

Similarly, *Wong* discloses claim element 1[g](4) as long as it discloses a switch in each stage, since the claim does not require that each switch have the “same size.” (Ex. 1002, ¶147.) And since it has already been shown above that *Wong* discloses a switch in each stage, *Wong* discloses this claim element. (*Supra* Section XII.A.1(e).) Indeed, *Wong* discloses that each switch in figures 13A-13B is of the same size. (Ex. 1002, ¶148.)

**(5) each multiplexer in each stage *may or may not*
*be of the same size.***

With respect to claim element 1[g](5), there is no antecedent basis for “each multiplexer.” To the extent the claim element can be understood, this claim feature does not require each stage to include a multiplexer because nowhere in claim 1 is it specified that each stage includes any multiplexers. Therefore, this claim element is disclosed by *Wong*. (Ex. 1002, ¶149.) Claim 1 does not require each stage to include a multiplexer, and therefore *Wong* discloses this claim feature whether or not it discloses each stage including a multiplexer. For example, if there are no multiplexers in the stages, then “each multiplexer in each stage may or may not be of the same size” is true as no multiplexers are present and therefore the further condition applied to those non-existent multiplexers (“may or may not be of the same size”) is also true. If there are multiplexers in each stage, then they are either “of the same size” or they are not, and the additional condition is also satisfied. (*Id.*)

In any event, even assuming the claim requires each stage to include a multiplexer, *Wong* discloses that each of its stages in figures 13A-13B includes a “multiplexer.” (Ex. 1002, ¶150.) While it is irrelevant whether the multiplexer(s) in each stage are of the same size, *Wong* discloses that each of the subnetworks in

figures 13A and 13B includes switches of the same size and further discloses that multiplexers of the same size can be used for switches of the same size. (*Id.*, ¶151.) For at least these reasons, *Wong* discloses each multiplexer in each stage may or may not be of the same size. (Ex. 1002, ¶¶149-151.)

- h) “Said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork; and”**

Wong discloses this claim element. (Ex. 1002, ¶¶152-165.) As an initial matter, a POSITA would have understood this claim element to mean that the incoming and outgoing links (together) for each switch include a plurality of forward connecting links and a plurality of backward connecting links.²² In other words, if a switch has one incoming link that is a forward connecting link and one outgoing link that is a forward connecting link, the claim feature of the incoming and outgoing links for the switch including a plurality of forward connecting links

²² The claim terms “forward connecting links” and “backward connecting links” are not used in the ’553 patent outside of the claims.

would be satisfied. (Ex. 1002, ¶152.) Similarly, if the switch has one incoming link that is a backward connecting link and one outgoing link that is a backward connecting link, the links for that switch would have been understood by a POSITA to include a plurality of backward connecting links. (*Id.*)

Such an interpretation of the claim is consistent with other portions of claim 1 and the recitations in independent claim 11. For example, claim elements 1[i]-1[j] recite what is included in the forward connecting links separately from what is included in the backward connecting links. (*See infra* Sections XII.A.1(i)-(j).) Similarly claim 11 separately recites “said incoming links comprising . . .” and “said outgoing links comprising . . .” (*See infra* Sections XII.A.10(h)-(i).) Thus, claim elements 1[i]-1[j] and claim 11 confirm that the incoming and outgoing links in claim 11 are being further characterized *individually*. In contrast, claim element 1[h] indicates the “incoming and outgoing links in each stage” taken together include a plurality of forward connecting links and a plurality of backward connecting links. (Ex. 1002, ¶153.)

Wong discloses the forward and backward connecting links as recited in claim element 1[h] by way of figures 13A-13B. For example, as illustrated in figure 13A, the incoming links and outgoing links for each switch of each stage include a plurality of forward connecting links.

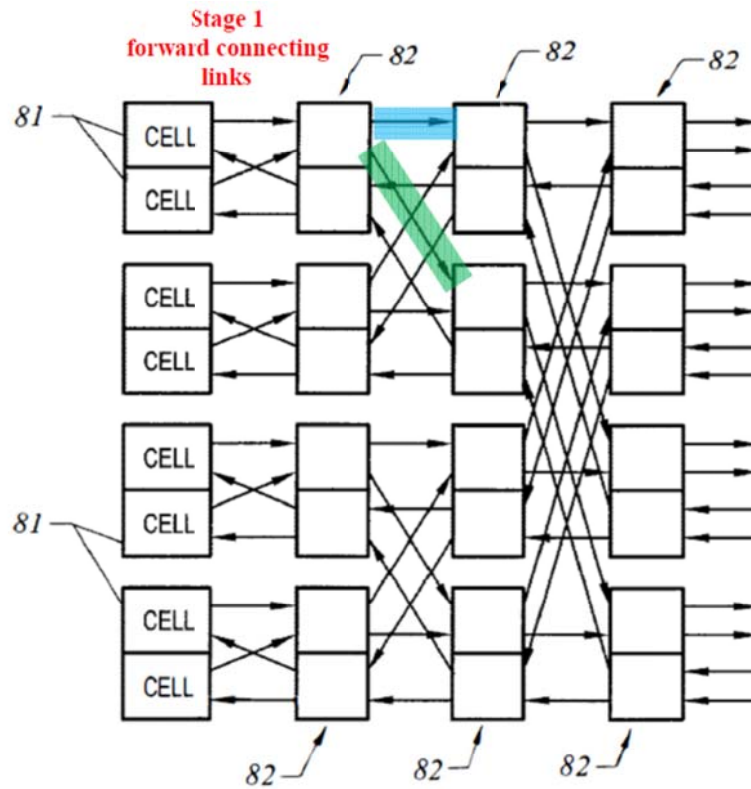


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show forward connecting links (blue and green) for stage 1 of the top subnetwork); Ex. 1002, ¶154.)

The forward connecting links shown in Figure 13A above are connected from a switch in stage 1 (“a stage”) to switches in stage 2 (“another stage in same said subnetwork or another said subnetwork”). For example, the forward connecting link annotated in blue is connected to a switch in another stage in the **same** subnetwork, whereas the forward connecting link annotated in green is connected to a switch in another stage in **another** subnetwork. (Ex. 1002, ¶155.)

Similar annotated versions of figure 13A showing the forward connecting links for stages 2 and 3 are provided below.

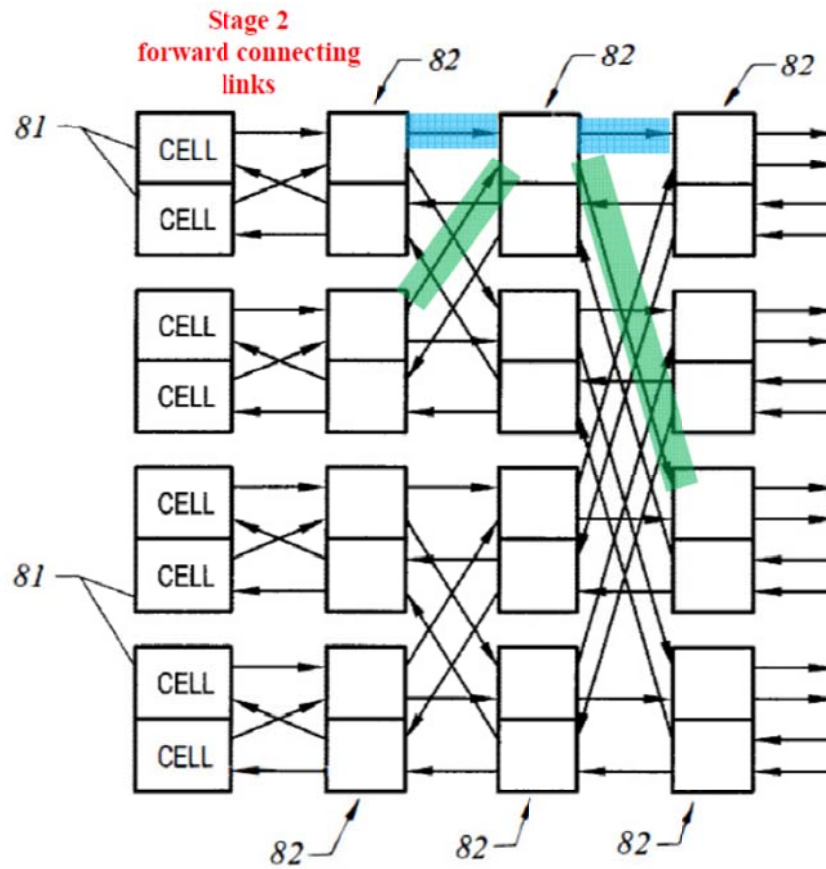


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show forward connecting links (blue and green) for stage 2 of the top subnetwork); Ex. 1002, ¶156.)

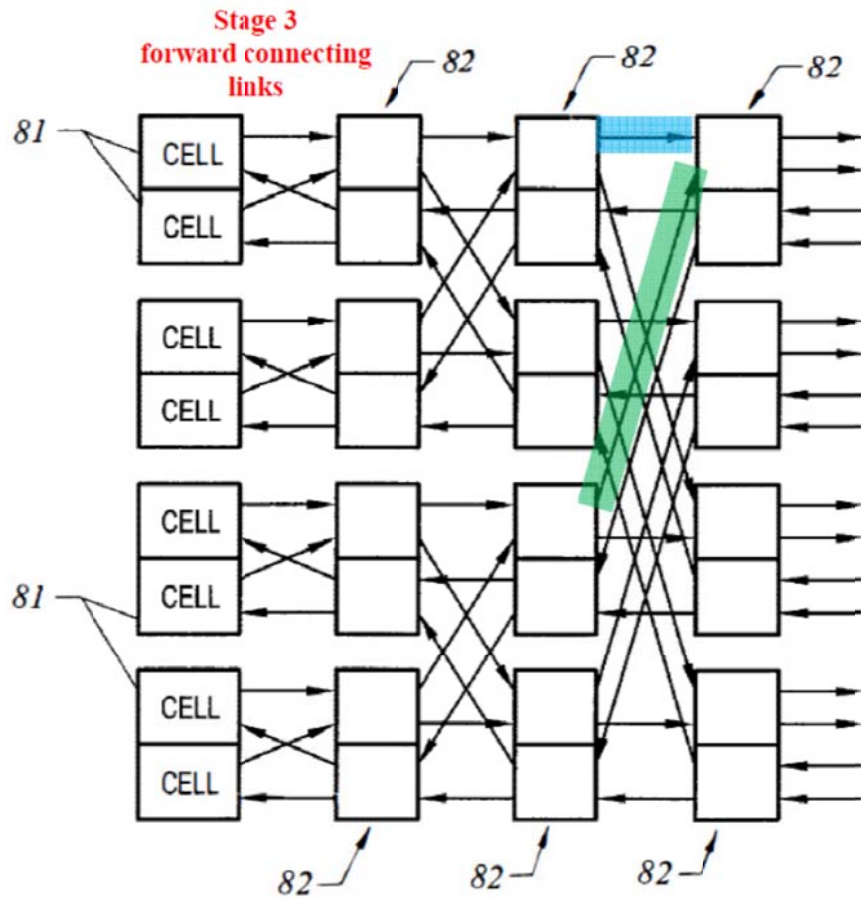
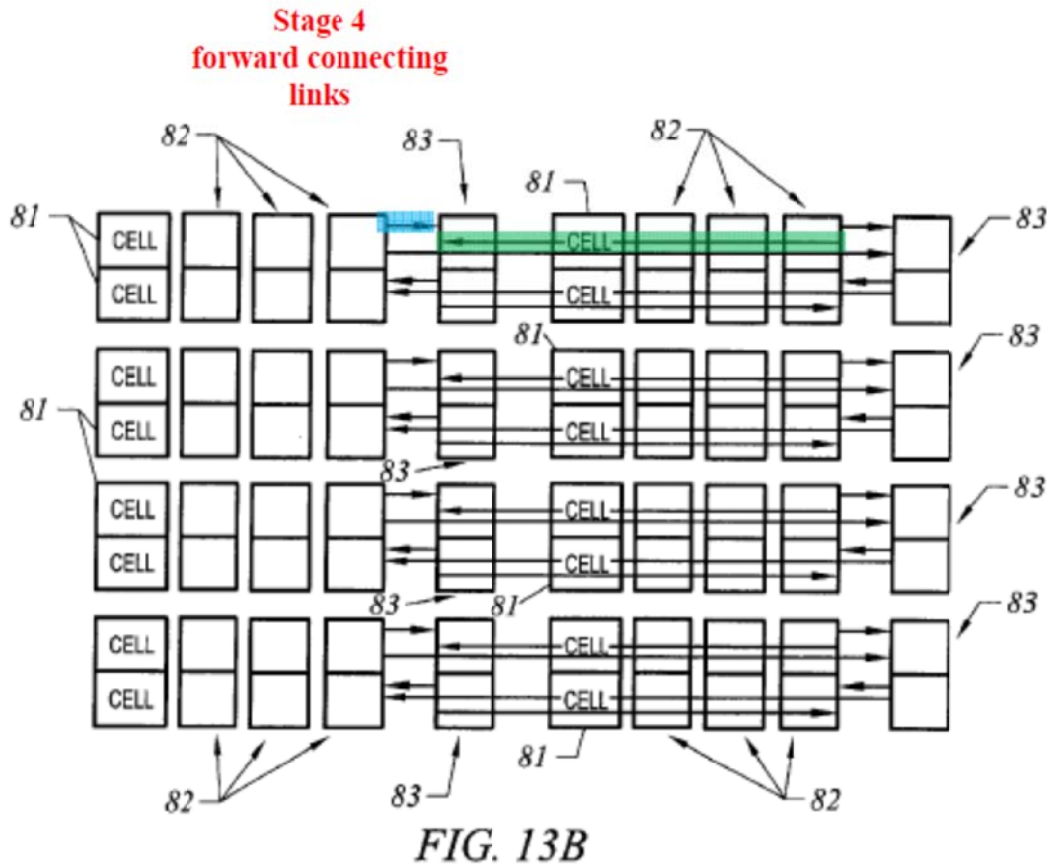


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show forward connecting links (blue and green) for stage 3 of the top subnetwork); Ex. 1002, ¶156.)²³

²³ While the annotated versions of figure 13A above highlight the forward connecting links for the top-most subnetwork, a POSITA would have recognized that figure 13A shows that each of the switches in each of the stages in each of the subnetworks includes a plurality of forward connecting links. (Ex. 1002, ¶157.)

Figure 13B also shows that the incoming links and outgoing links in each switch of each stage include a plurality of forward connecting links. In addition to the forward connecting links highlighted above with respect to figure 13A, which are also present in figure 13B, figure 13B includes additional forward connecting links. The additional forward connecting links shown in figure 13B include the forward connecting link annotated in blue which is connected from a switch in a stage (stage 3) to a switch in another stage (stage 4) in the **same** subnetwork, whereas the forward connecting link annotated in green is connected from a switch in a stage (stage 3) to a switch in another stage (stage 4) in **another** subnetwork. (Ex. 1002, ¶158.)



(Ex. 1008, FIG. 13B (annotated to show forward connecting links (blue and green) for stage 4 of the top subnetwork); Ex. 1002, ¶158.)²⁴

²⁴ While the annotated version of figure 13B above highlights the forward connecting links for the top-left subnetwork, the combination of figures 13A-13B shows that each of the switches in each of the stages in each of the subnetworks

Wong also discloses the backward connecting links as recited in claim element 1[h]. For example, as illustrated in Figure 13A, the incoming links and outgoing links for each switch of each stage include a plurality of backward connecting links.

illustrated in figure 13B includes a plurality of forward connecting links. (Ex. 1002, ¶159.)

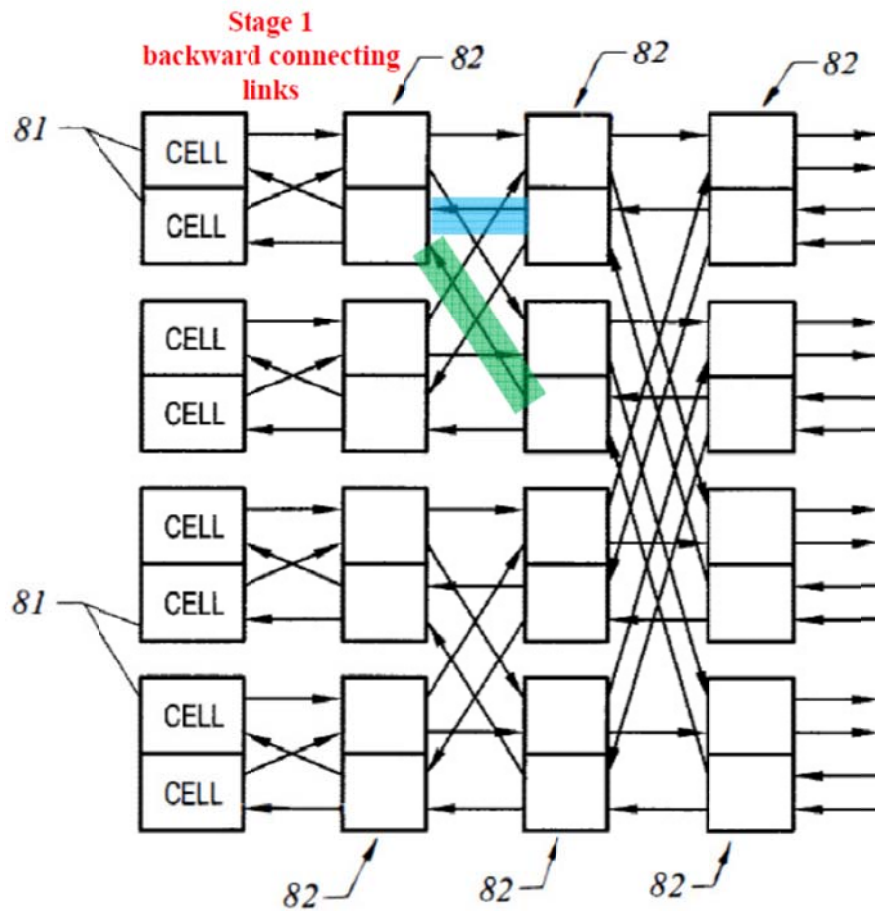


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show backward connecting links (blue and green) for stage 1 of the top subnetwork); Ex. 1002, ¶160.)

The backward connecting links shown in Figure 13A above are connected from switches in stage 2 (“a stage”) to a switch in stage 1 (“another stage”) in the same subnetwork or another subnetwork. For example, the backward connecting link annotated in blue above is connected to a switch in another stage in the same subnetwork, whereas the backward connecting link annotated in green is connected

to a switch in another stage in the another subnetwork. (Ex. 1002, ¶161.) Similar annotated versions of figure 13A below show the backward connecting links for stages 2 and 3.

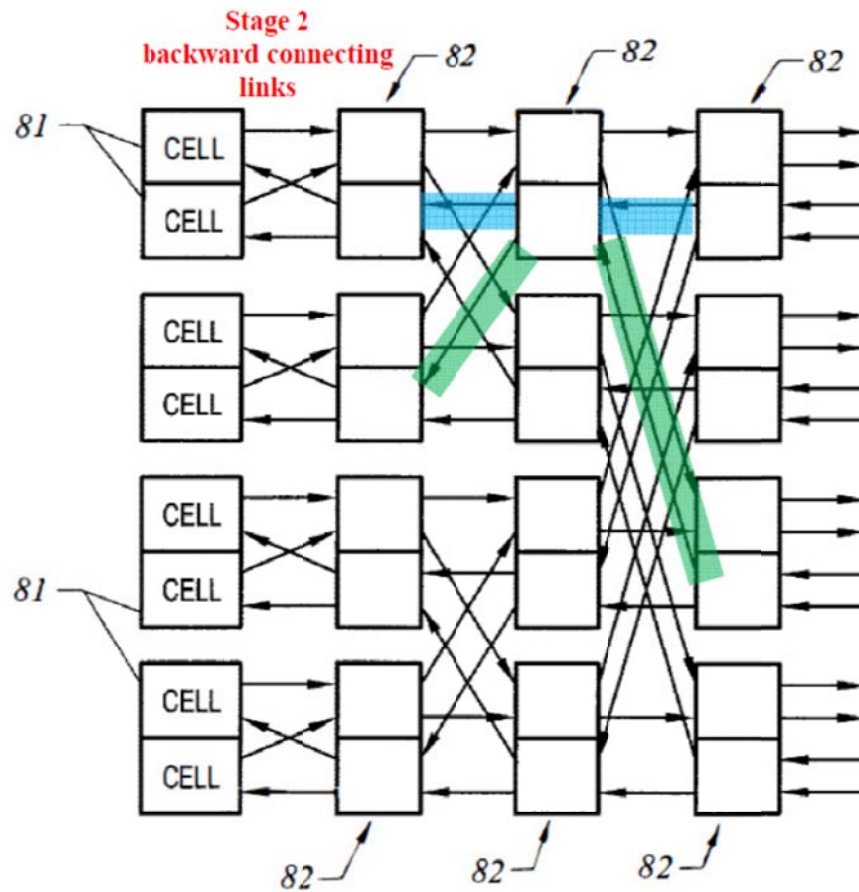


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show backward connecting links (blue and green) for stage 2 of the top subnetwork); Ex. 1002, ¶162.)

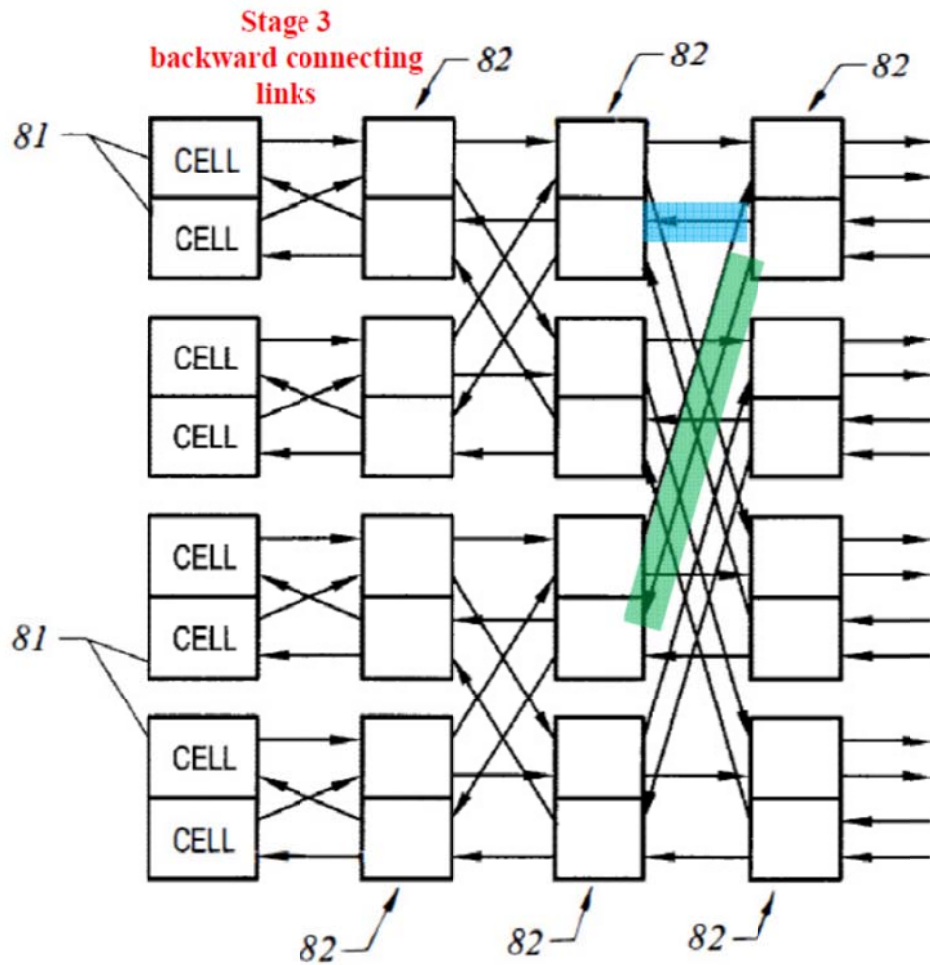


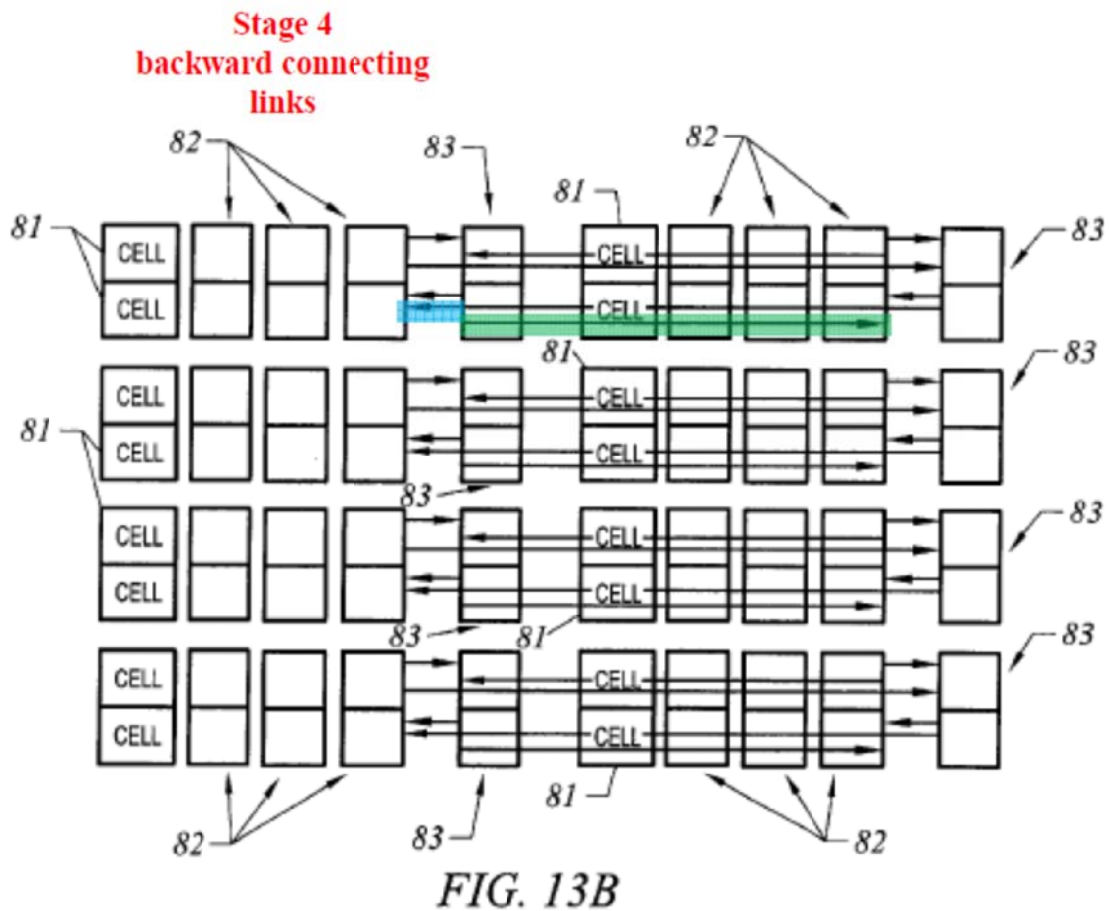
FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show backward connecting links (blue and green) for stage 3 of the top subnetwork); Ex. 1002, ¶162.)²⁵

²⁵ While the annotated versions of figure 13A above highlight the backward connecting links of the top-most subnetwork, a POSITA would have recognized that figure 13A shows that each of the switches in each of the stages in each of the

Figure 13B also shows that the incoming links and outgoing links in each switch of each stage include a plurality of backward connecting links. In addition to the backward connecting links described above with respect to figure 13A, which are replicated in figure 13B, figure 13B includes additional backward connecting links. (Ex. 1002, ¶164.) The additional backward connecting links shown in figure 13B below are connected from switches in a stage 4 (“a stage”) to switches in stage 3 (“another stage”) in same said subnetwork or another said subnetwork. For example, the backward connecting link annotated in blue below is connected to a switch in another stage in the same subnetwork, whereas the backward connecting link annotated in green is connected to a switch in another stage in the another subnetwork.

subnetworks illustrated includes a plurality of backward connecting links. (Ex. 1002, ¶163.)



(Ex. 1008, FIG. 13B (annotated to show backward connecting links (blue and green) for stage 4 of the top-left subnetwork); Ex. 1002, ¶164.)²⁶

²⁶ While the annotated version of figure 13B above highlights the backward connecting links for the top-left subnetwork, the combination of figures 13A-13B shows that each of the switches in each of the stages in each of the subnetworks

- i) **“Said forward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks, and”**

Wong discloses this claim element. (Ex. 1002, ¶¶166-171.) As an initial matter, this claim element does not further limit claim 1 because it simply recites several optional features. *MPHJ Tech. Invs., LLC*, 847 F.3d at 1379; *In re Johnston*, 435 F.3d at 1384. As discussed separately below, since each subpart of claim element 1[i] imposes an optional “zero or more” feature onto the network components (e.g. forward connecting links including “zero or more” straight links and cross links), *Wong* discloses claim element 1[i] regardless of the optional features imposed thereon. (Ex. 1002, ¶¶166-167.) For example, claim 1 requires “zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks.”²⁷ Because

illustrated in figure 13B includes a plurality of backward connecting links. (Ex. 1002, ¶165.)

²⁷ For convenience, “cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in on or more other

Wong discloses forward connecting links as discussed above (*supra* Section XII.A.1(h)), *Wong* discloses claim element 1[i] because *Wong* discloses that the forward connecting links include “zero or more” cross links and straight links.²⁸

Moreover, *Wong* discloses “said forward connecting links comprising *zero or more* straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork” because *Wong* discloses that the forward connecting links for each switch include at least one straight link connected from a switch in a stage in a subnetwork to a switch in another stage in

subnetworks” are referred to as “same-stage” cross links. In addition to same-stage cross links, claim 11 also recites “cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks,” which are referred to as “inter-stage cross links.”

²⁸ To the extent they can be understood, dependent claims 2, 4, 5-7, and 9 attempt to further limit the “zero or more cross links” recited in claim 1. Because claim 1 requires “zero or more” cross links, *Wong* discloses the features of claims 2, 4, 5-7, and 9 by virtue of disclosing the claimed forward and backward connecting links which include the “zero or more” cross links with the additional features of claims 2, 4, 5-7, and 9.

the same subnetwork. For example, such straight links are shown in annotated figure 13A below.

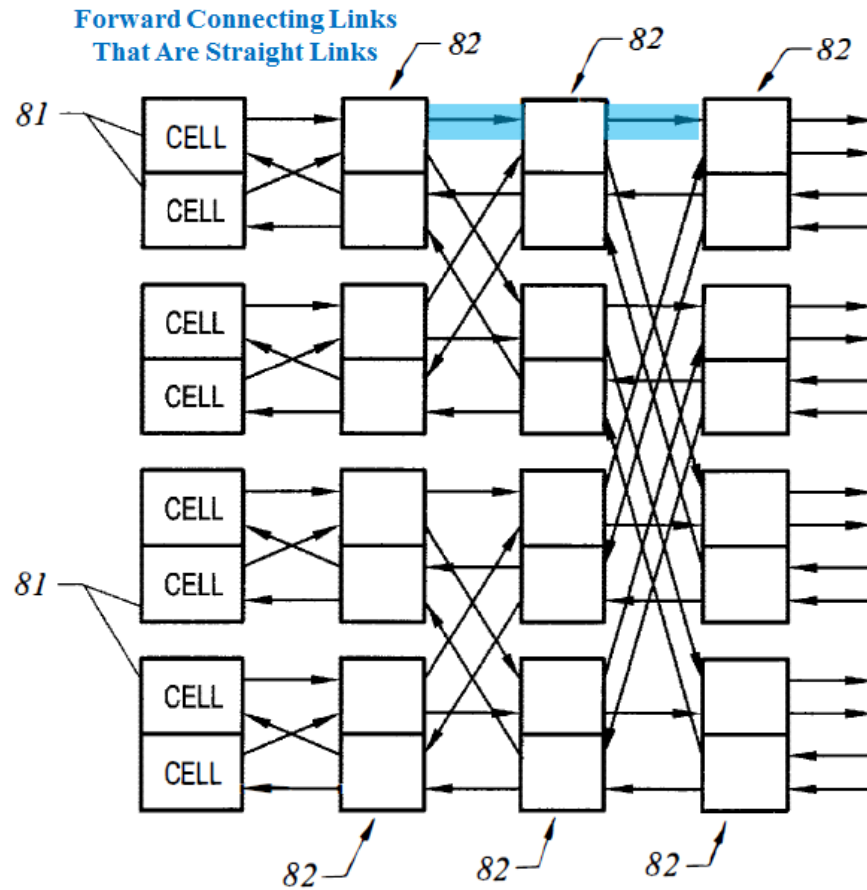


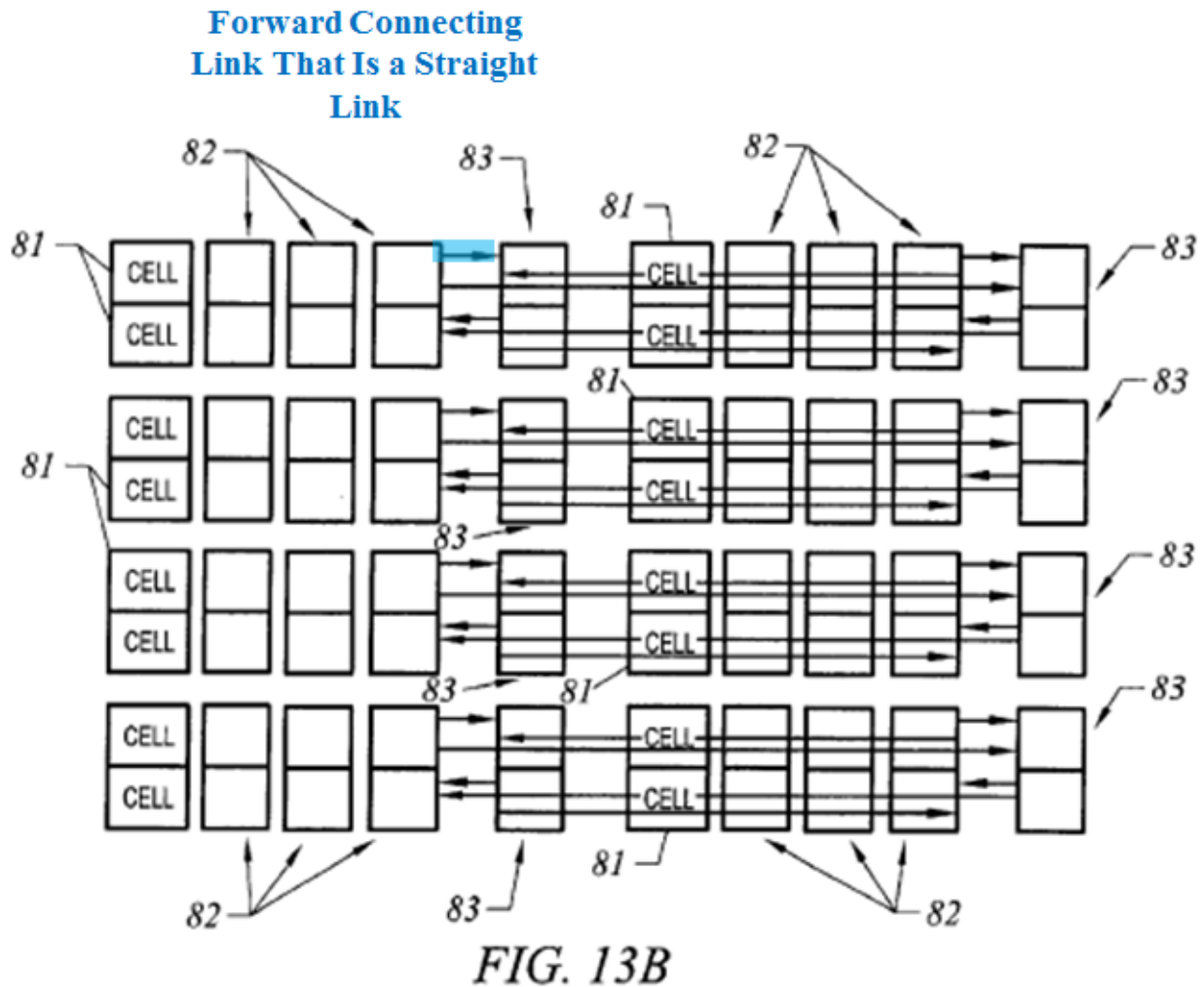
FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show forward connecting links that are straight links (blue) in the top subnetwork); Ex. 1002, ¶168.)²⁹

²⁹ While the annotations above are used to highlight the straight links in the top subnetwork, figure 13A shows at least one of the incoming or outgoing links for

Figure 13B also discloses the forward connecting links include at least one straight link connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork. For example, as shown in annotated figure 13B below, a forward link for stages 3 and 4 of the top-left subnetwork highlighted in blue is a “straight link.”

each switch in each subnetwork is a forward connecting link that is also a straight link. (Ex. 1002, ¶169.)



(Ex. 1008, FIG. 13B (annotated to show a forward connecting link that is a straight link for stages 3 and 4); Ex. 1002, ¶170.)³⁰

³⁰ While the annotation is only used to highlight a straight link for stages 3 and 4 of the top-left subnetwork, figure 13B shows, for each stage 4 switch shown in each

The embodiments shown in figures 13A and 13B of *Wong* include zero forward connecting links that are cross links connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks. Because *Wong* discloses zero same-stage cross links, *Wong* discloses “zero or more” same-stage cross links, as claimed. (Ex. 1002, ¶171.)

- j) **“Said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks.”**

Wong discloses this claim element. (Ex. 1002, ¶¶172-176.) As an initial matter, this claim element does not further limit claim 1 because it simply recites several optional features. *MPHJ Tech. Invs., LLC*, 847 F.3d at 1379; *In re Johnston*, 435 F.3d at 1384. As discussed separately below, since each subpart of claim element 1[j] imposes an optional “zero or more” feature onto the network components (e.g. backward connecting links including “zero or more” straight links and cross links), *Wong* discloses claim element 1[j] regardless of the optional

subnetwork, at least one of the incoming or outgoing links is a forward connecting link that is also a straight link. (Ex. 1002, ¶170.)

features imposed thereon. (Ex. 1002, ¶¶172-173.) In other words, because *Wong* discloses backward connecting links as discussed above (*supra* Section XII.A.1(h)), *Wong* discloses claim element 1[j] because *Wong* discloses that the backward connecting links include “zero or more” cross links and straight links.

Moreover, *Wong* discloses “said backward connecting links comprising *zero or more* straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork” because *Wong* discloses the backward connecting links for each switch include at least one straight link connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork. For example, such straight links are shown in annotated figure 13A below where each of the backward connecting links highlighted in blue is a “straight link.”

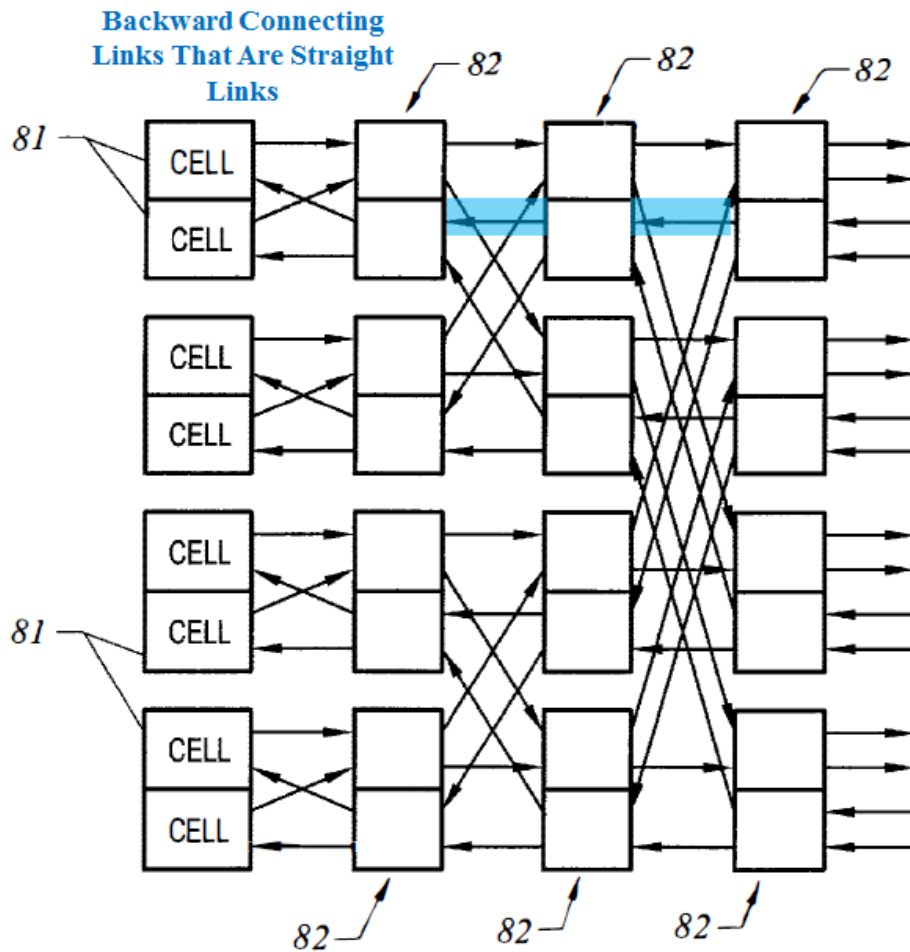


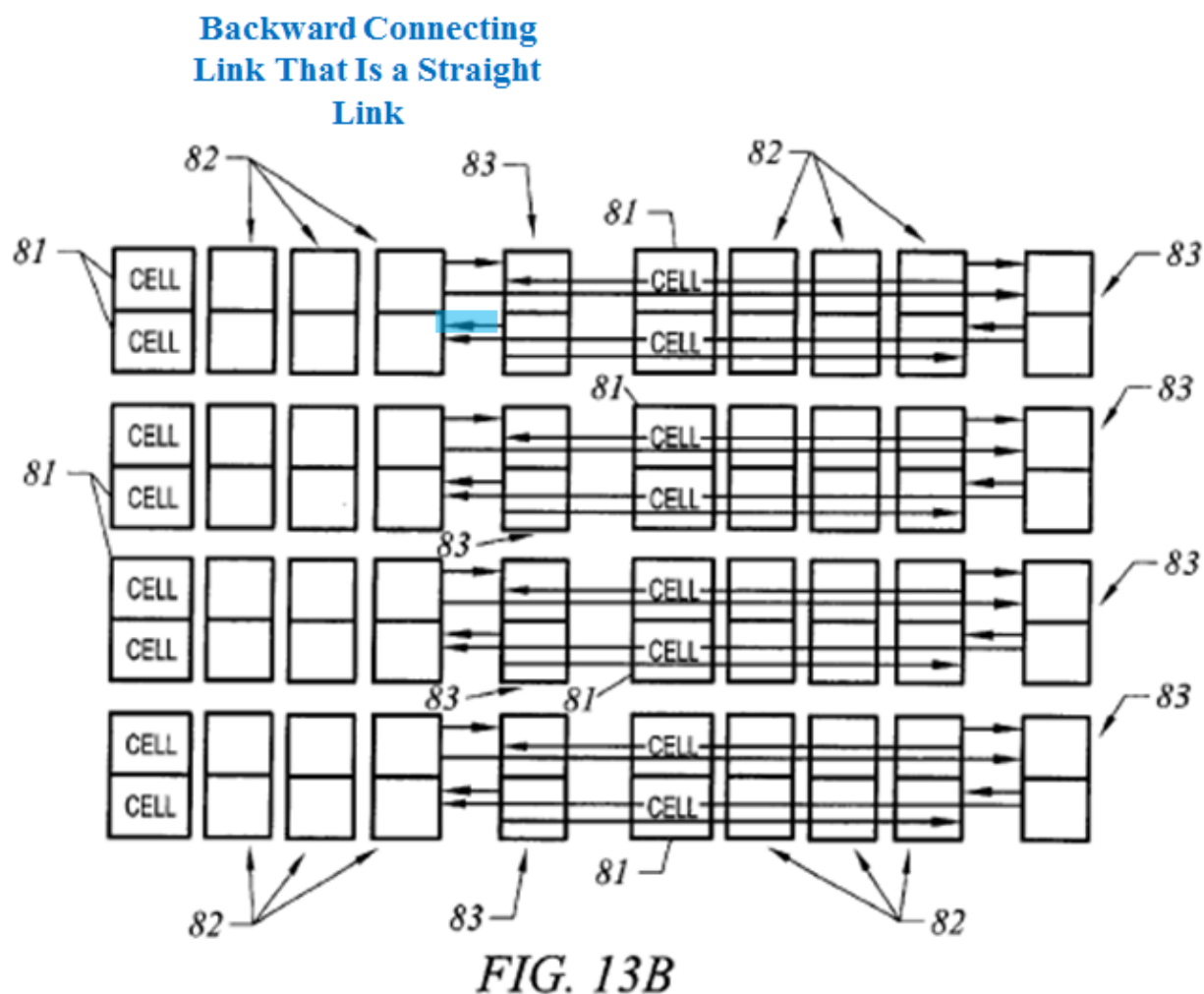
FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show backward connecting links that are straight links (blue) in the top subnetwork); Ex. 1002, ¶174.)³¹

³¹ While the annotations above are used to highlight the straight links in the top subnetwork, figure 13A shows at least one of the incoming or outgoing links is a

Figure 13B also discloses the backward connecting links include at least one straight link connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork. For example, as shown in annotated figure 13B below, a forward link for stages 3 and 4 of the top-left subnetwork highlighted in blue is a “straight link.”

backward connecting link that is also a straight link for each switch shown in each subnetwork. (Ex. 1002, ¶174.)



(Ex. 1008, FIG. 13B (annotated to show a backward connecting link that is a straight link for stages 3 and 4); Ex. 1002, ¶175.)³²

³² While the annotation is only used to highlight a straight link for stages 3 and 4 of the top-left subnetwork, figure 13B shows, for each stage 4 switch shown in each

The embodiments shown in figures 13A and 13B of *Wong* include zero backward connecting links that are cross links connected from a switch in a stage in a subnetwork to a switch in the *same numbered stage* in one or more other subnetworks. Because *Wong* discloses zero same-stage cross links, *Wong* discloses “zero or more” same-stage cross links, as claimed. (Ex. 1002, ¶176.)

2. Claim 2

- a) **“The network implemented in a non-transitory medium of claim 1, wherein said cross links between switches of stages in any two said subnetworks are connected as either vertical links only, or horizontal links only, or both vertical links and horizontal links.”**

Wong discloses this claim element. (Ex. 1002, ¶177.) While there is no antecedent basis for “said cross links,” it is assumed that the cross links recited in claim 2 are included in the “zero or more cross links” of the forward connecting links and the “zero or more cross links” of the backward connecting links of claim 1.

As discussed above with respect to claim elements 1[i] and 1[j], the embodiments shown in *Wong’s* figures 13A-3B include zero backward and

subnetwork, at least one of the incoming or outgoing links is a backward connecting link that is also a straight link. (Ex. 1002, ¶175.)

forward connecting links that are the same-stage cross links. (*See supra* Sections XII.1(i)-(j).) Thus, the embodiments shown in figures 13A and 13B include zero “cross links between switches of stages in any two said subnetworks [that] are connected as either vertical links only, or horizontal links only, or both vertical links and horizontal links.” In other words, since claim 2 requires “zero or more” same-stage cross links with the recited characteristic, *Wong* discloses the features of claim 2 whether or not *Wong* includes any cross links having the characteristics recited in claim 2. (Ex. 1002, ¶177.)

3. Claim 3

- a) **“The network implemented in a non-transitory medium of claim 2, wherein each subnetwork with its said stages is replicated in either said rows or said columns of the two-dimensional grid, or**

each subnetwork with said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid, or

each subnetwork with both its said stages, and said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid.”

Wong discloses this claim element. (Ex. 1002, ¶¶178-182.) Claim element 3[a] recites three possible configurations of each subnetwork separated by the two

“or” conjunctions. “When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art.” *Brown v. 3M*, 265 F.3d 1349, 1351 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with year date data in “at least one of two-digit, three-digit, or four-digit” representations, found unpatentable by a system that offsets year dates in only two-digit formats). Thus, to disclose claim element 3[a], the prior art must disclose at least one of the three possible configurations recited. *Wong*, by way of each of figures 13A and 13B, discloses at least the first configuration, i.e., “each subnetwork with its said stages is replicated in either said rows or said columns of the two-dimensional grid.”³³ (Ex. 1002, ¶¶179-181.)

³³ Notably, the second and third configurations of each subnetwork as set forth in claim 3 do not add any non-optional features in comparison to the first configuration, and *Wong* discloses the second and third configurations for the same reasons it discloses the first configuration. (Ex. 1002, ¶182.)

Figure 13A of *Wong* shows a subnetwork that includes a row of three switches (corresponding to three stages) replicated in four rows in one column.

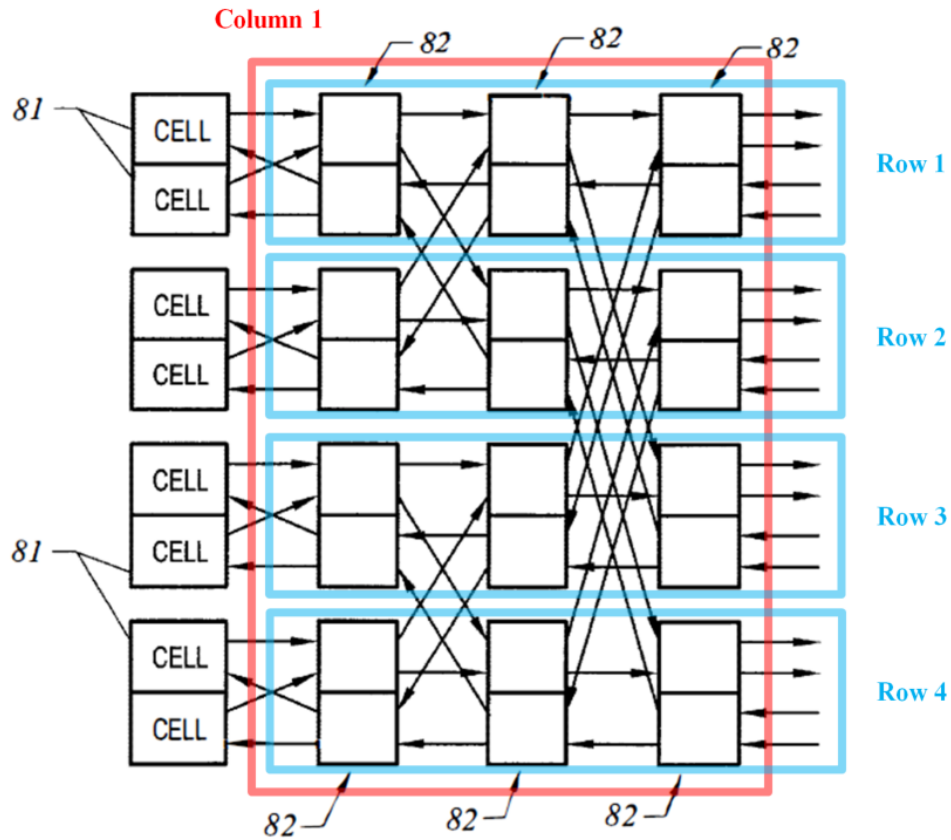


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show subnetworks in rows and columns); Ex. 1002, ¶179.)

Similarly, figure 13B of *Wong* shows a subnetwork that includes a row of four switches (corresponding to four stages) replicated in both rows and columns such that there are two columns of four rows.

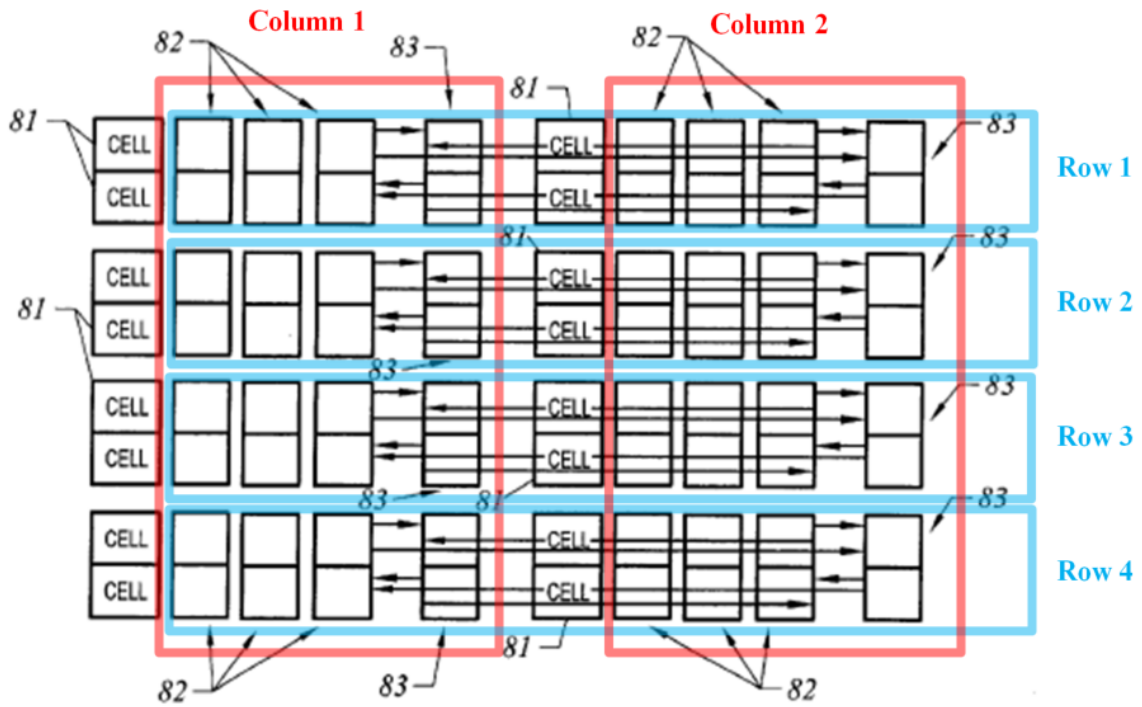


FIG. 13B

(Ex. 1008, FIG. 13B (annotated to show subnetworks in rows and columns); Ex. 1002, ¶180.) Figure 14A, which is another representation of the network and logic blocks of Figure 13B, further confirms this understanding of *Wong's* Figure 13B. (Ex. 1002, ¶181.)

4. Claim 4

- a) **“The network implemented in a non-transitory medium of claim 2, wherein said horizontal links between switches in two said stages are substantially of equal length and said vertical links between switches in two said stages are substantially of equal length in the entire two-dimensional grid of rows and columns, or**

said horizontal links between switches in two said stages are substantially of a hop length h and said vertical links between switches in two said stages are substantially of a hop length v where $h \geq 0$ and $v \geq 0$.”

Wong discloses this claim element. (Ex. 1002, ¶¶183-185.) Claim element 4[a] recites two possible configurations of the horizontal and vertical links separated by the two “or” conjunctions. Thus, to disclose claim element 4[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at 1351. Moreover, the “vertical links” and “horizontal links” recited in claim element 4[a] further modify the “zero or more cross links” of claim 1 by way of claim 2. (Ex. 1002, ¶183.)

Because the embodiments shown in figures 13A and 13B of *Wong* include “zero” same-stage cross links as recited in claim 1, those embodiments also disclose “zero” same-stage cross links that are connected as vertical or horizontal links as recited in claim 2. (*Supra* Sections XII.A.1(i)-(j); *see also supra* Section XII.A.2.) As such, the embodiments shown in figures 13A and 13B include “zero”

same-stage cross links that are connected by vertical and horizontal links having the additional characteristics recited in claim 4. For example, the embodiments shown in figures 13A and 13B include “zero” same-stage cross links that are implemented as vertical or horizontal links where “said horizontal links between switches in two said stages are substantially of equal length and said vertical links between switches in two said stages are substantially of equal length in the entire two-dimensional grid of rows and columns,” as recited in claim 4. (Ex. 1002, ¶184.) Similarly, the embodiments shown in figures 13A-13B also include “zero” same-stage cross links that are implemented as vertical or horizontal links where “said horizontal links between switches in two said stages are substantially of a hop length h and said vertical links between switches in two said stages are substantially of a hop length v where $h \geq 0$ and $v \geq 0$.” (Ex. 1002, ¶185.)

5. Claim 5

- a) **“The network implemented in a non-transitory medium of claim 1, wherein said incoming cross links and said outgoing cross links are connected through only one multiplexer at each switch.”**

Wong discloses this claim element. (Ex. 1002, ¶186.) While there is no antecedent basis for “said incoming cross links” and “said outgoing cross links” as recited in claim 5, *Wong* discloses the features of claim 5 to the extent the “said incoming cross links” and “said outgoing cross links” are interpreted as further

limiting the “zero or more” same-stage cross links in the forward and backward connecting links of claim 1.

Moreover, as discussed above with respect to claim 1, the embodiments shown in figures 13A-13B of *Wong* include “zero” same-stage cross links. (*Supra* Sections XII.A.1(i)-(j).) Thus, because those embodiments of *Wong* include “zero” same-stage cross links, those embodiments also include “zero” same-stage cross links that are connected through only one multiplexer at each switch as recited in claim 5. (Ex. 1002, ¶186.)

6. Claim 6

- a) “The network implemented in a non-transitory medium of claim 1, wherein said one or more cross links are connected between switches in two said stages that are not same numbered.”**

Wong discloses this claim element. (Ex. 1002, ¶187.) While there is no antecedent basis for “said one or more cross links,” *Wong* discloses the features of claim 6 to the extent the “said one or more cross links” are interpreted as further limiting the “zero or more” same-stage cross links in the forward and backward connecting links of claim 1.

Moreover, as discussed above with respect to claim 1, the embodiments shown in figures 13A-13B of *Wong* include “zero” same-stage cross links. (*Supra* Sections XII.A.1(i)-(j).) Thus, because those embodiments of *Wong* include

“zero” same-stage cross links, those embodiments also include “zero” same-stage cross links that are connected between switches in two said stages that are not same numbered as recited in claim 6. (Ex. 1002, ¶187.)

7. Claim 7

- a) **“The network implemented in a non-transitory medium of claim 6, wherein said one or more cross links are connected between at least one same numbered stage in all said subnetworks, or said one or more cross links are connected between at least one set of two not same numbered stages in all said subnetworks.”**

Wong discloses this claim element. (Ex. 1002, ¶188.) While there is no antecedent basis in claim 1 for “said one or more cross links” as recited in claim 7, *Wong* discloses the features of claim 7 to the extent the “said one or more cross links” are interpreted as further limiting the “zero or more” same-stage cross links in the forward and backward connecting links of claims 1 and 6.

Moreover, as discussed above with respect to claims 1 and 6, the embodiments shown in figures 13A-13B of *Wong* include “zero” same-stage cross links as recited in claim 6. (*Supra* Sections XII.A.1(i)-(j); *see also supra* Section XII.A.6.) Thus, because those embodiments of *Wong* include “zero” same-stage cross links, those embodiments also include “zero” same-stage cross links that are connected between switches in two said stages that are not same numbered as

recited in claim 6 and that are connected between at least one same numbered stage in all said subnetworks or connected between at least one set of two not same numbered stages in all said subnetworks as recited in claim 7. (Ex. 1002, ¶188.)

8. Claim 9

- a) **“The network implemented in a non-transitory medium of claim 1, wherein said cross links are implemented in two or more metal layers, or each switch is configurable by an SRAM cell or a Flash Cell or a flip-flop, or said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers are either inverting or non-inverting buffers, or some of said stages in a subnetwork comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ and each such switch having $d_i + m$ incoming links and $d_o + n$ outgoing links, or one or more of said stages in a said subnetwork comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers.”**

Wong discloses this claim element. (Ex. 1002, ¶¶189-192.) Claim element 9[a] modifies the network of claim 1 by way of five possible configurations separated by the four “or” conjunctions. Thus, to disclose claim element 9[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at

1351. As discussed below, *Wong* discloses at least three of the configurations set forth in claim 9. (Ex. 1002, ¶¶189-192.)

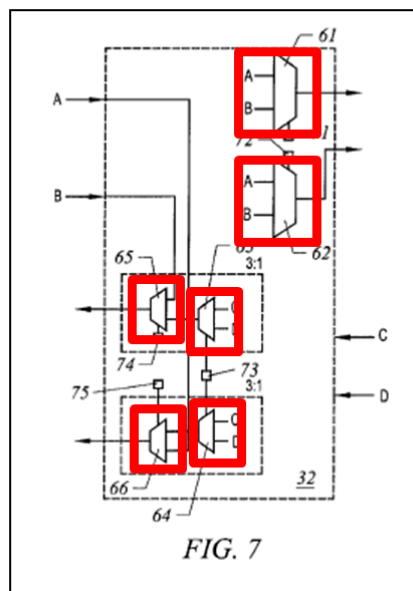
With respect to “said cross links are implemented in two or more metal layers,” there is no antecedent basis for “said cross links.” It is assumed that “said cross links” recited in claim 9 are included in the “zero or more cross links” of the forward and backward connecting links of claim 1. As discussed above with respect to claim 1, the embodiments shown in figures 13A and 13B of *Wong* include “zero” same-stage cross links as recited in claim 1. (*Supra* Sections XII.A.1(i)-(j).) Because those embodiments disclose zero same-stage cross links, those embodiments of *Wong* also include zero same-stage cross links that are “are implemented in two or more metal layers.” (Ex. 1002, ¶190.) Therefore, *Wong* discloses the features of claim 9.

Moreover, *Wong* also discloses “some of said stages in a subnetwork comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ and each such switch having $d_i + m$ incoming links and $d_o + n$ outgoing links.” It is assumed that this phrase simply requires that some of the stages include a switch that is 2x2 or greater in size such that the switch has at least 2 incoming links and 2 outgoing links. As discussed above with respect to claim element 1[e], such a switch is included in the stages of the networks shown in figures 13A-13B of

Wong. (*Supra* Section XII.A.1(e).) Therefore, *Wong* discloses the features of claim 9 for this additional reason. (Ex. 1002, ¶191.)

Furthermore, *Wong* also discloses “one or more of said stages in a said subnetwork comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers.” Specifically, as discussed above with respect to claim element 1[e], *Wong* discloses using the switch shown in figure 7 in the embodiments illustrated in figures 13A-3B of *Wong*. (*Supra* Section XII.A.1(e).) As shown in an annotated version of *Wong*’s figure 7 below, the switch includes “six 2:1 multiplexers” as recited in claim 9, and therefore, *Wong* discloses the features of claim 9 for this additional reason.

2:1 Multiplexers



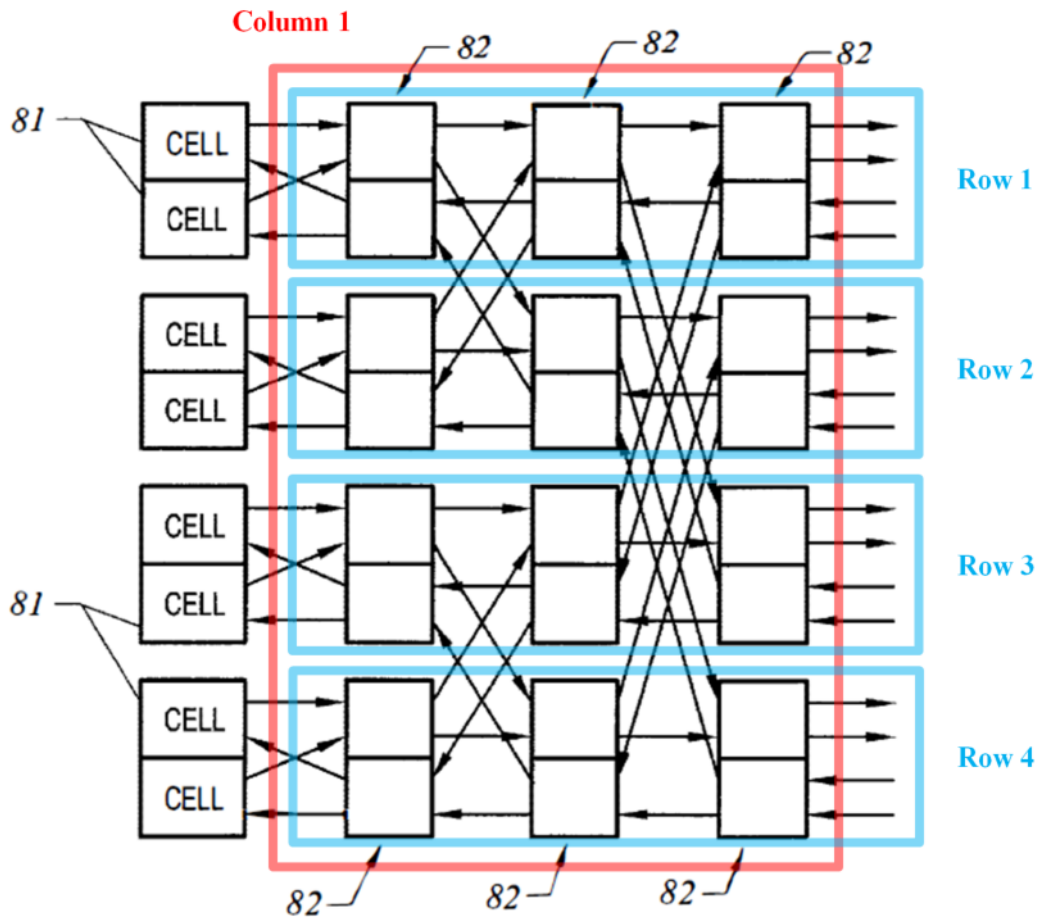
(Ex. 1008, FIG. 7 (annotated to show six 2:1 multiplexers); Ex. 1002, ¶192.)

9. Claim 10

- a) **“The network implemented in a non-transitory medium of claim 1, wherein said switches of size $d_i \times d_o$ are either fully populated or partially populated, or said plurality of subnetworks are implemented in a single dimension, or said plurality of subnetworks are either implemented in three or more dimensions or implemented in a 3D integrated circuit device.”**

Wong discloses this claim element. (Ex. 1002, ¶193.) Claim element 10[a] modifies the network of claim 1 by way of three possible configurations separated by the two “or” conjunctions. Thus, to disclose claim element 10[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at 1351.

Wong discloses that “said plurality of subnetworks are implemented in a single dimension” as set forth in claim 10. (Ex. 1002, ¶193.) For example, the embodiment shown in figure 13A of *Wong* implements the plurality of subnetworks in one dimension (one column).



(Ex. 1008, FIG. 13 (annotated); Ex. 1002, ¶193; *see also supra* Section XII.A.1(c).)

10. Claim 11

- a) “A network implemented in a non-transitory medium comprising”

The preamble of claim 11 recites features that track those of the preamble of claim 1. Thus, to the extent the preamble is limiting, *Wong* discloses the features of the preamble for at least the reasons presented above for claim element 1[a].

(*Supra* Section XII.A.1(a); Ex. 1002, ¶194.)

b) “a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links”

Claim element 11[b] recites features that track those of claim element 1[b]. *Wong* discloses this feature for at least the reasons presented above for element 1[b]. (*Supra* Section XII.A.1(b); Ex. 1002, ¶195.)

c) “said plurality of subnetworks arranged in a two-dimensional grid of rows and columns”

Claim element 11[c] recites features that track those of claim element 1[c]. *Wong* discloses this feature for at least the reasons presented above for element 1[c]. (*Supra* Section XII.A.1(c); Ex. 1002, ¶196.)

d) “each subnetwork comprising y stages, where $y \geq 1$; and”

Claim element 11[d] recites features that track those of claim element 1[d]. *Wong* discloses this feature for at least the reasons presented above for element 1[d]. (*Supra* Section XII.A.1(d); Ex. 1002, ¶197.)

e) “each stage comprising a switch of size $d_i \times d_o$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_o$ having d_i incoming links and d_o outgoing links; and”

Claim element 11[e] recites features that track those of claim element 1[e]. *Wong* discloses this feature for at least the reasons presented above for element 1[e]. (*Supra* Section XII.A.1(e); Ex. 1002, ¶198.)

- f) **“Said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork; and”**

Claim element 11[f] recites features that track those of claim element 1[f].

Wong discloses this feature for at least the reasons presented above for element 1[f]. (*Supra* Section XII.A.1(f); Ex. 1002, ¶199.)

- g) **“each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said inlet links and may or may not be comprising the same number of said outlet links; each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said stages; each stage may or may not be comprising the same number of switches; and each switch in each stage may or may not be of the same size, each multiplexer in each stage may or may not be of the same size and”**

Claim element 11[g] recites features that track those of claim element 1[g].

Wong discloses this feature for at least the reasons presented above for element 1[g]. (*Supra* Section XII.A.1(g); Ex. 1002, ¶200.)

- h) “Said incoming links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks, and”**

Wong discloses this claim element. (Ex. 1002, ¶¶201-207.) As an initial matter, this claim element does not further limit claim 11 as it simply recites several optional features. *MPHJ Tech. Invs., LLC*, 847 F.3d at 1379; *In re Johnston*, 435 F.3d at 1384. As discussed below, since each subpart of claim element 11[h] imposes an optional “zero or more” feature onto the network components such as the incoming links including “zero or more” straight links and two types of “zero or more” cross links, *Wong* discloses these features regardless of the optional features imposed thereon. (Ex. 1002, ¶¶201-202.) In other words, because *Wong* discloses incoming links as discussed above (*supra* Section XII.A.10(e)), *Wong* discloses claim element 11[h] because *Wong* discloses that the

incoming links include “zero or more” straight links and “zero or more” of each of the different types of cross links recited.³⁴ (Ex. 1002, ¶202.)

Moreover, *Wong* discloses “said incoming links comprising *zero or more* straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork” for the additional reason that *Wong* discloses that the incoming links include at least one straight link connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork as shown in figure 13A below. As can be seen, for each switch shown in each subnetwork, at least one of the incoming links is a straight link as recited. The incoming links for the switches that are straight links are highlighted in blue for stage 1, in green for stage 2, and in red for stage 3.

³⁴ To the extent they can be understood, dependent claims 12, 14, 15, and 19 attempt to further limit the “zero or more cross links” recited in claim 11. Because claim 11 requires “zero or more” cross links, *Wong* discloses the features of claims 12, 14, 15, and 19 because *Wong* discloses “zero or more” cross links with the features added by those claims.

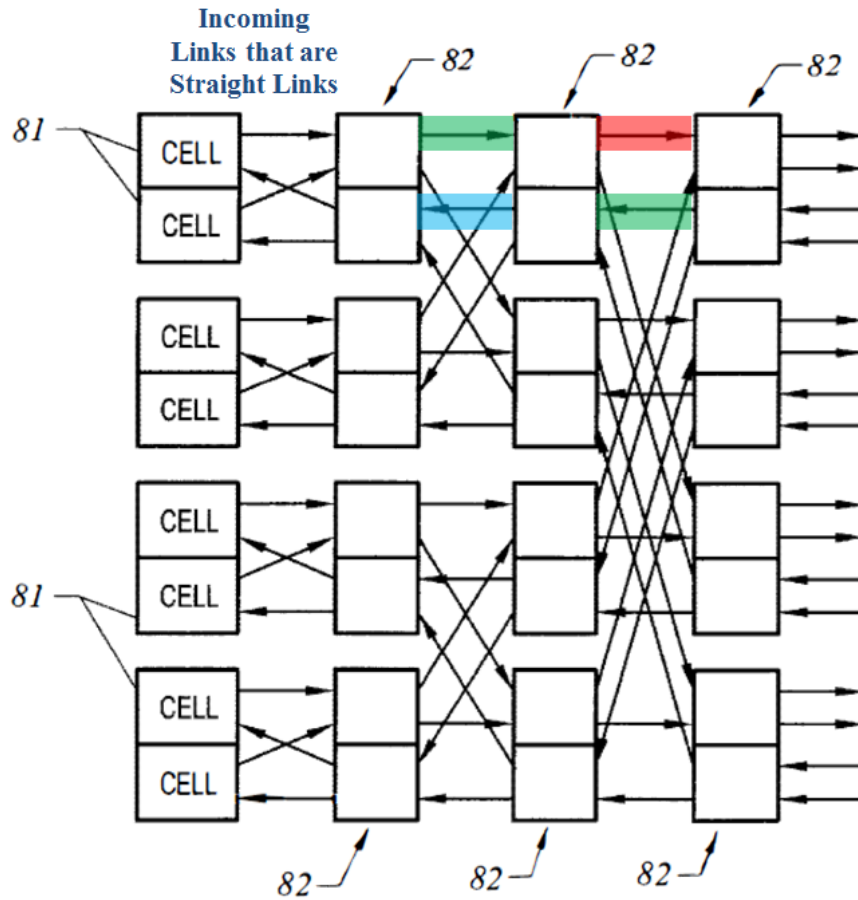
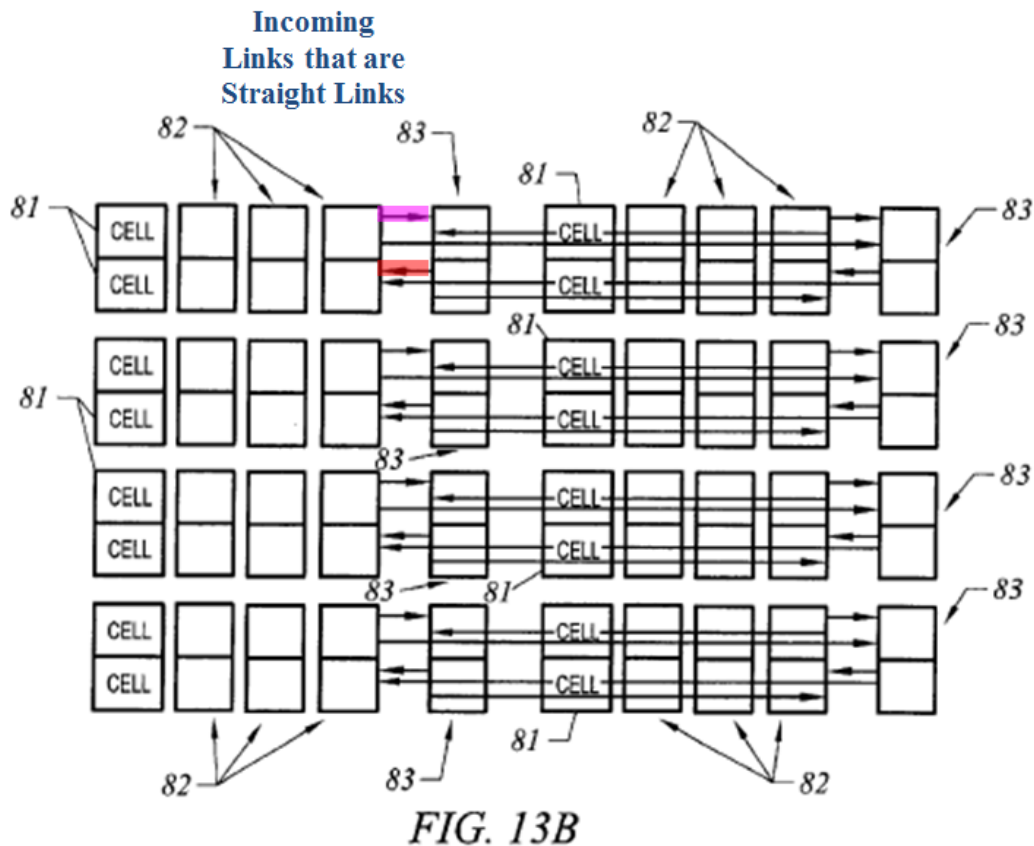


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show incoming links that are straight links); Ex. 1002, ¶203.)³⁵

³⁵ While the annotations in figure 13A above are used to highlight the straight links in the top subnetwork, a POSITA would have understood that figure 13A shows, for each switch shown in each subnetwork, at least one of the incoming links is a straight link. (Ex. 1002, ¶203.)

Figure 13B also shows that the incoming links for each switch of each stage include at least one straight link. For example, in addition to the straight links included in figure 13B based on the replication of the subnetworks of figure 13A, additional straight links are shown in annotated figure 13B below, where an additional straight link for stage 3 is shown in red, and a straight link for stage 4 is shown in purple.



(Ex. 1008, FIG. 13B (annotated to show incoming links that are straight links); Ex. 1002, ¶204.)

Wong further discloses “said incoming links ... also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in another subnetwork.” For example, *Wong* discloses “zero” such same-stage cross links. (Ex. 1002, ¶205.)

Wong also discloses “said incoming links ... also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks.” For example, *Wong* discloses that the incoming links for each switch include at least one such inter-stage cross link that goes between two different stages. As can be seen in annotated figure 13A below, for each switch shown in each subnetwork, at least one of the incoming links is an inter-stage cross link. The incoming links for the switches that are inter-stage cross links are highlighted in blue for stage 1, in green for stage 2, and in red for stage 3. (Ex. 1002, ¶206.)

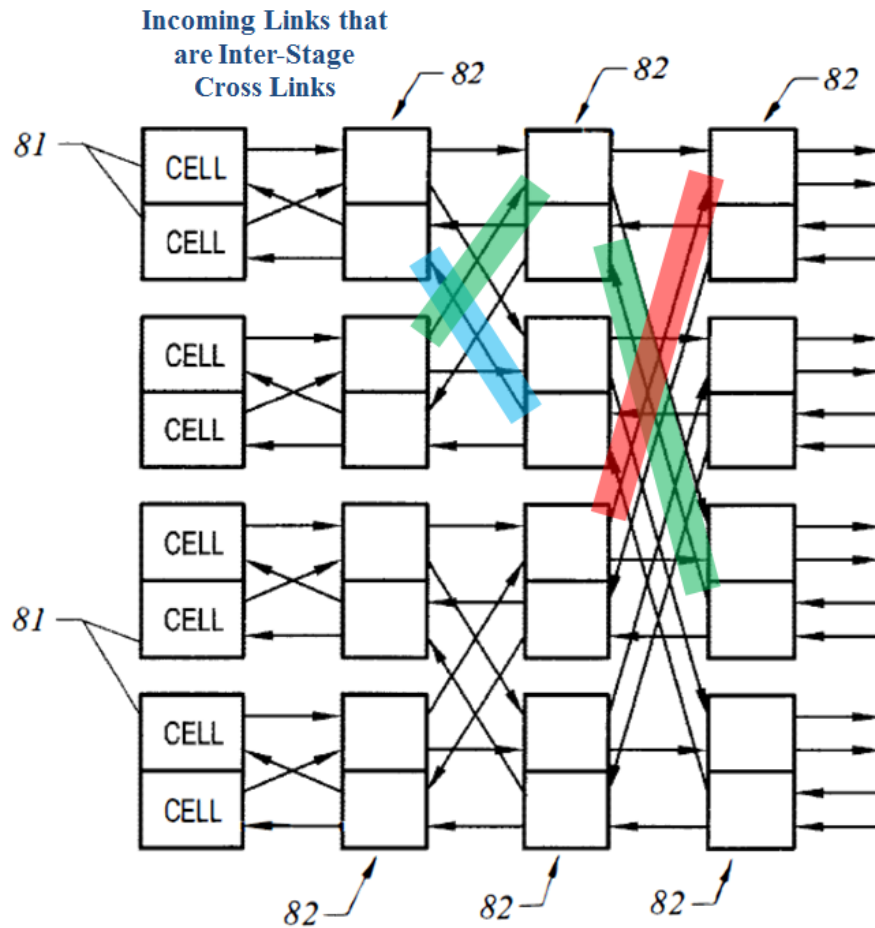
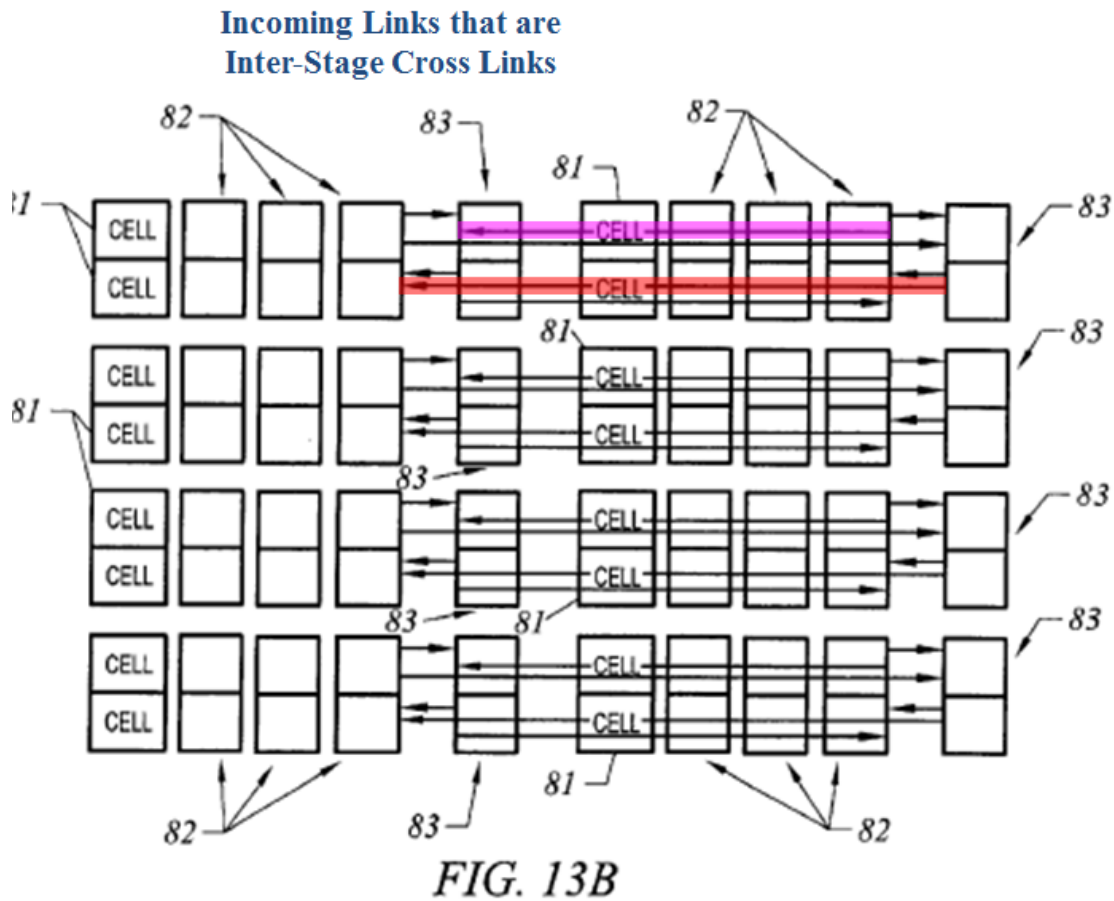


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show incoming links that are inter-stage cross links); Ex. 1002, ¶206.)

Figure 13B also shows that the incoming links in each switch of each stage include at least one inter-stage cross link that connects two different stages in two different subnetworks. For example, in addition to the inter-stage cross links included in figure 13B based on the replication of the subnetworks of figure 13A,

additional inter-stage cross links corresponding to stage 3 (red) and stage 4 (purple) are shown. (Ex. 1002, ¶207.)



(Ex. 1008, FIG. 13B (annotated to show incoming links that are inter-stage cross links); Ex. 1002, ¶207.)

- i) **“Said outgoing links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks, and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks.”**

Wong discloses this claim element. (Ex. 1002, ¶¶208-214.) As an initial matter, this claim element does not further limit claim 11 as it simply recites several optional features. *MPHJ Tech. Invs., LLC*, 847 F.3d at 1379; *In re Johnston*, 435 F.3d at 1384. As discussed below, since each subpart of claim element 11[i] imposes an optional “zero or more” feature onto the network components (e.g., outgoing links including “zero or more” straight links and two types of “zero or more” cross links), *Wong* discloses these features regardless of the optional features imposed thereon. (Ex. 1002, ¶¶208-209.) In other words, because *Wong* discloses outgoing links as discussed above (*supra* Section XII.A.10(e)), *Wong* discloses claim element 11[i] because *Wong* discloses that the incoming links include “zero or more” straight links and “zero or more” of each of the different types of cross links. (Ex. 1002, ¶209.)

Moreover, *Wong* discloses “said outgoing links comprising *zero or more* straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork” for the additional reason that *Wong* discloses that the outgoing links include at least one straight link connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork as shown in annotated figure 13A below. As can be seen, for each switch shown in each subnetwork, at least one of the outgoing links is a straight link as recited. The outgoing links for the switches that are straight links for the top-most subnetwork are highlighted in blue for stage 1, in green for stage 2, and in red for stage 3. (Ex. 1002, ¶210.)

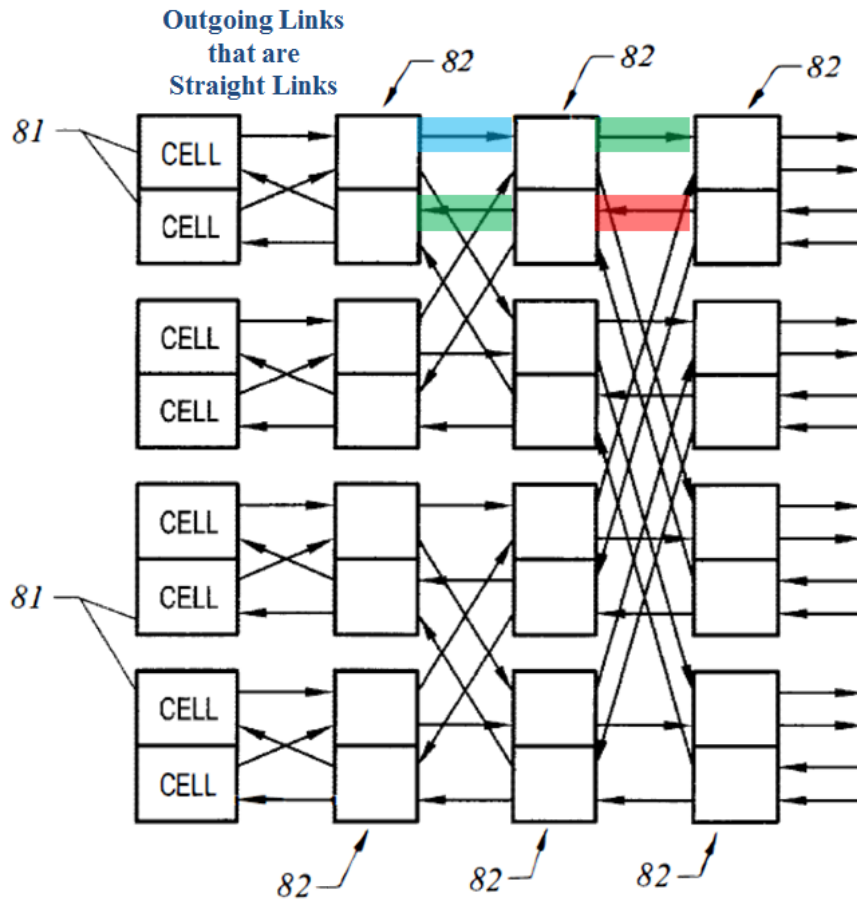
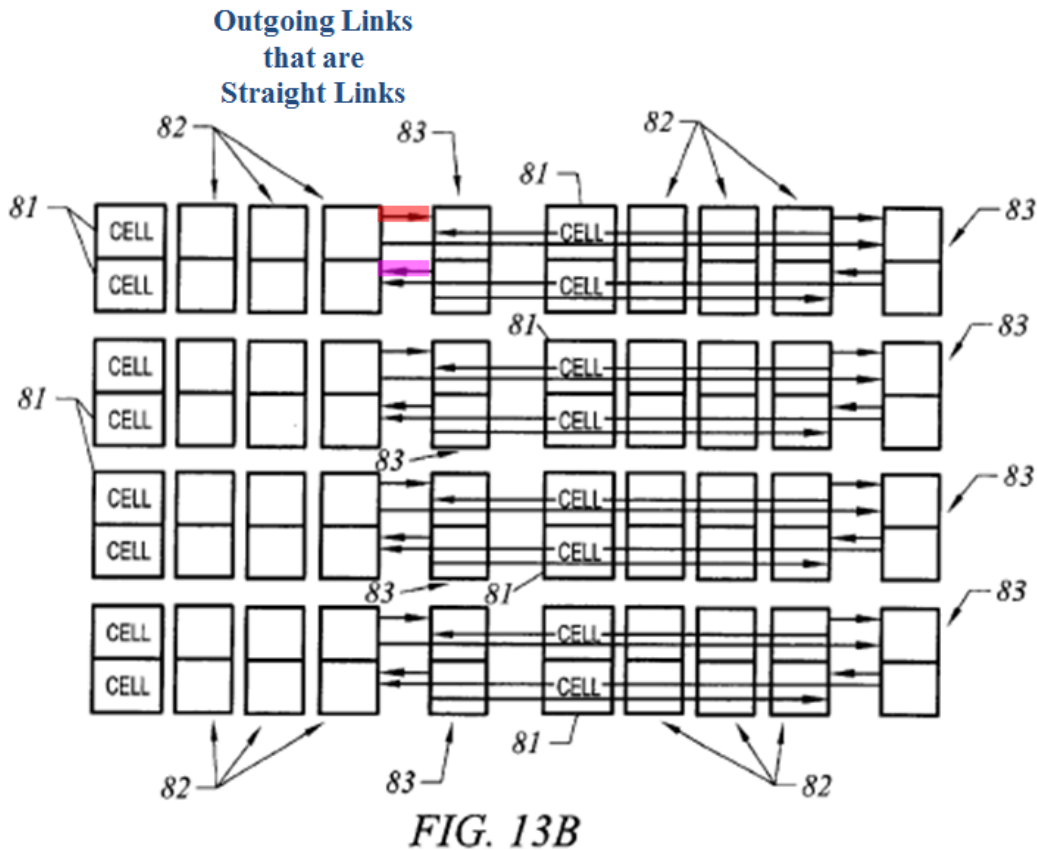


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show outgoing links that are straight links); Ex. 1002, ¶210.)³⁶

³⁶ While the annotations in figure 13A above are used to highlight the straight links in the top subnetwork, a POSITA would have understood that figure 13A shows at least one of the outgoing links is a straight link for each switch in each subnetwork. (Ex. 1002, ¶210.)

Figure 13B also shows that the outgoing links for each switch of each stage include at least one straight link. For example, in addition to the straight links included in figure 13B based on the replication of the subnetworks of figure 13A, additional straight links are shown in annotated figure 13B below, where an additional straight link for stage 3 is shown in red, and a straight link for stage 4 is shown in purple. (Ex. 1002, ¶211.)



(Ex. 1008, FIG. 13B (annotated to show outgoing links that are straight links); Ex. 1002, ¶211.)

Wong further discloses “said outgoing links ... also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in another subnetwork.” For example, *Wong* discloses “zero” such same-stage cross links, as required by claim 11. (Ex. 1002, ¶212.)

Wong also discloses “said outgoing links ... also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in a different numbered stage in one or more other subnetworks.” For example, as can be seen in annotated Figure 13A below, for each switch shown in each subnetwork, at least one of the outgoing links is an inter-stage cross link. The outgoing links for the switches that are inter-stage cross links for the top-most subnetwork are highlighted in blue for stage 1, in green for stage 2, and in red for stage 3. (Ex. 1002, ¶213.)

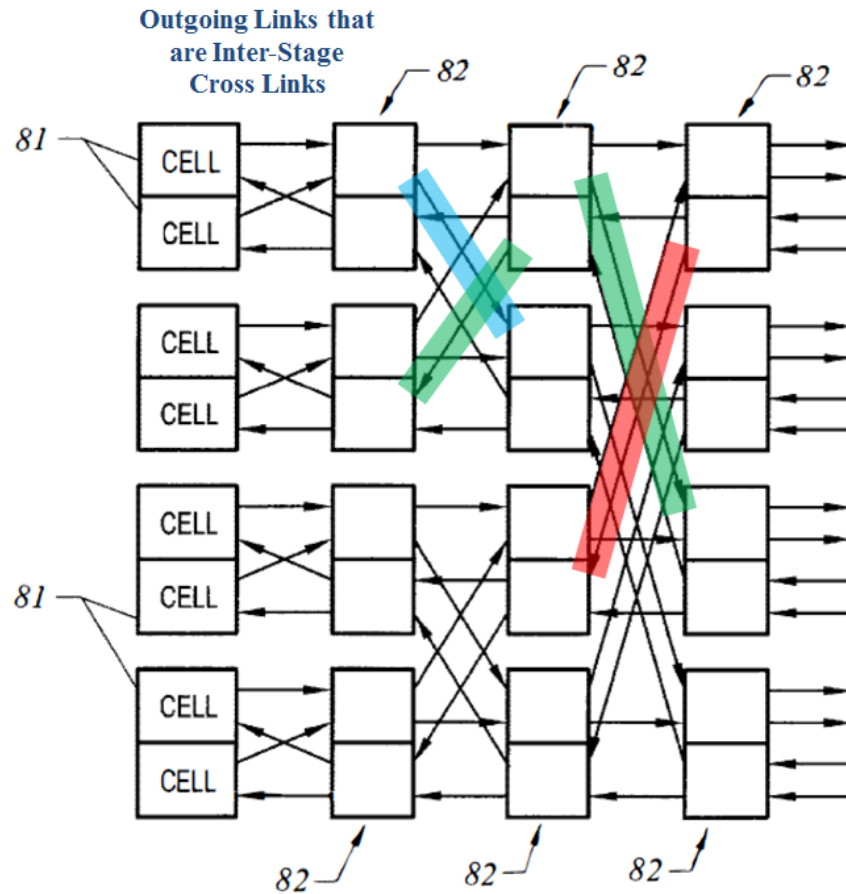
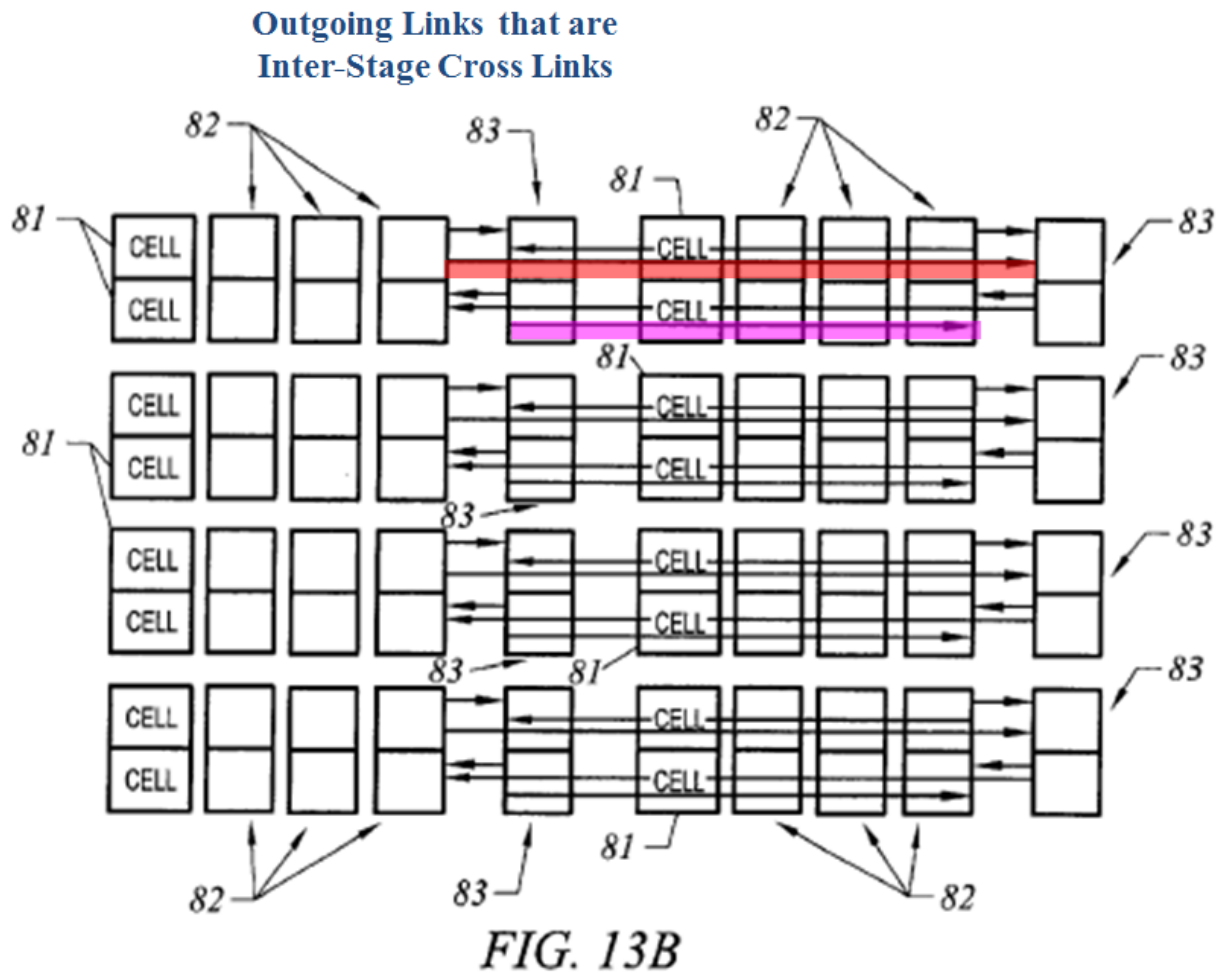


FIG. 13A

(Ex. 1008, FIG. 13A (annotated to show outgoing links that are inter-stage cross links); Ex. 1002, ¶213.)

Figure 13B also shows that the outgoing links in each switch of each stage include at least one inter-stage cross link that connects two different stages in two different subnetworks. For example, in addition to the inter-stage cross links included in figure 13B based on the replication of the subnetworks of figure 13A,

additional inter-stage cross links corresponding to stage 3 (red) and stage 4 (purple) are shown. (Ex. 1002, ¶214.)



(Ex. 1008, FIG. 13B (annotated to show outgoing links that are inter-stage cross links); Ex. 1002, ¶214.)

11. Claim 12

- a) **“The network implemented in a non-transitory medium of claim 11, wherein said cross links between switches of stages in any two said subnetworks are connected as either vertical links only, or horizontal links only, or both vertical links and horizontal links.”**

Wong discloses this claim element. (Ex. 1002, ¶215.) While there is no antecedent basis for “said cross links,” it is assumed that the cross links recited in claim 12 are included in the two types of “zero or more cross links” of the incoming links and the two types of “zero or more cross links” of the outgoing links of claim 11.

Because claim 12 requires “zero or more” same-stage or inter-stage cross links with the recited characteristic, *Wong* discloses the features of claim 12 whether or not *Wong* includes any cross links having the characteristics recited in claim 12. Indeed, even assuming that *Wong* discloses some cross links as recited in claim 11, but those cross links do not have the characteristics recited in claim 12, *Wong* still discloses “zero” cross links as recited in claim 12. (Ex. 1002, ¶215.)

12. **Claim 13**

- a) **“The network implemented in a non-transitory medium of claim 12, wherein each subnetwork with its said stages is replicated in either said rows or said columns of the two-dimensional grid, or**

each subnetwork with said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid, or

each subnetwork with both its said stages, and said horizontal links and said vertical links connected from and said horizontal links and said vertical links connected to is replicated in either said rows or said columns of the two-dimensional grid.”

Claim 13 recites features that track those of claim 3. *Wong* discloses this feature for at least the reasons presented above for claim 3. (*Supra* Section XII.A.3; Ex. 1002, ¶216.)

13. Claim 14

- a) **“The network implemented in a non-transitory medium of claim 12, wherein said horizontal links between switches in two said stages are substantially of equal length and said vertical links between switches in two said stages are substantially of equal length in the entire two-dimensional grid of rows and columns, or**

said horizontal links between switches in two said stages are substantially of a hop length h and said vertical links between switches in two said stages are substantially of a hop length v where $h \geq 0$ and $v \geq 0$.”

Wong discloses this claim element. (Ex. 1002, ¶217.) Claim element 14[a] recites two possible configurations of the horizontal and vertical links separated by the two “or” conjunctions. Thus, to disclose claim element 14[a], the prior art must disclose at least one of these configurations. *Brown*, 265 F.3d at 1351. Moreover, the “vertical links” and “horizontal links” recited in claim element 14[a] further modify the two types of “zero or more cross links” of the incoming links and the two types of “zero or more cross links” of the outgoing links of claim 11 by way of claim 12. (Ex. 1002, ¶217.) Because claim 14 requires “zero or more” same-stage or inter-stage cross links with the recited characteristics, *Wong* discloses the features of claim 14 whether or not *Wong* includes any cross links having the characteristics recited in claim 14.

14. Claim 15

- a) **“The network implemented in a non-transitory medium of claim 12, wherein said one or more cross links are connected between at least one same numbered stage in all said subnetworks or said one or more cross links are connected between at least one set of two not same numbered stages in all said subnetworks.”**

Wong discloses this claim element. (Ex. 1002, ¶218.) While there is no antecedent basis for “said one or more cross links” as recited in claim 15, *Wong* discloses the features of claim 15 to the extent the “said one or more cross links” is interpreted as further limiting the “zero or more” same-stage or inter-stage cross links in the incoming and outgoing links of claim 11 by way of claim 12.

Because claim 15 requires “zero or more” same-stage or inter-stage cross links with the recited characteristics, *Wong* discloses the features of claim 15 whether or not *Wong* includes any cross links having the characteristics recited in claim 15. Indeed, even assuming that *Wong* discloses some cross links as recited in claim 11, but those cross links do not have the characteristics recited in claims 12 and 15, *Wong* still discloses “zero” cross links as recited in claim 15. (Ex. 1002, ¶218.)

15. Claim 17

- a) **“The network implemented in a non-transitory medium of claim 11, wherein some of said stages in a subnetwork comprising a switch of size $(d_i + m) \times (d_o + n)$, where $d_i \geq 2$, $d_o \geq 2$, $m \geq 0$, $n \geq 0$ and each such switch having $d_i + m$ incoming links and $d_o + n$ outgoing links, or**
- one or more of said stages in a said subnetwork comprising six 2:1 multiplexers, or eight 2:1 multiplexers, or four 3:1 multiplexers, or four 4:1 multiplexers.”**

Claim 17 recites features similar to those set forth in claim 9. *Wong* discloses these features for at least the reasons presented above for claim 9. (*Supra* Section XII.A.8; Ex. 1002, ¶219.)

16. Claim 18

- a) **“The network implemented in a non-transitory medium of claim 11, wherein said switches of size $d_i \times d_o$ are either fully populated or partially populated, or**
- said plurality of subnetworks are implemented in a single dimension, or**
- said plurality of subnetworks are either implemented in three or more dimensions or implemented in a 3D integrated circuit device.”**

Claim 18 recites features that track those of claim 10. *Wong* discloses these features for at least the reasons presented above for claim 10. (*Supra* Section XII.A.9; Ex. 1002, ¶220.)

17. Claim 19

- a) **“The network implemented in a non-transitory medium of claim 11, wherein said one or more cross links are connected between at least one same numbered stage in all said subnetworks, and said same numbered stage may be any stage including the final stage.”**

Wong discloses this claim element. (Ex. 1002, ¶221.) While there is no antecedent basis for “said one or more cross links” as recited in claim 19, *Wong* discloses the features of claim 19 to the extent the “said one or more cross links” is interpreted as further limiting the “zero or more” same-stage or inter-stage cross links in the incoming and outgoing links of claim 11.

For instance, in order to disclose the features of claim 19, *Wong* need not disclose any cross links having the requirements added by claim 19. As long as *Wong* discloses “zero or more” cross links with the added characteristics of claim 19, *Wong* discloses the claimed cross links. Even assuming that *Wong* discloses some cross links as recited in claim 11, but those cross links do not have the characteristics recited in claim 19, *Wong* still discloses “zero” cross links as recited in claim 19. (Ex. 1002, ¶221.)

XIII. CONCLUSION

For the reasons given above, Petitioner requests institution of PGR for claims 1-7, 9-15, and 17-19 of the '553 patent, and a finding that the claims are unpatentable based on the above ground.

Respectfully submitted,

Dated: March 18, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,003,553 contains, as measured by the word processing system used to prepare this paper, 18,488 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: March 18, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 18, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,003,553 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent electronically to Patent Owner's litigation counsel listed below:

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