UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. Petitioner

v.

NUCURRENT, INC., Patent Owner

Patent No. 9,300,046

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,300,046

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LIST OF EXHIBITS

| Ex. 1001 | U.S. Patent No. 9,300,046 |
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| Ex. 1002 | Declaration of Dr. Steven Leeb |
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| Ex. 1004 | Prosecution History of U.S. Patent No. 9,300,046 |
| Ex. 1005 | U.S. Patent Application Publication No. 2007/0267718 A1 to Lee ("Lee") |
| Ex. 1006 | Semat and Katz, <i>Physics</i> , Chapters 29-32 (1958) |
| Ex. 1007 | RESERVED |
| Ex. 1008 | RESERVED |
| Ex. 1009 | U.S. Patent Application Publication No. 2009/0096413 A1 to Partovi ("Partovi") |
| Ex. 1010 | IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition (1996) |
| Ex. 1011 | U.S. Patent Application Publication No. 2007/0089773 A1 to Koester ("Koester") |
| Ex. 1012 | U.S. Patent Application Publication No. 2012/0280765A1 |
| Ex. 1013 | U.S. Patent No. 6,432,497 |
| Ex. 1014 | U.S. Patent No. 6,083,842 |
| Ex. 1015 | Reinhold et al., Efficient Antenna Design of Inductive Coupled RFID-Systems with High Power Demand (2007) |
| Ex. 1016 | U.S. Patent No. 4,549,042 |
| Ex. 1017 | U.S. Patent No. 5,812,344 |
| Ex. 1018 | Wheeler, Formulas for the Skin Effect (1942) |

| Ex. 1019 | U.S. Patent No. 7,236,080 ("Kyriazidou") |
|----------|---|
| Ex. 1020 | Alldred et al., "A 1.2 V, 60 GHz radio receiver with onchip transformers and inductors in 90 nm CMOS," Proc. IEEE Compound Semiconductor Integrated Circuits Symp., pp. 51-54, Nov. 2006 ("Alldred") |
| Ex. 1021 | RESERVED |
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| Ex. 1033 | Hu et al., "AC Resistance to Planar Power Inductors and the Quasidistributed Gap Technique," <i>IEEE Transactions on Power Electronics</i> , Vol. 16, No. 4, July 2001 ("Hu") |
| Ex. 1034 | RESERVED |
| Ex. 1035 | IEEE Xplore web page |

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| Ex. 1036 | Kraemer <i>et al.</i> , "Architecture Considerations for 60 GHzPulse Transceiver Front-Ends," CAS 2007 Proceedings Vol. 2, 2007 Int'l Semiconductor Conference (2007) |
|----------|---|
| Ex. 1037 | Varonen et al., "V-band Balanced Resistive Mixer in 65-nm CMOS," Proceedings of the 33rd European Solid-State Circuits Conference (2007) |
| Ex. 1038 | IEEE Xplore web page |
| Ex. 1039 | Lopera et al., "A Multiwinding Modeling Method for High Frequency Transformers and Inductors," <i>IEEE Transactions on</i> <i>Power Electronics</i> , Vol. 18, No. 3, May 2003 |
| Ex. 1040 | Leonavicius <i>et al.</i> , "Comparison of Realization Techniques for PFC Inductor Operating in Discontinuous Conduction Mode," <i>IEEE</i> <i>Transactions on Power Electronics</i> , Vol. 19, No. 2, March 2004 |
| Ex. 1041 | Roshen, W.A., "Fringing Field Formulas and Winding Loss Due to an Air Gap," <i>IEEE Transactions on Magnetics</i> , Vol. 43, No. 8, August 2007 |

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review of claims 1-3, 5-8, 10, 12, 13, 15-21, and 23-29 ("the challenged claims") of U.S. Patent No. 9,300,046 ("the '046 patent") (Ex. 1001), which, according to PTO records, is assigned to NuCurrent, Inc. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claim should be found unpatentable and canceled.

II. MANDATORY NOTICES

<u>Real Parties-in-Interest</u>: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

Related Matters: The '046 patent is at issue in *NuCurrent, Inc. v. Samsung Electronics Co. Ltd.* and *Samsung Electronics America, Inc.*, Case No. 1:19-cv-00798-DLC (S.D.N.Y.). The '046 patent shares the same specification as U.S. Patent No. 8,698,591 ("the '591 patent"); U.S. Patent No. 8,710,948 ("the '948 patent"); and U.S. Patent No. 8,680,960 ("the '960 patent"). Petitioner is concurrently filing petitions challenging these patents. Moreover, Patent Owner has asserted U.S. Patent No. 9,941,729 ("the '729 patent") in the above litigation.

<u>Counsel and Service Information</u>: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel is (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Howard Herr (*pro hac vice*

admission to be requested). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-NuCurrent-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '046 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-3, 5-8, 10, 12, 13, 15-21, and 23-29 should be canceled as unpatentable based on the following grounds:

<u>Ground 1</u>: Claims 1-3, 5-8, 10, 15-21, and 23-29 are unpatentable under pre-AIA 35 U.S.C. § 102 as anticipated by U.S. Patent Application Publication No. 2007/0267718 A1 to Lee ("Lee") (Ex. 1005).

<u>Ground 2</u>: Claim 12 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and U.S. Patent No. 7,030,725 to Ahn ("Ahn") (Ex. 1031).

<u>Ground 3</u>: Claim 13 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and U.S. Patent No. 7,236,080 ("Kyriazidou") (Ex. 1019).

<u>Ground 4</u>: Claim 23 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and U.S. Patent Application Publication No. 2009/0096413 A1 to Partovi ("Partovi") (Ex. 1009).

<u>Ground 5</u>: Claims 5-7 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and Hu et al., "AC Resistance to Planar Power Inductors and the Quasidistributed Gap Technique," *IEEE Transactions on Power Electronics*, Vol. 16, No. 4, July 2001 ("Hu") (Ex. 1033).

<u>Ground 6</u>: Claims 1-3, 6-8, 10, 15-21, and 23-29 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and Alldred *et al.*, "A 1.2 V, 60 GHz radio receiver with onchip transformers and inductors in 90 nm CMOS," *Proc. IEEE Compound Semiconductor Integrated Circuits Symp.*, pp. 51-54, Nov. 2006 ("Alldred") (Ex. 1020).

<u>**Ground** 7</u>: Claim 12 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee, Alldred, and Ahn.

<u>Ground 8</u>: Claim 13 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee, Alldred, and Kyriazidou.

<u>Ground 9</u>: Claim 5 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee, Alldred, and Hu.

The '046 patent issued from U.S. patent application no. 13/797,059 (the '059 application"), filed March 12, 2013. (Ex. 1001, Cover.) The '046 claims priority

to a series of related applications, including Provisional Application No. 61/158,688, filed March 9, 2009. For purposes of this proceeding only however, Petitioner assumes the earliest effective filing date of the '046 patent is March 9, 2009.

Lee published on November 22, 2007. (Ex. 1005, Cover.) Kyriazidou issued on June 26, 2007 (Ex. 1019, Cover.) Ahn issued on April 18, 2006 (Ex. 1031 at Cover.) Hu published in 2001. (Ex. 1033 at Cover.) Therefore, Lee, Kyriazidou, and Ahn are prior art under pre-AIA 35 U.S.C. § 102(b). Partovi was filed May 7, 2008. (Ex. 1009, Cover). Therefore, Partovi is prior art under pre-AIA 35 U.S.C. § 102(e).

Alldred is an IEEE publication that was publicly available to persons interested and skilled in the art in 2006, and at a minimum before March 9, 2009. Similarly, Hu is an IEEE publication that was publicly available to persons interested and skilled in the art in 2001, and at a minimum before March 9, 2009. The Board has routinely held that IEEE publications like Alldred and Hu are printed publications. For example, "[t]he Board has previously observed that 'IEEE is a well-known, reputable compiler and publisher of scientific and technical publications, and we take Official Notice that members in the scientific and technical communities who both publish and engage in research rely on the information published on the copyright line of IEEE publications." *Power* Integrations, Inc., v. Semiconductor Components Industries, LLC, IPR2018-00377,

Paper No. 10 at 10 (July 17, 2018) (quoting *Ericsson, Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41 at 11 (May 18, 2015)). Indeed, in *Ericsson*, the Board "accept[ed] the publication information on the IEEE copyright line on page 1 of [the IEEE reference] as evidence of its date of publication and public accessibility." *Ericsson*, IPR2014-00527, Paper 41, 10-11; *see also Coriant (USA) Inc. v. Oyster Optics, LLC*, IPR2018-00258, Paper 13 at 11 (June 6, 2018); *Microsoft Corp. v. Bradium Techs. LLC*, IPR2016-00449, Paper 9 at 13 (PTAB July 27, 2016) (noting generally that "IEEE publications, such as the one in which Reddy appeared, are distributed widely and intended to be accessible to the public").

Here, Alldred bears the marking "©2006 IEEE" at the top of the title page (page 1) and the footer of the first page of the article, and the copyright page bears the marking "Copyright © 2006 by The Institute of Electrical and Electronics Engineers, Inc." (Ex. 1020 at title page (page 1), copyright page (page 3); *see also* Ex. 1035 at 1 ("Published in: 2006 IEEE Compound Semiconductor Integrated Circuit Symposium" and "Date Added to IEEE Xplore: 26 February 2007" and "Publisher: IEEE").) With such markings, Alldred is similar to a reference that the Board recently found is a printed publication in *Microsoft Corp. v. Koninklijke Philips N.V.*, IPR 2017-00890, Paper 49 at 19 (Sept. 6, 2018). Moreover, several

IEEE publications that were published before the alleged invention date of the '046 patent, and that do not have any co-authors in common with Alldred, cite to Alldred, demonstrating that Alldred was publicly accessible before March 9, 2009. (Ex. 1036 at copyright page (page 3) ("Copyright © 2007 by the Institute of Electrical and Electronics Engineers."), 428 (citation [9] is to Alldred and includes a date of "2006"); Ex. 1037 at ii ("Copyright © 2007 by the Institute of Electrical and Electronics Engineers, Inc."), 363 (citation [3] is to Alldred and includes a date of "Nov. 2006").)

Similarly, Hu bears the marking "IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 16, NO. 4, JULY 2001" at the top of pages 558, 560, 562, 564, and 566, the title page similarly indicates "JULY 2001 VOLUME 16 NUMBER 4," the copyright page bears the marking "© 2001 by The Institute of Electrical and Electronics Engineers, Inc.," and the footer on page 558 bears the marking "©2001 IEEE." (Ex. 1033 at Title page (page 1), copyright page (page 2), 558, 560, 562, 564, 566; *see also* Ex. 1038 at 1 ("Date of Publication: Jul 2001" and "Published in: IEEE Transactions on Power Electronics (Volume: 16, Issue: 4 , Jul 2001)" and "Publisher: IEEE").) With such markings, Hu is similar to the *Microsoft* case referenced above. *Microsoft*, IPR2017-00890, Paper 49 at 19 (Sept. 6, 2018). Moreover, several IEEE publications that were published before the alleged invention date of the '046 patent, and that do not have any co-authors in common with Hu, cite to Hu, demonstrating that Hu was publicly accessible before March 9, 2009. (Ex. 1039 at title page (page 1) ("MAY 2003"), copyright page (page 2) ("Copyright © 2003 by The Institute of Electrical and Electronics Engineers, Inc."), 896 ("MAY 2003" and "© 2003 IEEE"), 906 (citation [17] is to Hu and includes a date of "July 2001"); Ex. 1040 at title page (page 1) ("MARCH 2004"), copyright page (page 3) ("Copyright © 2004 by The Institute of Electrical and Electronics Engineers, Inc."), 531 ("MARCH 2004" and "© 2004 IEEE"), 541 (citation [15] is to Hu and includes a date of "July 2001"); Ex. 1040 at title page (page 1) ("AUGUST 2007), copyright page (page 2) ("Copyright © 2004 by The Institute of Electrical and Electronics Engineers, Inc."), 531 ("MARCH 2004" and "© 2004 IEEE"), 541 (citation [15] is to Hu and includes a date of "July 2001"); Ex. 1041 at title page (page 1) ("AUGUST 2007), copyright page (page 2) ("Copyright © 2004 by The Institute of Electrical and Electronics Engineers, Inc."), 5387 ("AUGUST 2007" and "© 2007 IEEE"), 3394 (citation [2] is to Hu and includes a date of "Jul. 2001").)

Therefore, for all of the foregoing reasons, Alldred and Hu are printed publications and qualify as prior art under pre-AIA 35 U.S.C. § 102(b) by virtue of their publication in 2006 and 2001, respectively, or at least under pre-AIA 35 U.S.C. § 102(a) by virtue of their publication before March 9, 2009 (e.g., as demonstrated by citations in various other references to Alldred and Hu as discussed above).

None of these references were considered by the Patent Office during prosecution of the '046 patent. (*See*, *e.g.*, Ex. 1001, Cover ("References Cited"); Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '046 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering, or a similar discipline and at least two years additional relevant experience with power electronics, including design or manufacturing of inductors. (Ex. 1002, $\P\P15$ -16.)¹ More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '046 PATENT AND THE PRIOR ART

A. The '046 Patent

The '046 patent, titled "Method for Manufacture of Multi-Layer-Multi-Turn High Efficiency Inductors," is directed to "an inductor having a plurality of conductor layers separated by layers of insulator," "for incorporation within electric circuits." (Ex. 1001, Abstract, 1:37-40, 4:23-24; *see also id.* at 4:25-26 (disclosing the inductor described is "most notably" for "electrical circuits that

¹ Petitioner submits the declaration of Dr. Steven Leeb (Ex. 1002), an expert in the field of the '046 patent. (Ex. 1002, ¶¶1-16; Ex. 1003.)

operate within and above the radio frequency range of at least 3 kHz"); Ex. 1002, \P 30-34.) The '046 patent discloses that one of its objectives is "a reduction of resistance loss . . . of the inductor structure" with a "multi-layer wire configuration." (Ex. 1001, 4:16-22.)

With reference to figure 1, the '046 patent discloses "a high-level diagram of an inductor 100 for use in an electronic or electrical circuit . . . compris[ing] a coil 102 and a multi-layer wire 104," that "may have a plurality of turns 122 . . . around a central axis point 124." (*Id.*, 15:8-11, 16:31-36.)



(*Id.*, FIG. 1.)

The '046 patent further discloses various embodiments including "a double turn circular spiral-solenoidal coil" in figure 3B "where each turn has N layers," and "where 'N' is a number equal to or greater than one." (*Id.*, FIG. 3B, 12:34-36, 16:39-46.)



F I G. 3B

(Id., FIG. 3B.)

The '046 patent admits that many properties of inductors were known. For example, it admits that

In an inductor, electric current travels through the metallic coil generating a magnetic flux that is proportional to the amount of electric current. A change in electrical current elicits a corresponding magnetic flux proportional to the amount of current, which in turn, generates an electromotive force (EMF), measured in volts, that opposes the change in current. Inductance is a measure of the amount of EMF generated per unit change in current.

(Id., 1:55-65.) The '046 patent further admits that

An inductor is generally an electrical component or circuit that introduces inductance into a circuit. Inductance is generally a property of an electric circuit by which an electromotive force is induced as the result of a changing magnetic flux. The magnetic flux may change instantaneously or over time and thus become a time-varying magnetic flux. The magnetic flux is typically generated when a change in a frequency, a magnitude, a waveform shape, or combinations thereof, of the propagating electrical current occurs therewithin.

(*Id.*, 14:17-27; Ex. 1002, ¶33.)

The '046 patent also admits that impacts of the "skin depth" phenomenon on current distribution within conductors is well known, and explains that the skin depth "defines the electrical current cross-sectional area that is carries most of the current (is active) in the conducting wire of an inductor" (Ex. 1001, 2:50-55) and that "[w]ith higher frequencies, current that normally flows through the entire cross section of the wire comprising the inductor becomes restricted to its surface," thereby increasing resistance. (Ex. 1001, 2:61-67; Ex. 1002, ¶34.)

B. Lee

Lee relates to "a multilayer winding inductor" with "a plurality of looped conductive traces overlapping and separated from each other" and "a multi-level interconnect structure." (Ex. 1005, Abstract, ¶[0004]; Ex. 1002, ¶¶36-39.)

Lee discloses a top-down view of an embodiment of a multilayer winding inductor in figure 4A and a cross-section along line 4C-C' in figure 4C, which reveals the multilayer structure inside. (*Id.*, $\P[0031]$.)



FIG. 4A

(Id., FIG. 4A.)



FIG. 4C

(Id., FIG. 4C.)

Lee discloses that the inductor "includes two multi-level interconnect structures . . . embedded in an insulating layer on a substrate." (*Id.*, ¶[0031].) The interconnect structures further include "looped conductive traces" 311 and 321, and conductive plugs 323 and 325. (*Id.*, ¶[0031].) The conductive traces and plugs "may be copper, aluminum, or a combination thereof." (*Id.*, ¶[0033].) Lee also discloses that the insulating layer "may be dielectric layers 302, 304, 306, 308, 310, 312, and 314 successively deposed on the substrate." (*Id.*)

Lee further discloses that "external or internal circuits provide a current passing through the lower multi-level interconnect structure . . . and utilize the inductance induced by the inductor. (*Id.*, $\P[0034]$.) And "since the inductor includes two overlapping lower conductive traces, higher inductance can be obtained." (*Id.*, $\P[0035]$.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.* at 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. Toyota Motor Corp.

v. Cellport Systems, Inc., IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.,* 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior art references and the challenged claims, Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.² (Ex. 1002, ¶35.)

² Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '046 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

IX. DETAILED EXPLANATION OF GROUNDS

As discussed below, claims 1-3, 5-8, 10, 12, 13, 15-21, and 23-29 are unpatentable in view of the prior art. (Ex. 1002, \P 40-146.)

A. Ground 1: Lee Anticipates Claims 1-3, 5-8, 10, 15-21, and 23-29

1. Claim 1

Preamble: A method of manufacturing an inductor structure, the method comprising the following steps:

Lee discloses this limitation. (Ex. 1002, \P [41-42.) For example, Lee discloses a multi-layer "winding inductor." (*See*, *e.g.*, Ex. 1005, \P [0031], FIGS. 4A-4C; Ex. 1002, \P 41.) A plan view of the inductor is illustrated in figure 4A (reproduced below), showing the uppermost looped conductive trace 313 and other components. (Ex. 1005, \P [0020]-[0022], [0031]-[0034], FIG. 4A.)



(Ex. 1005, FIG. 4A (annotated); Ex. 1002, ¶41.)

As discussed below, Lee discloses how to construct the multilayer winding inductor ("method of manufacturing an inductor structure"). (See infra Sections IX.A.1(a)-(d); Ex. 1002, \P 42.)

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a) providing a first conductor layer and a second conductor layer, the first conductor layer and the second conductor layer being electrically conductive;

Lee discloses this limitation. (Ex. 1002, ¶¶43-44.) For example, as illustrated in annotated figure 4C below, Lee discloses that the inductor includes looped conductive trace 311 ("first conductor layer"), embedded in dielectric layer 310, and looped conductive trace 311 ("second conductor layer"), embedded in dielectric layer dielectric layer 308. (Ex. 1005, ¶¶[0024]-[0025], [0029], [0031]; *see also id.* at ¶¶[0026]-[0028], [0032]-[0033]; Ex. 1002, ¶¶43.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶43.)

Lee also discloses that these conductive traces 311 ("first conductor layer" and "second conductor layer") are electrically conductive at least because Lee describes these traces 311 as conductive traces formed from "copper, aluminum or combinations thereof," and further discloses a current may pass through these conductive traces to utilize the inductance. (*See, e.g.*, Ex. 1005, ¶¶[0025], [0026], [0034].) Accordingly, Lee discloses "providing a first conductor layer and a second conductor layer, the first conductor layer and the second conductor layer being electrically conductive." (Ex. 1002, ¶44.)

b) positioning an insulator layer between the first conductor layer and the second conductor layer; and

Lee discloses this limitation. (Ex. 1002, ¶45.) For example, as shown in the annotated figure 4C below, Lee discloses positioning a dielectric layer 308 ("insulator layer") in the space between two conductive traces 311 ("the first conductor layer and the second conductor layer"). (Ex. 1005, ¶ $[0025]^3$ (disclosing that "[t]he multi-level interconnect is embedded in the dielectric layers 308, 310 and 312, comprising a plurality of looped conductive traces 311 formed in the dielectric layers" and that "looped conductive traces 311 . . . are separated from each other"); Ex. 1002, ¶45.)

³ The embodiment of figures 4A-4C incorporates the disclosure of the embodiment of figures 3A-3C. (Ex. 1005, ¶[0031].)



(Ex. 1005, FIG. 4C (annotated to show that dielectric layer 308 is positioned in the space between two conductive traces 311); Ex. 1002, ¶45.) It was well known to those of ordinary skill in the art that dielectric materials are electrical insulators. (Ex. 1002, ¶45.) Furthermore, Lee reflects this understanding and discloses that dielectric layer 308 is an "insulator" layer, as claimed. (Ex. 1005, ¶[0031] ("the **insulating** layer may be dielectric layers 302, 304, 306, 308, 310, 312 and 314 successively disposed on the substrate 300.") (emphasis added); *see also id.* at ¶[0024]; Ex. 1002, ¶45.)

c) connecting the first conductor layer and the second conductor layer in an electrically parallel connection with at least two connectors, each connector having an electrical impedance;

Lee discloses this limitation. (Ex. 1002, ¶¶46-47.) For example, referring to the annotated figure 4C below, Lee discloses multiple conductive plugs 315 ("at least two connectors") electrically connecting conductive traces 311 in parallel ("connecting the first conductor layer and the second conductor layer in an electrically parallel connection") that are separated by dielectric layer 308. (Ex. 1005, ¶[0026] ("The conductive plugs 315 are disposed between the looped conductive traces 311 to serve as **an electrical connection therebetween**, in which **at least two conductive plugs 315** are disposed between the neighboring looped conductive traces 311. Thus, one of the conductive traces 311 is coupled with other conductive traces 311 **in parallel**") (emphasess added); Ex. 1002, ¶46.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶46.)

Furthermore, Lee discloses that conductive traces 311 are connected in parallel, by conductive plugs 315, which "may be copper, aluminum or a combination thereof." (*Id.*, ¶[0026].) Both copper and aluminum have an electrical impedance because all materials have an electrical impedance. (Ex. 1002, ¶47; Ex. 1001, 14:46-50 (explaining that resistance of a copper wire "at a frequency of 1 MHz is almost four times the dc value").) Indeed, the '046 patent admits that connectors can be those utilized in semiconductor technology or "**any conductive material**." (Ex. 1001, 16:13-19.) A POSITA would have therefore understood

that Lee discloses "each connector having an electrical impedance." (Ex. 1002, ¶47.)

d) wherein, when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current.

Lee discloses or suggests this limitation. (Ex. 1002, \P 48-56.) For clarity, this limitation is discussed below in two parts.

First, Lee discloses that "when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor." (*Id.*, ¶49.) Lee discloses that a current passes through the entire inductor of figure 4A including the "upper multi-level interconnect structure (i.e., upper conductive (Ex. 1005, ¶[0034].) The "upper conductive trace" refers to the trace)." conductive traces 311 (Ex. 1002, ¶49), which as discussed above disclose the claimed "first" and "second" conductor layer. (Supra Section IX.A.1(a).) A POSITA would have understood and readily recognized that the propagation of electrical current through the inductor (including the "first conductor layer") would necessarily result in generation of magnetic flux within the inductor because that is an inherent physical property of an inductor. (Ex. 1002, ¶49; see also Ex. 1002, The '046 patent reflects this understanding, and acknowledges that ¶¶18-25.) electric current traveling through a conductive coil will generate a magnetic flux.

(Ex. 1001, 1:55-57 ("In an inductor, electric current travels through the metallic coil generating a magnetic flux that is proportional to the amount of electric current."); Ex. 1002, ¶49.)

Second, Lee discloses that "a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current." (Ex. 1002, ¶50.)

To begin, as admitted by the '046 patent, the claimed limitation is an inherent property of an inductor. (*Id.*, $\P51$; Ex. 1001, 1:55-65, 14:17-27.) Therefore, as per the '046 patent, when there is a change in the inductor current's frequency, magnitude, or waveform shape, an inductance and a magnetic flux are necessarily generated. (Ex. 1002, $\P51$.) Accordingly, Lee necessarily discloses this feature because Lee discloses using an inductor. (*Id.*)

Furthermore, Lee discloses that a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current through its inductor because Lee discloses that an "inductance is induced" when a current passes through an inductor. (Ex. 1005, ¶[0034] (disclosing that "the external or internal circuits provide a current passing through" the inductor "and utilize the **inductance induced by the inductor**") (emphasis added).) "Inductance" is defined by the IEEE Standard Dictionary of Electrical and Electronics Terms as "the property of an electric circuit by virtue of which a

varying current induces an electromotive force in that circuit or in a neighboring circuit." (Ex. 1010 at 517 (emphasis added); Ex. 1002, ¶52.) Thus, given that Lee discloses the inductor induces "inductance" when an electric current passes through it, a POSITA would have understood that the current in Lee necessarily has "a change in at least one of a frequency, a magnitude, or a waveform shape" because such a change in necessary to induce an inductance. (Ex. 1002, ¶52.)

This understanding is consistent with Lee's disclosure that its inductors are "[c]onventionally . . . employed in integrated circuits designed for radio frequency (RF) band." (Ex. 1005, ¶[0005] (emphasis added); Ex. 1002, ¶53.) A POSITA would have understood that an RF circuit is an electrical circuit where a current oscillates at a frequency other than zero and is associated with circuits that can operate at very high frequencies (for example, frequencies as high as 100 GHz. (Ex. 1010 at 860 ("The present practicable limits of radio frequency are roughly 10 kHz (kilohertz) to 100 000 MHz (megahertz)"); Ex. 1020 at 1 (disclosing a 60 GHz RF signal).) Therefore, the current in an RF circuit necessarily changes in magnitude because it is oscillating. (Ex. 1002, ¶53.)

A change in the magnitude of the electrical current propagating through the inductor would have necessarily changed the magnetic flux generated within the inductor. (Ex. 1002, ¶54.) As explained by Dr. Leeb, generation of a magnetic field is associated with generation of magnetic flux, which changes with a change

in current through the inductor. (Ex. 1002, ¶54; Ex. 1006, 592-593, 601 ("When current is sent through a coil, a magnetic field is established through it, and any changes in the current generate changes in the magnetic flux through the coil."); Ex. 1006, 554-555; Ex. 1009, ¶[0212] (disclosing that a coil constructed with two or more layers can achieve a higher magnetic flux density than a single layer coil), FIG. 18.)

Furthermore, a POSITA would have understood that any change in current passing through Lee's inductor, including turning the circuit on for the first time, would necessarily create a transient event or transient period. (Ex. 1002, ¶55.) For instance, a current passing through Lee's circuit in response to the abrupt application of a DC voltage would necessarily take a finite amount of time, known as the transient period, to reach a steady-state value. (Ex. 1006, 604; *see also id.* at 603, 605; Ex. 1002, ¶55.) During this transient interval, at least the magnitude of current passing through the inductor would change (from zero to a value determined primarily by the series resistance in the circuit), and as discussed above, any change in the current would necessarily result in a change in the magnetic flux generated within the inductor.

Accordingly, Lee discloses "a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current," because the magnitude of the current propagating through the primary coil changes, which will necessarily generate a change in magnetic flux. (Ex. 1002, ¶56; *see* Ex. 1001, 1:55-65.)

- 2. Claim 2
 - a) The method of claim 1 further generating an electromotive force when at least one of the frequency, the magnitude, or the waveform shape is changed.

Lee discloses this limitation because the claimed feature is merely an inherent property of an inductor, where **any** change in the current flowing through the inductor results in the generation of an EMF (electromotive force) across the inductor that opposes this change in current. (Ex. 1002, ¶57; Ex. 1001, 1:55-65, 14:17-27.) Therefore, because Lee discloses an inductor, an electromotive force will necessarily be generated when there is change in "at least one of the frequency, the magnitude, or the waveform shape" of electrical current flowing through the inductor. (Ex. 1002, ¶57.)

Moreover, as discussed above in Section IX.A.1(d), Lee discloses passing a current through its inductor to induce an inductance. (*See supra* Section IX.A.1(d); Ex. 1005, ¶[0034] ("the external or internal circuits provide a current passing through" the inductor "and utilize the **inductance induced by the inductor**") (emphasis added).) Given that inductance is a measure of EMF generated in response to a change in current per unit time, (*see* Ex. 1006, 601; Ex. 1010 at 517), an "electromotive force" is necessarily generated in Lee's inductor when there is a

change in current through the inductor ("when at least one of the frequency, the magnitude, or the waveform shape of the propagated electrical current is changed"), as would occur with excitation of Lee's inductor by RF currents. (Ex. 1002, ¶58.)

Furthermore, as discussed in Section IX.A.1(d), the current through Lee's inductor necessarily changes (e.g., from zero to a finite, steady-state value) in response to an abruptly applied DC voltage, and such a change in current would necessarily generate an EMF in the inductor. (Ex. 1002, ¶59.)

- 3. Claim 3
 - a) The method of claim 1 further providing a magnitude of the magnetic flux proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current.

Lee discloses this limitation. (Ex. 1002, $\P\P60-62$.) As admitted by the '046 patent, the claimed limitation is an inherent property of an inductor. (*Id.*, $\P60$.) For example, the '046 patent admits that "[i]n an inductor, electric current travels through the metallic coil generating a magnetic flux that is proportional to the amount of electric current" and that "[a] change in electrical current elicits a corresponding magnetic flux proportional to the amount of current." (Ex. 1001, 1:55-61 (emphases added); Ex. 1002, $\P60$.) Therefore, Lee necessarily

discloses claim 3 because figures 4A-4C of Lee disclose an inductor. (Ex. 1002, ¶60.)

Furthermore, because Lee at least discloses a change in the magnitude of the current in its inductor (e.g., in response to current oscillating at an RF frequency and during the transient period following application of DC voltage) as discussed above in Section IX.A.1(d), Lee necessarily discloses "providing a magnitude of the magnetic flux is proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current." (*See supra* Section IX.A.1(d); Ex. 1002, ¶61.)

Furthermore, as discussed above in Section IX.A.1(d), a magnetic flux is a measure of magnetic field that passes through a specific area. (*Supra* Section IX.A.1(d); Ex. 1002, ¶62; Ex. 1006, 554-555.) Accordingly, a POSITA would have recognized that Lee discloses "a magnitude of the magnetic flux is proportional to the amount of change of...the magnitude...of the electrical current," given that the magnetic field that passes through a specific area is also proportional to the change in electrical current through the inductor. (Ex. 1002, ¶62; *see also* Ex. 1006, 592-593, 601 ("When current is sent through a coil, a magnetic field is established through it, and any changes in the current generate changes in the magnetic flux through the coil.").)
4. Claim 5

a) The method of claim 1 further providing a thickness of the first conductor layer about equal to a thickness of a skin depth of the first conductor layer at a given frequency.

Lee discloses this limitation. (Ex. 1002, $\P\P63-64$.) To start, a POSITA would have understood that the claimed "skin depth," as admitted by the '046 patent, is an inherent material property, which defines an outer portion of a conductor extending to a certain depth below a conductor's surface where most of the current flows. (Ex. 1002, $\P63$.)

This limitation is disclosed by Lee. (Ex. 1002, $\P64$.) Lee discloses that "[f]or example, . . . the looped conductive layer 311 has a thickness of about 0.53 µm. (Ex. 1005, $\P[0027]$.) Lee also discloses that the conductive layer 311 is formed of copper. (*Id.*, $\P[0026]$.) Lee further discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (*Id.*, $\P[0005]$.) The RF band includes several frequencies, ranging from about 10 kHz to 100 GHz. (Ex. 1002, $\P64$; Ex. 1010 at 860 ("The present practicable limits of radio frequency are roughly 10 kHz (kilohertz) to 100 000 MHz (megahertz).").) Therefore, at certain operating frequencies in the RF band, Lee's conductive layer 311 ("first conductor layer") has a "thickness . . . about equal to a thickness of a skin depth." (*Id.*) For example, at 15.13 GHz, which is a frequency within the RF band, the skin depth of copper (with a

resistivity of 1.678 10^{-8} ohm-meters and relative permeability of 1) is 0.53 µm, the same thickness as Lee's conductive trace 311 ("first conductor layer"). (*Id.* (citing https://chemandy.com/calculators/skin-effect-calculator.htm).)

5. Claim 6

a) The method of claim 1 further providing a thickness of the first conductor ranging from about 1.25 times to about 4 times a thickness of a skin depth of the first conductor layer at a given frequency.

Lee discloses this feature. (Ex. 1002, ¶¶65-66.) Lee discloses that "[f]or example, . . . the looped conductive layer 311 has a thickness of about 0.53 μ m. (Ex. 1005, ¶[0027].) Lee also discloses that the conductive layer 311 is formed of copper. (*Id.*, ¶[0026].) Lee further discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (*Id.*, ¶[0005].) The RF band includes several frequencies, including high frequencies such as 30 GHz and 100 GHz. (Ex. 1002, ¶65; Ex. 1010 at 860 ("The present practicable limits of radio frequency are roughly 10 kHz (kilohertz) to 100 000 MHz (megahertz).").)

Therefore, at certain operating frequencies in the RF band, Lee's conductive layer 311 ("first conductor layer") has a "thickness . . . about equal to or greater than a thickness of" its skin depth at that frequency. (Ex. 1002, $\P66$.) For example, at 30 GHz, which is a frequency within the RF band, the skin depth of copper (with a resistivity of 1.678 10^{-8} ohm-metres and relative permeability of 1)

is 0.3764 μ m. (*Id.* (citing https://chemandy.com/calculators/skin-effectcalculator.htm).) Similarly, at 100 GHz, the skin depth of copper is 0.2062 μ m, which is less than half the thickness of Lee's conductive layer 311. (*Id.*) At such frequencies, the thickness of looped conductive layer 311 (i.e., 0.53 μ m) is 1.4 times the skin depth at 30 GHz or 2.6 times the thickness at 100 GHz. (*Id.*)

6. Claim 7

a) The method of claim 1 further providing a thickness of the second conductor ranging from about 1.25 times to about 4 times a thickness of a skin depth of the second conductor layer at a given frequency.

Lee discloses this feature for at least the same reasons as it discloses claim 6. (Ex. 1002, $\P67$.) Specifically, the "second conductor layer" in Lee is one of the three conductive traces 311. (*See supra* Section IX.A.1(a).) Therefore, the analysis for claim 6 applies to the "second conductor layer" as well.

7. Claim 8

a) The method of claim 1 further providing a first conductor layer thickness about the same as a second conductor layer thickness.

Lee discloses this limitation. (Ex. 1002, $\P68$.) For example, as discussed above in Sections IX.A.1(a), looped conductive traces 311 correspond to the "first conductor layer" and the "second conductor layer." (*See supra* Sections IX.A.1(a).) Furthermore, because Lee discloses that "the looped conductive trace 321 may have the same thickness as the looped conductive traces 311" (Ex. 1005, $\P[0032]$), Lee discloses that each of the looped conductive traces 311 has the same thickness because plural conductive traces 311 have the same thickness as conductive trace 321. As a result, the conductive traces 311 have the same thicknesses. (Ex. 1002, $\P68$.)

8. Claim 10

a) The method of claim 1 further providing a thickness of a first skin depth of the first conductor layer about the same as a thickness of a second skin depth of the second conductor layer.

Lee discloses this limitation. (Ex. 1002, ¶69.) As discussed above in Section IX.A.4, a skin depth for a conductor, e.g, Lee's inductor, is determined based on the frequency of the current propagating through the conductor, and intrinsic properties of the conductor, including conductivity and permeability. (See supra Section IX.A.4.) At least because Lee discloses that traces 311 ("the first conductor layer" and "the second conductor layer") "may be copper, aluminum or a combination thereof," Lee discloses in an embodiment that these traces are made of the same material and, in that embodiment, the traces necessarily share the same conductivity and permeability. (Ex. 1005, [0026]; Ex. 1002, ¶69.) Lee also discloses that the first and second conductor layers share the same thickness and geometry. (Ex. 1005, ¶[0032]; Ex. 1002, ¶69.) Furthermore, because traces 311 belong to the same inductor, they are subject to the same excitation current and therefore the same excitation frequency. (Ex. 1002, ¶69.) Accordingly, each of traces 311 has about the same skin depth because they have the same current, frequency, conductivity, permeability, and geometry. (*Id.*) Thus, Lee discloses "a thickness of a first skin depth of the first conductor layer is about the same as a thickness of a second skin depth of the second conductor layer." (*Id.*)

9. Claim 15

a) The method of claim 1 further forming at least one of the first and second conductor layers from a thermally conductive material.

Lee discloses this limitation. (Ex. 1002, ¶70.) Lee discloses that the looped conductive traces 311 ("the first and second conductor layers") may be copper, which a POSITA would have understood is thermally conductive. (*Id.*; Ex. 1005, ¶[0026]; Ex. 1011 at ¶[0039] (describing copper as a "thermally conductive material"); Ex. 1013 at 4:37-39 (disclosing copper as "having a high thermal conductivity").)

10. Claim 16

a) The method of claim 1 further providing the connector comprising at least one of a via, a solder, a tab, a wire, a pin, a rivet, a filled mesh structure, a conductive polymer, a conductive composite, a conductive adhesive, a liquid metal, or a foamed metal.

Lee discloses this limitation in at least two ways. (Ex. 1002, ¶¶71-74.)

First, Lee discloses the claimed "connector" are conductive plugs 315, which may be "copper, aluminum or a **combination thereof**." (Ex. 1005, ¶[0026]

(emphasis added).) Accordingly, any of conductive plugs 315 in Lee ("connector") disclose the claimed "conductive composite." (Ex. 1002, ¶72.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶72; supra Section IX.A.1(c).)

Second, a POSITA would have understood that conductive plugs 315, connecting the looped conductive traces 311 ("the first and second conductor layers"), disclose the claimed "via[s]." (Ex. 1014 at 2:2-4 (describing that a "via plug...is comprised of a conductive material and is disposed within a via hole..."), 2:18-20 ("a copper plug within a via hole may contact the insulating layer surrounding the via hole.") (emphases added); Ex. 1002, ¶73.)

A POSITA would have recognized that a "via" was well-known in the electrical engineering field as an electrical connection between adjacent layers of, for example, a multi-layer printed circuit board, or PCB. (Ex. 1002, ¶74.) Indeed, the '046 patent admits that a via is "an electrically conductive connection from one layer to another." (Ex. 1001, 15:1-3; 16:13-20.) Just as the vias 144 of figure 4F in the '046 patent provide an electrical connection between conductive layers 138 and 140, the conductive plugs 315 as disclosed by Lee electrically connect the conductive traces 311 ("first conductor layer" and "second conductor layer"). (Ex. 1005, ¶[0026]; Ex. 1002, ¶74.) Accordingly, any of conductive plugs 315 in Lee ("connector") discloses the claimed "via." (Ex. 1002, ¶74.)

11. Claim 17

a) The method of claim 1 further providing at least two connectors electrically connecting the first conductor layer and the second conductor layer in parallel.

Lee discloses this limitation. (Ex. 1002, $\P75$.) For example, Lee discloses that at least two conductive plugs 315 ("at least one connector") electrically connect ends of conductive traces 311 (the first conductor layer and the second conductor layer) such that "one of the conductive traces 311 is coupled with other conductive traces 311 **in parallel**." (Ex. 1005, $\P[0026]$ (emphasis added), $\P[0010]$ ("The first conductive plug is disposed between the looped conductive traces to **electrically connect** the looped conductive traces, in which at least two first

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conductive plugs are disposed between the neighboring looped conductive traces.") (emphasis added); *see also id.* at claim 1 (disclosing conductive plugs "electrically connecting" looped conductive traces), claim 11 ("first looped conductive traces coupled in parallel"), claim 15 ("at least one pair of first conductive plugs connecting the first looped conductive traces in parallel"), claim 17; Ex. 1002, ¶75.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶75.)

12. Claim 18

a) The method of claim 1 further forming a structure in which the first and second conductor layers are positioned in about a parallel orientation, a perpendicular, or at an angular relationship

therebetween.

Lee discloses this limitation. (Ex. 1002, ¶¶76-77.) For example, Lee discloses that looped conductive traces 311 ("the first and second conductor layers") "overlap and are separated from each other." (Ex. 1005, ¶[0025]; *see also id.* at FIG. 4C.) Thus, a POSITA would have understood that traces 311 are positioned "in about a parallel orientation, about perpendicular, or at an angular relationship with respect to each other" because the conductive traces 311 are in different planes. (Ex. 1002, ¶77.)

- 13. Claim 19
 - a) The method of claim 1 further providing a third conductor layer and a fourth conductor layer electrically connected in parallel wherein the first and second conductor layers are connected electrically in parallel and are further connected electrically in series with the third and fourth conductor layer.

Lee discloses this limitation. (Ex. 1002, ¶¶78-83.)

First, Lee discloses "a third conductor layer and a fourth conductor layer electrically connected in parallel." (*Id.*, ¶79.) For example, as shown in the annotated figure 4C below, Lee's second multi-level interconnect structure includes a looped conductive trace 321 ("third conductor layer") embedded in a dielectric layer 306 and another looped conductive trace 321 ("fourth conductor

layer") embedded in dielectric layer 304. (Ex. 1005, ¶[0032]; see also id. at ¶[0031].)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶79.)

Furthermore, Lee discloses that looped conductive traces 321 ("third conductor layer" and "fourth conductor layer") are electrically connected in parallel by conductive plugs 323. (Ex. 1005, ¶[0035] ("since the **lower conductive trace** includes multilayer winding structure in which each conductive trace is connected **in parallel**, the series resistance can be reduced to maintain the Q value of the inductor.") (emphasis added); ¶[0034] (disclosing that "the multi-level interconnect structure formed by **the looped conductive traces 321 serves as**

another lower conductive trace of the inductor") (emphasis added); see also id. at $\P[0033]$ ("The conductive plugs 323 are disposed between the looped conductive traces 321 to serve as an electrical connection therebetween...thereby reducing the resistance of the multi-level interconnect structure to further reduce the series resistance."), *id.* at claim 20 ("the third looped conductive traces are coupled in parallel"); Ex. 1002, ¶80.)

Indeed, a POSITA would have also understood that looped conductive traces 321 are electrically connected in parallel based on figure 4C. (Ex. 1002, ¶81.) For example, as shown in the annotated figure 4C above, conductive plugs 323 connect the **same ends** of traces 321 ("third conductor layer" and "fourth conductor layer"), rather than **different ends** of the traces. (*Id.*) As such, a POSITA would have also understood that traces 321 ("third conductor layer" and "fourth conductor layer") are connected in parallel. (*Id.*)

Second, Lee discloses "wherein the first and second conductor layers are connected electrically in parallel and are further connected electrically in series with the third and fourth conductor layer." Lee discloses that the first and second conductor layers are connected electrically in parallel. (*Supra* Section IX.A.1(c).) Third, Lee discloses the first and second conductor layers "are further connected electrically in series with the third and fourth conductor layers are connected electrically in parallel. (*Id.*, ¶82.) For example, Lee discloses with reference to figure 4C that traces 311 ("first and

second conductor layers") and traces 321 ("third and fourth conductor layers") are electrically connected in series by conductive plug 325. (Ex. 1005, ¶[0033] ("The conductive plug 325 is disposed between the second end 56 of the looped conductive traces 311 and the first end 62 of the looped conductive layers 321 adjacent thereto, to serve as an electrical connection between the multi-level interconnect formed by the looped conductive traces 311 and the multi-level interconnect formed by the looped conductive traces 321."); *see also id.* at claim 20 ("the third looped conductive traces, the first looped conductive traces and the second conductive trace are connected **in series**" where the first looped traces correspond to traces 311 and the second looped traces correspond to traces 321) (emphasis added).)

Indeed, a POSITA would have also understood that looped conductive traces 311 ("first and second conductive layers") and 321 (the third and fourth conductor layers) are electrically connected in series based on figure 4C. (Ex. 1002, ¶83.) For example, as shown in the annotated figure 4C above, conductive plug 325 connects different ends of traces 311 and 321 ("second conductor layer" and "third conductor layer"), rather than the same ends of the traces. (*Id.*; *see also* Ex. 1005, ¶[0033].) As such, a POSITA would have also understood that traces 311 and 321 ("the first and second conductive layers" and "the third and fourth conductor layers") are connected in series. (*Id.*, ¶83.)

14. Claim 20

a) The method of claim 1 further connecting the inductor electrically within an electrical circuit operating at about 100 kHz or greater.

Lee discloses this limitation. (Ex. 1002, \P 84.) Lee discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (*Id.*, \P [0005].) The RF band includes frequencies above 100 kHz. (Ex. 1002, \P 84; *supra* Section IX.A.1(d).) Therefore, Lee's figures 4A-4C disclose "connecting the inductor electrically within an electrical circuit operating at about 100 kHz or greater." (Ex. 1002, \P 84.)

15. Claim 21

a) The method of claim 20 further selecting the electrical circuit from the group consisting of a mixer circuit, an impedance matching circuit, an upconverting mixer circuit, a downconverting mixer circuit, a modulator, a demodulator, a synthesizing circuit, a PLL synthesizing circuit, an amplifying circuit, an electrical driver circuit, an electrical detecting circuit, an RF log detector, an RF RMS detector, an electrical transceiver, a power controller, and combinations thereof.

Lee discloses this limitation. (Ex. 1002, ¶85.) As discussed above with respect to claim 20, Lee discloses that the on-chip inductor can be employed in RF circuits but does not limit the RF circuits to any particular circuit. (*Supra* Section IX.A.14.) Therefore, a POSITA would understand that Lee discloses connecting an inductor within a mixer circuit, which is an electrical circuit that is employed in

RF circuits. (See, e.g., Ex. 1020 at FIG. 1 (showing use of inductor in a Gilbertcell Mixer); see also Ex. 1002, ¶85.)

16. Claim 23

a) The method of claim 1 further connecting a control circuit electrically with the inductor.

Lee discloses this limitation. (Ex. 1002, ¶86.) As discussed above with respect to claim 20, Lee discloses that the on-chip inductor can be employed in RF circuits (*supra* Section IX.A.14), which a POSITA would have known includes a control circuit. (Ex. 1002, ¶86.) Therefore, Lee discloses connecting a control circuit electrically (e.g., a control circuit in an RF integrated circuit) with the inductor.

17. Claim 24

a) The method of claim 1 further providing at least the first and second conductor layers with at least a partial revolution.

Lee discloses this limitation. (Ex. 1002, ¶¶87-88.) For example, as shown in the annotated figure 4C below, Lee discloses that each of looped conductive traces 311 ("the first and second conductor layers") is separated by a gap g3. (Ex. 1005, ¶¶[0025], [0031], FIGs. 4A, 4C.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶87.)

Because Lee discloses that each of conducive traces 311 ("first and second conductor layers") is **looped** and separated by gap g3, Lee discloses that "at least the first and second conductor layers has at least a partial revolution." (Ex. 1002, ¶88.)

18. Claim 25

a) The method of claim 1 further providing the first conductor layer or the second conductor layer having a material selected from the group consisting of copper, titanium, platinum, platinum and iridium alloys, tantalum, niobium, zirconium, hafnium, nitinol, cobalt-chromium-nickel alloys, stainless steel, gold, a gold alloy, palladium, carbon, silver, a noble metal, a conductive polymer, a conductive adhesive, a conductive composite, a liquid metal, a foamed metal, a conductive tape, a conductive ribbon, a conductive foil, a conductive leaf, a wire, a deposited metal, a biocompatible material, and combinations thereof.

Lee discloses this limitation. (Ex. 1002, \P 89.) For example, Lee discloses that traces 311 ("first conductor layer" and "second conductor layer") "may be copper, aluminum or a combination thereof." (Ex. 1005, \P [0026].)

19. Claim **26**

a) The method of claim 1 further forming at least one insulator layer from an electrically insulative material.

Lee discloses this limitation. (Ex. 1002, ¶90.) For example, Lee discloses that dielectric layer 308 ("insulator layer") may be an "insulating layer" such as "silicon oxide, silicon nitride or low k dielectric material." (Ex. 1005, ¶[0024].) A POSITA would have understood that at least silicon oxide and silicon nitride are "electrically insulative material[s]" because dielectric layer 308 is an insulating layer. (Ex. 1002, ¶90; *see also* Ex. 1001, claim 27 (silicon dioxide is an electrically insulative material).)

20. Claim 27

a) The method of claim 1 further providing the insulator layer having an electrically insulative material selected from the group consisting of air, polystyrene, silicon dioxide, a biocompatible ceramic, a conductive dielectric material, a non-conductive dielectric material, a piezoelectric material, a pyroelectric material, a ferrite material, and combinations thereof.

Lee discloses this limitation. (Ex. 1002, ¶91.) For example, Lee discloses that dielectric layer 308 ("insulator layer") may be an "insulating layer" such as "silicon oxide, silicon nitride or low k dielectric material." (Ex. 1005, ¶[0024].)

21. Claim 28

Preamble: A method of manufacturing an inductor structure, the method comprising the following steps:

Lee discloses this limitation, for at least the same reasons as presented above

for the preamble of claim 1. (Supra Section IX.A.1(preamble); Ex. 1002, ¶92; see

also analysis below for the remaining elements of this claim.)

a) providing a first inductor subassembly comprising the following steps:

Lee discloses this limitation. (Ex. 1002, ¶93.) For example, as shown in annotated figure 4C below, Lee's first multi-level interconnect structure discloses

the claimed "first inductor subassembly." (Ex. 1005, $\P[0025]$; see also analysis below for claim limitations 28(a)(1)-(2).)

(1) i) providing a first conductive conductor layer and a second conductive conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive; ii) positioning a first insulator layer in a space between the first conductor layer and the second conductor layers;

Lee further discloses this limitation for at least the same reasons as presented

above for limitations 1(a)-(b). (Supra Sections IX.A.1(a)-(b); Ex. 1002, ¶94.)



FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶94.)

(2) iii) connecting the first conductor layer and the second conductor layer electrically in parallel with a first connector, the first connector having a first connector electrical impedance;

Lee discloses this limitation for at least the same reasons as presented above for limitations 1(c) and claim 17. (*Supra* Sections IX.A.1(c) and IX.A.11; Ex. 1002, ¶95.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶95.)

b) providing a second inductor subassembly comprising the following steps:

Lee discloses this limitation. (Ex. 1002, ¶96.) For example, as shown in the annotated figure 4C below, Lee's second multi-level interconnect structure discloses the claimed "second inductor subassembly." (Ex. 1005, ¶[0031]; see

infra Sections IX.A.21(b)(1)-(3) for the remaining elements of the claimed "second





(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶96.)

(1) i) providing a third conductor layer and a fourth conductor layer spaced apart from the third conductor layer, the third conductor layer and the fourth conductor layer being electrically conductive;

Lee discloses this limitation. (Ex. 1002, ¶¶97-99.) For example, as illustrated in annotated figure 4C below, Lee's inductor, in its second multi-level interconnect structure, includes another looped conductive trace 321 ("fourth conductor layer") that is embedded in dielectric layer 304, in addition to looped conductive trace 321 ("third conductor layer") that is embedded in dielectric layer

306. (Ex. 1005, ¶[0032]; see also id. at ¶¶[0031], [0033]-[0034]; supra Section

IX.A.13 (claim 19); Ex. 1002, ¶97.)



FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶97.)

Furthermore, Lee discloses that these conductive traces 321 ("third conductor layer" and "fourth conductor layer") are "separated from each other." (Ex. 1005, ¶[0032]; *see also id.* at Abstract (disclosing "a plurality of looped conductive traces overlapping and separated from each other"), ¶[0010], claim 2.) Thus, Lee discloses "a fourth conductor layer spaced apart from the third conductor layer." (Ex. 1002, ¶98.)

Lee also discloses that these conductive traces 321 ("third conductor layer" and "second conductor layer") are electrically conductive at least because Lee describes these traces 321 as **conductive** and that a **current** may pass through these conductive traces to induce inductance. (*See*, *e.g.*, Ex. 1005, ¶[0034].) Accordingly, Lee discloses "a fourth conductor layer spaced apart from the third conductor layer, the third conductor layer and the fourth conductor layer being electrically conductive." (Ex. 1002, ¶99.)

(2) ii) positioning a second insulator layer in a space between the third conductor layer and the fourth conductor layers;

Lee discloses this limitation. (Ex. 1002, ¶100.) For example, as shown in the annotated figure 4C below, Lee discloses dielectric layer 304 ("second insulator layer") that is positioned in the space between two conductive traces 321 ("the third conductor layer and the fourth conductor layers"). (Ex. 1005, ¶[0032] (disclosing that "the looped conductive layers 321 may be correspondingly disposed in the dielectric layers 302, 304 and 306" and that "[t]he looped conductive traces 321...are separated from each other.").)

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(Ex. 1005, FIG. 4C (annotated to show that dielectric layer 304 is positioned in the space between two conductive traces 321); Ex. 1002, ¶100.) Furthermore, Lee discloses that dielectric layer 304 is an "insulator layer," as claimed. (Ex. 1005, $\P[0031]$ ("the **insulating** layer may be dielectric layers 302, 304, 306, 308, 310, 312 and 314 successively disposed on the substrate 300.") (emphasis added); Ex. 1002, ¶100.)

(3) iii) connecting the third conductor layer and the fourth conductor layer electrically in parallel with a second connector, the second connector having a second connector electrical impedance; and

Lee discloses this limitation. (Ex. 1002, $\P\P101-103$.) For clarity, this limitation is discussed in two parts. (*Id.*, $\P101$.)

First, Lee discloses a second connector that electrically connects the third conductor layer and the fourth conductor layer in parallel. (Id., ¶102.) For example, as shown in the annotated figure 4C below, Lee discloses that a conductive plug 323 ("second connector") electrically connects two conductive traces 321 ("the third conductor layer and the fourth conductor layer") in parallel. (Ex. 1005, ¶[0035] ("since the lower conductive trace includes multilayer winding structure in which each conductive trace is connected in parallel, the series resistance can be reduced to maintain the Q value of the inductor") (emphasis added); ¶[0034] (disclosing that "the multi-level interconnect structure formed by the looped conductive traces 321 serves as another lower conductive trace of the inductor") (emphasis added); see also id. at ¶[0033] ("The conductive plugs 323 are disposed between the looped conductive traces 321 to serve as an electrical connection therebetween...thereby reducing the resistance of the multi-level interconnect structure to further reduce the series resistance."); claim 20 ("the third looped conductive traces are coupled in parallel") (emphasis added); see also Ex. 1002, ¶102.)

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(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶102.)

Second, Lee discloses that "conductive plugs 323 may be copper, aluminum or a combination thereof." (Ex. 1005, ¶[0033].) Both copper and aluminum have an electrical impedance because all materials have an electrical impedance. (Ex. 1002, ¶103; Ex. 1001, 14:46-50 (explaining that resistance of a copper wire "at a frequency of 1 MHz is almost four times the dc value").) A POSITA would have therefore understood that Lee discloses "the second connector having a second connector electrical impedance." (Ex. 1002, ¶103.)

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c) connecting the first inductor subassembly electrically in series to the second inductor subassembly;

Lee discloses "connecting the first inductor subassembly electrically in series to the second inductor subassembly." (Ex. 1002, ¶104.) For example, as shown in the annotated figure 4C below, Lee discloses that "the first inductor subassembly" (including traces 311 that are separated by dielectric layer 308, and conductive plugs 315) and "the second inductor subassembly" (including traces 321 that are separated by dielectric layer 304, and conductive plugs 323) are electrically connected in series by conductive plug 325. (Ex. 1005, FIG. 4C, ¶[0033]; *see also id.* at claim 20 ("the third looped conductive traces, the first looped conductive traces and the second conductive trace are connected **in series**" where the third looped traces correspond to traces 321s in figure 4C, the first looped traces correspond to traces 311s in figure 4C) (emphasis added); Ex. 1002, ¶104.)



FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶104.)

Indeed, a POSITA would have also understood based on figure 4C that the "first inductor subassembly" and "second inductor subassembly" are electrically connected in series. (Ex. 1002, ¶105.) For example, as shown in the annotated figure 4C above, unlike plugs 315, which connects both ends of traces 311, conductive plug 325 connects only one end of adjacent traces 311 and 321 (respectively being a part of "first inductor subassembly" and a part of "second inductor subassembly"). (*Id.*; *see also* Ex. 1005, ¶[0033].) As such, a POSITA

would have also understood that "first inductor subassembly" and "second inductor

subassembly" are connected in series. (Id., ¶105.)

d) wherein when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current.

Lee discloses this limitation for at least the same reasons presented above for

limitation element 1(d). (See supra Section IX.A.1(d); Ex. 1002, ¶106.)

- 22. Claim 29
 - a) The method of claim 28 further orienting the first conductor subassembly and the second inductor subassembly such that the first and second inductor subassemblies are positioned about parallel, about perpendicular, or at an angular relationship therebetween.⁴

Lee discloses this limitation. (Ex. 1002 ¶107.) For example, Lee discloses that the first and second inductor subassemblies (*supra* Section IX.21 (analysis for claim 28)) are separated from each other because "a conductive plug 325" connects the two assemblies. (Ex. 1005, ¶[0033]; *see also id.* at FIG. 4C.) Thus, a POSITA would have understood that the two subassemblies are positioned "in about a

⁴ The term "first conductor subassembly" has no antecedent basis. Petitioner assumes for purposes of this proceeding that "first conductor subassembly" refers to "first inductor subassembly."

parallel orientation, about perpendicular, or at an angular relationship with respect to each other" as the subassemblies are in different planes. (Ex. 1002, ¶107.)

B. Ground 2: Claim 12 is obvious over Lee in view of Ahn

1. Claim 12

a) The method of claim 1 further providing a thickness of the insulating layer less than about 5 cm.

Lee in combination with Ahn discloses or suggests this limitation. (Ex. 1002, ¶109-114.) Lee discloses a "multilayer winding inductor formed in a semiconductor chip" where conductive traces 311 ("first conductor layer" and "second conductor layer") are separated by insulating dielectric layers, including layer 308 ("insulating layer"). (Ex. 1005, ¶[0031].) Lee further discloses that its insulating layers may be silicon oxide or dielectric material. (Id., ¶[0024].) A POSITA would have understood that the scale of semiconductor components is in the micron range (1 micron is equal to 1/10000 cm) and that the thickness of layers, e.g. conductor layers or insulator layers, in semiconductor devices would be orders of magnitude smaller than 5 cm. (Ex. 1002, ¶109.) Indeed, Lee discloses conductor layer (311) is less than 1 micron. (Ex. 1005, ¶[0027].) As such, while Lee does not expressly disclose the thickness of its insulating layer, a POSITA would have understood the thickness of the insulating layer in Lee's inductor would have been much less than about 5cm. (Ex. 1002, ¶109.)

Like Lee, Ahn discloses "an integrated circuit structure" formed in a semiconductor substrate comprising spiral-shape inductors separated by insulating or dielectric layers. (Ex. 1031 at 1:15-17, 42-45, FIG. 1; *see also id.* at 5:33-6:2.) Just like Lee, Ahn discloses that insulating layers can be a dielectric or oxide. (*Id.*, 5:35-38.) Indeed, Ahn states that an oxide is "typically used for such purposes." (*Id.*; Ex. 1002, ¶110.)

In particular, Ahn discloses an embodiment in figure 4, reproduced below, with insulating layers 53 and 530 ("insulating layer") separating inductors 302 ("first conductor layer") and 312 ("second conductor layer"). (Ex. 1031 at 5:45-6:2; *see also id.* at 5:26-32 (describing the inductor layers as conductors).)

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(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶111.)

Ahn explains that insulating layer 53 (blue) "is preferably formed having a thickness of about 100 μ m," and insulating layer 530 (green) is preferably formed with a thickness "between about 30 μ m and about 50 μ m." (*Id.*, 5:52-59.) The insulator layers are sandwiched between conductive inductor layers 30 and 31 (yellow). (*Id.*, 5:52-66.) Thus, insulators 53 and 530 together form an insulator layer about 130 μ m to 150 μ m separating the conductors. (Ex. 1002, ¶112.)

Given the similarities between Lee and Ahn, a POSITA would have combined the teachings of Lee and Ahn because Lee discloses a multilayer winding inductor formed in a semiconductor substrate using oxide or dielectric insulator layers and Ahn discloses stacked inductors formed in a semiconductor substrate using oxide or a dielectric insulator layers. (*Id.*, ¶113.) A POSITA would have recognized that it would have been advantageous to combine the teachings of these references because Ahn discloses the thickness of insulator layers in semiconductor inductors, an aspect on which Lee is silent. (*Id.*) KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 415-18 (2007).

Moreover, the thickness of an insulating layer is a "result-effective variable" because it affects the overall thickness of the integrated circuit and also determines the amount of the insulation between conducting layers on both sides of the insulating layer. (Ex. 1002, ¶114.) Therefore, if "less than 5 cm" is an optimum number for the insulating layer thickness per claim 12, claim 12 is obvious because "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." In re Boesch, 617 F.2d 272, 276 (C.C.P.A. 1980); In re Aller, 220 F.2d 454, 456 (C.C.P.A. 1955); see also In re Applied Materials, Inc., 692 F.3d 1289, 1295 (Fed. Cir. 2012). This is especially true given that the '046 patent provides no evidence that "less than 5 cm" thickness produces a new or unexpected result, and thus the claimed range cannot form the basis of patentability. (Ex. 1002, ¶114.) In re Boesch, 617 F.2d at 276; In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

C. Ground 3: Claim 13 is Obvious over Lee in view of Kyriazidou

1. Claim 13

a) The method of claim 1 further providing an inductor quality factor greater than about 5.

Lee in combination with Kyriazidou discloses or suggests this limitation. (Ex. 1002, ¶¶115-118.) Lee discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (Ex. 1005, ¶[0005].) While Lee does not expressly disclose that the inductor of figures 4A-4C has an "an inductor quality factor greater than about 5," Lee notes that a high value of the quality factor is desirable. (*Id.*, ¶¶[0008], [0009].) A POSITA would have understood that a quality factor of 5 is a relatively modest value, and would understand that by "maintain[ing] the Q value of the inductor," Lee's inductor would exceed a quality factor of 5. (Ex. 1002, ¶116; Ex. 1005, ¶[0035].)

Kyriazidou similarly discloses that "on-chip inductors are significant components of RF integrated circuits and are used in oscillators, impedance matching networks, emitter degeneration circuits, filters, and/or baluns." (Ex. 1019 at 1:26-29.) It discloses that "inductors having a high Q-factor dissipate less power and thus improve the achievable gain. Further, high Q inductors allow an oscillating circuit to perform with minimal power injection from the driving transistor and hence minimize noise." (*Id.*, 1:39-44.) It further notes that "CMOS

technology is widely used for cost effective fabrication of . . . RF integrated circuits" and that "on-chip inductors using CMOS technology are known to have a **modest quality factor** in the range of **5 to 10**." (*Id.*, 1:58-64 (emphasis added).) Furthermore, Kyriazidou discloses that "in one embodiment of an on-chip inductor using CMOS technology, the quality factor may be increased to as much as 150." (*Id.*, 4:29-31.) Therefore, Kyriazidou expressly discloses an "inductor quality factor greater than about 5," and supports the fact that a POSITA would understand Lee's teaching that the disclosed invention maintains the quality factor value as suggesting using a quality factor greater than 5. (Ex. 1002, ¶117.)

In view of Kyriazidou, a POSITA would have found it obvious to fabricate Lee's inductor such that it has a quality factor of at least 5. (*Id.*, ¶118.) Indeed, a POSITA would have been motivated to do so because Lee discloses the use of onchip inductors in RF integrated circuits and Kyriazidou discloses that on-chip inductors in such circuits typically have "a modest quality factor in the range of **5** to 10" and that it is desirable to increase the quality factor even more given the benefits of a higher inductor quality factor. (*Id.*; Ex. 1019 at 1:60-64.) *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"). A POSITA would not only have been motivated to fabricate Lee's inductor such that it has a quality factor of at least 5 but also known how to do so. (Ex. 1002, ¶118.)

D. Ground 4: Claim 23 is Obvious over Lee in View of Partovi

1. Claim 23

a) The method of claim 1 further connecting a control circuit electrically with the inductor.

Lee in combination with Partovi discloses or suggests this feature. (Ex. 1002, ¶¶119-122.) Lee discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (Ex. 1005, ¶[0005].) Lee further discloses that the inductor of figures 4A-4C is connected to "external or internal circuits" that provide a current passing through the inductor. (*Id.*, ¶¶[0001], [0034].) But Lee does not disclose what those "external or internal circuits" are or how to utilize the inductor in RF circuits. (Ex. 1002, ¶120.) However, it would have been obvious to use Lee's inductor in an RF circuit, an example of which is disclosed by Partovi and where a control circuit is electrically connectable with the inductor. (*Id.*)

Partovi discloses "a system and method for inductive charging of portable devices." (Ex. 1009, ¶[0003].) The general principles of Partovi's inductive charging system are disclosed with reference to figure 2, which discloses power being transferred from a primary coil in a charger to a secondary coil in a receiver (e.g., in a mobile device). (*Id.*, ¶¶[0116]-[0117], FIG. 2; Ex. 1002, ¶121.) Figure

28 of Partovi discloses one implementation of the concepts disclosed in figure 2. (Ex. 1002, ¶121; Ex. 1009, ¶[0260]-[0261].) In particular, figure 28 discloses "a digital control scheme," where "[t]he primary (charger or power supply) 620 is controlled by a Micro Control Unit (MCU1)." (Ex. 1009, ¶[0261].) Partovi discloses that MCU1 receives signals from a Current Sensor that is connected in series with the primary coil L1 ("inductor") and then controls the power output by the primary coil L1 by controlling the switching frequency of FET Q1. (Id., ¶[0261]-[0265].) In particular, Partovi's figure 28 circuit operates at a frequency of "1-2 MHz" (id. at ¶[0265]), which a POSITA would have understood is in the RF band. (Ex. 1002, ¶121; Ex. 1010 at 860 ("The present practicable limits of radio frequency are roughly 10 kHz (kilohertz) to 100 000 MHz (megahertz)"; see also Ex. 1009, FIG. 10 (RFID reader in the charger circuit).) Accordingly, Partovi discloses or suggests "a control circuit is electrically connectable to the inductor." (Ex. 1002, ¶121.)


(Ex. 1009, FIG. 28 (excerpted and annotated); Ex. 1002, ¶121.)

In view of the above, a POSITA would have combined the teachings of Lee and Partovi because Lee discloses an on-chip inductor used in RF circuits and Partovi discloses the use of RF circuits for inductive power transfer. (Ex. 1002, ¶122.) A POSITA would have recognized that it would have been advantageous to combine the teachings of these references because Partovi discloses specific examples of the use of inductors in RF circuit, an aspect on which Lee is silent. (*Id.*) Furthermore, a POSITA would have understood that using an **on-chip** inductor in Lee in a circuit like in Partovi would have allowed reducing the size of Partovi's circuit because inductors created on-chip (as opposed to on a PCB like in Partovi) occupy less space. (Id.) Indeed, on-chip inductors have other advantages, such as "there are no assembly costs, as the inductors are formed directly on the circuit substrate, and tight tolerance can be achieved." (Ex. 1025 at ¶[0002].) As such, a POSITA would have been motivated to combine the teachings of Lee and Partovi such that Lee's inductor is used in a circuit like in Partovi. (Ex. 1002, ¶122.) See Unwired Planet, LLC v. Google Inc., 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"). A POSITA would have reasonably expected success in combining the teachings and would have known how to make the necessary changes to the teachings drawn from Lee and Partovi in order to make a functioning circuit. (Ex. 1002, ¶122.)

E. Ground 5: Claims 5-7 are obvious over Lee in view of Hu

1. Claim 5

Lee in view of Hu discloses or suggests this limitation. (Ex. 1002, ¶¶123-127.) To the extent that Lee does not inherently or explicitly discloses "providing a thickness of the first conductor layer about equal to a thickness of a skin depth of the first conductor layer at a given frequency," but Hu discloses such a feature and it would have been obvious to implement conductive trace 311 ("first conductor layer") in Lee such that its thickness is about one to two times the skin depth at a given operating frequency. (*Id.*, \P 124.)

Similar to Lee, Hu discloses an inductor operating in the RF range. (Ex. 1033 at 564 (disclosing an inductor designed for operating at a RF frequency, e.g., at 1 MHz); Ex. 1002, ¶125.) Hu further discloses that "the choice of conductor thickness" in the disclosed inductor is "already well understood." (Ex. 1033 at 559.) In particular, Hu discloses

since current will mainly flow in the top skin depth, a thickness of **one to two skin depths** is sufficient to achieve nearminimum ac resistance.

(Id.)

As such, when implementing each of the conductive traces (including "first conductor layer"), e.g., 311 and 321, in Lee's inductor, a POSITA would have found it obvious to ensure that the thickness of each of the conductive traces is at least **one to two skin depths** at the inductor's operating frequency in order to minimize conductor loss in these layers. (Ex. 1002, ¶126.) *See Unwired Planet*, 841 F.3d at 1003 (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]").

A POSITA would have understood that implementing the claimed feature would have involved no more than applying a known technique to a known device to yield a predictable result (e.g., designing and implementing a conductor based on the skin depth at a certain operating frequency or altering the operating frequency to ensure that the skin depth is one or two times the conductor thickness). (Ex. 1002, ¶127.) *See KSR*, 550 U.S. at 416.

2. Claims 6 and 7

Lee in view of Hu discloses or suggests the features of these claims. (Ex. 1002, ¶128.) As discussed above for claim 5, based on the teachings of Lee and Hu, a POSITA would have found it obvious to ensure that the thickness of each of the conductive traces (including "first conductor layer" and "second conductor layer") is at least **one to two skin depths** at the inductor's operating frequency in order to minimize conductor loss in these layers. (*See supra* Section IX.E.1.)

Therefore, the combination of Lee and Hu, which discloses using a conductor having a thickness of **one to two skin depths**, discloses claims 6 and 7, requiring the thicknesses of the first and second conductor layers to range from about 1.25 times to about 4 times a thickness of a skin depth of the conductor layers at a given frequency. (Ex. 1002, ¶129.)

F. Ground 6: Claims 1-3, 6-8, 10, 15-21, and 23-29 are Obvious over Lee in View of Alldred

1. Claim 1

As discussed above with respect to claim element 1(d), Lee discloses that the current through its inductor changes (e.g., because the current is an alternating current) and that such an understanding is consistent with Lee's disclosure of the use of on-chip inductors in RF circuits. (*Supra* Section IX.A.1(d).) As discussed below, Lee in combination with Alldred discloses the use of an on-chip inductor in an RF circuit where an alternating current propagates through the inductor. (Ex. 1002, ¶130.)

Lee discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (Ex. 1005, ¶[0005].) Lee further discloses that the **on-chip** inductor of figures 4A-4C is connected to "external or internal circuits" that provide a current to the inductor. (*Id.*, ¶¶[0001], [0034].) But Lee does not disclose what those "external or internal circuits" are. (Ex. 1002, ¶131.)

Alldred, however, discloses an example of an RF integrated circuit that uses on-chip inductors. Specifically, Alldred discloses "60-GHz radio receiver with onchip . . . inductors" (Ex. 1020 at Title.) Figure 1 (reproduced below) is a block diagram of the RF integrated circuit receiving a 60 GHz RF signal and that

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includes, among other things, a low noise amplifier (LNA) and a mixer. (*Id.*, 51 (FIG. 1); Ex. 1002, ¶132.)



Figure 1. Receiver block diagram.

(Ex. 1020 at 51 (FIG. 1).)

The LNA circuit is described in figure 2 and the mixer is described in figure 3. (*Id.*, 51, 52, FIGS. 2-3.) In particular, the LNA receives a 60 GHz and therefore, includes an inductor (see below) whose operating frequency is 60 GHz. (*See id.* at FIG. 2 (reproduced below); *id.* at 51 ("The inductors between the transistors in each stage absorb parasitic capacitance for increased gain over a broad bandwidth which extends beyond 60 GHz."); Ex. 1002, ¶133.)



Figure 2. Two-stage cascode LNA schematic.

(Ex. 1020 at FIG. 2 (annotated); Ex. 1002, ¶133.)

A POSITA would have combined the teachings of Lee and Alldred because Lee discloses that on-chip inductors are used in RF circuits and Alldred discloses one example of an RF circuit that uses on-chip inductors. (Ex. 1002, ¶134.) A POSITA would have recognized that it would have been advantageous to combine the teachings of these references because Lee discloses how to make on-chip inductors, an aspect on which Alldred is silent. (*Id.*) That is, the teachings of the two references complement each other. (*Id.*) Indeed, the combination of Lee with Alldred as discussed above in this section would have been a mere "combination of familiar elements according to known methods [to] yield predictable results," as such a combination would have combined teachings regarding Lee's on-chip inductors with Alldred's teachings regarding an RF circuit that uses such inductors. *KSR*, 550 U.S. at 416. Moreover, because these two references complement each other, a POSITA would have recognized that these references would have been beneficially combined in the above manner. (Ex. 1002, ¶134.) *KSR*, 550 U.S. at 418 (explaining that for an obviousness analysis "a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ), 421 ("A person of ordinary skill is also a person of ordinary creativity").

As discussed above, in the Lee-Alldred combination, the inductor would receive a 60 GHz signal and therefore, an AC current would propagate through the inductor. (Ex. 1002, ¶135.) Such an AC current (which changes in magnitude) would result in the change of magnetic flux generated within the inductor, and therefore, the Lee-Alldred combination discloses or suggests claim element 1(d). (*Id.*; *supra* Section IX.A.1(d).)

Lee in combination with Alldred discloses or suggests the remaining limitations of claim 1 for the reasons discussed above for claim 1 with the only modification to the analysis for claim 1 being that discussed above. (*Supra* Section IX.A.1; Ex. 1002, ¶136.)

2. Claim 2

Lee in combination with Alldred discloses or suggests the features of claim 2 for the reasons discussed above in Section IX.A.2. But claim 2 is disclosed or suggested for the additional reason that in the Lee-Alldred combination, an RF current (i.e., an alternating current) would propagate through Lee's inductor (*supra* Section IX.F.1) and because an AC current changes in magnitude over time, an EMF will necessarily be generated in the inductor. (Ex. 1002, ¶137; Ex. 1001, 1:55-65, 14:17-27.)

3. Claim 3

Lee in combination with Alldred discloses or suggests the features of claim 3 for the reasons discussed above in Section IX.A.3. But claim 3 is disclosed or suggested for the additional reason that in the Lee-Alldred combination, an RF current (i.e., an alternating current) would propagate through Lee's inductor (*supra* Section IX.F.1) and because an AC current changes in magnitude over time, the magnetic flux within the inductor will change proportionally to the change in current through the inductor. (Ex. 1002, ¶138; Ex. 1001, 1:55-65, 14:17-27.)

4. Claims 6 and 7

The Lee-Alldred combination discloses or suggests the features of this claim because at a 60 GHz frequency, the skin depth for Lee's inductor (formed of copper with a resistivity of $1.678 \ 10^{-8}$ ohm-metres and relative permeability of 1)

will be 0.2662 μ m, and therefore, the thickness (i.e., 0.53 μ m) of the looped conductive layers 311 (including the "first conductor layer" and the "second conductor layer") is almost two times the skin depth. (Ex. 1002, ¶139 (citing https://chemandy.com/calculators/skin-effect-calculator.htm); *supra* Section IX.F.1.)

5. Claim 20

Lee in combination with Alldred discloses or suggests the features of claim 20 because the inductor is connected within an LNA (low noise amplifier) ("electrical circuit") operating at 60 GHz. (Ex. 1002, ¶140; *supra* Section IX.F.1; *see* Ex. 1020 at FIG. 2.)

6. Claim 21

The Lee-Alldred combination discloses or suggests this limitation. (Ex. 1002, ¶141.) For example, as discussed above with respect to claim 20, in the Lee-Alldred combination, the "electrical circuit" is an LNA ("amplifying circuit"). (*Supra* Section IX.F.5.)

7. Claim 28

Lee in combination with Alldred discloses or suggests the features of claim 28 for reasons similar to those discussed in Section IX.A.21 (analysis for claim 28 in Section IX.A.) (Ex. 1002, ¶142.) The combination further discloses claim element 28(d) because it discloses that an AC current (which changes in

magnitude) propagates through Lee's inductor by virtue of Lee's inductor being implemented in an RF circuit like in Alldred. (*Supra* Section IX.F.1.) The propagation of such an AC current would result in the change of magnetic flux generated within the inductor. (*Id.*)

8. Claims 8, 10, 15-19, 23-27, and 29

Lee in combination with Alldred discloses or suggests the limitations of these claims for reasons similar to those discussed in Section IX.A for these claims. (Ex. 1002, ¶143.) The same analysis presented above for these claims in Ground 1 is also applicable for the Lee-Alldred combination discussed above in Sections IX.F.1 (claim 1) and IX.F.7 (claim 28). (Ex. 1002, ¶143.) The combination of Lee with Alldred does not affect the analysis for these claims in Section IX.A. (*Id.*)

G. Ground 7: Claim 12 is Obvious over Lee in View of Alldred and Ahn

As discussed above in Section IX.F.1, Lee in view of Alldred discloses or suggests all of the limitations of claim 1. But to the extent that the Lee-Alldred combination does not explicitly disclose claim 12, a POSITA would have combined the teachings of Lee and Alldred with Ahn for the same reasons that a POSITA would have combined the teachings of Lee with Ahn that renders claim 12 obvious (*supra* Section IX.B). Therefore, the Lee-Alldred-Ahn combination renders claim 12 obvious for reasons similar to those discussed above in Section IX.B. (Ex. 1002, ¶144.)

H. Ground 8: Claim 13 is Obvious over Lee in View of Alldred and Kyriazidou

As discussed above in Section IX.F.1, Lee in view of Alldred discloses or suggests all of the limitations of claim 1. But to the extent that the Lee-Alldred combination does not explicitly disclose claim 13, a POSITA would have combined the teachings of Lee and Alldred with Kyriazidou for the same reasons that a POSITA would have combined the teachings of Lee with Kyriazidou that renders claim 13 obvious (*supra* Section IX.C). Therefore, the Lee-Alldred-Kyriazidou combination renders claim 13 obvious for reasons similar to those discussed above in Section IX.C. (Ex. 1002, ¶145.)

I. Ground 9: Claim 5 is Obvious over Lee in View of Alldred and Hu

As discussed above in Section IX.F.1, Lee in view of Alldred discloses or suggests all of the limitations of claim 1. But to the extent that the Lee-Alldred combination does not explicitly disclose claim 5, a POSITA would have combined the teachings of Lee and Alldred with Hu for the same reasons that a POSITA would have combined the teachings of Lee with Hu that renders claim 5 obvious (*supra* Section IX.E.1). Therefore, the Lee-Alldred-Hu combination renders claim

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5 obvious for reasons similar to those discussed above in Section IX.E.1. (Ex. 1002, ¶146.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-3, 5-8, 10, 12, 13, 15-21, and 23-29 of the '046 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/ Naveen Modi (Reg. No. 46,224) Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,300,046 contains, as measured by the word-processing system used to prepare this paper, 13802 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: March 22, 2019

By: <u>/Naveen Modi/</u> Naveen Modi (Reg. No. 46,224) Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 22, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,300,046 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

> McDermott, Will & Emery LLP The McDermott Building 500 North Capitol Street, N.W. Washington, D.C. 20001

A courtesy copy was also sent via electronic mail to Patent Owner's

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