# UNITED STATES PATENT AND TRADEMARK OFFICE 

## BEFORE THE PATENT TRIAL AND APPEAL BOARD

> SAMSUNG ELECTRONICS CO., LTD.

Petitioner
v.

PROMOS TECHNOLOGIES, INC.
Patent Owner
U.S. Patent No. 6,597,201

## TABLE OF CONTENTS

I. INTRODUCTION ..... 1
II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8 ..... 1
III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a) ..... 2
IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a) ..... 2
V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b) ..... 2
A. Claims for Which Review Is Requested ..... 2
B. Statutory Grounds of Challenge ..... 2
VI. LEVEL OF ORDINARY SKILL IN THE ART ..... 6
VII. OVERVIEW OF THE '201 PATENT AND PRIOR ART ..... 6
A. The ' 201 Patent ..... 6
VIII. CLAIM CONSTRUCTION ..... 9
IX. DETAILED EXPLANATION OF GROUNDS ..... 10
A. Ground 1: Claims 1-6 Are Obvious over Fujioka and Yuh ..... 10

1. Claim 1 ..... 10
2. Claim 2 ..... 48
3. Claim 3 ..... 51
4. Claim 4 ..... 53
5. Claim 5 ..... 53
6. Claim 6 ..... 54
B. Ground 2: Claims 1-6 Are Obvious over Fujioka, Lee, and Yuh ..... 65
7. Claim 1 ..... 65
8. Claim 2 ..... 77
9. Claim 3 ..... 78
10. Claim 4 ..... 78
11. Claim 5 ..... 78
12. Claim 6 ..... 78
C. Ground 3: Claims 1-5 Are Obvious over AAPA, Yuh, and Fujioka ..... 79
13. Claim 1 ..... 79
14. Claim 2 ..... 95
15. Claim 3 ..... 97
16. Claim 4 ..... 98
17. Claim 5 ..... 98
X. CONCLUSION ..... 99

## LIST OF EXHIBITS

| Ex. 1001 | U.S. Patent No. 6,597,201 |
| :--- | :--- |
| Ex. 1002 | Declaration of R. Jacob Baker, Ph.D., P.E. |
| Ex. 1003 | Curriculum Vitae of R. Jacob Baker, Ph.D., P.E. |
| Ex. 1004 | Prosecution History of U.S. Patent No. 6,597,201 |
| Ex. 1005 | U.S. Patent No. 5,812,485 ("Yuh") |
| Ex. 1006 | U.S. Patent No. 5,942,917 ("Chappel") |
| Ex. 1007 | U.S. Patent No. 6,028,814 ("Lim") |
| Ex. 1008 | U.S. Patent No. 6,339,835 ("Reddy") |
| Ex. 1009 | Lee et al., "A 1 Gbit Synchronous DRAM Random Access Memory <br> with an Independent Subarray-Controlled Scheme and a Hierarchical <br> Decoding Scheme," IEEE Journal of Solid-State Circuits, Vol. 33, <br> No. 5, 1998 ("Lee") |
| Ex. 1010 | U.S. Patent No. 5,742,554 ("Fujioka") |
| Ex. 1011 | Wang et al., "Noise-Tolerant Dynamic Circuit Design," Proceedings <br> of the 1999 IEEE International Symposium on Circuits and Systems <br> VLSI, 1999 ("Wang") |
| Ex. 1012 | Kirihata et al., "A 390-mm', 16-Bank, 1-Gb DDR SDRAM with <br> Hybrid Bitline Architecture," IEEE Journal of Solid-State Circuits, <br> Vol. 34, No. 11, Nov. 1999 ("Kirihata") |
| Ex. 1013 | RESERVED |
| Ex. 1014 | RESERVED |
| Ex. 1015 | Taur et al., Fundamentals of Modern VLSI Devices, 2009 ("Taur") <br> Ex. 1016Baker, R. J., CMOS Circuit Design, Layout, and Simulation, First <br> Edition, IEEE Press 1997 ("Baker") |
| Ex. 1017 | File History for U.S. Provisional Application No. 60/185,301 |

## I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests inter partes review ("IPR") of claims 1-6 of U.S. Patent No. 6,597,201 ("the '201 patent") (Ex. 1001), which, according to PTO records, is assigned to ProMOS Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

## II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

Related Matters: Patent Owner has asserted the '492 patent against Petitioner in ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al., No. 1:18-cv-00307-RGA (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 5,934,974 ("the '974 patent"), 6,099,386 ("the '386 patent"), 6,469,559 ("the '559 patent"), and $6,163,492$ ("the '492 patent") in this action. Petitioner is concurrently filing petitions challenging one or more claims in these patents.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Chetan R. Bansal (Limited Recognition No. L0667). Service information is Paul Hastings LLP, 875 15th St. N.W.,

Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

## III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

## IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the ' 201 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

## V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

## A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1-6 ("challenged claims") of the '201 patent, and cancellation of these claims as unpatentable.

## B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable in view of the following grounds:

Ground 1: Claims 1-6 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over U.S. Patent No. 5,742,554 to Fujioka ("Fujioka") (Ex. 1010) and U.S. Patent No. 5,812,485 to Yuh ("Yuh") (Ex. 1005).

Ground 2: Claims 1-6 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Fujioka (Ex. 1010), Lee et al., "A 1 Gbit Synchronous DRAM Random Access Memory with an Independent Subarray-Controlled Scheme and a Hierarchical Decoding Scheme," IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998 ("Lee") (Ex. 1009), and Yuh (Ex. 1005).

Ground 3: Claims 1-5 are unpatentable under pre-AIA 35 U.S.C. § 103 over Applicant Admitted Prior Art ("AAPA") ${ }^{1}$, Yuh (Ex. 1005), and Fujioka (Ex. 1010).

The '201 patent issued from U.S. Application No. 09/650,494 ("the '494 application") filed August 29, 2000 and U.S. Provisional Application No. 60/185,301, filed February 28, 2000. (Ex. 1001, Cover).

Yuh issued on September 22, 1998. Fujioka issued on April 21, 1998. Thus, Yuh and Fujioka qualify as prior art at least under pre-AIA 35 U.S.C. § 102(b) with respect to the ' 201 patent.

Lee is an IEEE publication that was publicly available to persons interested and skilled in the art in May 1998, and at a minimum before February 28, 2000.
${ }^{1}$ AAPA qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 311(b) with respect to the '201 patent. See, e.g., One World Techs., Inc. v. Chamberlain Group, Inc., IPR2017-00126, slip op. at 9-10 (May 4, 2017) (Paper 8); see also Apple Inc., v. Qualcomm Inc., IPR2018-01316, slip op. at 22 (January 18, 2019) (Paper 7).

The Board has routinely held that IEEE publications like Lee are printed publications. For example, " $[t]$ he Board has previously observed that 'IEEE is a well-known, reputable compiler and publisher of scientific and technical publications, and we take Official Notice that members in the scientific and technical communities who both publish and engage in research rely on the information published on the copyright line of IEEE publications." Power Integrations, Inc., v. Semiconductor Components Industries, LLC, IPR2018-00377, Paper No. 10 at 10 (July 17, 2018) (quoting Ericsson, Inc. v. Intellectual Ventures I LLC, IPR2014-00527, Paper 41 at 11 (May 18, 2015)). Indeed, in Ericsson, the Board "accept[ed] the publication information on the IEEE copyright line on page 1 of [the IEEE reference] as evidence of its date of publication and public accessibility." Ericsson, IPR2014-00527, Paper 41, 10-11; see also Coriant (USA) Inc. v. Oyster Optics, LLC, IPR2018-00258, Paper 13 at 11 (June 6, 2018); Microsoft Corp. v. Bradium Techs. LLC, IPR2016-00449, Paper 9 at 13 (PTAB July 27, 2016) (noting generally that "IEEE publications, such as the one in which Reddy appeared, are distributed widely and intended to be accessible to the public").

Here, Lee bears the marking "IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 33, NO. 5, MAY 1998" at the top of each page, and the footer on the first page bears a marking "© 1998 IEEE." (Ex. 1009, 779-786.) With such
markings, Lee is similar to a reference that the Board recently found is a printed publication in Microsoft Corp. v. Koninklijke Philips N.V., IPR 2017-00890, Paper 49 at 19 (Sept. 6, 2018).

Moreover, Kirihata (Ex. 1012), an IEEE publication that was published in November 1999 (and thus before the alleged invention date of the '201 patent) and that does not have any co-authors in common with Lee, cites Lee, demonstrating that Lee was publicly accessible at least by November 1999. (Ex. 1012, 1580 (header stating "IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 11, NOVEMBER 1999" and footer stating "© 1998 IEEE," and listing co-authors other than those of Lee), 1586 (citation [28] is to Lee and includes a date of "May 1998").)

Therefore, for all of the foregoing reasons, Lee is a printed publication and qualifies as prior art under pre-AIA 35 U.S.C. § 102(b) by virtue of its publication in May 1998, or at least under pre-AIA 35 U.S.C. § 102(a) by virtue of its publication before February 28, 2000 (e.g., as demonstrated by Kirihata's citation to Lee).

None of Yuh, Fujioka, or Lee was considered by the Patent Office during prosecution of the '201 patent. (See generally Ex. 1001, References Cited.)

## VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '201 patent ("POSITA"), which for purposes of this proceeding is the late 1990s to early 2000s (including February 28, 2000, the filing date of the U.S. Provisional Application associated with the '201 patent), would have had a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated memory circuit design. (Ex. 1002, $\boldsymbol{\top} 20.)^{2}$ More education can supplement practical experience and vice versa. (Id.)

## VII. OVERVIEW OF THE ' 201 PATENT AND PRIOR ART

## A. The ' 201 Patent

The '201 patent relates to "dynamic predecoder for use in array decoding for integrated circuit memory chips." (Ex. 1001, 1:14-16; Ex. 1002, $\uparrow \uparrow 139-46$.) As disclosed by the '201 patent, "[d]ecoding circuitry is common in memory circuits to enable a particular row and/or a particular column for reading and/or writing." (Id., 1:17-19.) The '201 patent further discloses that such decoding circuitry often includes predecoder circuitry. (Id., 19-22.) According to the '201 patent, because "conventional predecoder circuits use static logic gates, typically full CMOS gates" such predecoder circuits are slow, require relatively large chip area, and

[^0]consume a large amount of power. (Id., 1:25-43.) Figure 2 of the '201 patent illustrates a predecoder that includes such a prior art predecoder, and the accompanying row decoders to which the predecoder is coupled, where the predecoder includes a static NAND gate.

(Id., FIG. 2.)
In order to overcome some of the alleged deficiencies of the prior art predecoders that rely on static logic gates, the '201 patent discloses predecoder circuits that use a dynamic NAND gates instead of a static NAND gate such as that shown in figure 2 above. (Id., 2:61-65.) Figure 3 of the '201 patent shows one such predecoder embodiment, where the static NAND of figure 2 , is replaced by a dynamic NAND.

(Id., FIG. 3.)
The dynamic NAND gate shown in the predecoder 30 of figure 3 includes a PMOS transistor 34 that receives a precharge signal P0B 44. (Id., 4:16-22.) The NMOS transistor 36 receives a row address line (RA 46) that "carries a row address selection signal." (Id., 4:23-30.) The NMOS transistor 38 has a gate electrode "connected to a bank active one shot line (BAOS) 48 which carries a bank active select signal." (Id., 4:31-34.) ${ }^{3}$ According to the '201 patent, the "bank active (BAOS) signal on bank active one shot line 48 goes HIGH when it is desired

[^1]to perform a decoding function for the particular memory cell bank associated with row predecoder circuit 30." (Id., 4:59-62.)

The above features were well known as discussed below in Section IX. (Ex. 1002, $\mathbf{9} \$ 61-241$; see also id., $\mathbf{9} \$ 48-60$ (describing the prior art).)

## VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under Phillips, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. Phillips, 415 F.3d at 1313; see also id., 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. Toyota Motor Corp. v. Cellport Systems, Inc., IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing Vivid Techs., Inc. v. Am. Sci. \& Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior art references and the challenged claims, Petitioner believes that no express
constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. ${ }^{4}$ (Ex. 1002, $\uparrow 47$.)

## IX. DETAILED EXPLANATION OF GROUNDS

As detailed below, the challenged claims are unpatentable based on Grounds 1-3. (Ex. 1002, 9 961 -241.)

## A. Ground 1: Claims 1-6 Are Obvious over Fujioka and Yuh

## 1. Claim 1

a) A method of predecoding an address selection signal in a memory circuit, comprising the steps of:

To the extent the preamble is limiting, Fujioka discloses this feature. (Ex. 1002, $9 \mathbb{1} 62-69$.) As explained below, Fujioka discloses a multi-bank memory in which addresses (e.g., row addresses) are predecoded by one or more predecoders and the predecoded addresses are then provided to decoders that further decode those predecoded addresses.

[^2]Figure 1 of Fujioka discloses "a block diagram of a DRAM" having four banks (bnk0~bnk3). (Ex. 1010, 3:47-48, 4:12-14.) Figure 2 of Fujioka discloses "a detailed block diagram of a memory chip which incorporates the DRAM shown in FIG. 1." (Id., 3:47-50, FIGs. 1-2.) As shown in annotated figure 2 below, Fujioka's memory includes a predecoder 2 (highlighted in red) within the memory chip 1. (Id., 4:45-54, FIG. 2.) Predecoder 2 receives address information from the address buffer/register circuit 4 (highlighted in blue) and provides a set of predecoded signals to corresponding decoding circuitry in decoder region 30 in each of the four banks. (Id., 4:58-5:7, FIG. 2; Ex. 1002, 9\{963-64.)

FIG. 2

(Ex. 1010, FIG. 2 (annotated); Ex. 1002, $\uparrow 63$.)

Fujioka's predecoding operation is further described below with reference to figures 3 and 4, where the discussion is focused at the bank level (i.e., for a single
bank). "FIG. 3 shows in detail each of banks of the memory chip shown in FIG. 2." (Ex. 1010, 5:9-10.) The decoder region 30 in each of the four banks "is supplied with a predecoded signal rap*z\# . . . from the corresponding predecoder 2 . . ." (Id., 5:29-32.) The predecoder 2 is described in further detail with reference to figure 4. For example, annotated figure 4 of Fujioka below shows that each bank includes predecoders 2-1, 2-2, and 2-3 (red), each of which decodes a different portion of the row address (blue). (Id., 5:50-56, FIG. 4; Ex. 1002, $\mathbf{9} \uparrow 665-$ 66.)

(Ex. 1010, FIG. 4 (annotated); Ex. 1002, 965 .)

Specifically, Fujioka discloses that "row address signals rla0~rla12" are supplied to "address buffers 4-1, 4-2, 4-3" (Ex. 1010, 5:62-65), which are then predecoded by predecoders 2-1, 2-2, 2-3. (Id., 6:19-28; Ex. 1002, $\uparrow 67$.

In view of the above, a POSITA would have understood that predecoder 2 in figure 2 is an abstraction of the predecoders across all banks in the memory chip 1 and that predecoders 2-1, 2-2, 2-3 (as shown in figure 4) constitute a subset of the predecoders in predecoder 2 shown in figure 2. (Ex. 1002, 9 968 -69.) Because Fujioka discloses operation of the predecoders 2 of figure 2, as well as predecoders 2-1, 2-2, 2-3 of figure 4, in the memory chip 1, Fujioka discloses a "method of predecoding" as recited in claim 1. (Id.) Fujioka's predecoding of the address signals discloses a "method of predecoding an address selection signal in a memory circuit" as recited in claim 1. (Id.; see also citations and analysis below for the remaining elements of this claim.)
b) providing a predecoder circuit comprising a dynamic NAND gate having a first circuit element and a second circuit element;

Fujioka in view of Yuh discloses or suggests this feature. (Ex. 1002, $9 \uparrow 770-$ 112.) As discussed above with respect to claim element 1 [a], Fujioka discloses predecoder circuits 2-1, 2-2, and 2-3. (Supra Section IX.A.1(a).) As explained below, each of these predecoder circuits 2-1, 2-2, and 2-3 comprises a "NAND
gate having a first circuit element and a second circuit element." (Ex. 1002, $\mathbf{9} \uparrow 770-$ 71.)

Figure 12 of Fujioka, shown in annotated form below, discloses an example predecoder circuit having four NAND gates. (Ex. 1010, 9:41-45, FIG. 12; Ex. 1002, $9972-85$ (explaining how the predecoder circuit of figure 12 is consistent with the configuration of predecoder circuits 2-1, 2-2, and 2-3).)

## FIG.I2


(Ex. 1010, FIG. 12 (annotated); Ex. 1002, 『772.)

Figure 13 of Fujioka shows a specific circuit arrangement of the NAND gate 27 highlighted above in figure 12. (Ex. 1010, 9:41-62.)

(Id., FIG. 13 (annotated); Ex. 1002, $\uparrow$ (86.)

The NAND gate 27 receives address signals ra0x and ra1x from the address buffer and a bank selection signal bnk\#x. (Ex. 1001, 9:57-10:14.) Depending on the states of these signals, NAND gate 27 outputs signal rap0z\#. (Id., 9:62-10-3; Ex. 1002, 987.$)$

Therefore, Fujioka discloses "providing a predecoder circuit comprising a ... NAND gate having a first circuit element and a second circuit element," as recited in claim element $1[b]$, where NAND gate 27 corresponds to the "NAND
gate" in which transistors Qn1 and Qn3 correspond to the "first circuit element" and "second circuit element," respectively. (Ex. 1002, $\mid 88$.)

But the NAND gate 27 shown in figure 13 of Fujioka is a static or "full" NAND circuit made up of six transistors. (Ex. 1002, 989 ; Ex. 1001, 2:1-5, FIG. 2.) As such, Fujioka does not disclose that the predecoder includes "a dynamic NAND gate" as recited in claim element $1[b]$. However, as discussed below, Yuh discloses using a "dynamic" NAND gate in a predecoder and a POSITA would have found it obvious to utilize a dynamic NAND gate for Fujioka's NAND gate 27 (discussed above with reference to figure 13 of Fujioka). (Ex. 1002, $\boldsymbol{9} \uparrow 89-112$.)

During prosecution of the '201 patent, Applicant acknowledged "that dynamic NAND gates were known in the prior art" but argued that the "use of a dynamic NAND gate in predecoder circuits to perform a predecoding function for memory circuits was not known or suggested by the prior art." (Ex. 1004 at 58, 75.) But to Applicant's assertions during prosecution, the use of dynamic NAND gates in predecoders in memory circuits was known at the time of the alleged invention, which is evidenced by, for example, Yuh. (Ex. 1002, $\boldsymbol{q} 990-96^{5}$.)

Like Fujioka, Yuh discloses a predecoder circuit in a memory device. (Id., 490.) For example, Yuh discloses with reference to figure 3 (reproduced below) a ${ }^{5}$ In fact, the use of a dynamic NAND in a predecoder is evident from figure 1 of the '201 patent, which is admitted as prior art. (Ex. 1002, 940, n.4.)
"column predecoder [30] of the conventional synchronous graphic RAM." (Ex. 1005, 4:33-34.) Therefore, a POSITA would have looked to Yuh when implementing Fujioka. (Ex. 1002, $\boldsymbol{\top} 90$. .)

(Ex. 1005, FIG. 3.)
As shown in figure 3 of Yuh, predecoder 30 includes a PMOS transistor P30 and NMOS transistor N30, whose gates are coupled to a signal EXTYAT. (Ex. 1005, 2:32-36.) The predecoder 30 also includes NMOS transistors N31, N32, and N33 (id., 2:37-40), each of which receives an address signal $A_{i}, A_{j}$, or $A_{k}$, respectively (id., 2:45-48, FIG. 3). The predecoder 30 additionally includes two
inverters INT30 and INT31 and a PMOS transistor P31 connected as shown in figure 3. (Id., 2:40-44, FIG. 3; Ex. 1002, ब991.)

A POSITA would have understood that transistors P30, N30, N31, N32, and N33 form a "dynamic NAND gate." (Ex. 1002, 9 T92-96.) First, a POSITA would have understood that transistors P30, N30, N31, N32, and N33 form a "NAND gate" because all four inputs (i.e., the enable signal EXTYAT and row address inputs $A_{i}, A_{j}$, and $A_{k}$ ) must be high for the output signal at "node 1 " to be low. (Id., 9992-93.) This is consistent with, for example, figures 7 and 8 of the '201 patent, which disclose dynamic NAND gates and where all the input signals must be high for the RAPB signal to be low. (Id.)

(Ex. 1005, FIG. 3 (annotated); Ex. 1002, 993.$)$
Second, a POSITA would have further understood that the NAND gate shown in figure 3 of Yuh is a "dynamic" NAND gate. ${ }^{6}$ (Ex. 1002, 994.$)$ A POSITA would have so understood because the NAND gate does not include full

[^3]set of CMOS transistors like in a "static" NAND gate. (Id.) For instance, unlike figure 13 of Fujioka, in which there is a PMOS transistor for every NMOS transistor, figure 3 of Yuh includes only one PMOS transistor P30 but includes four NMOS transistors. (Id.)

Indeed, figure 3 of Yuh discloses a "dynamic" NAND gate for the same reasons that each of figures 7 and 8 of the '201 patent disclose a "dynamic" NAND gate. (Id., 995.)

As explained below, a POSITA would have found it obvious to modify the circuit of figure 13 of Fujioka so that the "static" NAND gate is replaced by a "dynamic" NAND gate (like in Yuh) because such a modification would have provided several advantages (e.g., lower power consumption, more speed). (Id., T97.) Unwired Planet, LLC v. Google Inc., 841 F.3d 995, 1003 (Fed. Cir. 2016); KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 424 (2007).

A POSITA would have known the advantages of implementing logic circuits using dynamic logic gates, such as the dynamic NAND gate disclosed in Yuh, over using static logic gates, such as the static NAND gate disclosed in figure 13 of Fujioka. (Ex. 1002, 9998 -99 (citing Exs. 1006, 1007, 1008).) Indeed, it was well known prior to the alleged invention of the '201 patent that dynamic circuits (e.g., dynamic NAND gates) were faster and more power efficient compared to static NAND gates (such as the one disclosed in figure 13 of Fujioka). (Ex. 1005,

FIG. 3; Ex. 1011 at I-549, I-550; Ex. 1002, $9 \uparrow 98$-99.) The above understanding is consistent with the '201 patent, which describes dynamic logic gates as faster, taking up a smaller area, and consuming less power than static logic gates. (Ex. 1001, 2:2-12; Ex. 1002, $\mathbb{1} 100$.) As such, a POSITA would have been motivated to modify Fujioka in view of Yuh and a POSITA's knowledge, such that a dynamic NAND gate is used in place of the static NAND gate included in figure 13 circuit of Fujioka. (Ex. 1002, 『101.)

Modifying the circuit of figure 13 of Fujioka to replace the static NAND gate with a dynamic NAND gate would have only required removing two PMOS transistors (Qp3 and Qp2) from Fujioka's figure 13 circuit so that only a single PMOS transistor is provided (like in Yuh). (Id., $\mathbb{T} \uparrow 102,105-110$.) An exemplary and non-limiting demonstrative of the circuit of figure 13 of Fujioka modified in view of Yuh is provided below. (Id.)

(Ex. 1010, FIG. 13 (modified to remove PMOS transistors Qp3 and Qp2); Ex. 1002, $\uparrow 102$.

In view of the above, modifying Fujioka based on Yuh would have been obvious because a POSITA would have recognized that applying Yuh's technique (e.g., using a dynamic NAND gate in a predecoder) to Fujikoa's predecoder would have improved Fujioka's predecoder in the same way Yuh's use of a dynamic NAND gate improves Yuh's predecoder (e.g., reduces power consumption, increases speed, reduces chip area), and such application was within the level of ordinary skill. (Ex. 1002, बT103-104.) See Katz Interactive Call Processing Patent Litig. v. Am. Airlines, Inc., 639 F.3d 1303, 1323 (Fed. Cir. 2011); see also In re Schwemberger, 410 Fed. Appx. 298, 304 (Fed. Cir. 2010).

The modified Fujioka-Yuh predecoder discloses the claimed "providing a predecoder circuit comprising a dynamic NAND gate having a first circuit element and a second circuit element." (Ex. 1002, q\|T111-112.) For example, as illustrated in the annotated non-limiting and exemplary demonstrative below, the combination provides a predecoder having a dynamic NAND gate where the dynamic NAND gate includes a first NMOS transistor Qn1 ("first circuit element") and a second NMOS transistor Qn3 that ("second circuit element").

(Id., $\mathbb{1} 111$ (illustrating an exemplary configuration of the NAND gate in the Fujioka-Yuh combination).)
c) providing an inverter gate electrically coupled to said dynamic NAND gate and having an output terminal
electrically coupled to a plurality of row decoder circuits for the memory circuit;

The Fujioka-Yuh combination discloses or suggests this feature. (Ex. 1002,
9 91113-126.) As shown in a non-limiting demonstrative of the Fujioka-Yuh combination below, the Fujioka-Yuh combination includes an "inverter gate electrically coupled to said dynamic NAND gate and having an output terminal...." (Ex. 1002, 『113.)


Gate
(Ex. 1002, 『113.)

As further discussed below, Fujioka discloses that the output of the inverter is "electrically coupled to a plurality of row decoder circuits for the memory circuit," as recited in claim element $1[\mathrm{c}]$. (Id., $\mathbb{4} 114$.

As shown in annotated figure 12 of Fujioka below, the exemplary predecoder has four outputs (rap0z\# - rap3z\#), where each output is provided by an inverter. Figure 13 of Fujioka shows one of those outputs (rap0z\#). (Id., $\mathbb{1} 115$.

## FIG.I2


(Ex. 1010, FIG. 12 (annotated); Ex. 1002, 『115.)

## FIG.I3


(Ex. 1010, FIG. 13 (annotated) ${ }^{7}$; Ex. 1002, $\boldsymbol{\text { I }} 115$.)
Fujioka discloses that the outputs of each of the predecoders (and therefore, the outputs of the inverters) are "coupled to a plurality of row decoder circuits for the memory circuit." This is because, as discussed below, the outputs provided by each predecoder circuit (2-1, 2-2, 2-3) disclosed in Fujioka are coupled to a plurality of row decoder circuits (e.g., block decoders $10,1 / 4$ decoders 11 , and main

7 While the Fujioka-Yuh combination involves removing two of the PMOS transistors, the combination does not change the remaining configuration of Fujioka (e.g., how the output of the inverter is connected to the rest of Fujioka's circuitry). (Ex. 1002 at $\mathbb{1} 15$, n.11.)
word decoders 9). ${ }^{8}$ (Ex. 1010, FIG. 4, 6:28-36, 5:29-47, 5:48-57, 5:62-65, 6:22-27; Ex. 1002, © (116.)

For example, the outputs of predecoder 2-3 shown in annotated figure 4 below are provided to block decoders 10 , which select a particular block in the memory based on the row addresses rla8-rla12. (Ex. 1010, 6:38-40.) Because the block is selected based on the row address signals rla8-rla12, each of the block decoders 10 constitutes a row decoder circuit as the block decoders further decode a portion of the row address. (Id., 5:50-56, indicating the figure 4 shows the structure of row addresses and the decoders that decode the row addresses; id., 6:60-61; Ex. 1002, 『117.)

8 As explained by Dr. Baker, each of predecoder 2-1, 2-2, and 2-3 would be implemented based on the predecoder configuration of figure 12 such that the outputs of the predecoder of figure 12 would correspond to the outputs of predecoders 2-1, 2-2, and 2-3. (Ex. 1002 at $9 \uparrow / 77-85$.)

## Block Decoders


(Ex. 1010, FIG. 4 (annotated); Ex. 1002, ©117.)

As shown in more detail in annotated figure 6 below, the outputs of predecoders 2-3a and 2-3b, which form predecoder 2-3 in figure 4, are combined by the block decoders 10 to select one of 32 blocks in the bank. (Ex. 1010, 6:3739, FIGs. 4, 6.) As shown below in annotated figure 6, each of the block decoders (NAND gates 10) receives a predecoded row address signal from each of the predecoders 2-3a and 2-3b. (Id., FIG. 6.) Based on the predecoded address signals, one of the 32 NAND gates 10 outputs a low value that is subsequently
inverted to select a particular block in the bank of the memory. (Id.; Ex. 1002, ©118.)

## Block Decoders


(Ex. 1010, FIG. 6 (annotated); Ex. 1002, ©118.)

Each of the outputs of each of the predecoders 2-3a and 2-3b is provided to a plurality of the block decoders 10 . For example, each of braa0z-braa3z output from predecoder 2-3a is combined with each of brab0z-bra5z from predecoder 23b by one of the block decoders 10. (Ex. 1010, FIG. 6.) Therefore, each of the
outputs braa0z-braa3z is provided to six block decoders (one for each of brab0brab5), and each of brab0z-brab5z is provided to four block decoders (one for each of braa0-braa3). (Id.; Ex. 1002, 『119.)

Similarly, each of the outputs of the predecoder 2-2 is provided to a plurality of row decoders. For example, each output of the predecoder 2-2 is provided to a plurality of main word decoders, where Fujioka discloses that there are 64 main word decoders for each block. (Ex. 1010, 6:40-43, FIGs. 4, 5; see also id., claim 4.) As shown in annotated figure 4 below, each row predecoder 2-2 is coupled to a plurality of main word decoder circuits. (Ex. 1002, © 120 .)

(Ex. 1010, FIG. 4 (annotated); Ex. 1002, $\mathbb{9} 120$. )

As shown in figure 4 above, there are 64 main word decoders for each block. (Ex. 1010, FIG. 4) Just as the block decoders 10 in figure 6 combined one of the outputs from each of the predecoders $2-3 \mathrm{a}$ and $2-3 \mathrm{~b}$, each of the main word decoders combines one of the outputs from each of the predecoders 2-2a and 2-2b. (Id., 7:59-8:3.) For example, each output of predecoder 2-2a is provided to eight main word decoders in each set of main word decoders for each block (one for each of the outputs of predecoder $2-2 \mathrm{~b}$ ) and each output of predecoder $2-2 \mathrm{~b}$ is
provided to eight main word decoders in each set of main word decoders for each block (one for each of the outputs of predecoder 2-2a). Therefore, each output of the predecoders 2-2a and $2-2 \mathrm{~b}$ is provided to $8 \times 32=256$ main word decoders. (Ex. 1002, $9 \mathbb{1} \mid 121-122$.

(Ex. 1010, FIG. 5 (annotated); Ex. 1002, © 122.)

Each of the main word decoders constitutes a "row decoder circuit for the memory" as the main word decoders are used to further decode a portion of the row address to select a particular word line in the memory. (Ex. 1010, 5:37-38; id., 5:50-56, indicating the figure 4 shows the structure of row addresses and the decoders that decode the row addresses; id., 6:60-61; Ex. 1002, $\mathbb{1} 123$.

Figure 4 of Fujioka also shows that each of the outputs of the predecoder 2-1 is provided to a plurality of row decoder circuits. As shown in annotated figure 4 below, each main word decoder 9 is associated with four $1 / 4$ decoders 11 . (Ex. 1010, 8:52-9:4, FIGs. 4, 8, 9.) The outputs of the predecoder 2-1 are provided to the $1 / 4$ decoders corresponding to each of the main word decoders 11. (Id., 6:5659.) As noted above, there are 64 main word decoder circuits for each block and there are 32 blocks. Therefore the outputs of row predecoder 2-1 are provided to 2,048 1/4 decoders 11. (Ex. 1002, 124.)

(Ex. 1010, FIG. 4 (annotated); Ex. 1002, © 124. )

Each of the $1 / 4$ decoders 11 constitutes a "row decoder circuit for the memory" as the $1 / 4$ decoders are used to further decode a portion of the row address. (Ex. 1010, 5:50-56; Ex. 1002, థ125.)

Therefore, each predecoder of the Fujioka-Yuh combination includes an inverter gate that is coupled to the output of the dynamic NAND gate ("providing an inverter gate electrically coupled to said dynamic NAND gate") where the
output of the inverter is provided to a plurality of block decoders 10 , main word decoders 9 , or $1 / 4$ decoders 11 in the memory chip 1 ("[the inverter gate] having an output terminal electrically coupled to a plurality of row decoder circuits for the memory circuit"). (Ex. 1002, $\uparrow 126$.
d) selectively enabling said first circuit element with a first input signal comprising a self-timed one shot pulse signal indicative of an active memory bank for said memory circuit; and;

The Fujioka-Yuh combination discloses or suggests this feature. (Ex. 1002, 9¢(127-149.)

First, the Fujioka-Yuh combination discloses "selectively enabling said first circuit element with a first input signal . . . indicative of an active memory bank for said memory." (Id., 9|127-129.) The Fujioka-Yuh combination discussed above with respect to claim element $1[b]$ is reproduced below:

(Ex. 1002, 『127.)

As shown in the demonstrative above, transistor Qn1, which corresponds to the "first circuit element," receives the bank select signal bnk\#x, where the bank select signal indicates whether the bank within which the predecoder is included is selected (active). (Ex. 1010, 3:5-15; 9:45-48, 10:3-5, 7:8-11.) As described in Fujioka and depicted in the demonstrative above, if the bank selection signal bnk\#x is high (H), the output of the inverter 28 is low (L) and transistor Qn1 is off, whereas if the bank selection signal bnk\#x is low (L), the output of the inverter 28 is high (H) and transistor Qn 1 is on. Therefore, the Fujioka-Yuh combination
discloses turning the transistor Qn1 on or off based on the output of the inverter 28, which is the inverted version of the bank select signal bnk\#x ("selectively enabling said first circuit element with a first input signal" comprising a "signal indicative of an active memory bank for said memory circuit.") That is, the bank select signal bnk\#x is a "first input signal" and it is "indicative of any active memory bank for said memory circuit." (Ex. 1002, 『129.)

Second, while Fujioka does not explicitly disclose that the bank select signal bnk\#x is a "self-timed one shot pulse signal," Yuh discloses enabling predecoders using a "self-timed one shot pulse signal," and it would have been obvious to a POSITA to implement the bank select signal in the Fujioka-Yuh combination as a "self-timed one shot pulse signal." (Ex. 1002, $\mathbb{9} \uparrow 130-149$.) This is explained in detail below.

As discussed above with respect to claim element $1[\mathrm{~b}]$, Yuh discloses a "dynamic NAND gate" in figure 3. (Supra Section IX.A.1(b); Ex. 1002, $\mathbb{9} 131$.

(Ex. 1005, FIG. 3.)
Yuh discloses that the EXTYAT signal that enables the predecoder shown in figure 3 of Yuh (Ex. 1005, 2:19-20, 2:44-51) is "a self-timed one shot pulse signal." (Ex. 1002, $\mathbb{9} \uparrow 132-140$.) As shown in figure 1 of Yuh below, EXTYAT is generated based on a signal CASATV, which is "enabled during a read or write operation in the RAM." (Ex. 1005, 2:7-16; see also id. 1:41-2:32, FIGs. 1, 2; Ex. 1002, 『134.)

(Ex. 1005, FIG. 1 (annotated to show signal EXTYAT is fed back through circuit components including a delay portion 10.); Ex. 1002, $\mathbb{9} 134$.

The EXTYAT signal is a "one shot pulse signal" because it rises from a low level to a high level upon assertion of the CASATV signal, the high level is maintained for a certain period of time, and then EXTYAT falls back to a low level. (Ex. 1005, 2:27-31.) Specifically, EXTYAT is "LOW" when signal CASATV is "LOW" and becomes "HIGH" when "signal CASATV is input HIGH." (Id., 2:912.) By asserting CASATV (i.e., making CASATV "HIGH"), "signal EXTYAT is output HIGH" thereby enabling the predecoder. (Id., 2:12-20.) But once EXTYAT becomes "HIGH," it disables itself (i.e., goes LOW) after a period of time that is based on the time it takes EXTYAT to traverse through "inverter INT23, delay portion 10 and inverters INT24, INT25, and INT26." (Id., 2:27-31;

Ex. 1002, $9 \mathbb{1} 135-138$.$) The EXTYAT signal is, therefore, also a "self-timed"$ signal because, as discussed above, it disables itself after a certain period of time. (Ex. 1002, 『1139.) ${ }^{9}$

As discussed above, Yuh discloses that its predecoder uses a "self-timed one shot pulse signal" (i.e., the EXTYAT signal). Yuh discloses that the EXTYAT signal enables and disables predecoding because the address signals are only predecoded when the EXTYAT signal is HIGH. (Ex. 1005, 2:45-52; Ex. 1002, T140.) Therefore, the EXTYAT signal in Yuh performs the same function as the ${ }^{9}$ Notably, while Yuh's EXTYAT signal is disclosed to be a self-timed one shot signal, the '201 patent does not provide any support for what a "self-timed one shot" signal is or how such a signal would be generated. Indeed, the '201 patent describes the BAOS signal being generated "at the beginning of a bank active cycle that is bank specific" and further describes that "at the end of the cycle, the precharge cycle clock ( P 0 B ) signal fires to reset the predecoder and prepare the circuit for the next cycle." (Ex. 1001, 5:17-24.) It is unclear how the BAOS "one shot" signal in the '201 patent is self-timed, and instead, the description and timing diagrams shown in figures 4 and 6 of the '201 patent indicate that BAOS is not self-timed, but instead synchronized with the cycles of the memory. Beyond the simple label "self-timed one shot" in the claims, it is unclear how '201 patent supports the BAOS signal being "self-timed."
bank select signal (bnk\#x) in Fujioka, which also enables and disables predecoding. (Ex. 1002, 『140; Ex. 1010, 9:41-56.)

Accordingly, it would have been obvious to a POSITA to generate the bank select signals (e.g., bnk\#x) in the Fujioka-Yuh combination such that those bank select signals are self-timed one shot pulse signals like the EXTYAT signal in Yuh. (Ex. 1002, $\boldsymbol{\Phi} \uparrow 1141$-149.) The bank select signals in Fujioka are used to enable the predecoders (Ex. 1010, 9:43-56), but Fujioka does not provide details as to how those enable signals are generated. (Ex. 1002, $\mathbb{1} 141$.$) As discussed above, Yuh$ discloses details regarding how an enable signal for a predecoder can be generated, including how to generate an enable signal that is a self-timed one shot pulse signal.

Therefore, a POSITA would have been motivated to modify the FujiokaYuh combination such that the bank select signal (bnk\#x) is implemented as a selftimed one shot pulse signal like in Yuh. (Id., $9 \mathbb{T} \mid 142-148$.) As demonstrated below, implementing the bank select signals in the Fujioka-Yuh combination as self-timed one shot pulse signals is compatible with the functionality of the memory disclosed in Fujioka. Fujioka discloses a multi-bank memory, where the same address inputs are shared by each of the four banks included in the memory. (Ex. 1010, 4:12-19.) As further disclosed by Fujioka, a bank select signal is provided to the predecoders in each bank individually such that only the predecoders in the selected bank are
activated to decode the current state of the address inputs. (Id., 3:5-15; 9:45-48, 10:3-5, 11:41-58; Ex. 1002, 9142.$)$ Fujioka further discloses that each bank of the memory includes a number of blocks, where each block, and hence each bank, has its own respective set of sense amplifiers. (Ex. 1010, 4:14-15, "Each of the banks includes a predecoder 2 and a plurality of cell array/sense amplifier blocks 3-1, 32."; id., 4:62-64, FIGs. 1-3; Ex. 1002, థ143.)

A POSITA would have understood that a multi-bank memory such as that disclosed in Fujioka supports a different row being activated in each of the banks for read/write operations, thereby allowing for higher data throughput by interleaving accesses between banks. (Ex. 1002, $\boldsymbol{T} \mid 143-144$; Ex. 1010, 4:20-21.) Therefore, a POSITA would have understood that the bank select signal for a particular bank would only be asserted for a short period of time in order to enable the decoding circuitry for that selected bank to decode the address currently on the address inputs. (Ex. 1002, $\mathbb{1} 145$.) Once the address is decoded by the bank that is selected for that operation, the decoders in that bank are deselected such that when a new address appears on the address lines, which may be for a different bank, that address is not wrongly decoded by a non-selected bank. (Id.) In other words, the bank select signals are not asserted for an extended period of time when the address lines are shared amongst the banks. (Id.)

As noted above, Fujioka does not provide details as to the bank selector circuit 5 depicted, for example, in figure 4 of Fujioka. The bank selector 5 generates the bank select signals bnk0, bnk1, bnk2, and bnk3 based on the two highest order row addresses received from external to the chip via the address buffers 4 (rla14, rla13) or as generated by the refresh counter 14. Figure 4 does not show any other signals being received by the bank selector. (Ex. 1002, $\uparrow 1146$.)

As shown in the demonstrative below, the EXTYAT enable signal in Yuh is input to two transistors in the dynamic NAND circuit in the predecoder of Yuh in the same manner as the enable signal (bank select signal bnk\#x) is input to two transistors in the dynamic NAND circuit of the Fujioka-Yuh combination. (Ex. 1002, 『147.)

(Ex. 1002, 147.)
A POSITA would have understood that a pulse on the enable signal in the Fujioka-Yuh combination, just like that disclosed in Yuh, would allow the predecoders in the Fujioka-Yuh combination to be selectively enabled and disabled
at the appropriate times. (Ex. 1002, q9148-149.) Selectively enabling the predecoders in the Fujioka-Yuh combination would have allowed the row addresses provided to the memory in the Fujioka-Yuh combination to be only decoded by the selected bank by only enabling the decoder for that bank. (Id.) Using a self-timed one shot pulse signal for the bank select signal would have also ensured that that the predecoder would be disabled before a new address is presented on the shared address lines. (Id.) In view of the above benefits, a POSITA would have been motivated to implement the bank select signal (bnk\#x) as a "self-timed one shot pulse signal" like the EXTYAT signal in Yuh. (Id.) See Unwired Planet, 841 F.3d at 1003. A POSITA would have reasonably expected success in making such a modification without negatively affecting the operation of Fujioka's predecoders. (Ex. 1002, $\Phi \uparrow 1147-149$.)

Using such a self-timed one shot signal for the bank select is consistent with the disclosure of Fujioka, which indicates that the row address signals supplied to the memory are shared by all of the banks. (Id., $\mathbb{1} 149$.) Because all of the row address signals are shared, the bank select signal, which enables the predecoders, should only be asserted for the particular bank being accessed. (Id.) As shown in figure 4 of Fujioka, the bank selector 5, which is shared by all of the banks in the memory, does not receive any timing information that would be used to control the timing of the enable signals (bank select signals) provided by the bank selector.
(Id.) As such, using a signal similar to the self-timed EXTYAT signal of Yuh as each of the bank select signals bnk3x, bnk2x, bnk1x, and bnk0x in the FujiokaYuh combination is consistent with the operation of the memory in Fujioka. (Id.)

For at least these reasons, a POSITA would have found it obvious to implement the bank select signal provided to the dynamic NAND gate in the Fujioka-Yuh combination as a "self-timed one shot pulse signal."
e) selectively enabling said second circuit element with a second input signal indicative of a selected memory row address for said active memory bank.

The Fujioka-Yuh combination discloses or suggests this feature. (Ex. 1002,
9 1 150-152.) For example, as discussed above in Section IX.A.1(b), the FujiokaYuh combination may be illustrated by the following non-limiting demonstrative:

(Ex. 1002, $\uparrow 150$.

As shown above, transistor Qn3, which corresponds to the "second circuit element," receives the row address signal ra0x. (Ex. 1010, 9:43-45, 9:47-51.) As disclosed by Fujioka, when the bank select signal for the NAND gate shown in figure 13 is asserted, "the output signal rap0z\# is brought into an H level or an L level depending on the states of the output signals ra0x, ra1x from the address buffer." (Id., 9:62-10:1.) Therefore, as described in Fujioka and depicted in the demonstrative above, if the row address (ra0x) signal is low (L), the output of the transistor Qn 3 is off, whereas if the row address (ra0x) is high (H), the transistor

Qn3 is on. (Ex. 1002, $\mathbb{1} 151$.) Whether or not ra0X is high or low depends on the row being selected by the address provided to the memory circuit. Therefore, the Fujioka-Yuh combination discloses turning the transistor Qn3 on or off based on state of the row address signal ra0x provided as part of a selected memory row address ("selectively enabling said second circuit element with a second input signal indicative of a selected memory row address for said active memory bank.") The row address signal ra0x is shared by all banks in the memory, including the selected bank, and therefore is "indicative of a selected memory row address for said active memory bank." (Id.)

## 2. Claim 2

a) The method of claim 1 further comprising the steps of providing said predecoder circuit with a precharge circuit, generating a precharge control signal, and selectively enabling said precharge circuit with said precharge control signal.

The Fujioka-Yuh combination discloses or suggests this feature. (Ex. 1002, 9ब153-157.) For example, as discussed above in Section IX.A.1(b), the NAND gate included in the predecoder of the Fujioka-Yuh combination may be illustrated by the following non-limiting demonstrative:

(Ex. 1002, $\uparrow 153$.
A POSITA would have understood that transistor Qp1 in the above circuit is a "precharge circuit." (Ex. 1002, $\mathbb{1} 154$.$) Specifically, transistor Qp1 turns on$ when the bank selection signal bnk\#x is in an unselected state (H level) thereby providing a high level at the input of the inverter that outputs signal rap0z\#. (Id.; Ex. 1010, 10:3-8 (explaining that when bank selection signal bnk $\# \mathrm{x}$ is in an unselected state (H level), the output rap0z\# is a low level).) That is, transistor Qp1 pulls the input of the output inverter (i.e., the inverter rap0z\#) high to "forcibly" bring rap0z\# to a low level regardless of the states of the row address
signals ra0x and ra1x. (Id.) Therefore, transistor Qp1 is a "precharge" circuit and bnk\#x is a "precharge signal" because bnk\#x turns on transistors Qp1 allowing it to pull high the input to the output inverter. (Ex. 1002, $\mathbb{9} 155$.) Indeed, transistor Qp1 continues to pull the output of the NAND gate (i.e., the input to the output inverter high) until the bank selection signal bnk\#x goes to a selected level (L level) at which time the address signals ra0x and ra1x become meaningful (i.e., capable of affecting the output rap0z\#). (Id.; Ex. 1010, 9:43-56.)

Accordingly, the Fujioka-Yuh combination discloses "providing said predecoder circuit with a precharge circuit" because the combination provides transistor Qp1 in the predecoder circuit. (Ex. 1002, ©156.) The combination also discloses "generating a precharge control signal" because it discloses generating a bank selection signal bnk\#x. (Id.) The combination further discloses "selectively enabling said precharge circuit with said precharge control signal" because the bank selection signal bnk\#x turns transistor Qp1 on or off depending on whether it is high or low. ${ }^{10}$ (Id.)
${ }^{10}$ As discussed above with respect to claim element 1[d], the bank selection signal is "first input signal." For claim 2, Petitioner maps the same signal to the "precharge control signal." This is permissible because the '201 patent contemplates that the same signal can constitute both the "precharge signal" and the "first input signal." (See Ex. 1001, claim 4, "selectively enabling said

The understanding that Qp1 corresponds to a "precharge circuit" and that the signal provided to the gate of Qp1 is a "precharge control signal" is consistent with the disclosure of the '201 patent. (Ex. 1002, $\mathbb{1} 157$. )

## 3. Claim 3

a) The method of claim 2 wherein said precharge circuit is selectively enabled by said precharge control signal only during such periods of time in which said first circuit element is not enabled by said first input signal.

The Fujioka-Yuh combination discloses or suggests this feature. (Ex. 1002, 9 91 158-160.) For example, as discussed above in Section IX.A.1(b), the FujiokaYuh combination may be illustrated by the following non-limiting demonstrative:

[^4]
(Ex. 1002, 『158.)
As discussed above with respect to claim 2, transistor Qp1 turns on when the bank selection signal bnk\#x ("first input signal" and "precharge signal") is a high level, which makes the output of inverter 28 low. (Supra Section IX.A.2.) But when the output of inverter 28 is low, transistor Qn1 ("first circuit element") is turned off because transistor Qn1 is an NMOS transistor. (Ex. 1002, $\mathbb{1} 159$; Ex. 1010, 9:64-65 (explaining that transistor Qn1 requires the output of inverter 28 to a high level to turn on).) Therefore, the Fujioka-Yuh combination discloses "said precharge circuit is selectively enabled by said precharge control signal only
during such periods of time in which said first circuit element is not enabled by said first input signal" because transistor Qp1 ("precharge circuit") is only enabled by the bank selection signal bnk\#x ("precharge control signal") when transistor Qn1 is turned off by the bank selection signal bnk\#x ("first input signal"). (Ex. 1002, ©159.)

The understanding that Qp1 is only on when Qn1 is turned off in the Fujioka-Yuh combination such that "said precharge circuit is selectively enabled by said precharge control signal only during such periods of time in which said first circuit element is not enabled by said first input signal" is consistent with the disclosure of the '201 patent. (Ex. 1002, $\mathbb{1} 160$.)

## 4. Claim 4

a) The method of claim 1 further comprising the steps of providing said predecoder circuit with a precharge circuit, and selectively enabling said precharge circuit with said first input signal.

The Fujioka-Yuh combination discloses or suggests this feature. (Ex. 1002,
【161.) As discussed above with respect to claim 2, transistor Qp1 is a "precharge circuit" that is selectively enabled by bank selection signal bnk\#x ("first input signal"). (Supra Section IX.A.2.)

## 5. Claim 5

a) The method of claim 4 wherein said precharge circuit is selectively enabled by said first input signal only during such periods of time in which said first circuit element is
not enabled by said first input signal.
The combination of Fujioka and Yuh discloses or suggests this feature. (Ex.
1002, 【162.) As discussed above with respect to claim 3, transistor Qp1 ("precharge circuit") is selectively enabled by the bank selection signal bnk\#x ("selectively enabled by said first input signal") and when that happens, transistor Qn1 is turned off ("said first circuit element is not enabled by said first input signal"). (Supra Section IX.A.3.)

## 6. Claim 6

a) The method of claim 1 further comprising the step of selectively electrically coupling said inverter to one or more row decoder circuits provided for said memory circuit.

The combination of Fujioka and Yuh discloses or suggests this feature. (Ex. 1002, $99163-177$.$) For example and as demonstrated below, the block decoder$ circuitry disclosed in Fujioka selectively electrically couples each output of the predecoder 2-3a to a plurality of main word decoders in the row decoding scheme disclosed in Fujioka.

As discussed above with respect to claim feature 1 [c], in the Fujioka-Yuh combination, each of the predecoders 2-3, 2-2, and 2-1 shown in figure 4 of Fujioka includes an inverter gate at the output of the dynamic NAND circuits included in the predecoders. (Supra Section IX.A.1(c).) The output terminal of each inverter, which corresponds to an output of the predecoder, is electrically
coupled to a corresponding row decoder circuit (e.g., block decoder 10, main word decoder 9, or $1 / 4$ decoder 11). (Id.; Ex. 1002, $\mathbb{1} 164$.)

(Ex. 1002, $\uparrow 164$.
For example, as discussed above in Section IX.A.1(c), each output from the predecoder 2-3 (e.g., braa0z) is provided to a plurality of block decoders (NAND gates 10). (Ex. 1010, FIG. 6 (reproduced below).) As also discussed above in Section IX.A.1(c), this output (e.g., braa0z) would be output by an inverter in the predecoder 2-3a. Therefore, each inverter in predecoder 2-3 is "electrically
coupled" to a plurality of row decoder circuits (e.g., block decoders 10). (Id.; Ex. 1002, 『165.)

## Block Decoders


(Ex. 1010, FIG. 6 (annotated); Ex. 1002, 9165. )
As explained in detail below, each of the inverters in the predecoder 2-3 is "selectively" electrically coupled to one or more main word decoders 9 ("one or more row decoder circuits provided for said memory circuit"). Specifically, as explained below, the combination of a block decoder 10 and the inverter following
the block decoder 10 forms an AND gate that acts as a "switch" between the output of the predecoder 2-3 and a main word decoder 9. (Ex. 1002, $\mathbb{9} 166$.)

As shown in annotated figure 4 below, the outputs of predecoder 2-3 are provided to the block decoders 10, which in turn provide block selection information (blk*z) to the main word decoders 9. (Ex. 1010, 6:37-39; id., FIGs. 4, 6; Ex. 1002, 『167.)

## Main Word

## Block Decoders

FIG. 4

(Ex. 1010, FIG. 4 (annotated); Ex. 1002, ©167.)

As shown in more detail in annotated figure 6 below, each of the block decoders (NAND gates 10) receives a predecoded row address signal from each of
the predecoders 2-3a and 2-3b. (Id., FIG. 6.) For example, the block decoder 10 that is used to generate blk0z\# receives braa0z from predecoder $2-3 \mathrm{a}$ and brab0z from predecoder 2-3b (highlighted in blue below). (Id.; Ex. 1002, $\uparrow 168$.

## Block Decoders


(Ex. 1010, FIG. 6 (annotated); Ex. 1002, © 168.)

As shown in annotated figure 6 above, the output of each of the block decoders 10 is inverted by an inverter to produce each blk*z\# signal. Therefore, as shown below, the logical function performed by the block decoders (NAND) in combination with the subsequent inverter is a logical AND. (Ex. 1002, $\mathbb{4} 169$.)

(Ex. 1010, FIG. 6 (annotated); Ex. 1002, ©169.)

As explained below, a POSITA would have understood that the logical AND function selectively electrically couples a first one of the predecoder outputs (e.g. the output received from predecoder 2-3a) to the corresponding blk*z\# signal based on the state of the second one of the predecoder outputs (e.g. the output received from predecoder 2-3b). (Ex. 1002, $\uparrow 170$.)

It was well known before the alleged invention of the '201 patent that a twoinput AND gate, such as that formed by the combination of the NAND gate and
subsequent inverter shown in figure 6 of Fujioka, was a logic gate with the truth table depicted below.


| $A$ | $B$ | $C$ |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

(Ex. 1002, 『171.)

Therefore, the state of the second input 'B' (i.e., whether that input is LOW or HIGH) determines whether the state of the other input ' A ' is passed through the AND gate to the output 'C.' (Ex. 1002, 99172-173.) The demonstrative below shows that this relationship corresponds to the functionality of a switch where the input B of the AND gate controls the switch to select either (1) the input 'A' or (2) a logic LOW (' 0 ') as the output of the AND gate. (Id.)

$$
\mathbf{B}=\mathbf{0}
$$

$$
B=1
$$

A O


If $\mathbf{B}=0$, Output $\mathbf{C}=0$ (Regardless of A)

A


0
If $\mathbf{B}=1$, Output $\mathbf{C}=\mathbf{A}$
(A Passes Through)
(Ex. 1002, 『173.)

In view of the above, a POSITA would have understood that when the input to the block decoder 10 from predecoder 2-3b is LOW (' 0 '), the corresponding blk*z\# signal (i.e. output of the inverter coupled to the block decoder 10) is LOW (' 0 '). Such a POSITA would also have understood that, when the input to the block decoder 10 from predecoder 2-3b is HIGH (' 1 ') the corresponding blk*z\# signal is the same as the input of the block decoder from the predecoder 2-3a. The demonstrative below shows this relationship with respect to the block decoder 10 that is used to generate the blk0z\# signal, where the output of the predecoder 2-3b (brab0z) determines whether or not the output of the predecoder 2-3a (braa0z) is passed to blk0z\#. (Ex. 1002, 9174.$)$

(Ex. 1010, FIG. 6 (annotated); Ex. 1002, © 174. )

(Ex. 1002, 『174.)

In the annotated version of figure 6 above, if brab0z is $\operatorname{HIGH}$ (' 1 '), then blk0z\# = braa0z, whereas if brab0z is LOW (' 0 '), then blk0z\# is LOW (' 0 '). (Ex.

1002, $\mathbb{\$ 1 7 5 . )}$ Therefore, a POSITA would have understood that the block decoder 10 in combination with the inverter at its output "selectively couples" the input braa0z to the output blk0z\# based on the state of brab0z. (Id.) As discussed above with respect to claim feature $1[\mathrm{c}]$, each of braa0 z and brab 0 z corresponds to the output of a predecoder, and, more particularly, to the output of an inverter gate coupled to the output of a dynamic NAND in a predecoder of the Fujioka-Yuh combination. (Id.; see supra Section IX.A.1(c).) Therefore, the output of an inverter gate in the predecoder 2-3a, i.e., signal braa0z is "selectively electrically coupled" to one of the outputs of the block decoder 10, i.e., blk0z.

But, as explained below, each output of the block decoder 10 (e.g., blk0z) is provided to one or more main word decoders 9. For example, as shown in annotated figure 4 below, each of the outputs (blk*z\#) of the block decoders 10 is coupled to a plurality of main word decoders 9. (Ex. 1002, $\uparrow 176$.)

(Ex. 1010, FIG. 4 (annotated); Ex. 1002, 『176.)

For example, the top block decoder 10 ("b dec 0 ", highlighted in red), which corresponds to the block decoder discussed above with respect to figure 6 , generates the blk 0 z signal (highlighted in blue) that is provided to 64 main word decoders 9 (highlighted in green). (Ex. 1008 at FIG. 4; Ex. 1002, $\mathbb{1} 177$. ) As discussed above with respect to claim element $1[\mathrm{c}]$, each of the main word decoders 9 corresponds to a "row decoder circuit" as recited in claims 1 and 6. (Ex. 1002, 9177 ; see supra Section IX.A.1(c).) Therefore, a POSITA would have understood that each block decoder 10 "selectively electrically couples" the output it receives from predecoder 2-3a (e.g., braa0z) to a plurality of main word decoders
based on the state of an output from predecoder 2-3b (e.g., brab0z). (Ex. 1002, T177.) As noted above, the output of each of the predecoders corresponds to the output of an inverter in the predecoder of the Fujioka-Yuh combination. Therefore, a POSITA would have understood that the Fujioka-Yuh combination discloses claim 6. (Id.)

## B. Ground 2: Claims 1-6 Are Obvious over Fujioka, Lee, and Yuh 1. Claim 1

a) A method of predecoding an address selection signal in a memory circuit, comprising the steps of:

To the extent the preamble is limiting, Fujioka discloses this feature for the same reasons as discussed above in Section IX.A.1(a). (Ex. 1002, 『178.)
b) providing a predecoder circuit comprising a dynamic NAND gate having a first circuit element and a second circuit element;

Fujioka in view of Lee discloses or suggests this feature. (Ex. 1002, $19179-$ 197.) As discussed above in Section IX.A.1(b), Fujioka discloses a predecoder circuit comprising a "static" NAND gate having a first circuit element (Qn1) and a second circuit element (Qn3).

FIG.I3

(Ex. 1010, FIG. 13 (annotated); Ex. 1002, $\mathbb{\text { |l179.) }}$

But Fujioka does not disclose a "dynamic" NAND gate. (Supra Section IX.A.1(b).) However, as discussed below, Lee discloses a row predecoder circuit having a "dynamic NAND gate," and a POSITA would have been motivated, in light of Lee, to utilize a dynamic NAND gate for Fujioka's NAND gate 27 (discussed above with reference to figure 13 of Fujioka). (Ex. 1002, © 180.)

As discussed in Section IX.A.1(b), Applicant's contention that the "use of a dynamic NAND gate in predecoder circuits to perform a predecoding function for memory circuits was not known or suggested by the prior art." (Ex. 1004 at 58; id., 75.) Yuh demonstrates that such a contention is incorrect. (Supra Section
IX.A.1(b).) Lee similarly falsifies Applicant's contention and demonstrates that the use of dynamic NAND gates in predecoders was well-known.

Lee discloses "1 Gbit Synchronous Dynamic Random Access Memory with an Independent Subarray-Controlled Scheme and a Hierarchical Decoding Scheme". (Ex. 1009, 779 (Title).) The memory disclosed in Lee uses a "hierarchical decoding scheme with a dynamic CMOS series logic predecoder [that] achieves improvements in circuit speed, power, and complexity." (Id., 779 (Abstract, emphasis added).) Therefore, Lee discloses a decoding scheme that relies on both predecoders and decoders, and Lee further discloses that dynamic logic is used in the predecoders, thereby providing numerous advantages. (Id.; Ex. 1002, 『181.)

The predecoder disclosed in Lee is illustrated in figure 7(b), where the predecoder receives address signals ("address selection signals") that are predecoded by the predecoder to produce decoded address signals $\mathrm{DA}_{\mathrm{ij}}$. (Id., 783; Ex. 1002, © 182.$)$


Fig. 7. Circuit schematics for (a) conventional predecoder and (b) new CMOS series logic predecoder.
(Ex. 1009, FIG. 7(b) (annotated); Ex 1002 at 9182. )

The predecoder circuit of Lee includes a dynamic NAND, which is highlighted in the annotated excerpt of figure 7(b) below. (Ex. 1007 at 779, 783; id., FIG. 7(b); Ex. 1002, 『183.)


Gate
(Id., FIG. 7(b) (excerpt, annotated); Ex. 1002, 『1183.)
As shown in the annotated excerpt of figure $7(\mathrm{~b})$ above, when $\Phi_{\text {DAEP }}, \mathrm{A}_{\mathrm{i}}$, and $\mathrm{A}_{\mathrm{j}}$ are all high, the dynamic NAND output node (highlighted in green) is pulled low. Therefore the state of the output node is a logical NAND of $\Phi_{\text {DAEP }}, \mathrm{A}_{\mathrm{i}}$, and $A_{j}$. (Ex. 1002, $\left.\boldsymbol{1 9} 184-185.\right)$ Indeed, the dynamic NAND gate shown in annotated figure 7(b) of Lee above operates in the same manner as the dynamic NAND gates illustrated in the embodiments of the '201 patent, including those shown in annotated figures 7 and 8. (Ex. 1001, 5:3-17, FIG. 3; Ex. 1002, 『185-186.)

As shown in the annotated excerpt of figure 7(b) of Lee below, the dynamic NAND gate includes a "first circuit element" and a "second circuit element." Specifically, the transistor that receives the decoded address enable pulse signal $\Phi_{\text {DAEP }}$ is a "first circuit element" and the transistor that receives the address signal $A_{i}$ or the transistor that receives the address signal $A_{j}$ is a "second circuit element." (Ex. 1009, 783, FIG. 7.) Therefore, Lee discloses "providing a predecoder circuit comprising a dynamic NAND gate having a first circuit element and a second circuit element" as recited in claim element 1[b]. (Ex. 1002, $\mathbb{1} 187$. )

## Dynamic NAND <br> Output Node



First Circuit
Element

## Dynamic <br> NAND <br> Gate

(Ex. 1009, FIG. 7(b) (excerpt, annotated); Ex. 1002, $\mathbb{1} 187$.

As discussed above in Section IX.A.1(b), dynamic circuits were known to have several advantages (e.g., higher speed, lower power consumption, lesser chip area) over static circuits. (See supra Section IX.A.1(b).) For example, Lee discloses that using dynamic logic (e.g. the dynamic NAND circuit depicted in figure 7(b)) in a hierarchical decoding scheme provides "improvements in circuit speed, power, and complexity." (Ex. 1009, 779; Ex. 1002, $\mathbb{1} 188$.

Therefore, a POSITA would have been motivated to replace the static NAND gate in Fujioka (figure 13) with a dynamic NAND gate (like in Lee) because doing so would have resulted in, inter alia, reduced capacitance, faster speed, lower power consumption. (Ex. 1002, $\mathbb{1} 189$; supra Section IX.A.1(b).) See Unwired Planet, 841 F.3d at 1003; KSR, 550 U.S. at 424. Additionally, as a dynamic NAND gate requires fewer transistors than a static NAND gate, a POSITA would have been able to reduce the area occupied by the logic gate and thereby increase the density of the circuit components and number of bits that can be stored in a memory device. (Ex. 1002, ©189.)

Modifying the static NAND gate in Fujioka to be a dynamic NAND gate would have merely involved removing two of the PMOS transistors in the static NAND gate. A POSITA would have understood how to modify the static NAND of Fujioka to be a dynamic NAND as shown in Lee while preserving the functionality of the NAND gate and related circuitry. (Ex. 1002, बTी190-197; supra Section IX.A.1(b).) An exemplary and non-limiting demonstrative showing the modification is set forth below. (Id., $\mathbb{9} 190$.)

(Ex. 1002, 『190.)

As shown in the demonstrative above, the modified Fujioka-Lee row predecoder discloses the claimed "providing a predecoder circuit comprising a dynamic NAND gate having a first circuit element and a second circuit element." (Id., © 191.)
c) providing an inverter gate electrically coupled to said dynamic NAND gate and having an output terminal electrically coupled to a plurality of row decoder circuits for the memory circuit;

The Fujioka-Lee combination discloses or suggests this feature. (Ex. 1002, 94198-199.) As shown in the demonstrative of the Fujioka-Lee combination
(reproduced below), the Fujioka-Lee combination includes an "inverter gate electrically coupled to said dynamic NAND gate and having an output terminal ...." (Ex. 1002, 『198.)


Dynamic
NAND

## Gate

(Id., $\mathbb{1} 198$.$) Moreover, as discussed above in Section IX.A.1(c), the output$ terminal of the inverter (e.g., rap0z\#) is "electrically coupled to a plurality of row decoder circuits for the memory circuit." The combination of Fujioka and Lee does not change this aspect of Fujioka's circuit because the combination merely involves removing two of the PMOS transistors in Fujioka's figure 13 circuit. (Id., - 1199.$)$
d) selectively enabling said first circuit element with a first input signal comprising a self-timed one shot pulse signal indicative of an active memory bank for said memory circuit; and

Fujioka in combination with Lee and Yuh discloses or suggests this feature.
(Ex. 1002, $\mathbb{T} \mid 200-202$.$) The Fujioka-Lee combination discussed above with$ respect to claim element $1[\mathrm{~b}]$ is reproduced below:

(Ex. 1002, 『200.)

As discussed above in Section IX.A.1(d), Fujioka discloses "selectively enabling said first circuit element with a first input signal . . . indicative of an active memory bank for said memory" based on its disclosure of the bank selection
signal bnk\#x. (Supra Section IX.A.1(d).) The modification of Fujioka based on Lee does not affect this aspect of Fujioka. (Ex. 1002, 『|201.) Therefore, the Fujioka-Lee combination discloses "selectively enabling said first circuit element with a first input signal" comprising a "signal indicative of an active memory bank for said memory circuit." That is, the bank select signal bnk\#x is a "first input signal" and it is "indicative of any active memory bank for said memory circuit."

But the Fujioka-Lee combination discussed above does not explicitly disclose that the bank select signal bnk\#x is a "self-timed one shot pulse signal," as recited in claim element 1[d]. However, as discussed above in Section IX.A.1(d), Yuh discloses that one of the input signals to the dynamic NAND gate is a "selftimed one shot pulse signal." (Supra Section IX.A.1(d).) In view of Yuh's teachings, a POSITA would have found it obvious to modify the bank selection signal bnk\#x in the Fujioka-Lee combination to be a "self-timed one shot pulse signal," for reasons discussed above in Section IX.A.1(d). (Ex. 1002, $\uparrow$ 202.)
e) selectively enabling said second circuit element with a second input signal indicative of a selected memory row address for said active memory bank.

The Fujioka-Lee-Yuh combination discloses or suggests this feature. (Ex.
1002, $\boldsymbol{9}$ 203.) For example, as discussed above in Section IX.A.1(e) and as shown in the non-limiting demonstrative below, the combined Fujioka-Lee-Yuh circuit discloses turning the transistor Qn 3 on or off based on state of the row address
signal ra0x provided as part of a selected memory row address ("selectively enabling said second circuit element with a second input signal indicative of a selected memory row address for said active memory bank."). (See supra Section IX.A.1(e).)

(Ex. 1002, 203.) The combination of Fujioka with Lee and Yuh does not change this aspect of Fujioka.

## 2. Claim 2

The Fujioka-Lee-Yuh combination discloses or suggests this feature. (Ex. 1002, 【204.) Specifically, the combination discloses or suggests this feature for
the same reasons as those discussed above in Section IX.A.2. The combination of Fujioka with Lee and Yuh does not affect Fujioka's disclosure of this feature. (Id.)

## 3. Claim 3

The Fujioka-Lee-Yuh combination discloses or suggests this feature. (Ex. $1002, \mathbb{T} 205$.$) Specifically, the combination discloses or suggests this feature for$ the same reasons as those discussed above in Section IX.A.3. The combination of Fujioka with Lee and Yuh does not affect Fujioka's disclosure of this feature. (Id.)

## 4. Claim 4

The Fujioka-Lee-Yuh combination discloses or suggests this feature. (Ex. $1002, \mathbb{9}$ 206.) Specifically, the combination discloses or suggests this feature for the same reasons as those discussed above in Section IX.A.4. The combination of Fujioka with Lee and Yuh does not affect Fujioka's disclosure of this feature. (Id.)

## 5. Claim 5

The Fujioka-Lee-Yuh combination discloses or suggests this feature. (Ex. $1002, \boldsymbol{q}[207$.$) Specifically, the combination discloses or suggests this feature for$ the same reasons as those discussed above in Section IX.A.5. The combination of Fujioka with Lee and Yuh does not affect Fujioka's disclosure of this feature. (Id.)

## 6. Claim 6

The Fujioka-Lee-Yuh combination discloses or suggests this feature. (Ex.
1002, 【208.) Specifically, the combination discloses or suggests this feature for
the same reasons as those discussed above in Section IX.A.6. The combination of Fujioka with Lee and Yuh does not affect Fujioka's disclosure of this feature. (Id.)

## C. Ground 3: Claims 1-5 Are Obvious over AAPA, Yuh, and Fujioka

## 1. Claim 1

a) A method of predecoding an address selection signal in a memory circuit, comprising the steps of:

To the extent the preamble is limiting, AAPA discloses this feature. (Ex. 1002, $\boldsymbol{\top} \mid 209-213$.$) For example, AAPA discloses with reference to figure 2$ (reproduced below) a row predecoder 20 that predecodes row address selection signals RA0 and RA1 in a memory circuit. (Id.)

(Ex. 1001, FIG. 2 (annotated); Ex. 1002, 『[210.)

In particular, AAPA discloses that figure 2 is "a circuit schematic diagram of other prior art row predecoder [20] and row decoder circuits [12] of the type conventionally used in memory circuits." (Ex. 1001, 3:47-49 (emphases added.) AAPA discloses that P0B is a precharge clock signal that places row predecoder circuit 20 in a precharge cycle or in a decoding cycle depending on the signal level of POB, i.e., HIGH or LOW. (Id., 5:26-30 (the '201 patent admitting that precharge clock signals P0B disclosed in the alleged invention and in the AAPA operate identically); Ex. 1002, $\mid 212$.$) Row address (RA) signals RA0 and RA1 are$ the "row address selection signals" provided to the "row predecoder circuit" 20. (Ex. 1001, 4:36-44 (the '201 patent disclosing "row address line 46 is identified as RA0...a second row address line (RA1) 47, which carries a second row address selection signal"), 5:4-5 ("row address (RA) signal"); Ex. 1002, $\uparrow 1212$. )

Because AAPA discloses operations of the predecoder 20 of figure 2 in memory circuits (e.g., receiving and predecoding row addresses RA0 and RA1 using a logic/NAND gate, and providing a decoded signal RAP through inverter 24 to row decoder 12 and other row decoders used in memory circuits), AAPA discloses a "method of predecoding an address selection signal in a memory circuit" as recited in claim 1. (Ex. 1002, $\mathbb{4} 213$; see also citations and analysis below for the remaining elements of this claim.)
b) providing a predecoder circuit comprising a dynamic

NAND gate having a first circuit element and a second circuit element;

AAPA in view of Yuh discloses or suggests this feature. (Ex. 1002, $49214-$ 222.) As explained below, the AAPA-Yuh combination provides a predecoder circuit that comprises a dynamic NAND gate having a first NMOS transistor ("first circuit element") and a second NMOS transistor ("second circuit element"). (Id.)

As shown in annotated figure 2 below, AAPA discloses a row predecoder 20 that includes static NAND gate 22 having a first NMOS transistor that receives precharge clock signal P0B ("first circuit element") and a second NMOS transistor that receives row address selection signal RA0 ("second circuit element"). (Ex. 1001, 2:2-5; Ex. 1002, $\boldsymbol{\text { | } 2 1 5 . ) ~}$

(Ex. 1001, FIG. 2 (annotated to show a static NAND gate 22 (blue) having a first and a second NMOS transistors (green)); Ex. 1002, $\mathbb{4}$ [215.)

Therefore, the AAPA discloses "providing a predecoder circuit comprising a dynamic[static] NAND gate having a first circuit element and a second circuit element." But a POSITA would have found it obvious to replace the static NAND gate of the AAPA with a dynamic NAND gate in view of Yuh. (Ex. 1002, $\boldsymbol{9} 216$. ) During prosecution of the '201 patent, Applicant acknowledged "that dynamic NAND gates were known in the prior art" but argued that the "use of a dynamic NAND gate in predecoder circuits to perform a predecoding function for memory circuits was not known or suggested by the prior art." (Ex. 1004 at 58, 75.) But
the use of dynamic NAND gates in predecoders in memory circuits was known at the time of the alleged invention, which is evidenced by, for example, Yuh. (Ex. 1002, $\boldsymbol{\text { ब }}$ ( $48-49,216-217$.

Like AAPA, Yuh discloses a predecoder circuit in a memory device. (Id., T217.) For example, Yuh discloses with reference to figure 3 (reproduced below) a "column predecoder [30] of the conventional synchronous graphic RAM." (Ex. 1005, 4:33-34.) As discussed above in Section IX.A.1(b), figure 3 of Yuh discloses a "dynamic NAND gate" in a predecoder circuit. (Supra Section IX.A.1(b).)

(Ex. 1005, FIG. 3 (annotated); Ex. 1002, $\mid 217$. )
As also discussed above in Section IX.A.1(b), dynamic circuits were known to have several advantages (e.g., higher speed, lower power consumption, lesser chip area) over static circuits. Therefore, a POSITA would have been motivated to replace the static NAND gate in AAPA figure 2 with a dynamic NAND gate because doing so would have resulted in, inter alia, reduced capacitance, faster speed, lower power consumption. (Ex. 1002, $\mathbb{4}$ 218; supra Section IX.A.1(b).) See Unwired Planet, 841 F.3d at 1003; KSR, 550 U.S. at 424. Additionally, as a dynamic NAND gate requires fewer numbers of transistors than a static NAND
gate, a POSITA would have been able to reduce the area occupied by the logic gate and thereby increase the density of the circuit components and number of bits that can be stored in a memory device. (Ex. 1002, 9218. )

Modifying the static NAND gate in the AAPA to be a dynamic NAND gate would have merely involved removing two of the PMOS transistors in the static NAND gate. (Ex. 1002, $9 \uparrow 1219-222$.) Such a removal would not have negatively affected the operation of the circuit of figure 2. (Id.) An exemplary and nonlimiting demonstrative showing the modification is set forth below. (Ex. 1002, -T219.)

## FIG. 2

PRIOR ART

(Ex. 1002, 『219.)
As shown in the demonstrative above, the modified AAPA-Yuh row predecoder discloses the claimed "providing a predecoder circuit comprising a dynamic NAND gate having a first circuit element and a second circuit element." (Ex. 1002, $9 \uparrow \mid 221-222$.
c) providing an inverter gate electrically coupled to said dynamic NAND gate and having an output terminal electrically coupled to a plurality of row decoder circuits for the memory circuit;

The combination of AAPA and Yuh discloses or suggests this feature. (Ex. 1002, [223.) As discussed above in Section IX.C.1(b), the AAPA-Yuh combination replaces the static NAND gate in the AAPA with a dynamic NAND gate. This replacement does not alter the remaining circuit configuration of the AAPA. That is, the combination retains inverter 24 that is electrically coupled to the NAND gate and is coupled to a plurality of row decoder circuits for the memory circuit. (Ex. 1002, $\mathbb{9} 223$; see demonstrative below.)


## plurality of row decoder circuits for the memory circuit

(Id., |223.)
Accordingly, the AAPA-Yuh combination discloses claim element $1[\mathrm{c}]$.
d) selectively enabling said first circuit element with a first
input signal comprising a self-timed one shot pulse signal indicative of an active memory bank for said memory circuit; and;

AAPA in view of Yuh and Fujioka discloses or suggests this feature. (Ex. 1002, 9¢| $224-232$.

First, the AAPA-Yuh combination discloses "selectively enabling said first circuit element with a first input signal." (Id., $\mid 224$.$) For example, the P0B signal$ selectively enables the first circuit element and is therefore a "first input signal." (Id.)

An exemplary and non-limiting demonstrative showing the AAPA-Yuh combination is set forth below. (Ex. 1002, $\uparrow 225$; supra Section IX.A.1(b).)

## FIG. 2

PRIOR ART

(Ex. 1002, $\mathbb{4} 225$.$) A POSITA would have understood that the P0B signal will turn$ on/off (i.e., "selectively enable[e]") the transistor annotated as the first circuit element. (Id, $\mathbb{T} 226$.$) For instance, when P0B is a high level, it will turn on the first$ circuit element, and when P0B is a low level, it will turn off the first circuit element. (Id.) Therefore, the AAPA-Yuh combination discloses "selectively enabling said first circuit element with a first input signal," as recited in claim element 1[d]. (Id.)

But the AAPA does not explicitly disclose that the POB signal is a "selftimed one shot pulse signal," or that the P0B signal is "indicative of an active memory bank for said memory circuit," as recited in claim element 1 [d]. However, as discussed above in Section IX.A.1(d), Yuh discloses that one of the input signals (EXTYAT) to the dynamic NAND gate in Yuh is a "self-timed one shot pulse signal." (Supra Section IX.A.1(d), explaining that the EXTYAT signal is a "self-timed one shot pulse signal.") Furthermore, as discussed above in Section IX.A.1(d), Fujioka discloses a bank select signal (bnk\#x) that enables the predecoder circuit of a selected bank (i.e., the bank select signal is "indicative of an active memory bank for said memory circuit"). (Supra Section IX.A.1(d); Ex. 1002 at ब $\mid 227$.

A POSITA would have looked to both Yuh and Fujioka because both disclose predecoders in a memory. (Ex. 1002, $\mathbb{9} 228$.$) Indeed, Fujioka is in the$ same technical field (i.e., memory devices) as AAPA and Yuh, disclosing operations and designs of predecoder circuits used in a multi-bank memory device. (Ex. 1010, Abstract; Ex. 1001, 1:47-51, 1:60-65 (admitting that conventional predecoders include multiple memory banks); Ex. 1002, $\mathbb{2 2 8 . )}$ For example, similar to AAPA and Yuh, Fujioka discloses using combinations of predecoderdecoder circuit structures for address decoding in memory devices. (Ex. 1010, 9:40-10:28; Ex. 1002, $\boldsymbol{T} 228$.

Having looked to Fujioka, a POSITA would have been motivated to implement the P0B signal in the AAPA-Yuh predecoder as a bank select signal like in Fujioka because doing so would have allowed the AAPA-Yuh predecoder circuit to be used in a multi-bank memory. (Ex. 1002, $\mathbb{4} 229$.$) A POSITA would$ have understood that a multi-bank memory provides greater throughput (number of memory accesses per unit time) as it enables interleaving accesses between multiple active banks, thereby enabling certain delays with respect to a particular bank to be hidden. (Id., 【229.) Fujioka discloses selectively activating a particular memory bank while the other memory banks in the memory remain inactive, where the predecoders in the selected bank are enabled while the predecoders in the unselected banks are disabled. (Ex. 1010, 2:4-20, 2:66-3:15 10:11-14; Ex. 1002, - $\mid 1229$.$) For instance, Fujioka discloses with reference to Figures 12$ and 13 a predecoder comprising a NAND gate that receives address signals and a "bank selection signal" that activates or deactivates the predecoder. (Ex. 1010, 9:4010:14; Ex. 1002, $\mathbb{9}$ 229.) Because only the predecoders for a particular bank are enabled, Fujioka can share the same address bus across all of the memory banks. (Ex. 1010, 5:50-58 (disclosing the "address buffers" and "bank selector" are "shared by four banks"); Ex. 1002, $\mathbb{4} 229$.

Based on the teachings of Fujioka, a POSITA would have been motivated to implement the P0B signal in the AAPA-Yuh combination as a bank-select signal
similar to the bnk\#x signal used to select a bank and enable/disable the predecoders in Fujioka. (Ex. 1002, [230.) Doing so would be consistent with the enable/disable functionality of the P0B signal while allowing the AAPA-Yuh predecoder to be used in a multi-bank memory in which the address bus is shared, thereby reducing overall chip area. (Id., $\mathbb{4} 230$; Ex. 1001, 1:47-51 (disclosing that conventional memory devices "require separate address busses for each memory bank...[which] requires a relatively large amount of chip area, which translates into increased chip size for the memory circuit"), 1:60-65 (disclosing that conventional memory devices do "not permit sharing of the row address bus" and "separate address busses must be used for each memory bank" and that " $[t]$ he additional devices and the additional address busses inherently increase the memory circuit chip size, which is a drawback").) See Unwired Planet, 841 F.3d at 1003; KSR, 550 U.S. at 424.

A POSITA would have recognized that the proposed modification would have involved a combination of known prior art elements, according to known methods, to yield predictable results (e.g., a row predecoder that otherwise works as described in the AAPA-Yuh combination having its P0B signal implemented as a bank select signal like that of Fujioka). (Ex. 1002, $\uparrow 231$.$) See KSR, 550$ U.S. at 416.

Furthermore, a POSITA would have been motivated to implement the P0B signal as a "self-timed one shot" bank select signal for reasons similar to those discussed above in Section IX.A.1(d). (See supra Section IX.A.1(d).) As discussed immediately above, it would have been obvious for a POSITA to implement the P0B signal in the AAPA-Yuh predecoder as a bank select signal like that disclosed in Fujioka such that the P0B signal in the AAPA-Yuh-Fujioka combination would be a bank select signal capable of use in a multi-bank memory. (Ex. 1002, $\mathbb{9}$ 232.) As discussed above in section IX.A.1(d) with respect to the Fujioka-Yuh combination, POSITA would have found it obvious to implement such a bank select signal in a multi-bank memory that includes predecoders having dynamic NAND gates as a self-timed one shot pulse signal like the EXTYAT signal disclosed in Yuh. (See supra Section IX.A.1(d).) Therefore, for reasons similar to those discussed above regarding using a self-timed one shot pulse signal as disclosed in Yuh as the bank select signal in Fujioka, a POSITA would have implemented the P0B bank select signal in the AAPA-Yuh-Fujioka combination as a self-timed one shot pulse signal similar to the EXTYAT signal disclosed in Yuh. (Id.; Ex. 1002, 『1232.)
e) selectively enabling said second circuit element with a second input signal indicative of a selected memory row address for said active memory bank.

The AAPA-Yuh-Fujioka combination discloses or suggests this feature. (Ex. 1002, $9 \uparrow 2233-235$.$) For example, as discussed above in Sections IX.C.1(a), (b)$ and as shown in the non-limiting demonstrative below, a NMOS transistor receives a row address signal RA0 in the AAPA-Yuh combination. (See supra Sections IX.C.1(a), (b).)

## FIG. 2 <br> PRIOR ART


(Ex. 1002, 『233.)
Also discussed above in Section IX.C.1(b), address signals, such as RA0, being applied to the gate of the NMOS transistor, can make the transistor either conductive or non-conductive. (See supra Section IX.C.1(b).) And depending on the memory cell that is selected, address signal RA0 can go HIGH or LOW to
enable or disable the NMOS transistor. (Ex. 1002, $\mathbb{q} 234$.$) Accordingly, the$ combination of AAPA and Yuh discloses the claimed "selectively enabling said second circuit element with a second input signal indicative of a selected memory row address." (Id.)

Furthermore, as discussed above in Section IX.C.1(d), a POSITA would have combined teachings of AAPA, Yuh, and Fujioka when implementing a multibank memory device. Accordingly, the prior combination also discloses selectively enabling said second circuit element with a second input signal "indicative of a selected memory row address for said active memory bank" because in such a multi-bank memory, the row address selection signal RA0 is provided to all banks (including the selected bank). (Ex. 1002, $\mathbb{T} 235$.

## 2. Claim 2

The combination of AAPA, Yuh, and Fujioka discloses or suggests this feature. (Ex. 1002, q\{1236-237.) For example, the AAPA-Yuh-Fujioka combination discloses with reference to the demonstrative below that row predecoder 20 includes a PMOS transistor ("precharge circuit"). (Id.)

## F1G.2 <br> PRIOR ART


(Ex. 1002, 9236 ; Ex. 1001, FIG. 2 (excerpt).) The PMOS transistor is a precharge circuit because it pulls RAPB to a high level when the PMOS transistor is on. (Ex. 1002, $\mid 236$.

Furthermore, signal P0B is a "precharge control signal" because it turns the PMOS transistor ("precharge circuit") on or off. (Id., $\{237$.$) Therefore, the$ AAPA-Yuh-Fujioka combination discloses "generating a precharge control signal"
because it discloses generating signal P0B. (Id.) The combination also discloses "selectively enabling said precharge circuit with said precharge control signal" because it discloses turning the PMOS transistor on/off using the signal P0B. (Id.)

## 3. Claim 3

The combination of AAPA, Yuh, and Fujioka discloses or suggests this feature. (Ex. 1002, $\boldsymbol{q} \uparrow 238-239$.$) A POSITA would have understood that when$ signal P0B is LOW, the PMOS transistor ("precharge circuit") is enabled, but the same signal level (LOW) disables the NMOS transistor ("first circuit element"), rendering the NMOS transistor non-conductive. (Id., $\mathbb{q} 238$.)

## FIG. 2

PRIOR ART

(Ex. 1002, 『238.)
Thus, the PMOS transistor ("precharge circuit") and the NMOS transistor ("first circuit element") cannot be enabled at the same time. That is, the PMOS transistor ("precharge circuit") can be enabled only when the NMOS transistor ("first circuit element") is disabled. (Id., 【239.) Accordingly, the AAPA-YuhFujioka combination discloses "providing said predecoder circuit with a precharge circuit, and selectively enabling said precharge circuit with said first input signal." (Id.)

## 4. Claim 4

The combination of AAPA, Yuh, and Fujioka discloses or suggests this feature. (Ex. 1002, 9240 .) As discussed above with respect to claim 2, the PMOS transistor is a "precharge circuit" that is selectively enabled by signal P0B ("first input signal"). (Supra Section IX.C.2.)

## 5. Claim 5

The combination of AAPA, Yuh, and Fujioka discloses or suggests this feature. (Ex. 1002, 9241.$)$ As discussed above with respect to claim 3, the PMOS transistor is selectively enabled by the P0B signal ("selectively enabled by said first input signal") and when that happens, the first circuit element is turned off ("said first circuit element is not enabled by said first input signal"). (Supra Section IX.A.3.)

## X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims
1-6 of the ' 201 patent based on the grounds specified in this petition.
Respectfully submitted,
Dated: March 5, 2019
By:/Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

## CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § $42.24(\mathrm{~b})(1)$, the undersigned certifies that the foregoing Petition for Inter Partes Review of U.S. Patent No. 6,597,201 contains, as measured by the word-processing system used to prepare this paper, 13,931 words. This word count excludes the Table of Contents, Table of Authorities, List of Exhibits, Certificate of Compliance, and Certificate of Service.

Respectfully submitted,

Dated: March 5, 2019
By:/Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

## CERTIFICATE OF SERVICE

I hereby certify that on March 5,2019 , I caused a true and correct copy of the foregoing Petition for Inter Partes Review of U.S. Patent No. 6,597,201 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

Cook Alex McFarron Manzo Cummings \& Mehler Ltd Suite 2850<br>200 West Adams Street<br>Chicago IL 60606

A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel listed below:

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Counsel for Petitioner


[^0]:    ${ }^{2}$ Petitioner submits the declaration of Dr. R. Jacob Baker (Ex. 1002), an expert in the field of the '201 patent. (Ex. 1002 at $9915-15$; Ex. 1003.)

[^1]:    ${ }^{3}$ A typographical error in the '201 patent omits a significant portion of the quoted text from the text of the ' 201 patent. The omitted text can be found in the ' 494 application. (Ex. 1004 at 14 ('494 application at 6:28-31); Ex. 1002 at 942 , n. 5.)

[^2]:    ${ }^{4}$ Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '201 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

[^3]:    ${ }^{6}$ To the extent Patent Owner contends that the dynamic NAND gate only includes the NMOS transistors included in the pull-down chain corresponding to the dynamic NAND structure, then transistors N30, N31, N32, and N33 would constitute the "dynamic NAND" gate. (Ex. 1002, 992 n.8.)

[^4]:    precharge circuit with said first input signal."; see also id. at FIG. 8 (where the same signal 64 is input to transistor 58 ("first circuit element") and transistor 54 ("precharge circuit").)

