UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC,
Patent Owner

Case No.: To Be Assigned
U.S. Patent No. 7,739,487

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,739,487

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U.S. Patent and Trademark Office
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TABLE OF CONTENTS

Table of Authorities

Cases

Statutes and Codes

Rules and Regulations

EXHIBIT LIST

Exhibit No.	***Description***
1001	U.S. Patent No. 7,739,487 to Mylly *et al*. (the "'487 Patent")
1002	File History for U.S. Patent No. 7,739,487 to Mylly *et al*.
1003	Declaration of Dr. R. Jacob Baker
1004	Curriculum Vitae of Dr. R. Jacob Baker
1005	U.S. Patent. No. 6,279,114 to Toombs *et al*. ("Toombs")
1006	U.S. Patent. No. 7,058,779 to McClain
1007	U.S. Patent No. 7,012,845 to Kozakai *et al*. ("Kozakai")
1008	U.S. Patent No. 7,188,265 to Kurakata *et al*. ("Kurakata")
1009	Information Disclosure Statement ("Toombs IDS") and MultiMediaCard System Specification Version 1.4 ("MMC 1.4"), File History of U.S. Patent No. 6,279,114 to Toombs et al. ("Toombs File History")
1010	U.S. Patent No. 7,234,049 to Choi *et al.* ("Choi")
1011	U.S. Patent No. 5,535,357 to Moran *et al.* ("Moran")
1012	OneNAND Specification ("OneNAND")
1013	M-Systems DiskOnChip G3 Data Sheet ("MDOC")
1014	U.S. Patent No. 5,694,600 to Khenson *et al.* ("Khenson")
1015	U.S. Patent No. 7,555,568 to Huang

Exhibit No.	***Description***
1016	U.S. Patent No. 7,082,525 to Hutton *et al.* ("Hutton")
1017	U.S. Patent Publication No. 2004/0266480 to Hjelt *et al.* ("Hjelt")
1018	U.S. Patent No. 7,049,652 to Mokhlesi *et al*. ("Mokhlesi")
1019	U.S. Patent No. 7,136,994 to Zimmer *et al*. ("Zimmer")
1020	U.S. Patent No. 7,136,951 to Deng *et al.* ("Deng")
1021	U.S. Patent No. 7,631,245 to Lasser
1022	U.S. Patent No. 6,377,511 to Okuda *et al*. ("Okuda")
1023	U.S. Patent No. 5,689,459 to Chang *et al.* ("Chang")
1024	Third Joint Claim Construction and Prehearing Statement (N.D. Cal. Patent L.R. 4-3), filed in the related matter on Nov. 16, 2018
1025	Microsoft Computer Dictionary at 94, 150, 159, 310, 404, 480, 498, 515 (5th ed. 2002)
1026	U.S. Patent No. 6,842,818 to Okamoto *et al*. ("Okamoto")
1027	Comprehensive Dictionary of Electrical Engineering (Phillip A. Lapalante et al., 1st ed. 1999)

I. INTRODUCTION AND STATEMENT OF RELIEF REQUESTED (37 C.F.R. §42.22(a))

Kingston Technology Company, Inc. ("Petitioner" or "Kingston") hereby petitions to institute an *inter partes* review of Claims 6, 7, 13, 20, 21, 26, 42, and 52 (the "Challenged Claims") of U.S. Patent No. 7,739,487 (the "'487 Patent") to Mylly (Ex. 1001), and cancel these claims as unpatentable. The prior art presented in this Petition—U.S. Patent. No. 6,279,114 (Ex. 1005, "Toombs"), U.S. Patent. No. 7,058,779 (Ex. 1006, "McClain"), U.S. Patent No. 7,012,845 (Ex. 1007, "Kozakai"), and U.S. Patent No. 7,188,265 (Ex. 1008, "Kurakata") —were not considered during prosecution of the '487 Patent.

As discussed in detail below, Toombs and McClain render obvious Claims 6, 7, 20, and 21 under 35 U.S.C. §103; Toombs, McClain, and Kozakai render obvious Claims 6, 7, 20, and 21 under 35 U.S.C. §103; and Toombs, McClain, and Kurakata render obvious Claims 13, 26, 42, and 52 under 35 U.S.C. §103. Thus, there is a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim, and Petitioner respectfully requests that the Board institute a trial for *inter partes* review and cancel the Challenged Claims as unpatentable.

II. MANDATORY NOTICES

A. Real Party-In-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Kingston Technology Company, Inc., is a real party-in-interest. Petitioner's parent company, Kingston Technology Corporation ("Kingston Holding"), is a holding company without any employees or operations. However, because Kingston Holding is the sole owner of Petitioner and shares some directors, Petitioner identifies Kingston Holding as an additional real party-in-interest.

B. Identification of Related Matters (37 C.F.R. §42.8(b)(2))

Patent Owner Memory Technologies, LLC ("MTL") has asserted Claims 6, 7, 13, 20, 21, 26, 42, and 52 of the '487 Patent, as well as claims from U.S. Patent Nos. RE45,486 (the "RE '486 Patent"), RE45,542 (the "RE '542 Patent"), 7,565,469 (the "'469 Patent"), 7,827,370 (the "'370 Patent"), 8,307,180 (the "'180 Patent"), 9,063,850 (the "'850 Patent"), and 9,367,486 (the "'486 Patent") against Kingston in a co-pending litigation, *Memory Technologies, LLC v. Kingston Technology Co., Inc*., 8:18-cv-00171 (C.D. Cal.). MTL's original Complaint was filed on January 31, 2018, and served, at the earliest, on February 1, 2018.

In addition to this Petition, Kingston will be filing petitions for *inter partes* review of the other seven patents that MTL has asserted against it.

C. Counsel and Service Information (37 C.F.R. §§42.8(b)(3) & (b)(4))

Petitioner designates the following Lead and Backup Counsel. Concurrently filed with this Petition is a Power of Attorney for appointing the following Lead and Backup Counsel, per 37 C.F.R. §42.10(b). Service via hand-delivery may be made at the postal mailing addresses below. Petitioner consents to electronic service by e-mail at the following address: **kingston-487ipr@pillsburylaw.com**.

Lead Counsel	Back-Up Counsel
Robert C.F. Pérez (Reg. No. 39,328) PILLSBURY WINTHROP SHAW PITTMAN LLP 1650 Tysons Boulevard, 14th Floor McLean, VA 22101 Telephone: 703.770.7900 Facsimile: 703.770.7901	**Christopher Kao**, Kingston's counsel in the co-pending litigation (*Pro hac vice* motion to be filed) **Brock S. Weber**, Kingston's counsel in the co-pending litigation (*Pro hac vice* motion to be filed) PILLSBURY WINTHROP SHAW PITTMAN LLP Four Embarcadero Center, 22nd Floor San Francisco, CA 94111 Telephone: 415.983.1000 Facsimile: 415.983.1200

F. Payment of fees (37 C.F.R. §42.103)

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 033975 for the petition fee and for any other required fees.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Identification of Challenge

Pursuant to 37 C.F.R. §42.104(b), Petitioner shows the following grounds:

- Claims 6, 7, 20, and 21 are rendered obvious by Toombs (Ex. 1005) and McClain (Ex. 1006) under 35 U.S.C. §103;
- Claims 6, 7, 20, and 21 are rendered obvious by Toombs (Ex. 1005), McClain (Ex. 1006), and Kozakai (Ex. 1007) under 35 U.S.C. §103;
- Claims 13, 26, 42, and 52 are rendered obvious by Toombs (Ex. 1005), McClain (Ex. 1006), and Kurakata (Ex. 1008) under 35 U.S.C. §103.

The '487 Patent was filed on January 17, 2006 and does not claim priority to any foreign or U.S. patent application.

Toombs was filed in the United States on November 4, 1998 and issued on August 21, 2001. Thus, Toombs is prior art under at least 35 U.S.C. §§102(a), (b), and (e).

McClain was filed in the United States on March 5, 2002 and issued on June 6, 2006. Thus, McClain is prior art under at least 35 U.S.C. §102 (e).

Kozakai has an earliest filing date in the United States of September 23, 2003, published on June 30, 2005, and issued on March 14, 2006. Thus, Kozakai is prior art under at least 35 U.S.C. §§102(a) and (e).

Kurakata was filed in the United States on November 20, 2003, published on June 17, 2004, and issued on March 6, 2007. Thus, Kurakata is prior art under at least 35 U.S.C. §§102(a), (b), and (e).

The Declaration of Jake Baker, Ph.D., filed herewith (Ex. 1003), supports the challenge in this Petition that the Challenged Claims of the '487 Patent are invalid.

IV. BACKGROUND OF THE TECHNOLOGY

The '487 Patent is directed to booting a host device from a peripheral device. Ex. 1001, Abstract; Ex. 1003, ¶83. This technology was well-developed by the time the '487 Patent was filed in January 2006. Below is an overview of the state of the art prior to the filing date of the '487 Patent.

A. MMC Cards

The MultiMediaCard System Specification Version 1.4 ("MMC 1.4") defines specifications for MMC cards and the communications between MMC cards and their hosts. *See generally* Ex. 1009. MMC cards, like SD cards that followed them, are removable memory cards that can be used with computers, phones, and other devices. Ex. 1003, ¶74.

MMC 1.4 discloses the power-up process to turn on an MMC card and initialize it for use. Ex. 1009, Fig. 39 (shown below).

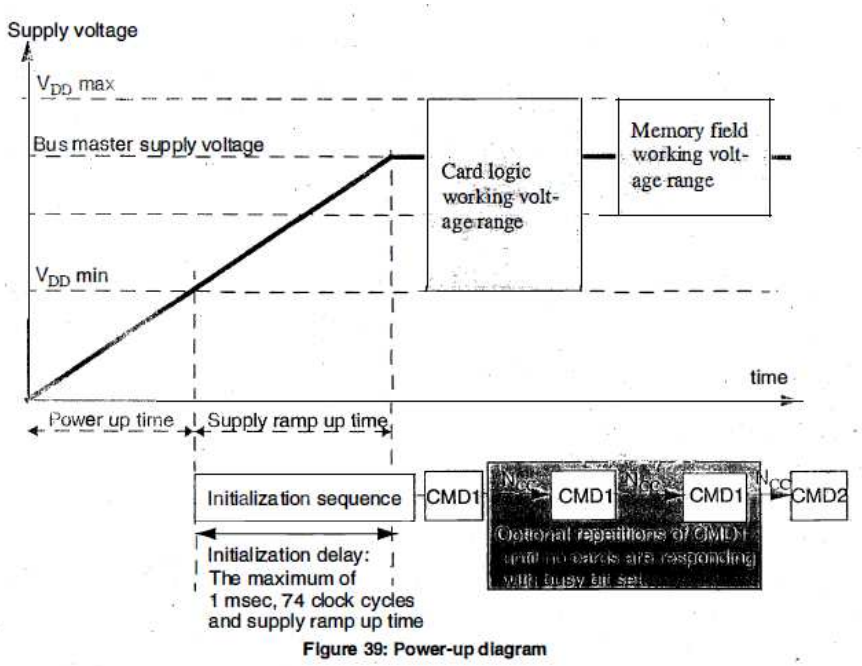


Figure 39: Power-up diagram

The power-up procedure includes a power-up time to ramp the supply voltage to the minimum value (*i.e.*, V_{DD} min) and a supply ramp up time to ramp the supply voltage to the bus master supply voltage level. *Id*. After the power-up time, "the host starts the clock and sends the initializing sequence on the CMD line." *Id.,* 64. The initialization sequence can be a "contiguous stream of logical '1's" and the sequence length is the maximum of "1msec, 74 clocks or the supply-ramp-up-time." *Id.,* 64-65. After the initialization sequence, the host or bus master transmits CMD1, which "is a special synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence." *Id.,* 64. Thus, the power-up procedure includes the power up

time, supply ramp up time, and synchronization time, as illustrated above in Figure 39. Ex. 1003, ¶74.

In addition to the power-up procedure, MMC 1.4 also discloses the termination of the command and data lines.

Parameter	Symbol	Min	Max.	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	100	kΩ	to prevent bus floating
Pull-up resistance for DAT	R_{DAT}	50	100	kΩ	to prevent bus floating
Bus signal line capacitance	C_L		250	pF	$f_{PP} \leq 5$ MHz, 30 cards
Bus signal line capacitance	C_L		100	pF	$f_{PP} \leq 20$ MHz, 10 cards
Single card capacitance	C_{CARD}		7	pF	
Maximum signal line inductance			16	nH	$f_{PP} \leq 20$ MHz

Ex. 1009, 67 (specifying bus signal line load). MMC 1.4 discloses resistors with a range of pull-up resistance for the command and data lines "to prevent bus floating." *Id.* The importance of the pull-up resistors is described in the context of the various timing diagrams disclosed in MMC 1.4, where the command and data terminals are pulled HIGH by the pull-up resistors when either terminal is not actively driven to a value. *See id.,* 48, 62 (describing high impedance (HIGH-Z) value); *see also* Ex. 1003, ¶75.

MMC 1.4 was included in an Information Disclosure Statement filed on November 4, 1998 during prosecution of Toombs ("Ex. 1005"). Ex. 1009, 1, 2.

Toombs issued on August 21, 2001. Ex. 1005. Accordingly, MMC 1.4 was publicly available at least as of August 21, 2001.

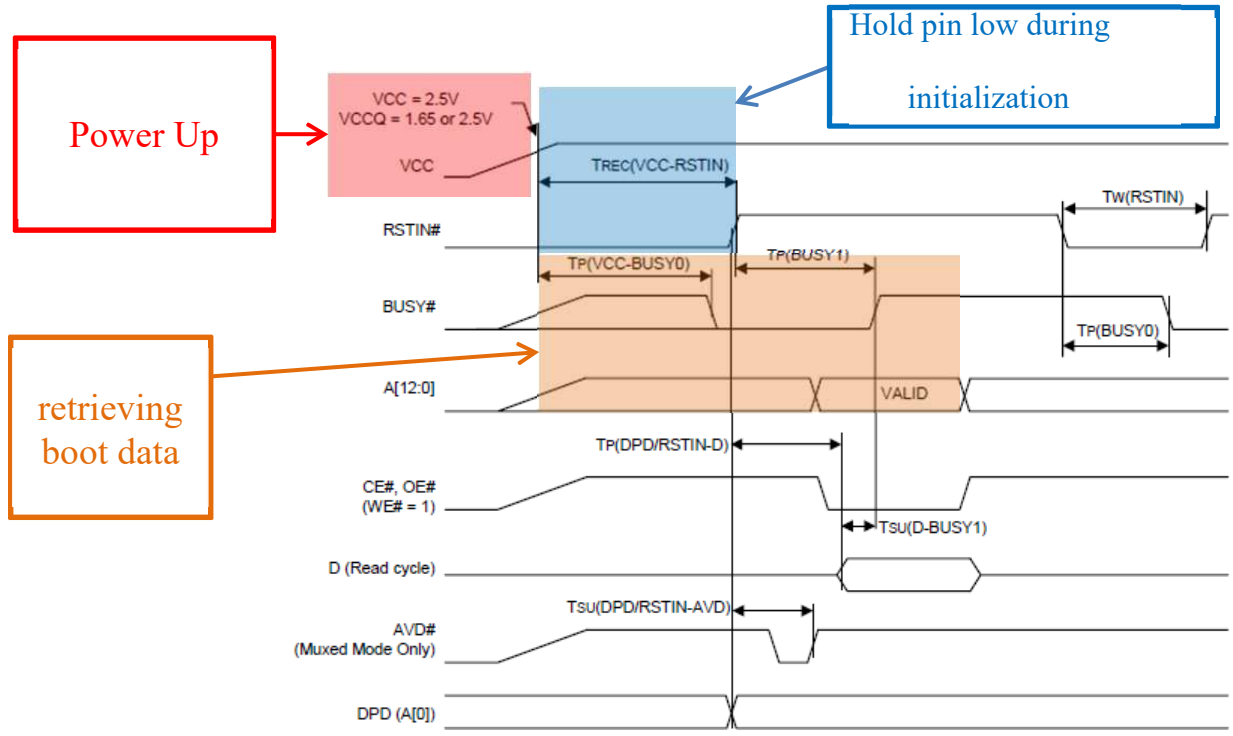
B. Booting from Flash Memory Devices

The advantages of non-volatile flash memory were well-known at the time of the '487 Patent. Ex. 1003, ¶77; *see* Ex. 1010, 1:33-38 (explaining that NAND flash memory is "easy to realize, has a large capacity, and is cost- effective," as well as "easy to fabricate and has a good integrity"). Two other types of boot devices, magnetic hard disks and floppy disks, were known to be "large and somewhat susceptible to mechanical failure." Ex. 1011, 1:38-40. In contrast, flash memory devices are "smaller, more rugged and consume less power." *Id.,* 1:48-50. Because of its advantages (*i.e.*, "fast access, low power consumption, high reliability, and relatively low cost"), flash memory could be used to replace hard disk drives. *See id.,* 1:55-58, 1:67-2:12. Accordingly, flash memory was used to boot computing devices. *See* Ex. 1011, 2:14-18 (replacing "the functionality of the BIOS, an operating system and a hard disk" with flash memory).

One example of a bootable flash memory was Samsung's OneNAND flash memory, which enabled boot from system power-up. Ex. 1012, 58, 103; *see also id.,* 5 ("Samsung offers a variety of Flash solutions including NAND Flash, OneNAND™ and NOR Flash. Samsung offers Flash products both component and

a variety of card formats including RS-MMC, MMC, CompactFlash, and SmartMedia."). Booting from OneNAND involved copying boot code from the flash memory into a buffer in response to power on reset and then reading the boot code from the buffer. *Id.,* 103; *see* Ex. 1010, 5:59-65.

Another example of a bootable flash memory was M-Systems' DiskOnChip ("DOC" or "MDOC"), which enabled boot in response to a signal received on a pin of the flash memory. Ex. 1013, 10, 36. MDOC included a boot block with an eXecute In Place (XIP) capability to enable the flash memory to be the only non-volatile memory in a system. *Id.,* 10. As shown in Figure 33, below, a host would power up the flash memory (highlighted in red) and assert reset by holding the RSTIN# pin in a low voltage state at power up to boot from the flash memory device (highlighted in blue):



Id., 90-91, Fig. 33 (annotated), Table 22. Then, the host would enable boot mode by de-asserting reset (*i.e.*, RSTIN# transitions from low to high). *Id.* After a delay, the flash memory device would download boot data from the flash memory to the boot block. *Id.* The host, in turn, would read the data from the boot block to continue the boot process (highlighted in orange). *Id.*

Thus, it was known at the time of the '487 Patent that a host could provide a boot signal to a flash memory by holding a pin of the memory in a low voltage state for a predefined period of time. Ex. 1003, ¶79.

C. Booting from Removable Flash Memory Devices

At the time of the ’487 Patent, it was also well-known that a computer could boot from a removable device. *See, e.g.*, Ex. 1014, 1:6-10. In addition to computers that could boot from removable devices, it was further known at the time of the ’487 Patent that a computer could boot from a removable flash memory device. *See, e.g.*, Ex. 1015, 16:11-21; *see infra*, Section X (Combination of Toombs and McClain).

For example, NAND flash memory devices, such as MMC cards, were used to reduce the time to boot computing devices, such as cellular phones. Ex. 1016, 3:49-51, 4:44-62 (describing MMC and SD cards as exemplary devices to be used for boot without first copying the boot data to RAM); *see also* Ex. 1003, ¶111. In addition, flash memory has several advantages over other dedicated storage devices, such as read-only memory (ROM). *Id.,* 3:34-48.

As another example, Universal Serial Bus (USB) drives containing flash memory could be plugged into a computer, which could detect the presence of the drive and then boot via the USB interface to the drive. *See* Ex. 1015, 16:11-21. Thus, it was known at the time of the ’487 Patent that a computer could boot from a removable flash memory device. Ex. 1003, ¶81.

As described in the prior art, and in the background of the '487 Patent, an MMC bus could be used to communicate with a flash memory device. Ex. 1017, ¶0060, Fig. 11; *see also* Ex. 1001, 1:20-22 ("The invention introduces a booting mechanism also to a formerly known serial protocol memory card interface (MMC IF)."). "MMC cards involve[] the transfer of data using a minimum number of signals." Ex. 1017, ¶0060. For example, Figure 11, below, shows an MMC interface for an MMC flash memory device:

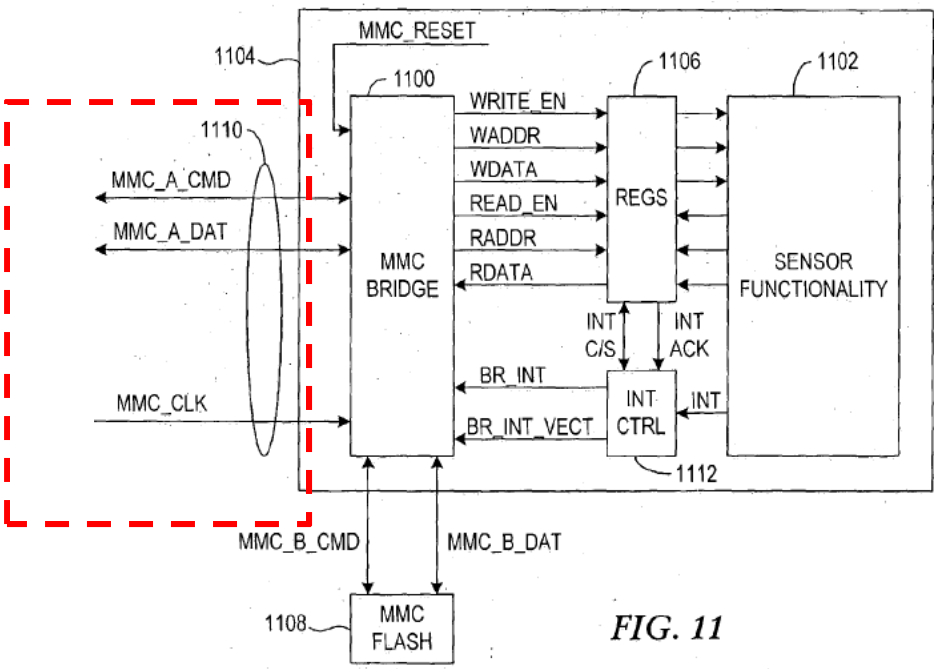


FIG. 11

Ex. 1017, Fig. 11 (emphasis added).

As shown above, MMC interface 1110 includes command, data, and clock lines for communication between the master (*i.e.*, host device) and the MMC card. *Id.,* Table 1, Fig. 11 (depicting an MMC interface with MMC_A_CMD,

MMC_A_DAT, and MMC_CLK lines). Both the command and data lines are bidirectional channels that operate in push-pull mode, "where, for example, a complementary pair of transistors is used to actively drive the interface level to a logic high or logic low." *Id.,* ¶0060. Bidirectional communication for the command line, for example, enables its use for both "card initialization and data transfer commands." *Id.*

Thus, it was known at the time of the '487 Patent that an MMC interface with only three lines (*i.e.*, command, data, and clock) could be used for communication to a flash memory device. Ex. 1003, ¶80.

V. OVERVIEW OF THE '487 PATENT

The '487 Patent relates to booting a host from a peripheral device, for example, a memory device. Ex. 1001, Abstract and 1:9-24. The memory device in the '487 Patent is a Secure Digital (SD) card or Multi Media Card (MMC). *Id*. The memory device and the host of the '487 Patent are connected via an MMC/SD interface, which includes power terminals, a data bus with data bus terminals, a clock line with a clock terminal, and a command line with a command terminal. *Id*., 2:28-40, Fig. 5 (illustrated below). As illustrated in Figure 5 below, the host includes a CPU and a controller and the memory device includes a controller and plurality of memory. *Id.*, Fig. 5.

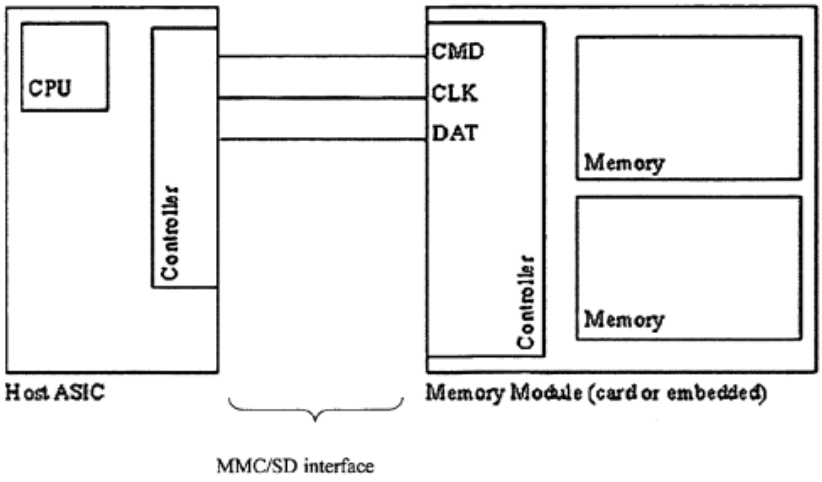


FIG. 5

The background of the '487 Patent acknowledges that "[b]oot definitions for existing mass memory components having a different electrical interface are already known." *Id*., 1:31-34. Each of these memory devices used "some signal state (e.g. separate pin reserved for booting) during certain stage of power up to indicate to the memory component that it should fetch the first sector (typically 512 B) of data to the IO buffers." *Id*., 1:34-38, 1:52-56.

The '487 Patent further explains that for MMC/SD devices, which do not have a separate pin for booting, fetching of first (sector) data during boot up of a host device required (i) initializing the card, (ii) reading/writing the registers, and (iii) performing a normal read access to a known address. *Id*., 2:1-11. The '487 Patent purports to achieve broader usability of MMC/SD devices without the use of an additional pin to signal boot by holding the CMD pin low for a duration or by

sending a command with an argument for boot using the CMD pin. *Id*., 2:16-25, 3:3-10, 3:63-4:30. Accordingly, the '487 Patent explains that the capabilities of existing MMC and SD cards can be extended without changing too many properties of the memory cards (*i.e*., without addition an additional pin to the MMC/SD interface). *Id*., 2:22-25, 17:23-26.

Figures 1 and 3 of the '487 Patent, below, illustrate the different booting mechanisms (*i.e*., by holding the CMD pin low for a duration and by sending a command with an argument for boot using the CMD pin). *Id*., Figs. 1, 3.

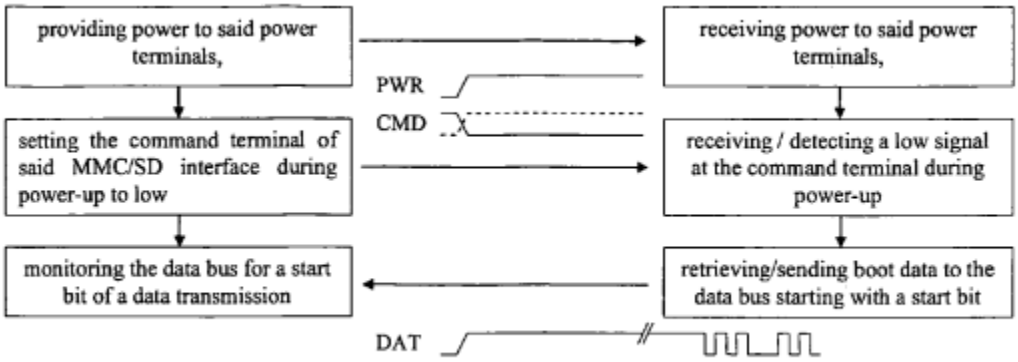


FIG. 1

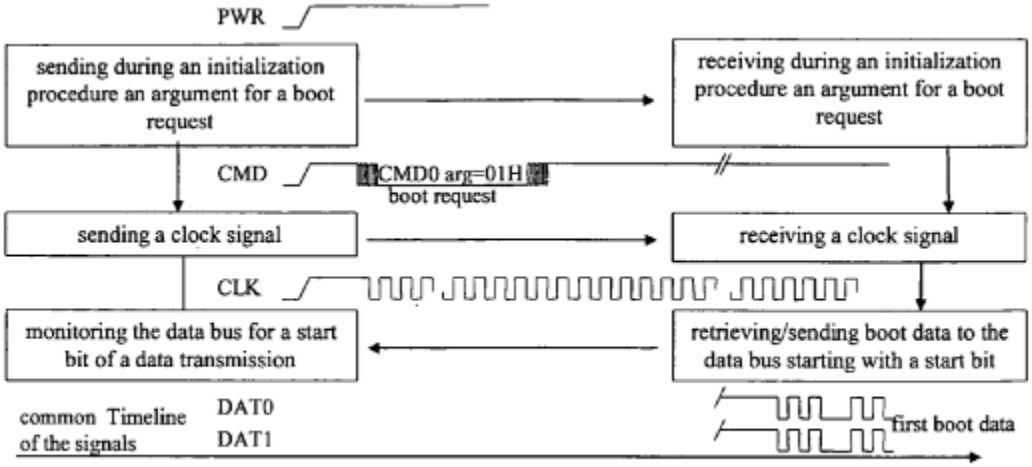


FIG. 3

As illustrated in Figure 1, above, a low signal is received at the command terminal during power up and then boot data is retrieved and sent via the data bus starting with a start bit. *Id*., 3:3-10, 3:63-4:30, Fig. 1. Further, as illustrated in Figure 3 above, an argument for a boot request is received during an initialization procedure, a clock signal is received at a clock terminal, and then boot data is retrieved and sent via the data bus starting with a start bit. *Id*. The host device part of the flowchart is depicted at the left side of Figures 1 and 3 while the part of the flowchart depicted on the right side of Figures 1 and 3 refers to actions or processes performed by or in the memory device. *Id*., 14:23-27.

VI. SUMMARY OF THE PROSECUTION HISTORY

The '487 Patent issued from U.S. Patent Application No. 11/333,799 (the '799 Application) filed on January 17, 2006. Ex. 1001.

The USPTO issued a Non-Final Office Action dated November 14, 2008 in which some of the originally-presented claims were rejected under 35 U.S.C. §101 and the other claims were indicated as being allowed. Ex. 1002, 89-92. A response with claims amendments was filed in response to the Office Action of November 14, 2008, which resulted in another Non-Final Office Action being issued by the USPTO. *Id*., 99-113, 119-122. In this Office Action, some of the claims were rejected under 35 U.S.C. §102 as being anticipated by Gillet (U.S. 2005/0132116) and other claims were indicated as being objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. *Id*., 119-122.

On July 14, 2009, the Applicant filed a response arguing that the Office Action dated April 15, 2009 was improper. *Id*., 128-146. The Applicant asserted that Gillet does not disclose "setting the command terminal of said MMC/SD interface during power-up to low." *Id*., 142. The Applicant acknowledged that Gillet discloses "setting one of the data bus lines (contacts 1, 8-13 / DAT1-DAT7) to a low state at a later, already powered up, state by the MMC card." *Id*. The Applicant explained that "Gillet relies upon a different device using a different line during a different period of time than the claimed invention." *Id*., 144.

A Notice of Allowance eventually issued on March 23, 2010 and the '799 Application issued as the '487 Patent. *Id.*, 293-296; Ex 1001.

On July 23, 2010, a request for a certificate of correction was filed by the Applicant to correct the title to recite "an MMC/SD Device Method a Host Device May Be Booted From." Ex. 1002, 313-314. The Applicant further sent a letter on August 31, 2010 providing a superseding request for a certificate of correction to further correct the title at Column 1, line 5 and on the Title Page, Item (54). *Id*., 318-319. On September 28, 2010, the superseding Certificate of Correction was issued. *Id*., 320.

The Toombs, McClain, Kozakai, and Kurakata references relied upon in this Petition were not considered during prosecution.

VII. CLAIM CONSTRUCTION

The Patent Office has adopted a rule by which claims are construed in accordance with "the standard used in federal courts, in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), which is articulated in *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005)." 83 FR 51340. Under this standard, claim construction begins with the language of the claims. *Phillips*, 415 F.3d at 1312-14. The "words of a claim are generally given their ordinary and customary meaning," which is

"the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id*., 1312-13. The specification is "the single best guide to the meaning of a disputed term and . . . acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication." *Id*., 1321 (internal quotation marks omitted). The prosecution history is another source of intrinsic evidence. *Id*., 1317.

All claim terms of challenged claims of the '487 Patent have been accorded their plain and ordinary meaning as understood by person of ordinary skill in the art and consistent with the intrinsic record. Petitioner's interpretation of the claim terms in the '487 Patent is further explained for each claim limitation in relation to the prior art discussed in the proposed grounds for invalidity, below, in Grounds 1-3.

Under the *Phillips* standard and for clarity, Petitioner provides the following specific construction.[1]

[1] Petitioner reserves the right to address any claim construction positions taken by the Patent Owner in its Preliminary Response, if any, including under 37 C.F.R. §42.108(c). Petitioner further reserves its ability to show that claims of the

A. "data frame"

Claims 6 and 20 recite a "data frame." Petitioner proposes construing this term as "data transmission" consistent with specification of the '487 Patent. Specifically, the specification of the '487 Patent clarifies that "data transmission" disclosed in Toombs (Ex. 1005) and the "data frame" recited in Claims 6 and 20 are analogous. *See* Ex. 1001, 4:39-40 ("monitoring the data bus terminals for a start bit of a data transmission/data frame"). Accordingly, Petitioner proposes construing the term "data frame" as "data transmission." Ex. 1003, 92.

VIII. A PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSA") with respect to the technology described in the '487 Patent would be a person with a bachelor's degree in electrical engineering or a closely related field, and two to three years of experience in the field of memory system design. Ex. 1003, ¶68. However, a higher level of education could make up for less experience, and vice versa. *Id*.

'487 Patent are invalid under 35 U.S.C. §112 in the co-pending litigation, despite offering explicit and implicit claim constructions herein.

IX. DESCRIPTION OF THE PRIOR ART

A. Toombs (Ex. 1005)

Toombs, entitled "Voltage Negotiation In A Single Host Multiple Cards System," describes a memory card with an MMC interface. Ex. 1005, 6:18-38, Fig. 14. Specifically, Toombs discloses an MMC bus that connects an MMC card to an MMC host, where the MMC bus includes the following MMC bus lines: power supply, communications (including both CMD and DAT), and clock. Ex. 1005, 6:60-65, 7:32-34. The data line (i.e., DAT) and the command line (i.e., CMD) are bidirectional communication lines and the clock line is provided for the MMC host to synchronize data transfer across the MMC bus. Ex. 1005, 7:41-47.

B. McClain (Ex. 1006)

McClain, entitled "Computer System Initialization Via Boot Code Stored In A Non-Volatile Memory Having An Interface Compatible With Synchronous Dynamic Random Access Memory," describes a non-volatile memory that has an SDRAM style memory interface and that is used to provide initialization (boot) code to a computer system. Ex. 1006, 2:7-10. Specifically, McClain describes booting from a non-volatile, flash memory using a single pin without requiring any additional control signals beyond those defined by a standard SDRAM interface. Ex. 1006, 3:34-37, 4:52-64.

C. Kozakai (Ex. 1007)

Kozakai, entitled "Nonvolatile Memory With Control Circuit Adapted To Distinguish Between Command Signal Interface Specifications And Having An Error Correction Function," describes a non-volatile memory, which includes a host interface section to perform inputting and outputting of signals to and from a controller, such as an external host CPU. Ex. 1007, 4:26-31. Specifically, Kozakai discloses that a "flash memory is enabled to function as a boot device by storing at the leading address ("0") of the memory array of the flash memory the program to be executed first time at the time of actuating the system." Ex. 1007, 19:21-24. Further, Kozakai describes that the data from the leading address ("0") of the memory array of the flash memory is read out in response to a low signal received at an external terminal (for example, PRE) of the flash memory from an external device, such as a host CPU, during power-up. Ex. 1007, 18:59-61, 19:1-9, 19:14-15, 19:40-46.

D. Kurakata (Ex. 1008)

Kurakata, entitled "Method Of Recognizing A Card Using A Select Signal During A Determination Mode And Switching From Low to High Resistance After The Determination," describes an MMC card that includes a plurality of connector terminals P0-P6 (corresponding to clock, power, data, and command terminals).

Ex. 1008, Fig. 1. Further, Kurakata discloses that the MMC card receives, during an initialization procedure of the MMC card, an initialization command CMD0 including an 8-bit command index, a 32-bit argument, and an 8-bit CRC code. Ex. 1008, 6:59-63.

X. GROUND 1: CLAIMS 6, 7, 20, AND 21 ARE RENDERED OBVIOUS BY *TOOMBS* AND *MCCLAIN*.

As shown below, Toombs and McClain render Claims 6, 7, 20, and 21 of the '487 Patent obvious under 35 U.S.C. §103. *See also* Ex. 1003, ¶¶108-145.

A POSA would have been motivated to combine Toombs and McClain. Toombs and McClain disclose a non-volatile, flash memory device. Ex. 1005, 1:30-32; Ex. 1006, 2:25-34. Further, Toombs discloses a MultiMediaCard (MMC) bus system that connects a flash memory device (for example, an MMC card) to an MMC host. Ex. 1005, 6:61-65. An MMC interface for the MMC card includes command, clock, and data lines that that transmit information between command, clock, and data terminals of the MMC card and the MMC host. Ex. 1005, 7:14-22, 7:41-47, 6:18-38, Fig. 14. Toombs' MMC interface also includes power supply lines Vss1, Vss2, and Vdd. Ex. 1005, 7:35-38, Fig. 14. Collectively, the power supply lines and the command, clock, and data lines make up the MMC bus lines. Ex. 1005, 7:32-34. Toombs also discloses the benefit of using a standard interface,

such as the MMC bus, to connect hosts to cards. *See id*., 6:11-16 ("connecting the host and the cards by implementing a standard interface protocol").

Toombs discloses various systems that include a non-volatile, flash memory with an MMC interface. Ex. 1005, 1:9-26. Those systems have experienced "continuous development" resulting in unlimited combinations, such as electronic toys, organizers, PDAs, cameras, smart phones, digital recorders, pagers, etc. *Id*. Figure 1 of Toombs shows various configurations ranging from extremely low-cost solutions up to high-cost solutions using personal computers with x86 processors:

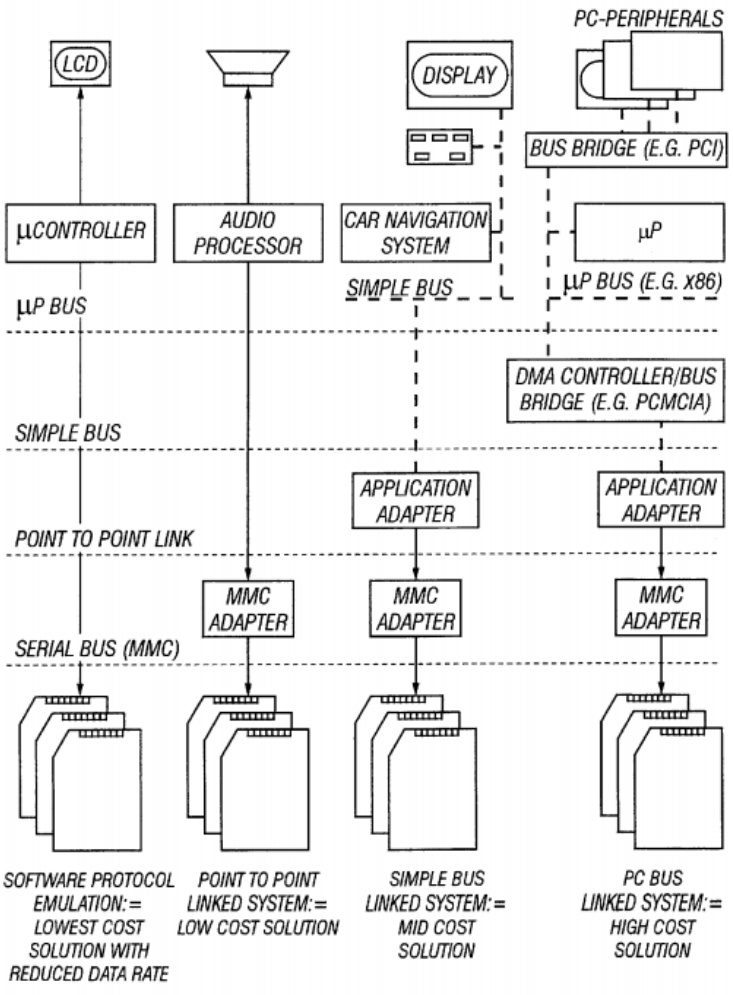


FIG. 1

While Toombs does not disclose booting from a non-volatile, flash memory device, McClain does. Specifically, McClain discloses booting from a non-volatile memory, flash memory. Ex. 1006, 2:25-32 ("reading boot code stored in a non-volatile memory, e.g., Flash memory").

As discussed above in Sections IV.B and IV.C it was known at the time of the '487 Patent that a host computer could boot from flash memory devices,

including removable flash memory devices such as MMC cards. Hutton, for example, teaches that NAND flash memory devices, such as MMC cards, were used to reduce the time to boot computing devices, such as cellular phones. Ex. 1016, 3:49-51, 4:44-62 (describing MMC and SD cards as exemplary devices to be used for boot without first copying the boot data to RAM); *see* also Ex. 1003, ¶111. Hutton's NAND flash memory device is used to store boot code, which is accessed in only 15 microseconds. Ex. 1016, 1:48-53, 3:51-57. In addition, Hutton teaches that flash memory has several advantages over other dedicated storage devices, such as read-only memory (ROM). *Id*., 3:34-48. Samsung's OneNAND flash is another example of a flash memory device for booting a host device in a variety of products including "RS-MMC, MMC, CompactFlash, and SmartMedia." Ex. 1012, 5, 103.

In addition to booting from MMC flash memory cards, at the time of the '487 Patent, it was known that a host could boot from other types of removable non-volatile flash memory devices. Ex. 1003, ¶112. Huang, for example, discloses an Intel computer motherboard with support for booting from a USB flash drive. Ex. 1015, 16:11-21. As another example, Deng discloses booting a computer host using a flash memory device connected via USB or a wireless interface. Ex. 1020, 3:5-14, 4:57-65.

Because Toombs discloses the continual development of MMC platforms and cards, and because it was well-known that a host could be booted from a flash memory device, including a removable flash memory device such as a MMC card, a POSA viewing Toombs and McClain would have been motivated to combine them by modifying the disclosure of an MMC memory card in Toombs in view of the disclosure of booting in McClain. *See* Ex. 1003, ¶113.

McClain describes using one signal for booting from a non-volatile, flash memory device without adding another control signal. Ex. 1006, 4:52-64. *see also* Ex. 1003, ¶114. The systems disclosed by Toombs explicitly contemplate using the standard MMC interface. Ex. 1005, 5:66-6:16, 7:32-46. In addition, McClain teaches the advantages of reducing the number of interface lines in a system and Toombs discloses using a minimal number of signals between a host and an MMC card. Ex. 1006, 2:1-12, 2:18-22; Ex. 1005, 6:18-20; *see* Ex. 1003, ¶114. Accordingly, a POSA would have been motivated to use the standard MMC interface in Toombs for booting a host device from an MMC card without adding another, special purpose control line for sending a boot signal. Ex. 1003, ¶114.

Further, a POSA would understand from McClain that any type of interface could be used for booting from a non-volatile, flash memory. Ex. 1006, 5:7-11; Ex. 1003, ¶115. For instance, in Toombs, the MMC interface only requires two

communication lines (i.e., DAT and CMD lines) and power and clock lines. Ex. 1005, 5:66-6:16, 7:32-46, Figs. 1, 14. Based on McClain's teachings, a POSA would understand that an interface to a flash memory could support boot without the addition of a special purpose boot line. Ex. 1006, 4:52-64; Ex. 1003, ¶115.

Accordingly, because Toombs discloses the standard MMC interface with two communication lines and because McClain contemplates supporting boot without adding a special purpose boot line, a POSA would have implemented booting via the MMC interface in Toombs by selecting between the two communication lines of the MMC interface (*i.e.*, command and data). Ex. 1003, ¶115. The clock and power lines would not have been used because they have other uses during system power-up, system reset, and boot. *Id.*. The clock line would be used for synchronization of information and the power line would be used to provide power to the peripheral device. *Id.*; Ex. 1005, 7:35-47. Between the command and data lines, the data line would be the most reasonable choice by a POSA for receiving data from the peripheral device during boot, such as the boot code disclosed in McClain. Ex. 1003, ¶115. ***The command line, on the other hand, would be the most logical choice by a POSA for indicating boot to the peripheral device***. *Id.*

Having selected the command line for boot, a POSA would select a state to indicate boot from a finite number of identified, predictable potential solutions. Ex. 1003, ¶116. Toombs teaches the need to continuously develop systems for MMC cards across a variety of applications spanning from low cost to high cost systems. Ex. 1005, 1:9-26, Fig. 1. In addition, McClain discloses that the flash memory could recognize system reset in order to know when to access initial code (i.e., the boot code) sequence "through the assertion of an unusual combination of standard SDRAM interface pins, such as the simultaneous assertion of CS#, RAS#, CAS#, and WE#." Ex. 1006, 4:32-38, Fig. 2. McClain also describes that one signal, such as Boot#, could serve the functions of system reset, boot selection, and addressing control without adding a special purpose boot line. Ex. 1006, 4:52-64; *See also* Ex. 1006, 4:32-51. Further, it was well-known that SDRAM interfaces provided for various operation modes that are set via a combination of the control signals and that specifications for computing systems often reserve unused states for future use. Ex. 1003, ¶104; Ex. 1022, 12:1-4; Ex. 1025, 16; Ex. 1009, 72; Ex. 1017, Table 4. Accordingly, because McClain discloses using an unusual combination of pins in order to know when to access boot code, because McClain describes using a single signal for system reset, boot selection, and addressing control without adding a special purpose boot line, and because it was well-known

that unused pins, bits, or state of pins could be reserved, a POSA would understand that McClain discloses using an unused state of a signal to indicate boot without the addition of a special purpose boot line. Ex. 1003, ¶¶116 and 104-107.

Because the command line transmits digital values, only two states are possible: a low value (*i.e.*, 0) or a high value (*i.e.*, 1). Ex. 1003, ¶116. The high value is used for normal initialization during which a "contiguous stream of logical '1's" are sent as an initialization sequence over approximately 74 clock cycles. Ex. 1005, 17:63-18:4. However, Toombs does not disclose any use of driving the command line to zero during initialization. Ex. 1003, ¶116. Thus, the low value for the command line is unused and unique during initialization and driving the command line to low represents the most logical value available to initiate boot on an MMC device. *Id.*

Because the use of an MMC interface was well-known, and because McClain demonstrates a POSA would implement boot for a flash memory device by using an unused state and without adding a special purpose boot line, a POSA would have been motivated to select the command line of the MMC interface and initiate boot by driving the command line low. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1742 (2007); Ex. 1003, ¶117. Indeed, a POSA would select this solution from a finite number of identified, predictable potential solutions. Ex.

1003, ¶117. The structures and function of a non-volatile, flash memory device for booting were well-known, and thus a POSA would have been capable of selecting the value of "0" (*i.e.*, low)—out of two known options, high or low—for the command line during power-up to indicate to the peripheral device that it should boot. *Id*.

A. Claim 6

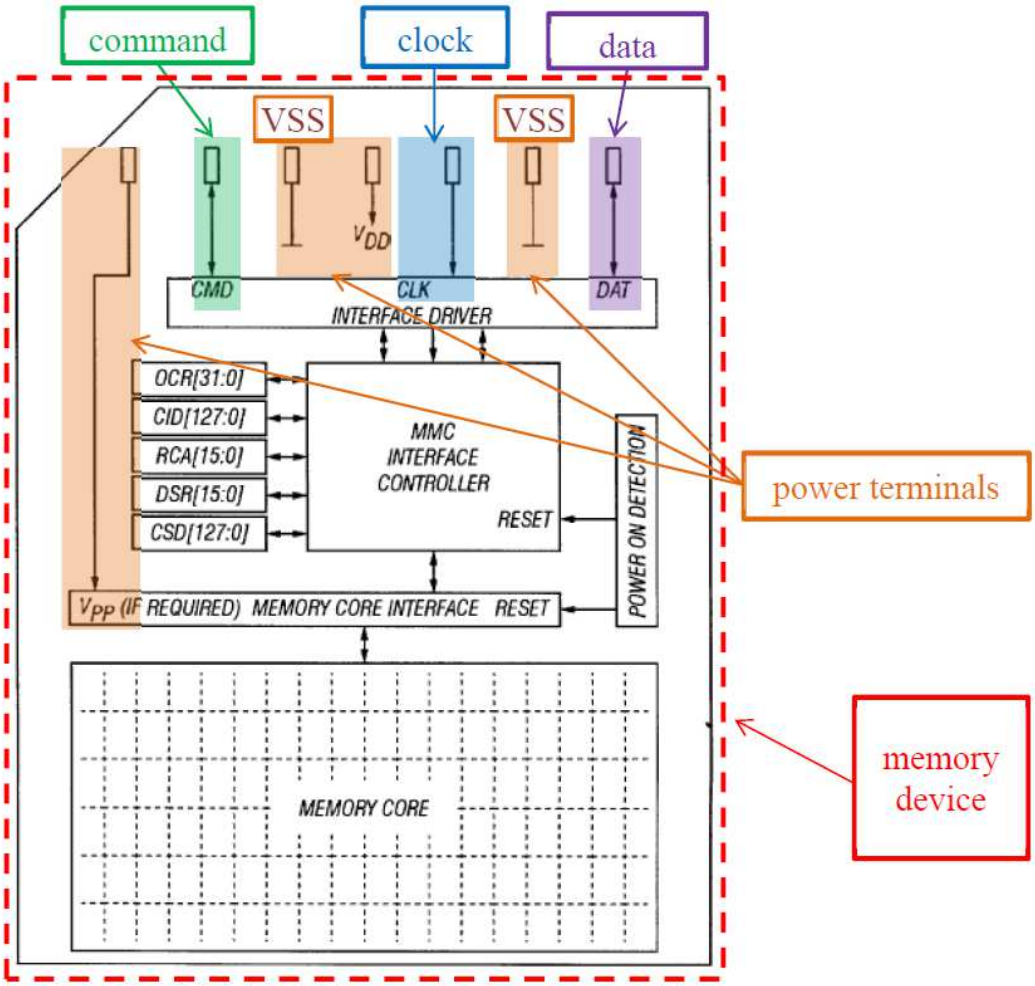
1. Claim 6 [preamble]

To the extent the preamble is limiting, Toombs and McClain disclose "[a] method for booting from a peripheral device having an MMC/SD-interface[2], via said MMC/SD interface with power terminals, a data bus with data bus terminals, a clock line with a clock terminal and a command line with command terminal."

Toombs discloses an MMC card including an MMC interface with all the terminals recited in Claim 6. Ex. 1003, ¶121. Specifically, Toombs discloses an MMC bus that connects an MMC card to an MMC host. Ex. 1005, 6:60-65. The MMC bus includes the following MMC bus lines: power supply, communications (including both CMD and DAT), and clock. Ex. 1005, 7:32-34. Figure 14

[2] MMC/SD means that an MMC or SD interface could be used. This is consistent with the specification of the '487 Patent. *See* Ex. 1001 at 1:10-12 ("More specifically the present invention relates to Multi Media Cards (MMC) or Secure Digital (SD-) cards.")

(annotated and as shown below) of Toombs illustrates an MMC card with command, clock, data, and power terminals that are connected to the MMC bus lines.



The power terminals (*i.e.*, Vdd, Vss1, Vss2, and Vpp) on the MMC card are used for receiving power. Ex. 1003, ¶121. In Figure 14, Vdd provides the main supply voltage, Vss provides the ground, and Vpp provides the programming voltage. Ex. 1003, ¶121. In Figure 14, the data line (*i.e.*, DAT) and the command

line (*i.e.*, CMD) are bidirectional communication lines and the clock line is provided for the MMC host to synchronize data transfer across the MMC bus. Ex. 1005, 7:41-47. In Fig. 30, Toombs describes an MMC interface with a data bus with data bus terminals. Ex. 1005, Fig. 30 (show below). Further, it is well-known that MMC card have multiple data bus terminals. Ex. 1026, Fig. 2. Thus, Toombs discloses a peripheral device (*i.e.*, MMC card) having an MMC interface with power, data, clock, and command terminals connected to an MMC bus with command and clock signals or lines, in addition to a data bus. Ex. 1003, ¶121.

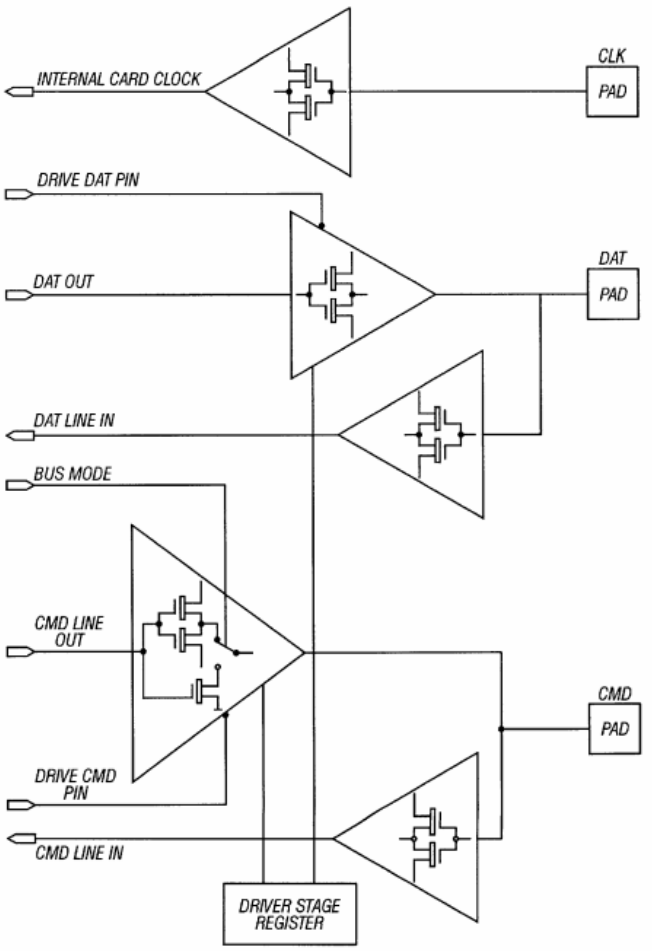


FIG. 30

McClain discloses "booting from a peripheral device," as recited in Claim 6. Ex. 1003, ¶122. Notably, McClain discloses a peripheral device providing boot code for the initialization and boot of the host device. Ex. 1006, 2:7-12, 3:33-37; *see also* Ex. 1003, ¶122. Therefore, the combination of Toombs and McClain, discloses and renders claim element 6 [preamble]. Ex. 1003, ¶122.

2. Claim 6[a]

Toombs discloses "receiving power at said power terminals of said MMC/SD-interface," as recited in claim 6. Toombs describes that the power supply lines include "Vss1, Vss2, and Vdd." Ex. 1005, 7:35-41. Specifically, Toombs describes that "[a]ll of these different voltages are provided to the MultiMediaCard card for performing different operations such as data read, write and erasure, etc." *Id.* In other words, Toombs discloses that the power terminals of an MMC card receive power to allow the MMC card to perform different operations. Ex. 1003, ¶123. Thus, Toombs discloses "receiving power at said power terminals of said MMC/SD-interface," as recited in claim element 6[a]. *Id*.

3. Claim 6[b]

Claim 6[b] recites "receiving a low signal at the command terminal before or during power up."[3] As described below, the combination of Toombs and McClain discloses and renders obvious claim element 6[b]. Ex. 1003, ¶¶124-127.

Toombs discloses a command terminal of an MMC interface. *See supra*, X.A.1. (Claim 6 [preamble]). McClain discloses several different options for

[3] Petitioner and Patent Owner both agreed in the related litigation matter that "during power up" and "during power up process" in the claims should be construed as "during the power up process of the peripheral device." Ex. 1024 at 3.

indicating boot at power up. Ex. 1003, ¶125. For example, McClain discloses indicating boot by asserting an unused state during power-up without the addition of a special purpose boot line.[4] *See* Ex. 1006, 4:32-28 (describing "an unusual combination of standard SDRAM interface pins, such as the simultaneous assertion of CS#, RAS#, CAS#, and WE#"); Ex. 1006, 3:38-43 (describing "during power-up (reset time), e.g., using the system reset generator 60 asserts the system reset signal 61, the internal state machine for sequential boot code access 70 for the system non-volatile memory pre-reads the first row of the memory array and has it ready for read by the end of the system reset time"); *see supra,* Section X; *see also* Ex. 1003, ¶125. The CS, RAS, CAS, and WE lines were well-known to be control lines for a standard SDRAM interface. Ex. 1003, ¶125.

McClain further discloses that a single line can be used to indicate boot without the addition of a special purpose boot line. Ex. 1006, 4:32-38, 4:52-64. Therefore, because McClain discloses using an unusual combination of pins in order to know when to access boot code during power-up, because McClain describes using a single signal for system reset, boot selection, and addressing control without adding a special purpose boot line, and because it was well known

[4] McClain refers to power up and reset interchangeably. *See, e.g.*, Ex. 1006 at 3:38 ("during power-up (reset time)").

that unused pins, bits, or state of pins could be reserved, a POSA would understand from this disclosure that without the addition of a special purpose boot line, a single line could be used to indicate boot using an unused state during power-up. Ex. 1003, ¶125; *see supra*, Section X.

A POSA would have selected the assertion of the command terminal to a low value. Ex. 1003, ¶126. Specifically, McClain recognizes the need for booting from a flash memory and that it is convenient to initiate such booting without the addition of a special purpose boot line. Ex. 1006, 2:25-32, 2:1-13, 4:59-64. Further, Toombs identifies a minimal number of lines for the MMC interface: power, clock, data, and command. *See* Ex. 1005, 6:18-38. Because the power line provides power to the peripheral device, the clock provides synchronization between the host and peripheral, and the data line is used for transmitting data during boot, a POSA would have selected the command line as the most logical choice to indicate boot to the peripheral device. Ex. 1005, 5:66-6:38; *see supra*, Section X (Combination of Toombs and McClain); Ex. 1003, ¶126.

Once a POSA had selected the command line, a POSA would have selected an unused value (*i.e.*, a unique value) to assert in order to indicate boot as disclosed in McClain. Ex. 1006, 4:32-38, 4:52-58 (asserting a single pin to indicate boot); Ex. 1003, ¶127; Ex. 1027, 12 (defining active low as "a logic signal

having its asserted state as the logic ZERO state"). A POSA would not have chosen to assert the command line high because Toombs discloses that the command line is ordinarily held high during initialization of the peripheral device. Ex. 1005, 17:63-66; Ex. 1003, ¶127. Moreover, if the command line is not driven to a value by the host, it would rise to a logical high value (*i.e.*, a value of 1) because it is terminated with a pull-up resistor, RCMD. Ex. 1005, 25:8-14; Ex. 1003, ¶127; *supra*, IV.A (MMC 1.4).

Thus, a POSA would choose to assert the command line low to indicate boot at power-up. *See* Ex. 1003, ¶127 (explaining that a low value on the command line would not conflict with other uses of the peripheral device and the command line would not involuntarily float to a low value); *See supra,* Section X. Thus, Toombs in view of McClain discloses and renders obvious receiving a low signal at the command terminal before or during power up. Ex. 1003, ¶127.

4. Claim 6[c]

Claim 6[c] recites "sending the first data of a predefined storage area via data bus, starting with a start bit of the first data frame." McClain discloses a non-volatile memory that "pre-reads the first row of the memory array and has it ready for read by the end of system reset time." Ex. 1006, 3:38-43. During system initialization, a first location in the first memory row, which corresponds to the

beginning of the boot code, is pre-read and sent to the host. *Id.*, 3:43-46; 4:39-43 ("[T]he non-volatile memory 20 must be able to recognize that it is being selected to deliver code."). A POSA would understand from this disclosure that the first location in the first row of the memory array in McClain discloses "the first data of a predefined storage area," as recited in Claim 6. Ex. 1003, ¶129. After the first location in the first row of the memory array is delivered, the memory array increments its "internal address to select the next location in the first memory row." Ex. 1006, 3:43-52. Thus, a POSA would understand from this disclosure in McClain that the boot code being delivered to the host from the flash memory device is predefined. Ex. 1003, ¶129.

Further, Toombs discloses a data line (*i.e.*, data bus) of an MMC interface. *See supra*, X.A.1 (Claim 6[preamble]). The data line is used to transfer data between the MMC host and MMC card connected to the MMC interface. Ex. 1005, 6:34-41. The data line is "maintained high when data is not being transmitted." *Id.*, 19:38-43. When data is transmitted, the "transmitted data block consists of a start bit (LOW), followed by a continuous data stream." *Id*. "The data stream contains the payload data (and error correction bits if an off-card ECC is used) and ends with an end bit (HIGH)." *Id.*, 41-43. In other words, the data block includes a start bit, payload, and an end bit. *Id.*, 38-43.

Figure 12 (shown below) of Toombs illustrates the data packet format (including the start bit) for sequential data and block data that, for example, may be returned from an MMC card in response to a read command.

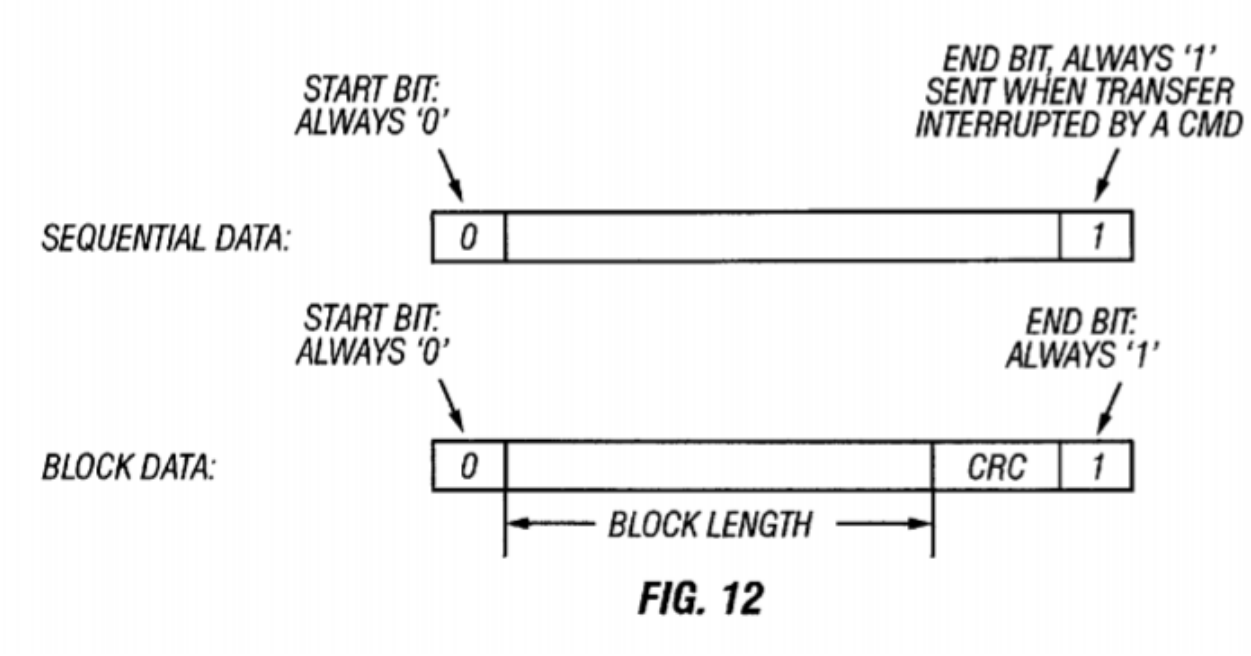


FIG. 12

See id., Fig. 12; *see also id.,* 9:12-16. When the MMC host issues a command, the MMC card responds with a start bit of '0' on the data line, followed by the payload data and then the end bit of '1.' *Id*., 19:38-20:29 (describing various types of data reads), Fig. 12. Thus, Toombs teaches a data transmission on a data line that begins with a start bit. Ex. 1003, ¶131.

In view of Toombs' disclosures regarding a start bit, a POSA would understand that a peripheral device would initiate a data transfer with the host device by using a start bit. Ex. 1003, ¶132. Moreover, the specification of the

'487 Patent clarifies that "data transmission" disclosed in Toombs and the "data frame" recited in Claim 6 are analogous. *See* Ex. 1001, 4:39-40 ("monitoring the data bus terminals for a start bit of a data transmission/data frame"). Thus, Toombs in combination with McClain teaches an MMC card (*i.e.*, peripheral device) that sends data, "starting with a start bit of the first data frame." Ex. 1003, ¶132. Moreover, McClain teaches that the first data frame or transmission represents the first data (*e.g.*, first row) of a predefined storage area in the flash memory. *Id.* Toombs in combination with McClain therefore discloses or renders obvious every limitation of Claim 6 and renders the claim obvious. *Id.*

B. Claim 7

Claim 7 recites that "said first data of a predefined storage area via data bus, are only send if and when receiving a low signal at said command terminal of said MMC/SD-interface during power-up process during the transmission of between 24 to 148, preferably between 60 and 100 and most preferably to 74 initialization clock cycles."

As discussed above, Toombs in combination with McClain discloses receiving a low signal at the command terminal (of the MMC interface) during power up. *See supra*, Section X.A.3 (Claim 6[b]). Further, Toombs in combination with McClain discloses "sending the first data of a predefined storage

area via data bus." *See supra*, Section X.A.4 (Claim 6[c]). Accordingly, in view of the discussion above with regard to Claim elements 6[b] and 6[c], a POSA would understand that Toombs in combination with McClain discloses sending boot data (*i.e.*, first data of a predefined storage area) via a data bus if and when a low signal is received at a command terminal during power up. Ex. 1003, ¶134.

Further, Toombs recognizes that the purpose of the clock is to "synchronize data transfer across the bus." Ex. 1005, 7:38-46. McClain also teaches the purpose of the clock by disclosing a signal for boot is "asserted for several clock cycles or some otherwise relatively long period to indicate a system reset." Ex. 1006, 4:52-55. Toombs further recognizes that an initialization sequence on the CMD line may last for 1 ms (*i.e.*, 74 initialization clock cycles). Ex. 1005, 17:65-18:4. In other words, Toombs discloses asserting 74 clock cycles during an initialization sequence. Ex. 1003, ¶135. Because Toombs in combination with McClain discloses receiving a low signal at the command terminal (of the MMC interface) during power up (*See supra*, Section X.A.3 (Claim 6[b])) and because receiving a low signal at the command terminal during power up is an initialization sequence, a POSA would recognize that Toombs in combination with McClain disclose receiving a low signal at the command terminal during the transmission of 74 clock cycles. Ex. 1003, ¶135.

Because Toombs teaches the transmission of an initialization sequence for 74 clock cycles, which is the "most preferable" duration recited in Claim 7, Toombs also teaches the "preferable" range of durations (*i.e.*, between 60 and 100 clock cycles) and the presumably less preferable rage of durations (*i.e.*, 24 to 148 clock cycles) that are recited in Claim 7. Ex. 1003, ¶136. Thus, the combination of Toombs and McClain discloses and renders Claim 7 obvious. *Id*.

C. Claim 20

1. Claim 20 [preamble]

To the extent that the preamble is limiting, Toombs and McClain disclose "[a] peripheral device having an MMC/SD-interface configured for booting a bootable host device configured for being booted from a peripheral device having an MMC/SD-interface." Toombs discloses a host device and a peripheral device connected via an MMC interface. *See supra*, Section X.A.1 (Claim 6[preamble]). McClain discloses a bootable host device being booted from a peripheral device (*i.e.*, a flash memory device). *See supra*, Section X.A.1 (Claim 6[preamble]). Therefore, the combination of Toombs and McClain discloses and renders obvious claim element 20 [preamble]. Ex. 1003, ¶138.

2. Claim 20[a]

Claim 20[a] recites "an MMC/SD-interface, provided with power terminals, a data bus with data bus terminals, a clock line with a clock terminal and a

command line with command terminal." Toombs discloses an MMC interface with power, clock, command, and data terminals. *See supra*, Section X.A.1 (Claim 6 [preamble]).

3. Claim 20[b]

Claim 20[b] recites "a peripheral device controller, connected to said MMC/SD-interface." Toombs discloses an MMC interface controller in an MMC card that is connected via interface drivers to the terminals of the MMC interface. Ex 1005, Fig. 14 (shown below). A POSA would therefore understand that the MMC interface controller connected via interface drivers to the terminals of the MMC interface in Toombs discloses "a peripheral device controller, connected to said MMC/SD-interface." Ex. 1003, ¶140.

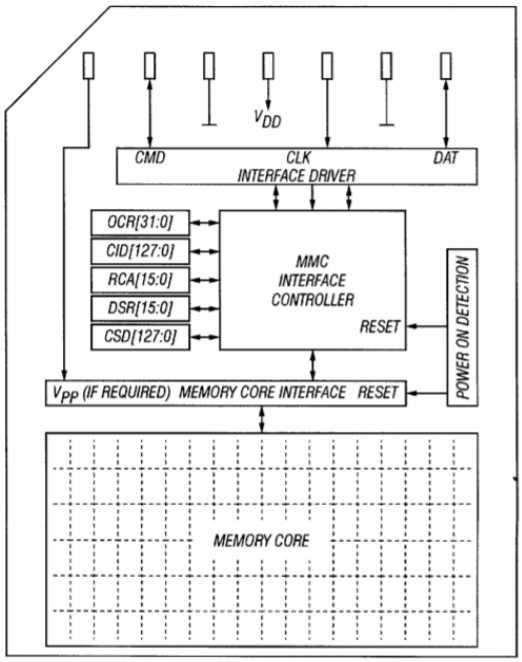


FIG. 14

4. Claim 20[c]

Claim 20[c] recites "a memory module, connected to said peripheral device controller."[5] Toombs discloses a memory core in an MMC card that is connected via a memory core interface to the MMC interface controller. Ex 1005, Fig. 14 (shown below). A POSA would therefore understand that the memory core connected via a memory core interface to the MMC interface controller in Toombs discloses "a memory module, connected to said peripheral device controller." Ex. 1003, ¶141.

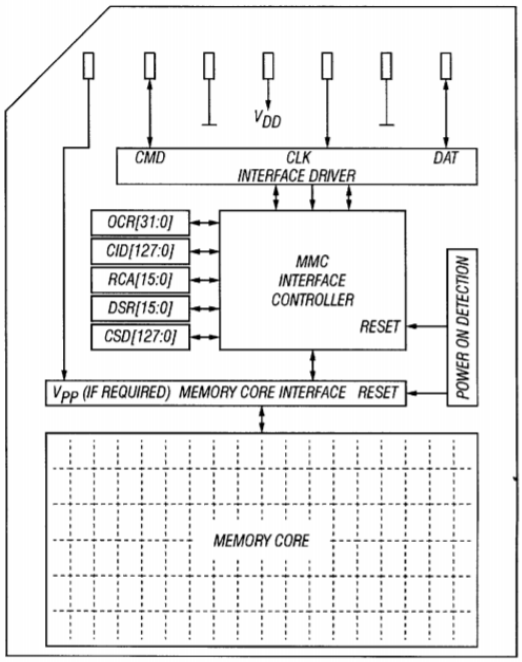


FIG. 14

[5] Petitioner and Patent Owner both agreed in the related litigation matter that "memory module" in the claims should be construed as a "memory portion of the peripheral device, or a sub-portion of the memory portion of the peripheral device." Ex. 1024 at 4.

5. Claim 20[d]

Claim 20[d] recites "wherein said peripheral device controller is configured for sending the first data of a predefined storage area via a data bus, starting with a start bit of the first data frame, when receiving power at the terminals of said MMC/SD-interface of said peripheral device, and a low signal at the command terminal of said MMC/SD-interface during power-up."

Toombs discloses receiving power at the terminals of an MMC interface of an MMC card. *See supra*, Section X.A.2 (Claim 6[a]). Moreover, Toombs in view of McClain discloses a host device sending a low signal on the command line to the command terminal of an MMC card during power-up. *See supra*, Section X.A.3 (Claim 6[b]).

In addition, Toombs in view of McClain discloses "sending the first data of a predefined storage area via data bus, starting with a start bit of the first data frame," as recited in Claim 6. *See supra*, Section X.A.4 (Claim 6[c]). In view of Toombs's disclosure, a POSA would understand that Toombs' MMC interface controller (as shown in Fig. 14 above) controls the process of sending data to a host via the data terminal. Ex. 1003, ¶144; Ex. 1005, Figs. 5-8, 14. Toombs in view of McClain further discloses that the boot data (*i.e.*, first data of a predefined storage area) is sent from an MMC card when receiving power at terminals of the

MMC interface of the MMC card and a low signal at the command terminal of the MMC card during power up. Ex. 1003, ¶144, Ex. 1006, 3:38-43, 4:52-64 (explaining that, during power up, a single signal may be received by a peripherical device and the peripherical device may retrieve and send boot data in response to this signal), *see supra* Section X.A.3 (Claim 6[b]); *see supra,* Section X (Combination of Toombs and McClain). Thus, Toombs in view of McClain discloses and renders this claim obvious. Ex. 1003, ¶144.

D. Claim 21

Toombs in combination with McClain discloses "said peripheral device controller is further configured to send said first data of a predefined storage area via data bus, only when receiving a low signal at said command terminal of said MMC/SD-interface before or during power-up process during the transmission of between 24 to 148, preferably between 60 and 100 and most preferably to 74 initialization clock cycles," as recited in Claim 21, for at least the reasons described above for Claim 7. *See supra*, Section X.B, X.C.5 (explaining that a POSA would understand that Toombs' MMC interface controller controls the process of sending data to a host via the data terminal).

XI. GROUND 2: CLAIMS 6, 7, 20, AND 21 ARE RENDERED OBVIOUS BY *TOOMBS*, *MCCLAIN*, AND *KOZAKAI*.

As shown below, Toombs, McClain, and Kozakai render Claims 6, 7, 20, and 21 of the '487 Patent obvious under 35 U.S.C. §103. *See also* Ex. 1003, ¶¶146-168.

A POSA would have been motivated to combine Toombs, McClain, and Kozakai. As explained above in Section X, a POSA would have been motivated to combine Toombs and McClain by modifying the disclosure of an MMC memory card in Toombs in view of the disclosure of booting in McClain. Similarly, because Kozakai also describes booting from a flash memory and because it was well-known that a host could be booted from a flash memory device, including a removable flash memory device such as a MMC card, a POSA would have been motivated to combine Toombs, McClain, and Kozakai by modifying the disclosure of an MMC memory card in Toombs in view of the disclosures of booting in McClain and Kozakai. Ex. 1007, 19:21-24, 19:40-46; Ex. 1003, ¶147.

As discussed above in Section X, a POSA would have been motivated to use the standard MMC interface in Toombs for booting a host device from an MMC card without adding another, special purpose control line for sending a boot signal and that the command line would be the most logical choice by a POSA for indicating boot to the peripheral device. Ex. 1003, 148; *see supra*, X.

Having selected the command line, a POSA would implement receiving a low signal at the command line of the MMC card to initiate boot and sending boot data in response to received low signal in view of Toombs, McClain, and Kozakai. Ex. 1003, ¶147. Toombs discloses that a high value is used for normal initialization during which a "contiguous stream of logical '1's" are sent as an initialization sequence over approximately 74 clock cycles. Ex. 1005, 17:63-18:4. Further, as discussed above, McClain demonstrates a POSA would implement boot for a flash memory device by using an unused state and without adding a special purpose boot line. *See supra*, Section X. Additionally, Kozakai discloses that a "flash memory is enabled to function as a boot device by storing at the leading address ('0') of the memory array of the flash memory the program to be executed first time at the time of actuating the system." Ex. 1007, 19:21-24. Further, Kozakai describes that the data from the leading address ("0") of the memory array of the flash memory is read out in response to a low signal received at an external terminal (for example, PRE) of the flash memory from an external device, such as a host CPU, during power-up. Ex. 1007, 18:59-61, 19:1-9, 19:14-15, 19:40-46. In other words, Kozakai describes that an external terminal of the flash memory receives a low signal during power-up and in response to the low signal, the flash

memory reads the data (*i.e.*, boot) from the leading address ("0") of the memory array and supplies it externally (*i.e.*, to the host CPU). Ex. 1003, ¶148.

Because the use of an MMC interface was well-known, because McClain demonstrates that a POSA would implement boot for a flash memory device by using an unused state and without adding a special purpose boot line, because Toombs discloses that a high value is already used for normal initialization, and because Kozakai describes receiving (at an external terminal of the flash memory) a low signal during power-up and reading boot data in response to the low signal, a POSA would have been motivated to select the command line of the MMC interface and initiate boot by driving the command line low during power-up. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1742 (2007); Ex. 1003, ¶148. The structures and function of a non-volatile, flash memory device for booting was well-known, and thus a POSA would have been capable of selecting a low signal for the command line during power-up to indicate to the peripheral device that it should boot. Ex. 1003, ¶148.

A. Claim 6

1. Claim 6 [preamble]

To the extent the preamble is limiting, Toombs and McClain disclose "[a] method for booting from a peripheral device having an MMC/SD-interface, via

said MMC/SD interface with power terminals, a data bus with data bus terminals, a clock line with a clock terminal and a command line with command terminal." *See supra*, Section X.A.1 (Claim 6 [preamble]).

Further, Kozakai discloses "booting from a peripheral device," as recited in Claim 6. Ex. 1003, ¶150. Notably, Kozakai discloses that a "flash memory is enabled to function as a boot device by storing at the leading address ('0') of the memory array of the flash memory the program to be executed first at the time of actuating the system." Ex. 1007, 19:21-24. Therefore, the combination of Toombs, McClain, and Kozakai discloses and renders obvious claim element 6 [preamble]. Ex. 1003, ¶150.

2. Claim 6[a]

Toombs discloses "receiving power at said power terminals of said MMC/SD-interface," as recited in Claim 6. *See supra*, Section X.A.2.

3. Claim 6[b]

Claim 6[b] recites "receiving a low signal at the command terminal before or during power up." As described below, the combination of Toombs, McClain, and Kozakai discloses and renders obvious claim element 6[b]. Ex. 1003, ¶¶152-153.

As discussed above in Sections X and XI, a POSA would have been motivated to use the standard MMC interface in Toombs for booting a host device

from an MMC card without adding another, special purpose control line for sending a boot signal and that the command line would be the most logical choice by a POSA for indicating boot to the peripheral device. *See supra*, Sections X, XI.

Having selected the command line, a POSA would implement receiving a low signal at the command line of the MMC card to initiate boot and sending boot data in response to received low signal in view of Toombs, McClain, and Kozakai. Ex. 1003, ¶153. Toombs discloses that a high value is used for normal initialization during which a "contiguous stream of logical '1's" are sent as an initialization sequence over approximately 74 clock cycles. Ex. 1005, 17:63-18:4. Further, as discussed above, McClain demonstrates a POSA would implement boot for a flash memory device by using an unused state and without adding a special purpose boot line. *See supra*, Section X. Additionally, Kozakai discloses that a "flash memory is enabled to function as a boot device by storing at the leading address ('0') of the memory array of the flash memory the program to be executed first time at the time of actuating the system." Ex. 1007, 19:21-24. Further, Kozakai describes that the data from the leading address ("0") of the memory array of the flash memory is read out in response to a low signal received at an external terminal (for example, PRE) of the flash memory from an external device, such as a host CPU, during power-up. Ex. 1007, 18:59-61, 19:1-9, 19:14-15, 19:40-46. In

other words, Kozakai describes that an external terminal of the flash memory receives a low signal during power-up and in response to the low signal, the flash memory reads the data (*i.e.*, boot) from the leading address ("0") of the memory array and supplies it externally (*i.e.*, to the host CPU). Ex. 1003, ¶153.

A POSA would have been motivated to select the command line of the MMC interface and initiate boot by driving the command line low during power-up, as explained above in Section X.

Thus, a POSA would choose to assert the command line low to indicate boot at power-up. *See* Ex. 1003, ¶153 (explaining that a low value on the command line would not conflict with other uses of the peripheral device and the command line would not involuntarily float to a low value); *see supra,* Section X. Thus, Toombs in view of McClain and Kozakai discloses or renders obvious receiving a low signal at the command terminal before or during power up. Ex. 1003, ¶153.

4. Claim 6[c]

Toombs in combination with McClain discloses "sending the first data of a predefined storage area via data bus, starting with a start bit of the first data frame." *See supra*, Section X.A.4.

Further, Kozakai discloses that a "flash memory is enabled to function as a boot device by storing at the leading address ('0') of the memory array of the flash

memory the program to be executed first time at the time of actuating the system." Ex. 1007, 19:21-24. Kozakai also describes that the data from the leading address ("0") of the memory array of the flash memory is read out in response to a low signal received at an external terminal (for example, PRE) of the flash memory from an external device, such as a host CPU, during power-up. Ex. 1007, 18:59-61, 19:1-9, 19:14-15, 19:40-46. A POSA would understand from these disclosures that "the leading address ("0") of the memory array" in Kozakai discloses "the first data of a predefined storage area," as recited in Claim 6. Ex. 1003, ¶155.

Therefore, the combination of Toombs, McClain, and Kozakai discloses and renders obvious claim element 6[c]. Ex. 1003, ¶155.

B. Claim 7

Claim 7 recites that "said first data of a predefined storage area via data bus, are only send if and when receiving a low signal at said command terminal of said MMC/SD-interface during power-up process during the transmission of between 24 to 148, preferably between 60 and 100 and most preferably to 74 initialization clock cycles."

As discussed above, Toombs in combination with McClain and Kozakai discloses receiving a low signal at the command terminal (of the MMC interface) during power up. *See supra*, Section XI.A.3 (Claim 6[b]). Further, Toombs in

combination with McClain and Kozakai discloses "sending the first data of a predefined storage area via data bus." *See supra*, Section XI.A.4 (Claim 6[c]). Accordingly, in view of the discussion above with regard to Claim elements 6[b] and 6[c], a POSA would understand that Toombs in combination with McClain and Kozakai discloses sending boot data (*i.e.*, first data of a predefined storage area) via a data bus if and when a low signal is received at a command terminal during power up. Ex. 1003, ¶157.

Further, Toombs recognizes that the purpose of the clock is to "synchronize data transfer across the bus." Ex. 1005, 7:38-46. McClain also teaches the purpose of the clock by disclosing a signal for boot is "asserted for several clock cycles or some otherwise relatively long period to indicate a system reset." Ex. 1006, 4:52-55. Toombs further recognizes that an initialization sequence on the CMD line may last for 1 ms (i.e., 74 initialization clock cycles). Ex. 1005, 17:65-18:4. In other words, Toombs discloses asserting 74 clock cycles during an initialization sequence. Ex. 1003, ¶158. Because Toombs in combination with McClain and Kozakai discloses receiving a low signal at the command terminal (of the MMC interface) during power up (*see supra*, Section XI.A.3 (Claim 6[b])) and because receiving a low signal at the command terminal during power up is an initialization sequence, a POSA would recognize that Toombs in combination with

McClain and Kozakai discloses receiving a low signal at the command terminal during the transmission of 74 clock cycles. Ex. 1003, ¶158.

Because Toombs teaches the transmission of an initialization sequence for 74 clock cycles, which is the "most preferable" duration recited in Claim 7, Toombs also teaches the "preferable" range of durations (*i.e.*, between 60 and 100 clock cycles) and the presumably less preferable rage of durations (*i.e.*, 24 to 148 clock cycles) that are recited in claim 7. Ex. 1003, ¶159. Thus, the combination of Toombs, McClain, and Kozakai discloses and renders Claim 7 obvious. *Id*.

C. Claim 20

1. Claim 20 [preamble]

To the extent that the preamble is limiting, Toombs, McClain, and Kozakai disclose "[a] peripheral device having an MMC/SD-interface configured for booting a bootable host device configured for being booted from a peripheral device having an MMC/SD-interface." Toombs discloses a host device and a peripheral device connected via an MMC interface. *See supra*, Section X.A.1 (Claim 6 [preamble]). McClain and Kozakai disclose a bootable host device being booted from a peripheral device (*i.e.*, a flash memory device). *See supra*, Sections X.A.1 (Claim 6 [preamble]), XI.A.1 (Claim 6 [preamble]). Therefore, the

combination of Toombs, McClain, and Kozakai discloses and renders claim element 20 [preamble]. Ex. 1003, ¶160.

2. Claim 20[a]

Claim 20[a] recites "an MMC/SD-interface, provided with power terminals, a data bus with data bus terminals, a clock line with a clock terminal and a command line with command terminal." Toombs discloses an MMC interface with power, clock, command, and data terminals. *See supra*, X.A.1 (Claim 6 [preamble]).

3. Claim 20[b]

Toombs discloses "a peripheral device controller, connected to said MMC/SD-interface." *See supra*, Section X.C.3 (Claim 20[b]).

4. Claim 20[c]

Toombs discloses "a memory module, connected to said peripheral device controller." *See supra*, Section X.C.4 (Claim 20[c]).

5. Claim 20[d]

Claim 20[d] recites "wherein said peripheral device controller is configured for sending the first data of a predefined storage area via a data bus, starting with a start bit of the first data frame, when receiving power at the terminals of said MMC/SD-interface of said peripheral device, and a low signal at the command terminal of said MMC/SD-interface during power-up."

Toombs discloses receiving power at the terminals of an MMC interface of an MMC card. *See supra*, X.A.2 (Claim 6[a]). Moreover, Toombs in view of McClain and Kozakai disclose a host device sending a low signal on the command line to the command terminal of an MMC card during power-up. *See supra*, XI.A.3 (Claim 6[b]).

In addition, Toombs in view of McClain and Kozakai discloses "sending the first data of a predefined storage area via data bus, starting with a start bit of the first data frame," as recited in Claim 6. *See supra*, Sections X.A.4 (Claim 6[c]), XI.A.4 (Claim 6[c]). In view of Toombs's disclosure, a POSA would understand that Toombs' MMC interface controller controls the process of sending data to a host via the data terminal. Ex. 1003, ¶167; Ex. 1005, Figs. 5-8, 14; *see supra,* Section X.C.5. Toombs in view of McClain and Kozakai further disclose that the boot data (*i.e.*, first data of a predefined storage area) is sent from an MMC card when receiving power at terminals of the MMC interface of the MMC card and a low signal at the command terminal of the MMC card during power up. Ex. 1003, ¶167; Ex. 1006, 3:38-43, 4:52-64 (explaining that, during power up, a single signal may be received by a peripherical device and the peripherical device may retrieve and send boot data in response to this signal); Ex. 1007, 18:59-61, 19:1-9, 19:14-15, 19:40-46 (explaining that an external terminal of the flash memory receives a

low signal during power-up and in response to the low signal, the flash memory reads the data (*i.e*., boot) from the leading address ("0") of the memory array and supplies it externally (i.e., to the host CPU)); *see supra* X.A.3 (Claim 6[b]), XI.A.3 (Claim 6[b]), XI (Combination of Toombs, McClain, and Kozakai). Thus, Toombs in view of McClain and Kozakai discloses and renders this claim obvious.

Ex. 1003, ¶167.

D. Claim 21

Toombs in combination with McClain and Kozakai disclose "said peripheral device controller is further configured to send said first data of a predefined storage area via data bus, only when receiving a low signal at said command terminal of said MMC/SD-interface before or during power-up process during the transmission of between 24 to 148, preferably between 60 and 100 and most preferably to 74 initialization clock cycles," as recited in Claim 21 for at least the reasons noted above for Claim 7. *See supra*, XI.B, XI.C.5 (explaining that a POSA would understand that Toombs' MMC interface controller controls the process of sending data to a host via the data terminal).

XII. GROUND 3: CLAIMS 13, 26, 42, AND 52 ARE RENDERED OBVIOUS BY *TOOMBS*, *MCCLAIN*, AND *KURAKATA*.

As shown below, Toombs, McClain, and Kurakata render Claims 13, 26, 42, and 52 of the '487 Patent obvious under 35 U.S.C. §103. *See also* Ex. 1003, ¶¶169-195.

A POSA would have been motivated to combine Toombs, McClain, and Kurakata. As discussed above in Section X, a POSA would have been motivated to use the standard MMC interface in Toombs for booting a host device from an MMC card without adding another, special purpose control line for sending a boot signal and that the command line would be the most logical choice by a POSA for indicating boot to the peripheral device. Ex. 1003, ¶169; *see supra*, X.

Having selected the command line, a POSA would implement receiving an argument for a boot request at the peripheral device during an initialization procedure of the peripheral device and sending boot data to a host in response to received argument for boot request in view of Toombs, McClain, and Kurakata. Ex. 1003, ¶170. Specifically, McClain describes using one signal (for example, an unused signal) for a boot request from a non-volatile, flash memory device without adding another control signal during an initialization procedure of the peripheral device. Ex. 1006, 4:52-64; *see also* Ex. 1006, 34-37 (explaining the boot code for initializing the system, which includes the flash memory, is stored in the flash

memory); *see also* Ex. 1006 53-55 (explaining that the system stars initialization process by issuing reads to the non-volatile memory address range); *see also* Ex. 1003, ¶170; *See also*, Section X. Further, Kurakata discloses an MMC card that receives, during an initialization procedure of the MMC card, an initialization command CMD0 including an 8-bit command index, a 32-bit argument, and an 8-bit CRC code. Ex. 1008, 6:59-63. Because Toombs uses a "contiguous stream of logical '1's" as an initialization sequence, a POSA would recognize that an unused state implemented during an initialization procedure of the MMC card in Toombs would be something other than a "contiguous stream of logical '1's." Ex 1003, ¶170. Ex. 1005, 17:63-18:4. In fact, a POSA will be motivated to implement an initialization command CMD0 including a 32-bit argument for the boot request during the initialization procedure of the MMC card in view of Kurakata. Ex. 1003, ¶170.

In other words, because the use of an MMC interface was well-known, because the command line in Toombs would be the most logical choice by a POSA for indicating boot to the peripheral device, because McClain demonstrates that a POSA would implement a boot request from a non-volatile, flash memory device by using an unused state and without adding a special purpose boot line during an initialization procedure of the peripheral device, and because Kurakata discloses

sending an initialization command CMD0 including a 32-bit argument to an MMC card during the initialization procedure of the MMC card, a POSA would have been motivated to select the command line of the MMC interface, initiate boot by sending a command with an argument for boot request during an initialization procedure of the MMC card to the command line of the MMC card, and send boot data to a host in response to the MMC card receiving the argument for boot request at its command line. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1742 (2007); Ex. 1003, ¶171.

The structures and function of a non-volatile, flash memory device for booting were well-known, and thus a POSA would have been capable of selecting an argument for a boot request for the command line during initialization of the MMC card to indicate to the MMC card that it should boot. Ex. 1003, ¶171.

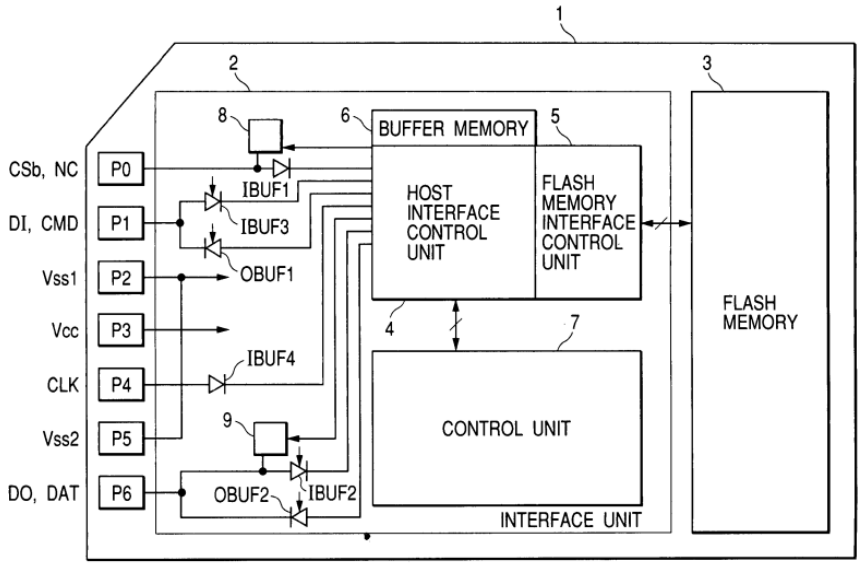
A. Claim 13

1. Claim 13 [preamble]

Toombs and McClain disclose "[a] method for booting a host device from a peripheral device having an MMC/SD-interface with power terminals, a data bus with data bus terminals, a clock line with a clock terminal and a command line with command terminal." *See supra*, Section X.A.1 (Claim 6 [preamble]).

Further, Kurakata discloses an MMC card including an MMC interface with all the terminals recited in Claim 13. Ex. 1003, ¶173. Specifically, Figure 1 (as shown below) of Kurakata illustrates an MMC interface with power terminals (for example, terminals P2, P3, and P5), a data terminal (for example, terminal P6), a clock terminal (for example, terminal P4), and command terminal (for example, terminal P1). Ex. 1008, Fig. 1.

FIG. 1



Therefore, the combination of Toombs, McClain, and Kurakata discloses and renders obvious claim element 13 [preamble]. Ex. 1003, ¶174.

2. Claim 13[a]

Claim 13[a] recites "receiving during an initialization procedure of the peripheral device an argument for a boot request from said host device at said

MMC/SD-interface of the peripheral device." The combination of Toombs, McClain, and Kurakata discloses this feature.

Toombs describes a MultiMediaCard (MMC) bus system that connects a flash memory device (for example, an MMC card) to an MMC host. Ex. 1005, 6:61-65. An MMC interface for the MMC card includes command, clock, and data lines that that transmit information between command, clock, and data terminals of the MMC card and the MMC host. Ex. 1005, 7:14-22, 7:41-47, 6:18-38, Fig. 14. Further, McClain discloses using one signal (for example, an unused signal) for a boot request from a non-volatile, flash memory device without adding another control signal during an initialization procedure of the peripheral device. Ex. 1006, 4:52-64; *See also* Ex. 1006, 3:34-37 (explaining the boot code for initializing the system, which includes the flash memory, is stored in the flash memory); *See also* Ex. 1006 3:53-55 (explaining that the system stars initialization process by issuing reads to the non-volatile memory address range); *See also* Ex. 1003, ¶176; *See supra*, Section X.

Accordingly, as discussed above in Section X, a POSA would have been motivated to use the standard MMC interface in Toombs for booting a host device from an MMC card without adding another, special purpose control line for sending a boot signal to the MMC card during an initialization procedure of the

MMC card and that the command line would be the most logical choice by a POSA for indicating boot to the MMC card. Ex. 1003, ¶176; *see supra*, X. In other words, based on the teachings of Toombs and McClain, a POSA would have been motivated to implement the reception of a boot request from a host device at an MMC interface of the MMC card during the initialization of the MMC card. Ex. 1003, ¶176.

While Toombs and McClain do not specifically describe an argument for a boot request, Kurakata discloses an MMC card that receives, during an initialization procedure of the MMC card, an initialization command CMD0 including an 8-bit command index, a 32-bit argument, and an 8-bit CRC code. Ex. 1008, 6:59-63. Since Toombs already uses a "contiguous stream of logical '1's" as an initialization sequence, a POSA would recognize that an unused state of McClain implemented during an initialization procedure of the MMC card in Toombs would be something other than a "contiguous stream of logical '1's." Ex. 1003, ¶177. In fact, a POSA will be motivated to implement an initialization command CMD0 including a 32-bit argument for the boot request during the initialization procedure of the MMC card in view of Kurakata. Ex. 1003, ¶177.

In other words, a POSA would have been motivated to select the command line of the MMC interface so that MMC interface of the MMC card receives an

argument for a boot request from a host device during the initialization procedure of the MMC card, as discussed above. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1742 (2007); Ex. 1003, ¶178; *Supra*, Section XII.

Therefore, the combination of Toombs, McClain, and Kurakata discloses and renders obvious claim element 13[a]. Ex. 1003, ¶178.

3. Claim 13[b]

Claim 13[b] recites "receiving a clock signal at the clock terminal." Toombs and Kurakata disclose this feature. Specifically, Toombs discloses an MMC bus that connects an MMC card (which includes a clock terminal) to an MMC host. Ex. 1005, 6:60-65, 7:32-34, Fig. 14. The clock terminal receives a clock signal. Ex. 1005, 6:17-23 (explaining that a clock signal CLK is communicated between the host and the MMC card). Further, Kurakata also describes an MMC card including a clock input terminal CLK (for example, terminal P4) that receives a clock signal. Ex. 1008, 5:1-18, Fig. 1, 5:53-58 (explaining that a clock signal is received at terminal P4).

Therefore, the combination of Toombs, McClain, and Kurakata discloses and renders obvious claim element 13[b]. Ex. 1003, ¶179.

4. Claim 13[c]

Claim 13[c] recites "sending data starting with a start bit of a data transmission to said host device via said MMC/SD-interface, if and when boot data are stored in said peripheral device."

Toombs discloses a data line (*i.e.*, data bus) of an MMC interface. *See supra*, X.A.1 (Claim 6[preamble]). The data line is used to transfer data between the MMC host and MMC card connected to the MMC interface. Ex. 1005, 6:34-41. The data line is "maintained high when data is not being transmitted." *Id*., 19:38-43. When data is transmitted, the "transmitted data block consists of a start bit (LOW), followed by a continuous data stream." *Id*. "The data stream contains the payload data (and error correction bits if an off-card ECC is used) and ends with an end bit (HIGH)." *Id*., 41-43. In other words, the data block includes a start bit, payload, and an end bit. *Id*., 38-43.

Figure 12 (shown below) of Toombs illustrates the data packet format (including the start bit) for sequential data and block data that, for example, may be returned from an MMC card in response to a read command.

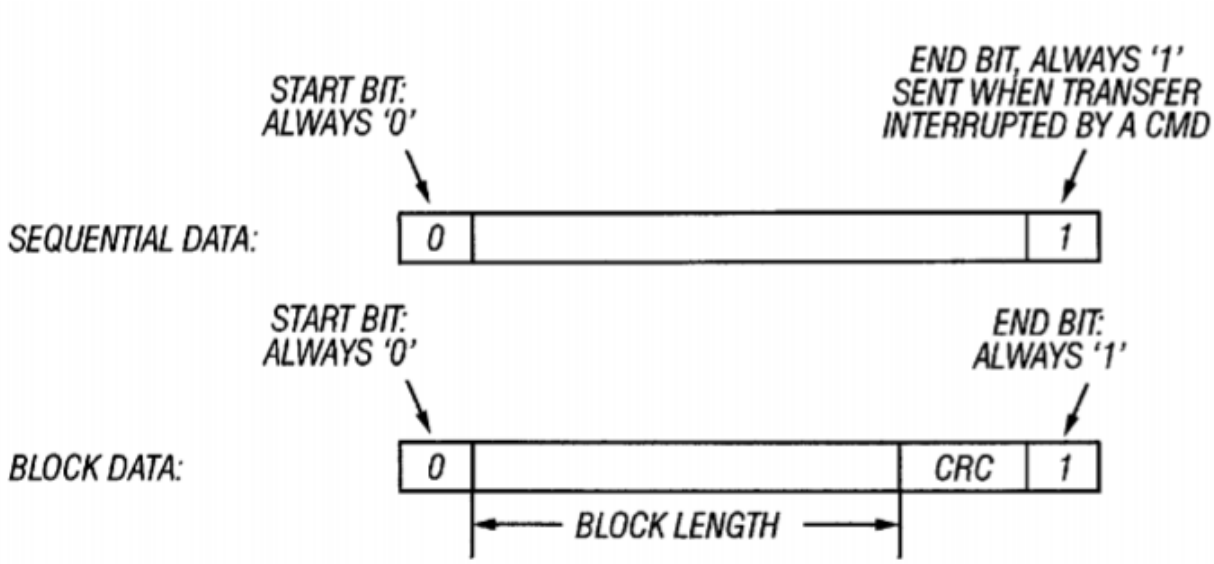


FIG. 12

See id., Fig. 12; *see also id.,* 9:12-16. When the MMC host issues a command, the MMC card responds with a start bit of '0' on the data line, followed by the payload data and then the end bit of '1.' *Id*., 19:38-20:29 (describing various types of data reads), Fig. 12. Thus, Toombs teaches "sending data starting with a start bit of a data transmission to said host device via said MMC/SD-interface," as recited in Claim 13[c]. Ex. 1003, ¶182.

Further, McClain discloses a non-volatile memory that "pre-reads the first row of the memory array and has it ready for read by the end of system reset time." Ex. 1006, 3:38-43. During system initialization, a first location in the first memory row, which corresponds to the beginning of the boot code, is pre-read and sent to the host. *Id.*, 3:43-46; 4:39-43 ("[T]he non-volatile memory 20 must be able to

recognize that it is being selected to deliver code."). Based on such description of McClain, a POSA would recognize that McClain implements a system in which boot data is sent from a peripheral device to the host if and when boot data is stored in the peripheral device. Ex. 1003, ¶183.

Accordingly, because McClain implements a system in which boot data is sent from a peripheral device to the host if and when boot data is stored in the peripheral device, because Toombs teaches "sending data starting with a start bit of a data transmission to said host device via said MMC/SD-interface," and because a POSA would have been motivated to combine Toombs and McClain by modifying the disclosure of an MMC memory card in Toombs in view of the disclosure of booting in McClain, a POSA would recognize that Toombs and McClain disclose sending boot data starting with a start bit of a data transmission to a host device via an MMC interface if and when boot data is stored in an MMC card. Ex. 1003, ¶184. *See supra*, X.

Therefore, the combination of Toombs, McClain, and Kurakata discloses and renders obvious claim element 13[c]. Ex. 1003, ¶184.

B. Claim 26

1. Claim 26 [preamble]

Toombs and McClain disclose "[a] peripheral device configured for booting a bootable host device configured for being booted from an peripheral device, said peripheral device," as recited in Claim 26[preamble]. *See supra*, Section X.C.1 (Claim 20[preamble]). Kurakata also discloses a peripheral device (for example, an MMC card). Ex. 1008, Fig. 1.

2. Claim 26[a]

Toombs and McClain disclose "an MMC/SD-interface, comprising power terminals, a data bus with data bus terminals, a clock line with a clock terminal and a command line with command terminal," as recited in Claim 26[a]. *See supra*, Section X.C.2 (Claim 20[a]). Further, Kurakata also discloses an MMC card including an MMC interface with all the terminals recited in Claim 26[a]. *See supra*, Section XII.A.1 (Claim 13 [preamble]).

3. Claim 26[b]

Toombs and McClain disclose "a peripheral device controller, connected to said MMC/SD-interface," as recited in Claim 26[b]. *See supra*, Section X.C.3 (Claim 20[b]). Further, Kurakata discloses an MMC interface (for example, terminals P0-P6) that is connected to an interface unit 2 (including a host interface control unit 4, flash memory control unit 5, and control unit 7). Ex. 1008, 4:51-54,

Fig. 1. A POSA would recognize the interface unit 2 (including a host interface control unit 4, flash memory control unit 5, and control unit 7) to correspond to the "peripheral device controller." Ex. 1003, ¶187.

4. Claim 26[c]

Toombs and McClain disclose "a memory module, connected to said peripheral device controller," as recited in Claim 26[c]. *See supra*, Section X.C.4 (Claim 20[c]). Further, Kurakata discloses a flash memory 3 connected to the interface unit 2. Ex. 1008, 4:35-38, Fig. 1. A POSA would recognize this connection between the flash memory 3 and the interface unit 2 to disclose "a memory module, connected to said peripheral device controller," as recited in Claim 26[c]. Ex. 1003, ¶188.

5. Claim 26[d]

Claim 26[d] recites "wherein said peripheral device being configured for sending data starting with a start bit of a data transmission via said MMC/SD-interface to said host device, in case boot data are stored in the peripheral device, if and when receiving an argument for a boot request from said host device at said MMC/SD-interface of the peripheral device, and when receiving a clock signal at the clock line."

Toombs and McClain disclose "wherein said peripheral device being configured for sending data starting with a start bit of a data transmission via said MMC/SD-interface to said host device, in case boot data are stored in the peripheral device." *See supra*, Section XII.A.4 (Claim 13[c]).

Further, Toombs, McClain, and Kurakata disclose "receiving an argument for a boot request from said host device." *See supra*, XII.A.2 (Claim 13[a]). At least based on McClain's teaching that the boot code is read and sent to a host in response to a boot request, and based on Toombs, McClain, and Kurakata disclosing "receiving an argument for a boot request from said host device," a POSA would recognize that Toombs, McClain, and Kurakata disclose sending boot data to a host device if and when receiving an argument for a boot request. Ex. 1003, ¶191; Ex. 1006, 3:38-43, 3:43-46; 4:39-43 ("[T]he non-volatile memory 20 must be able to recognize that it is being selected to deliver code."). Accordingly, because Toombs and McClain disclose "wherein said peripheral device being configured for sending data starting with a start bit of a data transmission via said MMC/SD-interface to said host device, in case boot data are stored in the peripheral device," and because a POSA would recognize that Toombs, McClain, and Kurakata disclose sending boot data to a host device if and when receiving an argument for a boot request, it would be logical and obvious for

a POSA to implement sending data starting with a start bit of a data transmission via an MMC interface to a host device, in case boot data are stored in an MMC card, if and when receiving an argument for a boot request. Ex. 1003, ¶191.

Additionally, Toombs discloses that the clock line is provided for the MMC host to synchronize data transfer across the MMC bus. Ex. 1005, 7:41-47. *See also*, Ex. 1005, 6:21-24 (explaining the use of a clock signal for synchronizing data transfer). McClain also recognizes the need for a clock signal to indicate when a data value should be delivered. Ex. 1006, 1:38-40; *See also*, Ex. 1006, 4:53-55 (explaining that a boot signal could be asserted for several clock cycles or some otherwise relatively long period). Because Toombs and McClain disclose sending a clock signal to an MMC card to synchronize data transfer across the MMC bus, a POSA would recognize that Toombs, McClain, and Kurakata disclose sending data when receiving a clock signal at a clock line. Ex. 1003, ¶192. Accordingly, because Toombs and McClain disclose "wherein said peripheral device being configured for sending data starting with a start bit of a data transmission via said MMC/SD-interface to said host device, in case boot data are stored in the peripheral device" and because a POSA would recognize that Toombs, McClain, and Kurakata disclose sending data when receiving a clock signal at a clock line, it would be logical and obvious for a POSA to implement sending data starting with

a start bit of a data transmission via an MMC interface to a host device, in case boot data are stored in an MMC card, if and when receiving a clock signal at the clock line. Ex. 1003, ¶192.

Therefore, the combination of Toombs, McClain, and Kurakata discloses and renders obvious claim element 26[d]. Ex. 1003, ¶193.

C. Claim 42

Claim 42 recites that "said argument for a boot request comprises an argument for CMD0 command." Toombs, McClain, and Kurakata disclose "receiving during an initialization procedure of the peripheral device an argument for a boot request from said host device at said MMC/SD-interface of the peripheral device." *See supra*, Section XII.A.2 (Claim 13[a]). Because Kurakata discloses an MMC card that receives, during an initialization procedure of the MMC card, an initialization command CMD0 including an 8-bit command index, a 32-bit argument, and an 8-bit CRC code, a POSA would recognize that Toombs, McClain, and Kurakata disclose an argument for boot request comprising an argument for CMD0 command. Ex. 1008, 6:59-63; Ex. 1003, ¶194.

D. Claim 52

Toombs, McClain, and Kurakata disclose "wherein said peripheral device controller is further configured to receive an argument for a boot request

comprising an argument for CMD0 command." *See supra*, Section XII.C (Claim 42).

XIII. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests that a trial for *inter partes* review of the '487 Patent be instituted and that Claims 6, 7, 13, 20, 21, 26, 42, and 52 be rejected and canceled.

Dated: January 31, 2019

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR §42.24(a)(1)(i). This brief contains 13,979 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR §42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 2016, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR §42.6(a)(2)(ii) and typestyle requirements of 37 CFR §42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word 2016 in Times New Roman 14 point font.

Dated: January 31, 2019

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true copy of the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,739,487** and supporting materials (Exhibits 1001 - 1027 and Power of Attorney) have been served in its entirety this 31st of January, 2019, by e-mail and Federal Express on Patent Owner at the correspondence address for the attorney of record for the 7,739,487 Patent shown in USPTO PAIR, as well as on counsel for Patent Owner in the co-pending litigation:

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