UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC,
Patent Owner

Case No.: To Be Assigned
U.S. Patent No. RE45,542

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. RE45,542

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I. INTRODUCTION AND STATEMENT OF RELIEF REQUESTED (37 C.F.R. §42.22(a))

Kingston Technology Company, Inc. ("Petitioner" or "Kingston") hereby petitions to institute an *inter partes* review of Claims 18, 23-24, 28-29, 32-33, and 37-40 (the "Challenged Claims") of U.S. Patent No. RE45,542 (the "RE542 Patent") to Mylly (Ex. 1001), and cancel those claims as unpatentable.

As discussed below, the prior art anticipates and/or renders obvious the Challenged Claims under 35 U.S.C. § 102 and/or § 103. Accordingly, there is a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim, and Petitioner respectfully requests that the Board institute a trial for *inter partes* review and cancel all Challenged Claims as unpatentable.

II. MANDATORY NOTICES (37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner Kingston Technology Company, Inc., is a real party-in-interest. Petitioner's parent company, Kingston Technology Corporation ("Kingston Holding"), is a holding company without any employees or operations. However, because Kingston Holding is the sole owner of Petitioner and shares some directors, Petitioner identifies Kingston Holding as an additional real party-in-interest.

B. Identification of Related Matters (37 C.F.R. § 42.8(b)(2))

Patent Owner Memory Technologies, LLC ("MTL") has asserted the Challenged Claims of the RE542 Patent, as well as claims from seven other patents, against Kingston in a co-pending litigation, *Memory Technologies, LLC v. Kingston Technology Co., Inc*., 8:18-cv-00171 (C.D. Cal.). MTL's original Complaint was filed on January 31, 2018, and served, at the earliest, on February 1, 2018.

In addition to this Petition, Kingston has or will be filing petitions for *inter partes* review of the other seven patents that MTL has asserted against it.

C. Lead and Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner designates the following Lead and Backup Counsel. Concurrently filed with this Petition is a Power of Attorney for appointing the following Lead and Backup Counsel, per 37 C.F.R. § 42.10(b). Service via hand-delivery may be made at the postal mailing addresses below. Petitioner consents to electronic service by e-mail at the following address: **Kingston-RE542ipr@pillsburylaw.com**.

Lead Counsel	Back-Up Counsel
Robert C.F. Pérez (Reg. No. 39,328) PILLSBURY WINTHROP SHAW PITTMAN LLP 1650 Tysons Boulevard, 14th Floor McLean, VA 22101 Telephone: 703.770.7900 Facsimile: 703.770.7901	**Christopher Kao**, Kingston's counsel in the co-pending litigation (*Pro hac vice* motion to be filed) **Brock S. Weber**, Kingston's counsel in the co-pending litigation (*Pro hac vice* motion to be filed) PILLSBURY WINTHROP SHAW PITTMAN LLP Four Embarcadero Center, 22nd Floor San Francisco, CA 94111 Telephone: 415.983.1000 Facsimile: 415.983.1200

D. Payment of fees (37 C.F.R. §42.103)

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 033975 for the petition fee and for any other required fees.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Identification of Challenge (37 C.F.R. § 42.104(b))

Pursuant to 37 C.F.R. §42.104(b), Petitioner requests that Claims 18, 23-24, 28-29, 32-33, and 37-40 of the RE542 Patent be cancelled as anticipated or rendered obvious based on the following grounds:

Ground	RE542 Patent Claims	Basis for Rejection
1	18, 23, 28-29, 32-33, 37, 38, and 40	§ 102 based on Garner
2	18, 23-24, 28-29, 32-33, and 37-40	§ 103 based on Garner and Toombs

The Declaration of Jacob Baker, Ph.D., P.E, filed herewith (Ex. 1002, "Baker Decl."), supports the challenge in this Petition that the Challenged Claims are invalid as anticipated and obvious

B. Patents and Publications Relied Upon

U.S. Patent No. 5,724,592 ("Garner"), entitled "Method and Apparatus for Managing Active Power Consumption in a Microprocessor Controlled Storage Device," was filed on December 5, 1996 and issued March 3, 1998. Garner is prior art under at least 35 U.S.C. §§ 102(a), 102(b) and 102(e). Garner was not previously presented to the PTO in the context of the RE542 Patent.

U.S. Patent No. 6,279,114 ("Toombs"), entitled "Voltage Negotiation in a Single Host Multiple Cards System," was filed on November 4, 1998 and issued August 21, 2001. Toombs is prior art under at least 35 U.S.C. §§ 102(a) and 102(e).

IV. BACKGROUND OF THE TECHNOLOGY

Generally, the RE542 Patent relates to power management of peripheral devices, such as memory cards. (Ex. 1002, ¶¶73-74.) A memory card is a device for storing electronic data. (*Id.*, ¶75.) By 2002, several types of memory cards that use flash or EEPROM memory were in existence, including MultiMediaCard, CompactFlash, and PCMCIA memory cards. (*Id.*, ¶76.)

A memory card typically relies on a host electronic device (*e.g.,* laptop) to which it is connected for power. (*Id.*, ¶77.) Different hosts may have different power-supply restrictions or preferences, and different memory cards may have different power needs. (*Id.*) Because memory cards were intended to work with a variety of hosts, the issue of compatibility between hosts and memory cards was well-recognized by 2002. (Ex. 1007, 1:48-62; Ex. 1008, 1:36-56.) A well-known solution to the problem was to allow hosts and memory cards to negotiate the desired operating configuration. (Ex. 1002, ¶78.) For example, a host may read the configuration options supported by a memory card and cause the card to operate in a selected option. (Ex. 1007, 2:12-20, Ex. 1008, 15:42-49.)

Power management circuits have been used by memory devices since at least the 1970s. (Ex. 1002, ¶79.) A well-known power-management technique was for hosts to specify a mode of operation for memory cards, which in turn affects the operational configuration of the memory cards. (*Id.*, ¶80.) Memory cards capable of operating in different modes typically start at a default mode and change to a different mode upon request or meeting triggering conditions. (*Id.*, ¶81-82.)

Power consumption, which is often measured in Watt-Hours, refers to the amount of energy that is consumed or used over a period of time. (*Id.*, ¶85.)

Limiting the rate at which power is used would, in effect, limit power consumption. (*Id.*)

Well-known operational configurations that limit power consumption include, *e.g.,* clock frequency, bus width, and operating voltage/current. (*Id.*, ¶¶86-89.) For example, a low clock frequency limits power consumption lower than a higher frequency. (*Id.,* ¶¶90-91.)

V. OVERVIEW OF THE RE542 PATENT

A. Summary of the Claimed Subject Matter

The RE542 Patent claims foreign priority to Finnish Patent Application No. 20020594, filed March 27, 2002. The RE542 Patent is directed to methods and systems for determining and managing power consumption of a peripheral device (*e.g.,* MultiMediaCards). (Ex. 1002, ¶93.) According to the patent, the described solution is needed to address power-consumption compatibility issues between peripheral devices and the variety of host electronic devices to which they can connect. (Ex. 1001, 1:61-2:4.) An illustrative embodiment of the RE542 Patent is shown in Figure 2.

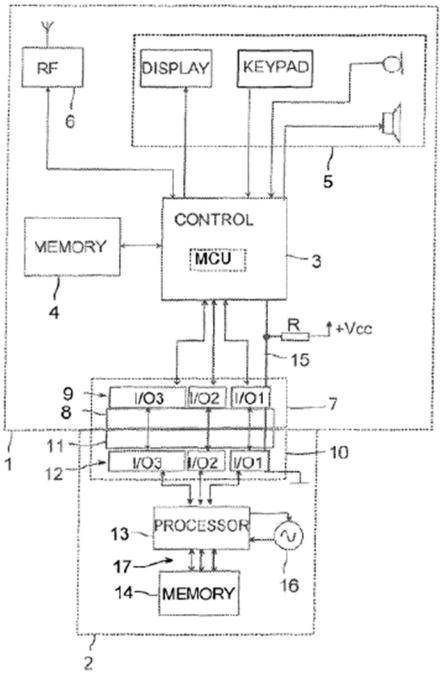

Fig 2

Figure 2 shows a peripheral device 2 connected to an electronic device 1 that supplies power to the peripheral device. (*Id.*, 4:41-48.) The peripheral device comprises a connector 10 for connecting the peripheral device to the electronic device. (*Id.*, 4:41-43.) The peripheral device also comprises "a processor 13 or the like for controlling the functions of the peripheral device 2," and a clock generator 16 for generating clock signals for the processor. (*Id.*, 4:57-59, 5:1-4.) Further, the peripheral device comprises a memory 14 for storing program code and data, including "a first maximum value and a second maximum value for power consumption," with the first maximum value being lower than the second. (*Id.*,

4:65-5:1, 5:31-32.) In one embodiment, the two values define a range from which to select. (*Id.*, 7:31-34.)

The RE542 Patent describes an embodiment where "the suitable power consumption value can be negotiated by the electronic device and the peripheral device." (*Id.*, 9:27-31.) The operations performed by the devices are discussed with reference to Figure 3, copied below.

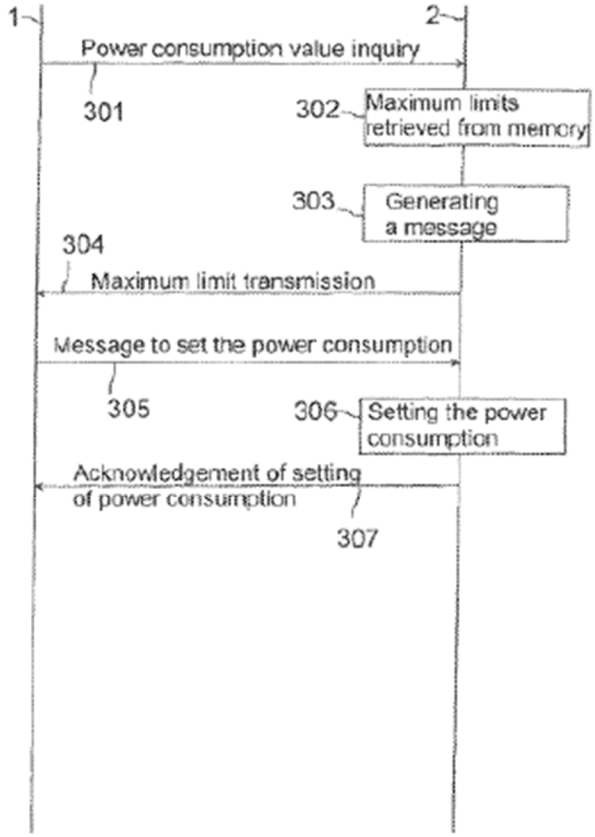

Fig 3

During startup, the power consumption of the peripheral device is set to a default value, and the processor also sets the clock generator to a frequency that corresponds to this power consumption value. (*Id.*, 5:26-34, 7:23-25.) Thereafter, the host electronic device queries the peripheral device for its first and second maximum power consumption values. (*Id.*, 5:48-54, Fig. 3, label 301.) In response, the peripheral device reads the requested values from memory (Fig. 3, label 302), generates a reply message containing the values (label 303), and sends the message to the host (label 304). (*Id.*, 5:56-6:5.) The host then selects from the received values and sends a "power control message indicat[ing] the power consumption value which is to be set as the maximum value for the peripheral device" (label 305). (*Id.*, 6:6-17.) Upon determining that the message is a power control message, the processor of the peripheral device "reads the maximum value for power consumption indicated in the message (block 306)." (*Id.*, 6:17-21.) Thereafter, the processor sets the clock frequency and/or bus width to a value corresponding to the maximum value for power consumption. (*Id.*, 6:21-27.) Other possible configuration adjustments include setting the operating voltage, current consumption, bus frequency, and operating mode (*e.g.,* "active mode" or "power-saving mode") of memory banks. (*Id.*, 8:1-39.)

The RE542 Patent recognizes that several operational configurations that effectively limit a peripheral device's power consumption were well-known in the art. For example, in its background section, the RE542 Patent described power consumption being affected by clock frequency and bus width. (*Id.*, 2:49-59.) Additionally, the RE542 Patent stated that "it should be evident that other methods for adjusting power consumption are also known," such as by controlling operating voltage and current consumption. (*Id.*, 7:64-8:10.)

As explained below, the techniques disclosed in the RE542 Patent were also well-known in the prior art. (Ex. 1002, *Sections VII*, and *VIII*.)

B. Prosecution History of the RE542 Patent

The RE542 Patent claims priority to a Finnish patent application, No. 20020594, filed on March 27, 2002. On March 26, 2003, the Applicant filed U.S. Patent Application No. 10/401,338 ("'338 Application") (Ex. 1004). The '338 Application issued as U.S. Patent No. 7,278,033 ("'033 Patent") on November 2, 2007 (Ex. 1005). On May 24, 2013, the Applicant sought reissue of the '033 Patent and filed Application No. 13/902,227 ("'227 Application") (Ex. 1006). The resulting RE45,542 Patent (Ex. 1001) issued on June 2, 2015.

The prosecution history of the '338 Application clarifies the origin of the claim limitation, "a default value and a limiting value," as recited in Claim 28 of

the RE542 Patent. On June 26, 2006, the Applicant amended the claims to replace "first maximum value" and "second maximum value" with "first maximum limiting value" and "second maximum limiting value," respectively. (Ex. 1004, p. 291-297.) The amendment was advanced with an argument that the cited prior art did not teach a "maximum power consumption" set between two limiting values. (*Id.*, p. 298.) The Examiner rejected the claims because the words "maximum" and "limit" were superfluous or confusing, since "by the applicant's own admission, these values are merely limiting values for the maximum value, and not the maximum value themselves." (*Id.*, p. 312.) Accordingly, the Examiner recommended that the terms be amended to recite a first and second "limiting value for the power consumption." (*Id.*) In response to this rejection, the Applicant replaced "first maximum limiting value" and "second maximum limiting value" with "default value" and "limiting value," respectively. (*Id.*, p. 321-327.)

The prosecution history of the reissuance of the RE542 Patent is particularly relevant to the means-plus-function element and the "maximum power consumption" element. The reissue application added the dependent claims at issue in this IPR and sought to add the following limitation to independent Claim 28: "wherein the means for setting the maximum power consumption includes a processor configured to read an indication of the value from the received

information and to set the maximum power consumption to the value based on the indication." (Ex. 1006, p. 38-40.) The Applicant cited to "6:12-25" as the alleged support for this limitation. (*Id.*, p. 41.)

With respect to the means-plus-function term, the Examiner rejected the added limitation because "processor" specified a structure for the recited function and therefore did not comply with Section 112 ¶6. (*Id.*, p. 231-32.) In response, the Applicant replaced the added limitation with the language that ultimately issued, which removed "processor," and added Claim 38, which specified a processor as the means-plus-function element in Claim 28. (*Id.*, p. 259, 261.)

With respect to the term, "maximum power consumption," the Examiner found it indefinite because the usage of "maximum" conflicts with its ordinary meaning. (*Id.*, p. 231.) The Examiner reasoned that since "maximum power consumption" is set to a value between the default and limiting values, it is not actually a "maximum." (*Id.*) In response, the Applicant submitted a declaration from the inventor, Kimmo Mylly, to explain that "maximum" is a limit on power consumption. Citing to the declaration, the Applicant explained:

> A POSA ("person having ordinary skill in the art at the time of filing the application") would understand that "maximum" as recited, at least "relates to a maximum limit on the fluctuating power consumption of a peripheral device." (Mylly Decl. ¶8.) "[A POSA] recognized that the power consumption of a peripheral device

> fluctuated over the course of its operation. As a result, the 'maximum power consumption' recited in the claims related to a limit on the fluctuating power consumption of the peripheral device." (*Id.,* ¶12.)

(*Id.*, p. 266-267.)

VI. CLAIM CONSTRUCTION (37 C.F.R. § 42.104(b)(3))

The Patent Office has adopted a rule by which claims are construed in accordance with "the standard used in federal courts, in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), which is articulated in *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005)." 83 FR 51340. Under this standard, claim construction begins with the language of the claims. *Phillips*, 415 F.3d at 1312-14. The "words of a claim are generally given their ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id*. at 1312-13. The specification is "the single best guide to the meaning of a disputed term and . . . acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication." *Id*. at 1321 (internal quotation marks omitted). The prosecution history is another source of intrinsic evidence. *Id*. at 1317.

All claim terms of challenged claims of the RE542 Patent have been accorded their plain and ordinary meaning as understood by person of ordinary skill in the art and consistent with the intrinsic record. Petitioner's interpretation of the claim terms in the RE542 Patent is further explained for each claim limitation in relation to the prior art discussed in the proposed grounds for invalidity, below, in Grounds 1 and 2.

Under the *Phillips* standard and for clarity, Petitioner provides the following specific constructions.[1]

A. "peripheral device"

The specification of the RE542 Patent discloses that a peripheral device can be connected to an electronic device (*e.g.,* laptops) and "expand the properties of the electronic device and to produce auxiliary functions." (Ex. 1001, 1:44-53; Ex. 1002, ¶141.) The disclosed examples of peripheral devices include internal devices (*e.g.,* memory cards and PCMCIA cards) and external devices (*e.g.,* cameras). (Ex. 1001, 1:47-60, 4:20-28, 9:55-61; Ex. 1002, ¶¶142-43.) Further, the recited "peripheral device" should at least be broad enough to cover memory cards,

[1] Petitioner reserves the right to address any claim construction positions taken by the Patent Owner in its Preliminary Response, if any, including under 37 C.F.R. § 42.108(c). Petitioner further reserves its ability to show that claims of the RE542 Patent are invalid under 35 U.S.C. §112 in the co-pending litigation, despite offering explicit and implicit claim constructions herein.

as recited in dependent Claims 32 ("the peripheral device is a memory card") and 39 ("the memory card is a MultiMediaCard"). (Ex. 1002, ¶¶144-46.) Accordingly, a person of ordinary skill in the art at the time of the alleged invention ("POSITA") would understand the term "peripheral device" to mean "an internal or external device capable of expanding the properties of or produce auxiliary functions for a connected electronic device." (*Id*., ¶147.)

B. "default value"

Claims 18 and 28 recite in relevant part: (1) "a memory storing a default value ... for power consumption of the peripheral device" and (2) "a maximum power consumption of the peripheral device is set at a startup stage to said default value." Accordingly, the "default value" is at least a power consumption value to which the "maximum power consumption" is set. (Ex. 1002, ¶149.)

In addition, the ordinary meaning of "default" is "an adopted preselected option when no alternative has been specified," which is consistent with the term's usage in the specification. (*Id*., ¶150.) The specification states that during initialization of the peripheral device, "the power consumption of the peripheral device 2 is set to a default value which ... is a power consumption value according to the first maximum limit." (Ex. 1001, 5:25–31.) This initialization corresponds to the claimed "startup stage." (Ex. 1002, ¶150.) Further, the specification states

that unless the host subsequently selects a different value, the corresponding power consumption configurations need not be adjusted "because this value is the default value." (Ex. 1001, 6:59-62.) This implies that the default value is preselected to be set as the peripheral device's "maximum power consumption." (Ex. 1002, ¶150.)

The specification and claims do not specify or restrict the "default value" and "limiting value" to any particular type of measurement. Both values are "for power consumption of the peripheral device." (Ex. 1001, cl. 28; cls. 33, 37.) However, there is no requirement that the power consumption value be, *e.g.,* a specific clock frequency or any measure of power consumption (*e.g.,* Watt-Hours). (Ex. 1002, ¶80.) The specification and claims only state that the clock can be adjusted to a frequency that corresponds to the power consumption value, maximum limit, or other similar terms. (Ex. 1001, 5:32-34, 6:21-25, 14:18-22, cl. 31.) The exact nature of the "power consumption value" is not specified. Thus, the "default value" should not be limited to any particular type of measurement.

Accordingly, a POSITA would have understood "default value" to mean "a preselected power consumption value to which the 'maximum power consumption' of the peripheral device is set when no alternative has been specified." (Ex. 1002, ¶151.)

C. "limiting value"

Claims 18 and 28 recite in relevant part: (1) "a memory storing a ... limiting value for power consumption of the peripheral device"; (2) "said limiting value ... is defined for the power consumption of the peripheral device"; and (3) "setting the maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value." Accordingly, the "limiting value" is at least a power consumption value to which the "maximum power consumption" can be set. (Ex. 1002, ¶152.)

The term "limiting value" does not appear in the specification, but the prosecution history of the RE542 shows that it evolved from "second maximum value." (Ex. 1004, pp. 25-29, 291-97, 321.) In response to a rejection stating that the word "maximum" in "second maximum value" "lack[s] any significant meaning," the Applicant replaced the element with "second maximum limiting value" and argued that the "first value and the second value are limiting values for the maximum, the maximum being not yet set." (*Id.* pp. 280, 291-98). After the Examiner maintained his position that then-recited elements are not actually "maximum" values, the Applicant deleted the word "maximum" and replaced "second maximum limiting value" with "limiting value." (*Id.* pp. 312, 321.) In the

specification, the "second maximum limit" (or similar terms) is "the power consumption value which is to be set as the maximum value for the peripheral device[.]" (Ex. 1001, 6:14-17.)

As discussed *supra* in Section *VI.B*, the specification and claims do not specify or restrict the "limiting value" or power consumption values in general to any particular type (*e.g.,* there is no requirement that it be a clock frequency or power consumption measurement). Thus, the "limiting value," similar to the "default value," should not be limited to any particular type of measurement.

While Claims 18 and 28 restrict the "limiting value" to be "higher than said default value," there is no requirement in Claim 28 for it to be the highest, which is a limitation added by dependent Claim 33. (Ex. 1002, ¶¶158-59.) The specification states that there may be "more than two different maximum limits" (Ex. 1001, 7:31-33), which implies the possibility of having intermediate values between the lowest and highest values. (Ex. 1002, ¶159.) Thus, the "limiting value" need not be the highest; it only needs to be higher than the "default value" as recited in Claim 28.

Accordingly, a POSITA would have understood "limiting value" to mean "a power consumption value (1) to which the 'maximum power consumption' of the peripheral device can be set and (2) is higher than the 'default value.'" (*Id*., ¶160.)

D. "maximum power consumption of the peripheral device"

A POSITA would have recognized that the RE542 Patent describes an approach for limiting power consumption of a peripheral device that involves: (1) setting the peripheral device's maximum power consumption to a desired value and (2) adjusting operational configurations, such as clock frequency and bus width. (Ex. 1002, ¶163.) For example, the specification states that in addition to setting the power consumption value, the clock frequency or bus width is "also" set (Ex. 1001, 5:25-34, 3:45-54) or "[n]ext" set (*Id*., 6:17-25, Fig. 3.). These operations are reflected in the claims, which recite that the "maximum power consumption of the peripheral device" (1) is set to the "default value" and can be set to "a value," (*see* Claim 28), and (2) the clock generator can be set to a "first frequency corresponding to the maximum power consumption of the peripheral device" (Claim 31).

A POSITA would understand that the term "maximum power consumption of the peripheral device" refers to a setting (*e.g.,* a configuration parameter) of the peripheral device because it is repeatedly described as being set to a desired value. (Ex. 1002, ¶164.) For example, Claims 18 and 28 recite that the "maximum power consumption of the peripheral device is set at a startup stage to said default value" and that the "means for setting the maximum power consumption of the peripheral

device to a value" is configured to "set the maximum power consumption of the peripheral device to the value." (Claim 38.) The specification similarly states: "Signaling between the electronic device and the peripheral device sets a maximum value for the power consumption of the peripheral device which is between said first and second maximum values." (Ex. 1001, Abstract; *see also*, *e.g.,* 2:67-3:39, 3:48-52, 5:25-32, 6:14-17, 6:31-38, 6:45-49, 7:21-25, 8:61-64, 9:10-18, Fig. 3.)

The specification states that after the processor determines that a received message is a power control message, it "reads the maximum value for the power consumption indicated in the message (block 306)." (Ex. 1001, 6:17-21.) The referenced "block 306" is labeled in Figure 3 as "Setting the power consumption." According to Dr. Baker, "in this particular description the power consumption of the device is set when the processor processes and recognizes the received maximum value." (Ex. 1002, ¶165.) In another example, the specification states that the processor sets the "power consumption of the peripheral device" to a "power consumption value," and "also sets the frequency of the clock generator 16 to correspond to this power consumption value." (Ex. 1001, 5:25-34.) A POSITA would reasonably interpret this to encompass a scenario where the power consumption value is stored in memory or a register. (Ex. 1002, ¶165.) Thus,

according to Dr. Baker, a POSITA would reasonably understand that "the maximum power consumption could be set in any conventional manner, such as writing the specified value into a particular register/memory or processing and recognizing a value specified in a control message." (*Id.*)

Further, a POSITA would recognize that the value of the maximum power consumption is not limited to any particular type (*e.g.,* Watt-Hours, frequency, and bus width). (Ex. 1002, ¶166.) The specification has broadly characterized the power consumption of the peripheral device being set to a "level" and a "less power consuming state" in response to an electronic device operating "in a power saving mode." (Ex. 1001, 9:10-18, 7:14-20.) Further, the specification states that both clock frequency and bus width can be changed according to the same maximum power consumption limit. (Ex. 1001, 6:21-27, 9:1-4.) This is further evidence that the "maximum power consumption" can be a generic value since it can affect two different types of operational configurations (i.e., clock frequency and bus width).

The prosecution history further shows that "maximum power consumption" does not have to be the actual power-consumption limit (*e.g.,* specified in Watt-Hours), but can be any value that effectively (even indirectly) sets a limit on power consumption. (Ex. 1002, ¶167.) During prosecution, the Applicant submitted a

declaration from the inventor of the RE542 Patent, who stated that "the 'maximum power consumption' recited in the claims relates to a maximum limit on the fluctuating power consumption of a peripheral device," which may be limited by, *e.g.,* clock frequency. (*Id*.) According to Dr. Baker, a POSITA would reasonably interpret this statement to mean that a maximum power consumption value "either directly or indirectly affects the actual power consumption of the peripheral device to be within a limit." (*Id*.)

The value of the "maximum power consumption" affects how the peripheral device subsequently adjusts its operational configurations (*e.g.,* clock frequency) to stay within the limit. (Ex. 1002, ¶168.) For example, once the maximum power consumption is set to a value, the processor adjusts the clock frequency to correspond to that value. (Ex. 1001, 5:25-34, 6:14-27, 7:52-63, cl. 31.) Other operational configurations that may be configured according to the maximum power consumption value include bus width, operating voltage, among others. (*Id*., 6:25-27, 7:44-8:49; Ex. 1002, ¶169.)

Any of these operational configurations set according to the maximum power consumption in turn limits the power consumption of the peripheral device during operation. (Ex. 1002, ¶¶86-91, 168.) The specification explains that clock frequency and bus width (Ex. 1001, 2:49-59, 7:35-51), among other operational

configurations (*Id*., 7:64-8:43), affect power consumption. The inventor of the RE542 Patent stated in a declaration that a POSITA would have recognized that "the 'maximum power consumption' recited in the claims relates to a maximum limit on the fluctuating power consumption of a peripheral device." (Ex. 1006, p. 270.) The inventor explains:

> The skilled artisan knew that a memory device approached maximum power consumption at a particular clock frequency when it performed the most power-demanding operations (*e.g.,* writing multiple banks at the same time). Conversely, power consumption at that frequency setting would fluctuate below the maximum power consumption when the device performed less demanding operation (*e.g.,* accessing only one memory bank at a time).

(*Id*., p. 271.)

As explained in Dr. Baker's declaration, because the clock frequency establishes a rate at which power can be consumed (similar to a lightbulb's wattage), the maximum power that can be consumed over the time period (*e.g.,* Watt-Hours) is limited. (Ex. 1002, ¶¶86-87.) A POSITA would have known that by affecting the operational configurations, the "maximum power consumption" would effectively limit the actual power consumption of the peripheral device. (*Id*., ¶¶86-89, 171.)

Accordingly, a POSITA would understand that this limitation means "a setting by which the peripheral device limits (directly or indirectly) its power consumption." (*Id*., ¶173.)

VII. LEVEL OF ORDINARY SKILL IN THE ART

The RE542 Patent relates to the field of power management systems for managing power consumption of peripheral devices, such as memory cards. (Ex. 1002, ¶71.) A POSITA "would be a person with a bachelor's or master's degree in electrical engineering or a closely related field and two to three years of academic or industry experience in the field of memory system design." (*Id.*) Someone with less technical education but more practical experience or vice versa may also meet this standard. (*Id.*)

VIII. BRIEF DESCRIPTION OF PRIOR ART RELIED UPON

A. Overview of Garner (U.S. Patent No. 5,724,592)

Garner discloses a flash memory system capable of being placed in different power-expending modes by a host device. (Ex. 1007, 2:12-19.) To address compatibility issues between hosts and storage devices, Garner aims to "allow storage devices to function with all of these possible systems in the power ranges available to each of these systems." (*Id.*, 1:48-59, 4:40-45.)

In one embodiment, Garner describes a microprocessor-controlled flash memory storage device 15, shown in Figure 2.

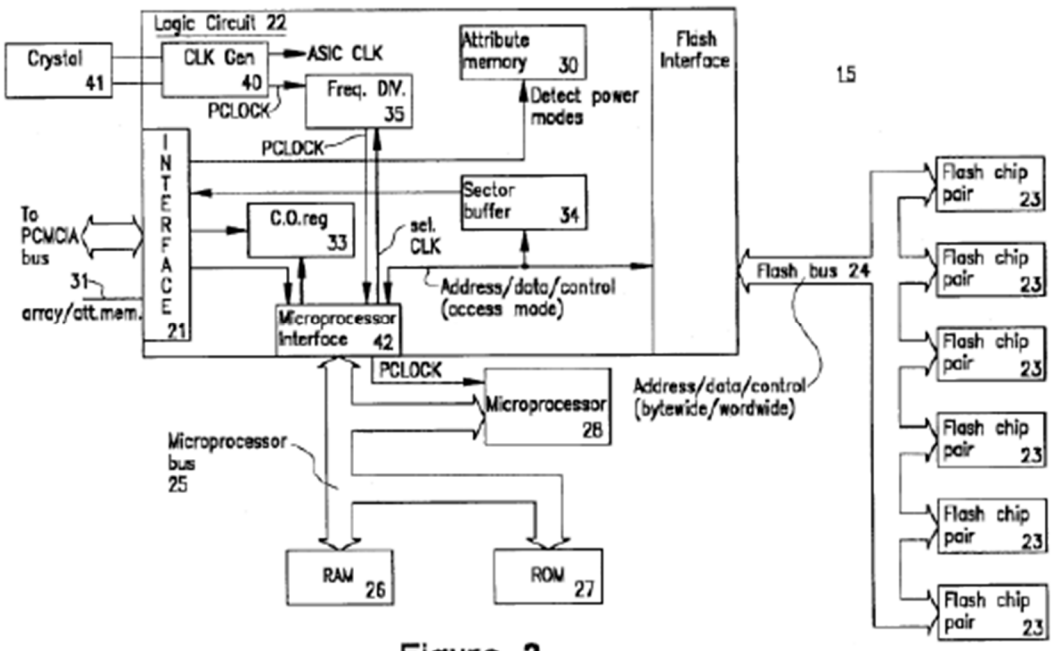

Figure 2

The storage device is configured to connect to and obtain power from a host digital device (*e.g.,* computer). (*Id.*, 4:36-45, Fig. 1.) The storage device connects to the host through interface 21, PCMCIA bus, and PCMCIA bridge circuit 16 (shown in Fig. 1). (*Id.*, 3:26-33, 3:57-58.) Incoming signals are decoded by the interface and processed by logic circuit 22, which is "assisted in its operation by a microprocessor 28." (*Id.*, 3:59-4:16.)

In one embodiment, the storage device can operate in four different power modes "which use progressively less power," including a "lowest power mode"

and a "highest power mode." (*Id.*, 5:3-31.) The available power modes are stored in attribute memory 30 and may be represented by two-bit "power tuples." (*Id.*, 5:12-15.)

In operation, the host can selectively place the storage device in a power mode supported by the device. The storage device starts up in a default mode, and in one embodiment it "always powers up in the lowest power mode." (*Id.*, 5:26-31, 6:48-51.) The storage device is configured such that the host can read its attribute memory and select any of the four available power modes. (*Id.*, 5:15-21.) The host then writes its power-mode selection into, *e.g.,* configuration options register 33. (*Id.*, 5:19-26.) Based on the host's selection, the storage device then configures, *e.g.,* its clock frequency and/or data-access bandwidth. (*Id.*, 5:41-6:15.) For example, the four power modes correspond to 16MHz, 8MHz, 4MHz, and 1MHz, respectively. (*Id.*, 5:50-60.) Garner further explains that clock frequency and data-access bandwidth affects how much power is expended. (*Id.*, 5:46-50, 5:66-6:3.)

B. Overview of Toombs (U.S. Patent No. 6,279,114)

Toombs discloses a MultiMediaCard flash memory device capable of operating in a voltage range selected by a host. (Ex. 1008, 1:51-56, 16:21-25.)

The invention addresses the problem of voltage compatibility between one or more memory cards and the host to which they are connected. (*Id.*, 1:51-56.)

An embodiment of a MultiMediaCard is shown in Figure 14:

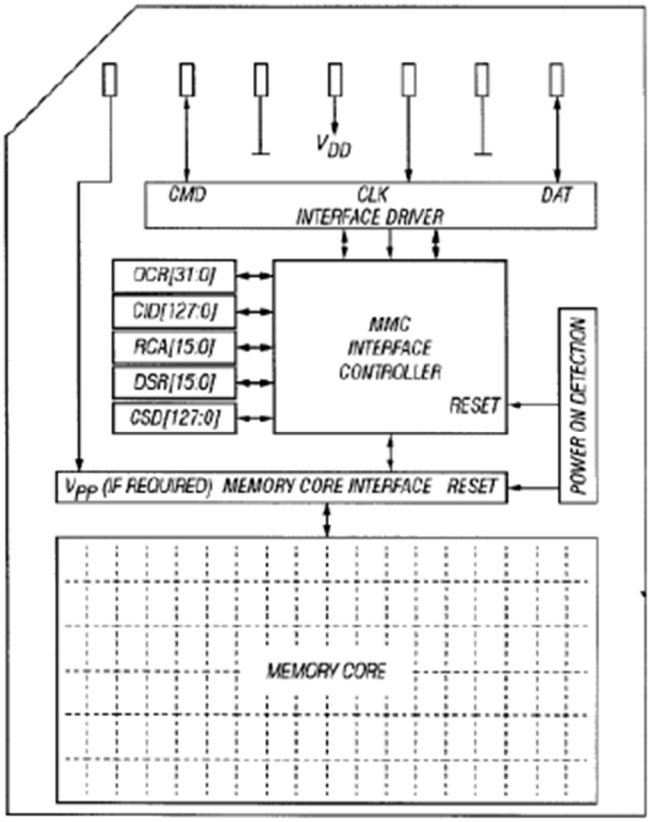

FIG. 14

The MultiMediaCard is designed to connect a host device through its connector pins. (*Id.*, Fig. 1; Ex. 1002, ¶186.) Figure 14 shows several connector pins on the top edge of the MultiMediaCard, including power supply pins (*e.g.,* V_{DD} and V_{PP}) and communication pins (*e.g.,* CMD and DAT). (Ex. 1008, 7:32-44; Ex. 1002, ¶186.) Figure 14 further shows that CMD and DAT signals are passed

from the Interface Driver to the MMC Interface Controller for processing. (*Id.*) As shown, the Controller has exclusive access to the registers, which means the host cannot read/write to the registers directly. (*Id.*)

Toombs discloses a MultiMediaCard capable of negotiating an operating voltage with a host. (Ex. 1008, 15:22-24, 16:21-25.) The MultiMediaCard stores its operating voltage range (including "minimum and maximum operating values") in its OCR register. (*Id.*, 15:27-38, 15:66-16:9, Fig. 15.) During voltage negotiation with the host, the host queries the MultiMediaCard for its operating voltage range by sending a command. (*Id.*, 15:42-16:20, Fig. 38A.) "After a common operating voltage is determined by the host, the host sends the determined VDD voltage window as an operand of the command SEND_OP_COND (CMD1). In response to this command, each of the active cards will define its OCR register value according to this voltage." (*Id.*, 16:21-25.)

IX. CLAIM-BY-CLAIM EXPLANATION OF GROUNDS OF UNPATENTABILITY

All of the Challenged Claims are unpatentable as explained below.

A. GROUND 1: Garner anticipates Claims 18, 23, 28-29, 32-33, 37, 38, and 40 under § 102.

1. Independent Claim 18

a. 18 (preamble) "A peripheral device comprising:"

To the extent the preamble is limiting, Garner teaches it. (Ex. 1002, ¶¶190-93.) "Peripheral device" should be construed as discussed in *Section VI.A*, *supra*.

Garner discloses a memory or storage device 15 that provides "storage functions" to a host digital device. (Ex. 1007, 1:34-37, 1:48-52, 3:54-57, 4:49-52.) Figures 1 and 2 of Garner show storage device 15 being connected through PCMCIA to the host's "peripheral component interface (PCI) bus." (*Id.*, 3:18-21, emphasis added.) This is similar to the RE542 Patent's description of a peripheral device being a PCMCIA card for memory expansion. (Ex. 1001, 1:47-53; Ex. 1002, ¶191.) Thus, Garner's storage device teaches this element.

b. 18(a) "a memory storing a default value and a limiting value for power consumption of the peripheral device;"

Garner teaches this limitation. (Ex. 1002, ¶¶194-98.) A "default value" and a "limiting value" should be construed as discussed in *Sections VI.B* and *C*, *supra*.

The storage device 15 in Garner comprises an attribute memory 30 that stores four "power-expending modes" which "use progressively less power," including a "lowest power mode" and a "highest power mode." (Ex. 1007, 2:11-

19, 5:12-19, 5:26-31; Ex. 1002, ¶195.) The power modes may be stored in the attribute memory as two-bit "power tuples." (Ex. 1007, 5:12-25.) Alternatively, instead of power modes, it would have been obvious to a POSITA that power consumption values (*e.g.,* in power/energy units) corresponding to the power modes can be stored. (Ex. 1002, ¶195.) It would have been an obvious design choice to store either power modes or power consumption values to achieve the same functional purpose of informing a host of the different power configurations supported by the storage device. (*Id.*) Discussions hereinafter relating to Garner's power modes apply equally to corresponding power consumption values. The selected power mode (or power consumption value) for the storage device limits power consumption of the storage device by causing corresponding adjustments to, *e.g.,* the clock frequency. (Ex. 1007, 5:40-61; Ex. 1002, ¶196.)

The power mode of the storage device can be set to any one of the supported power modes, including the highest and the lowest. (Ex. 1007, 5:19-29.) The "storage device always powers up in the lowest power mode," and can be subsequently changed by the host to a different mode, such as the highest power mode. (Ex. 1007, 6:40-57, 5:25-31.) The lowest and highest power modes teach the "default value" and "limiting value," respectively. (Ex. 1002, ¶197.) Thus, Garner teaches this limitation.

c. 18(b) "means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,"

Petitioner Kingston and Patent Owner have agreed in the related litigation involving this patent that this phrase is a means-plus-function term and have agreed that the function is, "connecting the peripheral device to an electronic device for supplying power to the peripheral device," and have agreed that the structure is "connector 11 of FIG. 1 and FIG. 2, 4:43-48" of the RE542 Patent, "and structural equivalents thereof." (Ex. 1010 at 1.) Garner discloses this function and structure. (Ex. 1002, ¶¶199-205.)

The storage device 15 can connect to a host (*e.g.,* computer), which supplies power to the storage device. (Ex. 1007, 1:34-59, 2:7-19; Ex. 1002, ¶201.) The storage device connects to the host through interface 21, PCMCIA bus 17, and PCMCIA bridge circuit 16. (*Id.*, 1:48-59, Figs. 1, 2; Ex. 1002, ¶199.) Any one or more of the interface, PCMCIA bus, and PCMCIA bridge circuit disclose the "connector" shown and described in the RE542 Patent at FIGs. 1 and 2, and 4:43-48, for connecting the peripheral device to an electronic device, "as they perform the same exact function in the same way to supply power to the peripheral device." (Ex. 1002, ¶200.)

Further, because the host supplies power to the storage device and the two are connected through the interface, PCMCIA bus, and PCMCIA bridge circuit, a POSITA would have recognized that these components must be the connector conduit for supplying power to the storage device. (Ex. 1002, ¶202.) In addition, a POSITA would have recognized that PCMCIA connectors, as disclosed in Garner, are capable of supplying power to and commonly did supply power to PCMCIA memory cards. (*Id.*)

Therefore, Garner discloses this limitation. (*Id*., ¶¶199-205.)

d. 18(c) "wherein the power consumption of the peripheral device is set at a startup stage to said default value,"

Garner teaches this limitation. (Ex. 1002, ¶¶206-214.)

Garner discloses that the power mode of the storage device 15 can be set to any of the four supported power modes to limit power consumption of the storage device. (Ex. 1002, ¶206.) In particular, Garner discloses that power tuples stored in a register (*e.g.,* bits 4 and 5 of configuration options register 33) designate the device's power mode. (Ex. 1007, 5:22-26.) Alternatively, a POSITA would have recognized that an alternative design choice is to store a corresponding power consumption value instead of a power mode to achieve the same function of indicating a desired configuration (hereinafter, discussions relating to storing a

desired power mode applies equally to storing a corresponding power consumption value). (Ex. 1002, ¶¶206-07.) The power mode reduces "the power used by components of the flash EEPROM memory arrays to a level compatible with a particular host system." (Ex. 1007, 2:7-10.) This is accomplished by the microprocessor testing "the state of the bits 4 and 5 in the configurations register 33 and run[ning] the appropriate setup process," such as adjusting the clock frequency and/or data-access bandwidth. (Ex. 1007, 5:32-6:15; Ex. 1002, ¶209.) This in turn limits power consumption, as explained by Dr. Baker (Ex. 1002, ¶¶152-56, 209-10), Garner (Ex. 1007, 5:45-50, 5:62-6:3), the RE542 Patent (Ex. 1001, 2:49-55), and its inventor (Ex. 1006, p. 271).

Garner further discloses that the storage device has a default power mode, which can be designated by the bits "00." (Ex. 1007, 5:29-31, 7:14-19.) In certain embodiments, "the storage device always powers up in the lowest power mode" (or alternatively, the lowest power consumption value), which corresponds to the recited "default value." (*Id*., 6:48-51.)

e. 18(d) "wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,"

Garner teaches this limitation. (Ex. 1002, ¶¶215-17.)

The recited "default value" and "limiting value" are both "for power consumption of the peripheral device." A POSITA would therefore recognize that the comparative term "higher" applies to values for power consumption. (Ex. 1002, ¶215.) As discussed earlier, Garner's "highest power mode" and "lowest power mode" can read on the claimed "limiting value" and "default value," respectively. The storage device uses more power in the "highest power mode" than in the "lowest power mode," because the "highest power mode" corresponds to relatively higher clock frequency and/or data-access bandwidth. (Ex. 1007, 5:12-15, 5:46-6:15; Ex. 1002, ¶215.) The highest and lowest power modes are defined in the attribute memory 30. (Ex. 1007, 5:12-29.)

In the event the comparative term "higher" applies to the indicators (*e.g.,* two-bit power tuples) used for representing power consumption values, a POSITA would nevertheless find this limitation to be taught by Garner. (Ex. 1002, ¶216.) Garner discloses that the default power mode is represented by 00. (Ex. 1007, 5:29¬ 31, 7:14-19.) In an embodiment where the highest power mode is the default, 00 would represent the highest power mode. (*Id*., 5:29-31.) Since Garner also discloses an embodiment where the lowest power mode is the default, a POSITA would have recognized that it would be represented by 00 in that embodiment. (Ex. 1002, ¶216.) Further, Dr. Baker explains that a POSITA would

have recognized that "the particular bits used for representing information, such as power consumption value or power mode, is arbitrary." (*Id.*) Thus, a POSITA would have recognized that the highest and lowest power modes can be represented by 11 and 00, respectively. (*Id.*) As such, 11 is "higher" than 00.

Therefore, Garner discloses this limitation.

f. 18(e) "wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and"

Petitioner Kingston and Patent Owner have agreed in the related litigation involving this patent that this phrase is a means-plus-function term and have agreed that the function is, "setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value," and have agreed that the structure is "processor 13 of Fig. 1, Fig. 2, Fig. 3, 2:49- 59, 4:57-59, 6:6-30, 6:27-30" of the RE542 Patent, "and structural equivalents thereof." (Ex. 1010 at 1-2.) Garner discloses this function and structure. (Ex. 1002, ¶¶218-225.)

Garner's storage device 15 comprises a microprocessor 28 that discloses "a processor." (*Id*., ¶¶218-223.) The storage device receives from the host signals

that cause a selected power mode (or power consumption value) to be written to a register. (*Id.*, ¶221.) The power tuples (corresponding to the "value") indicated by the host can be stored in bits 4 and 5 of the configurations option register 33. (Ex. 1007, 5:19-31; 6:63-7:3, 7:45-59 ("a configuration register which stores a power mode configuration value, provided by a host processor").) The "microprocessor, responsive to commands from the host processor, [] read[s] the configuration register and [] control[s] operations related to the flash EEPROM array in accordance with the power mode configuration value." (*Id*., 7:55-59; 5:32-38, 7:3-9.)

The microprocessor 28 is also configured for "setting the maximum power consumption of the peripheral device to a value." (Ex. 1002, ¶¶222-23.) Garner discloses that "the microprocessor 28 tests the state of the bits 4 and 5 in the configuration options register 33 and runs the appropriate setup process" in order to "place the storage device 15 in the proper power mode for operation." (Ex. 1007, 5:32-38, 7:3-9.) Examples of the setup process include controlling the frequency divider circuit to set the processor clock frequency (PCLOCK) to a value that corresponds to the selected power mode (*e.g.,* 16MHz for the highest power mode), and setting the data-access bandwidth (*e.g.,* wordwide for the highest power mode). (*Id.*, 5:40-6:15). To do this, a POSITA would have

recognized that "the microprocessor must process the bits' values and identify the power mode that corresponds to the 'appropriate setup process.'" (Ex. 1002, ¶¶222-23.) This identification of the desired power mode to select and then "run[] the appropriate set up process" corresponds to the claimed step of setting the maximum power consumption of the device to the value. (*Id.*)

Garner further discloses that the "value" "is in a range from said default value to said limiting value, said range including said default value and said limiting value." (Ex. 1002, ¶224.) As discussed immediately above, the power mode selected by the host corresponds to the "value," and as discussed in *Section IX.A.1.b*, the lowest and highest power modes correspond to the "default value" and "limiting value," respectively. Garner discloses that the storage device supports "four distinct power modes of operation which use progressively less power," two of which being the lowest and highest power modes. (Ex. 1007, 5:12¬ 29.) A POSITA would have recognized that the four power modes from the lowest to the highest define a range. (Ex. 1002, ¶224.) Garner also discloses that the host can select any of the four power modes, including the lowest and highest. (Ex. 1007, 5:12-31.)

Therefore, Garner discloses this limitation.

g. 18(f) "wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device."

Garner teaches this limitation. (Ex. 1002, ¶¶218-23, 226-28.)

Garner discloses that the host can "place the storage device in the proper power mode of operation" by sending the selected power tuples to the storage device. (Ex. 1007, 2:12-19, 5:15-25.) The storage device is configured to receive signals from the host through PCMCIA bus, PCMCIA bridge, and interface 21, which "decod[es] signals furnished on the PCMCIA bus to a logic circuit 22." (*Id.*, 3:25-33, 3:57-60, Figs. 1 and 2.) The storage device then stores the power tuples (or alternatively power consumption values) provided by the host in, *e.g.,* bits 4 and 5 of the configuration options register. (*Id.*, 5:19-25, 7:51-59.) The stored power tuples are subsequently used "for setting the maximum power consumption of the peripheral device." Thus, the signals from the host that caused the selected power tuples to be stored correspond to the claimed "information." (Ex. 1002, ¶227.)

Therefore, Garner discloses this limitation.

2. Dependent Claim 23 "The peripheral device according to the claim 18, wherein said default value and at least one limiting value are stored in the peripheral device."

Garner discloses this limitation. (Ex. 1002, ¶229-32.)

Claim 18 is disclosed by Garner, as explained in *Section IX.A.1*.

Section IX.A.1.b explains that Garner's lowest and highest power modes, which correspond the claimed "default value" and "limiting value," respectively, are stored in the attribute memory of the storage device. (Ex. 1007, 5:3-31.)

Therefore, Garner discloses every additional limitation introduced by Claim 23.

3. Independent Claim 28

a. 28 (preamble) "A peripheral device comprising:"

As discussed in *Section IX.A.1.a*, Garner discloses this limitation. (*See* Ex. 1002, ¶233.)

b. 28(a) "a memory storing a default value and a limiting value for power consumption of the peripheral device;"

As discussed in *Section IX.A.1.*, Garner discloses this limitation. (*See* Ex. 1002, ¶234.)

c. 28(b) "a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,"

As discussed in *Section IX.A.1.c*, Garner discloses this limitation. (*See* Ex. 1002, ¶235.)

d. 28(c) "wherein a maximum power consumption of the peripheral device is set at a startup stage to said default value,"

As discussed in *Section IX.A.1.d*, Garner discloses this limitation. (*See* Ex. 1002, ¶236.)

e. 28(d) "wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,"

As discussed in *Section IX.A.1.e*, Garner discloses this limitation. (*See* Ex. 1002, ¶237.)

f. 28(e) "wherein the peripheral device comprises means for setting the maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and"

As discussed in *Section IX.A.1.f*, Garner discloses this limitation. (*See* Ex. 1002, ¶238.)

g. 28(f) "wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device, and"

As discussed in *Section IX.A.1.g*, Garner discloses this limitation. (*See* Ex. 1002, ¶239.)

h. 28(g) "wherein the means for setting the maximum power consumption of the peripheral device is

configured to obtain the value, as indicated by the received information, and to set the maximum power consumption of the peripheral device to the value."

As discussed in *Section IX.A.1.f*, Garner discloses this limitation. (*See* Ex. 1002, ¶240.)

Accordingly, Claim 28 is anticipated because each of its limitations is disclosed by Garner. (Ex. 1002, ¶241.)

4. Dependent Claim 29 "The peripheral device according to the claim 28, wherein said default value and at least one limiting value are stored in the peripheral device."

As discussed in *Section IX.A.2*, Garner discloses this limitation. (Ex. 1002, ¶242.)

Claim 28 is disclosed by Garner, as explained in *Section IX.A.1*.

Section IX.A.1.b explains that Garner's lowest and highest power modes, which correspond the claimed "default value" and "limiting value," respectively, are stored in the attribute memory of the storage device. (Ex. 1007, 5:3-31.)

Therefore, Garner discloses every additional limitation introduced by Claim 29.

5. Dependent Claim 32 "The peripheral device of claim 28, wherein the peripheral device is a memory card."

As explained in *Section IX.A.3*, Garner discloses every limitation of Claim 28. (Ex. 1002, ¶244.)

Garner's storage device is a flash EEPROM memory that can be joined to a host via PCMCIA (Personal Computer *Memory Card* International Association). (Ex. 1007, 3:27-48, Figs. 1, 2) (emphasis added). Thus, a POSITA would have recognized that the storage device is a "memory card." (Ex. 1002, ¶245.)

Therefore, Garner discloses every additional limitation introduced by Claim 32.

6. Dependent Claim 33 "The peripheral device of claim 28, wherein the limiting value is a highest possible power consumption of the peripheral device."

As explained in *Section IX.A.3*, Garner discloses every limitation of Claim 28. (Ex. 1002, ¶247.)

Section IX.A.1.b explains that Garner's highest power mode discloses the claimed "limiting value." The highest power mode is the highest of the "total of four possible power modes of operation." (Ex. 1007, 5:22-26.) Further, the highest power mode corresponds to the highest clock frequency and/or data-access bandwidth, which results in the highest power consumption for the storage device. (Ex. 1007, 5:47-6:15; Ex. 1002, ¶248.)

Therefore, Garner discloses every additional limitation introduced by Claim 33.

7. Dependent Claim 37 "The peripheral device of claim 28, wherein the default value is a lowest possible maximum power consumption for the peripheral device."

As explained in *Section IX.A.3*, Garner discloses every limitation of Claim 28. (Ex. 1002, ¶250.)

Section IX.A.1.b explains that Garner's lowest power mode discloses the claimed "default value." The lowest power mode is the lowest of the "total of four possible power modes of operation." (Ex. 1007, 5:22-26.) Further, the lowest power mode corresponds to the lowest clock frequency and/or data-access bandwidth, which results in the lowest power consumption for the storage device. (Ex. 1007, 5:47-6:15; Ex. 1002, ¶251.)

Therefore, Garner discloses every additional limitation introduced by Claim 37.

8. Dependent Claim 38 "The peripheral device of claim 28, wherein the means for setting the maximum power consumption of the peripheral device comprises a processor operable to set the maximum power consumption of the peripheral device to the value."

As explained in *Section IX.A.3*, Garner discloses every limitation of Claim 28. (Ex. 1002, ¶253.)

Section IX.A.1.f and *h* explained that the microprocessor disclosed in Garner discloses the means-plus-function limitation. The microprocessor "function[s]

essentially as a general purpose processor in a manner well known to those skilled in the art." (Ex. 1007, 4:7-10; Ex. 1002, ¶254.)

Therefore, Garner discloses every additional limitation introduced by Claim 38.

9. Dependent Claim 40 "The peripheral device of claim 28, wherein the range includes values other than the default value and the limiting value."

As explained in *Section IX.A.3*, Garner discloses every limitation of Claim 28. (Ex. 1002, ¶256.)

Section IX.A.1.f explained that the claimed "range" is taught by the four power modes of Garner. (Ex. 1007, 5:12-31; Ex. 1002, ¶257.) The four power modes include two intermediate power modes other than the highest and lowest power modes, which teach the claimed "default value and the limiting value." (Ex. 1007, 5:22-31, 5:50-61, 6:13-15; Ex. 1002, ¶257.)

Therefore, Garner discloses every additional limitation introduced by Claim 40.

B. GROUND 2: The combination of Garner and Toombs renders Claims 18, 23-24, 28-29, 32-33, and 37-40 obvious under § 103.

A POSITA would have found it obvious to combine (1) Garner's teaching of a power consumption management system and (2) Toombs' teaching of a MultiMediaCard to arrive at the alleged invention of the RE542 Patent. (Ex. 1002,

¶¶259-61.) A POSITA looking to improve either Garner or Toombs would have been motivated to look to techniques used in the other reference because both references relate to similar fields of endeavor (managing and configuring memory cards), address similar problems (power compatibility between memory cards and hosts), and disclose similar solutions (allowing negotiation between host and card to determine the operating configuration). (*Id.*) As discussed below, it would have been obvious to a POSITA to modify Garner in view of Toombs, as well as to modify Toombs in view of Garner.

Garner in view of Toombs

It would have been obvious to a POSITA that the storage device in Garner can adopt the form factor of a MultiMediaCard as taught in Toombs. (Ex. 1002, ¶262.) Since MultiMediaCard is also a type of flash memory, a POSITA would have recognized that substituting its small form factor for that of the storage device in Garner would have been a simple substitution of known elements. (*Id.*) A POSITA would have been motivated to do so to decrease the size of the storage device. (*Id.*) The modified MultiMediaCard would be capable of negotiating with its host to determine mutually acceptable power consumption levels, a benefit that Garner teaches. (*Id.*) The modification would expand the market for Garner's power management solution to the numerous host devices that were configured to

accept MultiMediaCard cards, and further enable the modified MultiMediaCards to operate with different types of hosts. (*Id.*) This achieves Garner's objective of allowing the storage device to "function with as many types of digital systems as possible." (Ex. 1007, 1:60-62.)

As part of the modification, it would have been obvious to a POSITA to combine the connector pins and form factor taught in Toombs, as shown in Figure 14, with the flash memory storage device of Garner because such combination would achieve the desirable and predictable result of provide the flash storage device with electrical contacts and standard form factor for electrically connecting to an external device or interface. (Ex. 1002, ¶263.) A POSITA would have recognized that the connector pins, once combined with Garner's storage device, would continue to perform the same function as described in Toombs. (*Id.*) This result is predictable and within the level of skill in the art since connector pins have long been used by memory cards and other types of electrical peripheral devices for receiving and outputting electronic signals, as confirmed by the teachings of Toombs. (*Id.*)

A POSITA would have recognized that the modification may also involve modifying Garner's storage device to accommodate the communication protocol of MultiMediaCards. (*Id.*, ¶264.) For example, Garner's microprocessor may be

modified to handle host commands and register access, since a MultiMediaCard's host may be unable to access the card's registers directly. (*Id.*)

In view of Garner and Toombs' teachings, it would have been obvious and within the level of skill of a POSITA to make the modification. (*Id.*, ¶¶265-66.) Garner describes a microprocessor-controlled memory/storage device 15 configured to manage power consumption according to the power mode selected by a host and written into a register (*e.g.,* configuration options register 33). (Ex. 1007, Abstract, 1:10-13, 5:19-25.) The storage device comprises a microprocessor 28. (*Id.*, Fig. 2.) In view of Toombs' teachings, a POSITA would have found it obvious to modify the microprocessor to handle host commands for writing a selected power mode into a register. (Ex. 1002, ¶¶265-66.) Toombs teaches a MultiMediaCard with a MMC Interface Controller that is configured to process commands from the host and write to the MultiMediaCard's registers. (*Id.*) Toombs discloses that during voltage negotiation, the host determines an acceptable voltage range supported by the MultiMediaCard and "sends the determined VDD voltage window as an operand of the command SEND_OP_COND (CMD1). In response to this command, each of the active cards will define its OCR register value according to this voltage." (Ex. 1008, 16:21-25.) Figure 14 shows that the MMC Interface Controller is configured to

receive the CMD and DAT signals and has exclusive access to the registers. (Ex. 1002, ¶¶265-66.) Thus, a POSITA would have recognized that the Controller is responsible for processing the host's command and operand and, in response, writing the specified voltage range into the OCR register. (*Id.*)

In view of Toombs, a POSITA would have found it obvious that the storage device in Garner can be modified to have a central microprocessor that handles register-access commands from the host and controls access to the registers. (Ex. 1002, ¶267.) By applying Toombs' known technique for commanding a memory card to store data, a POSITA would have recognized that in Garner, signals from the host for writing the selected power mode to the register (Ex. 1007, 5:19-21) can be a command and an operand specifying a desired power mode. (Ex. 1002, ¶267.) Further, a POSITA would have also found it obvious to modify the architecture of Garner's storage device in a manner taught by Toombs (*e.g.,* Figure 14) such that the microprocessor is configured to receive commands and operands from the host and control access to the registers. (*Id.*, ¶¶268-69.)

For example, Dr. Baker explains that the storage device shown in Figure 2 of Garner can be modified (modification shown below) by removing the data path, highlighted in red, from interface 21 to configuration operations register 33. (*Id.*) This represents the host not having direct access to write to the register 33. (*Id.*)

The remaining data path, highlighted in green, shows that the microprocessor 28 (via microprocessor interface 42) handles incoming signals from the host and controls access to the configuration options register 33. (*Id.*)

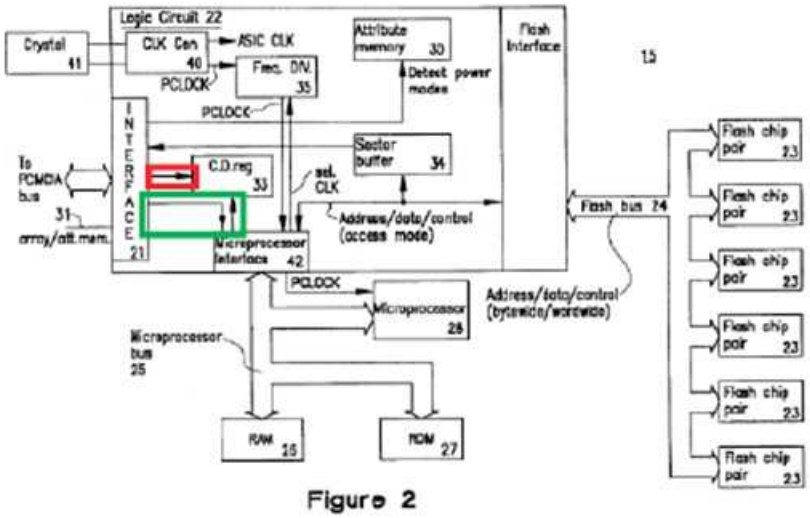

Figure 2

In this modified system, the host in operation may send a command and operand specifying the desired power mode to the storage device. (*Id.*, ¶267.) In response, the microprocessor of the storage device may process the command and write the desired power mode into the configuration options register. (*Id.*, ¶¶268-69.)

A POSITA would have been motivated to combine Garner and Toombs as described above for a variety of reasons. A POSITA would have recognized that having the microprocessor handle register-access commands provides a layer of logical abstraction to the host. (*Id.*, ¶270.) This benefits the host because the host

would not need to know precisely where to store data (*e.g.,* bits 4 and 5 in the configuration options register 33, as disclosed in Garner). (*Id.*) Instead, as shown in Toombs, the host can simply sends a SEND_OP_COND command with a voltage-range operand. (*Id.*) This design is also beneficial to the memory storage device because it allows the device to unilaterally alter the storage location without needing to inform the host. (*Id.*)

Another benefit of having a microprocessor-controlled memory device is the flexibility afforded to device designers for changing how the device operates. (*Id.*, ¶271.) Since the microprocessor operates according to the stored software or processes (Ex. 1007, 4:13-16), a POSITA would have recognized that the manner in which commands are handled and data are stored can be altered simply with a software update. (Ex. 1002, ¶271.) Since both Garner and Toombs address compatibility issues of memory cards, a POSITA would have recognized the importance of enabling memory devices to have the flexibility to change its operation if the need arises. (*Id.*)

A POSITA would have also recognized that a microprocessor controlling access to registers provides the benefit of simplifying the overall system design and providing extra protection to the memory card since a single unit has control over read/write operations. (*Id.*, ¶272.) Configuring the registers to be exclusively

controlled by the microprocessor provides the storage device with stability and predictability with respect to what is written to its registers, and prevents the host from writing improper or incorrectly formatted data to the configuration register. (*Id.*)

Toombs in view of Garner

For similar reasons, a POSITA would have found it obvious to modify a MultiMediaCard, such as the one disclosed in Toombs, to include the power consumption management capabilities of Garner. (Ex. 1002, ¶273.) In particular, Garner teaches how to configure a memory card to operate in a power mode selected by a host and adjust operating configurations (*e.g.,* clock frequency) accordingly to limit power consumption. (Ex. 1007, 2:11-19, 5:12-61.) A POSITA would have been motivated to modify Toombs' MultiMediaCard to include Garner's power consumption management capabilities because doing so would improve compatibility with hosts, as explained in Garner. (Ex. 1002, ¶273.) Garner states that it is "desirable to allow any [removable] storage device ... to function with as many different types of digital systems as possible." (Ex. 1007, 1:60-62.) However, because powers supplied by hosts differ, Garner recognize a need to improve compatibility between hosts and memory cards. (*Id.*, 1:48-59.) Toombs similarly recognizes compatibility issues faced by MultiMediaCards.

(Ex. 1008, 1:37-41, 15:39-44, 16:14-20.) To address compatibility issues, both Toombs and Garner devised a solution where the host and the memory card negotiate an acceptable operational configuration. (Ex. 1007, 2:11-20; Ex. 1008, 1:50-55.) While Toombs addresses operating voltage compatibility (Ex. 1008, 10:5-13, 16:21-25), it does not address power consumption compatibility. A POSITA would have been motivated to modify Toombs in accordance with Garner to design a MultiMediaCard with power consumption management capabilities in order to further improve compatibility. (Ex. 1002, ¶273.)

Further, it would have been obvious to a POSITA that Garner's teaching can be implemented by a MultiMediaCard. (*Id.*, ¶¶274-75.) A POSITA would have recognized that the storage device 15 in Garner is a flash memory card (Ex. 1007, 2:3-20, 3:27-33) and a MultiMediaCard is a type of flash memory card (Ex. 1008, 1:27-32, 1:45-47, Figs. 1 and 14). (Ex. 1002, ¶273.) Moreover, a POSITA would have recognized that a MultiMediaCard capable of negotiating operating voltages (Toombs) can similarly be configured to negotiate power-expenditure modes (Garner), since the negotiation solutions described in Garner and Toombs utilize similar underlying techniques of configuring a memory card to store supported operational configurations for selection by a host. (Ex. 1002, ¶275.)

It would have been obvious to a POSITA to modify Toombs' MultiMediaCard to store supported power modes as described in Garner. (*Id.*, ¶276.) Garner discloses that four supported power modes, represented as two-bit power tuples, are stored in the attribute register of the storage device. (Ex. 1007, 5:3-31.) Similarly, Toombs discloses that the MultiMediaCard stores supported voltage profile information in its OCR register. (Ex. 1008, 9:61-64, 10:5-13, 15:42-49, 15:67-16:13.) Toombs also disclose a CSD register "responsible for providing information to the MultiMediaCard host on how to access the card content." (Ex. 1008, 10:21-33, 11:51-67 (storing "the minimum and maximum values for read and write currents").) Thus, it would have been obvious to a POSITA that the MultiMediaCard of Toombs can be modified to store supported power modes in its OCR or CSD register (or in any other register). (Ex. 1002, ¶276.) Using the OCR/CSD register (Toombs) rather than the attribute register (Garner) to store power modes is a simple substitution of known technologies with similar functionality. (*Id.*) While Figure 15 of Toombs may show all 32 bits of the OCR register being occupied, one skilled in the art would have recognized that the size of the register and the assignments of the bits are both simple design choices that can be adjusted to accommodate or be replaced by power modes. (*Id.*) Alternatively, it would have been obvious to a POSITA that an attribute register

can be added to Toombs' MultiMediaCard for storing supported power modes. (*Id.*) The attribute register would be used in the same way it had been used in Garner to yield a predictable result of storing data regarding card operation/compatibility. (*Id.*)

A POSITA would have also found it obvious to modify Toombs' MultiMediaCard such that it operates in the lowest power mode during its power-up sequence (Ex. 1008, 17:33-46), as Garner teaches. (Ex. 1002, ¶277.) Garner expressly explains that one motivation for starting up in the lowest power mode is to address the possibility of the MultiMediaCard not being able to function with a host that provides insufficient power. (Ex. 1007, 6:46-51.) Thus, a POSITA would have recognized that powering up in the lowest supported power mode achieves the predictable and desirable result of improving the likelihood that the MultiMediaCard would function upon startup when used with low-power hosts – thus expanding the market for the card by making them compatible with more hosts. (Ex. 1002, ¶277.)

Further, a POSITA would have found it obvious to modify Toombs' MultiMediaCard in view of Garner to handle a host's commands for setting the power mode. (Ex. 1002, ¶278.) Garner teaches a host causing a selected power mode to be stored in a register of the storage device. (Ex. 1007, 5:19-31, 7:51-54.)

Toombs discloses that the MMC Interface Controller of the MultiMediaCard is configured to receive commands (*e.g.,* SEND_OP_COND) and operands indicating selected voltage ranges, and in response store the voltage range in the OCR register. (Ex. 1008, 16:21-25, Fig. 14.) It would have been obvious to a POSITA that a similar command protocol can be used to set the power mode. (Ex. 1002, ¶278.) For example, the MultiMediaCard can be configured to receive and process a host's command and operand that specifies a power mode selection, and in response write the selected power mode to the OCR register. (*Id.*) While in Garner the power mode selection is written to a configuration options register (Ex. 1007, 5:19-31), it would be obvious to a POSITA that the power mode selection can instead be stored in any other register, such as the OCR register of the MultiMediaCard. (Ex. 1002, ¶279.) Doing so amounts to a simple substitution of one register for another. (*Id.*) Indeed, Garner itself stated that the power mode could instead be written to an ATA features register. (*Id.*) Alternatively, it would have been obvious to a POSITA that a configuration options or features register taught by Garner can be added to Toombs' MultiMediaCard for storing the selected power mode. (*Id*.) The register would be used in the same way it had been used in Garner to yield a predictable result of storing data regarding the host's selected power mode. (*Id.*)

A POSITA would have also found it obvious to modify the MultiMediaCard of Toombs such that its MMC Interface Controller is configured to read the selected power mode from the register and adjust the clock frequency accordingly. (Ex. 1002, ¶280.) Garner discloses that the microprocessor 28 reads the power mode stored in the register and adjusts the clock frequency of a clock generator accordingly. (Ex. 1007, 5:32-60, 7:3-8, 7:55-59, 8:6-9.) A POSITA would have found it obvious that the function performed by Garner's microprocessor can equally be performed by the MMC Interface Controller, since both are circuitry for processing data and controlling the operation of a memory card. (Ex. 1002, ¶280.) Alternatively, a POSITA would have recognized that the Controller of Toombs could be incorporated or substituted with a general-purpose processor, such as the microprocessor in Garner (Ex. 1007, 4:4-10), in order to provide MultiMediaCards with Garner's power management functionalities. (Ex. 1002, ¶280.) While Toombs does not expressly disclose a clock generator, a POSITA would have recognized the MultiMediaCard inherently or obviously (in view of Garner's clock generator) includes a clock generator since all digital controllers/processors require clock signals to operate. (*Id.*, ¶281.) In addition, it would have been obvious to a POSITA to use a frequency divider circuit in the modified MultiMediaCard to adjust the frequency of the clock signal generated by the clock generator, as taught

by Garner. (Ex. 1007, 5:50-53, Fig. 2; Ex. 1002, ¶281.) Combining the frequency divider circuit in Garner with the MultiMediaCard amounts to a combination of known elements that yields a predictable result of enabling the Controller/microprocessor to change the clock signal's frequency. (Ex. 1002, ¶281.) A POSITA would have been motivated to adjust the clock frequency based on the power mode because, as explained in Garner, changing the clock frequency will change the power consumption of the device. (Ex. 1007, 5:46-50; Ex. 1002, ¶281.)

In either combination described above, the combined teachings of Garner and Toombs disclose, teach, or suggest every limitation of Claims 18, 23-24, 28-29, 32-33, and 37-40.

1. Independent Claim 18

a. 18 (preamble) "A peripheral device comprising:"

To the extent that the preamble is limiting, it is taught by both Garner and Toombs. (Ex. 1002, ¶283-85.)

As explained in *Section IX.A.1.a,* to the extent the preamble is a limitation, it is taught by the storage device in Garner. (Ex. 1002, ¶283.)

Toombs teaches "detachable cards such as memory cards or I/O interfaces," such as MultiMediaCards. (Ex. 1008, 1:9-11, 1:45-47, Figs. 1 and 14.) A

MultiMediaCard is a "peripheral device" as evidenced by Claim 28's dependent claims, which recite that the "peripheral device" includes "a memory card" (Claim 32) and "a MultiMediaCard" (Claim 39). (Ex. 1002, ¶284.)

b. 18(a) "a memory storing a default value and a limiting value for power consumption of the peripheral device;"

Garner teaches this limitation, as discussed above in *Section IX.A.1.b*. As explained therein, Garner discloses a register storing the supported power modes, including the lowest and highest. (Ex. 1007, 5:3-15.) Also explained therein is that corresponding power consumption values (*e.g.,* in power/energy units) can alternatively be stored to achieve the same functional purpose. (Ex. 1002, ¶286.)

Toombs teaches various registers storing values relating to the operation and compatibility of the memory card. (Ex. 1008, 9:41-59.) In view of Garner's disclosures relevant to this limitation, it would have obvious to a POSITA to modify Toombs' MultiMediaCard to similarly store the supported power modes or power consumption values in such a register (*e.g.,* OCR or CSD register), as discussed in *Section IX.B*. (Ex. 1002, ¶287.)

c. 18(b) "means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,"

Garner teaches this limitation, as discussed above in *Section IX.A.1.c*. (Ex. 1002, ¶289.) Alternatively, it would have been obvious that the storage device of Garner can be combined with the connector pins taught by Toombs. (*Id.*) The connector pins also teach this limitation. (Ex. 1002, ¶290-91.)

Toombs discloses a MultiMediaCard as shown in Figure 14, copied below:

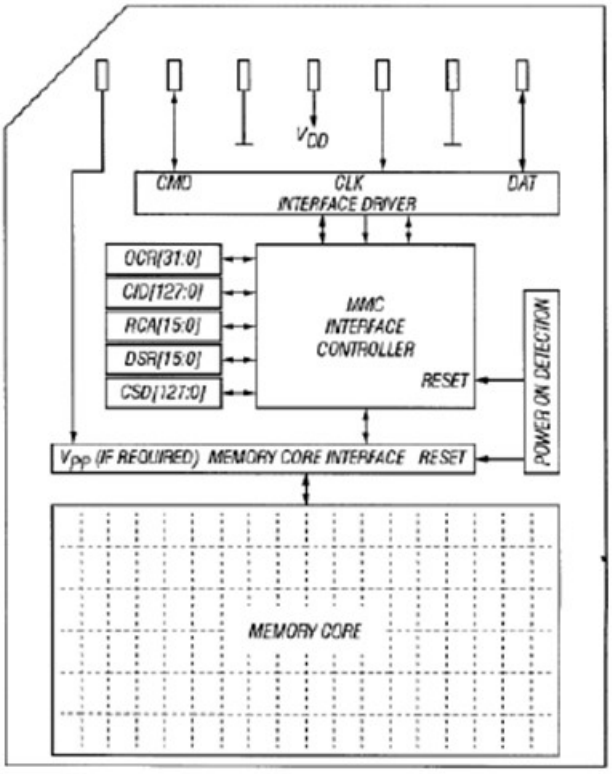

FIG. 14

The top edge of the MultiMediaCard comprises connector pins for connecting the MultiMediaCard to a host computer system. (Ex. 1002, ¶291; Ex. 1008, Figure 1.)

Certain connector pins (*e.g.,* CMD and DAT) are "for bidirectional communications between the MultiMediaCard host and the MultiMediaCard cards." (Ex. 1008, 7:41-44.) Also shown are two connector pins, V_{DD} and V_{PP}, for supplying power to the MultiMediaCard. (Ex. 1002, ¶291.) Toombs discloses that different voltages, "Vss1, Vss2, and Vdd," are "provided to the MultiMediaCard card for performing different operations such as data read, write and erasure, etc." (Ex. 1008, 7:32-40.) Thus, the connector pins shown in Figure 14 teaches this limitation. (Ex. 1002, ¶¶290-92.)

d. 18(c) "wherein the power consumption of the peripheral device is set at a startup stage to said default value,"

Garner teaches this limitation, as discussed above in *Section IX.A.1.d*. (Ex. 1002, ¶293.)

In view of Garner's disclosures relevant to this limitation, it would have obvious to a POSITA to modify Toombs' MultiMediaCard to similarly power up in a default power mode (*e.g.,* the lowest power mode or lowest power consumption value), as discussed in *Section IX.B*. (Ex. 1002, ¶294.)

e. 18(d) "wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,"

Garner teaches this limitation, as discussed above in *Section IX.A.1.e*. (Ex. 1002, ¶296.)

In view of Garner's disclosures relevant to this limitation, it would have obvious to a POSITA to modify Toombs' MultiMediaCard to similarly store the four supported power modes, including the highest and lowest, as discussed in *Section IX.A.1.b*. (Ex. 1002, ¶297.)

f. 18(e) "wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and"

Garner in view of Toombs teaches "a processor." (Ex. 1002, ¶¶299-300.) As discussed above under *Section IX.B*, a POSITA would have found it obvious to modify Garner in view of Toombs such that its microprocessor is configured to process register-access commands and operands from the host and write the selected power mode to the register. (Ex. 1002, ¶¶299-300.) Garner's microprocessor, which may function essentially as a general-purpose processor in a manner well known to those skilled in the art," corresponds to "a processor." (*Id.*)

Toombs in view of Garner also teaches "a processor." (*Id*.) Toombs discloses a MultiMediaCard comprising an MMC Interface Controller. (Ex. 1008, Fig. 14.) A POSITA would have recognized that the Controller as shown is configured to receive communication signals (*e.g.,* commands CMD and data DAT) from the host and has exclusive access to the registers. (Ex. 1002, ¶¶299-300.) Thus, a POSITA would have recognized that in one embodiment the Controller is responsible for (1) processing the host's command (*e.g.,* SEND_OP_COND (CMD1)) and operand indicating a desired operating voltage window, and (2) writing the voltage window into the OCR register. (Ex. 1008, 15:42-53, 16:21-25.) A POSITA would have recognized that the MMC Interface Controller is therefore "a processor" because it is a circuitry that processes electronic data or signals. (Ex. 1002, ¶¶299-300.) Alternatively, as discussed in *Section IX.B*, it would have been obvious to a POSITA that the MMC Interface Controller could be substituted by or incorporated with a general-purpose processor, such as the microprocessor in Garner. (*Id*.)

Garner teaches "setting the maximum power consumption of the peripheral device to a value." (Ex. 1002, ¶301.) Garner discloses that the host reads the power modes stored on the storage device, selects one, and writes the selected power mode to a register. (Ex. 1007, 5:19-31, 6:63-7:3, 7:45-59.) An alternative

design choice is to read, select, and write a power consumption value. (Ex. 1002, ¶301.) Storing the selected power mode in the register causes operational configurations to be changed, such as clock frequency. (Ex. 1007, 5:32-61, 7:3-8.) As explained by Garner (Ex. 1007, 5:46-50) and Dr. Baker (Ex. 1002, ¶163-72), the clock frequency effectively limits power consumption of the storage device. Thus, the storing of the power mode (the "value") selected by the host discloses "set the maximum power consumption of the peripheral device to the value." (Ex. 1002, ¶301.)

As discussed in *Section IX.B*, a POSITA would have found it obvious to modify (1) Garner in view of Toombs and (2) Toombs in view of Garner, such that the two combinations' respective microprocessor and Controller are configured to control access to registers. (Ex. 1002, ¶302.) This includes writing the host's power mode selection into a register, as taught by Garner. (*Id.*) Accordingly, both combinations teach "a processor" for "setting the maximum power consumption of the peripheral device to a value." (*Id.*)

Garner further discloses that the "value" is "in a range from said default value to said limiting value, said range including said default value and said limiting value." (Ex. 1002, ¶303.) As discussed immediately above, the power mode selected by the host corresponds to the "value," and as discussed in Section

Sections IX.A.1.b, d, e, the lowest and highest power modes correspond to the "default value" and "limiting value," respectively. Garner discloses that the storage device supports "four distinct power modes of operation which use progressively less power," two of which being the lowest and highest power modes. (Ex. 1007, 5:12-29.) A POSITA would have recognized that the four power modes from the lowest to the highest define a range. (Ex. 1002, ¶303.) Garner also discloses that the host can select any of the four power modes, including the lowest and highest. (Ex. 1007, 5:12-31.) Thus, Garner discloses that the power mode selected by the host is "in a range from said default value to said limiting value, said range including said default value and said limiting value." (Ex. 1002, ¶303)

g. 18(f) "wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device."

Garner discloses that the storage device 15 is "configured to receive information from the electronic device." (Ex. 1002, ¶305.) Garner discloses that the host can selectively write a selected power mode into a register of the storage device. (Ex. 1007, 2:12-19, 4:49-57, 5:15-21, 6:63-7:9.) Signals from the host are received via PCMCIA and interface 21, which "provides appropriate circuitry for decoding signals furnished on the PCMCIA bus to a logic circuit 22." (Ex. 1007,

3:25-33, 3:59-60.) Garner further discloses that the storage device has a "configuration register which stores a power mode configuration value, **provided by a host processor**" and also "a microprocessor, **responsive to commands from the host processor**...." (Ex. 1007, 7:51-59 (emphasis added).)

Toombs also discloses that the MultiMediaCard is "configured to receive information from the electronic device." (Ex. 1002, ¶300.) The MultiMediaCard is configured to receive CMD and DAT signals from the host. (Ex. 1008, 7:32-44, Figs. 1 and 14.) For example, the MultiMediaCard is configured to receive a SEND_OP_COND (CMD1) command from the host and associated operands. (Ex. 1008, 16:21-25.)

The combined teachings of Garner and Toombs disclose that the received information is "for setting the maximum power consumption of the peripheral device." (Ex. 1002, ¶307.) As discussed in *Section IX.B*, a POSITA would have found it obvious to combine Garner and Toombs such that Garner's storage device or Toombs' MultiMediaCard may receive from the host a command and operand (the received "information") and in response write the power mode (or power consumption value) specified by the operand in a register. (Ex. 1002, ¶307.) As discussed in *Section IX.B.1.d* (via *Section IX.A.1.d*), the power mode stored in the register causes the clock frequency and/or data-access bandwidth to adjust

accordingly, which in turn affects the power consumption of the storage device. (*Id.*) Thus, the received command and operand is "for setting the maximum power consumption of the peripheral device." (Ex. 1002, ¶307.)

2. Dependent Claim 23 "The peripheral device according to the claim 18, wherein said default value and at least one limiting value are stored in the peripheral device."

Claim 18 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

Section IX.B.1.b explains that Garner's lowest and highest power modes, which correspond the claimed "default value" and "limiting value," respectively, are stored in the attribute memory of the storage device. (Ex. 1007, 5:3-31.)

Therefore, Garner and Toombs discloses every additional limitation introduced by Claim 23. (Ex. 1002, ¶309-11.)

3. Dependent Claim 24 "The peripheral device according to the claim 18, wherein said peripheral device is a MultiMediaCard™ peripheral device."

With respect to Ground 1, *Section IX.A.1* of this declaration established that Garner discloses every limitation of Claims 18. With respect to Ground 2, *Section X.B.1* established that Garner and Toombs teach every limitation of Claims 18. For both Grounds 1 and 2, it would have been obvious to one skilled in the art that the "peripheral device" can be a MultiMediaCard. (Ex. 1002, ¶312.)

Toombs discloses a MultiMediaCard. (Ex. 1008, 1:45-47, Fig. 14; Ex. 1002, ¶338.)

As discussed in *Section IX.B*, it would have been obvious to a POSITA that the storage device in Garner can have the form factor of a MultiMediaCard as taught in Toombs. (Ex. 1002, ¶¶313-15.)

4. Independent Claim 28

a. 28 (preamble) "A peripheral device comprising:"

As discussed in *Section IX.B.1.a*, Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶316.)

b. 28(a) "a memory storing a default value and a limiting value for power consumption of the peripheral device;"

As discussed in *Section IX.B.1.b*, Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶317.)

c. 28(b) "a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,"

As discussed in *Section IX.B.1.c*, Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶318.)

d. 28(c) "wherein a maximum power consumption of the peripheral device is set at a startup stage to said default value,"

As discussed in *Section IX.B.1.d*, Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶319.)

e. 28(d) "wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,"

As discussed in *Section IX.B.1.e*, Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶320.)

f. 28(e) "wherein the peripheral device comprises means for setting the maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and"

As discussed in *Section IX.B.1.f*, Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶321.)

g. 28(f) "wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device, and"

As discussed in *Section IX.B.1.g,* Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶322.)

h. 28(g) "wherein the means for setting the maximum power consumption of the peripheral device is

configured to obtain the value, as indicated by the received information, and to set the maximum power consumption of the peripheral device to the value."

As discussed in *Section IX.B.1.f,* Garner and Toombs disclose this limitation. (*See* Ex. 1002, ¶323.)

Section IX.B.1.f explained that Garner and Toombs teach "wherein the means for setting the maximum power consumption of the peripheral device is configured ... to set the maximum power consumption of the device to the value." As discussed therein, Garner's microprocessor and Toombs' MMC Interface Controller each teaches the structure of this means-plus-function element, and the selected power mode (or power consumption value) disclosed in Garner teaches the claimed "value." (Ex. 1002, ¶324.)

The combinations of Garner and Toombs further teach that Garner's microprocessor and Toombs' Controller are "configured to obtain the value, as indicated by the received information." (Ex. 1002, ¶¶325-26.) With respect to portion of the limitation that recites "the value, as indicated by the received information," *Section IX.B.1.f* explains that the received command and operand specifying a power mode teach the claimed "received information," and *Section IX.B.1.g* explains that the specified power mode teaches the claimed "value." (*Id*.)

Therefore, the power mode indicated by the received command and operand teaches the recited "value, as indicated by the received information."

Section IX.B explains that a POSITA would have found it obvious to modify (1) Garner in view of Toombs and (2) Toombs in view of Garner, such that the two combinations' respective microprocessor and Controller are configured to process incoming commands and operands from the host and in response write the power mode selection to a register. (*Id*.) Thus, a POSITA would have understood that the microprocessor/Controller must obtain the selected power mode (the "value") as indicated by the received command/operand (the "received information") in order to write the power mode selection into the register. (*Id.*)

Accordingly, since every limitation of Claim 28 is taught by the combined teachings of Garner and Toombs, Claim 28 is rendered obvious. (Ex. 1002, ¶328.)

5. Dependent Claim 29 "The peripheral device according to the claim 28, wherein said default value and at least one limiting value are stored in the peripheral device."

Claim 28 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

As discussed in *Section IX.A.2*, Garner discloses the additional limitations introduced by dependent Claim 29. (Ex. 1002, ¶329.)

In view of Garner's disclosures relevant to this limitation, it would have obvious to a POSITA to modify Toombs' MultiMediaCard to similarly store the

supported power modes in one of its registers (*e.g.,* OCR/CSD register), as discussed in *Section IX.B.1.b*. (Ex. 1002, ¶330.)

6. Dependent Claim 32 "The peripheral device of claim 28, wherein the peripheral device is a memory card."

Claim 28 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

As discussed in *Section IX.A.5*, Garner discloses the additional limitations introduced by dependent Claim 32. (Ex. 1002, ¶333.)

Furthermore, Toombs' MultiMediaCard is a memory card. (Ex. 1008, 1:27-32, Fig. 14; Ex. 1002 ¶334.)

7. Dependent Claim 33 "The peripheral device of claim 28, wherein the limiting value is a highest possible power consumption of the peripheral device."

Claim 28 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

As discussed in *Section IX.A.6*, Garner discloses the additional limitations introduced by dependent Claim 33. (Ex. 1002, ¶337.)

In view of Garner's disclosures relevant to this limitation, it would have obvious to a POSITA to modify Toombs' MultiMediaCard to similarly have four supported power modes (including the highest power mode), as discussed in *Section IX.A*. (Ex. 1002, ¶338.)

8. Dependent Claim 37 "The peripheral device of claim 28, wherein the default value is a lowest possible maximum power consumption for the peripheral device."

Claim 28 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

As discussed in *Section IX.A.7*, Garner discloses the additional limitations introduced by dependent Claim 37. (Ex. 1002, ¶341.)

In view of Garner's disclosures relevant to this limitation, it would have obvious to a POSITA to modify Toombs' MultiMediaCard to similarly have four supported power modes (including the lowest power mode), as discussed in *Section IX.A*. (Ex. 1002, ¶342.)

9. Dependent Claim 38 "The peripheral device of claim 28, wherein the means for setting the maximum power consumption of the peripheral device comprises a processor operable to set the maximum power consumption of the peripheral device to the value."

Claim 28 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

As discussed in *Section IX.A.8,* Garner discloses the additional limitations introduced by dependent Claim 38. (Ex. 1002, ¶345.)

As discussed in *Section IX.B* Toombs' Controller is a "processor" or alternatively it would have been obvious to a POSITA that the Controller can be replaced by or incorporated with the microprocessor taught by Garner. (Ex. 1002,

¶334.) The Controller/microprocessor is operable to set the maximum power consumption, as explained in *Section IX.B.1.f*.

10. Dependent Claim 39 "The peripheral device of claim 32, wherein the memory card is a MultiMediaCard."

Claim 28 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

As discussed in *Section IX.B.3*, Garner in view of Toombs disclose, this limitation. (Ex. 1002, ¶348.)

11. Dependent Claim 40 "The peripheral device of claim 28, wherein the range includes values other than the default value and the limiting value."

Claim 28 is disclosed by Garner and Toombs, as explained in *Section IX.B.1*.

As discussed in *Section IX.A.9*, Garner discloses the additional limitations introduced by dependent Claim 40. (Ex. 1002, ¶351.)

As discussed in *Section IX.B.1.f*, the four power modes in Garner teach the claimed "range." The four power modes include two intermediate power modes other than the highest and lowest power modes. (Ex. 1007, 5:12-31; Ex. 1002, ¶351.)

X. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests that a trial for *inter partes* review of the RE542 Patent be instituted and that Claims 18, 23-24, 28-29, 32-33, and 37-40 be rejected and canceled.

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Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 13,988 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word Document, the word processing program used to create it.

The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word Document in Times New Roman 14-point font

Dated: January 30, 2019

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true copy of the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. RE45,542** and supporting materials (Exhibits 1001 - 1013 and Power of Attorney) have been served in its entirety this January 30, 2019, by e-mail and Federal Express on Patent Owner at the correspondence address for the attorney of record for the RE45,542 Patent shown in USPTO PAIR, as well as on counsel for Patent Owner in the co-pending litigation:

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