

U.S. Patent No. 8,307,180
Petition for *Inter Partes* Review

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC
Patent Owner

Case No.: To Be Assigned
U.S. Patent No. 8,307,180

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 8,307,180**

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Patent Trial and Appeal Board
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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1001	U.S. Pat. No. 8,307,180 to Hyvönen et al.
1002	Declaration of Dr. R. Jacob Baker
1003	CF+ and CompactFlash Specification Revision 3.0
1004	U.S. Pat. No. 7,478,248 to Ziv et al.
1005	U.S. Pat. No. 6,681,304 to Vogt et al.
1006	U.S. Pat. No. 6,279,114 to Toombs et al.
1007	U.S. Pat. No. 7,409,489 to Sinclair
1008	U.S. Pat. Pub. No. 2006/00220054 to Elhamias
1009	File History for U.S. Pat. No. 8,307,180
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1011	U.S. Pat. Publ. No. 2008/0080688 to Burgan et al.
1012	U.S. Pat. No. 5,809,340 to Bertone et al.
1013	U.S. Pat. Publ. No. 2006/0280077 to Suwa
1014	U.S. Pat. No. 7,152,801 to Cuellar et al.
1015	<i>CompactFlash Association Announces Availability of Revision 3.0 of the CF+ & CompactFlash Specification; Revision 3.0 Increases CF Interface Data Transfer Rate to 66MB/sec</i> , BUSINESS WIRE (Jan. 7, 2005)
1016	U.S. Pat. Publ. No. 2007/079015 to Royer, Jr. et al.
1017	U.S. Pat. No. 3,653,001 to Ninke

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1018	Public Key Infrastructure: Implementation and Design, by Suranjan Choudhury et al.
1019	Assignment History for U.S. Pat. No. 7,478,248 to Ziv et al.
1020	Assignment History for U.S. Pat. No. 6,279,114 to Toombs et al.
1021	Assignment History for U.S. Pat. No. 7,409,489 to Sinclair et al.
1022	Third Joint Claim Construction and Prehearing Statement (N.D. Cal. Patent L.R. 4-3), filed in the related matter on Nov. 16, 2018
1023	Affidavit of Christopher Butler, Internet Archive
1024	Exhibit A to the Affidavit of Christopher Butler
1025	Declaration of Michael Asao

I. INTRODUCTION AND STATEMENT OF RELIEF REQUESTED (37 C.F.R. §42.22(a))

Kingston Technology Company, Inc. (“Petitioner” or “Kingston”) hereby petitions to institute an *inter partes* review of Claims 1-3, 5, 12, 13, 16-19, 21, 28, 29, 32, and 35 (the “Challenged Claims”) of U.S. Patent No. 8,307,180 (the “’180 Patent”) to Hyvonen *et al.* (Ex. 1001), and cancel those claims as unpatentable.

As discussed below, the prior art anticipates and/or renders obvious the Challenged Claims of the ’180 Patent under 35 U.S.C. § 102 and/or § 103. Accordingly, there is a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim, and Petitioner respectfully requests that the Board institute a trial for *inter partes* review and cancel all Challenged Claims as unpatentable.

II. MANDATORY NOTICES (37 C.F.R. §42.8(A)(1))

A. Real Party-In-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Kingston Technology Company, Inc., is a real party-in-interest. Petitioner’s parent company, Kingston Technology Corporation (“Kingston Holding”), is a holding company without any employees or operations. However, because Kingston Holding is the sole owner of Petitioner and shares some directors, Petitioner identifies Kingston Holding as an additional real party-in-interest.

B. Identification of Related Matters (37 C.F.R. §42.8(b)(2))

Patent Owner Memory Technologies, LLC (“MTL”) has asserted the Challenged Claims of the ’180 Patent, as well as claims from seven other patents, against Kingston in a co-pending litigation, *Memory Technologies, LLC v. Kingston Technology Co., Inc.*, 8:18-cv-00171 (C.D. Cal.). MTL’s original Complaint was filed on January 31, 2018, and served on Kingston, at the earliest, on February 1, 2018.

In addition to this Petition, Kingston has or will be filing petitions for *inter partes* review of the other seven patents that MTL has asserted against it.

C. Counsel and Service Information (37 C.F.R. §§42.8(b)(3) & (b)(4))

Petitioner designates the following Lead and Backup Counsel. Concurrently filed with this Petition is a Power of Attorney for appointing the following Lead and Backup Counsel, per 37 C.F.R. § 42.10(b). Service via hand-delivery may be made at the postal mailing addresses below. Petitioner consents to electronic service by e-mail at the following address: **Kingston-180ipr@pillsburylaw.com**.

Lead Counsel	Back-Up Counsel
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D. Payment of Fees (37 C.F.R. §42.103)

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 033975 for the petition fee and for any other required fees.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests that the Challenged Claims of the '180 Patent be cancelled as anticipated or obvious based on the following grounds:

Ground	'180 Patent Claims	Basis for Rejection
1	1, 3, 9, 10, 12, 19, 21, 27, 28, and 30	§ 102 based on <i>CompactFlash</i>
2	1, 5, 16, 17, 21, 32, and 35	§ 103 based on <i>Ziv and Vogt</i>
3	2, 3, 18, and 19	§ 103 based on <i>Ziv, Vogt, and Toombs</i>
4	1, 2, 3, 5, 16, 17, 18, 19, 21, 32, and 35	§ 103 based on <i>Sinclair</i> and <i>Toombs</i>

5	12, 13, 28, 29	§ 103 based on <i>CompactFlash</i> and <i>Elhamias</i>
6	12, 13, 28, 29	§ 103 based on <i>Ziv, Vogt</i> , and <i>Elhamias</i>

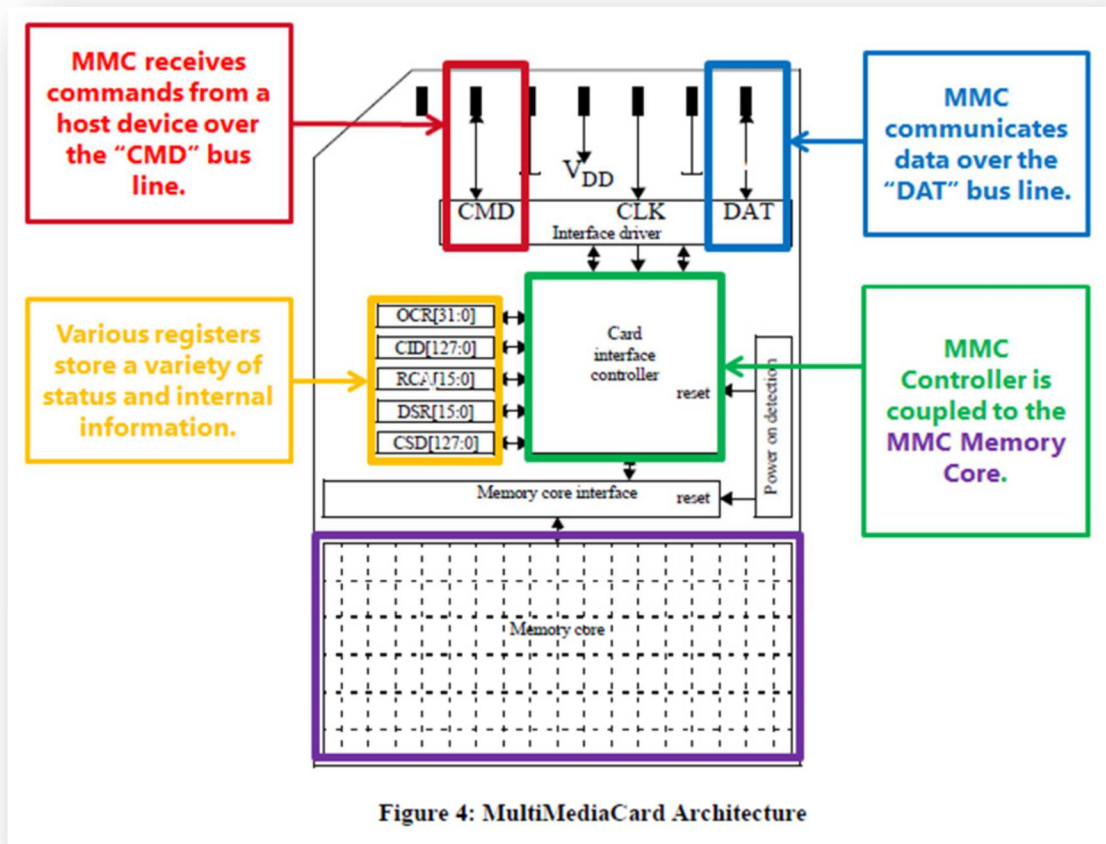
The Declaration of R. Jacob Baker, Ph.D., P.E., filed herewith (Ex. 1002, “Baker Decl.”), supports the challenge in this Petition that the Challenged Claims are invalid as anticipated and obvious.

IV. A PERSON OF ORDINARY SKILL IN THE ART

Relative to the ’180 Patent, a person of ordinary skill in the art (“POSITA”) is a person having at least a bachelor’s degree in electrical engineering, computer engineering, or equivalent training, with at least two years of academic or industry experience in the field of memory system design. Ex. 1002 at ¶¶65. However, a higher level of education could make up for less experience, and vice versa. *Id.*

V. BACKGROUND OF THE TECHNOLOGY

A memory device is used to store electronic data. Ex. 1002 at ¶¶68-71. By 2008, several types of memory devices that use flash or EEPROM memory were in existence, including MultiMediaCard (“MMC”) and CompactFlash (“CF”). *Id.* at ¶¶71. A memory device can communicate with a host device. Ex. 1010 at 19. As depicted below, for example, an MMC receives commands from a host device over a “CMD” bus and communicates data over the “DAT” bus line. Ex. 1002 at ¶74; *see* Ex. 1010 at 142.



Ex. 1010 at Fig. 4 (annotated).

A MMC also includes a group of registers that can store information about the memory card. *Id.* at 19. For example, the MMC device's CSD (Card Specific Data) register provides information on how to access the memory card, including data format, data transfer speed, etc. *Id.* at 68, Table 22.

VI. OVERVIEW OF THE '180 PATENT

The '180 Patent issued on November 6, 2012 from U.S. Patent Application No. 12/039,672 ('672 Application) filed on February 28, 2008.

A. Summary of the Claimed Subject Matter

The Challenged Claims generally relate to access profiles. An access profile “governs the current access operations to the memory device.” Ex. 1001 at 4:57-58. The Challenged Claims, in particular, relate to activating an access profile and configuring a memory device in accordance with an access profile, so that the device is effective for a usage in accordance with the activated profile.

The access profiles are stored in a register of the memory and correspond to memory access operations, such as “a read, a write, an erase, and a modify attribute operation.” *Id.* at 1:62-64, 5:1-3, 6:17-21, 7:4-13. An access profile can be stored elsewhere. *Id.* at 5:14-17.

The ’180 Patent specification describes the invention as applicable “in any stand-alone or embedded system that comprises or accesses a memory device.” *Id.* at 5:24-27. When connected to such a system, the memory device can “receive one or more commands . . . for activating a particular access profile.” *Id.* at 4:29-32. The portion of the system that issues commands to the memory device is referred to as a “host.” *Id.* at 2:59-63.

The ’180 Patent specification also describes configurations that may correspond to access profiles. For instance, in a “burst profile mode [an access profile], corresponding to fast, contiguous data access,” the memory device is configured so that “after receiving all the data” to be written from a host, it may

“indicate ‘exit busy’ and set the transfer mode to ‘transfer state,’ thus facilitating faster execution of subsequent accesses by the host.” *Id.* at 7:18-21.

Other access profiles may cause the device to configure itself such that a particular profile is “associated with different partitions of the memory device,” including either “logical or physical partitions.” *Id.* at 7:36-37. Similarly, a profile may result in a device configuration such that access operations are “map[ped] ... to certain sections of the physical memory with special characteristics.” *Id.* at 7:49-52. Finally, some access profiles may result in a configuration such that the device postpones “management” or “background operations” until after the data transfer. Ex. 1001 at 3:61-64, 4:43-49.

B. The ’180 Patent Prosecution History

Before issuance of the ’180 Patent, the Applicant responded to three office actions and submitted a notice of appeal and a pre-appeal brief. Ex. 1009 at 327, 393, 406, 440. The resulting ’180 Patent issued on Nov. 6, 2012.

The first office action rejected the claims as anticipated by *Burgan*. *Id.* at 443. *Burgan* teaches smart phones with various profiles, such as a work profile and a family profile, that are accessed in response to caller ID information of a received call. Ex. 1011 at ¶¶5-6.

Applicant’s response to the first office action is relevant to the “command” claim element. According to Applicant, “[a] *command in the context of the*

various embodiments of the present application, and in any other context for that matter, *suggests some type of authoritative direction or instruction to do/not to do something.*” *Id.* at 427 (emphasis supplied). Using this definition, Applicant submitted that a POSITA would not equate the received Caller ID information in *Burgan* with an actual “command,” because a Caller ID is a “passive” identifier. Ex. 1009 at 427.

Unconvinced by the Applicant’s argument, the Patent Office subsequently issued a final rejection on July 6, 2011, maintaining the rejection. *Id.* at 408. In response, Applicant repeated its arguments in a Reply to the Final Office Action. *Id.* at 399-401. Applicant thereafter filed a notice of appeal and a pre-appeal brief. *Id.* at 382, 393-96. The Pre-Appeal Panel decided to withdraw the rejection and issue a new office action. *Id.* at 357.

The Examiner then rejected the claims over *Suwa* and *Bertone*. *Id.* at 329. Applicant made substantial amendments to the claims to distinguish *Suwa* and *Bertone* by further limiting a predefined access profile and the received one or more commands. *Id.* at 259-268. For example, the amendments to Claim 17 are shown below:

17. (Currently Amended) A memory device, comprising:
one or more registers for storing one or more predefined access profiles associated with said memory device, said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;
~~receiving means~~ a controller for receiving one or more commands related to said at least one usage of said memory device, said one or more commands for activating said one or more predefined access profiles associated with said memory device, said controller also
; and
~~_____ configuring means~~ for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.

Id. at 261.

Applicant also clarified the claim limitation, “configuring access to said memory device.” Applicant argued that, unlike the claim requiring “configuring access to said memory device,” the memory device in *Bertone* only configures the memory device according to “timing characteristics to control the speed performance of the memory module.” Ex. 1009 at 266-67. Applicant argued that merely changing an operating speed for the memory device **does not** constitute an access configuration.

Ex. 1012 at Fig. 5 (annotated).

Applicant also contended that *Suwa* does not configure an access profile, because the switcher in *Suwa* “automatically completes necessary changes to use

the selected mode” upon activation. *Id.* at 266. Applicant argued that the claimed invention requires that the **activation** of an access profile **occurs separately** from the **access configuration** of the memory device.

A Notice of Allowance subsequently issued. Ex. 1009 at 244.

VII. CLAIM CONSTRUCTION

A. Legal Overview

The Patent Office has adopted a rule by which claims are construed in accordance with “the standard used in federal courts, in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).” 83 FR 51340. Under this standard, claim construction begins with the language of the claims. *Phillips*, 415 F.3d at 1312-14. The “words of a claim are generally given their ordinary and customary meaning,” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Id.* at 1312-13. The specification is “the single best guide to the meaning of a disputed term and . . . acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication.” *Id.* at 1321 (internal quotation marks omitted). The prosecution history is another source of intrinsic evidence. *Id.* at 1317.

All claim terms of Challenged Claims of the '180 Patent have been accorded their plain and ordinary meaning as understood by POSITA and consistent with the intrinsic record. Petitioner's interpretation of the claim terms in the '180 Patent is further explained for each claim limitation in relation to the prior art discussed in the proposed grounds for invalidity, below, in Grounds 1-6.

Under the *Phillips* standard and for clarity, Petitioner provides the following specific constructions.¹

B. Claim Terms

1. "predefined access profile"

The Challenged Claims describe "access profiles" in several different ways. An access profile may be a mode, setting, control, or logic for an access operation, each of which is disclosed in the specification. The Board should construe "predefined access profile" to mean a "mode, setting, control, or logic defined in advance for reading, writing, modifying, deleting, or changing the attributes of data." Ex. 1002 at ¶¶127-129

¹ Petitioner reserves the right to address any claim construction positions taken by the Patent Owner in its Preliminary Response, if any, including under 37 C.F.R. § 42.108(c). Petitioner further reserves its ability to show that claims of the '180 Patent are invalid under 35 U.S.C. §112 in the co-pending litigation, despite offering explicit and implicit claim constructions herein.

For example, the '180 Patent discloses that a profile can be a mode: “one profile may be defined as a burst profile **mode**, corresponding to a fast, contiguous data access **mode**.” Ex. 1001 at 7:15-18 (emphasis added); *see also id.* at Claim 18 (reciting predefined access profiles that “correspond to at least one of a random and a sequential mode of access”); *id.* at 4:44-52 (random mode profile).

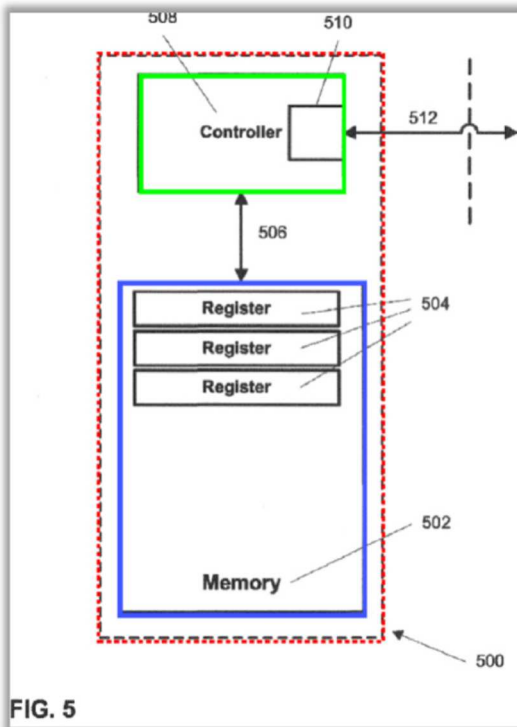
The specification also describes that profiles can be a control or setting: “the access profile associated with a media device may be adapted to comprise different **control and/or setting** profiles that are associated with different partitions of the memory device.” *Id.* at 7:33-36 (emphasis added). Lastly, the specification states that “an access profile may be implemented as a binary file that further comprises the required **logic** to implement an access profile.” *Id.* at 5:14-19 (emphasis added).

2. **“configuring access”**

The Challenged Claims provide that the “predetermined access profiles” configure access to the “memory device.” The Board should construe “configuring access” to mean “setting the memory device for reading, writing, modifying, deleting, or changing the attributes of data.” Ex. 1002 at ¶¶130-132.

In Fig. 5 of the '180 Patent, the “memory device” (red box) includes many components. Ex. 1001 at Fig. 5; 4:26-42. For example, as depicted below, memory device 500 contains a “memory” 502 (blue box), “controller” 508 (green

box), an interface (506) through which communications between the controller and the memory may be conducted, and another interface (512) for communications with a host device.



Id. at Fig. 5.

Thus, the proposed construction provides that the predefined access profiles can also configure data on the controller (green box) or other components of the “memory device” (red box), as indicated by the intrinsic evidence. Ex. 1002 at ¶¶130-132.

3. “usage”

The Challenged Claims provide that the term “usage” is associated with use of the claimed memory device by the host. The Board should construe the term “usage” to mean “host activity in accordance with the predefined access profile.” Ex. 1002 at ¶¶133-134.

For example, the Challenged Claims provide that the memory device “receives one or more commands related to a least one usage of said memory device and that the predefined access profiles” determine how access is configured for said at least one usage. Ex. 1001 at 2:39-67, Claim 1 (emphasis added). Because the commands are “received” for a usage “of the memory device” and the “access is configured” for the usage, it is clear that “usage” refers to host activity, as that is where the commands can originate and the device that is accessing the memory card. This is also clear from the specification. Specifically, the ’180 Patent states that an access profile “governs the current access operations to the memory device” by the host device. Ex. 1001 at 4:52-59.

VIII. SUMMARY OF THE PRIOR ART

A. CompactFlash

A CompactFlash device is a flash memory mass storage device. Ex. 1002 at ¶136. SanDisk first manufactured a CompactFlash device in 1994. Ex. 1014 at 1:56-59. CompactFlash quickly became the go-to portable mass storage device for

electronic devices. Ex. 1002 at ¶137. CompactFlash remains popular and is supported by many devices. *Id.*

In 1995, the CompactFlash Association was formed by a group of international companies with the goal of creating an industry standard for flash-based mass storage. *Id.* at ¶138. The CompactFlash specification establishes the methods, processes, and practices for both the CompactFlash device and a host interacting with the device. *Id.* at ¶136.

On December 23, 2004, the CompactFlash Association released CompactFlash Specification Revision 3.0 (*CompactFlash*). Ex. 1003 at 1; Ex. 1025 at ¶7 (Declaration of Michael Asao, consultant for the CompactFlash Association). *CompactFlash* was made publicly available to any interested member of the public free of charge prior to 2008, as, for example, the CompactFlash Association publicly announced on January 6, 2005 that *CompactFlash* “is available to download free from the CFA website at <http://www.compactflash.org>.” Ex. 1024 at 9; Ex. 1023 at ¶6 (authenticating page 9 of Ex. 1024 as an accurate representation of the January 6, 2005 announcement by the CompactFlash Association); *see also* Ex. 1015 (Jan. 7, 2005 article stating that “[t]he CF Specification Revision 3.0 is available to download free from the CFA web site at <http://www.compactflash.org>”); Ex. 1016 at ¶3 (describing an

exemplary hard drive that utilizes a CompactFlash interface “as described in the CF+ and CompactFlash Specification Revision 3.0, published by the CompactFlash Association, Palo Alto, Calif., Dec. 23, 2004, <http://www.compactflash.org>.”) (published on Apr. 5, 2007).

Moreover, *CompactFlash* was freely and publicly available online from the CompactFlash website as of at least January 13, 2005. Ex. 1025 at ¶7; Ex. 1024 at 2-3 (displaying the CompactFlash homepage indicating that *CompactFlash* “is now available to download” on Jan. 13, 2005); *Id.* at 6 (displaying the registration form that once submitted included a link for a free download for *CompactFlash*); Ex. 1023 at ¶6 (authenticating pages 2-3 of Ex. 1024 as an accurate representation of the CompactFlash Association website on Jan. 13, 2005 and page 6 of Ex. 1024 as an accurate representation of the CompactFlash registration form on January 27, 2005). *See Crestron Electronics Inc. v. Intuitive Building Controls Inc.*, Case IPR2015-01460, slip op. at 12-22 (PTAB Jan. 14, 2016) (Paper 14). Accordingly, *CompactFlash* qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 102(b). *CompactFlash* was not previously presented to the PTO in the context of the ’180 Patent.

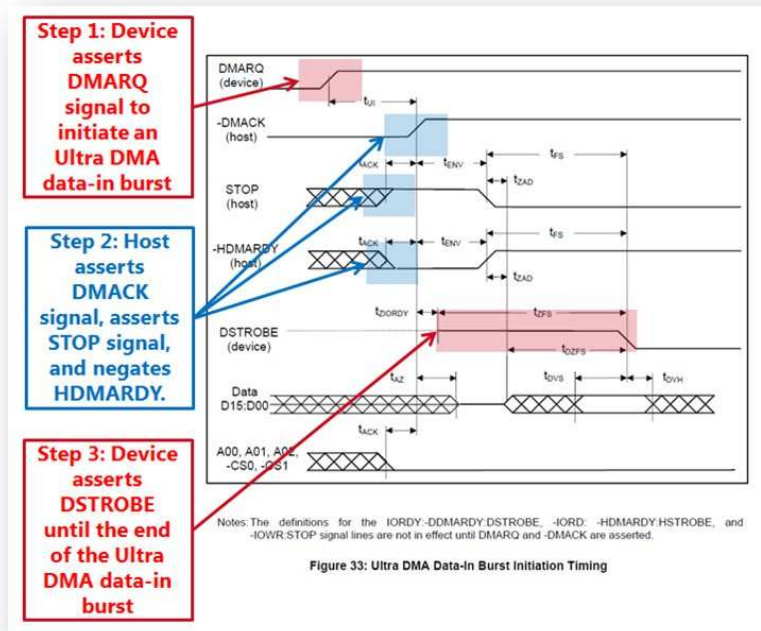
The CompactFlash Association made improvements to direct memory access (DMA) data transfer in Revision 3. A DMA data transfer occurs directly

between the hardware subsystem and the memory device, rather than involving the host's CPU as an intermediary. Ex. 1002 at ¶143. In this manner, transfer speeds are boosted and the CPU is freed to work on other tasks while the transfer occurs. *Id.* Starting with Revision 3.0, "UltraDMA" was introduced, which boosted DMA transfer speed four-fold from the prior "MultiWord DMA" transfer. Ex. 1015 ("Ultra DMA 33 and UltraDMA66 [sic] interface modes will increase the CompactFlash interface data transfer rate to 66 MB/sec.").

CompactFlash also introduced several Ultra DMA modes. Ex. 1003 at 137. A CompactFlash controller configures a CompactFlash device to perform the Ultra-DMA transfer according to a protocol based on the mode selected. When a host sets an Ultra DMA mode, the memory device automatically disables any enabled MultiWord DMA mode. *Id.* at 158. In response, the memory device sets the selected Ultra DMA mode in a task file register. *Id.* at 120.

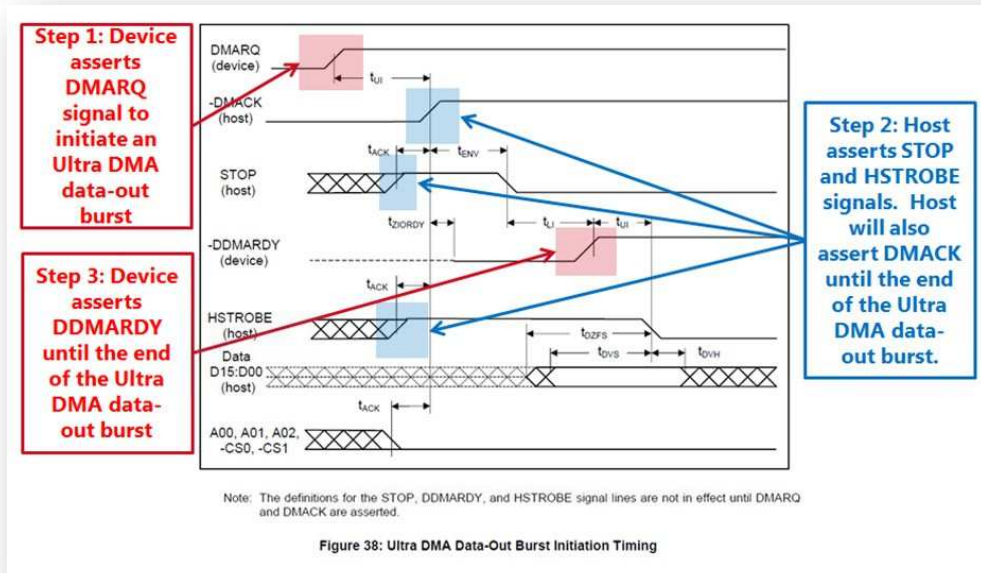
The host may subsequently communicate a READ DMA or WRITE DMA command to transfer data to the device. *Id.* at 52. The CompactFlash device, in response, will begin the Ultra DMA-specific initiation protocol to configure the memory device for an Ultra DMA transfer. *Id.* at 68-70. As illustrated for a data-in burst in Fig. 33 and a data-out burst in Fig. 38 (both shown below), the controller starts the initiation phase of the Ultra DMA burst by asserting a

DMARQ signal. *Id.* at 75-76, 81-82. After the host responds by asserting and/or negating several signals, the controller will assert either a DSTROBE signal or DDMARDY signal until the end of the burst. *Id.* at 75-76, 81-82. Finally, unlike



the older MultiWord DMA modes, the device will calculate a CRC value to ensure the accuracy of the data transferred in the Ultra DMA modes. *Id.* at 90. If the memory device detects errors, an Error Register is updated to reflect the error. *Id.* at 90.

Id. at Fig. 33 (annotated).

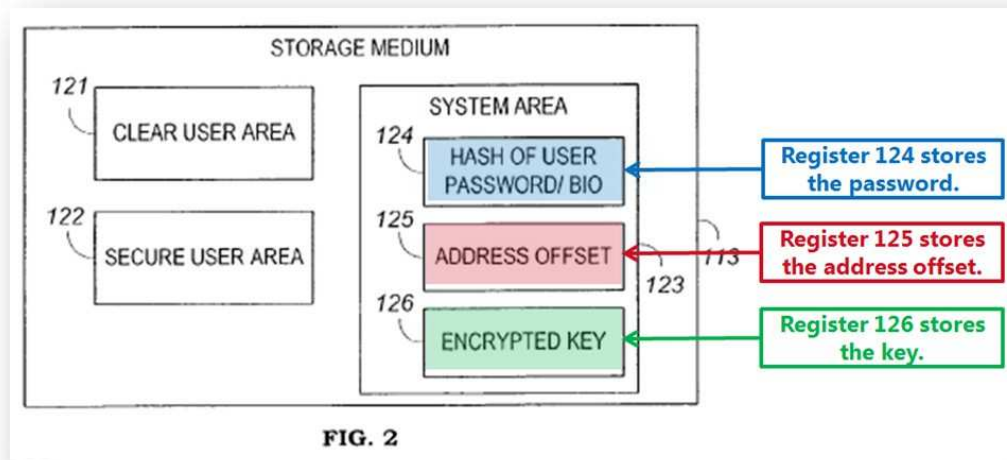


Id. at Fig. 38 (annotated).

B. United States Patent No. 7,478,248 (*Ziv*)

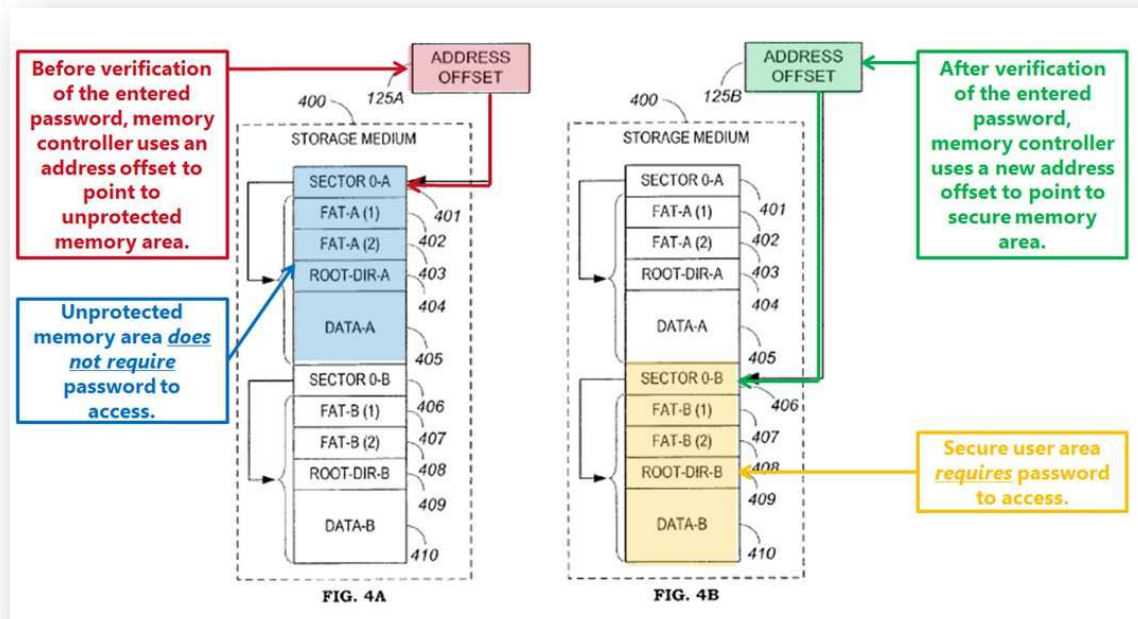
Ziv was filed November 27, 2002, and published on May 27, 2004. *Ziv* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Ziv* was not previously presented to the PTO in the context of the '180 Patent.

Ziv discloses a memory controller that allows profile-based access to an encrypted partition of memory. Ex. 1004 at Abstract. A user first selects a password that is hashed and stored in a register. *Id.* at 4:15-20. The system also generates a cryptographic key, which is used with a stored address offset for accessing the secure area. *Id.* at 5:14-15.



Id. at Fig. 2 (annotated).

The secure memory area is activated when the host transmits a valid password to the controller. *Id.* at 6:15-22. Then the memory controller remounts the memory by using the stored address offset in the register to point to the secure partition (as illustrated in Fig. 4B). *Id.* at 6:42-49, Fig. 4B (shown below).



Id. at Figs. 4A-B (annotated).

C. United States Patent No. 6,681,304 (Vogt)

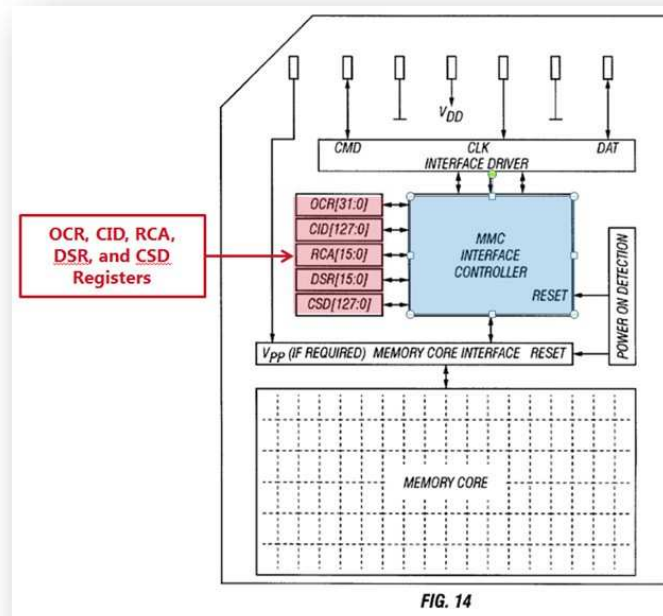
Vogt was filed June 30, 2000 and issued on January 20, 2004. *Vogt* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Vogt* was not previously presented to the PTO in the context of the '180 Patent.

Vogt teaches a "password verify" command to access hidden storage in a memory device. Ex. 1005 at 6:35-37, 8:11-30, 11:53-55.

D. United States Patent No. 6,279,114 (Toombs)

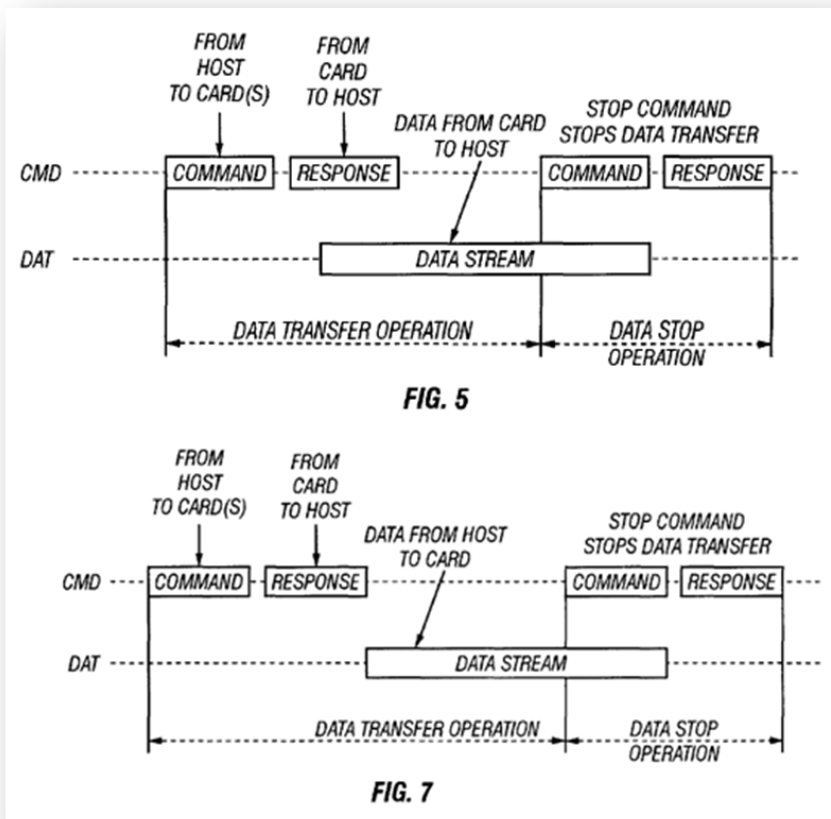
Toombs was filed November 4, 1998, and issued on August 21, 2001. *Toombs* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Toombs* was not previously presented to the PTO in the context of the '180 Patent.

Toombs teaches a MultiMediaCard having parameters stored in various registers as shown in Fig. 14 below. Ex. 1006 at 1:9-14, 6:18-38, 10:22-33, Fig. 14.



Id. at Fig. 14 (annotated).

Toombs also teaches two types of data transfer processes. *Id.* at 8:34-34. One type involves sequential data transfer commands, which initiate a sequential, “continuous data stream.” *Id.* at 8:35-37; Fig. 5, 7 (shown below); Ex 1002 at ¶191. The sequential data transfer commands reduce command overhead to a minimum, because data is transferred sequentially in a DAT line. Ex. 1006 at 8:39-43.



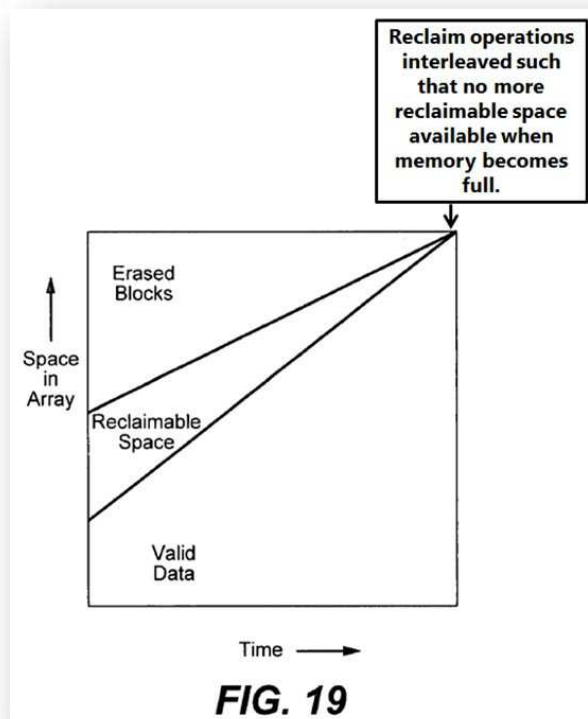
Id. at Figs. 5, 7.

E. United States Patent No. 7,409,489 (*Sinclair*)

Sinclair was filed on October 25, 2005, claims priority to U.S. Provisional App. No. 60/705,388 filed on August 3, 2005, and was published on February 8, 2007. *Sinclair* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Sinclair* was not previously presented to the PTO in the context of the '180 Patent.

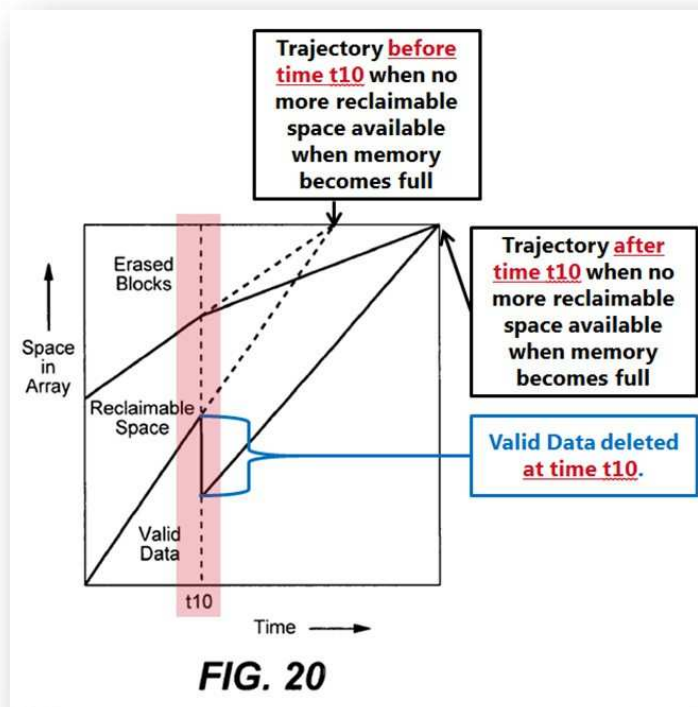
Sinclair discloses selectable reclaim operation modes that provide optimizations to the rate that memory reclaim operations (*i.e.*, background/management operations) occur. Ex. 1007 at Abstract. Reclaim

operations convert memory containing obsolete data into writeable memory. *Id.* at 2:9-11. An exemplary reclaim operation mode is the Reclaim Normal mode, which can be activated by the host sending a “Reclaim_normal” command to the memory controller. *Id.* at 23:27-30, 23:47-51. This changes the configuration of the memory device to interject reclaim operations between write commands received from the host. *Id.* at 23:47-51, 2:50-57. The device calculates an optimal interleave ratio of reclaim operations to write commands such that the memory card will run out of writeable memory only when no reclaimable memory remains. *Id.* at 2:50-57.



Id. at Fig. 19 (displaying a time graph illustrating an optimal interleave of reclaim operations to write operations) (annotated).

The interleave ratio can be recalculated periodically or when triggered by a host command. *Id.* at 18:17-26. As shown in Fig. 20, when host issues a delete command to the memory device at time t_{10} , the system alters the interleave ratio such that the time when no more reclaimable space is available shifts to the newly anticipated time when the memory will be filled to capacity. *Id.* at 18:12-26.



Id. at Fig. 20 (annotated).

Sinclair also describes other reclaim modes selectable by the host, such that that “the host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity.” *Id.* at 23:27-30, 23:36-59.

F. United States Patent Publication No. 2006/00220054 (*Elhamias*)

Elhamias was filed on July 28, 2004 and was published on February 2, 2006. *Elhamias* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Elhamias* was not previously presented to the PTO in the context of the ’180 Patent.

Elhamias discloses a memory card that adapts its operation according to the application to which it is applied or the conditions under which it is operated. Ex. 1006 at ¶8. *Elhamias* further discloses that the “maximum rate of data transfer between the host and the card is limited by the number of parallel data paths that are used.” *Id.* at ¶22. Thus, the memory card is able to receive data in parallel for its storage and send data to the host in parallel from the memory. *Id.*

IX. GROUND FOR CHALLENGE

Inter partes review of Claims 1-3, 5, 12-13, 16-19, 21, 28-29, 32, and 35 of the ’180 Patent is requested as follows.

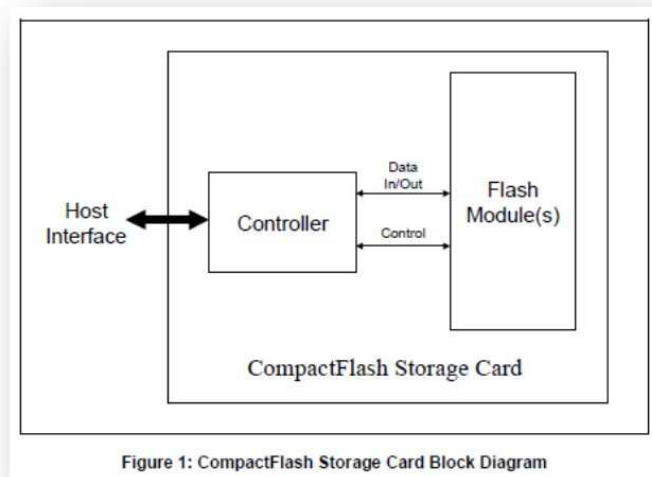
A. GROUND 1: Claims 1-3, 5, 16-19, 21, 32 and 35 are unpatentable under 35 U.S.C. § 102 over *CompactFlash*

As shown below, CompactFlash anticipates Claims 1-3, 5, 16-19, 21, 32 and 35 of the '180 Patent under 35 U.S.C. § 102. *See also* Ex. 1002 at ¶¶203-265.

1. Independent Claim 1

(i) A method for configuring access to a memory device, comprising:

A CompactFlash device is a memory device and contains a “controller and flash memory module(s).” Ex. 1003 at 19; Ex. 1002 at ¶203.

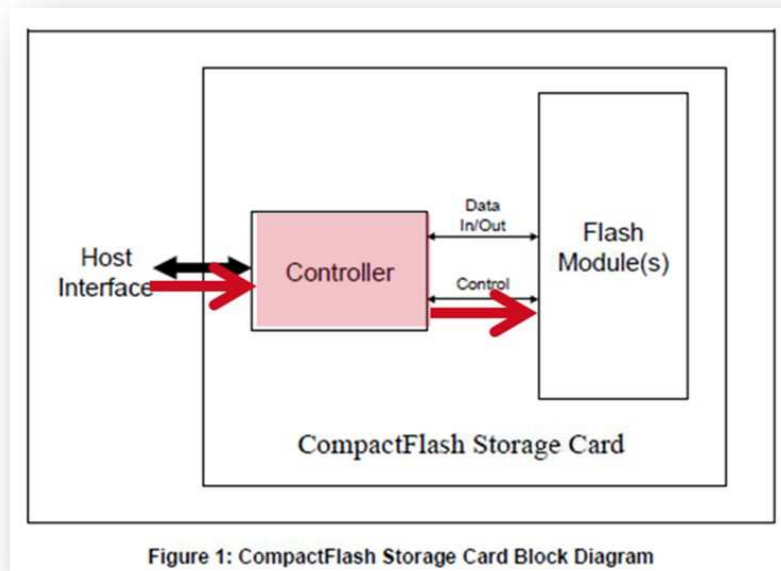


Ex. 1003 at Fig. 1 (annotated).

Furthermore, CompactFlash discloses a method for improvements to direct memory access (DMA) data transfer. Ex. 1003 (“Ultra DMA 33 and UltraDMA66 [sic] interface modes will increase the CompactFlash interface data transfer rate to 66 MB/sec.”); Ex. 1002 at ¶204.

(ii) **receiving one or more commands related to at least one usage of said memory device,**

CompactFlash has a CompactFlash controller, which receives a SET FEATURES command from the host. The SET FEATURES command is communicated from the host to the CompactFlash controller to select one of the MultiWord or Ultra DMA modes. *Id.* at 15, 156-57. The SET FEATURES command instructs the controller to set the DMA mode to the selected MultiWord DMA mode or Ultra DMA mode for subsequent DMA access operations (*i.e.*, the usage), such as READ DMA and WRITE DMA. *Id.* at 15, 157-58.



Id. at Fig. 1 (annotated). Thus, *CompactFlash* discloses this element. Ex. 1002 at ¶¶205-206.

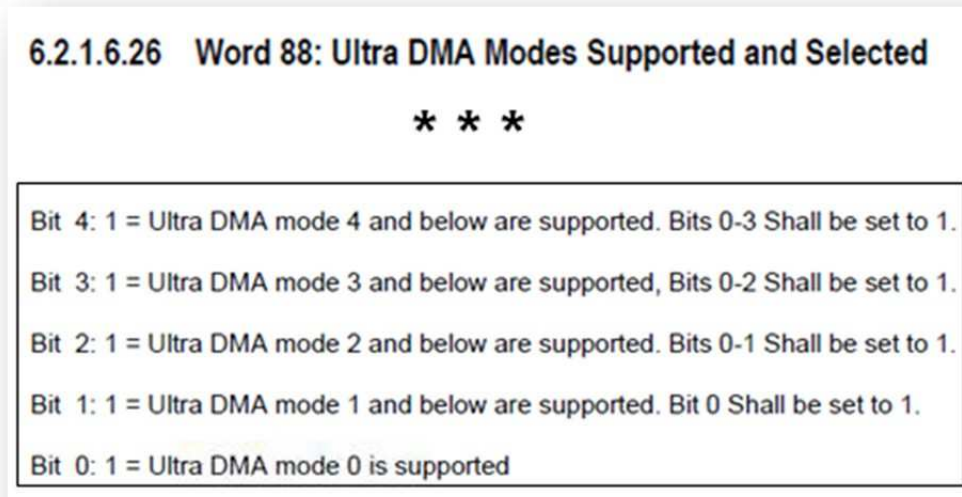
- (iii) **said one or more commands for activating one or more predefined access profiles associated with said memory device,**

CompactFlash discloses MultiWord and Ultra DMA modes stored in a register on the CompactFlash device. As shown in Table 53, below, various MultiWord DMA and Ultra DMA modes are supported, each of which constitutes a pre- defined access profile.

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Id., at 158 (equating MultiWord DMA and Ultra DMA “Mode[s]” as “transfer mode number[s]”). For example, the following Ultra DMA Modes are possible:



Id. at 132-33; 137.

Each DMA mode is an access profile, because the selected mode is used to determine the memory device configuration for the subsequent DMA access operations to the memory device. *See* Ex. 1001 at 3:56-58 (“***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device.***”) (emphasis supplied); Ex. 1002 at ¶¶206-211. For instance, if an Ultra DMA mode is activated (unlike MultiWord DMA modes) the device configures itself to perform a CRC check calculation after the data transfer. Ex. 1003 at 90 (“CRC errors are detected and reported only while operating in Ultra mode.”). In addition, unlike the MultiWord DMA modes, each

Ultra DMA mode uses both the rising and falling edge of the clock signal to transfer data and utilizes HDMARDY, DDMARDY, and DSTROBE signals, which are not part of a MultiWord DMA access operation. Ex. 1002 at ¶211; Ex. 1003 at 44, Fig. 32 (illustrating the MultiWord DMA transfer initialization process).

Furthermore, each Ultra DMA mode is different. As an example, after a pause in an Ultra DMA data burst, a memory device will be prepared to receive up to two additional data words for Ultra DMA Modes 0-2 and up to three additional data word for DMA Modes 3-5. *Id.* at 70. Finally, each mode is associated with different maximum transfer rates. *Id.* at Tables 21-22; Ex. 1002 at ¶233.

Each MultiWord and Ultra DMA mode is effective for determining access configuration for the usage. Specifically, the controller configures the CompactFlash device for an access operation according to the host-selected DMA mode. *Cf.* Ex. 1007 at Fig. 32 with Ex. 1007 at Figs. 32, 38 (illustrating the difference in initialization process between a MultiWord DMA transfer and an Ultra DMA transfer). For example, enabling an Ultra DMA mode causes the controller to initiate the Ultra DMA protocol (rather than the MultiWord DMA protocol) when receiving a READ DMA or WRITE DMA command (*i.e.*, at least one usage of the memory device) from the host. Ex. 1003 at 68. Similarly,

enabling a MultiWord DMA mode causes the controller to initiate the MultiWord DMA protocol (rather than the Ultra DMA protocol) when receiving a READ DMA or WRITE DMA command (*i.e.*, usage) from the host. Ex. 1003 at 68; Ex. 1002 at ¶¶209-11.

These DMA modes are access profiles because use of each DMA Mode requires the use of a specific DMA *protocol*, not merely the selection of particular timing characteristics. Ex. 1003 at 68 (“[T]he *Ultra DMA protocol* shall be used instead of the *Multiword DMA protocol*.... This protocol applies to the Ultra DMA data burst only.”). *See* Ex. 1009 at 266-67. Moreover, in the example of Ultra DMA, “[s]everal signal lines are redefined to provide different functions during an Ultra DMA burst.” *Id.* at 68.

Furthermore, unlike the Applicant’s argument in the Prosecution History that changing the operating speed does not affect an access operation, the DMA modes ***directly affect*** access operations. Ex. 1009 at 266-67. The selected DMA mode dictates the specific DMA protocol that the memory device utilizes. Moreover, the selection of an Ultra DMA profile rather than a MultiWord DMA profile requires the device to perform a CRC comparison to ensure the accuracy of the data transferred. Ex. 1003 at 90 (“CRC errors are detected and reported ***only while operating in an Ultra mode.***”) (emphasis supplied); Ex. 1002 at ¶210.

With respect to the commands for activating one or more predefined access profiles, the SET FEATURES command sent from the host activates a selected MultiWord DMA mode or Ultra DMA mode (*i.e.*, a predefined access profile) from among the available modes supported by the device. Ex. 1003 at 157, Table 53 (indicating bits representing a host-selected DMA mode) (shown below).

Table 53: Transfer mode values		
Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Ex. 1003 at Table 53 (annotated).

For example, for Ultra DMA modes, the Set transfer mode subcommand (using the transfer mode values in Table 53) in the SET FEATURES command allows “a host to select the Ultra DMA mode at which the system operates.” *Id.* at 69.

Thus, *CompactFlash* discloses this element. Ex. 1002 at ¶¶207-211.

(iv) **said predefined access profiles being effective for determining how access to said memory device is configured for said at least one usage; and**

As discussed above, *CompactFlash* discloses that each MultiWord and Ultra DMA mode (*i.e.*, predefined access profile) is effective for determining how access to the memory device is configured for a usage. *See supra* Section IX.A.1(ii); Ex. 1002 at ¶¶212-213.

The “usage” in *CompactFlash* relates to the host activity in accordance with the selected DMA mode (*e.g.*, a READ DMA or WRITE DMA operation). Ex. 1003 at 68. Specifically, the controller configures the CompactFlash device for a host- initiated access operation according to the host-selected DMA mode. *Cf.* Ex. 1003 at Fig. 32 *with id.* at Figs. 32, 38 (illustrating the difference in initialization process between a MultiWord DMA transfer and an Ultra DMA transfer). For example, enabling an Ultra DMA mode causes the controller to initiate the Ultra DMA protocol (rather than the MultiWord DMA protocol) when receiving a READ DMA or WRITE DMA command from the host. *Id.* at 68. Similarly, enabling a MultiWord DMA mode causes the controller to initiate the MultiWord DMA protocol (rather than the Ultra DMA protocol) when receiving a READ DMA or WRITE DMA command from the host. *Id.* at 68.

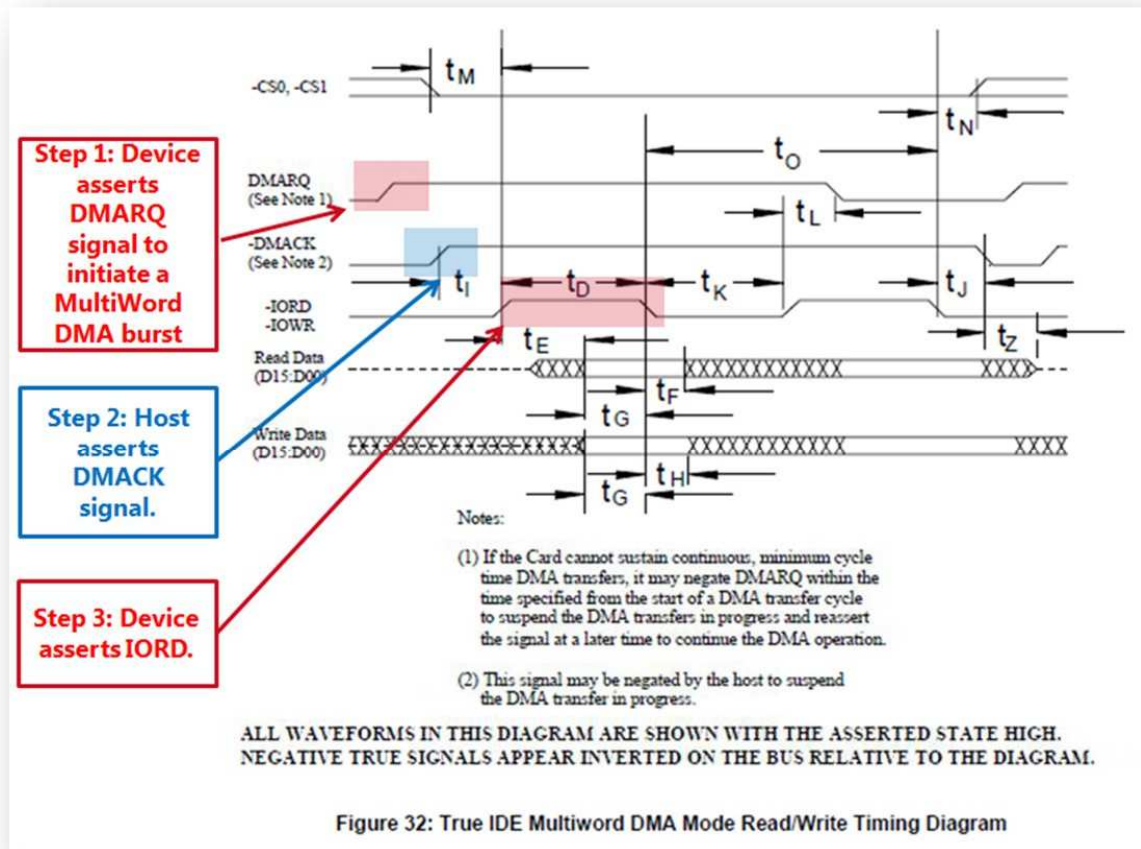
(v) **configuring access to said memory device in accordance with at least one of said access profiles so**

that said memory device is effective for said at least one usage.

The CompactFlash controller configures the access to the memory device according to the selected DMA mode (*i.e.*, one of the MultiWord or Ultra DMA modes), so that the CompactFlash device is effective to perform a DMA access operation (*i.e.*, usage) using the selected DMA mode. Ex. 1002 at ¶¶214-215.

After a host communicates a READ DMA or WRITE DMA command following the selection of a DMA mode, the controller will begin the DMA-specific initiation protocol to configure access to the memory device for either a MultiWord DMA transfer or an Ultra DMA transfer in the selected mode. *Id.* at Figs. 32-33, 38.

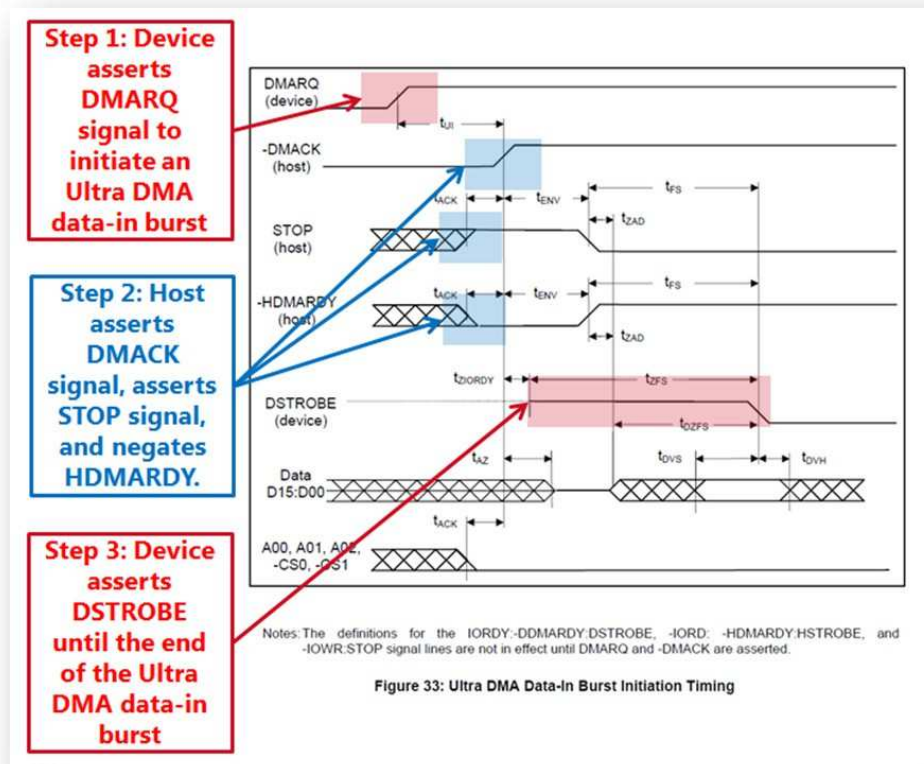
For example, in a MultiWord DMA mode, the controller starts the initiation phase of the MultiWord DMA burst by asserting a DMARQ signal (Step 1 of Fig. 32). The host, in response, asserts a DMACK signal (Step 2 of Fig. 32), and, in turn, the controller responds by asserting the IORD signal (Step 3 of Fig. 32).



Id. at Fig. 32 (annotated).

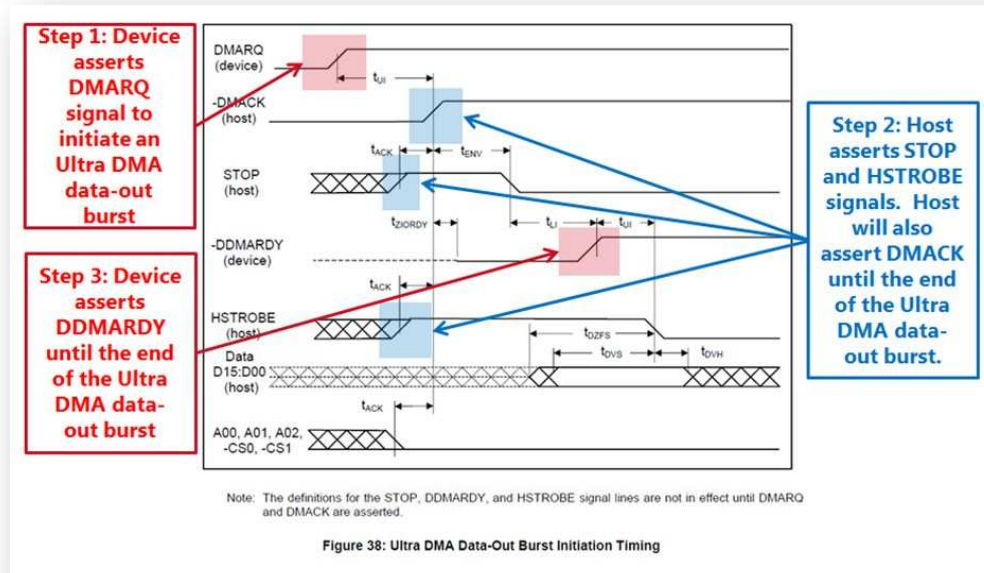
As another example, when an Ultra DMA mode is activated, the controller starts the initiation phase of the Ultra DMA burst by asserting a DMARQ signal (Step 1 of Fig. 33). *Ex. 1003* at 76. The host then asserts a DMACK signal (Step 2 of Fig. 33). *Id.* at Fig. 33. Only at that point do the other signal lines become effective, permitting the transfer. *Id.* (“The definitions for the ...DSTROBE... and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are

asserted). The device will assert a DSTROBE signal line to start the data-in burst (Step 3 of Fig. 33). *Id.* at Fig. 33.



Id. at Fig. 33 (annotated).

For a data-out burst, the device will wait to negate any signal until generating a STROBE edge (*see* Step 3 of Fig. 38). *Id.* at 70. At this point, the memory device is now configured for usage (*i.e.*, to perform a data transfer under the selected Ultra DMA mode).



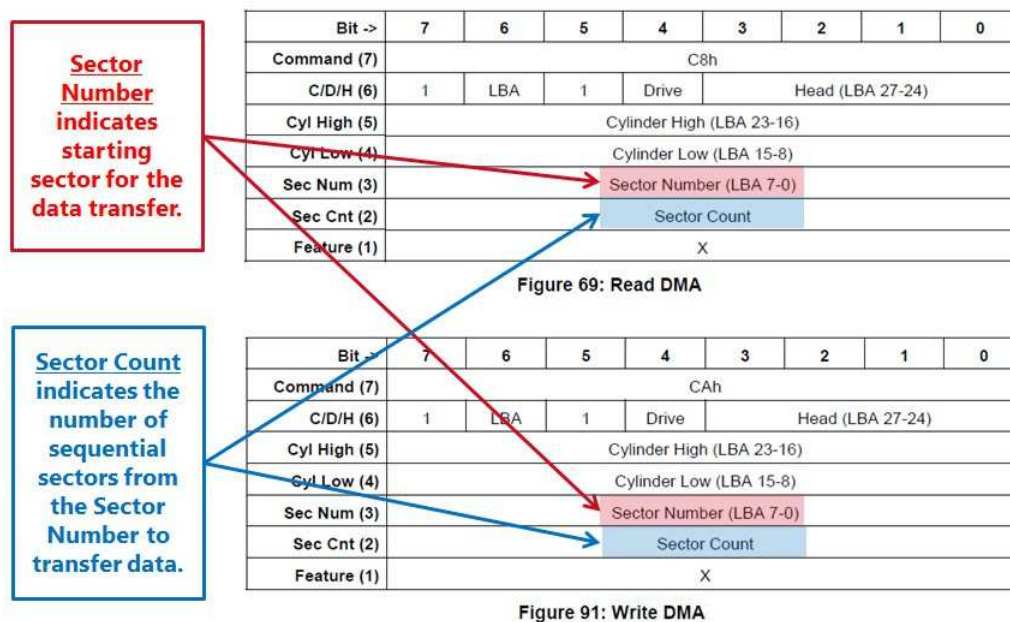
Id. at Fig. 38 (annotated).

2. Dependent Claim 2

- (i) The method of claim 1, wherein said one or more access profiles correspond to at least one of a random and a sequential mode of access.

CompactFlash discloses a READ DMA and WRITE DMA command under one of the MultiWord or Ultra DMA modes (*i.e.*, a predefined access profile) that corresponds to a sequential mode of access. Ex. 1003 at 145 (“[The Read DMA] command uses DMA mode *to read from 1 to 256 sectors as specified in the Sector Count* register.... *The transfer begins at the sector specified in the Sector Number Register*”), 164 (“[The Write DMA] command uses DMA mode *to write from 1 to 256 sectors as specified in the Sector Count* register.... *The transfer begins at*

the sector specified in the Sector Number Register.”) (emphasis added). The CompactFlash device performs read and write access operations by accessing the starting place of the transfer in the memory (*i.e.*, the Sector Number) and continuing for a number of sequential sectors (*i.e.*, the Sector Count). *Id.* at 145, 164; Ex. 1002 at ¶¶216-27.



Ex. 1003 at Figs. 69, 91 (annotated).

Accordingly, READ and WRITE DMA operations correspond to a sequential mode of access. *See id.* at 145; Ex. 1002 at ¶226. Both start at a specified Sector Number and continue to access (*i.e.*, read or write) in sequence the number sectors indicated in the Sector Count. Ex. 1003 at 145, 164; Ex. 1002 at ¶¶218-25.

3. Dependent Claim 3

- (i) **The method of claim 2, wherein said access profiles correspond to at least one of a read, a write, an erase, and a modify attribute operation.**

In *CompactFlash*, the various DMA profiles correspond to and support READ DMA (*i.e.*, a read operation) and WRITE DMA (*i.e.*, a write operation). Ex. 1003 at 145, 164; Ex. 1002 at ¶¶228-230.

4. Dependent Claim 5

- (i) **The method of claim 1, wherein said one or more access profiles are adapted to produce an optimized performance associated with said memory device.**

For purposes of the Petition, Petitioner applies Patent Owner’s proposed construction in the above-identified related matter of the claim term “adapted to produce an optimized performance associated with said device” in Claim 21 to mean “designed to produce an improved memory device performance with higher reliability, increased speed, increased lifetime, or reduced energy consumption, than compared to the same memory device not implementing said one or more access profiles.” Ex. 1022 at 21. *CompactFlash* discloses this subject matter. Ex. 1002 at ¶¶231-233.

Each DMA mode is designed to produce an improved memory device performance with increased speed (*i.e.*, higher throughput). Ex. 1002 at ¶233; *see, e.g.*, Ex. 1015 (“Ultra DMA ... modes will increase the CompactFlash interface

data transfer rate[.]”). Each DMA mode is an optimization as it “reduces the processor power required to manage the CompactFlash data transfers.” *Id.* Moreover, at the time of *CompactFlash*, the Ultra DMA modes provided the maximum read and write speed available to CompactFlash devices. *Id.*

In addition, in reading and writing data in an Ultra DMA transfer, the host device and the memory controller perform error detection. Ex. 1003 at 90 (“CRC errors are detected and reported only while operating in Ultra mode.”). The host device may select a slower Ultra DMA mode if excessive errors are encountered, thereby improving the reliability of the memory device performance. *Id.*

5. Dependent Claim 16

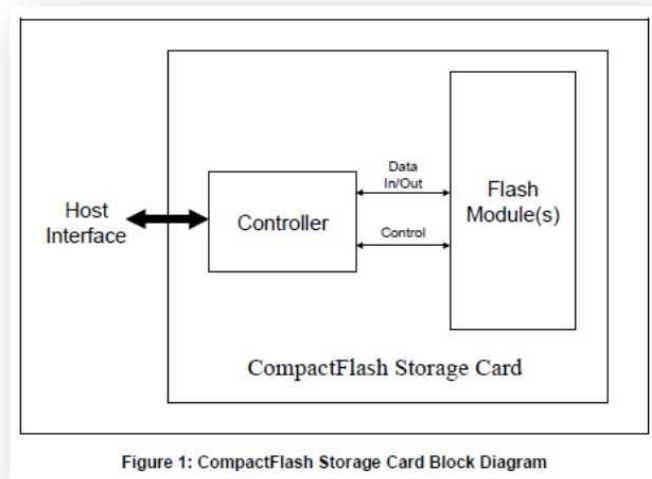
- (i) **The method of claim 1, further comprising a default access profile that is used to configure said memory device upon power up.**

When executing a power-on or hardware reset, *CompactFlash* discloses that the device may revert to a default non-Ultra DMA mode, like a MultiWord DMA mode. Ex. 1003 at 69. As discussed above, each MultiWord DMA mode may be an access profile. *See supra* IX.A.1(iii); Ex. 1002 at ¶234.

6. **Independent Claim 17**

(i) **A memory device, comprising:**

A CompactFlash device is a memory device and contains a “controller and flash memory module(s).” Ex. 1003 at 19; Ex. 1002 at ¶203.



Ex. 1003 at Fig. 1 (annotated).

(ii) **one or more registers for storing one or more predefined access profiles associated with said memory device,**

The predefined profiles are stored in the card and are available via the “IDENTIFY DEVICE data [which] indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting.” Ex. 1003 at 69, 128 (“Table 47 specifies ... data returned by the Identify Device Command”), 132-33. The IDENTIFY DEVICE data also indicates support of certain MultiWord DMA modes. *Id.* at 132-33.

For instance, Word 88 of the Identify Device Information “identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected.” *Id* at 137. This data is stored in a portion of memory (*i.e.*, a register) in the device, and is made available to the host via a “buffer” (*i.e.*, register), which the host can access, in response to an IDENTIFY DEVICE command. Ex. 1002 at ¶240; Ex. 1003 at 128 (“The parameter words in the buffer have the ... meanings defined in Table 47[.]”).

Moreover, when the host selects a supported profile, the selected access profile is stored in a register in the CompactFlash device. Ex. 1002 at ¶¶235-240. For example, the host may use the “Set transfer mode subcommand” (designated “Feature 03h”) which is part of the “SET FEATURES” command to “select the Ultra DMA mode at which the system operates.” Ex. 1003 at 69, 156-58. When invoking this subcommand, the selected MultiWord or Ultra DMA mode is identified by storing a value corresponding to the selected access profile “in the Sector Count *register*.” Ex. 1003 at 157 (emphasis supplied).

With respect to storing one or more predefined access profiles associated with said memory devices, *CompactFlash* discloses this subject matter. *See* Section above at IX.A.1(iii); Ex. 1002 at ¶¶235-247.

- (iii) **said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;**

See Section above at IX.A.1.(iv).

- (iv) **a controller for receiving one or more commands related to said at least one usage of said memory device,**

See Section above at IX.A.1.(ii).

- (vi) **said one or more commands for activating said one or more predefined access profiles associated with said memory device,**

See Section above at IX.A.1.(iii).

- (viii) **said controller also for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.**

See Section above at IX.A.1.(v).

7. Dependent Claim 18

- (i) **The memory device of claim 17, wherein said one or more access profiles correspond to at least one of a random and a sequential mode of access.**

See Section above at IX.A.2.(i).

8. Dependent Claim 19

- (i) **The memory device of claim 18, wherein said access profiles correspond to at least one of a read, a write, an erase, and a modify attribute operation.**

See Section above at IX.A.3.(i).

9. Dependent Claim 21

- (i) The memory device of claim 17, wherein said one or more access profiles are adapted to produce an optimized performance associated with said memory device.

See Section above at IX.A.4.(i).

10. Dependent Claim 32

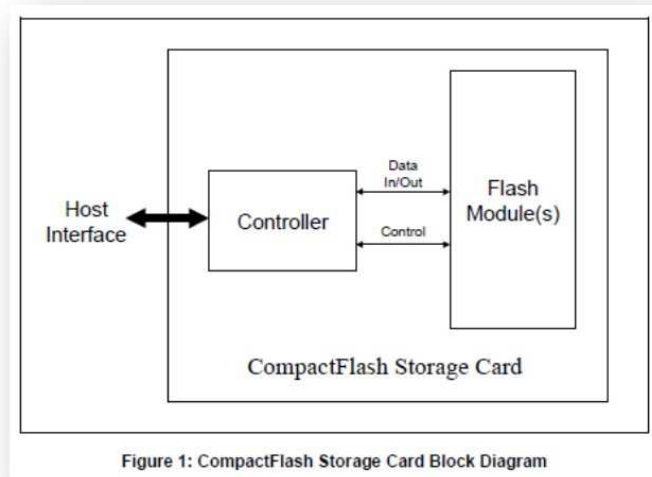
- (i) The memory device of claim 17, further comprising a default access profile that is used to configure said memory device upon power up.

See Section above at IX.A.5.(i)..

11. **Independent Claim 35**

- (i) **A computer program product embodied on a non-transitory computer-readable medium, comprising:**

A CompactFlash device is a memory device and contains a “controller and flash memory module(s).” Ex. 1003 at 19; Ex. 1002 at ¶203.



Ex. 1003 at Fig. 1 (annotated).

To the extent this preamble is limiting, which it is not, the disclosed “controller” in *CompactFlash* is a part of a computing system that manages the operations to be carried out from a computer or software program. Ex. 1002 at ¶¶260-61. Furthermore, a POSITA would understand that the operations and functionality disclosed in CompactFlash as shown in this Ground 1 would necessarily be carried out by a computer program embodied on a non-transitory

computer-readable medium (*i.e.*, as instructions carried out in memory). Ex. 1002 at ¶261.

- (ii) **a computer code for receiving one or more commands related to at least one usage of a memory device,**

See Section above at IX.A.1.(ii).

- (iii) **said one or more commands for activating one or more predefined access profiles associated with said memory device,**

See Section above at IX.A.1.(iii).

- (iv) **said predefined access profiles being effective for determining how access to said memory device is configured for said at least one usage; and**

See Section above at IX.A.1.(iv).

- (v) **a computer code for configuring access to said memory device in accordance with at least one of said access profiles so that said memory device is effective for said at least one usage.**

See Section above at IX.A.1.(v).

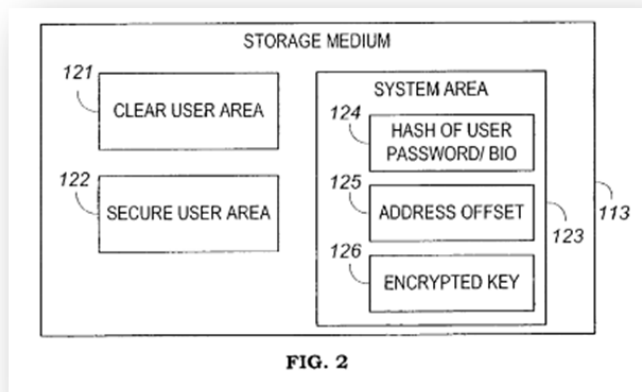
B. GROUND 2: Claims 1, 5, 16, 17, 21, 32, and 35 are unpatentable under 35 U.S.C. § 103(a) in view of *Ziv* and *Vogt*.

As shown below, *Ziv* and *Vogt* render obvious Claims 1, 5, 16, 17, 21, 32, and 35 of the '180 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶266-326.

1. **Independent Claim 1**

(i) **A method for configuring access to a memory device, comprising:**

Ziv discloses a memory device, such as a portable storage device that includes storage memory. Ex. 1004 at 3:48-55, Fig. 2; Ex. 1002 at ¶¶276-77.



Id. at Fig. 2.

Furthermore, *Ziv* discloses at least a method for securing data on a portable storage device and thus configuring access to a memory device, as shown below.

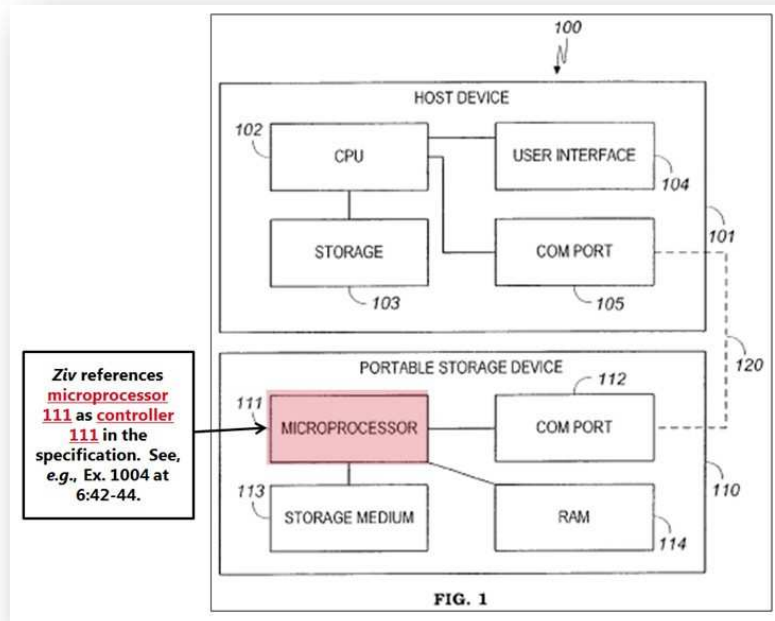
Ex. 1004, *Title* and *Abstract*; Ex. 1002 at ¶¶276.

(ii) **receiving one or more commands related to at least one usage of said memory device,**

Ziv discloses a controller (microprocessor) in the memory device that receives a command indicating the password entered to gain access the secure area.

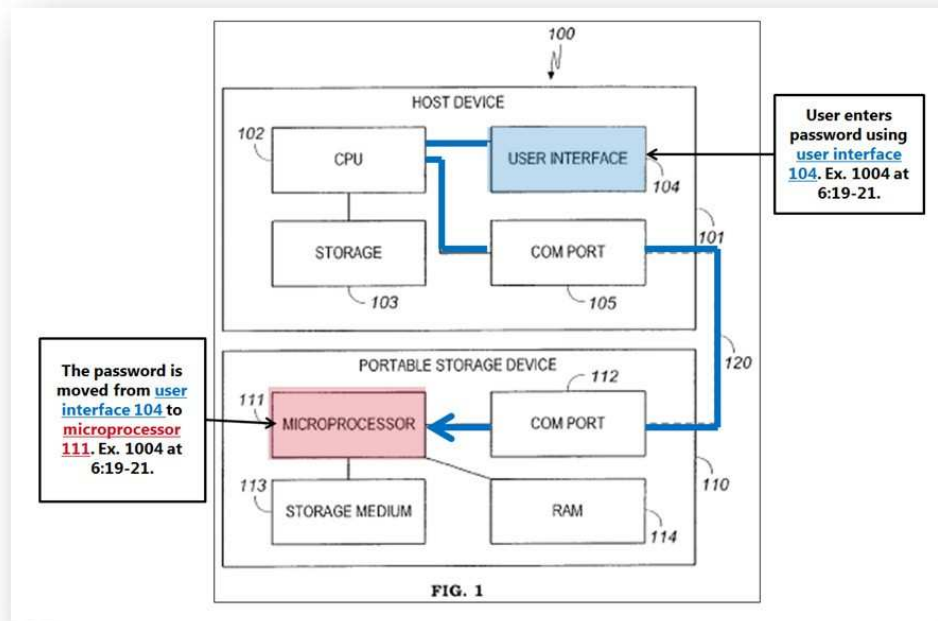
Ex. 1004 at 6:42-44 (“*[C]ontroller 111* dismounts and remounts portable storage

device 110[.]” (emphasis added). A POSITA would understand the microprocessor to be a controller. Ex. 1002 at ¶279.



Ex. 1004 at Fig. 1 (annotated).

The controller receives a command indicating the password entered. *Id.* at 6:19-30 (“If the password has been entered ... via user interface 104, then in step 702 this password is moved to microprocessor 111.... [T]he hashed entered password is then compared to the hashed stored password in register 124.”), Fig. 1 (below). In other words, the host system instructs (*i.e.*, sends a command to) the controller (microprocessor) to use the entered password to gain access to the secure memory area (*i.e.*, the usage). Ex. 1002 at ¶280.



Ex. 1004 at Fig. 1 (annotated).

To the extent the Board disagrees that an instruction to use the entered password to gain access to the secure memory area in *Ziv* teaches the claimed “command,” it would have been obvious nevertheless to use the command-based password authentication method in *Vogt* in the memory device of *Ziv*. In particular, *Vogt* discloses a “password verify” command that communicates the entered password to the flash device, like a MMC card. Ex. 1005 at 6:36-38 (“The OS sends a ‘password verify’ command to the flash. **The command ... includes the entered password.**”) (emphasis supplied). The “password verify” command instructs the internal processor to “compare[] the entered password with the stored password value.” Ex. 1005 at 6:30-32.

It would have been obvious to combine the teachings of *Ziv* and *Vogt* to form a memory controller that receives the “password verify” command in *Vogt* for the following reasons. Ex. 1002 at ¶¶266-275.

Simple Substitution of One Known Element for Another

Ziv’s memory device differs from the claimed device at most by the “command” element. Ex. 1002 at ¶266. Commands, especially commands communicating a password, were well-known in the art to be a fundamental approach to communicating information between devices. *Id.* at ¶¶266, 270; Ex. 1005 at 6:36-38. A POSITA could have substituted one known element (a controller receiving a password) for the other (a controller receiving a command containing the password) and the results would have been predictable (a controller receiving a command containing the password). Ex. 1002 at ¶¶266-69.

Moreover, those predictable results would have included the known advantages of *Ziv*’s memory device, which provides access to a secure memory area, and the known advantages of a command, which include reliably and efficiently communicating a password from the host system to memory device. Ex. 1004 at 6:19-23; Ex. 1005 at 3:23-24; Ex. 1002 at ¶269.

Analogous Art

A POSITA would have been motivated to look to the teachings of the prior art due to the similar field, technology, and time frame of *Vogt* and *Ziv*. Ex. 1002 at ¶270. Both patents concern securing data using non-volatile memory in the early 2000s. Ex. 1004 at 3:48-55; Ex. 1005 at 1:13-15. In addition, both patents describe a solution to a similar problem—improving security of portable flash drives using a secure memory and password. Ex. 1004 at 1:60-63 (“[A] portable storage device for securing data stored in the device in a way that will be both convenient and secure.”); Ex. 1005 at 2:5-12 (“Techniques for implementing hidden storage in a non-volatile memory storage,” where “[t]he hidden storage area cannot be accessed without a valid password.”).

Known Technique to a Known Device to Yield Predictable Results

Base system: *Ziv* discloses a memory device, such as a SecureDigital or CompactFlash device, that receives an entered password from the host system. Ex. 1004 at 6:19-30; Ex. 1002 at ¶273.

Known technique: As shown by *Vogt*, receiving a command containing a password was well-known. Ex. 1005 at 6:36-38.

Predictable results and improved system: A POSITA would have recognized that implementing *Vogt*’s structured communication protocol of the

“password verify command” in *Ziv*’s memory device would yield the predictable result of a memory device that receives an entered password through a structured command, like the password verify command. Ex. 1002 at ¶274.

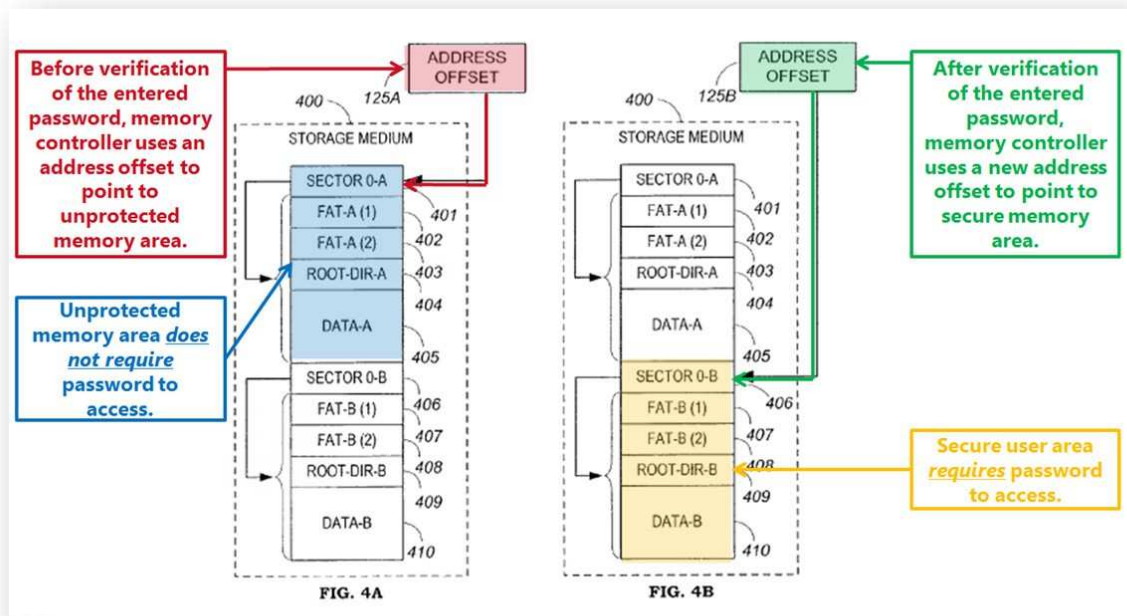
As such, using *Vogt*’s password-command implementation of communicating a password was an obvious design choice to implement *Ziv*’s teaching of communicating a password. *Id.* at ¶¶266-75.

(iii) **said one or more commands for activating one or more predefined access profiles associated with said memory device,**

The password hash, address offset, and key in *Ziv* constitutes a predefined access profile that governs the access operations to the memory. *See* Ex. 1001 at 3:56-58 (“***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device.***”) (emphasis added). Additionally, each of these components forms an access profile. Ex. 1002 at ¶¶283.

Access to the secure user data is only available when a hash of an entered password matches the password hash stored in the register. Ex. 1004 at 4:11-12 (“[A] secure area 122 that contains secure user data [is] accessible only upon the provision of a password[.]”). In addition, the address offset governs access operations to the memory. After entering the proper password, the memory device uses the stored address offset to properly view the secure memory area. Ex. 1004

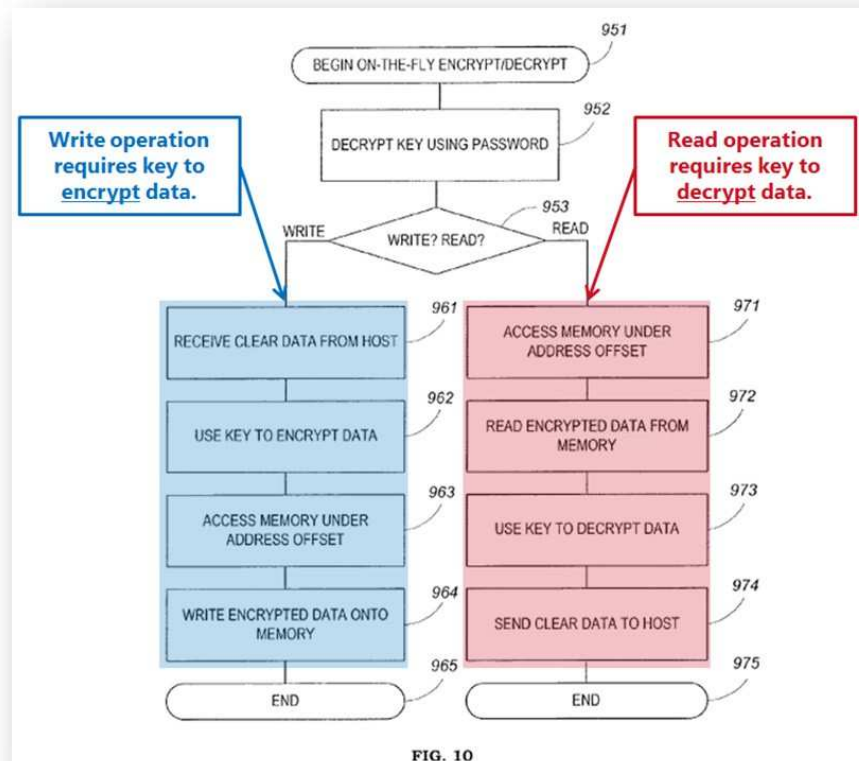
at 6:46-48 (“[H]ost 101 will seek ‘sector 0’ of the remounted device, controller 111 will use offset 125B to point at ‘sector 0-B’ 406[.]”). Without the address offset, the secure area will not be properly mounted (*i.e.*, accessible). *Id.*; Ex. 1002 at ¶284.



Ex. 1004 at Fig. 4A-4B (illustrating the use of the address offset to access the secure area) (annotated).

Moreover, the key governs the access operations to the memory. The key is the “permanent encryption key for all data stored in the secure memory.” *Id.* at 7:7-9. Without the key, a user cannot read or write to the secure area. *Id.* at 7:7-9, 7:36- 46 (instructing the controller to decrypt data being read from and encrypt

data being read to the secure memory area using the key), Fig. 10 (shown below);
Ex. 1002 at ¶285.



Ex. 1004 at Fig. 10 (annotated).

As disclosed above, the command is the entering of the password from a host system to the memory controller. *Ziv* further discloses that a password entry from the host triggers several activation procedures associated with the predefined access profile. The entered password in *Ziv* activates a comparison of a hash of the entered password with the stored password hash. Ex. 1004 at 6:28-30; Ex. 1002 at ¶287.

Additionally, the password in *Ziv* activates the decryption of the stored key. Ex. 1002 at ¶288. When the entered password matches the stored password, the microprocessor decrypts the key of the predefined access profile. Ex. 1004 at 7:32-35.

The communication of a proper password also activates the remounting of the memory according to the address offset. Ex. 1002 at ¶289. After remounting, the stored address offset is used to point to the secure memory area. Ex. 1004 at 6:44-46 (“[W]hen remounting device 110, controller 111 will use an address offset[.]”).

Alternatively, the “password verify” command in the *Ziv-Vogt* combination activates the predefined access profile for substantially similar reasons as discussed above. Ex. 1005 at 6:30-32; Ex. 1002 at ¶¶282-89.

(iv) **said predefined access profiles being effective for determining how access to said memory device is configured for said at least one usage; and**

The “at least one usage,” in the context of *Ziv*, is the host’s access to the secure memory area. *See* Ex. 1004 at 1:60-63.

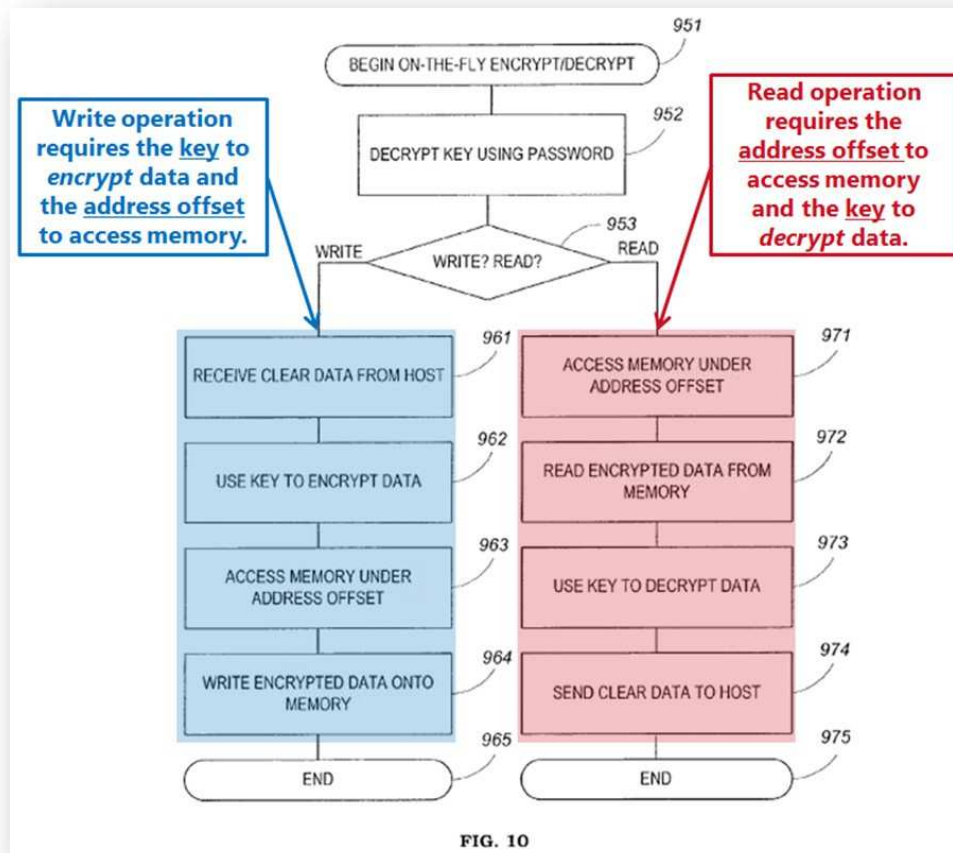
As explained with respect to the previous claim element, the password hash, address, and key in *Ziv* are all effective for determining how access to the memory device is configured, as each is necessary to view, read from, or write to the secure memory area. Ex. 1002 at ¶¶290-293.

- (v) **configuring access to said memory device in accordance with at least one of said access profiles so that said memory device is effective for said at least one usage.**

The controller in *Ziv* configures access to the secure memory area in accordance with the password hash, address offset, and key (*i.e.*, predefined access profile), so that the memory device is effective for the host to view, read from, or write to the secure memory area (*i.e.*, the usage). Ex. 1002 at ¶¶294-296.

The secure memory area is only accessible when the microprocessor uses the stored address offset to point to the proper memory sector, which it does after the user enters the correct password. Ex. 1004 at 6:45-52; Ex. 1002 at ¶295.

The microprocessor must also configure the access operations to perform on-the-fly encryption/decryption. When accessing the secure memory area, the microprocessor must apply the encryption key to properly read from and/or write to the secure memory area. Ex. 1004 at 7:35-46, Fig. 10 (shown below); Ex. 1002 at ¶296.



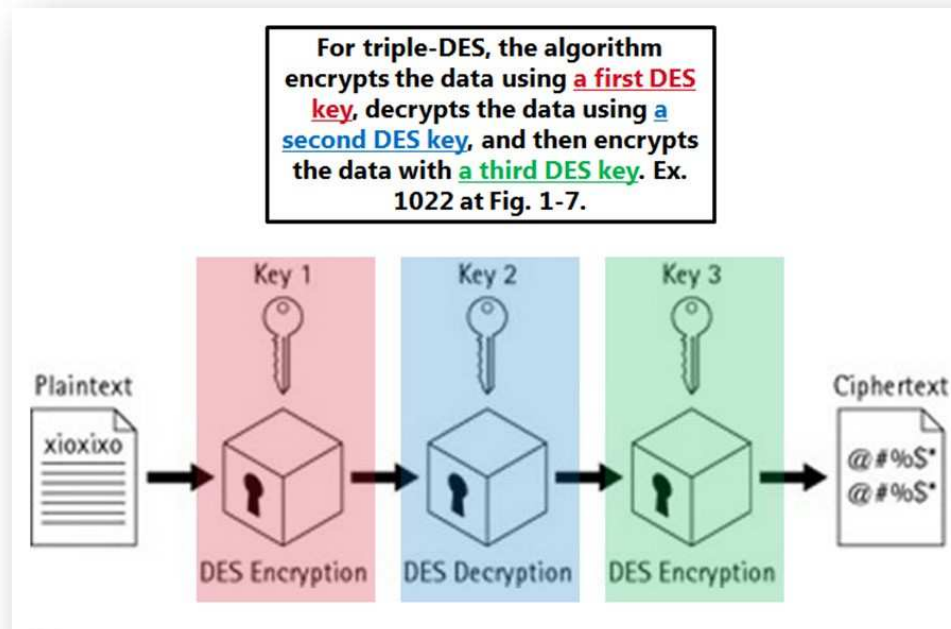
Ex. 1004 at Fig. 10 (annotated)

2. Dependent Claim 5

The access profiles in *Ziv* are adapted to produce an optimized performance when the user enters the password and configures the size of the secure storage memory area. Ex. 1004 at 5:1-8; Ex. 1002 at ¶¶297-203. The provisioning of the password and secure memory storage size optimizes the performance of the memory device by the user selecting the appropriate password and memory storage size deemed fit for the memory device's security and usage. Ex. 1002 at ¶298.

The encryption key and address offset of the access profile also provides an additional optimized performance by allowing the host to properly read from and write to the secure access area of the memory device. *Id.* at ¶299.

Ziv also permits selecting a security algorithm optimized to the “desired security level.” Ex. 1004 at 1:38-41 (“A file that is considered confidential will be encrypted using a common encryption algorithm such as Data Encryption Standard (DES) or triple-DES using a secret key known only to the user.”), 7:9-11 (describing encrypting the key using a “desired security level”); Ex. 1002 at ¶¶300-303. In selecting a security algorithm like DES or triple-DES, the host must balance the speed associated with the security algorithm like DES to the added security that a security algorithm like triple-DES provides. Ex. 1002 at ¶301. For example, a host may implement a DES security algorithm for its speed or a triple-DES security algorithm for its security. Ex. 1018 at 15 (“Triple–DES is a minor variation of DES. Although, three times slower than DES, it can be much more secure if used properly.”), Fig. 1-7 (shown below); Ex. 1002 at ¶301.



Ex. 1018 at Fig. 1-7 (annotated).

The selection of the security algorithm affects the data throughput by varying the processing time required to encrypt/decrypt data, memory device lifetime by varying the level of security to prevent unauthorized access to data, and power optimization by varying the amount of processor operations required to complete the encryption and decryption. Ex. 1002 at ¶302.

3. Dependent Claim 16

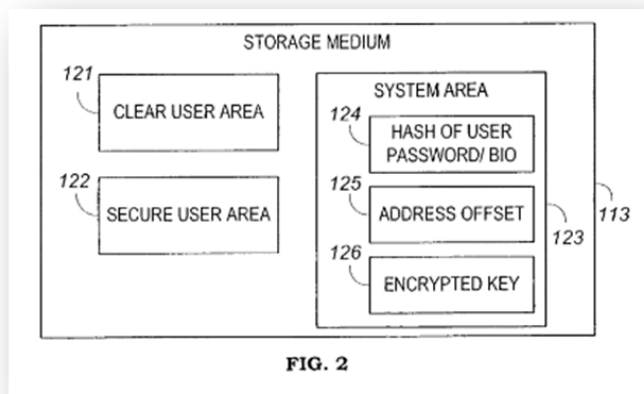
Ziv comprises a default access profile (*i.e.*, access to the clear user area) that is used to set up the memory device upon power up. Ex. 1004 at 6:2-4 (“By default, microprocessor 111 uses an address offset of zero, thus the host sees clear

user area 121[.]”); Ex. 1002 at ¶¶304-305. The access to the clear user area does not require entry of a password. *Id.* at 6:4-7.

4. Independent Claim 17

(i) A memory device, comprising:

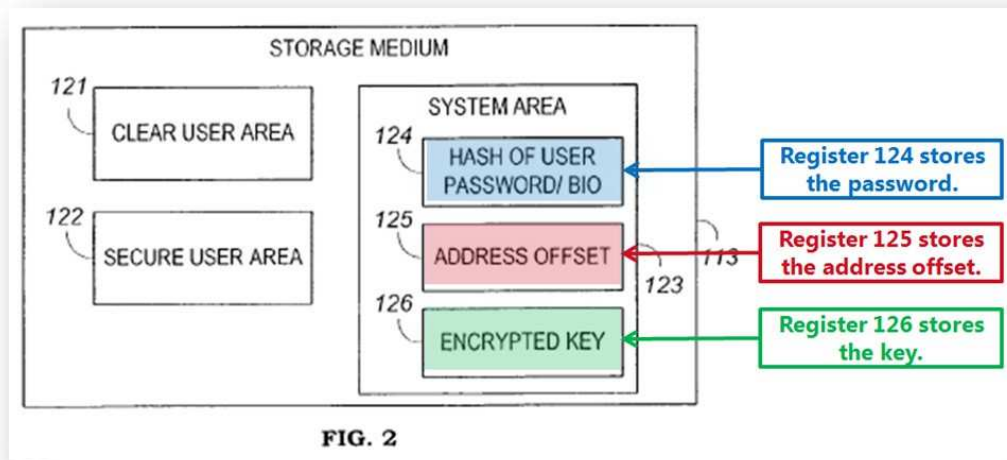
Ziv discloses a memory device, such as a portable storage device that includes storage memory. Ex. 1004 at 3:48-55, Fig. 2.



Id. at Fig. 2.

(ii) one or more registers for storing one or more predefined access profiles associated with said memory device,

Ziv discloses a predefined access profile that contains a password hash, an address offset, and a key, which are predefined. *Id.* at 5:1-25 (describing initial setup); Ex. 1002 at ¶¶307-313. The password hash, address offset, and key are each stored in registers (as illustrated in Fig. 2). Ex. 1004 at 4:16-20, Fig. 2.



Id. at Fig. 2 (annotated).

Ziv discloses storing one or more predefined access profiles associated with said memory devices. *See* Section above at IX.B.1(iii); Ex. 1002 at ¶¶307-313.

- (iv) **said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;**

See Section above at IX.B.1.(iv).

- (v) **a controller for receiving one or more commands related to said at least one usage of said memory device,**

See Section above at IX.B.1.(ii).

- (vi) **said one or more commands for activating said one or more predefined access profiles associated with said memory device,**

See Section above at IX.B.1.(iii).

- (vii) **said controller also for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.**

See Section above at IX.B.1.(v).

5. Dependent Claim 21

See Section above at IX.B.2.(i).

6. Dependent Claim 32

See Section above at IX.B.3.(i).

7. Independent Claim 35

- (i) **A computer program product embodied on a non-transitory computer-readable medium, comprising:**

Ziv discloses “a portable storage device [that] is connected to a computer, the computer takes control over the read/write operation via its operating system.”

As such, to the extent the preamble is limiting, which it is not, *Ziv* discloses a

computer program embodied on a non-transitory computer-readable medium.

Ex. 1002 at ¶322.

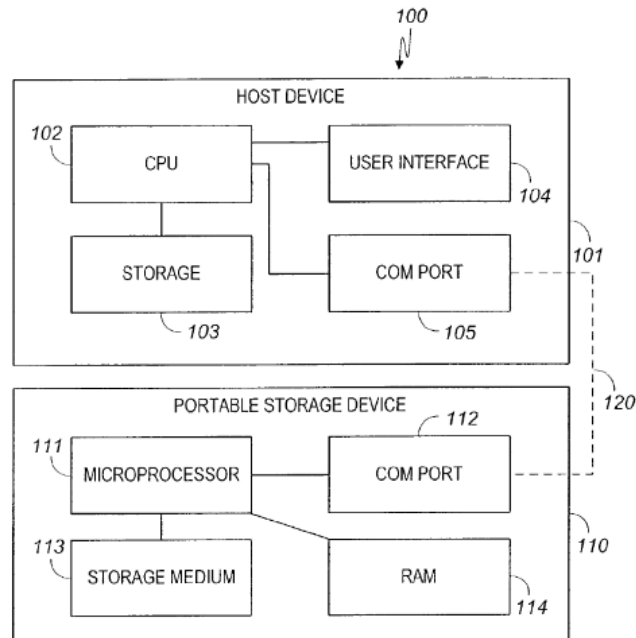


FIG. 1

Ex. 1004 at Fig. 1.

- (ii) a computer code for receiving one or more commands related to at least one usage of a memory device,

See Section above at IX.B.1.(ii).

- (iii) said one or more commands for activating one or more predefined access profiles associated with said memory device,

See Section above at IX.B.1.(iii).

- (iv) said predefined access profiles being effective for determining how access to said memory device is configured for said at least one usage; and

See Section above at IX.B.1.(iv).

- (v) **a computer code for configuring access to said memory device in accordance with at least one of said access profiles so that said memory device is effective for said at least one usage.**

See Section above at IX.B.1.(v).

C. GROUND 3: Claims 2-3, and 18-19 are unpatentable under 35 U.S.C. § 103(a) in view of *Ziv*, *Vogt*, and *Toombs*.

As shown below, *Ziv*, *Vogt*, and *Toombs* render obvious Claims 2-3 and 18-19 of the '180 Patent under 35 U.S.C. § 103. See also Ex. 1002 at ¶¶327-343.

1. Dependent Claim 2

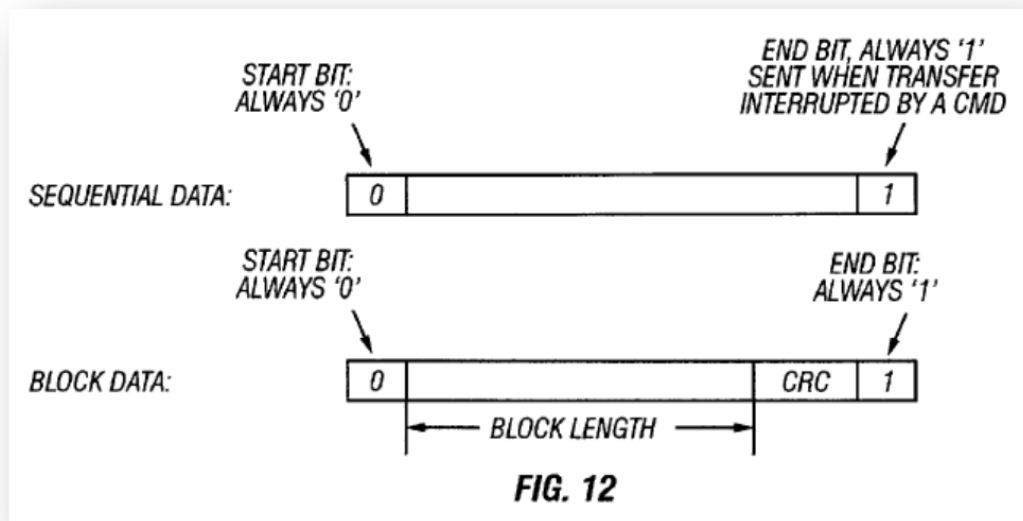
- (i) **The method of claim 1, wherein said one or more access profiles correspond to at least one of a random and a sequential mode of access.**

Independent Claim 1 in view of *Ziv* and *Vogt* is addressed in Ground 2 above at Section IX.B.1.

As disclosed in *Ziv*, the read/write commands to the secure area using the hashed password, address offset, and key (*i.e.*, predefined access profile) correspond to a random or sequential mode of access. Random mode of access and sequential mode of access are the only two types of access methods for reading from and/or writing to memory. Ex. 1002 at ¶334.

Further, *Toombs* teaches these two fundamental types of data transfer: sequential data transfer (sequential mode of access) and block-oriented data transfer (random mode of access). Ex. 1002 at ¶335; Ex. 1006 at 8:34-34 (“[T]wo

types of data transfer commands are defined: Sequential commands, and Block-oriented commands.”). The sequential data transfer commands initiate a “continuous data stream[.]” Ex. 1006 at 8:35-37. A single block-oriented transfer initiates a single block transfer. *Id.* at 22:6-10.



Id. at Fig. 12 (illustrating the difference between sequential data and block data).

A POSITA would understand that the read/write commands associated with the access profile in *Ziv* may also include the sequential read/write commands or single read/write commands disclosed by *Toombs*. Ex. 1002 at ¶¶336-338. It would have been obvious to include the sequential read and write command as taught by *Toombs* in the combined *Ziv-Vogt* memory device:

Explicit Teaching to Combine

As described in *Ziv*, the read and write operations perform under well-established standards. Ex. 1004 at 1:23-25 (“[T]he computer controls all read/write operations under well-established standards.”). Sequential and single block read operations and sequential write operations are basic transfer techniques to perform reading and writing operations. Ex. 1006 at 8:34-34. Accordingly, a POSITA would have looked for a basic transfer technique, like the sequential or single block read and write operations of *Toombs*, to perform the read/write operations of *Ziv*. Moreover, the sequential operations of *Toombs* were known to be advantageous as they reduce addressing overhead and improve efficiency during sequential access. *See id.* at 8:39-43 (“This [sequential data transfer] mode reduces the command overhead to an absolute minimum[.]”); Ex. 1002 at ¶328. Block-oriented commands were also advantageous as they ensured a successful data transfer. Ex. 1006 at 8:44-45.

A POSITA would have further been motivated to look to the teachings of the prior art due to the similar field, technology, and time frame of *Toombs*, *Ziv*, and *Vogt*. Ex. 1002 at ¶329. All three patents center on accessing flash memory. Ex. 1004 at 4:4-9; Ex. 1005 at 2:19-20; Ex. 1006 at 1:30-33; Ex. 1002 at ¶329.

Use of Known Technique to Improve Similar Devices in the Same Way

As described in *Ziv*, “well-established standards” control the read and write operation to the secure memory area. Ex. 1004 at 1:23-25. As taught in *Toombs*, sequential and single-block read/write operations were known standard techniques for reading and writing operations. Ex. 1006 at 8:34-34.

It was within a POSITA’s skill to apply the technique of sequential and single-block read and write commands in *Toombs* with the read and write command in the memory device described in *Ziv*. M.P.E.P. 2143(I)(B); Ex. 1002 at ¶¶330-32. Predictably, the *Ziv-Vogt* memory device would efficiently perform sequential read and write operations or single-block read and write operations to read from or write to the secure memory area. *Id.* at ¶¶330-32.

2. Dependent Claim 3

- (i) **The method of claim 2, wherein said access profiles correspond to at least one of a read, a write, an erase, and a modify attribute operation.**

Independent Claim 1 in view of *Ziv*, and *Vogt* is addressed in Ground 2 above at Section IX.B.1.

The address offset and key in *Ziv* corresponds to at least read and write operations. Ex. 1002 at ¶339. The address offset allows the host to properly read from and write to the secure memory area by pointing the controller to the secure memory area. *See* Ex. 1004 at 6:46-49, Fig. 10 (noting address offset is used in

on-the-fly encryption/decryption). In addition, because the key is required to properly read from and write to the secure memory area, the key also corresponds to reading and writing operations. *Id.* at 7:36-46.

3. Dependent Claim 18

Independent Claim 17 in view of *Ziv* and *Vogt* is addressed in Ground 2 above at Section IX.B.4.

See Section above at IX.C.1.

4. Dependent Claim 19

Independent Claim 17 in view of *Ziv* and *Vogt* is addressed in Ground 2 above at Section IX.B.4.

See Section above at IX.C.2.

D. GROUND 4: Claims 1-3, 5, 16-19, 21, 32, and 35 are unpatentable under 35 U.S.C. § 103(a) in view of *Sinclair* and *Toombs*.

As shown below, *Sinclair* and *Toombs* render obvious Claims 1-3, 5, 16-19, 21, 32, and 35 of the '180 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶344-410.

1. **Independent Claim 1**

(i) **A method for configuring access to a memory device, comprising:**

Sinclair discloses at least a “method for managing space in a non-volatile memory,” which corresponds to configuring access to a memory device, as further shown below. Ex. 1007 at Abstract, Claims 1-14; Ex. 1002 at ¶¶352-353.

(ii) **receiving one or more commands related to at least one usage of said memory device,**

In *Sinclair*, the controller receives commands to select the appropriate reclaim mode. Ex. 1007 at 23:28-30 (“[T]he host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity”); Ex. 1002 at ¶¶354-56. The selection is related to at least one usage (*i.e.*, “expected host activity” including “idle”). Ex. 1007 at 23:27-30, 41-44.

(iii) **said one or more commands for activating one or more predefined access profiles associated with said memory device,**

Sinclair discloses a “Reclaim_normal” mode that is a predefined access profile associated with the memory device and is stored in a portion of the memory (*i.e.*, register). Ex. 1007 at 2:50-57, 10:20-22; Ex. 1002 at ¶¶357-359; *see* Ex. 1001 at 3:56-58 (“***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device.***”) (emphasis supplied). The Reclaim Normal mode is the default mode that governs the access

operations to the memory device. Ex. 1007 at 23:36-24:8. In this mode, the memory device calculates an optimal interleave ratio of reclaim operations to write commands such that a memory card will not run out of writeable memory until there is no reclaimable memory left. *Id.* at 2:50-57, Fig. 19.

Similarly, the host may also issue a “Reclaim_on” command or a “Reclaim_off” command to select other reclaim modes. *Id.* at 23:36-59. The controller performs continuous reclaim operations in Reclaim On mode and, conversely, prohibits reclaim operations in Reclaim Off mode. *Sinclair*, further, contemplates optional Maximum and Minimum Interleave modes that perform reclaim operations at a maximum or minimum interleave rate. *Id.* at 23:64-24:6. The Reclaim On, Maximum Interleave, Reclaim Normal, Minimum Interleave, and Reclaim Off mode each constitutes a predefined access profile. Ex. 1002 at ¶¶354-56. These various reclaim modes are selectable by the host based on the host’s expected activity. Ex. 1007 at 23:25-29

After receiving a reclaim mode command, such as the “Reclaim_normal” command, the controller begins reclaiming memory as specified by the selected profile. Ex. 1007 at 23:27-30. For instance, in Reclaim Normal mode, reclaiming occurs “according to an adaptive schedule.” *Id.* at 24:1-3.

(iv) **said predefined access profiles being effective for determining how access to said memory device is configured for said at least one usage; and**

In *Sinclair*, the host selects a predefined access profile, like Reclaim Normal mode, to optimally interrupt host write operations (*i.e.*, determine how access to the memory device is configured) based on an expected host activity (*i.e.*, usage). *Id.* at 23:28-30; Ex, 1002 at ¶¶360-361.

The selection of Reclaim Normal mode, for example, causes the memory controller to configure the device to optimally interleave memory access operations (*e.g.*, write/read) with reclaim operations. Ex. 1007 at Abstract. (“A memory controller ... schedules the reclaim operations to be evenly distributed between write operations until the memory is full.”).

Reclaim On mode and Reclaim Off mode similarly cause access configuration changes. In Reclaim On mode, the host sits “idle” by not sending additional commands as the memory device performs continuous reclaim operations. *Id.* at 23:38-44. In Reclaim Off mode, the memory device inhibits reclaim operations and only host operations are performed. *Id.* at 23:55-56.

- (v) **configuring access to said memory device in accordance with at least one of said access profiles so that said memory device is effective for said at least one usage.**

In *Sinclair*, the memory controller calculates an optimal interleave ratio of reclaim operations to write operations in Reclaim Normal mode. Ex. 1007 at 2:56-57. Once calculated, the memory controller configures access to the memory device according to the optimal interleave ratio. *Id.* at 18:46-49. The memory device will then interleave memory access operations, like write and reclaim operations. *Id.* at 18:46-49; Ex. 1002 at ¶356. This ensures write operations to the memory device are effective as long as reclaimable memory remains. Ex. 1007 at 18:17-26.

Similarly, the memory controller configures access to the device in Reclaim On mode and Reclaim Off mode. In Reclaim On mode, the host is “idle” while the memory device performs continuous reclaim operations. *Id.* at 23:38-44. In Reclaim Off mode, reclaim operations are inhibited and only host access operations are performed. *Id.* at 23:55-56. *Sinclair* discloses this element. Ex. 1002 at ¶¶362-363.

2. Dependent Claim 2

During the Reclaim Normal mode, reclaim operations are interleaved with write operations. Ex. 1007 at 17:58-60. Moreover, these write operations can either be a sequential or random mode of access. Ex. 1002 at ¶¶364-367.

One method of reclaim operations is data compaction, which rearranges blocks into *a sequential format*. *Id.* at 12:28-30; Ex. 1002 at ¶¶365-66. *Sinclair* teaches the benefit of sequential access: “one advantage of sequentially storing data is that it may not necessary to maintain an index of the locations of different sectors, thus reducing the overhead associated with maintaining such an index.” Ex. 1007 at 12:51-54. Accordingly, the reclaim operation associated with the Reclaim Normal mode corresponds to a sequential mode of access as the controller can now access a sequentially-arranged set of data. Ex. 1002 at ¶¶366-67.

3. Dependent Claim 3

Sinclair teaches that the Reclaim Normal mode corresponds to interleaving reclaim operations *with host data write operations*. Ex. 1007 at 24:1-3 (emphasis supplied).

4. Dependent Claim 5

Reclaim Normal mode is adapted to produce an optimized performance associated with the memory device. Ex. 1002 at ¶¶370-373. First, the reclaim operation in the Reclaim Normal mode “allows programming of host data to

continue at a constant rate until the memory is full.” Ex. 1007 at 22:56-61.

Without a Reclaim Normal mode, data programming is impeded when no writeable memory remains (*Id.* at 17:23-25), whereas Reclaim Normal ensures higher reliability such that the memory device does not utilize all writeable memory prematurely. *Id.* at 22:56-61. This ensures an optimized performance in accordance with at least data throughput. Ex. 1002 at ¶371. *Sinclair* further teaches changing the interleave ratio to optimize the data programming speed if conditions in the memory change. Ex. 1007 at 18:17-26. In addition, the controller in Reclaim Off mode only performs host operations, thereby “provid[ing] maximum host data write performance.” *Id.* at 23:55-58.

Finally, the reclaim modes support “wear leveling” of the device (*id.* at 16:5-11), which a POSITA would understand improves device lifetime through wear leveling technology. Ex. 1002 at ¶373.

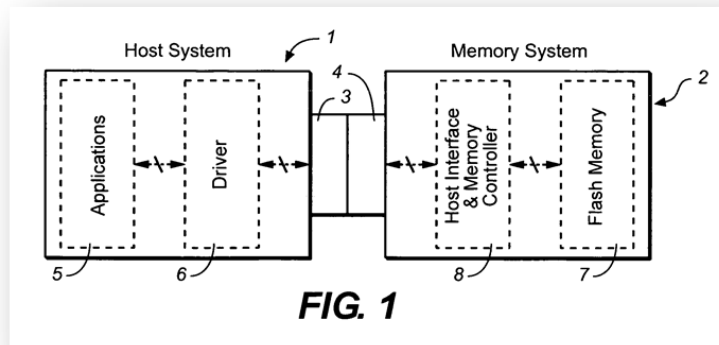
5. Dependent Claim 16

Sinclair discloses a default access profile, like the Reclaim Normal mode, that configures the memory device upon power up. Ex. 1007 at 23:47-48; Ex. 1002 at ¶375.

6. **Independent Claim 17**

(i) **A memory device, comprising:**

Sinclair discloses “the operation of re-programmable non-volatile memory systems such as semiconductor flash memory[.]” Ex. 1007 at 1:17-19, Fig. 1.



Id. at Fig. 1.

(ii) **one or more registers for storing one or more predefined access profiles associated with said memory device,**

One or More Registers

Sinclair discloses that exemplary flash memory systems that perform the reclaim operation modes are CompactFlash and MultiMediaCard memories. *Id.* at 1:17-20, 4:28-32. Each of these standardized memory technologies includes a register that stores internal information (*e.g.*, available commands/features). Ex. 1002 at ¶¶385-386. A POSITA would understand that the register in a flash memory system (like CompactFlash or MultiMediaCard) would store the available reclaim modes. *Id.* at ¶¶383-86. Moreover, when the host selects a reclaim mode,

that selection would be stored in a portion of the flash memory system (*i.e.*, a register). *Id.* at ¶387.

Sinclair further discloses that a reserved portion of the memory capable of storing operating firmware and data (like supported reclaim modes) (*i.e.*, a register) is used by the memory controller. Ex. 1007 at 10:20-22 (“[A]t least one metablock 167 is usually allocated as a reserved block for storing operating firmware and data used by the memory controller.”); Ex. 1002 at ¶386. The available reclaim modes are part of the “operating firmware and data used by the memory controller,” because they control the reclaim activity of the memory. Ex. 1007 at 10:20-22; Ex. 1002 at ¶386. *Sinclair* thus discloses a portion of the memory capable of storing information regarding the various supported reclaim modes. Ex. 1007 at 10:20-22.

To the extent that a register for storing access profiles is not inherently disclosed in *Sinclair*, it would have been obvious to store the selectable reclaim modes described by *Sinclair* in a memory register as described by *Toombs*. Ex. 1002 at ¶387.

Toombs discloses registers for a MultiMediaCard that store “a variety of status and internal information” available to a host. Ex. 1006 at 9:46-48. Since a host must select an appropriate reclaim mode, a POSITA would recognize the

benefits of using the register in *Toombs* to store the host-selectable reclaim modes in *Sinclair* for the host to select. Ex. 1002 at ¶388. The memory device should inform the host of the supported reclaim modes in order for the host to make an informed selection of an available reclaim mode. *Id.* at ¶389.

Moreover, it would be obvious to use a register to store the host-selected reclaim mode (*i.e.*, profile) as such registers were taught in *Toombs* as a desirable and efficient way of communicating card configuration information to the host. Ex. 1002 at ¶389.

Analogous Art

Toombs and *Sinclair* are in a similar field, technology, and time frame. Ex. 1002 at ¶¶345-46. Both *Toombs* and *Sinclair* expressly teach an exemplary embodiment using MMC. Ex. 1007 at 4:28-31; Ex. 1006 at 2:9-11; Ex. 1002 at ¶345. Moreover, a POSITA would have especially been motivated to consider *Sinclair* and *Toombs* together because these two references are both assigned to SanDisk. Ex. 1020; Ex. 1021; Ex. 1002 at ¶346.

Combining Prior Art Elements According to Known Methods to Yield Predictable Results

Registers storing card-supported operational modes were well-known in the art. Ex. 1006 at 9:46-48. A POSITA could have combined one prior art element (a register for storing card-supported modes) with another prior art element (memory

devices supporting certain reclaim modes) according to a known method (combining known functionalities from two different devices into a single device) and the results would have been predictable (storing the supported reclaim modes in a register). M.P.E.P. 2143(I)(B); Ex. 1002 at ¶348. Moreover, those predictable results would have included the known advantages of *Sinclair*'s memory device, which performs reclaim operations at a frequency defined by the host-selected reclaim mode. Ex. 1007 at 23:64-24:6, 2:50-57; Ex. 1002 at ¶349.

Known Technique to a Known Device to Yield Predictable Results

Base system: *Sinclair* discloses a memory device that provides host-selectable reclaim modes. Ex. 1007 at 2:50-57 (disclosing “[a] hierarchy of possible reclaim modes” as selectable modes); Ex. 1002 at ¶382.

Known technique: As shown by *Toombs*, storing card-supported modes of operation in a register was well-known. Ex. 1006 at 9:46-48 (“[E]ach of the cards of the system comprises a group of registers for storing a variety of status and internal information”); Ex. 1002 at ¶349. For example, the Card-Specific Data (CSD) register in *Toombs* stores the supported card command classes for a MMC card. Ex. 1006 at 10:65-67.

Predictable results and improved system: A POSITA would have been motivated to store the supported reclaim modes on a register to take advantage of

known register-based approach for communicating available options to a host and receiving selections from the host in order to implement *Sinclair*'s system of allowing the host to select from available reclaim modes. Ex. 1002 at ¶350. A register storing available reclaim modes would have been an obvious and desirable design choice. Ex. 1002 at ¶351.

Sinclair discloses storing one or more predefined access profiles associated with said memory devices. *See* Section above at IX.D.1(iii).

- (iii) **said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;**

See Section above at IX.D.1(iv).

- (iv) **a controller for receiving one or more commands related to said at least one usage of said memory device,**

See Section above at IX.D.1(ii).

- (v) **said one or more commands for activating said one or more predefined access profiles associated with said memory device,**

See Section above at IX.D.1(iii).

- (vi) **said controller also for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.**

See Section above at IX.D.1(v).

7. **Dependent Claim 18**

See Section above at IX.D.2.

8. **Dependent Claim 19**

See Section above at IX.D.3.

9. **Dependent Claim 21**

See Section above at IX.D.4.

10. **Dependent Claim 32**

See Section above at IX.D.5.

11. **Independent Claim 35**

- (i) **A computer program product embodied on a non-transitory computer-readable medium, comprising:**

Sinclair discloses an “operation of re-programmable non-volatile memory systems ... to the management of available space within such memories.”

Ex. 1007 at 1:17-23.

- (ii) **a computer code for receiving one or more commands related to at least one usage of a memory device,**

See Section above at IX.D.1.(ii).

- (iii) **said one or more commands for activating one or more predefined access profiles associated with said memory device,**

See Section above at IX.D.1.(iii).

- (iv) said predefined access profiles being effective for determining how access to said memory device is configured for said at least one usage; and

See Section above at IX.D.1.(iv).

- (v) a computer code for configuring access to said memory device in accordance with at least one of said access profiles so that said memory device is effective for said at least one usage.

See Section above at IX.D.1.(v).

E. GROUND 5: Claims 12, 13, 28, 29 are unpatentable under 35 U.S.C. § 103 in view of *CompactFlash* and *Elhamias*

As shown below, *CompactFlash* and *Elhamias* render obvious Claims 12, 13, 28 and 29 of the '180 Patent under 35 U.S.C. § 103. See also Ex. 1002 at ¶¶411-425.

1. Dependent Claim 12

- (i) The method of claim 1, wherein said configuring is adapted in parallel for two or more access profiles.

Independent Claim 1 in view of *CompactFlash* is addressed in Ground 1 above under Section IX.A.1. Non-volatile memory cards are disclosed in *Elhamias*. Ex. 1002 at ¶412; Ex. 1008 at ¶7.

Additionally, *Elhamias* discloses that a memory device may include predetermined access profiles that are activated in parallel. For example, *Elhamias* discloses that the disclosed storage device can utilize “memorize access sequences issued by the host under various predefined conditions, such as host reset or power

on boot sequence. As the sequence of host commands following these predefined conditions are usually the same, the storage device can use this information to optimize operation for the expected commands.” Ex. 1008 at ¶10. *Elhamias* further discloses that the “SD card 35 contains nine surface electrical contacts 10-18...Contact 12 receives commands (CMD) from the host and sends responses and status signals back to the host. The remaining contacts 10, 11, 17 and 18 (DAT 2, DAT 3, DAT 0, and DAT 1, respectively) receive data in parallel for storage in its non-volatile memory and send data to the host in parallel from the memory. Ex. 1008 at ¶22. Thus, in combination with *CompactFlash*, *Elhamias* discloses that a memory device may include predetermined access profiles (from *CompactFlash*) that are activated in parallel (as parallel commands and data transmissions are disclosed in *Elhamias*). Ex. 1002 at ¶¶417-19.

A POSITA would combine the memory device from *CompactFlash*, where the memory device receives commands from one or more predefined access profiles, with a memory card capable of conducting two or more memory access operations in parallel, as in *Elhamias*. Ex. 1002 at ¶¶411-416. Indeed, the memory device in *Elhamias* is a desirable type of storage medium that a POSITA would implement in the memory device of *CompactFlash* as an obvious design choice. Ex. 1002 at ¶419. For example, *Elhamias* specifically suggests that *Elhamias* is

“removable non-volatile memory cards [that] include a memory array and a controller that performs as the memory control and the host interface function.

These removable cards are plugged into a different of variety of devices[.]”

Ex. 1008 at ¶7.

Further, *CompactFlash* and *Elhamias* are in a similar field, technology, and time frame. Ex. 1002 at ¶¶411-413.

Moreover, a POSITA would have especially been motivated to combine *CompactFlash* and *Elhamias*, as there are express motivations in the art for this combination, because *Elhamias* improves the efficiency of data transfer, and *CompactFlash* specifically introduced Ultra DMA modes to improve the efficiency of *CompactFlash* memory devices. Ex. 1002 at ¶414. Similarly, a POSITA would have recognized that *Elhamias* also provides greater control for the *CompactFlash* host to order its operations. *Id.* at ¶415. Using the advantages of *CompactFlash* of performing read and write operations under a well-established standard, a POSITA would have been motivated by the teachings of *Elhamias* to use host prioritization of data to gain the advantage of meeting read and write operations in *CompactFlash*. *Id.*

2. Dependent Claim 13

- (i) **The method of claim 12, wherein said configuring is carried out in accordance with Joint Electron Devices Engineering Council Standard (JESD84) standard for embedded Multimedia Card (eMMC).**

Independent Claim 1 in view of *CompactFlash* and the method of claim 12 is addressed in Ground 1 above at Section IX.A.1 and in Ground 5 above at Section IX.E.1, respectively.

Elhamias discloses that “[t]he MMC card has the same dimensions and operates similarly to the SD card ... [t]he contacts of the card are connected through respective pins of the socket to its host system.” Ex. 1008 at ¶22.

These exemplary embodiments are in accordance with the Joint Electron Devices Engineering Council Standard (JESD84) standard for embedded Multimedia Card (eMMC). Ex. 1002 at ¶421.

3. Dependent Claim 28

Independent Claim 17 in view of *CompactFlash* is addressed in Ground 1 above at Section IX.A.6.

See Section above at Section IX.E.1.(i).

4. Dependent Claim 29

Independent Claim 17 in view of *CompactFlash* and the memory device of Claim 28 is addressed in Ground 1 above at Section IX.A.6 and in Ground 5 above at Section IX.E.3, respectively.

See Section above at Section IX.E.2.(i).

F. GROUND 6: Claims 12, 13, 28, 29 are unpatentable under 35 U.S.C. § 103 in view of *Ziv*, *Vogt*, and *Elhamias*

As shown below, *Ziv*, *Vogt*, and *Elhamias* render obvious Claims 12, 13, 28 and 29 of the '180 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶426-444.

1. Dependent Claim 12

Independent Claim 1 in view of *Ziv* and *Vogt* is addressed in Ground 2 above at Section IX.B.1.

Additionally, *Vogt* discloses embedding the flash memory within a device (e.g., cell phone). *See* Ex. 1005 at 2:32-42. The “flash memory is *embedded* in the device, and cannot be easily reset or replaced.” *Id.* at 11:16-19 (emphasis added).

Elhamias discloses configuring in parallel, such that this combination discloses Claim 12, as explained above in Section IX.E.1.(i).

The reasons to combine *Ziv* with *Vogt* are addressed above in Section IX.C.1.(i). A POSITA would have further combined the flash memory device in *Vogt* and/or *Elhamias* with the storage medium described in *Ziv* and would see benefits in doing so. Ex. 1002 at ¶¶427-31. The flash memory device in *Elhamias* and *Vogt* is a desirable type of storage medium that a POSITA would implement in the memory device in *Ziv* as an obvious design choice. Ex. 1002 at ¶¶427-31. For instance, *Elhamias* discloses that a memory device may include predetermined

access profiles that are activated in parallel, as discussed above. For example, *Elhamias* discloses that its storage device can utilize “memorize access sequences issued by the host under various predefined conditions, such as host reset or power on boot sequence. As the sequence of host commands following these predefined conditions are usually the same, the storage device can use this information to optimize operation for the expected commands.” Ex. 1008 at ¶10. *Elhamias* further discloses that the “SD card 35 contains nine surface electrical contacts 10-18...Contact 12 receives commands (CMD) from the host and sends responses and status signals back to the host. The remaining contacts 10, 11, 17 and 18 (DAT 2, DAT 3, DAT 0, and DAT 1, respectively) receive data in parallel for storage in its non-volatile memory and send data to the host in parallel from the memory.” Ex. 1008 at ¶22.

Similarly, *Vogt* discloses the “benefit from inclusion of security primitives in flash memory,” further confirming the desirability of combining *Vogt* with systems, such as *Ziv*, that involve secure access to data in a memory device. Ex. 1005 at 2:32-35.

Lastly, a POSITA would have combined *Ziv*, *Vogt*, and *Elhamias* for similar reasons as with the *CompactFlash-Elhamias* combination discussed in Ground 5—they are in similar fields and timeframes, a POSITA would have recognized the

express motivations to combine these references for efficiency and control gains, and the combination brings together known techniques to yield predictable results.

Ex. 1002 at ¶¶426-433.

2. Dependent Claim 13

Independent Claim 1 in view of *Ziv* and *Vogt* is addressed in Ground 2 above at Section IX.B.1.

See Section IX.E.2.(i).

3. Dependent Claim 28

Independent Claim 17 in view of *Ziv* and *Vogt* is addressed in Ground 2 above at Section IX.B.1.

See Section above at Section IX.F.1.(i).

4. Dependent Claim 29

Independent Claim 17 in view of *Ziv* and *Vogt* is addressed in Ground 2 above at Section IX.B.1.

See Section above at Section IX.F.2.(i).

X. CONCLUSION

Kingston respectfully requests that *inter partes* review of the '180 Patent be instituted and that Claims 1-3, 5, 12-13, 16-19, 21, 28, 29, 32, and 35 be cancelled as unpatentable under 35 U.S.C. § 318(b).

Dated: January 30, 2019

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 13,982 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the “Word Count” feature of Microsoft Word 2016, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word 2016 in Times New Roman 14-point font.

Dated: January 30, 2019

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true copy of the foregoing
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,307,180
and supporting materials (Exhibits 1001 - 1025 and Power of Attorney) have been
served in its entirety this 30th of January, 2019, by e-mail and Federal Express on
Patent Owner at the correspondence address for the attorney of record for the
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