UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

PTAB Case No.: To Be Assigned
U.S. Patent No. 6,127,875
Title: COMPLIMENTARY DOUBLE PUMPING VOLTAGE BOOST CONVERTER

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,127,875 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-.80, 42.100-.123

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Patent Trial and Appeal Board
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TABLE OF CONTENTS

Page

Exhibit List

Micron Exhibit #	Description
Ex. 1001	U.S. Patent No. 6,127,875 ("875 Patent")
Ex. 1002	File History for U.S. Patent No. 6,127,875 ("875 Patent FH")
Ex. 1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
Ex. 1004	*Curriculum Vitae* of Dr. R. Jacob Baker
Ex. 1005	U.S. Patent No. 5,801,997 ("Hsieh")
Ex. 1006	*Exhibit number not used*
Ex. 1007[1]	Baker, R. Jacob et al., *CMOS Circuit Design, Layout, and Simulation*, IEEE Press, 1998 ("Baker")
Ex. 1008	*Exhibit number not used*
Ex. 1009	U.S. Patent No. 4,229,667 ("Heimbigner")
Ex. 1010	IEEE Standard Dictionary of Electrical and Electronics Terms, ANSI/IEEE Std 100-1988 (4th ed. 1988) ("IEEE Standard Dictionary")
Ex. 1011	Chambers Dictionary of Science and Technology, Vol. 1, A-K (1974) ("Chambers Dictionary")
Ex. 1012	Mano, M. Morris, *Digital Logic and Computer Design*, Prentice-Hall, Inc., 1979 ("Mano")
Ex. 1013	Kang, Sung-Mo and Leblebici, Yusuf, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw-Hill Companies, Inc., 1996 ("Kang")

[1] *See* Ex. 1016 for further publication information.

Micron Exhibit #	**Description**
Ex. 1014	Modern Dictionary of Electronics, Revised and Updated (6th ed. 1997) ("Modern Dictionary of Electronics")
Ex. 1015	*Exhibit number not used*
Ex. 1016	Declaration of James L. Mullins regarding R. J. Baker et al., *CMOS Circuit Design, Layout, and Simulations* ("Mullins Decl.")
Ex. 1017	*Exhibit number not used*
Ex. 1018	*Exhibit number not used*

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123, Micron Technology, Inc. ("Petitioner" or "Micron") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-3 of U.S. Patent No. 6,127,875, titled "Complimentary Double Pumping Voltage Boost Converter" (Ex. 1001, the "875 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 875 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 875 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang Registration No. 73,604 (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Jared Bobrow (jared.bobrow@weil.com) *Pro Hac Vice Application To Be Submitted* Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3034; F: 650-802-3100

Petitioner consents to service by electronic mail at the following addresses:

jason.lang@weil.com,
jared.bobrow@weil.com, and
Micron.Northstar.IPR@weil.com.

Pursuant to 37 C.F.R. § 42.10(b), Petitioner's Power of Attorney is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

North Star Innovations, Inc. ("Patent Owner" or "North Star") has asserted the 875 Patent and U.S. Patent Nos. 5,943,274 (the "274 Patent"), 7,171,526 (the "526 Patent"), and 6,465,743 (the "743 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *North Star Innovations, Inc. v. Micron Technology, Inc.*, 17-cv-506-LPS-CJB (D. Del.) ("Co-Pending Litigation"). North Star also has asserted the 875 Patent, the 274 Patent, U.S. Patent Nos. 6,917,555 (the "555 Patent"), and U.S. Patent No. 6,101,145 (the "145 Patent") in the following action: *North Star Innovations, Inc. v. Kingston Technology Co., Inc.*, 8:17-cv-1833 (C.D. Cal.) (complaint filed on October 20, 2017).

In addition to this Petition, Petitioner is filing an additional petition for *inter partes* review of the 875 Patent, one petition for *inter partes* review of the 274 Patent, two petitions for *inter partes* review of the 526 Patent, and one petition for *inter partes* review of the 743 Patent.[2]

The 875 Patent does not claim priority to any foreign or U.S. patent application.

2.5. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 601788.

2.6. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence address of record for the 875 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

Ground #1: Claims 1-3 of the 875 Patent are invalid under (pre-AIA) 35 U.S.C. § 102(e) on the ground that they are anticipated by U.S. Patent No. 5,801,997 to Hsieh et al., entitled "Ping-Pong Boost Circuit," filed on June 24, 1997 and issued on September 1, 1998 (Ex. 1005, "Hsieh").

[2] These petitions will be filed before May 3, 2018.

The Hsieh reference was not cited or considered by the Patent Office during prosecution of the 875 Patent.

This ground is explained below and is supported by the Declaration of Dr. R. Jacob Baker (Ex. 1003, "Baker Decl.").

Statement of Non-Redundancy: Ground #1 in this Petition (Petition 1) is not redundant of Grounds #1-3 in the other petition for *inter partes* review of the 875 Patent (Petition 2) that Petitioner is filing contemporaneously herewith. Ground #1 in Petition 1 is based on Hsieh, which is prior art under § 102(e), while the Grounds in Petition 2 are based on Foss, which is prior art under § 102(b). Thus, to the extent that Patent Owner may seek to rely upon an earlier conception and reduction to practice, Hsieh is not cumulative of Foss. Moreover, Hsieh, unlike Foss, has independent boost and phase signals, which completely removes the issue of whether these signals must be independent (claim elements 1.1-1.2 recite "phase signals," and claim elements 1.3-1.4 separately recite "a boost signal," creating the issue whether these must be independent and completely different signals). Also, Ground #1 in Petition 1 is not redundant of Grounds #2 and #3 in Petition 2 because it discloses a different implementation of a non-inverting buffer. Specifically, Foss in view of Baker or Rabii discloses a cascade of two inverters as a non-inverting buffer, while Hsieh discloses a circuit including an inverter and a NOR gate that is a non-inverting buffer when enabled.

4. BACKGROUND OF TECHNOLOGY

4.1. Voltage Boosting Circuits

The evolution of integrated circuit technology has resulted in smaller devices that operate with lower supply voltages and lower power consumption. Ex. 1003, ¶33. A lower supply voltage, however, usually is unable to support complex functions such as, for example, integrated input/output circuits that practice industry standards (*e.g.*, PCIe (Peripheral Component Interconnect express) or USB (Universal Serial Bus) protocols). *Id*. To facilitate these functions, a voltage boosting circuit[3] has long been used to generate an output voltage greater than the input supply voltage. *Id.*, ¶35.

The 875 Patent does not claim to have invented voltage boosting circuits, nor could it. Ex. 1003, ¶36. Voltage boosting circuits have been known for decades before the filing of the 875 Patent. *Id.*, ¶35 (citing Ex. 1009, Abstract, 1:54-2:10 and Ex. 1007, pp. 84-88 to illustrate the well-known nature of such voltage boosting circuits). Indeed, the 875 Patent describes as admitted prior art a

[3] A voltage boosting circuit is often referred to as a "voltage boosting converter," "voltage boost circuit," "boost circuit," "voltage pump," "charge pump," "booster drive," etc. We use these terms interchangeably throughout this Petition. Ex. 1003, ¶34.

basic voltage boosting circuit 10, which is depicted in FIGS. 1, 2, and 2A reproduced below.

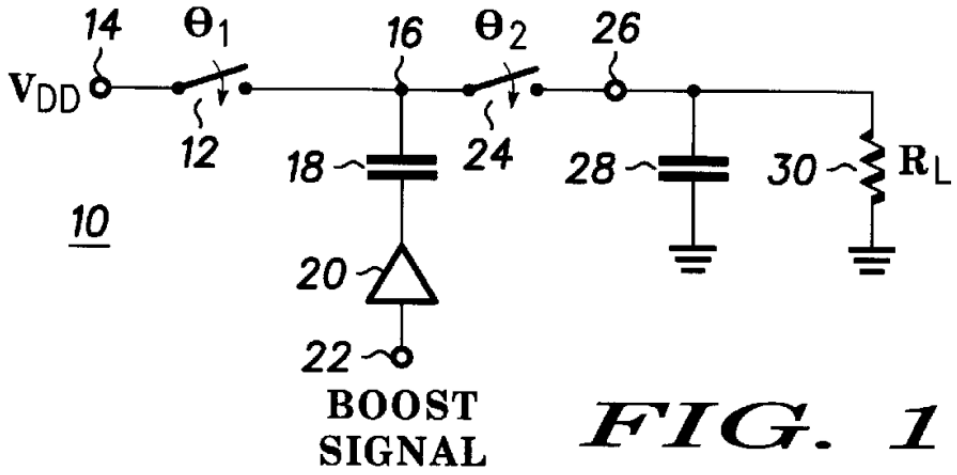


FIG. 1

- PRIOR ART -

Ex. 1001, FIG. 1

As shown in FIG. 1, an input voltage V_{DD} is supplied at terminal 14 and an output voltage is provided at terminal 26. Capacitor 18 is used to boost the output voltage, and capacitor 28 is used to store charge and to regulate the output voltage. A boost signal is provided to a terminal of capacitor 18 via buffer 20. The boost signal is used to generate a boost voltage for the voltage boosting circuit by charging capacitor 18. Ex. 1001, 1:23-43, FIG. 1. Furthermore, two switches 12 and 24 operate (*i.e.*, are turned on and off) in response to a pair of clock signals C1 and C2, which are opposite to each other and change periodically in clock cycles as shown in FIGS. 2A and 2 below. *Id.*, 1:23-50, FIGS. 2A and 2. Ex. 1003, ¶¶36-38.

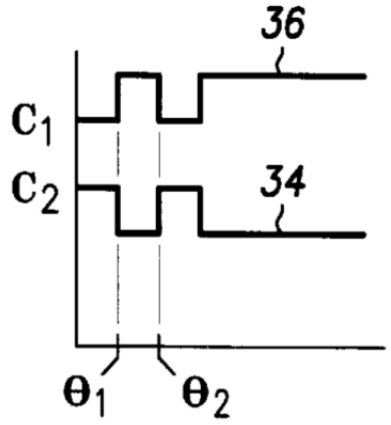


FIG. 2A

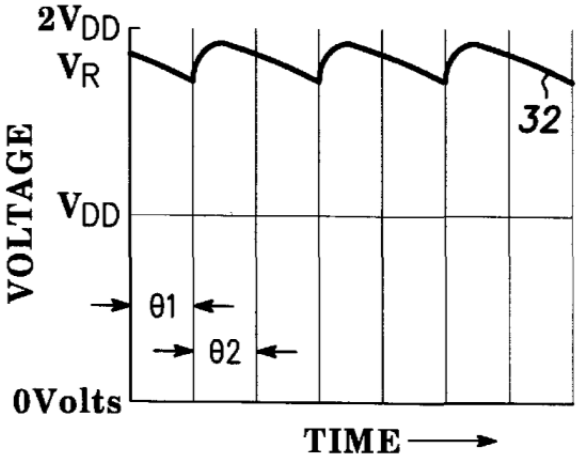


FIG. 2

Ex. 1001, FIG. 2A **Ex. 1001, FIG. 2**

This prior art voltage boosting circuit operates as follows. During the first half of a clock cycle (identified as θ_1 in FIGS. 2A and 2 above), switch 12 is closed, switch 24 is open, and the boost signal is at the ground level. As a result, the top terminal of capacitor 18 is connected to the supply voltage V_{DD}, and the output of buffer 20 is in a low voltage level state (*i.e.*, a potential at ground level), causing the bottom terminal of capacitor 18 to be at ground level. Thus, capacitor 18 is charged to the voltage V_{DD}. During the second half of the clock cycle (identified as θ_2 in FIGS. 2A and 2 above), switch 12 is open, switch 24 is closed, and the boost signal is increased to the supply voltage V_{DD}. As a result, the output of buffer 20 is in a high voltage level state (*i.e.*, a potential of V_{DD}), which causes the bottom terminal of capacitor 18 to have the potential of V_{DD}. Because capacitor 18 has been previously charged to the voltage V_{DD} in the first half of the

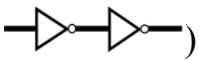
clock cycle, the potential at the top of capacitor 18 is then boosted to substantially $2V_{DD}$. Subsequently, capacitor 18 discharges to capacitor 28 and the load R_L to provide the output voltage. Consequently, the output voltage of the circuit is first boosted to substantially $2V_{DD}$ and then decays as current is delivered to the load R_L. In the first half of the next clock cycle, capacitor 18 is charged back to V_{DD} again, and the output voltage continues to decay as current is continuously delivered to the load R_L. Ex. 1001, 1:23-50, FIG. 1. Ex. 1003, ¶¶39-40.

The manner in which the output voltage (identified as V_R) changes over time is illustrated in FIG. 2, shown above. During each full clock cycle, the resulting output voltage is boosted only once (*i.e.*, at the beginning of the second half of the clock cycle, θ_2), and decays in the remaining time period, which is a large portion of the clock cycle. Ex. 1001, 1:43-52, FIG. 2; Ex. 1003, ¶41.

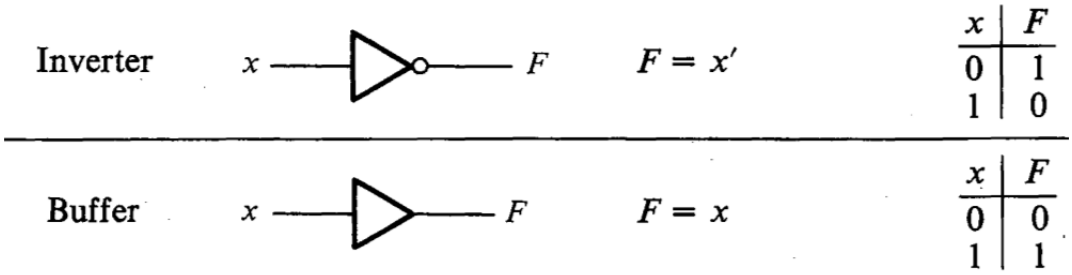
4.2. Buffer

In the context of integrated circuits, a buffer refers to an isolating circuit coupled between a driving circuit and a driven circuit that is used to prevent the driven circuit from influencing the driving circuit. Ex. 1010, pp. 6-7. In other words, a buffer decouples its output from its input, thus avoiding reaction between a driving and a driven circuit. Ex. 1011, p. 4. Ex. 1003, ¶42.

A buffer can be, for example, an inverting buffer or a non-inverting buffer. Ex. 1003, ¶¶43-44. A non-inverting buffer is often referred to simply as a buffer.

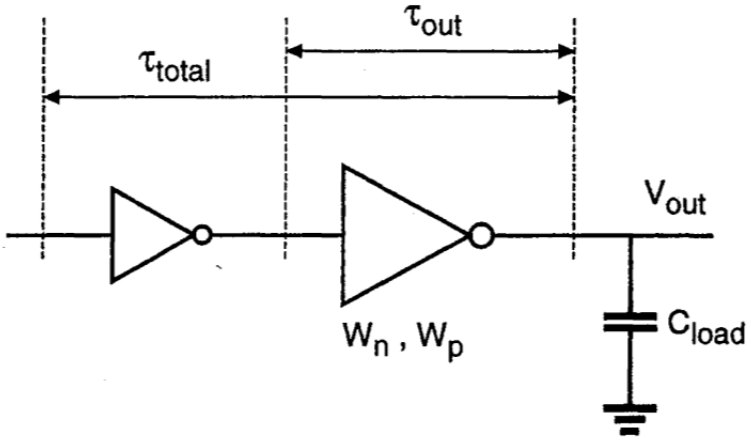
It was well known in the art to represent an inverting buffer using, for example, the schematic symbol of a NOT Gate (*i.e.*, ) and to represent a non-inverting buffer using, for example, the schematic symbol of a Buffer Gate (*i.e.*, ). *Id.* It was also well known in the art to implement a non-inverting buffer by sequentially connecting two inverting buffers into a cascade. Thus, a non-inverting buffer can also be represented by a cascade of two schematic symbols of a NOT Gate (*i.e.*, ). *Id.*, ¶45.

For example, Mano shows using the schematic symbol of a NOT Gate (*i.e.*, ) to represent an inverter (*i.e.*, inverting buffer), and using the schematic symbol of a Buffer Gate (*i.e.*, ) to represent a buffer (*i.e.*, non-inverting buffer). Ex. 1003, ¶46 (citing Ex. 1012, p. 9).



Ex. 1012, p. 9

For another example, Kang shows using a cascade of two inverters to implement a two-stage CMOS buffer (*i.e.*, non-inverting buffer). Ex. 1003, ¶47 (citing Ex. 1013, pp. 11-12).



Ex. 1013, p. 12

Moreover, a buffer can be a tri-state buffer with an enabling signal (or enable input). Such a tri-state buffer behaves as a certain type of buffer (*e.g.*, an inverting buffer or a non-inverting buffer) only when it is enabled (*i.e.*, when the enabling signal is a desired value, *e.g.*, high or low). When the tri-state buffer is not enabled (*i.e.*, when the enabling signal is not the desired value), the output of the tri-state buffer is not affected by its input. Ex. 1003, ¶48 (citing Ex. 1007, pp. 71-72).

For example, Baker describes a tri-state non-inverting buffer (simplified as "tri-state buffer" in Figure 12.23) and a tri-state inverting buffer, shown in the below figures. Ex. 1003, ¶49 (citing Ex. 1007, pp. 71-72).

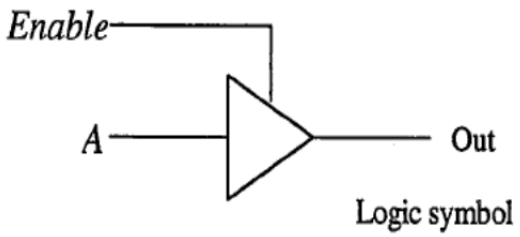


Figure 12.23 Tri-state buffer.

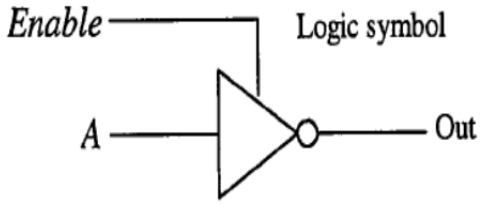


Figure 12.24 Tri-state inverting buffer.

Ex. 1007, pp. 71-72

The terms "inverting buffer" and "non-inverting buffer" are construed in Section 7.2.1 below.

5. OVERVIEW OF THE 875 PATENT[4]

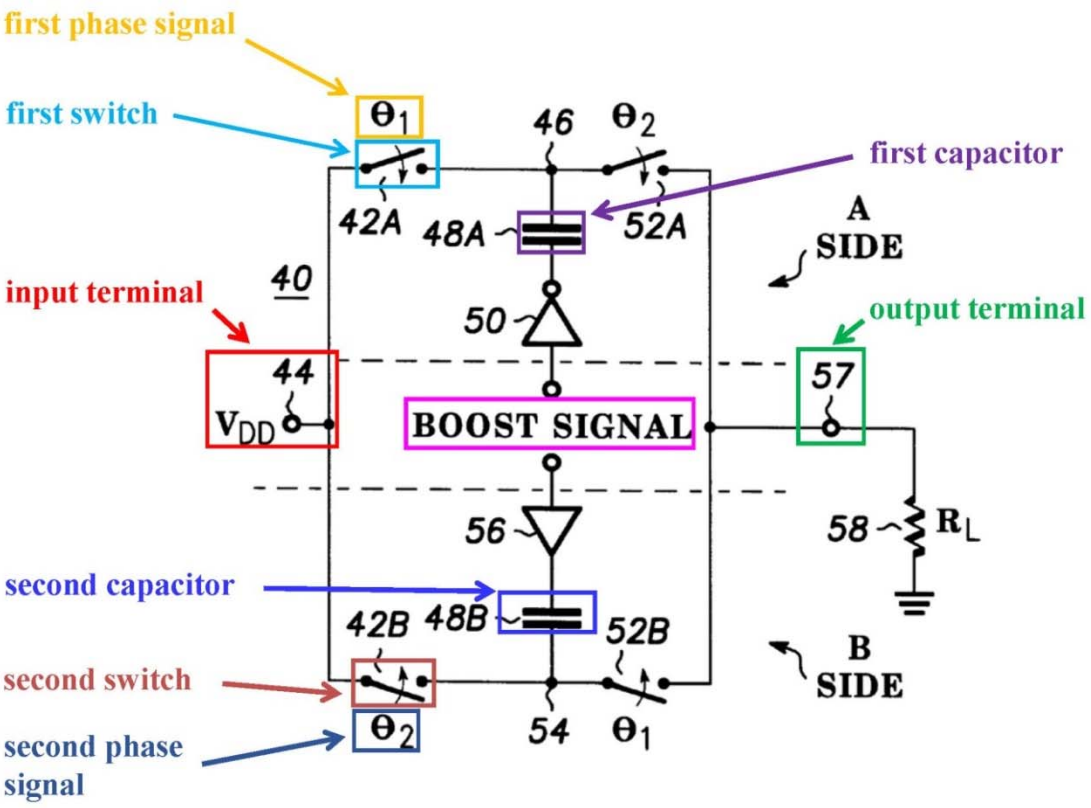
The 875 Patent relates generally to voltage boosting circuits that are suited to be manufactured in integrated circuit form. Ex. 1001, 1:5-9. The 875 Patent alleges that the prior art voltage boosting circuit shown in its FIG. 1 (reproduced and described above in Section 4.1) causes a significant amount of distortion to the output voltage. *Id.*, 1:51-52. To address this issue, the 875 Patent teaches a complementary double pumping voltage boost circuit that purportedly achieves less output voltage distortion than the prior art voltage boosting circuit described above. *Id.*, 2:66-3:3. In simple terms, the 875 Patent alleges that its voltage boosting circuit produces more of a static, level output than in the prior art. The

[4] The 875 Patent was filed on August 13, 1998 and issued on October 3, 2000.

875 Patent alleges that the claimed boost circuit reduces the output voltage distortion because the circuit allegedly boosts the output voltage in both halves of a clock cycle, thus pumping the voltage twice as frequently as the prior art circuits and roughly halving the discharge time. *Id.*, 2:66-3:3. Ex. 1003, ¶52. Note that the claims of the 875 Patent do not require achieving less output voltage distortion or pumping the voltage at any specific frequency. Ex. 1001, 5:9-6:17. Ex. 1003, ¶53.

As illustrated below, the components and architecture of this voltage boost circuit are set forth in claims 1-3 of the 875 Patent and shown in FIG. 3 (reproduced below with colored annotations identifying the corresponding components).

> 1. A boost circuit having an input terminal and an output terminal, comprising:
> a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;
>
> a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;
>
> a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and
>
> a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.
>
> (Ex. 1001, 5:9-6:3.)



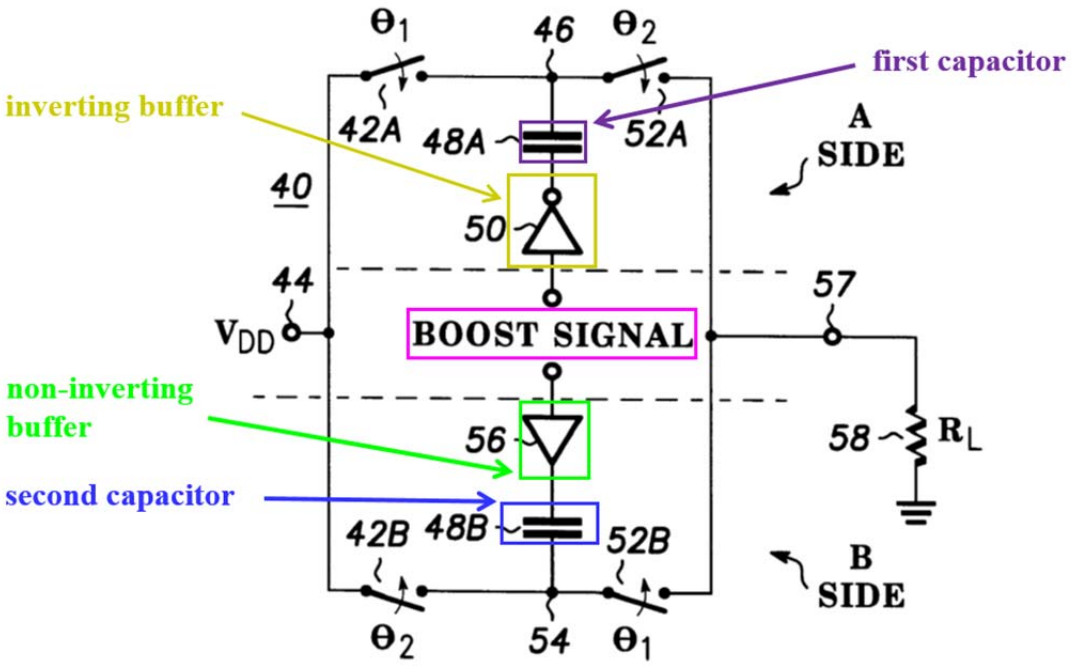
Ex. 1001, FIG. 3 (with annotations)

2. The boost circuit of claim 1, further including:

an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and

a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor.

(Ex. 1001, 6:4-10.)



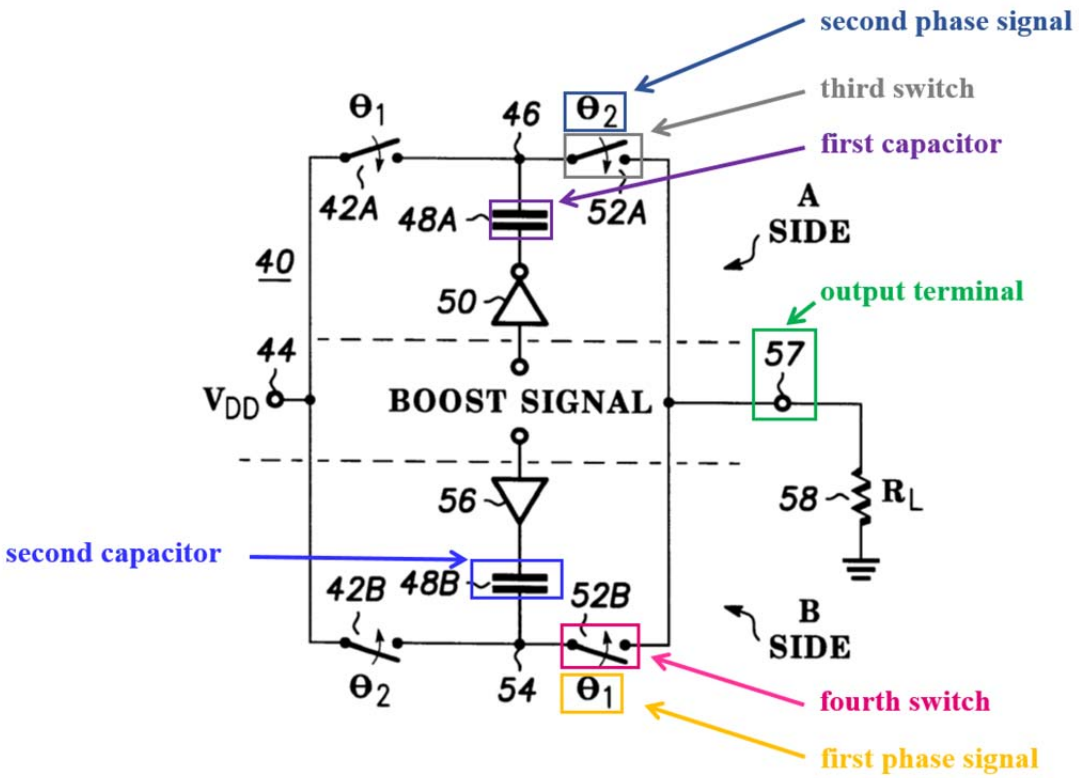
Ex. 1001, FIG. 3 (with annotations)

3. The boost circuit of claim 1, further including:

a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and

a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal.

(Ex. 1001, 6:11-17.)



Ex. 1001, FIG. 3 (with annotations)

As shown in FIG. 3, the voltage boost circuit includes two symmetric portions, an A side portion and a complementary B side portion. Each of these two portions is similar to the prior art voltage boosting circuit described above. Ex. 1001, 2:18-23. Ex. 1003, ¶55.

In operation, during the first half of a clock cycle, switches 42A and 52B are closed, switches 42B and 52A are open, and the boost signal is at the potential of V_{DD}. As a result, the A side portion operates similarly to the prior art voltage boosting circuit in the first half of a clock cycle. Specifically, the top terminal of capacitor 48A is connected to V_{DD} and the bottom terminal of capacitor 48A is

connected to the ground level (as a result of the high level boost signal being inverted by the inverter 50), causing capacitor 48A to be charged to V_{DD}. In the meantime, assuming capacitor 48B has been charged to V_{DD} during a previous half cycle, then the B side portion operates similarly to the prior art voltage boosting circuit in the second half of a clock cycle. That is, the potential at the bottom terminal of capacitor 48B is boosted to substantially $2V_{DD}$. The capacitor 48B then discharges to load 58 (*i.e.*, resistor R_L) to provide an output voltage at terminal 57. Consequently, the output voltage is first boosted to substantially $2V_{DD}$, and then decays as current is continuously delivered to load 58. Ex. 1001, 2:38-56. Ex. 1003, ¶¶56-58.

Symmetrically, during the second half of the clock cycle, switches 42A and 52B are open, switches 42B and 52A are closed, and the boost signal is dropped to the ground level. The A side portion and the B side portion switch roles, where capacitor 48B is charged to V_{DD}, and capacitor 48A (which has been charged to V_{DD} in the previous half cycle) is boosted to substantially $2V_{DD}$ and then discharges to provide the output voltage. As a result, the output voltage again is first boosted to substantially $2V_{DD}$, and then decays as current is continuously delivered to load 58. Ex. 1001, 2:56-63. Ex. 1003, ¶¶59-61.

The manner in which the output voltage (identified as V_R) changes over time is illustrated in FIG. 4 shown below. The output voltage V_R is boosted in both

halves of each clock cycle, thus the voltage is pumped twice as frequently as in the admitted prior art circuit. Ex. 1003, ¶62.

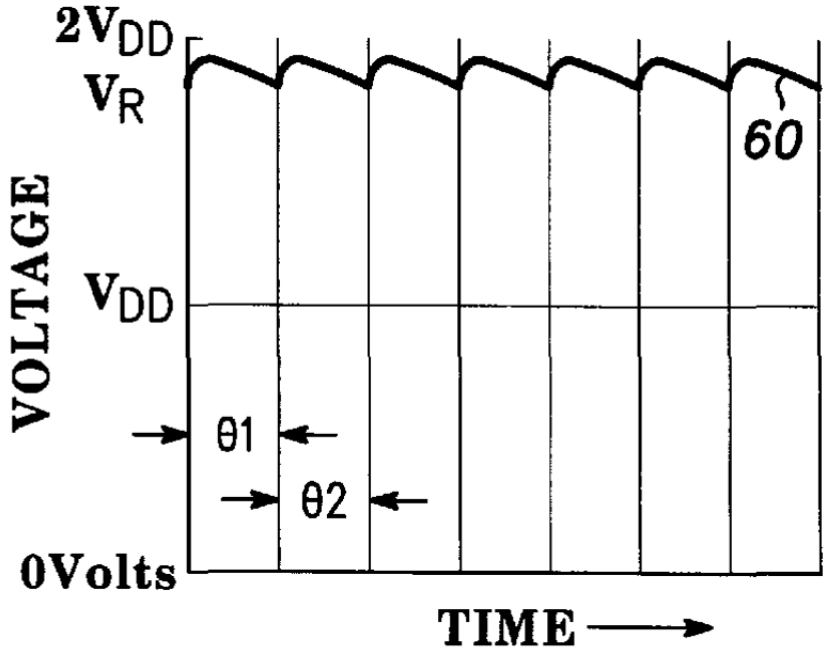


FIG. 4

Ex. 1001, FIG. 4

6. 875 PATENT PROSECUTION HISTORY

The application leading to the 875 Patent was originally filed on August 13, 1998 with 18 claims. Ex. 1002, pp. 8-24. In a Preliminary Amendment filed on February 17, 1999, Applicant added new claims 19-24. *Id.*, pp. 46-49. The added claims 19-21 were allowed in a first Office Action dated November 24, 1999, and

issued as claims 1-3 of the 875 Patent.[5] *Id.*, pp. 50-57, 75-78. During prosecution, the Examiner considered only three prior art references. Ex. 1003, ¶64.

[5] As to the prosecution of the non-issued claims, Applicant canceled original claims 10-18 in the Preliminary Amendment. In the first Office Action, claims 1 and 22 were rejected under 35 U.S.C. § 112; claim 1 was rejected as anticipated by U.S. Pat. No. 5,644,534 (Soejima); claims 2, 3, 5 and 6 were rejected as anticipated by U.S. Pat. No. 5,917,367 (Woo); and claims 23 and 24 were objected to as being dependent upon the rejected independent claim 22. Ex. 1002, pp. 50-57. In a Response dated April 7, 2000, Applicant canceled claims 1-9 and amended claims 22 and 23. *Id.*, pp. 60-64. In a second Office Action dated May 9, 2000, claim 22 was rejected under 35 U.S.C. § 112; and claims 22-24 were rejected as anticipated by U.S. Pat. No. 5,889,428 (Young). *Id.*, pp. 65-71. After Applicant canceled claims 22-24, the application was allowed and claims 19-21 issued as claims 1-3 respectively. *Id.*, pp. 73-78.

7. CLAIM CONSTRUCTION[6]

7.1. Applicable Law

The 875 Patent will expire on August 13, 2018 – a date which is before these proceedings will conclude. Accordingly, Petitioner has applied the claim construction principles of *Phillips* rather than the broadest reasonable interpretation standard applicable to non-expired patents. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (*en banc*).

7.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art (POSA) at the time of the invention and

[6] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 875 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 875 Patent.

consistent with the intrinsic record. Petitioner respectfully submits that the following terms should be construed for this IPR:

7.2.1. "buffer" limitations (claim 2)

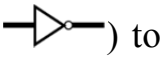
The 875 Patent does not define the term "buffer." Dictionary definitions for buffer include, for example, "an isolating circuit used to prevent a driven circuit from influencing a driving circuit," and "an electronic circuit to decouple the output of the buffer from its input, thus avoiding reaction between a driving and a driven circuit." Ex. 1010, pp. 6-7. Ex. 1011, p. 4. These definitions are consistent with the usage of "buffer" in the specification of the 875 Patent and consistent with the ordinary meaning of this term to a POSA. Ex. 1003, ¶¶77-78. Thus, under the *Phillips* standard, the term "buffer" would have been understood to mean "a circuit that isolates or decouples its output from its input." *Id.*, ¶78.

7.2.1.1. "inverting buffer"

The 875 Patent does not define the term "inverting buffer." A POSA would have understood that an inverting buffer refers to a buffer circuit that functions as an inverter. Ex. 1003, ¶¶44, 85. The Modern Dictionary of Electronics defines an inverter as "a circuit with one input and one output, and its function is to invert the input," and describes that "[w]hen the input is high, the output is low, and vice versa." Ex. 1014, p. 4. This definition is consistent with the usage of "inverting buffer" in the specification of the 875 Patent and consistent with the ordinary

meaning of this term to a POSA. Ex. 1003, ¶86. Also, as discussed above in Section 4.2, an inverting buffer can be a tri-state inverting buffer that behaves as an inverter only when it is enabled (*i.e.*, when its enabling signal is a certain value).

Thus, under the *Phillips* standard, the term "inverting buffer" would have been understood to mean "a circuit that isolates or decouples its output from its input, and when enabled, generates an output that is an inversion of its input (*i.e.*, when the input is high, the output is low, and vice versa)." Ex. 1003, ¶86.

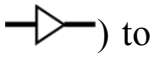
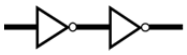
The 875 Patent uses the schematic symbol of a NOT Gate (*i.e.*, ) to represent an inverting buffer (*e.g.*, inverting buffer 50 in FIG. 3). Ex. 1001, FIG. 3. The specification of the 875 Patent, however, does not describe how the inverting buffer is implemented. Ex. 1003, ¶87.

7.2.1.2. "non-inverting buffer"

The 875 Patent does not define the term "non-inverting buffer." A POSA would have understood that a non-inverting buffer refers to a buffer circuit whose output is not inverted from its input. Ex. 1003, ¶¶43, 88. Also, as discussed above in Section 4.2, a non-inverting buffer can be a tri-state non-inverting buffer that behaves as a non-inverter only when it is enabled (*i.e.*, when its enabling signal is a certain value).

Thus, under the *Phillips* standard, the term "non-inverting buffer" would have been understood to mean "a circuit that isolates or decouples its output from

its input, and when enabled, generates an output that is not inverted from its input (*i.e.*, when the input is high, the output is high, and when the input is low, the output is low)." Ex. 1003, ¶89.

The 875 Patent uses the schematic symbol of a Buffer Gate (*i.e.*, ) to represent non-inverting buffer 56 in FIG. 3. Ex. 1001, FIG. 3. The specification of the 875 Patent, however, does not describe how the non-inverting buffer is implemented. Furthermore, as discussed above in Section 4.2, a non-inverting buffer can be implemented by, for example, sequentially connecting two inverting buffers into a cascade. Thus, a non-inverting buffer can also be represented using, for example, a cascade of two schematic symbols of a NOT Gate (*i.e.*, ). Ex. 1003, ¶90.

7.3. Clarification of Other Claim Terms

Although the following terms need not be construed for this IPR, Petitioner provides the following clarifications.

7.3.1. "coupled" limitations (claims 1-3)

7.3.1.1. "coupled to"

A term "A 'coupled to' B"[7] would not have been understood to mean that A

[7] "A" and "B" each represents a device or terminal in a circuit throughout this Petition.

and B must be directly connected. For example, as shown in FIG. 3, the 875 Patent discloses terminal 46 of capacitor 48A being connected to output terminal 57 via switch 52A. The specification of the 875 Patent describes that terminal 46 is coupled to output terminal 57 via switch 52A. Ex. 1001, 2:33-35 ("Terminals 46 and 54 are **coupled respectively via a pair of switches 52A and 52B to** output 57").[8] Ex. 1003, ¶69.

Moreover, the term "A 'coupled to' B" would not have been understood to mean that A and B are always connected. For example, the 875 Patent discloses terminal 46 of capacitor 48A being connected to output terminal 57 via switch 52A, even though switch 52A is open (thus disconnecting terminal 46 from output terminal 57) during the first half of each clock cycle. Ex. 1001, 2:38-56. Ex. 1003, ¶70.

7.3.1.2. "coupled between"

Similar to the term "coupled to," a term "A 'coupled between' B and C"[9] would not have been understood to mean that A must be directly connected to B and C. For example, as shown in FIG. 3, the 875 Patent describes that switch 42A is positioned between input terminal 44 and output terminal 57, with one end

[8] Emphasis is added throughout unless otherwise noted.

[9] "C" represents a device or terminal in a circuit throughout this Petition.

directly connected to input terminal 44 and another end connected to output terminal 57 via switch 52A. Ex. 1003, ¶72.

Additionally, similar to the term "coupled to," the term "A 'coupled between' B and C" would not have been understood to mean that A is always connected to B and C. Ex. 1003, ¶73.

7.3.1.3. "coupled for receiving"

A term "A 'coupled for receiving' D"[10] would not have been understood to mean that A must receive the exact voltage signal of D. For example, as shown in FIG. 3, the 875 Patent describes that capacitor 48A is "coupled for receiving" a boost signal via inverting buffer 50, and that capacitor 48B is "coupled for receiving" the boost signal via non-inverting buffer 56. Ex. 1003, ¶74. Yet, when the boost signal goes through a buffer, the output is not the exact same signal that was input to the buffer, but instead is a signal that is pulled from a power or ground rail depending on the value of the input and the type of buffer (*e.g.*, inverting, non-inverting). *Id*.

A term "A 'coupled for receiving' D" would not have been understood to mean that A must directly receive D. For example, the 875 Patent describes that capacitor 48A is "coupled for receiving" a boost signal by indirectly receiving an

[10] "D" represents a signal throughout this Petition.

inversion of the logical value of the boost signal via inverting buffer 50, and that capacitor 48B is "coupled for receiving" the boost signal by indirectly receiving the logical value of the boost signal via non-inverting buffer 56. Ex. 1003, ¶75.

Additionally, similar to the terms "coupled to" and "coupled between," the term "A 'coupled for receiving' D" would not have been understood to mean that A always receives (directly or indirectly) the logical value of D or an inversion of the logical value of D. Ex. 1003, ¶76.

8. PERSON OF ORDINARY SKILL IN THE ART

A POSA with respect to the technology described in the 875 Patent would be a person with at least a Bachelor of Science degree in electrical engineering or a closely related field, along with at least 4-5 years of experience in the design of integrated circuits. An individual with an advanced degree in a relevant field would require less experience in the design of integrated circuits. Ex. 1003, ¶¶27-31.

9. DESCRIPTION OF THE PRIOR ART

9.1. U.S. Patent No. 5,801,997 ("Hsieh")[11]

To address the same issue that motivated the alleged invention of the 875 Patent, Hsieh discloses the same voltage boosting circuit that is described in the 875 Patent, employing the same complementary double pumping voltage boost concept. In sum, just like the voltage boosting circuit of the 875 Patent, Hsieh's voltage boosting circuit has two symmetric boost circuits that generate a first instance and a second instance of a boost voltage in two halves of every clock cycle respectively, which are alternately used to bring the voltage of a signal line to a target boosted level. Ex. 1005, 3:2-20, FIG. 7. Hsieh even calls this circuit a "reciprocating or ping-pong voltage boosting circuit" (*id.,* Abstract), which is similar to the name "complimentary [sic] double pumping voltage boosting circuit" used in the 875 Patent. Ex. 1003, ¶96.

Hsieh begins by raising the same issue associated with a conventional boost circuit that is described in the 875 Patent. Specifically, like the 875 Patent, Hsieh

[11] Hsieh was filed on June 24, 1997 and issued on September 1, 1998, and is therefore prior art at least under § 102(e). *See* Ex. 1005. Hsieh was not cited to or discussed by the Examiner during prosecution of the 875 Patent. *See* Section 6 above.

describes a prior art boost circuit that uses the charging and discharging of a capacitor to provide a boosted voltage. Ex. 1005, 2:1-7, FIG. 1. For the same reason provided in the 875 Patent (*i.e.*, a certain time period is needed to recharge the capacitor in each clock cycle), Hsieh's prior art boost circuit causes a significant amount of distortion to the output voltage, *i.e.*, it can only generate a boosted voltage for a small portion of a clock cycle, and the output voltage falls below a desired power supply voltage for a large portion of the clock cycle (which is described as a recovery time in Hsieh). *Id.,* 2:39-57, FIG. 3a. Hsieh further describes that shortening the recovery time for the conventional boost circuit is impractical because it will result in an incomplete recovery, which causes the output voltage to decrease progressively in subsequent cycles and which will lead to a fault within the memory. *Id.,* 2:58-67, FIG. 3b. Ex. 1003, ¶¶92-94.

To address this issue, Hsieh teaches a ping-pong boost circuit that has the same architecture and components, and operates in the same manner, as the complementary double pumping voltage boost circuit described in the 875 Patent. Ex. 1003, ¶95. Hsieh's ping-pong boost circuit is shown in FIG. 7, which is reproduced below with colored annotations identifying the corresponding components recited in the claims and shown in FIG. 3 of the 875 Patent (*see* Section 5, above).

1. A boost circuit having an input terminal and an output terminal, comprising:
a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;

a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;

a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and

a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.

2. The boost circuit of claim 1, further including:

an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and

a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor.

3. The boost circuit of claim 1, further including:

a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and

a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal.

(Ex. 1001, 5:9-6:17.)

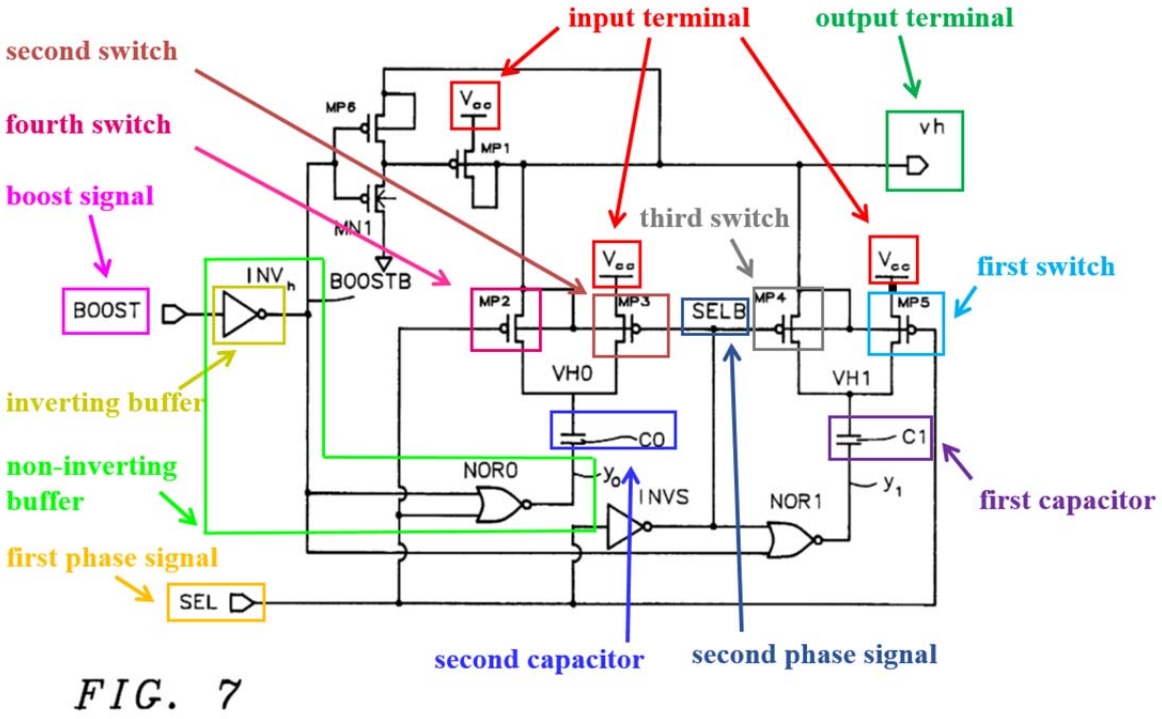


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

As shown in FIG. 7, Hsieh's ping-pong boost circuit has a pMOSFET transistor Mp5 (*i.e.*, a first switch) coupled between an input terminal that receives a power supply voltage source V_{cc} and an output terminal that provides an output voltage V_h, and a pMOSFET transistor Mp3 (*i.e.*, a second switch) coupled between the input terminal and the output terminal. Ex. 1005, 4:66-5:4, 5:16-21, FIG. 7. Transistor Mp5 is operated by select signal SEL (*i.e.*, a first phase signal), and transistor Mp3 is operated by signal SELB (*i.e.*, a second phase signal). *Id.*, 4:66-5:4, 5:16-21, FIG. 7. As shown in FIG. 7 and described in the specification of Hsieh, SELB is inverted from select signal SEL by inverter INVS, and thus SEL and SELB are opposite to each other. *Id.*, 5:31-33, FIG. 7. Ex. 1003, ¶¶98-100.

Hsieh's ping-pong boost circuit also has a first capacitor C1 with top terminal VH1 coupled to the output terminal and a bottom terminal that receives output signal y1 of NOR gate NOR1, and a second capacitor C0 with top terminal VH0 coupled to the output terminal and a bottom terminal that receives output signal y0 of NOR gate NOR0. Ex. 1005, 5:5-11, 5:22-29, FIG. 7. Both signals y1 and y0 are generated from a boost signal BOOST. *Id.*, FIG. 7. Hsieh's ping-pong boost circuit further has a pMOSFET transistor Mp4 (*i.e.*, a third switch) coupled between top terminal VH1 of capacitor C1 and the output terminal, and a pMOSFET transistor Mp2 (*i.e.*, a fourth switch) coupled between top terminal VH0 of capacitor C0 and the output terminal. *Id.*, 4:61-65, 5:12-15, FIG. 7. Transistor Mp4 is operated by signal SELB, and transistor Mp2 is operated by select signal SEL. *Id.* Ex. 1003, ¶¶101-104.

As shown in FIG. 7 and described in the specification, Hsieh's ping-pong boost circuit operates in the same manner as the voltage boost circuit of the 875 Patent. Specifically, when boost signal BOOST is logical 1 and select signal SEL is logical 0, transistors Mp5 and Mp2 are conducting, and transistors Mp3 and Mp4 are not conducting. The output signal of NOR Gate NOR0 (*i.e.*, y0) is logical 1, which means output signal y0 is "placed at the level of the power supply voltage source V_{cc}." Ex. 1005, 5:53-57. Thus, the bottom terminal of capacitor C0 is at V_{cc}. As a result, top terminal VH0 of capacitor C0 is boosted to substantially $2V_{cc}$

(assuming capacitor C0 has previously been charged to V_{cc}). Like capacitor 48B in the first half of a clock cycle in the 875 Patent, capacitor C0 discharges to provide output voltage V_h. *Id.*, 5:53-61, FIG. 7. Ex. 1003, ¶105.

Symmetrically and similarly, when boost signal BOOST is logical 1 and select signal SEL is logical 1, transistors Mp5 and Mp2 are not conducting, and transistors Mp3 and Mp4 are conducting. The output signal of NOR Gate NOR1 (*i.e.*, y1) is logical 1, which means output signal y1 is "placed at the level of the power supply voltage source V_{cc}." Ex. 1005, 6:11-15. Thus, the bottom terminal of capacitor C1 is at V_{cc}. As a result, top terminal VH1 of capacitor C1 is boosted to substantially $2V_{cc}$ (assuming capacitor C1 has previously been charged to V_{cc}). Like capacitor 48A in the second half of the clock cycle in the 875 Patent, capacitor C1 discharges to provide output voltage V_h. *Id.*, 6:11-19, FIG. 7. Ex. 1003, ¶106.

Additionally, when boost signal BOOST is logical 0, both output signals y0 and y1 are logical 0. And, regardless what logical value select signal SEL takes, the circuit causes both terminals VH0 and VH1 to be connected to the power supply voltage source V_{cc}. As a result, both capacitors C0 and C1 are being charged to V_{cc}. Ex. 1005, 5:36-52, 5:62-6:10, FIG. 7. Ex. 1003, ¶107.

10. GROUND #1: CLAIMS 1-3 OF THE 875 PATENT ARE UNPATENTABLE AS BEING ANTICIPATED BY HSIEH

10.1. Claim 1 is anticipated by Hsieh

10.1.1. [1.0] "A boost circuit having an input terminal and an output terminal, comprising:"

To the extent that the preamble is limiting, Hsieh discloses this limitation. Specifically, Hsieh discloses a ping-pong boost circuit ("boost circuit") having an input terminal for receiving a power supply voltage source V_{cc} ("input terminal") and an output terminal V_h ("output terminal"). Ex. 1005, at Title ("**Ping-Pong Boost Circuit**"), Abstract ("A reciprocating or **ping-pong voltage boosting circuit** is described"), 4:50-53 ("An embodiment of the **ping-pong boost circuit** is shown in FIG. 7. The p-type MOSFET (pMOSFET) Mp1 has a source connected [to] the **power supply voltage source V_{cc}** and a drain and bulk connected to the **output terminal V_h**."), FIG. 7. Ex. 1003, ¶133.

As shown in FIG. 7 (reproduced below with annotations), the sources of pMOSFET transistors Mp1, Mp3 and Mp5 are all connected to the power supply voltage source V_{cc}. Ex. 1005, 4:66-67, 5:16-17, FIG. 7. A POSA would have understood that the sources of those transistors are essentially connected to a common input terminal that receives the power supply voltage source V_{cc}. That is, those transistors share the same input terminal. Ex. 1003, ¶134.

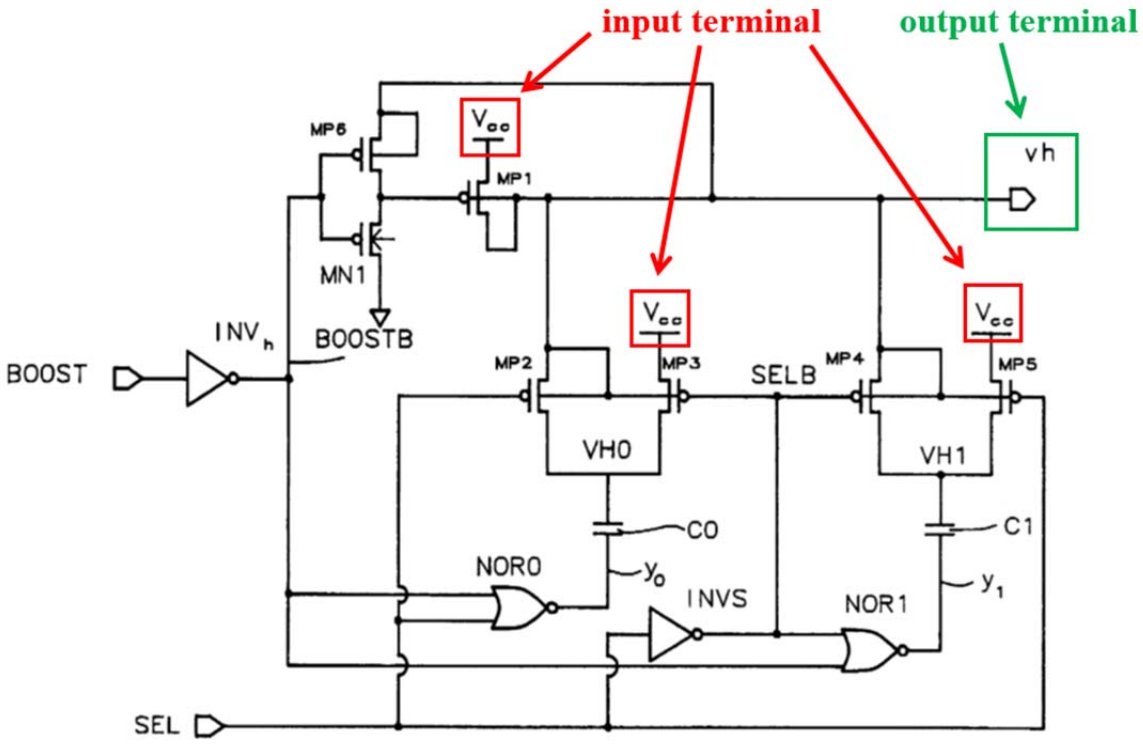


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Thus, by disclosing the ping-pong boost circuit ("boost circuit") that has an input terminal V_{cc} ("input terminal") and an output terminal V_h ("output terminal"), Hsieh discloses a boost circuit having an input terminal and an output terminal.

10.1.2. [1.1] "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;"

Hsieh discloses this limitation.

First, Hsieh discloses that transistor Mp5 ("first switch") is operated by select signal SEL ("first phase signal")[12]. Specifically, as shown in FIG. 7 (reproduced below with annotations), Hsieh discloses that transistor Mp5's gate is connected to select signal SEL. Ex. 1005, 5:16-21, FIG. 7. Hsieh further describes that conducting of transistor Mp5 is controlled by select signal SEL. *Id.,* 5:36-47 (describing that transistor Mp5 is conducting when select signal SEL is logical 0), 5:62-6:6 (describing that transistor Mp5 is not conducting when select signal SEL is logical 1). Thus, transistor Mp5 is a switch operated by select signal SEL, which is the first phase signal. Ex. 1003, ¶137.

[12] Note that SEL is opposite in phase to SELB (see following limitation, [1.2]), and is a "phase signal" because it has phases in which it is logical 0 and logical 1. Ex. 1005, 5:36-6:6.

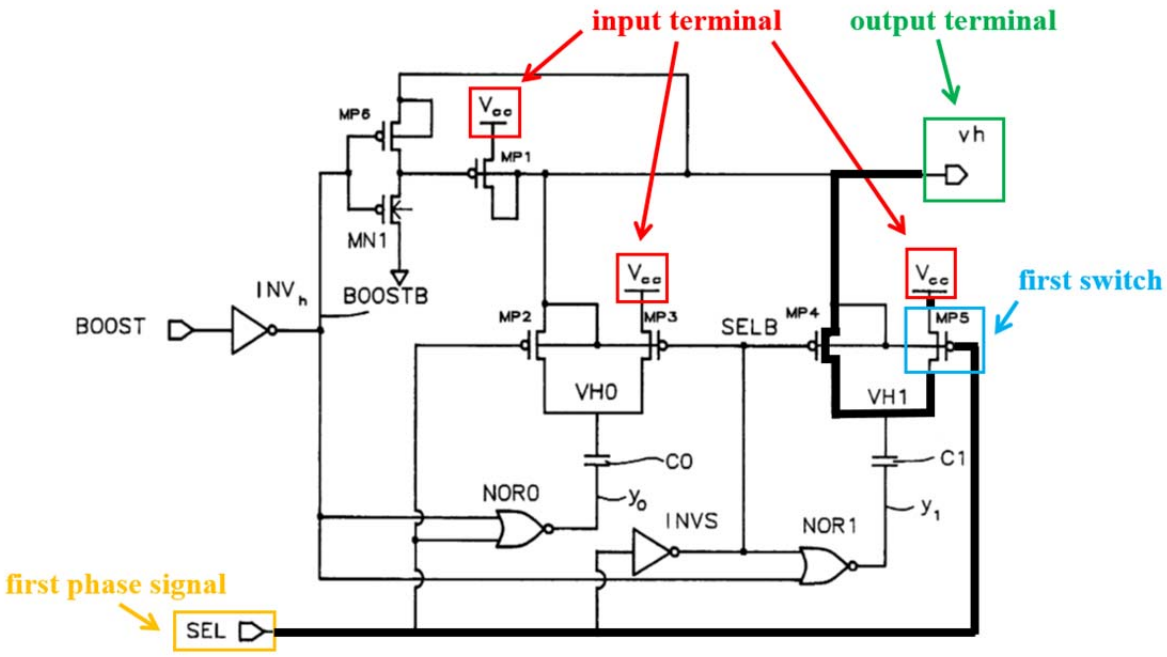


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Second, Hsieh discloses that the transistor Mp5 ("first switch") is coupled between input terminal V_{cc} ("input terminal") and output terminal V_h ("output terminal"). As shown in FIG. 7, transistor Mp5 is positioned between input terminal V_{cc} and output terminal V_h. Specifically, transistor Mp5 is directly connected to input terminal V_{cc} and connected to output terminal V_h via transistor Mp4. Ex. 1005, 5:12-21, FIG. 7. Ex. 1003, ¶138. Thus, transistor Mp5 is coupled between input terminal V_{cc} and output terminal V_h. *See* Section 7.3.1.2. Ex. 1003, ¶98.

Thus, by disclosing that transistor Mp5 ("first switch") is operated by select signal SEL ("first phase signal"), and is connected to input terminal V_{cc} and output terminal V_h ("coupled between the input terminal and the output terminal"), Hsieh discloses a first switch coupled between the input terminal and the output terminal and operated by a first phase signal.

10.1.3. [1.2] "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;"

Hsieh discloses this limitation.

First, Hsieh discloses that transistor Mp3 ("second switch") is operated by signal SELB ("second phase signal"). Specifically, as shown in FIG. 7 (reproduced below with annotations), Hsieh discloses that transistor Mp3's gate is connected to signal SELB. Ex. 1005, 5:1-3. Ex. 1003, ¶141.

Signal SELB ("second phase signal") is opposite to select signal SEL ("first phase signal"). Hsieh describes that signal SELB is inverted from select signal SEL by inverter INVS. Ex. 1005, 4:66-5:4, 5:31-33 ("**The inverter INVS forms the inverted form of the select signal SELB from the input SELECT**"), FIG. 7. Hsieh also describes that the two signals take opposite logical values at the same time (*i.e.*, when one is logical 1, the other is logical 0, and vice versa). *Id.*, 5:36-39 ("If … the select signal[] is at a logical 0 … the inverted select signal SELB is at a logical 1."), 5:62-65 ("Now if … the select signal[] will change to a logical 1 …

the inverted select signal SELB is at a logical 0."). Ex. 1003, ¶¶142-143. Furthermore, a POSA would have understood that "SELB" means SEL "bar" which, by convention, is the opposite of SEL. *Id.*, ¶144. Additionally, a POSA would have understood that, in light of FIGS. 5 and 7 of the 875 Patent,[13] the first and second phase signals are opposite to each other even though the signal paths for SEL and SELB are not identical. *Id.*, ¶145. Thus, SELB ("second phase signal") is opposite to SEL ("first phase signal"). *Id.*, ¶145.

Hsieh further describes that signal SELB controls when transistor Mp3 is conducting. Ex. 1005, 5:36-47 (describing that transistor Mp3 is not conducting when select signal SEL is logical 0, or equivalently, when signal SELB is logical 1), 5:62-6:6 (describing that transistor Mp3 is conducting when select signal SEL is logical 1 or, equivalently, when signal SELB is logical 0). Thus, transistor Mp3

[13] FIGS. 5 and 7 of the 875 Patent show that a first clock signal θ_1 goes through voltage translator 86 to operate switch 74, and a second clock signal θ_2 goes through another voltage translator 120 plus capacitor 124 to operate switch 82. Ex. 1001, 3:40-48, 4:28-36, FIGS. 5 and 7. The 875 Patent still treats the two clock signals as being opposite. *Id.,* 5:11-15. Accordingly, a POSA would have understood that, even though the signal paths for θ_1 and θ_2 in the 875 Patent are not identical, the signals are nonetheless considered to be opposite. Ex. 1003, ¶146.

is a switch operated by signal SELB, which is the second phase signal opposite to select signal SEL ("first phase signal"). Ex. 1003, ¶146.

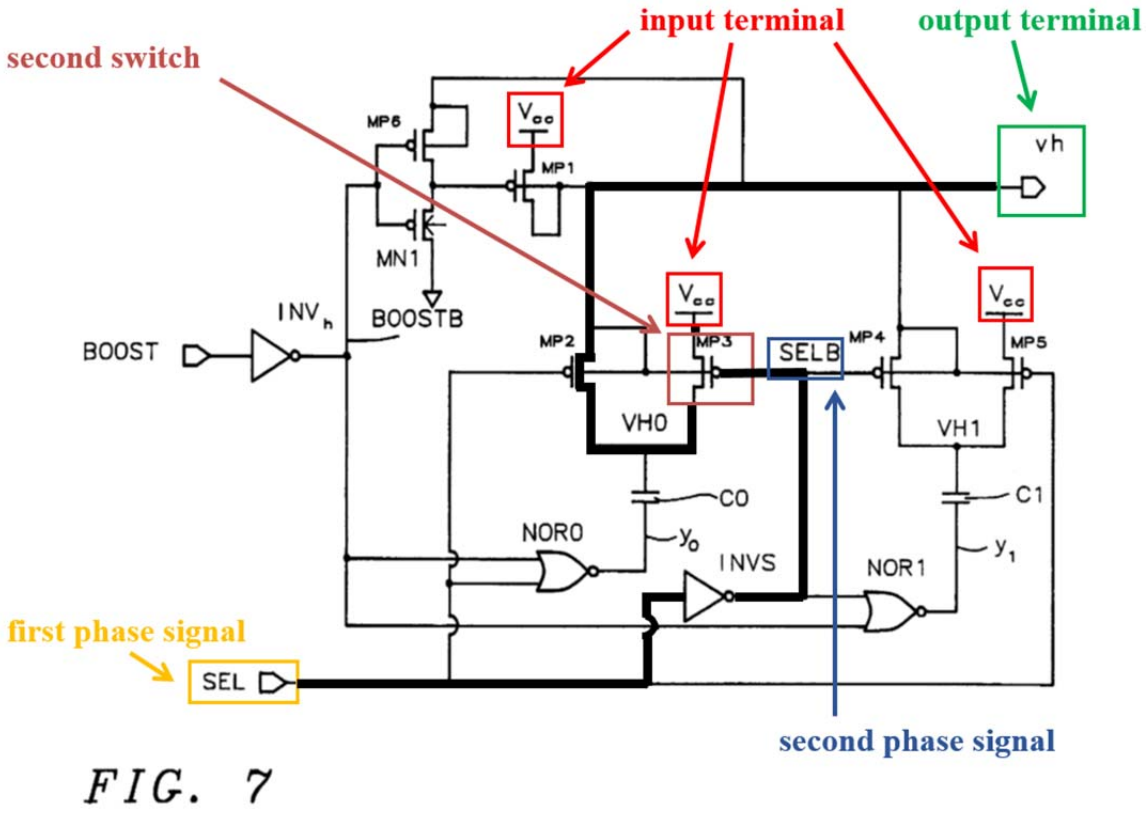


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Second, Hsieh discloses that transistor Mp3 ("second switch") is coupled between input terminal V_{cc} ("input terminal") and output terminal V_h ("output terminal"). As shown in FIG. 7, transistor Mp3 is positioned between input terminal V_{cc} and output terminal V_h. Specifically, transistor Mp3 is directly connected to input terminal V_{cc} and connected to output terminal V_h via transistor Mp2. Ex. 1005, 4:66-5:4, FIG. 7. Ex. 1003, ¶147. Thus, transistor Mp3 is

coupled between input terminal and output terminal. *See* Section 7.3.1.2. Ex. 1003, ¶99.

Thus, by disclosing that transistor Mp3 ("second switch") is (a) operated by signal SELB ("second phase signal"), which is opposite to select signal SEL ("first phase signal"), and (b) connected to input terminal V_{cc} and connected to output terminal V_h ("coupled between the input terminal and the output terminal"), Hsieh discloses a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal.

10.1.4. [1.3] "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and"

Hsieh discloses this limitation.

First, Hsieh discloses that capacitor C1 ("first capacitor") has top terminal VH1 ("first terminal") coupled to output terminal V_h ("output terminal"). Specifically, as shown in FIG. 7 (reproduced below with annotations), Hsieh discloses that top terminal VH1 of capacitor C1 is connected to output terminal V_h via transistor Mp4. Ex. 1005, 5:12-29, FIG. 7. Thus, top terminal VH1 of capacitor C1 is coupled to output terminal V_h. *See* Section 7.3.1.1. Ex. 1003, ¶150.

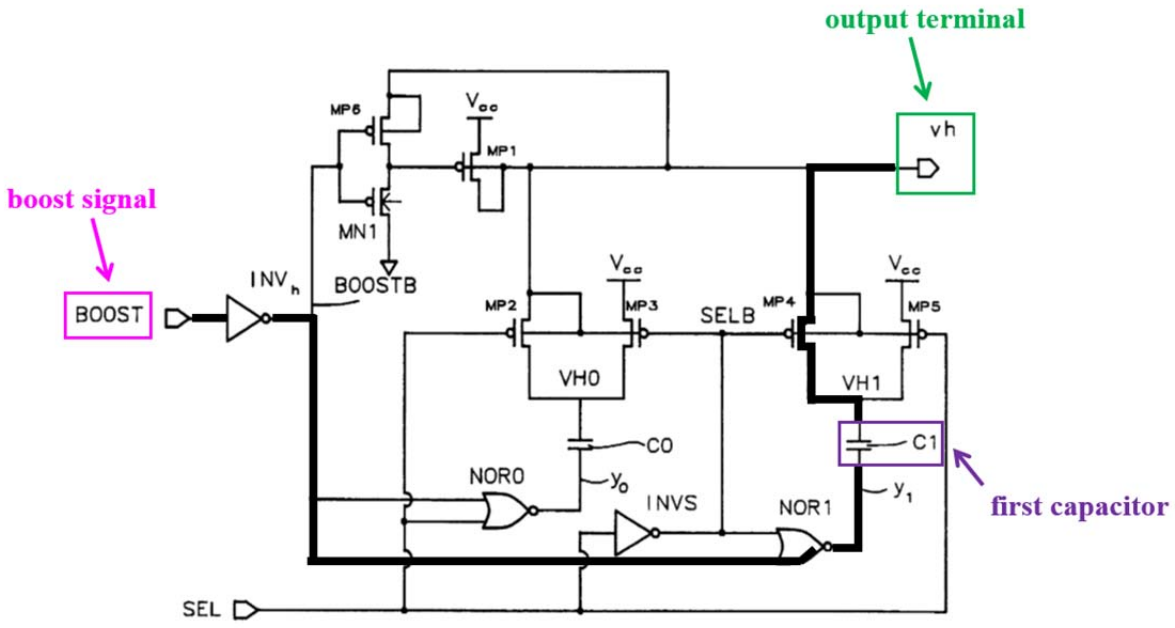


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Second, Hsieh discloses that capacitor C1 ("first capacitor") has a bottom terminal ("second terminal") coupled for receiving a signal BOOST ("boost signal").[14] Specifically, as shown in FIG. 7, Hsieh discloses a circuit, including

[14] Signal BOOST is a "boost signal." Not only is it named "BOOST," but it is input to the ping-pong boost circuit and is used to generate a boosted voltage. Specifically, signal BOOST is used to boost the voltage of capacitors C0, C1 to generate a boosted voltage for the ping-pong boost circuit. Thus, it is a boost signal. *See* Ex. 1005, 5:36-6:19, FIG. 7. Ex. 1003, ¶155.

inverter INVB,[15] inverter INVS, and NOR gate NOR1, which receives signal BOOST as an input and outputs the signal y1 to the bottom terminal of capacitor C1. Ex. 1005, 5:22-29, FIG. 7. A POSA would have understood that this circuit is a non-inverting buffer that operates similarly to the tri-state non-inverting buffer discussed above in Section 4.2 (*i.e.*, with select signal SEL serving as an enabling signal). Specifically, when SEL is logical 1, this non-inverting buffer is enabled, and output y1 is the logical value of the input BOOST. When SEL is logical 0, this non-inverting buffer is disabled, and output y1 is always logical 0 regardless of the value of its input BOOST. Thus, when the non-inverting buffer is enabled, the output signal y1 is the logical value of the input BOOST. Ex. 1003, ¶¶152-153. Thus, the bottom terminal of capacitor C1 is coupled for receiving signal BOOST. *See* Section 7.3.1.3. *Id*., ¶¶152-154.

Thus, by disclosing capacitor C1 ("first capacitor") having top terminal VH1 connected to output terminal V_h via transistor Mp4 ("first terminal coupled to the output terminal"), and a bottom terminal coupled to a circuit (including inverter INVB, inverter INVS, and NOR gate NOR1) for receiving signal BOOST ("second terminal coupled for receiving a boost signal"), Hsieh discloses a first capacitor

[15] This inverter is described in the specification of Hsieh as "INVB" while mistakenly labeled as "INVh" in FIG. 7. *See, e.g.*, Ex. 1005, 5:30-35.

having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal.

10.1.5. [1.4] "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal."

Hsieh discloses this limitation.

First, Hsieh discloses that capacitor C0 ("second capacitor") has top terminal VH0 ("first terminal") coupled to output terminal V_h ("output terminal"). Specifically, as shown in FIG. 7 (reproduced below with annotations), Hsieh discloses that top terminal VH0 of capacitor C0 is connected to output terminal V_h via transistor Mp2. Ex. 1005, 4:61-5:11, FIG. 7. Thus, top terminal VH0 of capacitor C0 is coupled to output terminal V_h. *See* Section 7.3.1.1. Ex. 1003, ¶158

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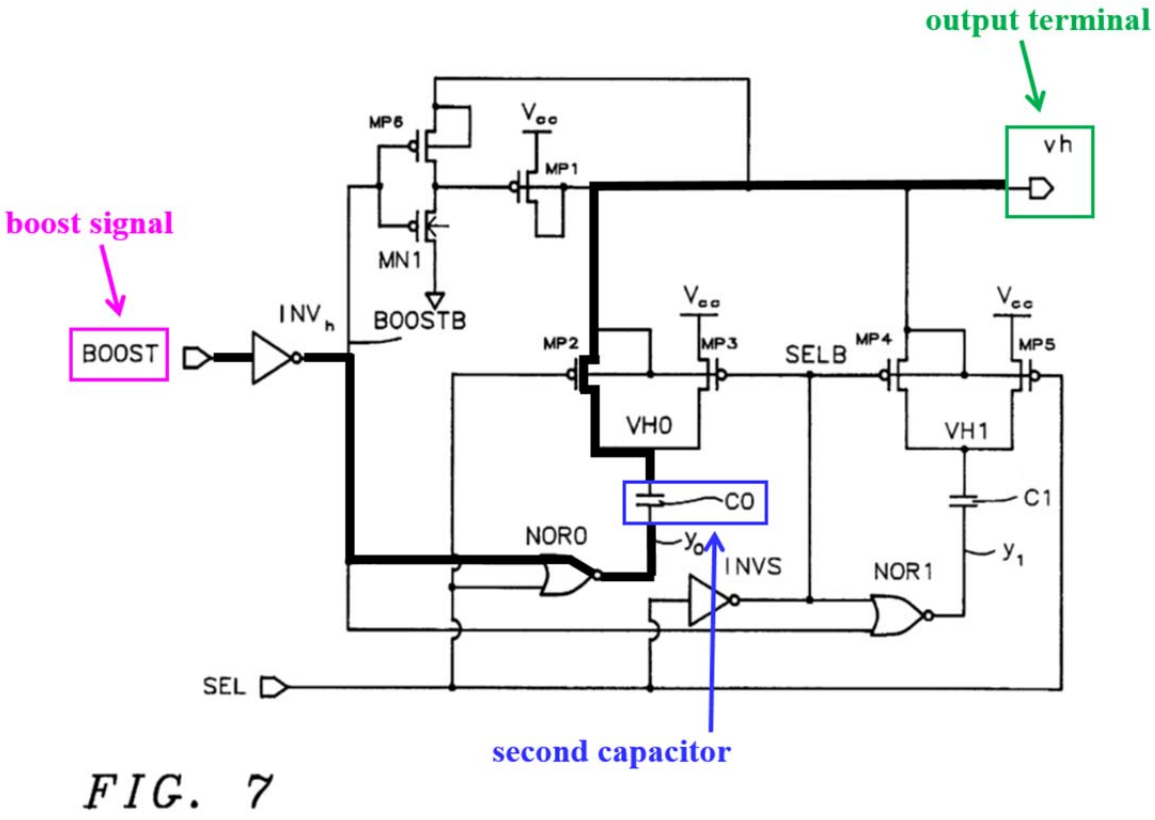


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Second, Hsieh discloses that capacitor C0 ("second capacitor") has a bottom terminal ("second terminal") coupled for receiving signal BOOST ("boost signal"). Specifically, as shown in FIG. 7, Hsieh discloses a circuit, including inverter INVB and NOR gate NOR0, which receives signal BOOST as an input and outputs signal y0 to the bottom terminal of capacitor C0. Ex. 1005, 5:6-11, FIG. 7. Similar to above analysis for Claim [1.3] in Section 10.1.4, a POSA would have understood that this circuit is a non-inverting buffer that operates similarly to the tri-state non-inverting buffer discussed above in Section 4.2 (*i.e.*, with select signal SEL serving

as an enabling signal). Specifically, when SEL is logical 0, this non-inverting buffer is enabled, and output y0 is the logical value of input BOOST. When SEL is logical 1, this non-inverting buffer is disabled, and output y0 is always logical 0 regardless of the value of its input BOOST. Thus, when the non-inverting buffer is enabled, the output signal y0 is the logical value of input BOOST. *See also* analysis for Claim [2.2] in Section 10.2.3 below. Ex. 1003, ¶161. Thus, the bottom terminal of capacitor C0 is coupled for receiving signal BOOST. *See* Section 7.3.1.3. *Id*., ¶159.

Thus, by disclosing capacitor C0 ("second capacitor") having top terminal VH0 connected to output terminal V_h via transistor Mp2 ("first terminal coupled to the output terminal"), and a bottom terminal coupled to a circuit (including inverter INVB and NOR gate NOR0) for receiving signal BOOST ("second terminal coupled for receiving the boost signal"), Hsieh discloses a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.

10.2. Claim 2 is anticipated by Hsieh

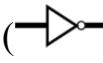
10.2.1. [2.0] "The boost circuit of claim 1, further including:"

Hsieh discloses this limitation. *See* above analysis for Claim 1, Section 10.1.

10.2.2. [2.1] "an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and"

Under the *Phillips* standard, "inverting buffer" means "a circuit that isolates or decouples its output from its input, and when enabled, generates an output that is an inversion of its input (*i.e.*, when the input is high, the output is low, and vice versa)." *See* Section 7.2.1.1.

Hsieh discloses this limitation.

First, Hsieh discloses an inverting buffer, namely, inverter INVB. Specifically, as shown in FIG. 7 (reproduced below with annotations) and described in the specification, inverter INVB is illustrated as an inverting buffer (), it decouples its input signal BOOST ("boost signal") and its output signal BOOSTB, and it inverts its input signal BOOST to generate its output signal BOOSTB. Ex. 1005, 5:30-31 ("**The inverter INVB forms the inverted boost signals BOOSTB from the input BOOST**"), FIG. 7. Thus, inverter INVB is an inverting buffer. *See* Section 7.2.1.1. Ex. 1003, ¶165.

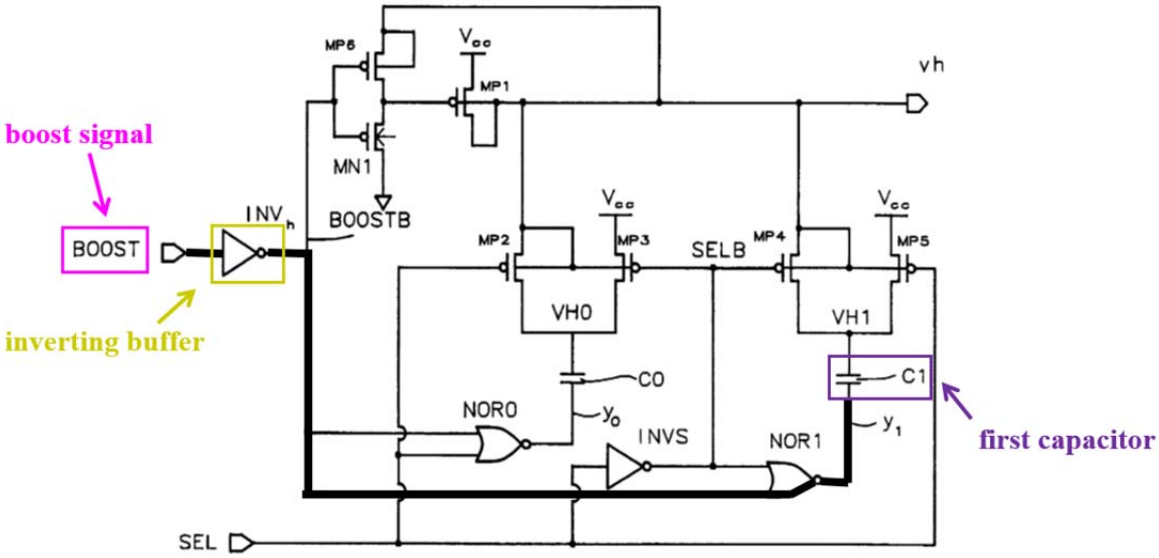


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Second, Hsieh discloses that inverter INVB ("inverting buffer") has an input coupled for receiving signal BOOST ("boost signal"). Specifically, as shown in FIG. 7, inverter INVB directly receives signal BOOST as its input. Ex. 1005, 5:30-31, FIG. 7. Ex. 1003, ¶166.

Third, Hsieh discloses that inverter INVB ("inverting buffer") has an output coupled to the bottom terminal ("second terminal") of capacitor C1 ("first capacitor"). Specifically, as shown in FIG. 7, the output of inverter INVB is connected to the bottom terminal of capacitor C1 via NOR gate NOR1. Ex. 1005, 5:22-26, FIG. 7. Thus, the output of inverter INVB is coupled to the bottom terminal of capacitor C1. *See* Section 7.3.1.1. Ex. 1003, ¶167.

Thus, by disclosing inverter INVB ("inverting buffer") having an input receiving signal BOOST ("an input coupled for receiving the boost signal") and an output connected to the bottom terminal of capacitor C1 via NOR gate NOR1 ("an output coupled to the second terminal of the first capacitor"), Hsieh discloses an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor.

10.2.3. [2.2] "a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor."

Under the *Phillips* standard, "non-inverting buffer" means "a circuit that isolates or decouples its output from its input, and when enabled, generates an output that is not inverted from its input (*i.e.*, when the input is high, the output is high, and when the input is low, the output is low)." *See* Section 7.2.1.2.

Hsieh discloses this limitation.

First, Hsieh discloses a non-inverting buffer, namely, a circuit including inverter INVB and NOR gate NOR0 (identified in below FIG. 7). Specifically, as shown in FIG. 7 (reproduced below with annotations), this buffer circuit decouples its input (*i.e.*, BOOST, the "boost signal") and its output (*i.e.*, y0). Ex. 1005, 5:5-9, FIG. 7. Ex. 1003, ¶¶169-170.

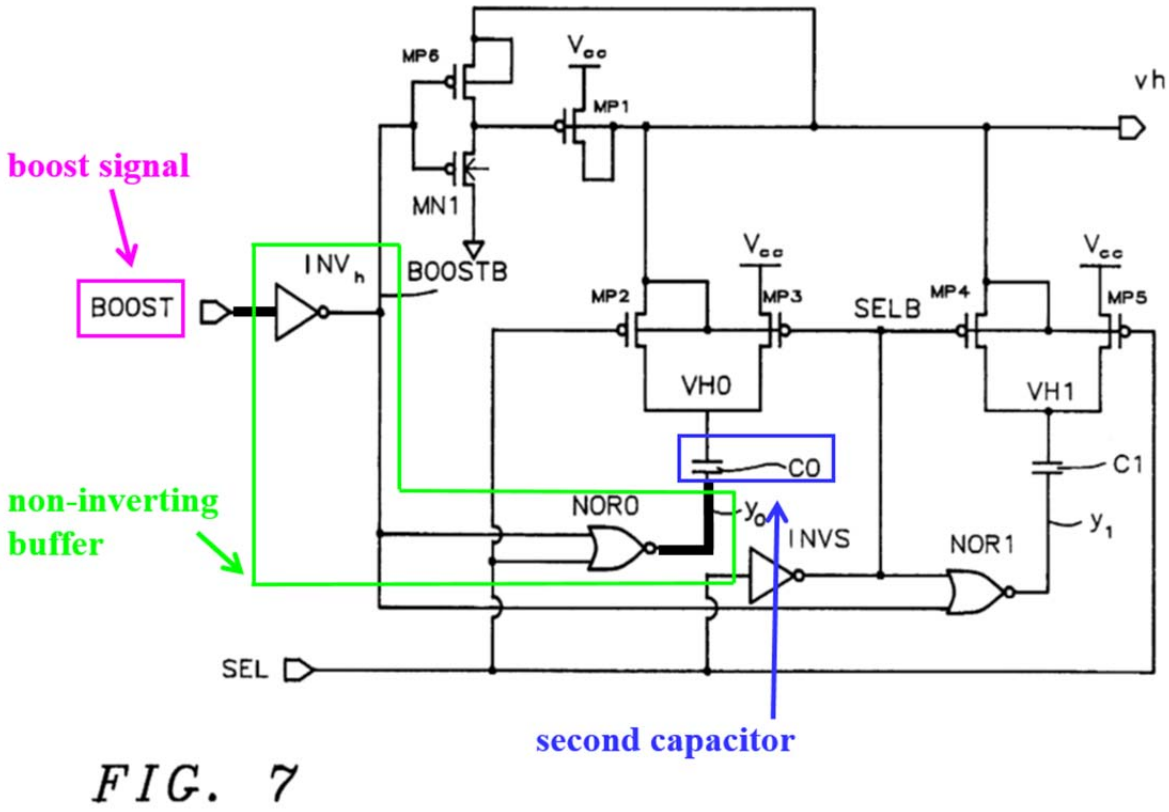


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Furthermore, when select signal SEL is logical 0, this circuit's output (*i.e.*, y0) is not inverted from its input (*i.e.*, BOOST). When select signal SEL is logical 1, this circuit's output (*i.e.*, y0) is always logical 0 regardless of its input (*i.e.*, BOOST). A POSA would have understood that such a circuit operates similarly to the tri-state non-inverting buffer that is discussed above in Section 4.2. *See also* analysis for Claim [1.4] in Section 10.1.5 above. Ex. 1003, ¶171. Specifically, select signal SEL is an "enabling signal" for this circuit. *Id.*, ¶171. That is, the circuit is "enabled" (*i.e.*, output y0 changes with, or depends on, input BOOST)

when select signal SEL is logical 0, and is "disabled" (*i.e.*, output y0 does not change with, and does not depend on, input BOOST) when select signal SEL is logical 1. *Id.*, ¶171. The truth table below illustrates the relationship among the input signal (*i.e.*, BOOST), output signal (*i.e.*, y0), and "enabling signal" (*i.e.*, SEL) of this circuit. *Id.*, ¶171.

BOOST	y0	SEL
1	**1**	**0 (enabled)**
0	**0**	
1	**0**	**1 (disabled)**
0		

Thus, the above-described circuit is a non-inverting buffer because it decouples its output (*i.e.*, y0) from its input (*i.e.*, BOOST), and when it is "enabled" (*i.e.*, when select signal SEL is logical 0), its output is not inverted from its input (*i.e.*, when BOOST is high, y0 is high, and when BOOST is low, y0 is low). *See* Section 7.2.1.2. Ex. 1003, ¶172.

Second, Hsieh discloses that this non-inverting buffer circuit has an input coupled for receiving signal BOOST ("boost signal"). Specifically, as shown in FIG. 7, inverter INVB directly receives signal BOOST as its input. Ex. 1005, 5:30-31, FIG. 7. Thus, the input of the non-inverting buffer circuit is coupled for receiving signal BOOST. Ex. 1003, ¶173.

Third, Hsieh discloses that this non-inverting buffer circuit has an output coupled to the bottom terminal ("second terminal") of capacitor C0 ("second capacitor"). Specifically, as shown in FIG. 7, NOR gate NOR0 has an output directly connected to the bottom terminal of capacitor C0. Ex. 1005, 5:5-6, FIG. 7. Thus, the output of the non-inverting buffer circuit is coupled to the bottom terminal of capacitor C0. Ex. 1003, ¶174.

Thus, by disclosing a circuit (formed by inverter INVB and NOR gate NOR0) that has an input receiving signal BOOST ("an input coupled for receiving the boost signal") and an output connected to the bottom terminal of capacitor C0 ("an output coupled to the second terminal of the second capacitor"), and that operates similarly to a tri-state non-inverting buffer, Hsieh discloses a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor.

10.3. Claim 3 is anticipated by Hsieh

10.3.1. [3.0] "The boost circuit of claim 1, further including:"

Hsieh discloses this limitation. *See* above analysis for Claim 1, Section 10.1.

10.3.2. [3.1] "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and"

Hsieh discloses this limitation.

First, Hsieh discloses that transistor Mp4 ("third switch") is operated by signal SELB ("second phase signal"). Specifically, as shown in FIG. 7 (reproduced below with annotations), Hsieh discloses that transistor Mp4's gate is connected to signal SELB. Ex. 1005, 5:12-15, FIG. 7. Hsieh further describes that SELB controls when transistor Mp4 is conducting. *Id.*, 5:36-47 (describing that transistor Mp4 is not conducting when select signal SEL is logical 0 or, equivalently, when signal SELB is logical 1), 5:62-6:6 (describing that transistor Mp4 is conducting when select signal SEL is logical 1, or equivalently, when signal SELB is logical 0). Thus, transistor Mp4 is a switch operated by signal SELB, which is the second phase signal. Ex. 1003, ¶¶177-178.

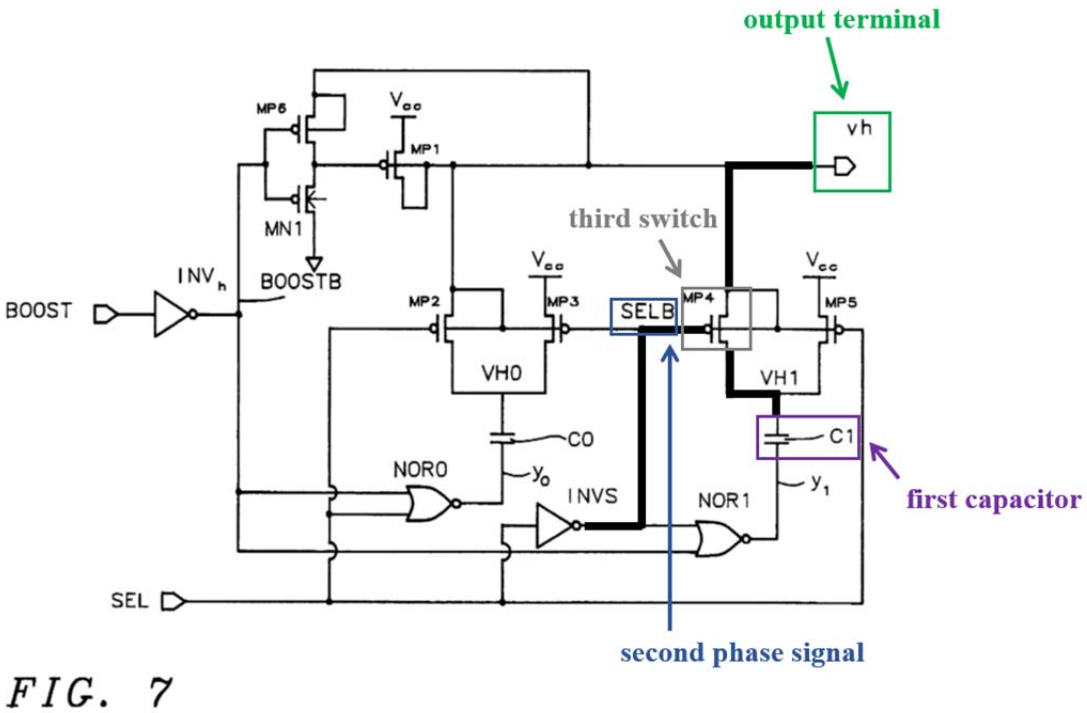


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Second, as shown in FIG. 7, Hsieh discloses that transistor Mp4 ("third switch") is coupled between top terminal VH1 of capacitor C1 ("first terminal of the first capacitor") and output terminal V_h ("output terminal"). Ex. 1005, FIG. 7. Ex. 1003, ¶179.

Thus, by disclosing transistor Mp4 ("third switch") that is operated by signal SELB ("second phase signal"), and is coupled between top terminal VH1 of capacitor C1 and output terminal V_h ("coupled between the first terminal of the first capacitor and the output terminal"), Hsieh discloses a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal.

10.3.3. [3.2] "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal."

Hsieh discloses this limitation.

First, Hsieh discloses that transistor Mp2 ("fourth switch") is operated by select signal SEL ("first phase signal"). Specifically, as shown in FIG. 7 (reproduced below with annotations), Hsieh discloses that transistor Mp2's gate is connected to select signal SEL. Ex. 1005, 4:61-65, FIG. 7. Hsieh further describes that SEL controls when transistor Mp2 is conducting. *Id.*, 5:36-47 (describing that transistor Mp2 is conducting when select signal SEL is logical 0), 5:62-6:6 (describing that transistor Mp2 is not conducting when select signal SEL is logical

1). Thus, transistor Mp2 is a switch operated by select signal SEL, which is the first phase signal. Ex. 1003, ¶182.

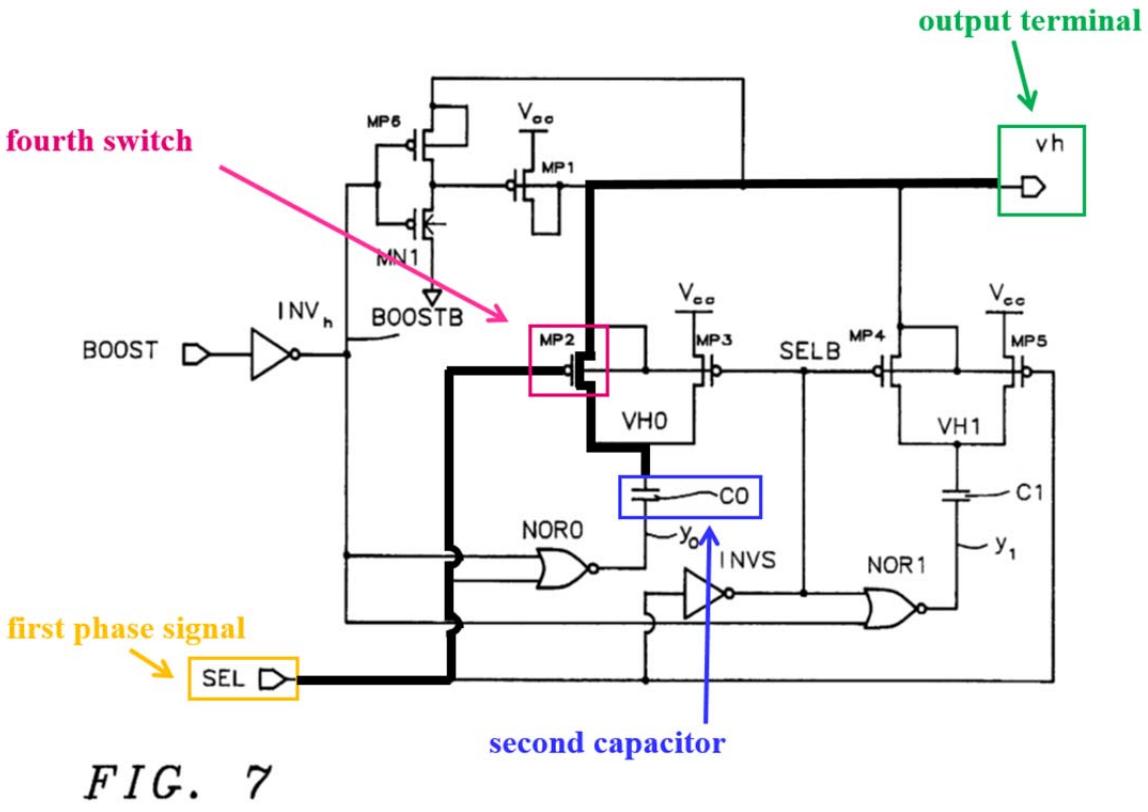


FIG. 7

Ex. 1005, FIG. 7 (with annotations)

Second, as shown in FIG. 7, Hsieh discloses that transistor Mp2 ("fourth switch") is coupled between top terminal VH0 of capacitor C0 ("first terminal of the second capacitor") and output terminal V_h ("output terminal"). Ex. 1005, FIG. 7. Ex. 1003, ¶183.

Thus, by disclosing transistor Mp2 ("fourth switch") that is operated by select signal SEL ("first phase signal"), and is coupled between top terminal VH0

of capacitor C0 and output terminal V_h ("coupled between the first terminal of the second capacitor and the output terminal"), Hsieh discloses a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal.

11. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1-3 of the 875 Patent is requested.

Respectfully submitted,

Dated: May 1, 2018

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CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 9,157 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 2010, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word 2010 in Times New Roman 14 point font.

Dated: May 1, 2018

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	May 1, 2018
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 6,127,875 with Micron's Exhibit List Power of Attorney Exhibits Ex. 1001 - Ex. 1005, Ex. 1007, Ex. 1009 - Ex. 1014, Ex. 1016
Persons served	Patent Owner's Address of Record: NXP USA, Inc. Law Department 6501 William Cannon Drive West TX30/OE62 Austin, TX 78735 Additional Addresses Known as Likely to Effect Service: North Star Innovations, Inc. 600 Anton Blvd., Suite 1350 Costa Mesa, CA 92626 Edward C. Flynn Cohen & Grace, LLC 105 Braunlich Drive, Suite 300 Pittsburgh, PA 15237 Robert W. Morris Eckert, Seamans, Cherin & Mellott, LLC 10 Bank St., Suite 700 White Plains, NY 10606

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