UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner

PTAB Case No.: To Be Assigned
U.S. Patent No. 5,943,274
Title: METHOD AND APPRATUS FOR AMPLIFYING A SIGNAL TO PRODUCE A LATCHED DIGITAL SIGNAL

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 5,943,274 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-.80, 42.100-.123

Mail Stop **"PATENT BOARD"**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

Page

EXHIBIT LIST

Micron Exhibit #	Description
Ex. 1001	U.S. Patent No. 5,943,274 ("274 Patent")
Ex. 1002	File History for U.S. Patent No. 5,943,274 ("274 Patent FH")
Ex. 1003	Declaration of R. Jacob Baker, Ph.D. (" Baker Decl.")
Ex. 1004	*Curriculum Vitae* of R. Jacob Baker, Ph.D.
Ex. 1005	Japanese Patent Application No. H4-170816 ("Tachibana") with certified translation
Ex. 1006	U.S. Patent No. 4,891,792 ("Hanamura")
Ex. 1007	Allen, Phillip E. and Holberg, Douglas R., *CMOS Analog Circuit Design*, Holt, Rinehart and Winston, 1987 ("Allen & Holberg")
Ex. 1008	Baker, R. Jacob et al., *CMOS Circuit Design, Layout, and Simulation*, IEEE Press, 1998 ("Baker")
Ex. 1009	Gray, Paul R. and Meyer, Robert G., *Analysis and Design of Analog Integrated Circuits, Second Edition*, John Wiley & Sons, 1977, 1984 ("Gray & Meyer")
Ex. 1010	Wang, Niantsu, *Digital MOS Integrated Circuits, Design for Applications*, Prentice Hall, 1989 ("Wang")
Ex. 1011	Douglas-Young, John, *Illustrated Encyclopedia Dictionary of Electronics*, New York: Parker Publishing Company, Inc., 1981 ("Douglas-Young")
Ex. 1012	Laplante, Phillip A. (ed.), Comprehensive Dictionary of Electrical Engineering, Florida: CRC Press, 1999 ("Laplante")
Ex. 1013	U.S. Patent No. 5,594,691 ("Bashir")
Ex. 1014	U.S. Patent No. 5,124,589 ("Shiomi")
Ex. 1015	U.S. Patent No. 4,916,670 ("Suzuki")
Ex. 1016	U.S. Patent No. 5,455,803 ("Kodama")
Ex. 1017	U.S. Patent No. 5,083,296 ("Hara")
Ex. 1018	U.S. Patent No. 5,404,338 ("Murai")
Ex. 1019	Prince, Betty, "Semiconductor Memories, *A Handbook of Design, Manufacture, and Application, 2nd Edition*, John Wiley & Sons, 1983, 1991 ("Prince")
Ex. 1020	U.S. Patent No. 6,392,948 ("Lee")
Ex. 1021	U.S. Patent No. 5,592,415 ("Kato")
Ex. 1022	U.S. Patent No. 4,272,834 ("Noguchi")
Ex. 1023	U.S. Patent No. 4,760,561 ("Yamamoto")
Ex. 1024	U.S. Patent No. 5,781,469 ("Pathak")

Micron Exhibit #	Description
Ex. 1025	Sclater, Neil and Markus, John, *McGraw-Hill Electronics Dictionary, 6th Edition*, R.R. Donnelley & Sons Company, 1997 ("McGraw-Hill")
Ex. 1026	U.S. Patent No. 4,720,686 ("Westwick")
Ex. 1027	EP Patent Application No. 0 345 621 A2 ("Meadows")

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123, Micron Technology, Inc. ("Petitioner" or "Micron") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-12, 14-16, and 20-23 of U.S. Patent No. 5,943,274, titled "Method and Apparatus for Amplifying a Signal to Produce a Latched Digital Signal" (Ex. 1001, the "274 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a)

Petitioner certifies that the 274 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 274 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3, 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang Registration No. 73,604 (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Brian Chang Registration No. 74,301 (brian.chang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3936; F: 650-802-3100

Lead Counsel	**Back-Up Counsel**
	Jared Bobrow (jared.bobrow@weil.com) *Pro Hac Vice Application To Be Submitted* Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3034; F: 650-802-3100

Petitioner consents to service by electronic mail at the following addresses: jason.lang@weil.com, brian.chang@weil.com, jared.bobrow@weil.com, and Micron.Northstar.IPR@weil.com. Pursuant to 37 C.F.R. § 42.10(b), Petitioner's Power of Attorney is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1)

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2)

North Star Innovations, Inc. ("Patent Owner" or "North Star") has asserted the 274 Patent and U.S. Patent Nos. 6,127,875 (the "875 Patent"), 7,171,526 (the "526 Patent"), and 6,465,743 (the "743 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *North Star Innovations, Inc. v.*

Micron Technology, Inc., 17-cv-506-LPS-CJB (D. Del.) ("Co-Pending Litigation"). North Star also has asserted the 875 Patent, the 274 Patent, U.S. Patent No. 6,917,555 (the "555 Patent"), and U.S. Patent No. 6,101,145 (the "145 Patent") in the following action: *North Star Innovations, Inc. v. Kingston Technology Co., Inc.*, 8:17-cv-1833 (C.D. Cal.) (Compliant filed on October 20, 2017).

In addition to this Petition, Petitioner is filing an additional two petitions for *inter partes* review of U.S. Patent No. 6,127,875, two petitions for *inter partes* review of U.S. Patent No. 7,171,526, and one petition for *inter partes* review of U.S. Patent No. 6,465,743.[1]

The 274 Patent does not claim priority to any foreign or U.S. patent application.

2.5. Fee for Inter Partes Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 601788.

2.6. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence address of record for the 274 Patent is attached.

[1] These petitions will be filed before May 3, 2018.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (37 C.F.R. § 42.104(B))

Ground #1: Claims 1-3, 8-12, 14-16, 20, and 21 of the 274 Patent are invalid under (pre-AIA) 35 U.S.C. § 102(b) on the ground that they are anticipated by Japanese Patent Application No. H4-170816 to Tachibana *et al.*, entitled "Semiconductor integrated circuit," filed on November 5, 1990 and published by the Japanese Patent Office on June 18, 1992 (Ex. 1005, "Tachibana")[2]. The 274 Patent was filed on February 2, 1998 with no claim to an earlier effective filing date, so Tachibana is prior art under at least 35 U.S.C. §§ 102(a) and (b).

Ground #2: Claims 4-7 of the 274 Patent are invalid under (pre-AIA) 35 U.S.C. § 103 on the ground that they are obvious over Tachibana in view of the knowledge of a person of ordinary skill in the art.

Ground #3: Claims 22 and 23 of the 274 Patent are invalid under (pre-AIA) 35 U.S.C. § 103 on the ground that they are obvious over Tachibana in view of U.S. Patent No. 4,891,792 to Hanamura, et al., entitled "Static Type Semiconductor Memory With Multi-Stage Sense Amplifier," filed on July 6, 1988 and issued on January 2, 1990 (Ex. 1006, "Hanamura"). Hanamura is prior art under at least §§ 102(a) and (b).

[2] All citations to Tachibana are to the original publication page numbering.

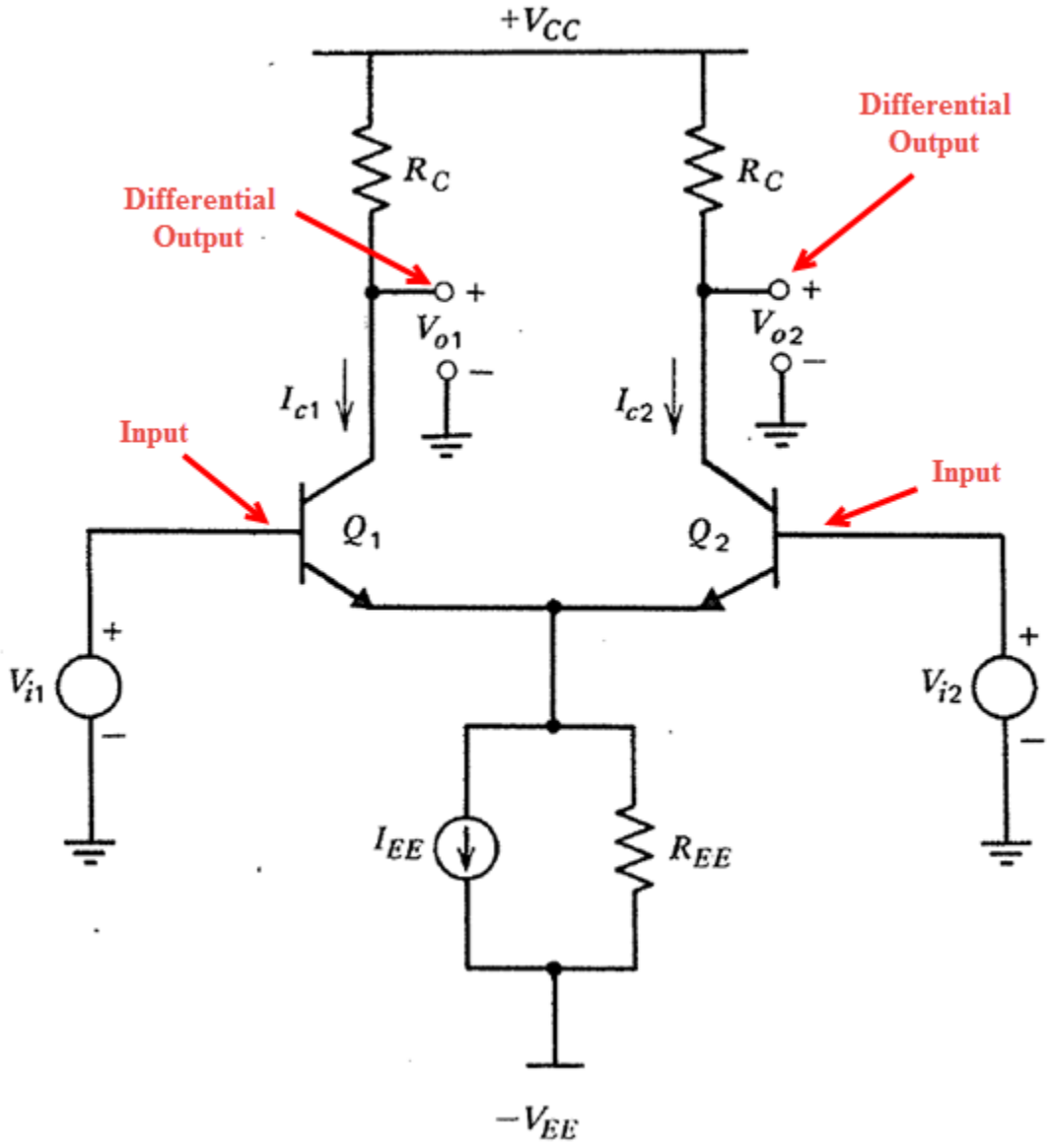
Neither Tachibana nor Hanamura was considered by the Examiner during prosecution of the 274 Patent.

4. BACKGROUND OF TECHNOLOGY

The 274 Patent relates generally to output stages for memory integrated circuits. At the time that the 274 Patent was filed in 1999, it was known and common in the art for semiconductor memories to include an output stage between the sense amplifiers of the memory cell array (which the 274 Patent calls a bit cell array) and the data I/O pins. *See, e.g.*, Ex. 1001, Fig. 1; 1:23-25; Ex. 1005, Fig. 10; Ex. 1003, ¶32. The purpose of the output stage is to drive the external load of the memory device. Ex. 1007, p. 10. In the prior art, the output stage typically included a differential amplifier, which is a type of circuit that amplifies the difference between two input voltages. Ex. 1001, 1:2-28; Ex. 1007, p. 26; Ex. 1008, p. 30, 32; Ex. 1003, ¶34. The output stage also commonly included a latching circuit to store the amplified output signals from the differential amplifier. Ex. 1001, 1:29-33. This was done to ensure a consistent output logic level on the I/O pins while the differential amplifier is detecting the next data value. *Id.*; Ex. 1003, ¶34.

4.1. Differential Amplifiers

As discussed above, a differential amplifier accepts two inputs and amplifies the voltage difference between the two inputs. An example of a basic prior art differential amplifier circuit is shown below:

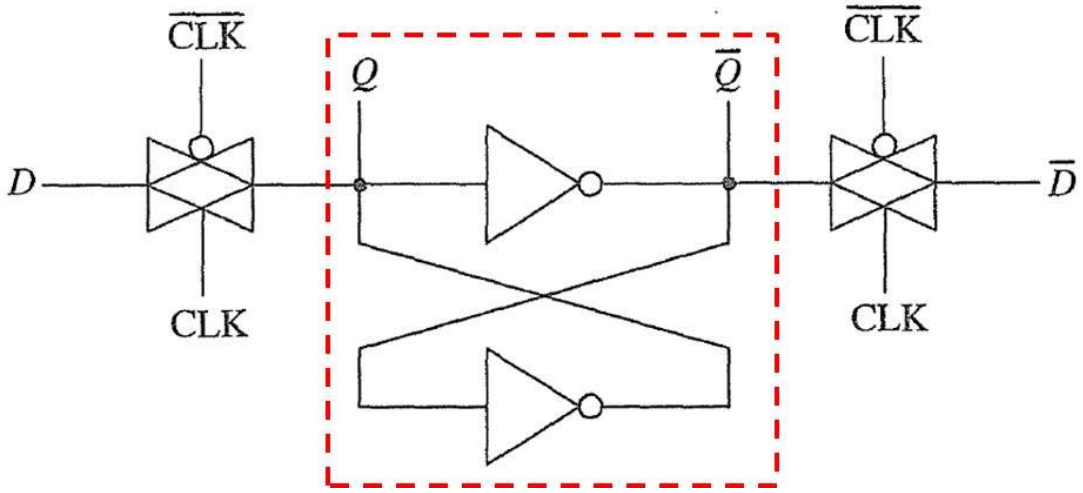


Ex. 1009, Fig. 3.26 (p. 10).

In the figure above, bipolar transistors Q_1 and Q_2 form a transistor pair that amplifies the difference between the inputs V_{i1} and V_{i2}. When V_{i1} is applied to transistor Q_1, the voltage drops across resistor R_C that is connected to Q_1, causing an output to appear at output terminal V_{o1}. At the same time, the current flow through transistor Q_1 causes a voltage drop across resistor R_{EE}. Because both transistors Q_1 and Q_2 are connected to resistor R_{EE}, this voltage drop causes the current flow through transistor Q_2 to decrease, which in turn causes an output to appear at output terminal V_{o2}. The differential outputs V_{o1} and V_{o2} are inverted with respect to one another (*i.e.*, equal and opposite), and can be used as differential inputs for subsequent circuit components or, if only a single output is needed, the other can be discarded. Ex. 1003, ¶¶36-37.

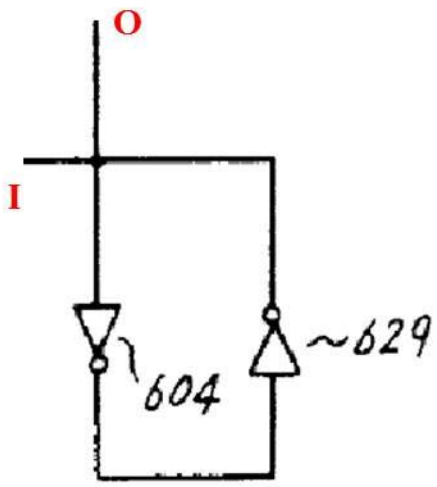
4.2. Latch Circuits

A latch is a circuit with two stable states that is used to store state information. Ex. 1010, pp. 21-22. Latches were commonly used in the prior art to form memory elements, and are still used in this way in the present day. *Id.*; Ex. 1003, ¶38. The figure below illustrates a cross-coupled pair of inverters forming a latch that was known in the prior art. *See* Ex. 1008, pp. 26-27 ("The cross-coupled connection of inverters is sometimes referred to as a latch").



In the latch above, the D input is connected to Q, and the $\overline{D}$ input is connected to $\overline{Q}$. In this context, a horizontal bar over a signal letter indicates the inverse of the signal (*i.e.*, if D is 1, $\overline{D}$ is 0 and vice versa). Additionally, the outputs of the two inverters are cross-coupled to one another, which allows the circuit to maintain the most recent input value. For example, if D is input with a value of 1, the output of the top inverter is 0, which is coupled to the input of the bottom inverter. The bottom inverter then outputs a 1, which is coupled to the input of the top inverter to form a repeating loop. Thus, even when the transmission gates are non-conducting, the cross-coupled inverter pair will latch and "remember" the previous value of D until a new value is passed through the transmission gates. *See* Ex. 1008, p. 26; Ex. 1003, ¶¶39-40.

The Tachibana reference, which is discussed in greater detail herein, discloses a similar latch comprised of two inverters:



Ex. 1005, Fig. 15 (excerpted and annotated)

In the figure above, the input to the latch has been annotated with a red letter "I," and the output with a red letter "O." In this basic latch circuit, the input value of I passes through inverter 604, where it is inverted, *i.e.*, an input value of 1 outputs from inverter 604 as 0, and an input value of 0 outputs from inverter 604 as 1. The output of inverter 604 then inputs to inverter 629, where it is inverted again. As a result, the output of inverter 629 always equals the original input value of I. The output from inverter 629 (which has the same value as the original input) is output from the latch on O. Ex. 1003, ¶¶41-42.

If the input I stops providing an input value (*e.g.*, if the circuit stage preceding the latch stops conducting current), the previous value of I is maintained within the latch circuit because the output of inverter 629, which carries the previous value of I, is also shorted to the input of inverter 604, thus maintaining a

loop even in the absence of input on I. In contrast, if the value on I *changes*, then the value stored in the latch also changes accordingly. Ex. 1003, ¶43.

5. OVERVIEW OF THE 274 PATENT

The claims of the 274 Patent are directed specifically to providing a "clock-free" latch for a memory output stage. According to the specification of the 274 Patent, prior art output stages purportedly used two clock signals: one signal to clock the differential amplifier portion, and one signal to clock the latch portion. Ex. 1001, 1:33-37. The 274 Patent alleges that this caused problems because the timing relationship between the two clock signals could not be "consistently controlled due to manufacturing process variations, temperature variations, power supply voltage variations, etc." *Id*., 1:37-40. The purported solution to this problem, according to the 274 Patent, was to use an output stage "that does not require two or more clocks." *Id*., 1:40-44. In the claims of the 274 Patent, this requirement of not using two or more clocks is reflected in limitations requiring a "clock-free latch." Ex. 1003, ¶44. Claim 1 is reproduced below as illustrative, with the clock-free latch limitation underlined.

> 1. An apparatus for use as an output stage of a memory device, the apparatus comprising:
>
> a timing circuit;
>
> a differential amplifier responsive to the timing circuit;

an impedance control circuit;

a level converter responsive to the differential amplifier and the impedance control circuit; and

a clock-free latch responsive to the level converter.

6. 274 PATENT PROSECUTION HISTORY

The application that ultimately issued as the 274 Patent was filed on February 2, 1998, with original claims 1-24. The Examiner issued a first office action Notice of Allowability on March 5, 1999, with an examiner's amendment making non-substantive revisions to the specification. The Examiner's reasons for allowance stated that the prior art of record purportedly "fails to show an apparatus and a method for use as an output stage of a memory device, utilizing a timing circuit, a differential amplifier responsive to the timing circuit, an impedance control circuit, a level converter responsive to the differential amplifier and the impedance control circuit, and a clock-free latch responsive to a level converter, as represented in claims 1, 14, 20, and 21." Neither the Tachibana reference nor the Hanamura reference that are relied upon in this Petition was part of the art of record during prosecution, which consisted of only five U.S. patents.

7. CLAIM CONSTRUCTION

7.1. Applicable Law

The 274 Patent expired on February 2, 2018. Accordingly, Petitioner has applied the claim construction principles of *Phillips* rather than the broadest reasonable interpretation standard applicable to non-expired patents. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012; *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (*en banc*).

7.2. Construction of Claim Terms

All claim terms have been accorded their plain and ordinary meaning as understood by a person having ordinary skill in the art ("POSA") and consistent with the intrinsic record.[3]

[3] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 274 Patent for failure to satisfy the requirements of 35 U.S.C. § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this petition shall be construed as a waiver of such challenge, or agreement that the requirements of § 112 are met for any claim of the 274 Patent.

8. PERSON OF ORDINARY SKILL IN THE ART

A POSA with respect to the technology described in the 274 Patent would be a person with at least a Bachelor of Science degree in electrical engineering or a closely related field, along with at least 4-5 years of experience in the design of integrated circuits. An individual with an advanced degree in a relevant field would require less experience in the design of integrated circuits. Ex. 1003, ¶¶26-30.

9. DESCRIPTION OF THE PRIOR ART

9.1. Japanese Patent Pub. H4-170816 ("Tachibana")[4]

Tachibana discloses a "low-power-consumption ECL gate circuit and buffer circuit" for semiconductor devices. Ex. 1005, p. 110. Tachibana recognized that prior art devices used an ECL (emitter-coupled logic) circuit to provide high-speed output buffers. *Id*. In order to drive the load capacitance of the output terminals in such circuits at high speeds, a large steady-state current was required. *Id*. As advances in integrated circuits created a demand for multi-bit output capabilities, however, the steady-state current required to drive the output buffer circuit also increased. *Id*. Tachibana discloses, for example, that a typical prior art ECL

[4] Tachibana was published on June 18, 1992 and is therefore prior art at least under § 102(b). *See* Ex. 1005, p. 109.

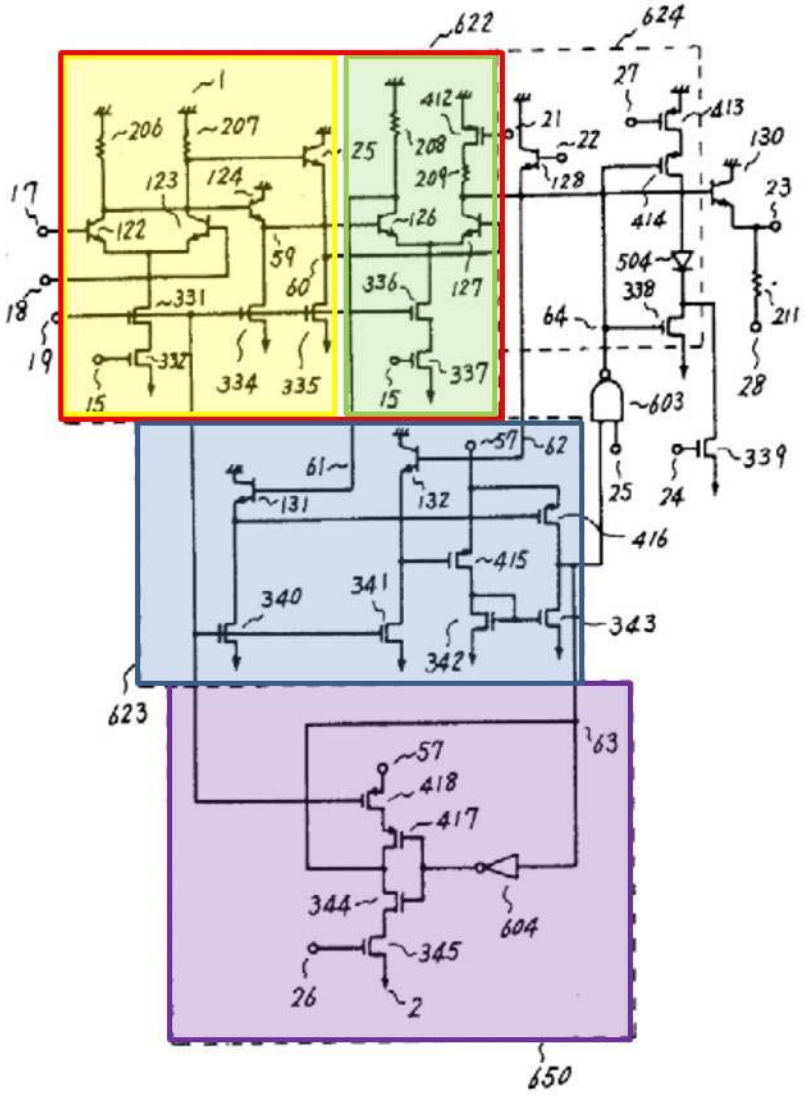
output buffer circuit required around 20mW of power to output a single bit of data, meaning that a 64 bit output from the same circuit would have required around 1.3W of power, "which is roughly 50% of the power of the entire memory." *Id*. To address this problem, Tachibana discloses various embodiments of an output buffer circuit that utilizes a latch circuit comprised of a differential amplifier and a MOS transistor, in which the differential amplifier is not supplied with current when the output data is being held in the latch, thereby reducing the power consumption of the output buffer circuit. *Id*.; Ex. 1003, ¶51.

Tachibana discloses multiple different implementations of its ECL buffer circuit. A first embodiment is shown in Figure 1, below.

Tachibana's Figure 1 embodiment uses a two-stage differential amplifier 622 (in red). Ex. 1005, p. 111. The first stage (in yellow) is comprised of resistors 206 and 207, bipolar transistors 122-125, and NMOS transistors 331-335. *Id*. The second stage (in green) has a similar structure comprised of resistors 208 and 209, bipolar transistors 126 and 127, NMOS transistors 336 and 337, and PMOS transistor 412. *Id*. As shown below, NMOS transistors 331 and 336 control current flow to the first and second stages, respectively, of differential amplifier 622. Outputs 61 and 62 of the second differential amplifier stage are inputs into ECL-MOS level conversion circuit 623 (in blue). Output 63 of the ECL-MOS

level conversion circuit is an input into latch circuit 650 (in purple). Ex. 1003, ¶¶52-53.

FIG. 1



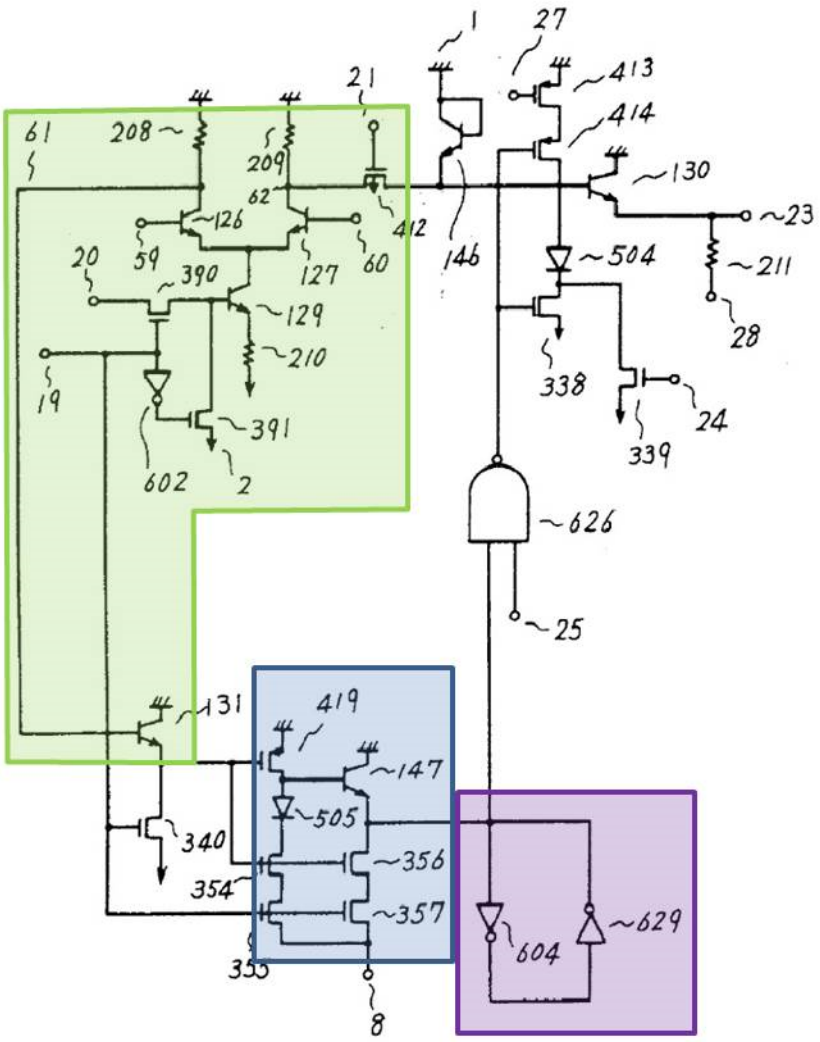
Tachibana teaches that when clock signal 19 is at low level, NMOS transistors 331 and 336 are both non-conducting. Ex. 1005, p. 111. As a result, current does not flow to the two differential amplifier stages when clock signal 19 is low. *Id.*; Ex. 1003, ¶¶54.

As shown in Figure 2 of Tachibana, when clock signal 19 is low, clock signal 26 is high. Ex. 1005, Fig. 2. Clock signals 19 and 26 control PMOS transistor 418 and NMOS transistor 345 of latch circuit 650, and in particular, PMOS transistor 418 and NMOS transistor 345 are both conducting when clock signal 26 is high (and clock signal 19 is low). *Id*., p. 112. As a result, the latch circuit 650 is operational when clock signal 26 is high (and clock signal 19 is low), causing the latch circuit 650 to "remember[] that the terminal 63 was at low-level potential during the previous read," *i.e.,* output the data value that was read in the previous read cycle, which in this example is a low data value ("0"). *Id*.; Ex. 1003, ¶¶55-56.

Thus, when data is in the "held" state (*i.e.*, outputting a previously latched value), the output buffer depicted in Tachibana's Figure 1 lowers power consumption by setting clock signal 19 to low and clock signal 26 to high, thereby deactivating the differential amplifier and causing the latch circuit 650 to output the previously read data value. Ex. 1003, ¶57. Although this implementation of Tachibana's circuit uses a separate clock signal (26) to control the latch circuit 650, Tachibana further discloses embodiments in which the latch circuit is controlled by the output of an ECL-MOS level conversion circuit, rather than a clock signal. Ex. 1003, ¶58.

Figure 15, below, provides an example of one such embodiment.

FIG. 15

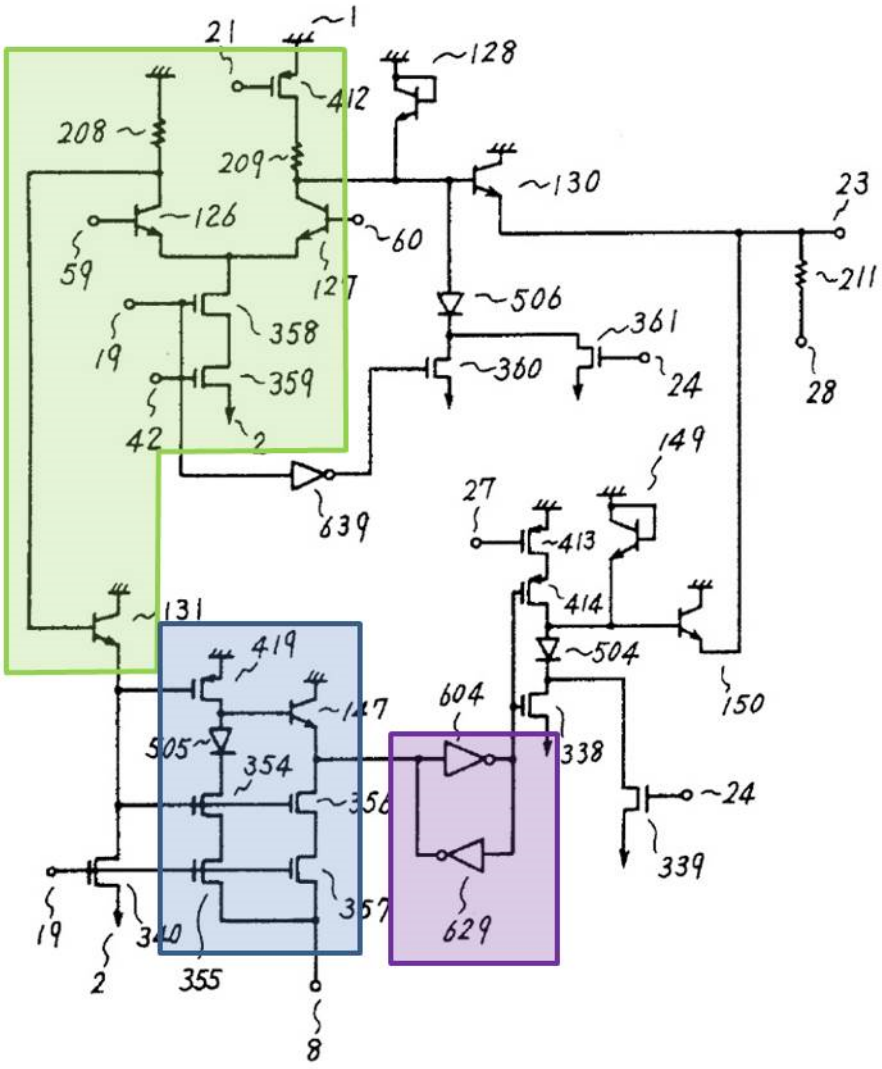


The embodiment of Figure 15 uses a single-stage differential amplifier (in green) that is similar in structure to the second stage of Figure 1's differential amplifier 622, comprised of resistors 208 and 209, bipolar transistors 126 and 127, bipolar transistor 131, and PMOS transistor 412. Ex. 1003, ¶¶58-59. Additionally, the differential amplifier in Figure 15 uses a bipolar transistor 129, resistor 210, NMOS transistors 390 and 391, and inverter circuit 602 in place of the NMOS

transistors 336 and 337 used in Figure 1. Ex. 1005, p. 119. The embodiment of Figure 15 also replaces Figure 1's ECL-MOS level conversion circuit 623 with a circuit, having "the same operation as" the ECL-MOS level conversion circuit 623, comprised of a bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354-357 (in blue). *Id*. Inverter circuits 604 and 629 (in purple) are used as a latch circuit in place of Figure 1's latch circuit 650. *Id*. As can be seen in Figure 15, the only input into the latch in this embodiment (inverters 604 and 629) is the output signal of the ECL-MOS level conversion circuit; unlike in the Figure 1 embodiment, the latch is clock-free and does not respond to a separate clock signal 26. Ex. 1003, ¶59.

Figure 17, below, provides an additional embodiment similar to Figure 15. As in Figure 15, the Figure 17 embodiment uses inverters 604 and 629 as a clock-free latch circuit (in purple), and they respond only to the output of the ECL-MOS level conversion circuit comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354-357 (in blue). Ex. 1003, ¶¶60-61.

FIG. 17

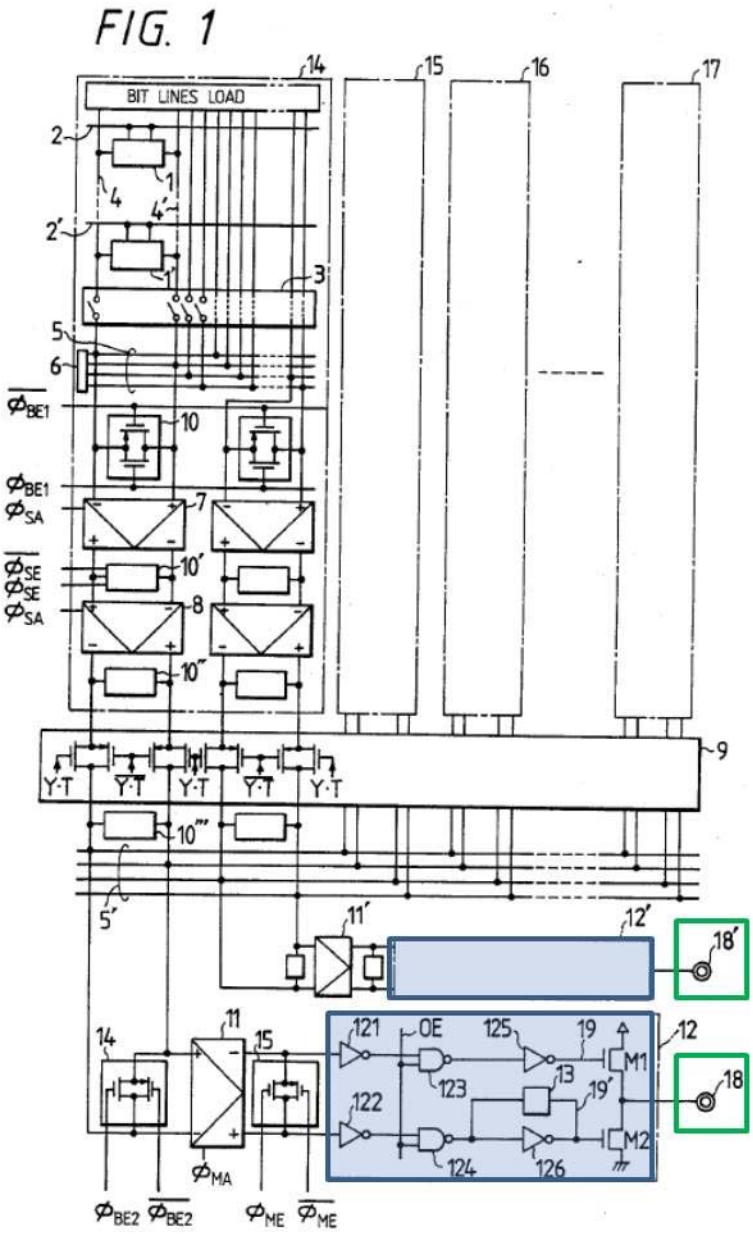


9.2. U.S. Patent No. 4,891,792 ("Hanamura")[5]

Hanamura discloses a semiconductor memory device comprised of four memory arrays 14, 15, 16, and 17 that are coupled together by a multiplexer 9 and

[5] Hanamura was filed on July 6, 1988 and issued on January 2, 1990, and is therefore prior art under at least §§102(a) and §102(b). *See* Ex. 1006.

a common data bus line pair 5'. Of particular relevance to this Petition, Hanamura discloses that each memory array has a plurality of data output buffers and data outputs; memory array 14, for example, is coupled to data output buffer 12, which outputs on data output 18, as well as data output buffer 12', which outputs on data output 18'. Ex. 1003, ¶63.



Also, Hanamura discloses that the memory cells (1, 1') and sense amplifiers (7, 8) in memory array 14 are coupled to a bit line load circuit, which is labeled "Bit Lines Load" at the top of the figure above. Ex. 1003, ¶64.

10. GROUND #1: CLAIMS 1-3, 8-12, 14-16, 20, AND 21 OF THE 274 PATENT ARE UNPATENTABLE AS ANTICIPATED BY TACHIBANA

10.1. Tachibana Anticipates Claim 1

10.1.1. [1.P] "An apparatus for use as an output stage of a memory device, the apparatus comprising:"

To the extent that the preamble is a limitation, Tachibana discloses this limitation.

Tachibana, in Figure 10, discloses a BiCMOS memory, which is a memory device. Ex. 1005, p. 117; Fig. 10. As shown in Figure 10, the BiCMOS memory includes an output buffer circuit 608, which is an output stage of the BiCMOS memory. *Id*., p. 117; Fig. 10. Tachibana discloses that output buffer circuit 608 is the output buffer circuit of Figure 1. *Id*., p. 117. Further, Tachibana also discloses that Figures 15 and 17 are circuits that provide "the same operation as" the circuit in Figure 1. *Id*., pp. 119-120. Thus, Tachibana discloses that the circuits in Figures 15 and 17 are also output stages for a BiCMOS memory. Ex. 1003, A1-A3.

Accordingly, Tachibana discloses an apparatus for use as an output stage (the circuit of Figures 15 and 17) of a memory device (the BiCMOS memory of Figure 10).

10.1.2. [1.1] "a timing circuit;"

Tachibana discloses this limitation. Tachibana discloses terminals 19, 21, and 27 that are inputs into the circuits shown in Figures 15 and 17.

FIG. 15

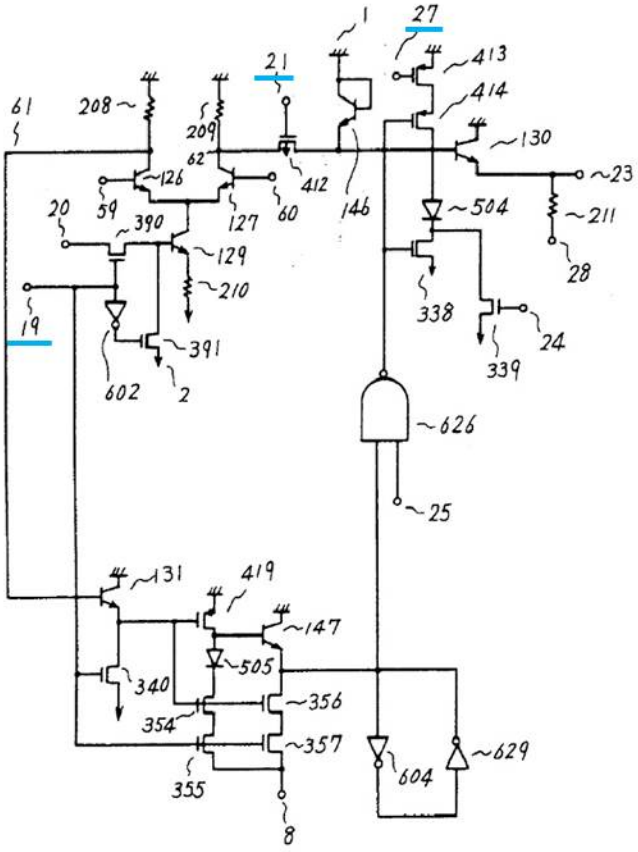
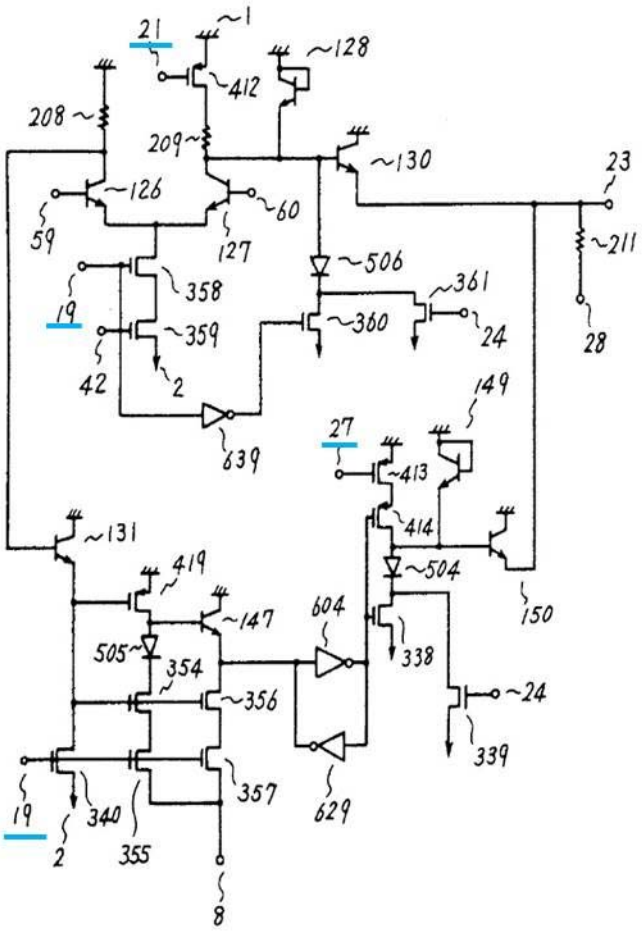
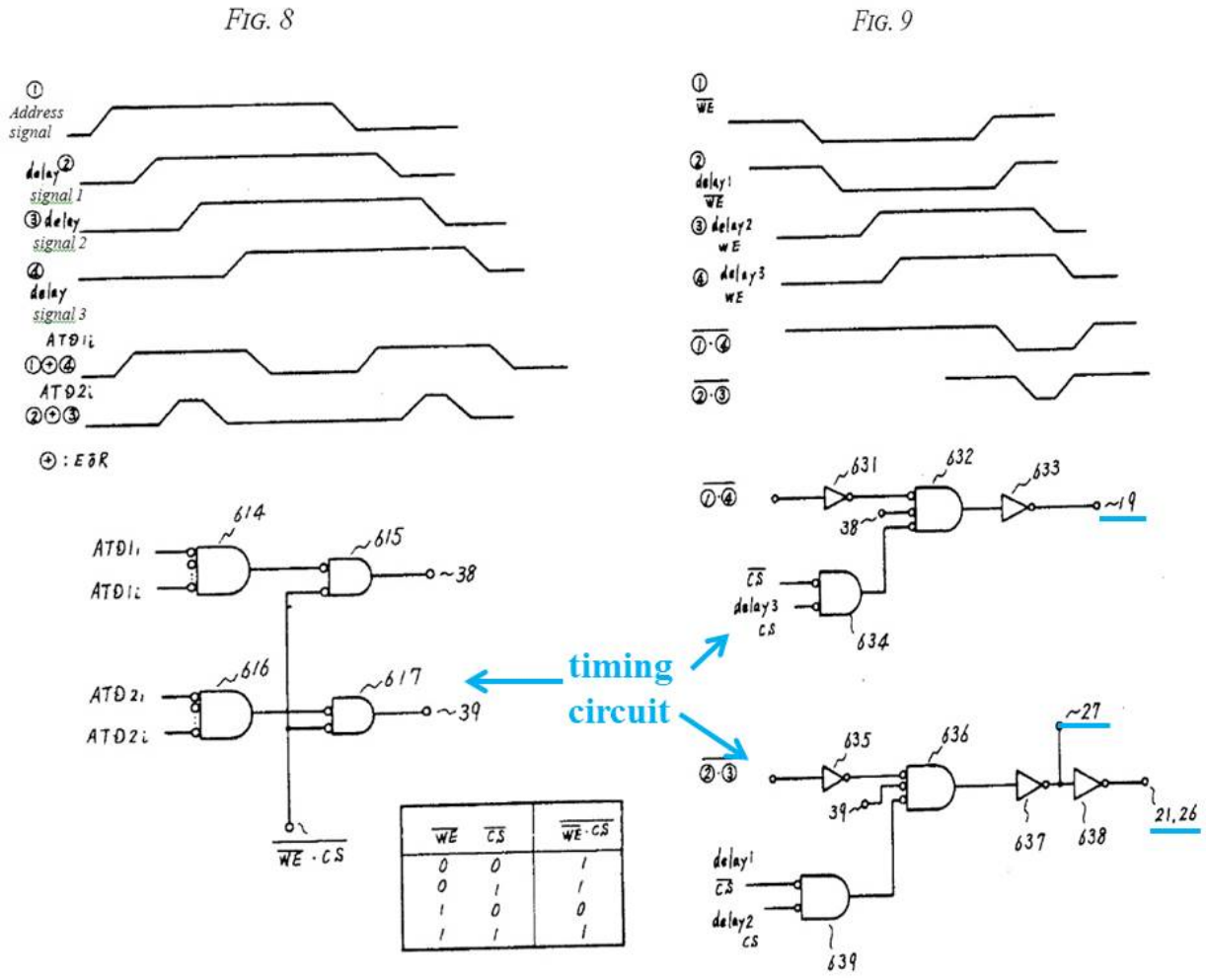


FIG. 17



Tachibana expressly discloses that "19, 21, 24, 26, 27 are clock signal terminals." Ex. 1005, p. 111. Although this description is provided in connection with Figure 1, Tachibana explains that in Figures 15 and 17, elements and terminals "with the same number" as in Figure 1 "correspond to the element with the same number in the circuit" of Figure 1. *Id.*, pp. 119-120. Thus, the terminals 19, 21, and 27 in Figures 15 and 17 are clock signal terminals. Ex. 1003, A3-A7.

Tachibana further discloses, in Figures 8 and 9, a circuit (depicted in three sections) that generates the signals for terminals 19, 21, and 27:



WE	CS	WE · CS
0	0	1
0	1	1
1	0	0
1	1	1

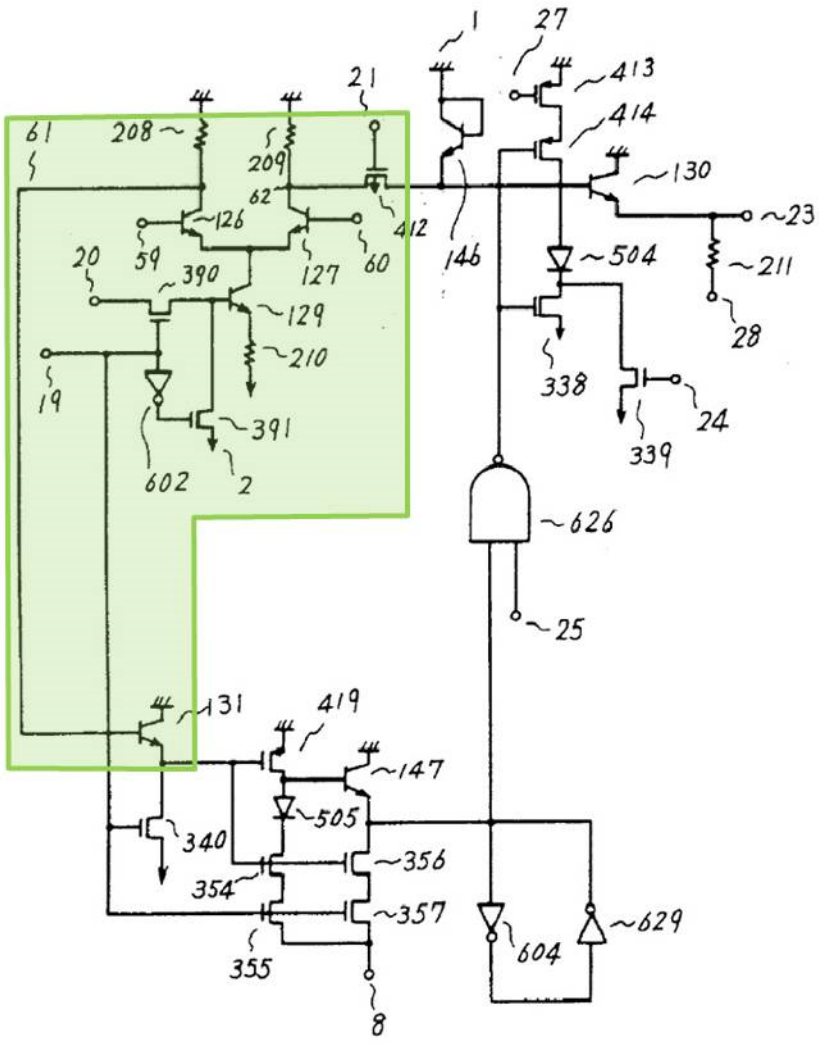
Because terminals 19, 21, and 27 are clock signal terminals, a POSA would have understood that the signals transmitted on those terminals are clock signals, and the circuits used to generate them are timing circuits. Ex. 1003, A3-A7. This is consistent with how a POSA would have understood the term "timing circuit" as used in the 274 Patent, which describes, for example, that "timing circuit 104 is used to provide two versions of clock signal 78." Ex. 1001, 5:26-27; Ex. 1003, A6-A7.

Accordingly, Tachibana discloses a timing circuit (the circuit in Figures 8 and 9).

10.1.3. [1.2] "a differential amplifier responsive to the timing circuit;"

Tachibana discloses this limitation. Tachibana discloses, in Figure 15, a differential amplifier comprised of resistors 208 and 209, bipolar transistors 126 and 127, PMOS transistor 412, bipolar transistor 129, resistor 210, NMOS transistors 390 and 391, inverter circuit 602, and bipolar transistor 131.

FIG. 15

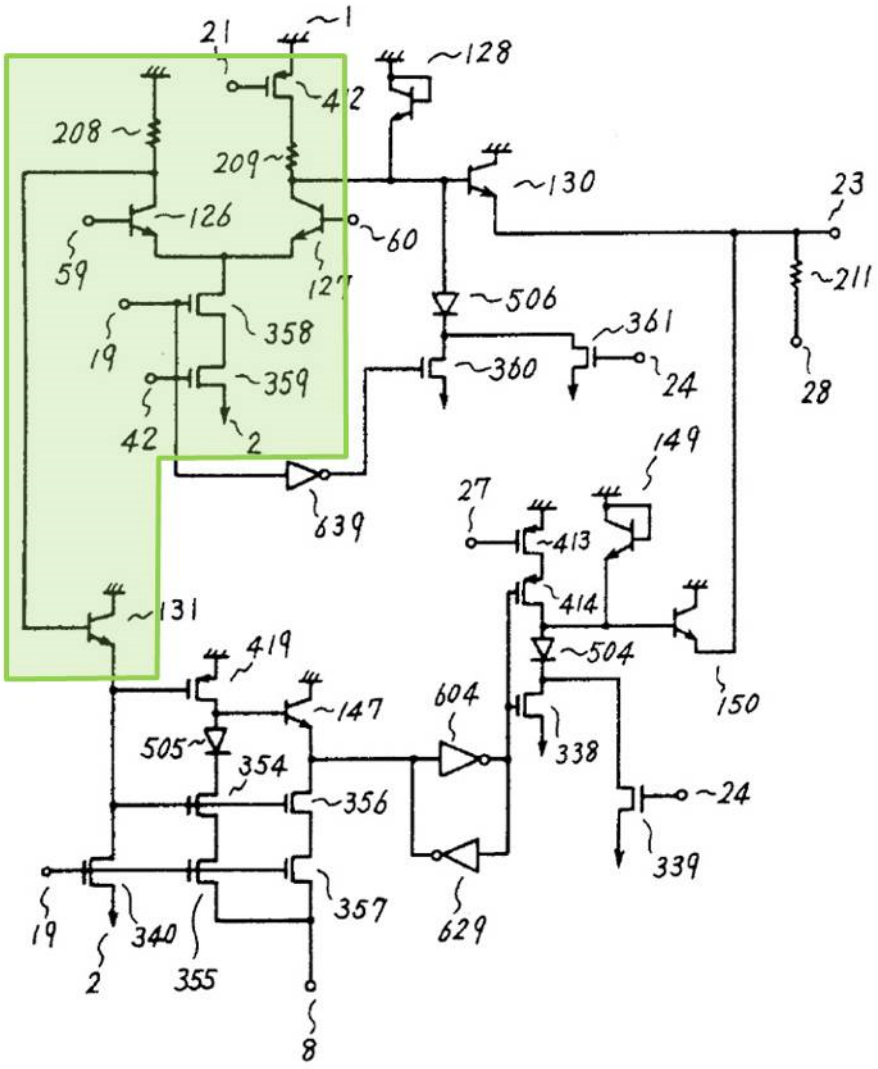


While Tachibana's description of Figure 15 does not expressly describe this portion of the circuit as a "differential amplifier," Tachibana expressly states that the circuit of Figure 15 "achieves the same operation as the circuit in FIG. 1," that "[e]lements and terminals with the same number as those of the circuit in FIG. 1 correspond to the element with the same number in the circuit in FIG.1," and that "the operation is essentially the same" as that of the circuit in Figure 1. Ex. 1005,

p. 119. Tachibana's description of Figure 1 expressly discloses "a differential amplifier comprised of resistors 208, 209, bipolar transistors 126, 127, NMOS transistors 336, 337, and PMOS transistor 412." *Id*., p. 111. Tachibana further expressly states that in the circuit of Figure 15, "NMOS transistors 336, 337 of the current source in FIG. 1 were substituted with a bipolar transistor 129, resistor 210, NMOS transistors 390, 391, and inverter circuit 620." *Id*., p. 119. A POSA would therefore have understood Tachibana to disclose that in Figure 15, resistors 208 and 209, bipolar transistors 126 and 127, PMOS transistor 412, bipolar transistor 129, bipolar transistor 131, resistor 210, NMOS transistors 390 and 391, and inverter circuit 602 comprise a differential amplifier. Ex. 1003, A7-A10, A11-A13.

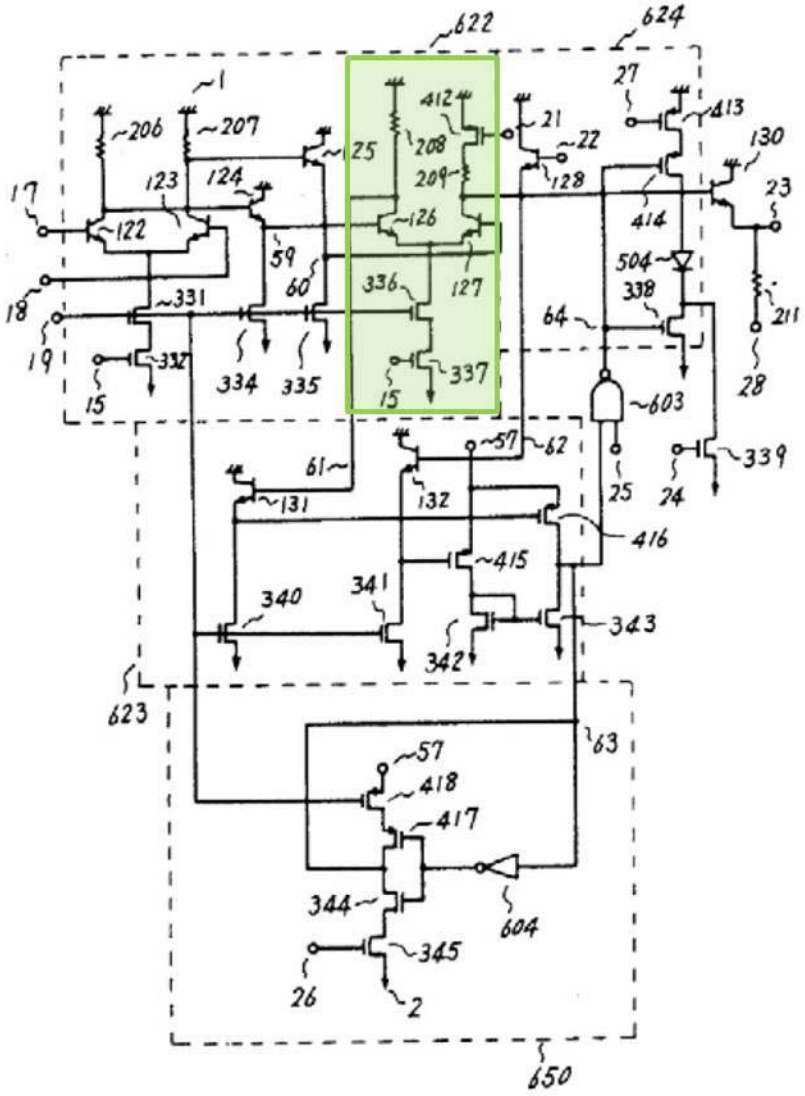
Tachibana also discloses a similar differential amplifier in Figure 17, comprised of resistors 208 and 209, bipolar transistors 126 and 127, NMOS transistors 358 and 359, and PMOS transistor 412. Ex. 1003, A10-A11.

FIG. 17



As can be seen by comparison with Figure 1, below, the portion of Figure 17 highlighted above is substantially similar to Figure 1's "differential amplifier comprised of resistors 208, 209, bipolar transistors 126, 127, NMOS transistors 336, 337, and PMOS transistor 412," with the NMOS transistors being numbered 358 and 359 instead of 336 and 337:

FIG. 1



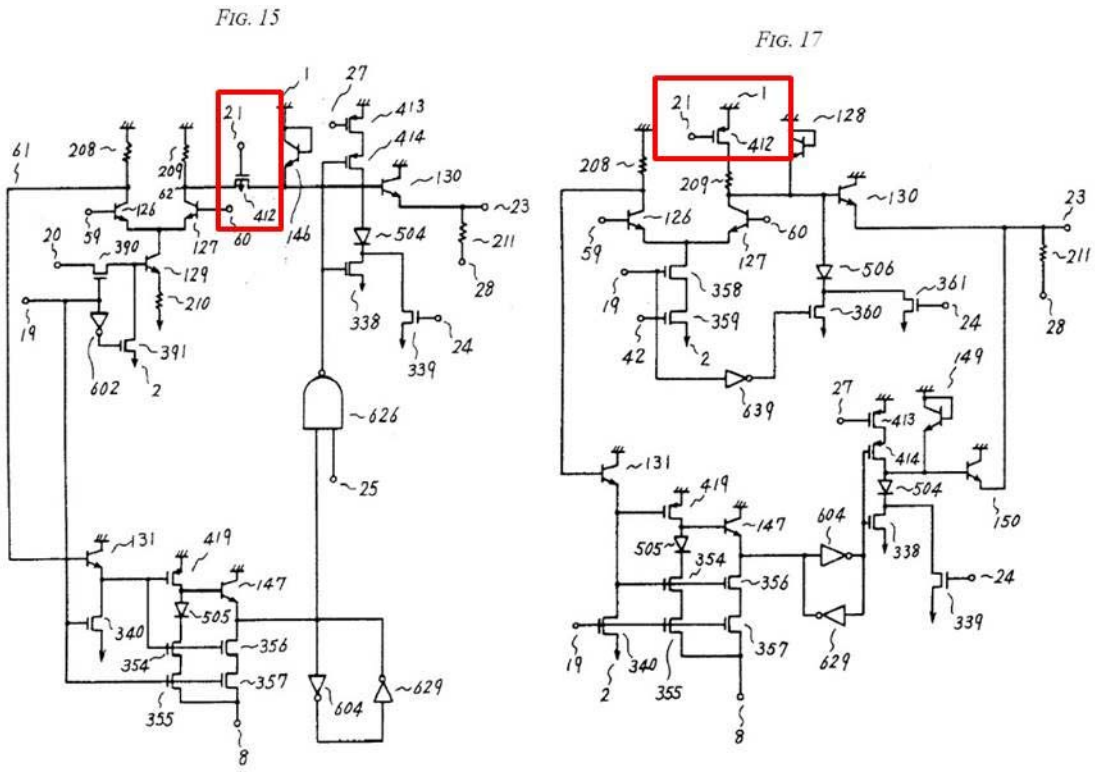
Tachibana further discloses that the respective differential amplifiers in Figures 15 and 17 are responsive to the circuit depicted in Figures 8 and 9. In particular, Tachibana discloses that the level of the signal on terminal 19, which is generated by the circuit in Figures 8 and 9, affects the level of output signals 61 and 62 of the differential amplifiers in Figures 15 and 17. When 19 is at low-level potential, "the potential of terminal 61 attains the GND terminal's potential of 0

V." Ex. 1005, p. 111. When 19 is at high-level potential, "the potential of terminal 60 is now (2ns in FIG. 2) higher than the potential of terminal 59," which causes "the potential of terminal 62 to attain the low level and the potential of terminal 61 to attain the high level." *Id*., p. 113. As shown in Figure 2, the difference in value between the potentials of terminals 61 and 62 is larger than the difference in value between the potentials of terminal 59 and 60 when 19 is at high-level potential, indicating that when 19 is at high-level potential, the differential amplifier is amplifying the difference between its two inputs (terminals 59 and 60). *Id*., Fig. 2. Tachibana therefore discloses that the respective differential amplifiers in Figures 15 and 17 are responsive to the circuit in Figures 8 and 9. Ex. 1003, A13-14.

Accordingly, Tachibana discloses a differential amplifier (in Figures 15 and 17, comprised of the components discussed above) responsive to the timing circuit (the circuit in Figures 8 and 9).

10.1.4. [1.3] "an impedance control circuit;"

Tachibana discloses this limitation. Tachibana discloses a PMOS transistor 412 in the embodiments of Figures 15 and 17, as shown below:



In connection with Figure 15, Tachibana discloses that PMOS transistor 412 controls the output impedance of the differential amplifier by setting it to "high impedance" when PMOS transistor 412 is non-conducting. Ex. 1005, p. 119. Further, Tachibana expressly states that in Figures 15 and 17, elements and terminals identified by the same reference numeral "correspond to the element with the same number" in Figure 1. *Id.*, pp. 119-120. In connection with Figure 1, Tachibana discloses that "PMOS transistor 412 is an element that serves to set the impedance of output element 62 of differential amplification circuit 622 to high impedance in the data held state. In the data held state, PMOS transistor 412 is in the non-conducting state, so setting the output impedance of output terminal 62 of differential amplification circuit 622 to high impedance causes differential

amplification circuit 622 to cease to affect the potential of terminal 62." *Id*., p. 112. PMOS transistor 412 is therefore an impedance control circuit because it is a circuit that controls the output impedance of the differential amplifier[6]. Ex. 1003, A14-A19.

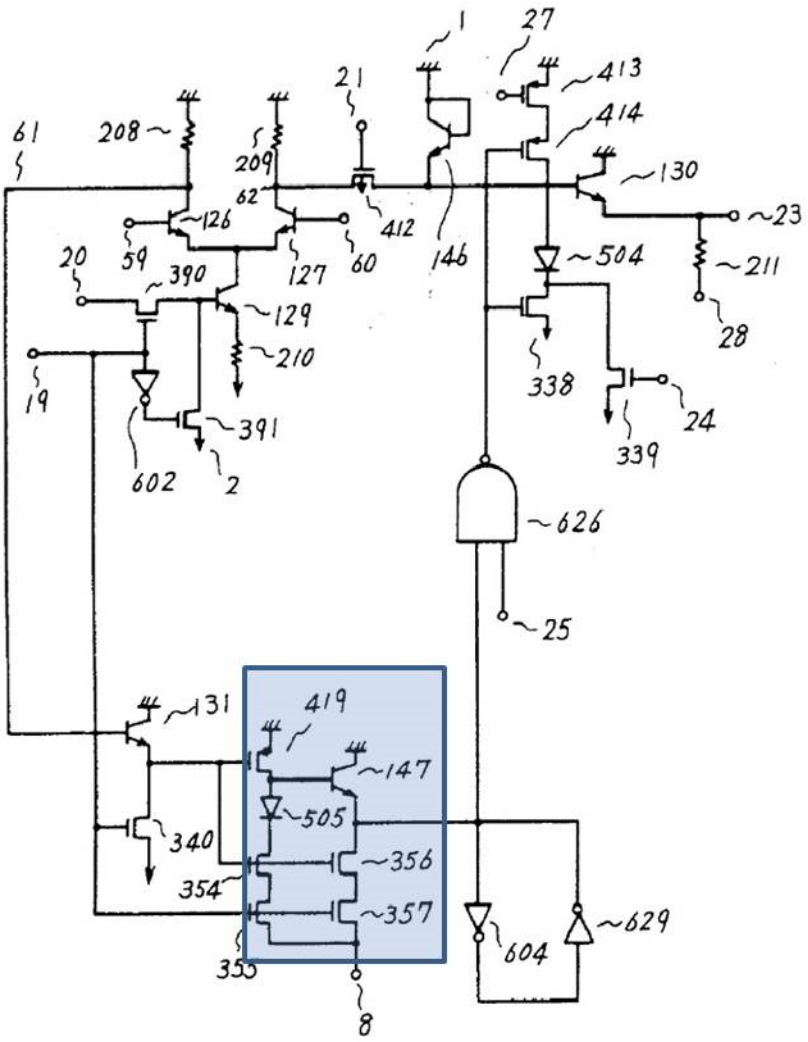
Accordingly, Tachibana discloses an impedance control circuit (PMOS transistor 412).

10.1.5. [1.4] "a level converter responsive to the differential amplifier and the impedance control circuit; and"

Tachibana discloses this limitation. Tachibana discloses a circuit in Figure 15 comprising a bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357, as shown below:

[6] Additionally, transistor 340 in Figures 15 and 17 is an impedance control circuit because it controls the impedance of the ECL-MOS level conversion circuit. Ex. 1003, A15.

FIG. 15



See also Ex. 1005, p. 119. Tachibana discloses that this circuit is "used instead of the ECL-MOS level conversion circuit 623 for clock control in FIG. 1," and that it "has the same operation as the ECL-MOS level conversion circuit in FIG. 11." *Id.* Tachibana describes "PMOS transistors 400, 401, diodes 500, 501, bipolar transistors 108, 109, and NMOS transistors 306, 307, 308, 309" in Figure 11 as "elements comprising a level conversion circuit," and explains that this

circuit performs "boosting" of a signal "over two stages." *Id.*, pp. 117-118. As shown in Figure 11, below, a single "stage" of this circuit is substantially similar to the circuit identified above in Figure 15:

FIG. 15

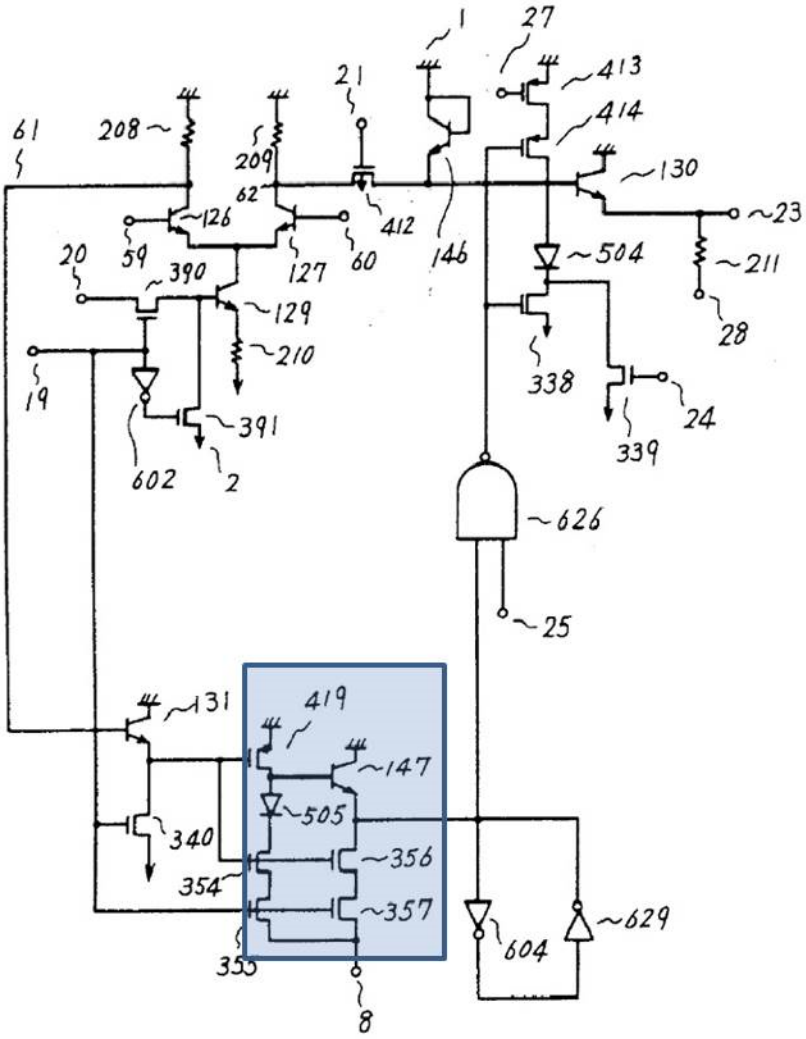
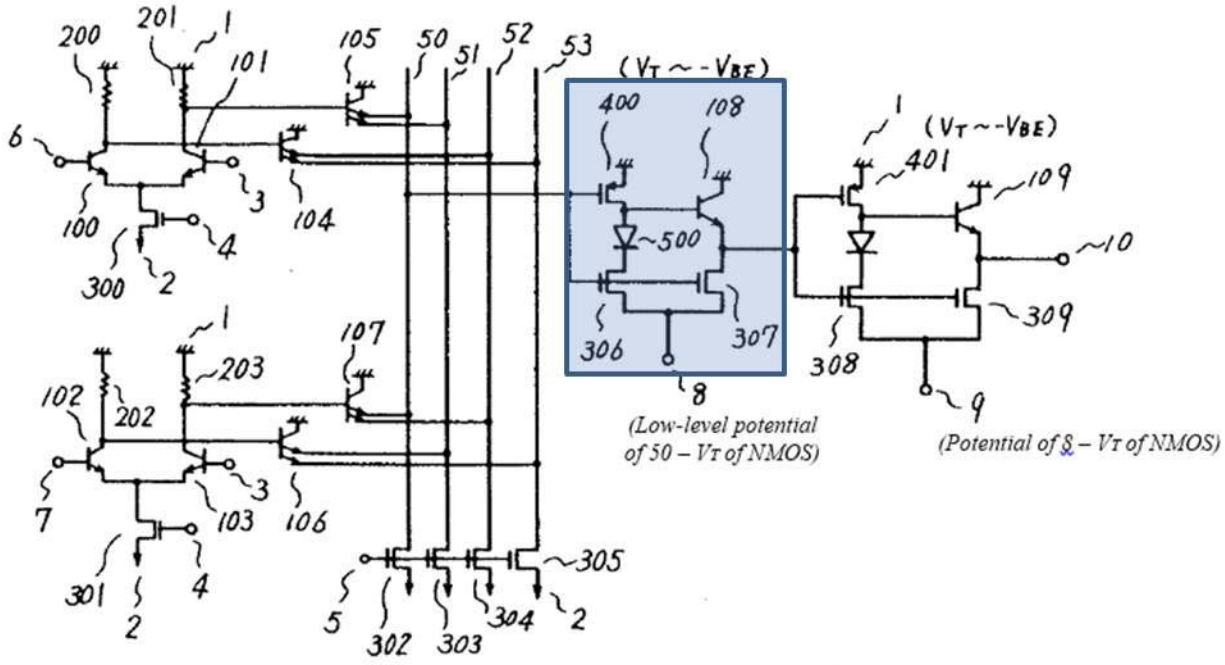


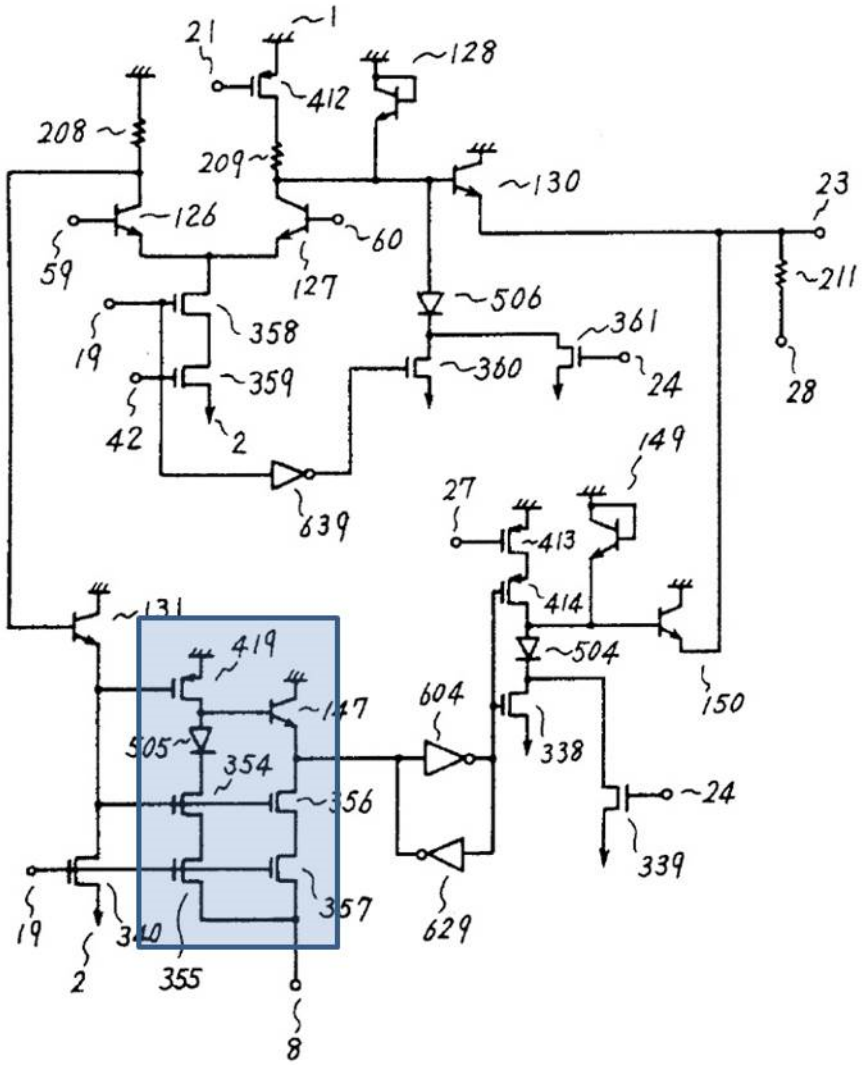
FIG. 11



Tachibana further describes ECL-MOS level conversion circuit 623 in Figure 1 as "a level conversion circuit for clock signal control comprised of a MOS transistor that amplifies the output signal of differential amplifier 622 to the level at which the MOS transistor operates." *Id*., p. 111. A POSA would therefore have understood the circuit in Figure 15 comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357 to also be an ECL-MOS level conversion circuit, which is a level converter because it converts the amplitude of the output signal from the differential amplifier to MOS transistor levels. Ex. 1003, A19-A25.

Tachibana also discloses, in Figure 17, a circuit identical to the one discussed above in Figure 15, comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357:

FIG. 17



Because Tachibana discloses that elements in Figure 17 "with the same number as those of the circuits in FIG. 1, FIG. 15, and FIG. 16 correspond to the element with the same number in the circuit in FIG. 1, FIG. 15, and FIG. 16," Ex.

1005, p. 120, a POSA would have understood that this circuit in Figure 17, like the identical one in Figure 15, "has the same operation as the ECL-MOS level conversion circuit in FIG. 11" and is therefore a level converter. *Id*., p. 119. Ex. 1003, A23-A25.

In the embodiments of Figures 15 and 17, the respective ECL-MOS level conversion circuits discussed above are responsive to the differential amplifier and the PMOS transistor 412. In both embodiments, one of the outputs of the differential amplifier (reference numeral 61 in Figure 15; unnumbered output of bipolar transistor 126 in Figure 17) is an input to the ECL-MOS level conversion circuit through bipolar transistor 131, as indicated in the figures below:

FIG. 15

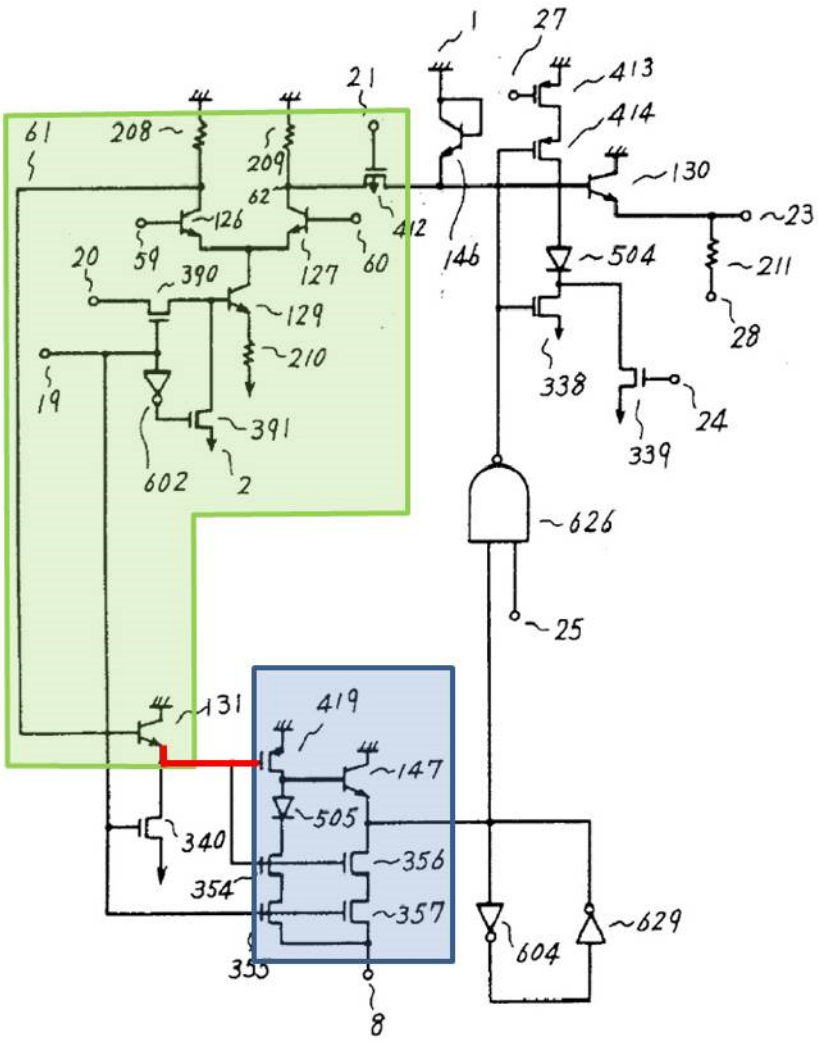
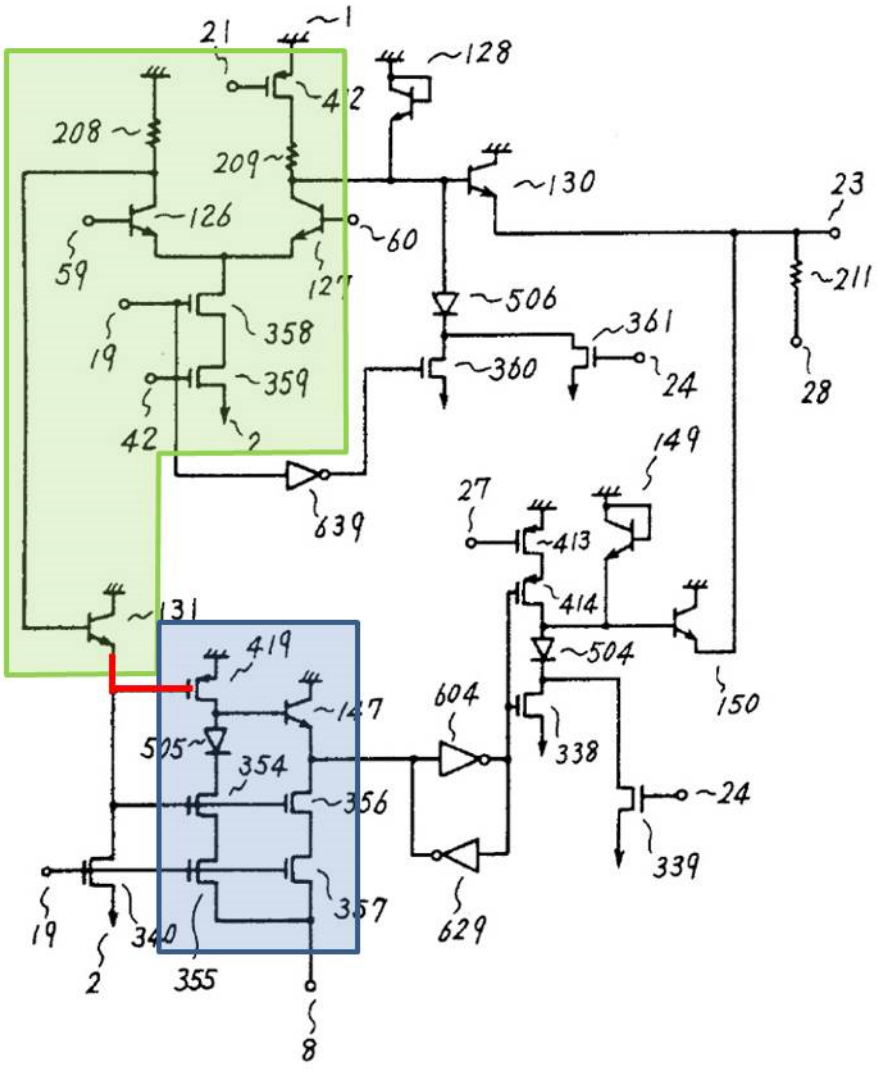

1
27
413
414
21
61
208
209
62
130
23
126
412
146
504
211
20
59
390
127
60
129
28
210
338
19
24
391
339
602
2
626
25
131
419
147
505
340
356
354
357
604
629
355
8

FIG. 17



The ECL-MOS level conversion circuits are therefore responsive to the differential amplifier. Ex. 1003, A22-23, A25.

Additionally, as discussed above, PMOS transistor 412 affects the output potential of the differential amplifier by setting the impedance of output 62 (and its corresponding unlabeled output in Figure 17) to high impedance when it is activated. *Id*., pp. 112, 119. This changes the amount of current that flows through

resistor 209 and transistor 127, which in turn changes the current flow through resistor 208 and transistor 126. This changes the potential on output 61 (and its corresponding unlabeled output in Figure 17), which as noted above, is an input to the ECL-MOS level conversion circuit. Ex. 1003, A22-23, A25.

Accordingly, Tachibana discloses a level converter (comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357 in Figures 15 and 17) responsive to the differential amplifier (the differential amplifier in Figures 15 and 17, as discussed above in limitation [1.2]) and the impedance control circuit (PMOS transistor 412) [7].

10.1.6. [1.5] "a clock-free latch responsive to the level converter."

Tachibana discloses this limitation. In both Figure 15 and Figure 17, Tachibana discloses a circuit comprised of two inverters 604 and 629:

[7] Additionally, the ECL-MOS level conversion circuit is responsive to transistor 340 in Figures 15 and 17. Transistor 340 is an impedance control circuit because it controls the impedance of the ECL-MOS level conversion circuit. Ex. 1003, A15.

FIG. 15

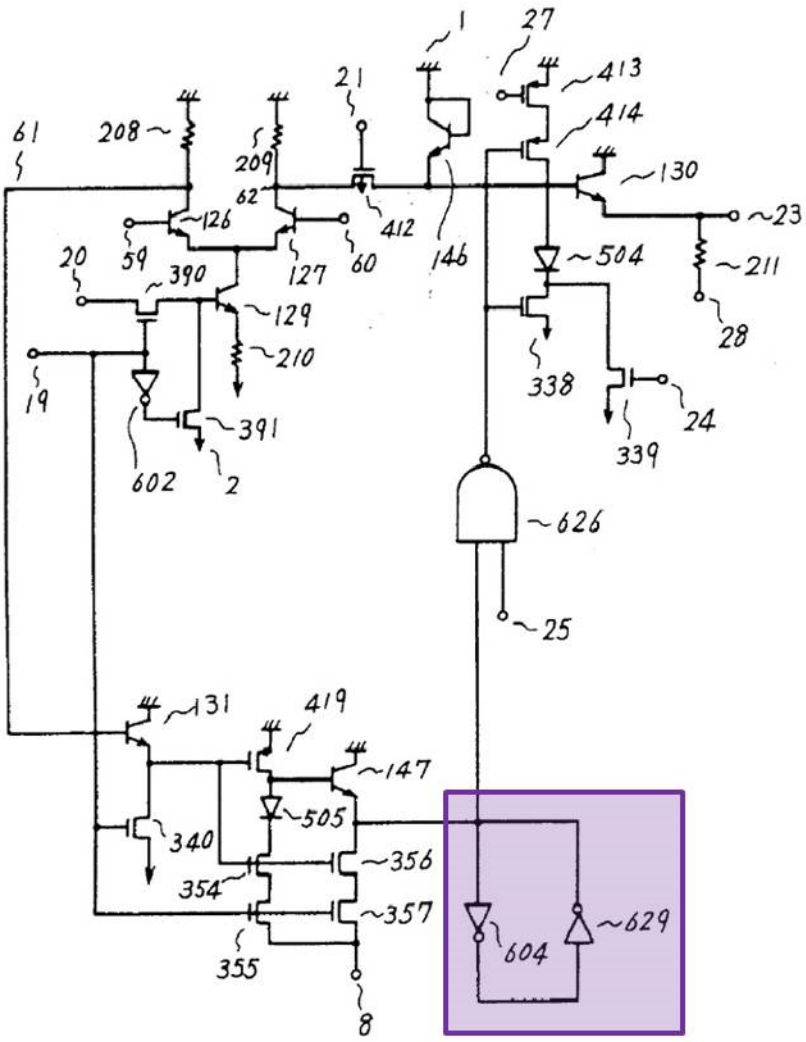
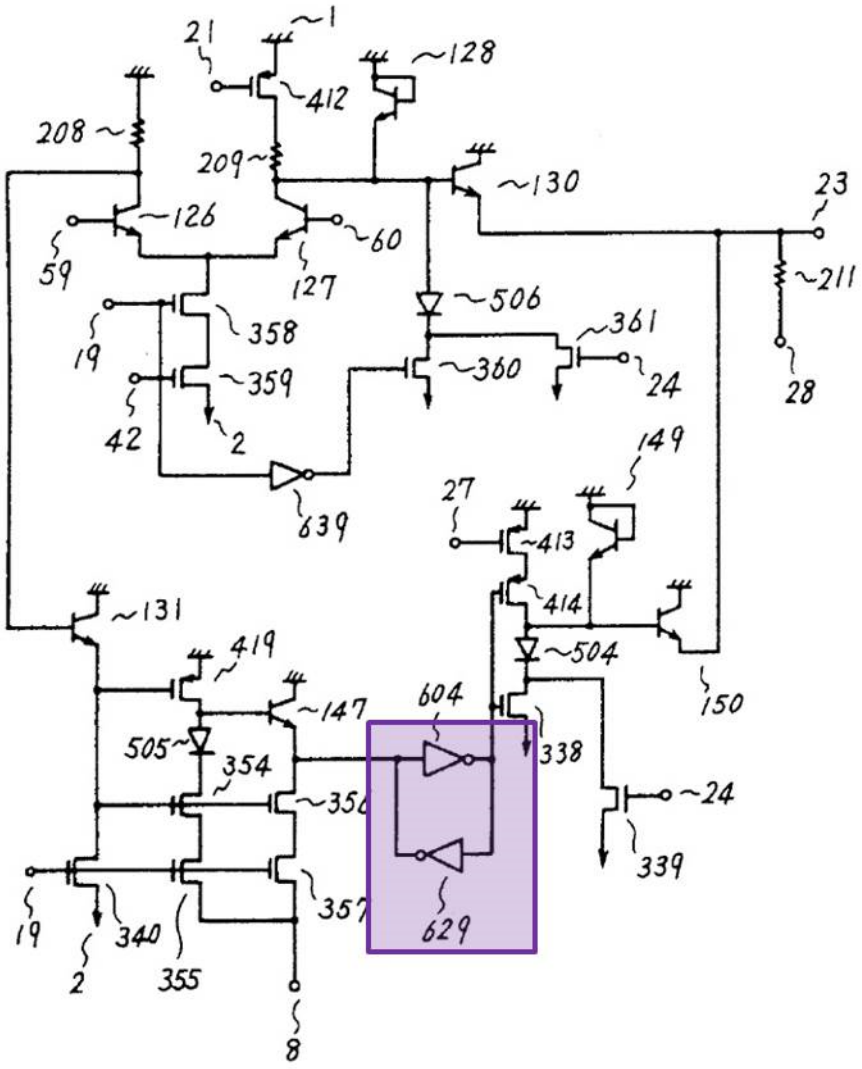

1
27
413
414
21
61
208
209
62
130
23
126
412
59
60
127
146
504
211
20
390
129
28
210
338
19
24
391
339
602
2
626
25
131
419
147
505
340
356
354
357
629
604
355
8

FIG. 17



In connection with Figure 15, Tachibana discloses that the inverters 604 and 629 "were used for the latch circuit 650 in FIG.1 instead of a clock inverter circuit." Ex. 1005, p. 119. A POSA would therefore have understood the inverters 604 and 629 in Figure 15 to comprise a latch. Ex. 1003, A25-29. Moreover, as discussed above, Tachibana discloses that elements in Figure 17 "with the same number as those of the circuits in FIG. 1, FIG. 15, and FIG. 16 correspond to the

element with the same number in the circuit in FIG. 1, FIG. 15, and FIG. 16." Ex. 1005, p. 120. A POSA would therefore have understood that the inverters 604 and 629 in Figure 17 correspond to the inverters 604 and 629 in Figure 15, and therefore that they also comprise a latch. Ex. 1003, A25-29. Additionally, as noted in the Background of the Technology section, coupling two inverters in this way was a commonplace method of forming a latch. Ex. 1003, ¶38.

Tachibana discloses that the latch comprised of inverters 604 and 629 is clock-free, because as shown in Figures 15 and 17 below, the *only* input into this portion of the circuit is the output from the ECL-MOS level converter:

FIG. 15

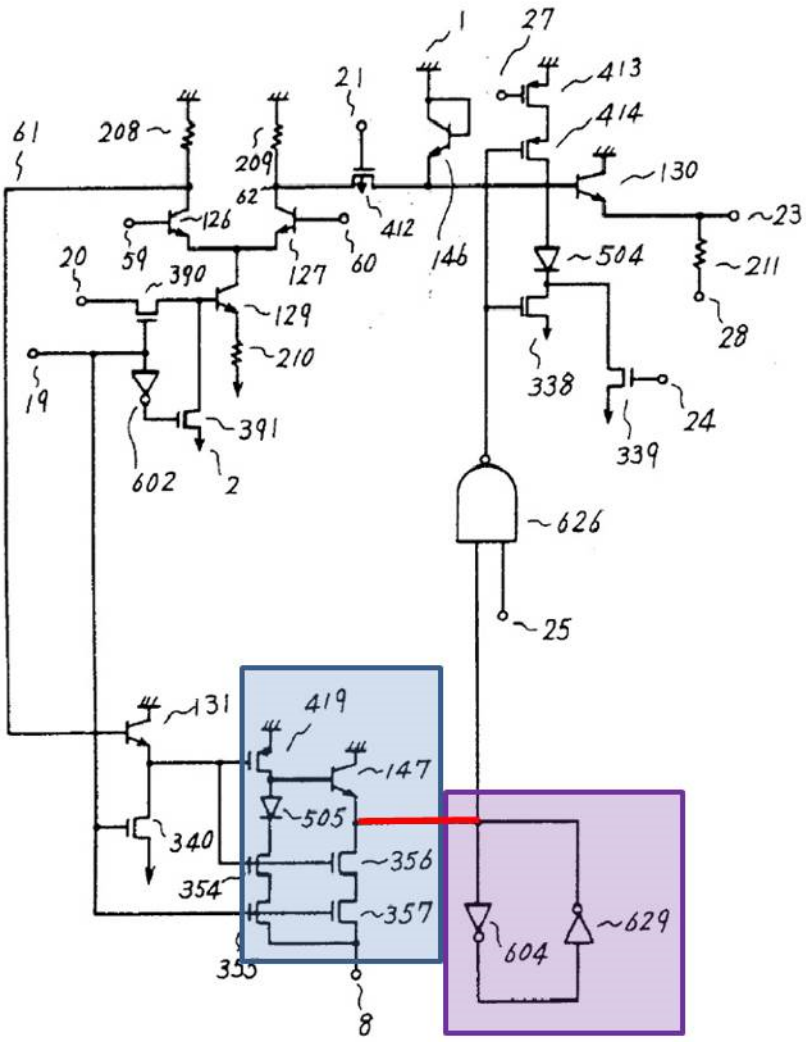
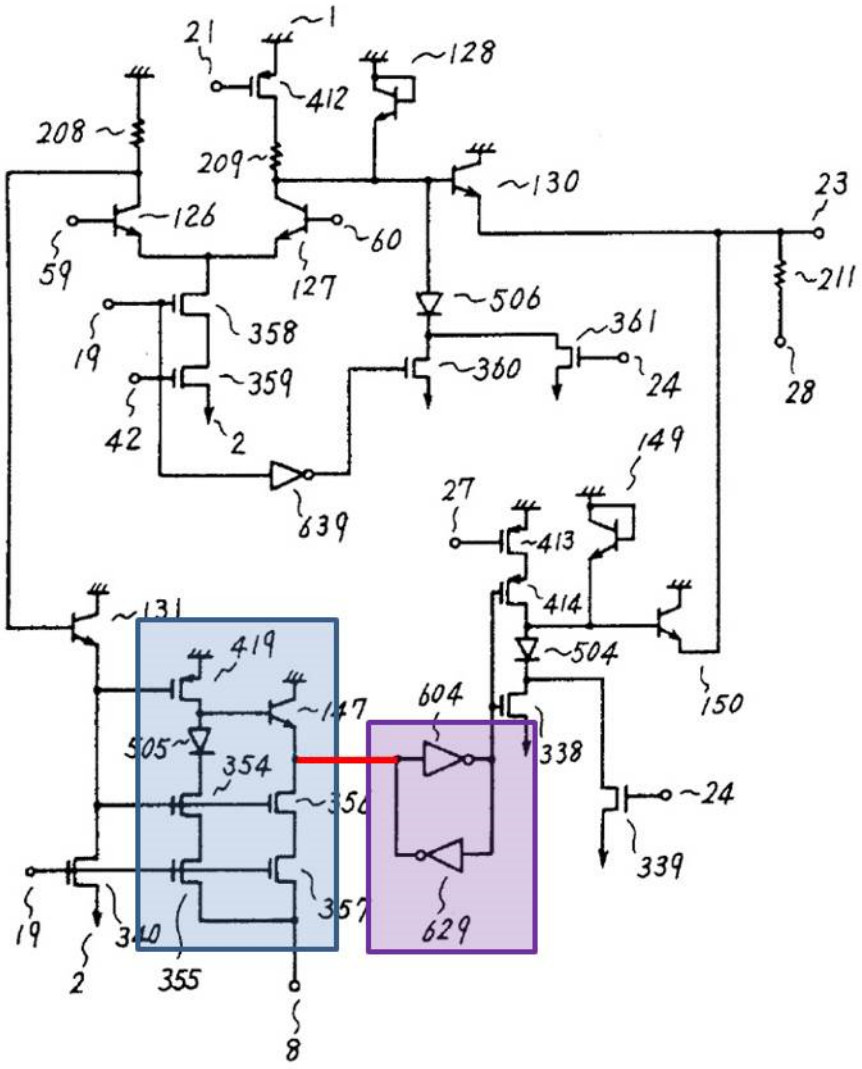

1
27
413
414
21
61
208
209
62
130
23
126
412
146
59
60
127
504
211
20
390
129
28
210
338
19
24
391
339
602
2
626
25
131
419
147
505
340
356
354
357
629
604
355
8

FIG. 17



As seen in the figures above, the latch comprised of inverters 604 and 629 does not take any clock signal as an input. Additionally, because the latch takes the output of the ECL-MOS level converter as its input, it is responsive to the ECL-MOS level converter. Ex. 1003, A25-29.

Accordingly, Tachibana discloses a clock-free latch (inverters 604 and 629 in Figures 15 and 17) responsive to the level converter (comprised of bipolar

transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357 in Figures 15 and 17).

10.2. Tachibana Anticipates Claim 2

10.2.1. [2.0] "The apparatus of claim 1, wherein the timing circuit is a clock delay circuit."

For the reasons discussed in Section 10.1, Tachibana discloses the apparatus of claim 1.

Tachibana further discloses this limitation. Although the 274 Patent does not expressly define a "clock delay circuit," the only embodiment disclosed in the 274 Patent for a clock delay circuit is a timing circuit with two output signals that are generated by passing an input signal (clock 78) through a number of intervening inverters (146, 147, 148) and other logic gates (149):

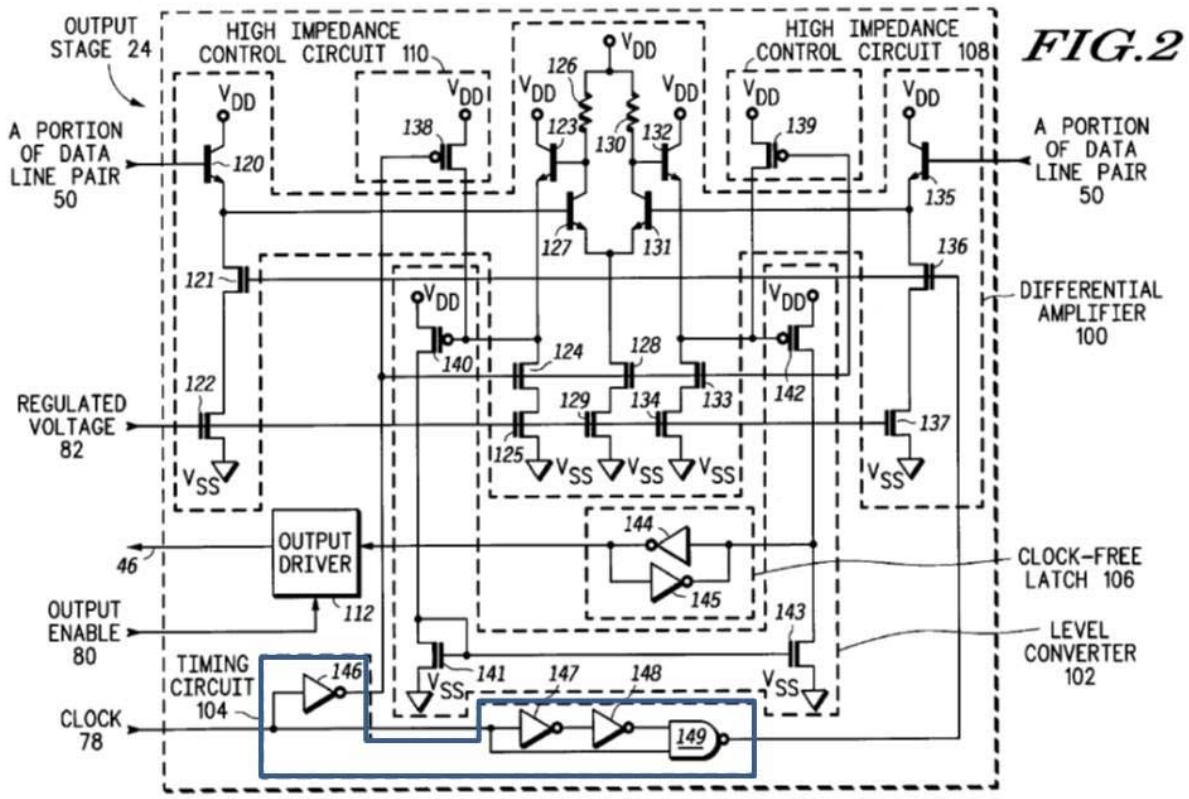


FIG.2

Tachibana similarly discloses a timing circuit that outputs a plurality of clock signals generated by passing input signals through intervening logic gates. In particular, the timing circuit disclosed in Figures 8 and 9 of Tachibana outputs clock signals 19, 21, 26, and 27, each of which is a clock signal that is generated by passing input signals through the logic that makes up the timing circuit. Ex. 1003, A29-A31.

FIG. 8

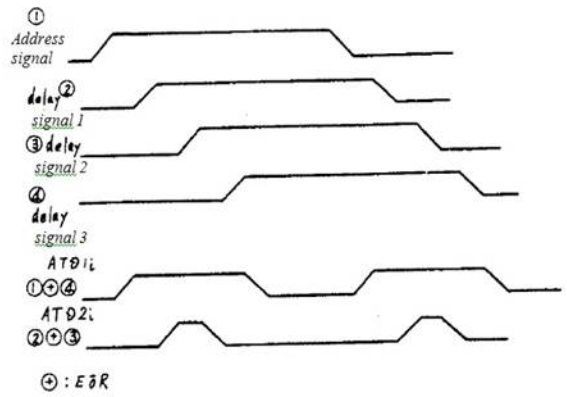
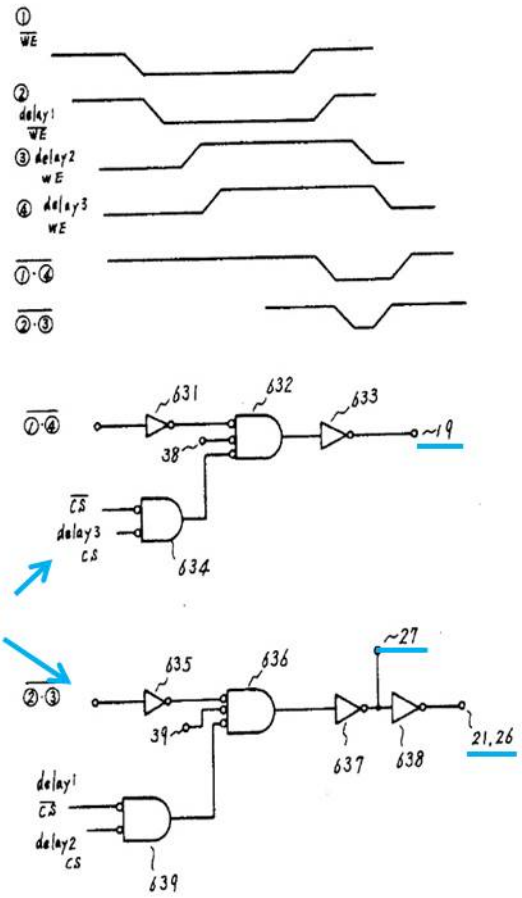


FIG. 9



WE	CS	WE · CS
0	0	1
0	1	1
1	0	0
1	1	1

As shown in the figure above, the timing circuit takes input signals $ATD1_1$, $ATD1_i$, $ATD2_1$, $ATD2_i$, $\overline{\overline{WE} \cdot CS}$[8], $\overline{CS}$, delay3 CS, $\overline{② \cdot ③}$, delay1 $\overline{CS}$, and delay2 CS and outputs signals 19, 21, 26, and 27 after passing the initial inputs through a series of inverters and other logic gates. Thus, the timing circuit in Figures 8 and 9

[8] As shown in Figures 6 and 8 of Tachibana, $\overline{\overline{WE} \cdot CS}$ is a signal formed by inverting signal 25, which is a signal created by ANDing together the write enable signal $\overline{WE}$ and the chip select signal CS. Ex. 1005, Figs. 6, 8.

of Tachibana is a clock delay circuit, as that term is used in the 274 Patent. Ex. 1003, A29-A30.

Tachibana expressly discloses that "19, 21, 24, 26, 27 are clock signal terminals," and therefore the signals they carry are clock signals. Ex. 1005, p. 111.

Accordingly, Tachibana discloses a timing circuit that is a clock delay circuit.

10.3. Tachibana Anticipates Claim 3

10.3.1. [3.0] "The apparatus of claim 1, wherein the clock-free latch includes a first inverter and a second inverter."

For the reasons discussed in Section 10.1, Tachibana discloses the apparatus of claim 1. Additionally, for the reasons discussed in Section 10.1.6, Tachibana discloses that a first inverter 604 and a second inverter 629 comprise the clock-free latch. *See* claim [1.5]. Accordingly, Tachibana discloses that the clock-free latch includes a first inverter (inverter 604) and a second inverter (inverter 629). Ex. 1003, A31-A32.

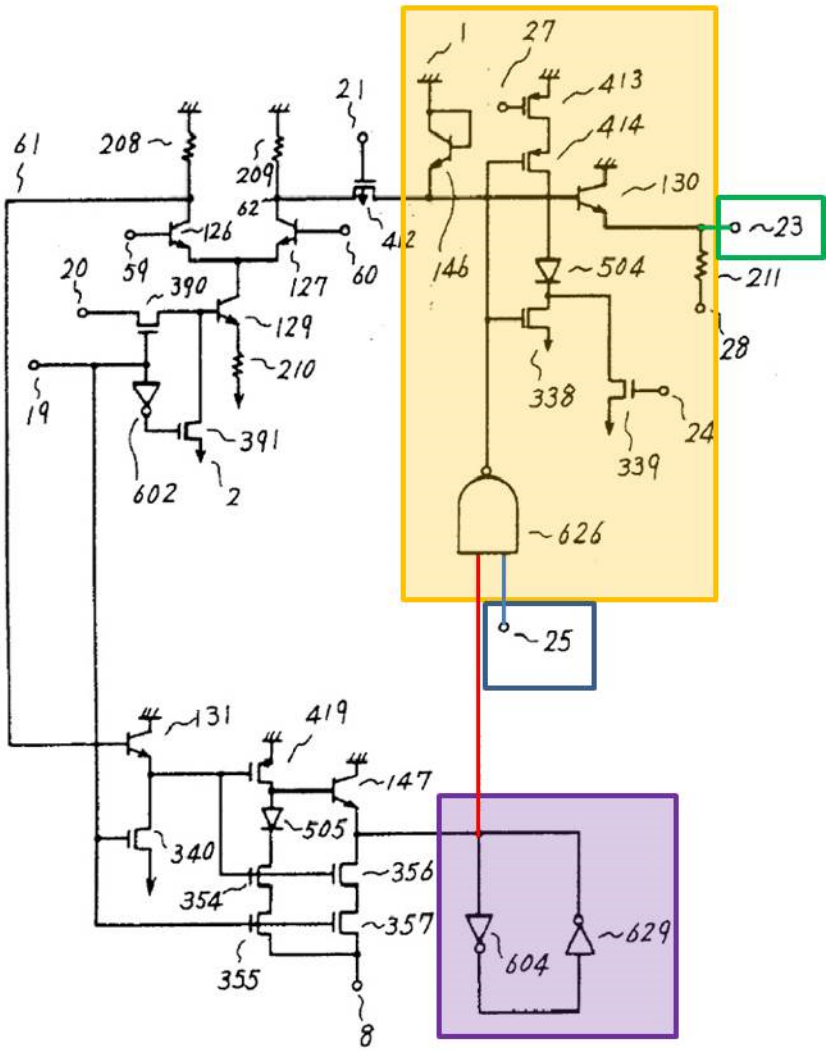
10.4. Tachibana Anticipates Claim 8

10.4.1. [8.0] "The apparatus of claim 1, further comprising a driver module responsive to the clock-free latch, the driver module receiving an output enable signal and producing an output signal."

As discussed above in Section 10.1, Tachibana discloses the apparatus of claim 1.

Tachibana discloses, in Figure 15, a module that receives the output of the latch circuit (comprised of inverters 604 and 629), receives a signal on control terminal 25, and outputs a signal on terminal 23. The module is indicated in the figures below in yellow:

FIG. 15



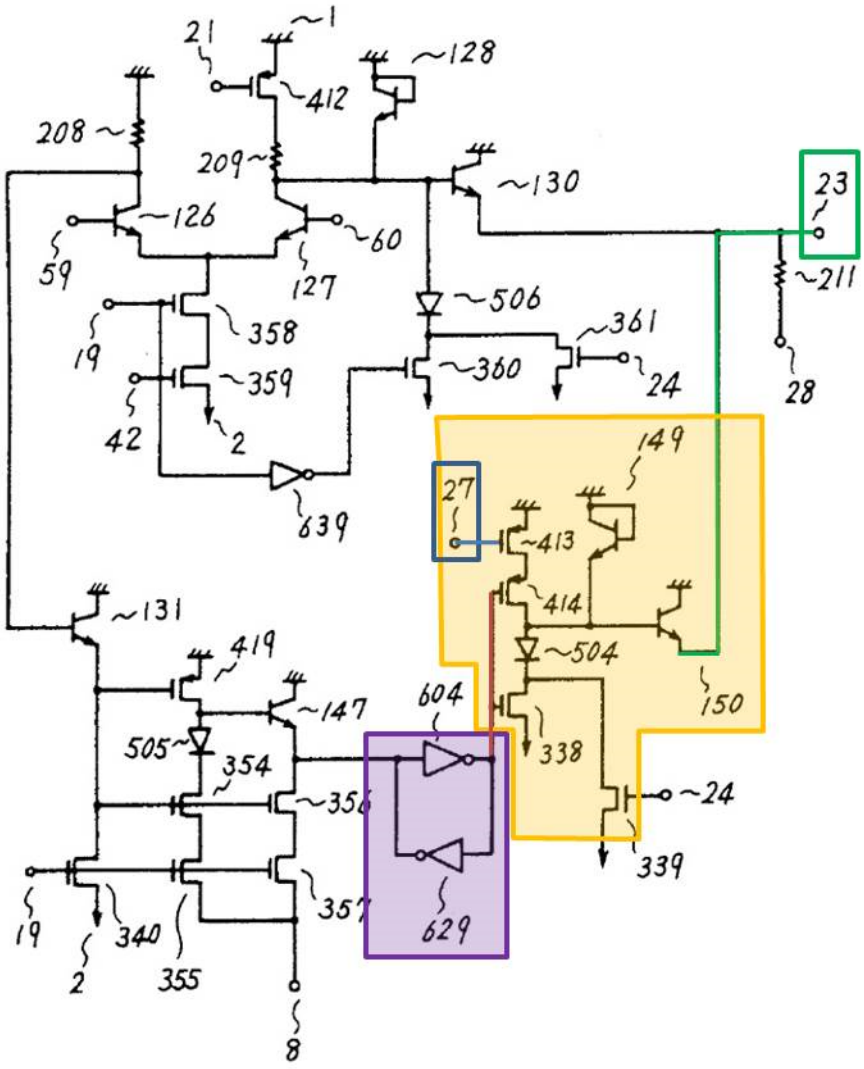
As can be seen in the figures, the output of the latch circuit comprised of inverters 604 and 629 is an input to NAND gate 626. The signal on terminal 25 is

also an input to NAND gate 626. Tachibana describes that "25 is a control terminal during write and chip non-select" and that because of this, "high level potential is provided in the read state." Ex. 1005, pp. 111-112. Although this is provided in the context of Figure 1, Tachibana discloses that elements and terminals in Figures 15 and 17 that have the same reference numeral as elements in Figure 1 correspond to those same elements, *id.*, pp. 119-120, and therefore a POSA would have understood that 25 is a control terminal that provides a high level signal during read operations in Figures 15 and 17, which enables output during read operations. In other words, the signal on terminal 25 is an output enable signal. Ex. 1003, A33-A34. Thus, the output of the NAND gate 626 is responsive to the output of the latch circuit and the signal on terminal 25, which are the two inputs to the NAND gate 626. Because the output of the NAND gate 626 is, in turn, an input into the rest of the module indicated in yellow, the module is therefore responsive to the latch. Ex. 1003, A32-A36.

Finally, Tachibana discloses that terminal 23 "is an output terminal." Ex. 1005, p. 111; *see also id*., p. 124.

Similarly, Figure 17 discloses a module that receives the output of the latch circuit (comprised of inverters 604 and 629), receives a signal on control terminal 25, and outputs a signal on terminal 23.

FIG. 17



As shown in Figure 17, the output of the latch circuit comprised of inverters 604 and 629 is an input into the module annotated in yellow. Clock signal 27 is also an input into this module. The module outputs the output signal 23. Ex. 1003, A36-A37.

Thus, Tachibana discloses a driver module (as indicated above in Figures 15 and 17) responsive to the clock-free latch (comprised of inverters 604 and 629), the

driver module receiving an output enable signal (the signal on control terminal 25 in Figure 15, and control terminal 27 in Figure 17) and producing an output signal (the signal on output terminal 23).

10.5. Tachibana Anticipates Claim 9

10.5.1. [9.0] "The apparatus of claim 1, wherein the level converter includes a plurality of transistors."

As discussed above in Section 10.1, Tachibana discloses the apparatus of claim 1.

Additionally, as discussed above, Tachibana discloses that the level converter includes a plurality of transistors. Tachibana discloses that the ECL-MOS level conversion circuit includes a plurality of transistors comprised of at least bipolar transistor 147, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357. *See* claim [1.4]. Ex. 1003, A37.

10.6. Tachibana Anticipates Claim 10

10.6.1. [10.0] "The apparatus of claim 1, wherein the differential amplifier has an output driven by at least one of an emitter and a source of a transistor.

As discussed above in Section 10.1, Tachibana discloses the apparatus of claim 1.

Additionally, Tachibana discloses this limitation. Tachibana discloses in Figures 15 and 17 that a bipolar transistor 131 provides the output of the differential amplifier to the ECL-MOS level conversion circuit:

FIG. 15

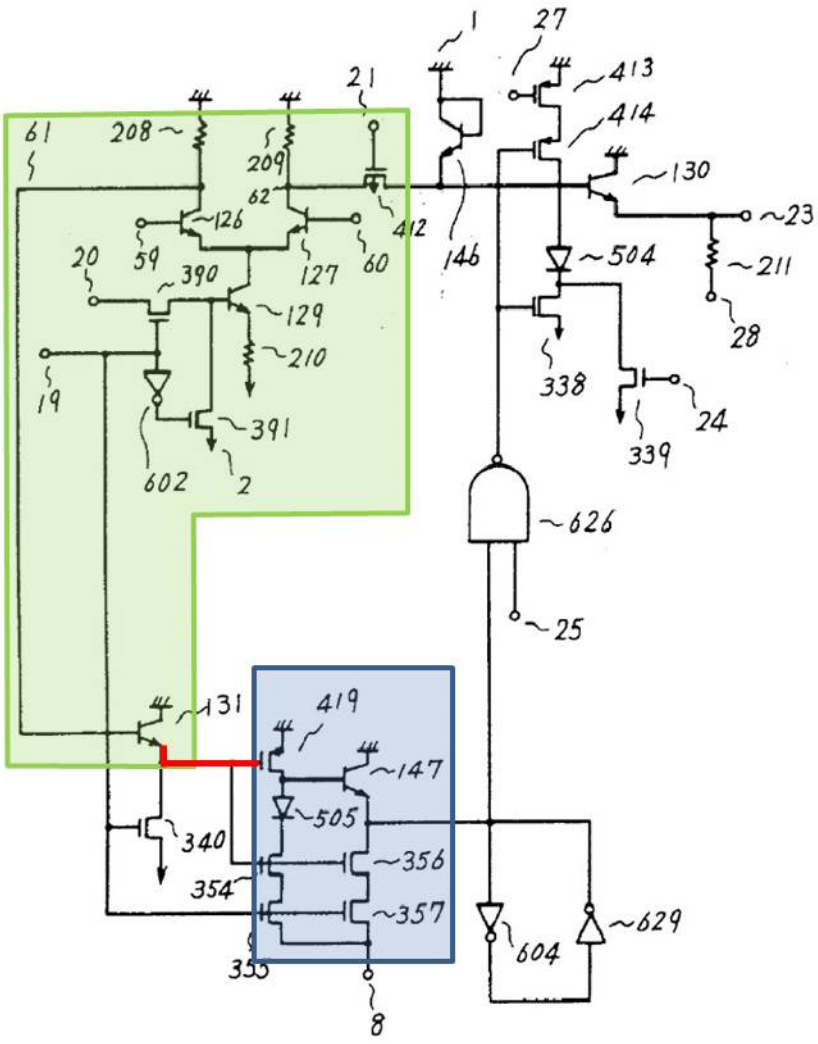
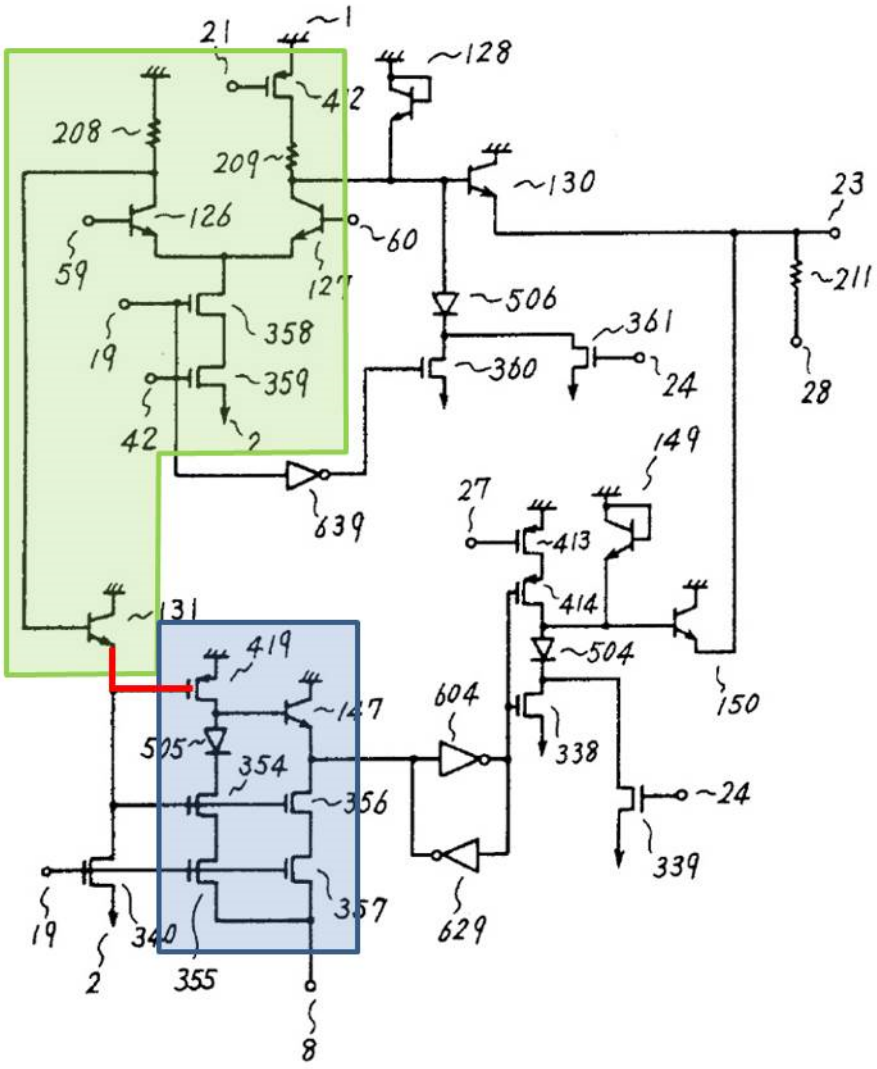

1
27
413
414
21
61
208
209
62
130
23
126
412
146
504
211
20
59
390
127
60
129
28
210
338
19
24
391
339
602
2
626
25
131
419
147
505
340
356
354
357
604
629
355
8

FIG. 17



As can be seen in the figures above, the emitter of bipolar transistor 131 (indicated by the arrow pointing away from the base of the transistor) drives the output of the differential amplifier to the ECL-MOS level conversion circuit. Ex. 1003, A37-A41. This is consistent with the disclosure in the 274 Patent, which in Figure 2 shows one of the two outputs of the long-tailed transistor pair (127 and 131) being driven by the emitter of bipolar transistor 123. *Id*. Accordingly,

Tachibana discloses that the differential amplifier has an output driven by at least one of an emitter (the emitter of bipolar transistor 131) and a source of a transistor (bipolar transistor 131).

10.7. Tachibana Anticipates Claim 11

10.7.1. [11.0] "The apparatus of claim 1, wherein the impedance control circuit is a switching element connected to a power source."

As discussed above in Section 10.1, Tachibana discloses the apparatus of claim 1.

Additionally, Tachibana discloses that the impedance control circuit is a switching element connected to a power source. Tachibana describes that PMOS transistor 412 switches between a "non-conducting state" (during data held state) and a "conducting state" (during data read). Ex. 1005, pp. 112-113. A POSA would therefore have understood that PMOS transistor 412 is a "switching element." As discussed above, PMOS transistor 412 is an impedance control circuit because it sets the output impedance of the differential amplifier to high impedance when in the non-conducting state. *See* claim [1.3]. Ex. 1003, A41-A42.

Further, as shown in Figure 15 below, PMOS transistor 412 is connected to a ground terminal through resistor 209. Similarly, as shown in Figure 17 below, PMOS transistor 412 is connected to ground terminal 1.

FIG. 15

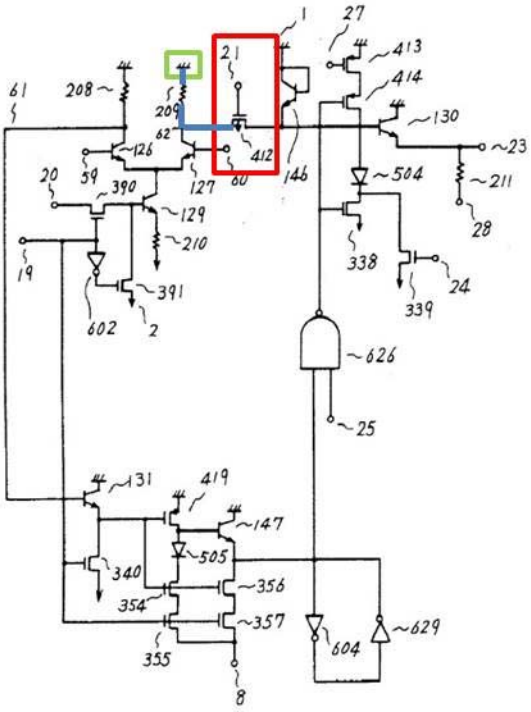
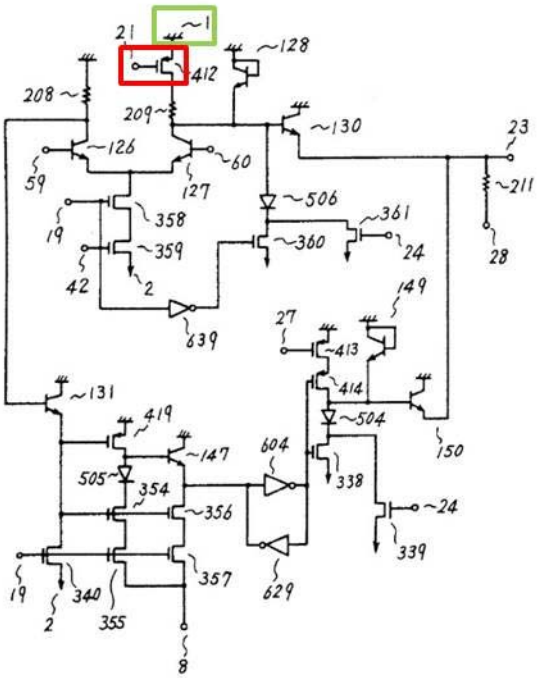


FIG. 17



The ground terminals are power sources because they supply power at ground voltage level. Ex. 1003, A41-A42.

Accordingly, Tachibana discloses that the impedance control circuit (PMOS transistor 412) is a switching element connected to a power source (a ground terminal).

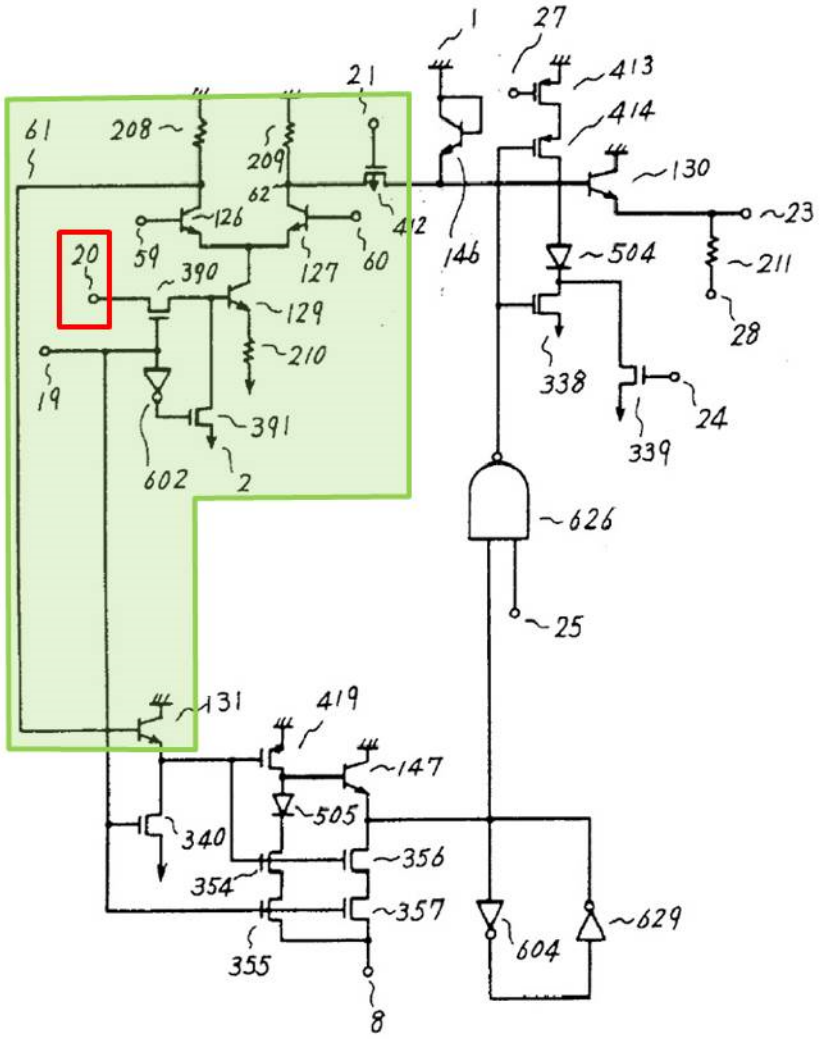
10.8. Tachibana Anticipates Claim 12

10.8.1. [12.0] "The apparatus of claim 1, wherein the differential amplifier receives a regulated voltage signal."

As discussed above in Section 10.1, Tachibana discloses the apparatus of claim 1.

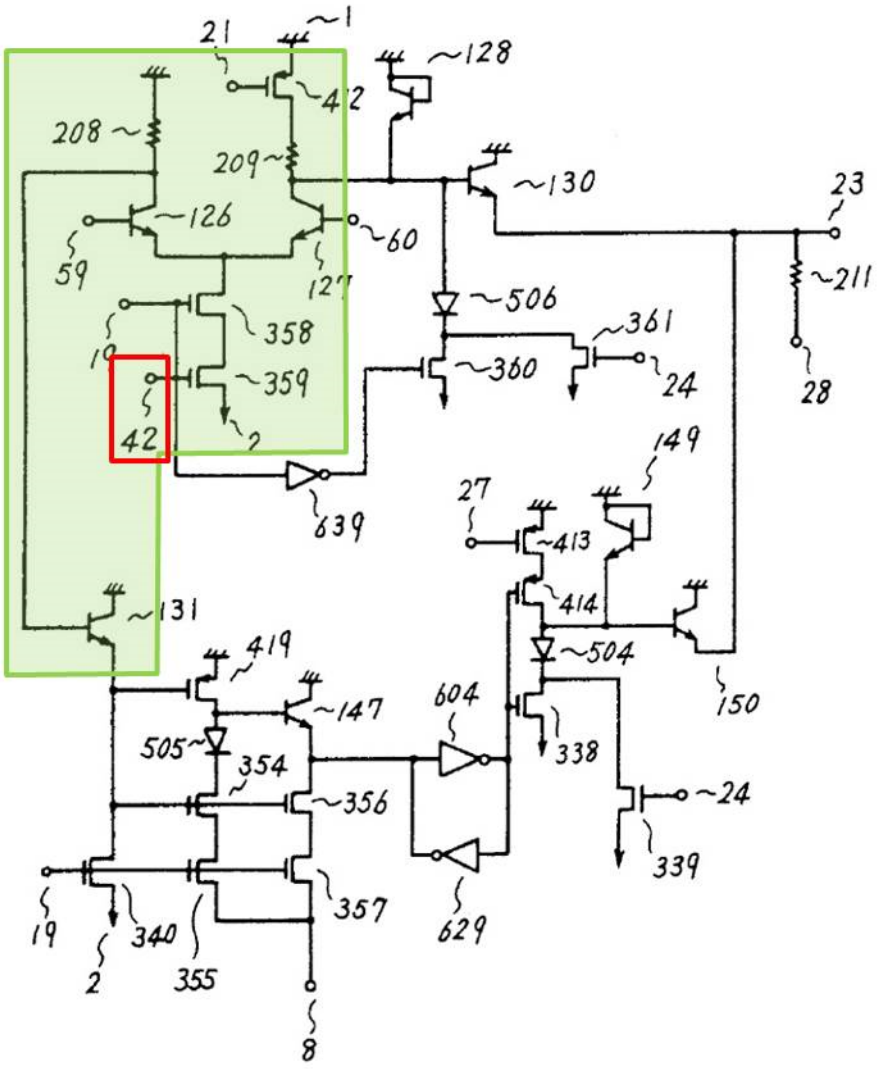
Additionally, Tachibana discloses that the differential amplifier receives a regulated voltage signal. Tachibana discloses that in Figure 15, the differential amplifier circuit receives a constant voltage from terminal 20, as shown below:

FIG. 15



Similarly, in Figure 17, Tachibana discloses that the differential amplifier circuit receives a constant voltage from terminal 42:

FIG. 17



Tachibana describes both terminal 20 and terminal 42 as "constant voltage terminals." *See* Ex. 1005, pp. 119-120, 124. Because the voltage on these terminals is constant, the voltage signal is regulated. This is consistent with the disclosure of the 274 Patent, which explains that the regulated voltage provides a current "which is substantially independent of the power supply voltage and temperature," *i.e.*, constant. Ex. 1001, 4:51-56. Ex. 1003, A42-A46.

Accordingly, Tachibana discloses that the differential amplifier receives a regulated voltage signal (from constant voltage terminal 20 or 42).

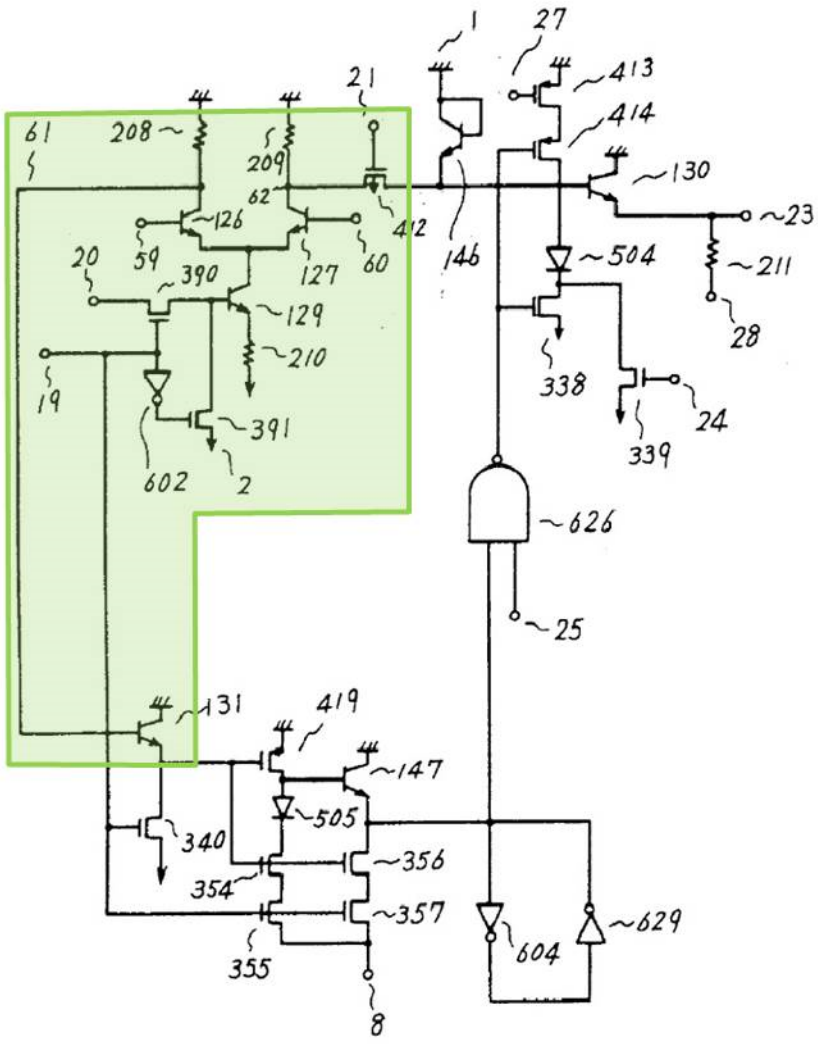
10.9. Tachibana Anticipates Claim 14

10.9.1. [14.P] "A method of amplifying a signal to produce a latched digital signal, the method comprising the steps of:"

To the extent the preamble is limiting, Tachibana discloses this limitation.

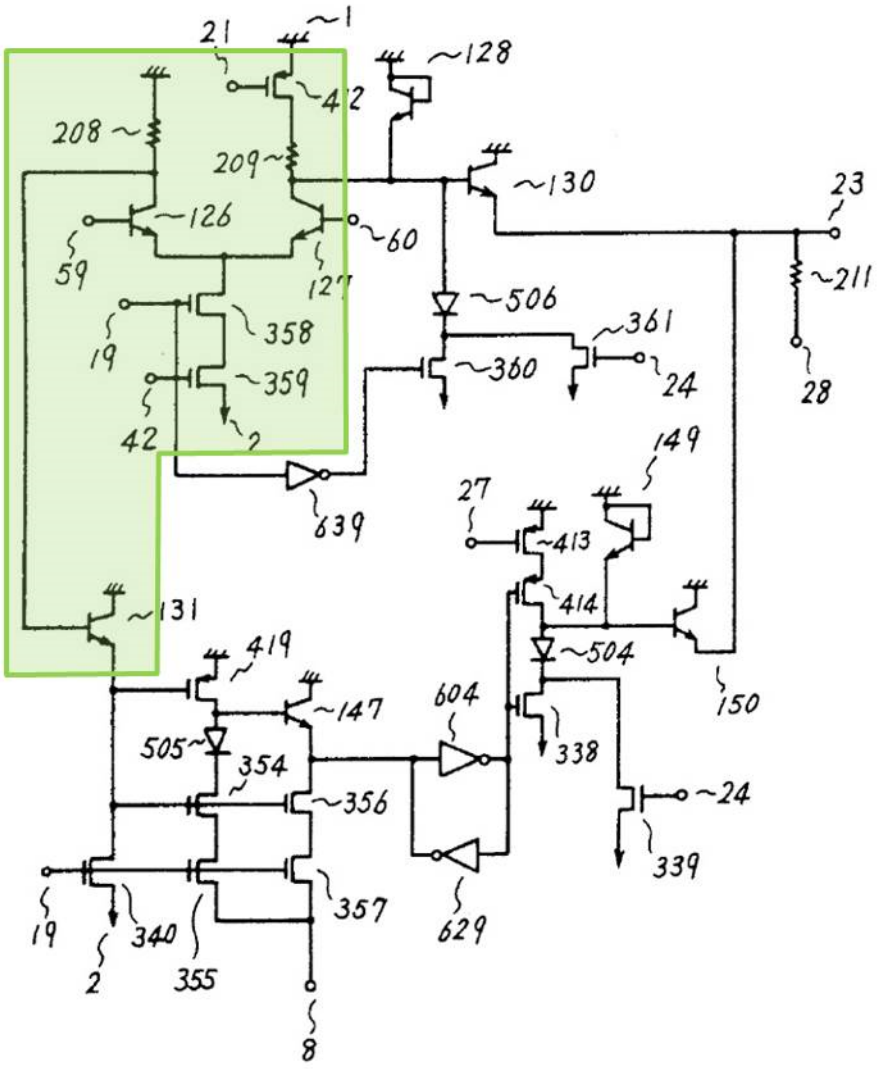
As discussed in connection with claim [1.2], Tachibana discloses a differential amplifier in Figure 15 comprising resistors 208 and 209, bipolar transistors 126 and 127, PMOS transistor 412, bipolar transistor 129, bipolar transistor 131, resistor 210, NMOS transistors 390 and 391, and inverter circuit 602. *See* claim [1.2]. Ex. 1003, A46.

FIG. 15



Tachibana also discloses a differential amplifier in Figure 17, comprising resistors 208 and 209, bipolar transistors 126 and 127, bipolar transistor 131, NMOS transistors 358 and 359, and PMOS transistor 412. *See* claim [1.2]. Ex. 1003, A46.

FIG. 17



As discussed in the Background of the Technology, the function of a differential amplifier is to amplify a signal, in particular, the difference between two input signals. Ex. 1003, A46. In Figures 15 and 17, the respective differential amplifiers discussed above amplify the difference between input signal 59 and input signal 60. Ex. 1003, A46.

As further discussed in connection with claim [1.4] and [1.5], the output 61 of the differential amplifier in Figures 15 and 17 is passed to a latch circuit comprised of inverters 604 and 629 through an ECL-MOS level conversion circuit, as shown below. *See also* claim [1.4], [1.5]. Ex. 1003, A46.

FIG. 15

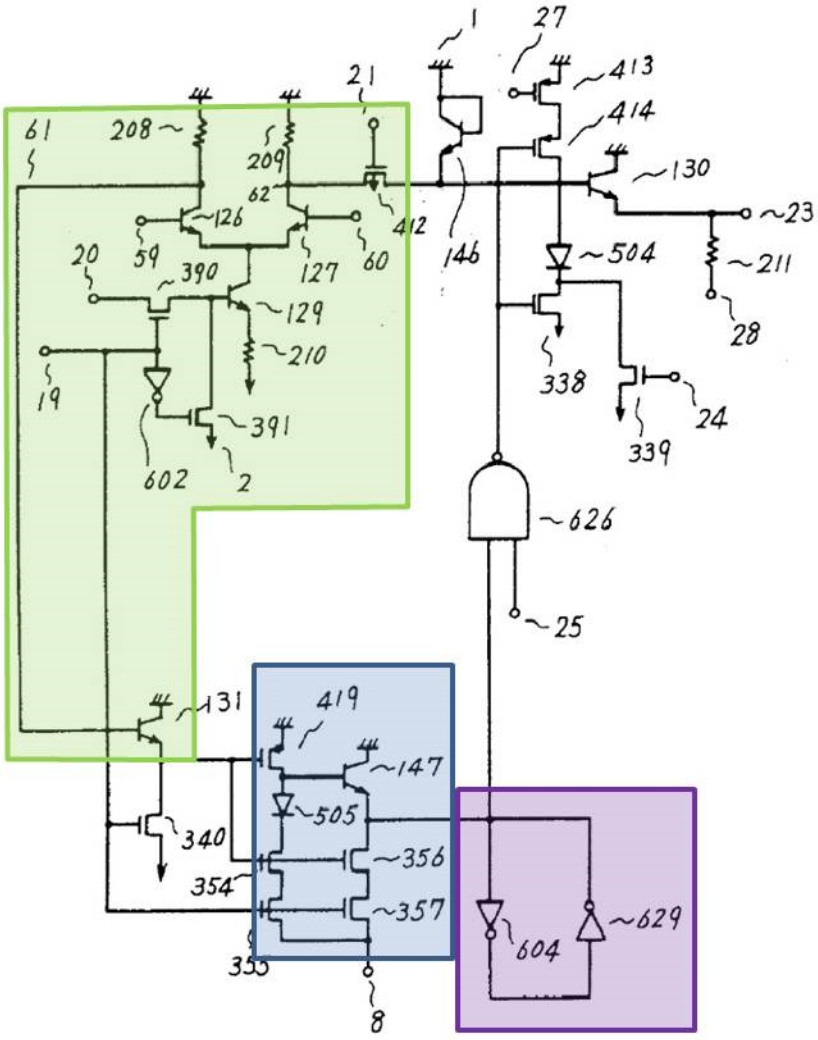
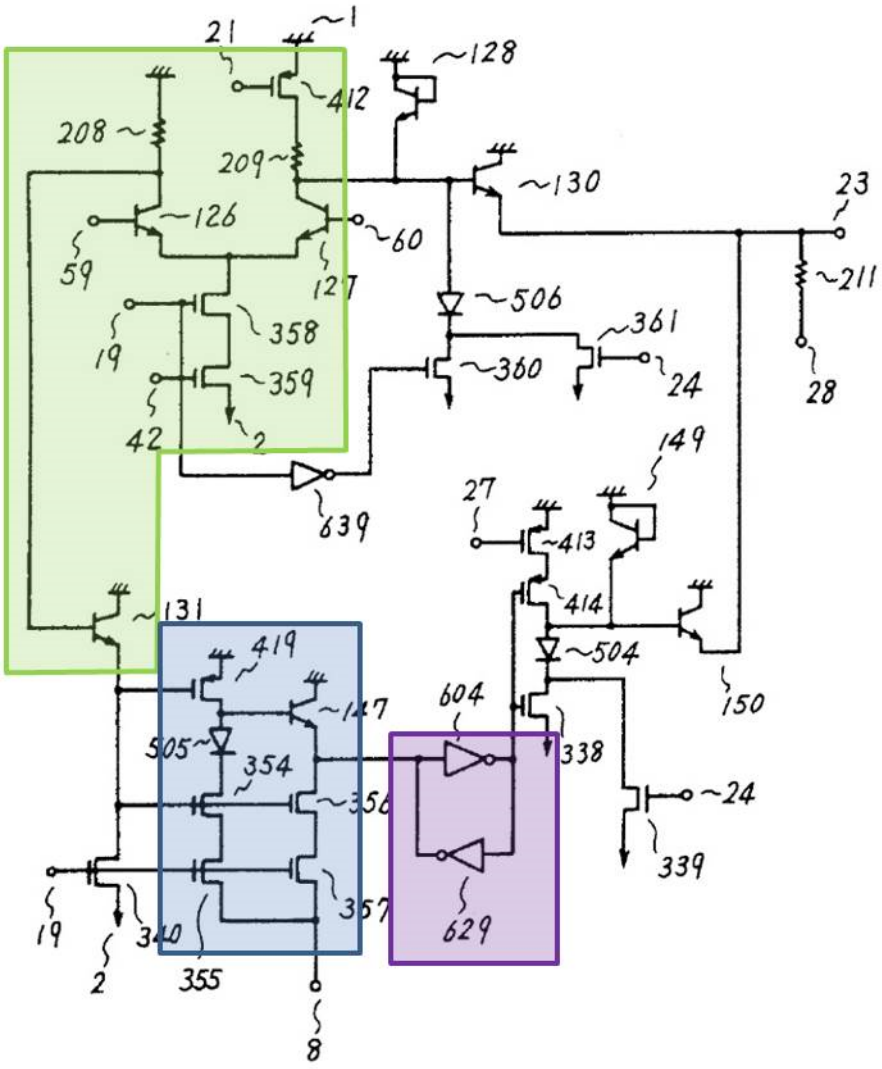


FIG. 17



Thus, the signal produced by the differential amplifier is latched by inverters 604 and 629, becoming a latched digital signal. Ex. 1003, A46.

Accordingly, Tachibana discloses amplifying a signal (the difference between input signals 59 and 60) to produce a latched digital signal.

10.9.2. [14.1] "amplifying a differential input to produce a differential output in response to a clock signal;"

As discussed in the immediately preceding section, Tachibana discloses amplifying the difference between input signals 59 and 60 and outputting the result as differential outputs on internal terminals 61 and 62 (unlabeled in Figure 17). *See* claim [14.P]. Ex. 1003, A46-A47. These outputs are each a differential output because they each reflect the amplified difference between the inputs 59 and 60. Ex. 1003, A47.

FIG. 15

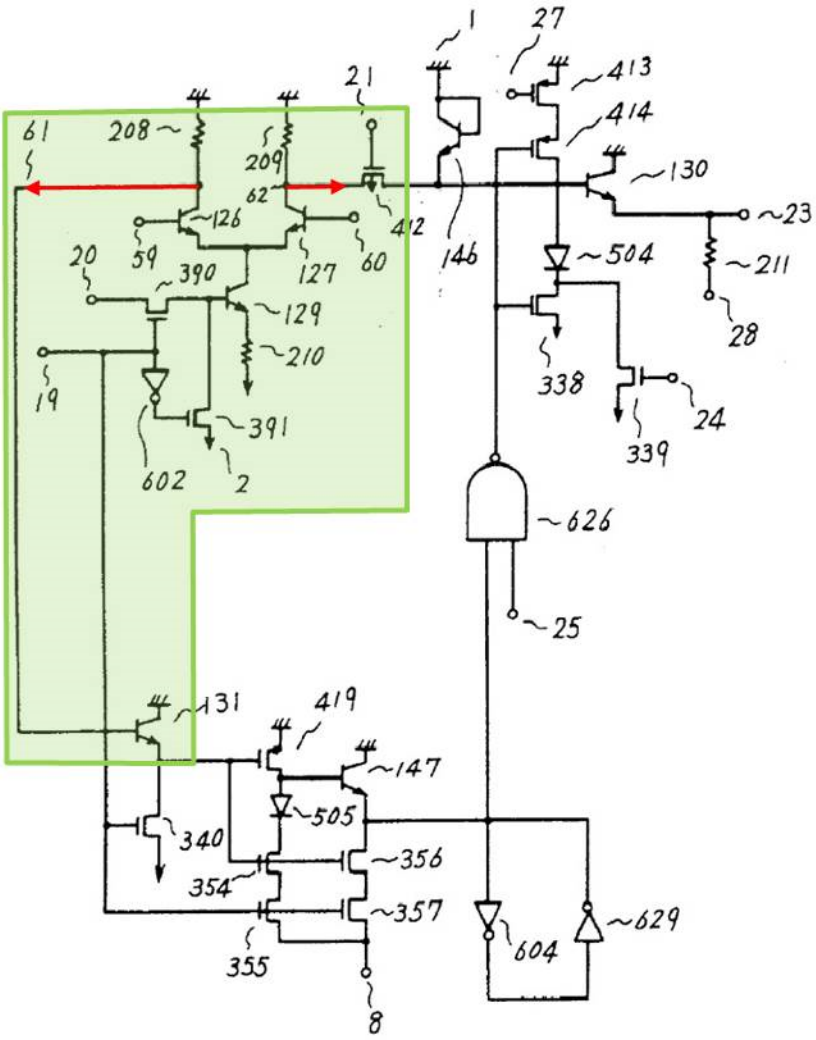
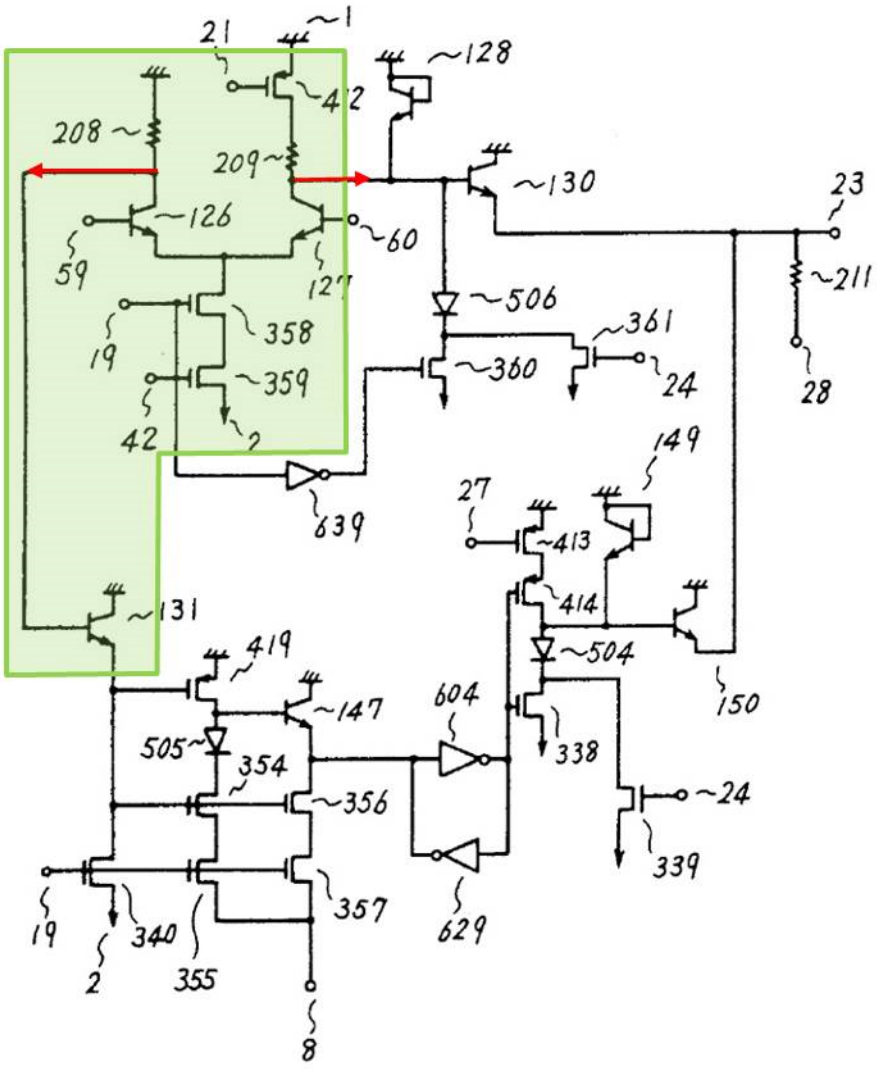


FIG. 17



Additionally, Tachibana discloses that this amplifying is done in response to a clock signal. In particular, as discussed in connection with claim [1.2], the differential amplifier in Figures 15 and 17 responds to the clock signal received on clock terminal 19. *See* claim [1.2]. When the signal on 19 is low, current does not flow to the differential amplifier, and the differential amplifier outputs the ground voltage level on both outputs 61 and 62 (unlabeled in Figure 17). Ex. 1005, p. 111.

When the signal on 19 is high, the differential amplifier is active and amplifies the difference between inputs 59 and 60. *Id*., p. 113. Ex. 1003, A46-A47.

Accordingly, Tachibana discloses amplifying a differential input (the difference between input signals 59 and 60) to produce a differential output (output signals 61 and 62) in response to a clock signal (the signal received on clock signal terminal 19).

10.9.3. [14.2] "level converting the differential output to produce a level converted signal;"

As discussed in connection with claim [1.4], Figures 15 and 17 of Tachibana discloses an ECL-MOS level conversion circuit comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357, the function of which is to level convert the output 61 of the differential amplifier to MOS transistor levels. Ex. 1005, p. 119; *see* claim [1.4]. As discussed with respect to the previous limitation, output 61 is a differential output because it reflects the amplified difference between the two inputs. Accordingly, the ECL-MOS level conversion circuit level converts the differential output. Ex. 1003, A47.

FIG. 15

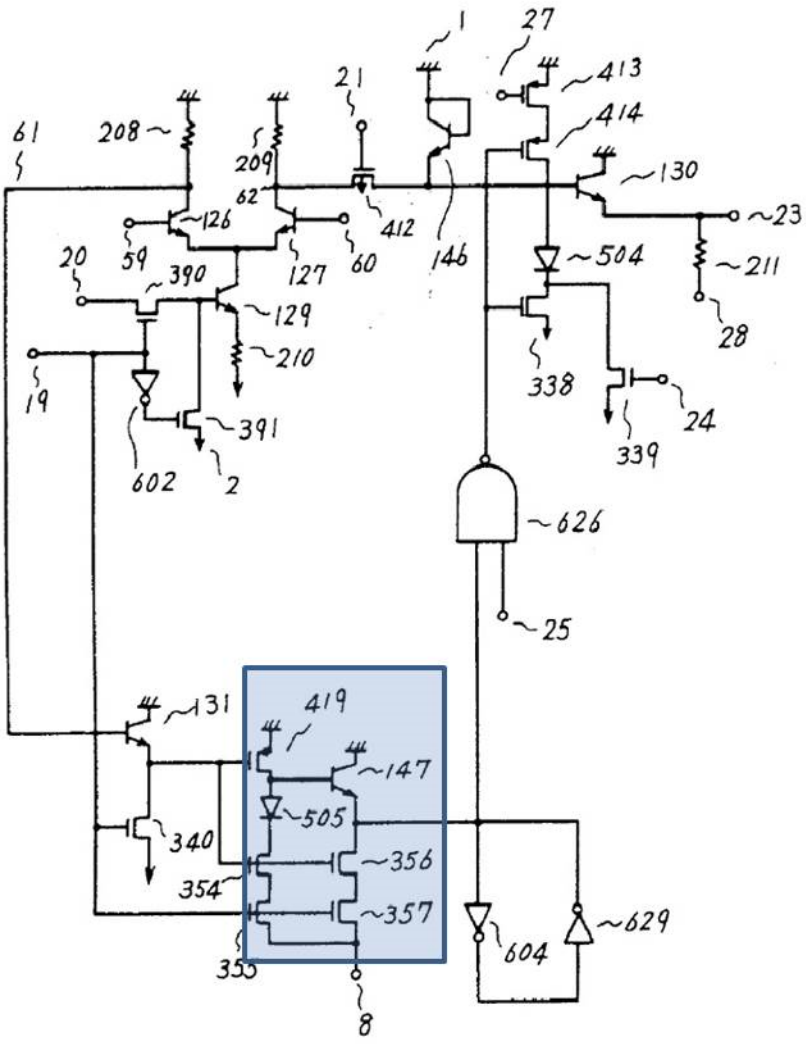
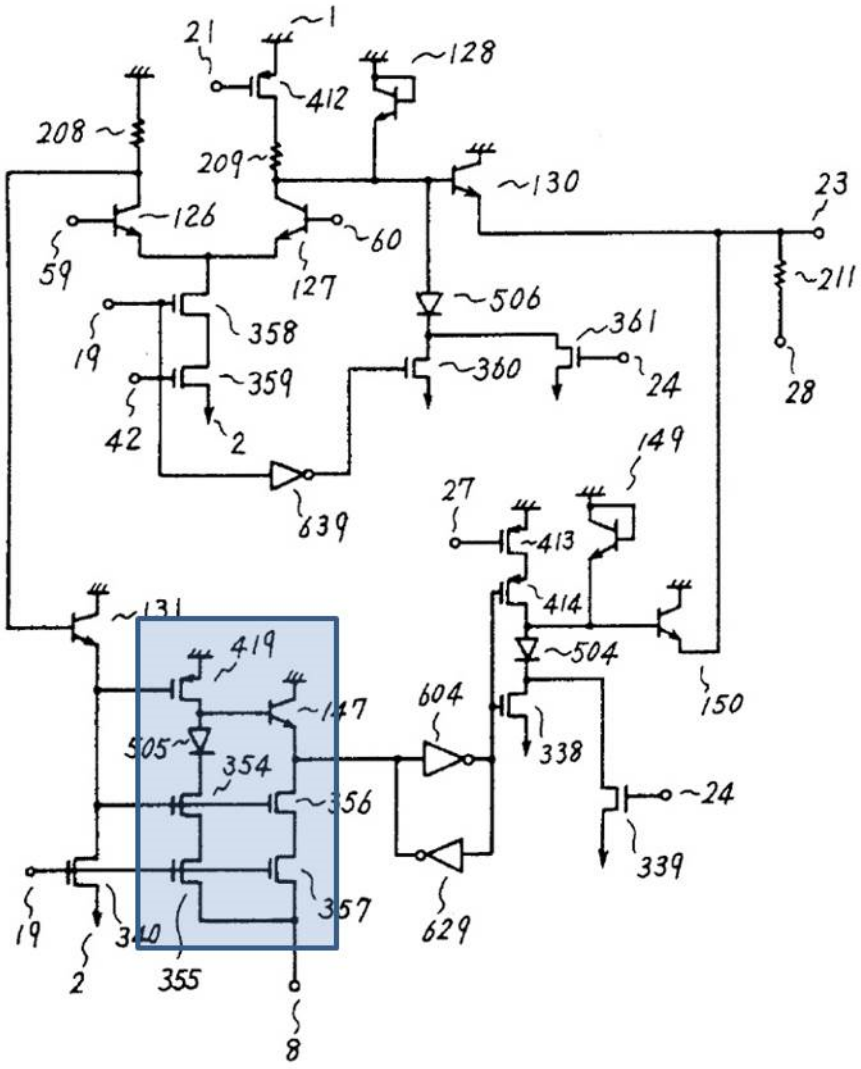

1
27
413
414
21
61
208
209
62
130
23
126
412
146
59
60
127
504
211
20
390
129
28
210
338
19
24
391
339
602
2
626
25
131
419
147
505
340
356
354
357
604
629
355
8

FIG. 17



Accordingly, Tachibana discloses level converting the differential output (using the ECL-MOS level conversion circuit) to produce a level converted signal (the output of the ECL-MOS level conversion circuit).

10.9.4. [14.3] "detecting a change in impedance at an input of a clock-free latch and latching the level converted signal at the clock-free latch to produce the latched digital signal; and"

Tachibana discloses this limitation. As discussed in connection with claim [5.0], when the ECL-MOS level conversion circuit is in a high impedance state due to signal 19 being low, inverters 604 and 629 continue to latch the level converted signal value that they received from the ECL-MOS level conversion circuit in the previous read operation. Ex. 1005, pp. 111-112; *see also* claim [5.0]. When signal 19 switches to high, the ECL-MOS level conversion circuit switches to a low impedance state and provides a new level converted signal to inverters 604 and 629, which then latch the new value. *See* claim [5.0]. Ex. 1003, A47.

Accordingly, Tachibana discloses detecting a change in impedance (detecting when the ECL-MOS level conversion circuit changes from the high impedance state to the low impedance state) at an input of a clock-free latch (inverters 604 and 629) and latching the level converted signal at the clock-free latch to produce the latched digital signal.

10.9.5. [14.4] "outputting the latched digital signal."

Tachibana discloses this limitation. As discussed in connection with claim 8, Tachibana discloses, in Figures 15 and 17, a module that receives the output of the latch circuit (comprised of inverters 604 and 629), and outputs it on terminal 23. *See* claim [8.0]. Ex. 1003, A48.

FIG. 15

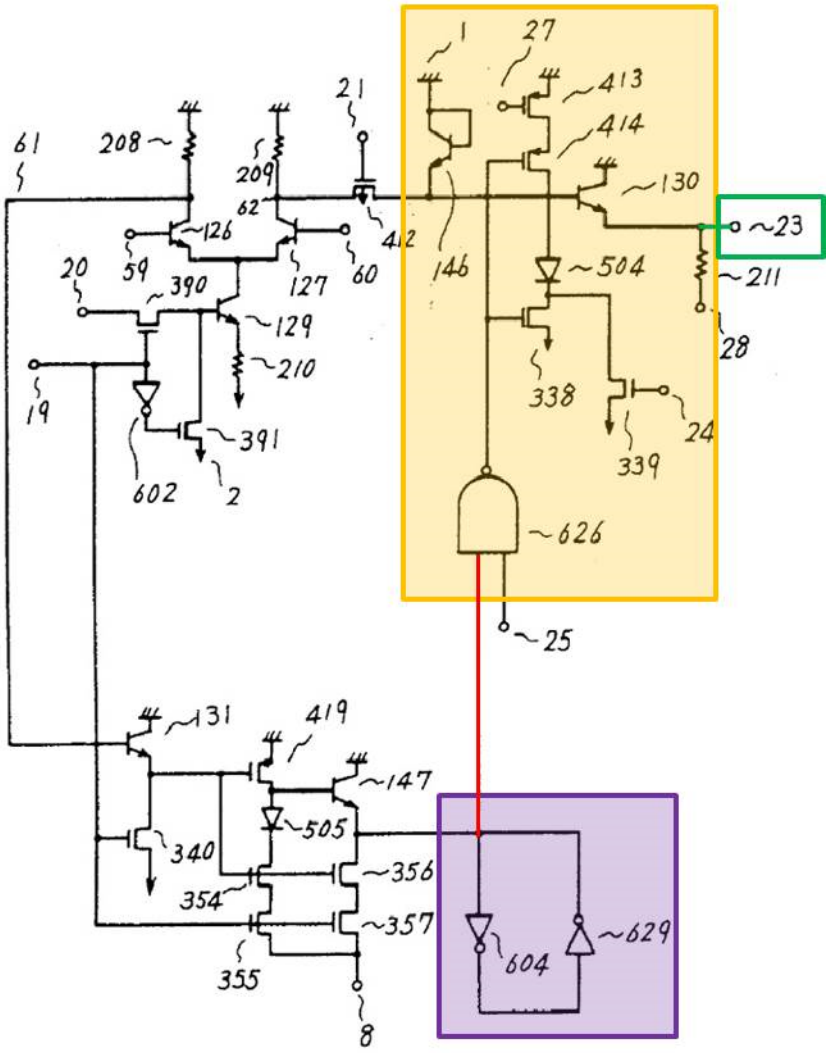
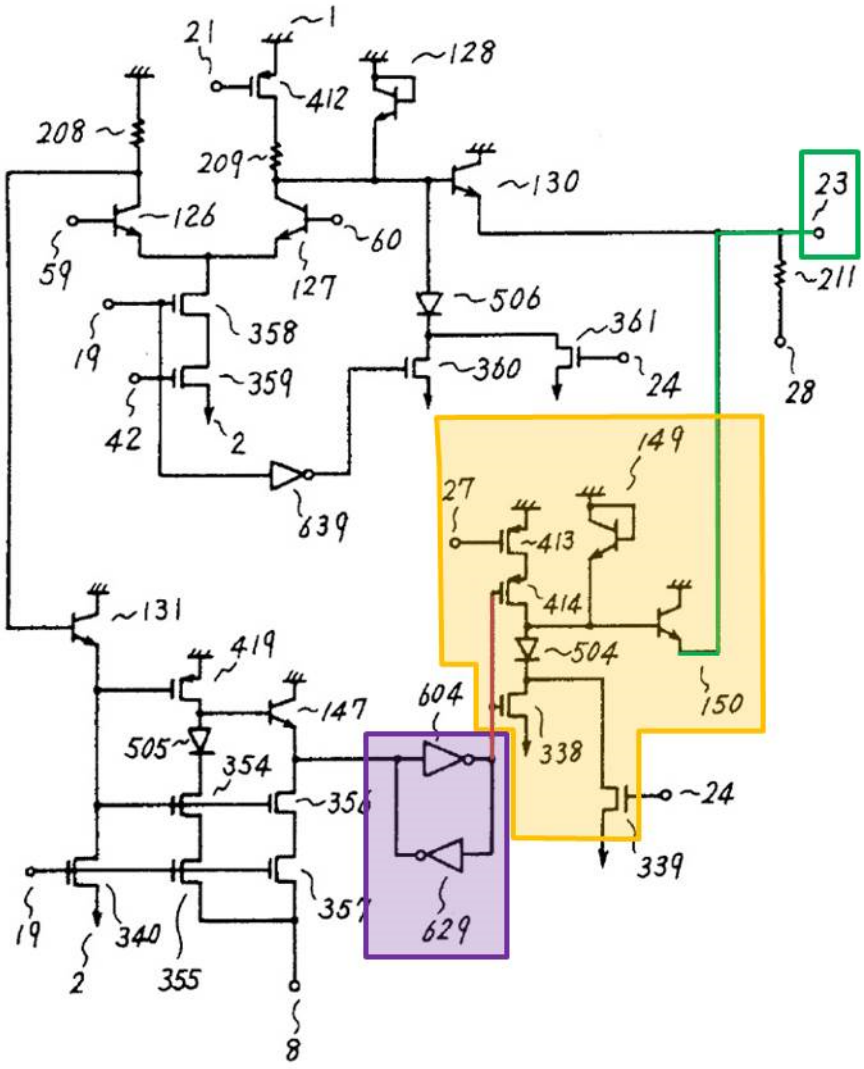

1
27
413
414
130
23
21
61
208
209
62
126
412
146
504
211
28
20
59
390
127
60
129
210
338
24
19
391
339
602
2
626
25
131
419
147
505
340
356
354
357
629
604
355
8

FIG. 17



Accordingly, Tachibana discloses outputting the latched digital signal.

10.10. Tachibana Anticipates Claim 15

10.10.1. [15.0] "The method of claim 14, further comprising the step of providing the level converted signal to the clock-free latch."

As discussed in Section 10.9, Tachibana discloses the method of claim 14.

Tachibana further discloses providing the level converted signal to the clock-free latch. As discussed in connection with claim [1.5], the output of the ECL-MOS level conversion circuit in Figures 15 and 17 (*i.e.*, the level converted signal) is provided as an input to inverters 604 and 629 (*i.e.*, the clock-free latch), as shown below. *See also* claim [1.5]. Ex. 1003, A48.

FIG. 15

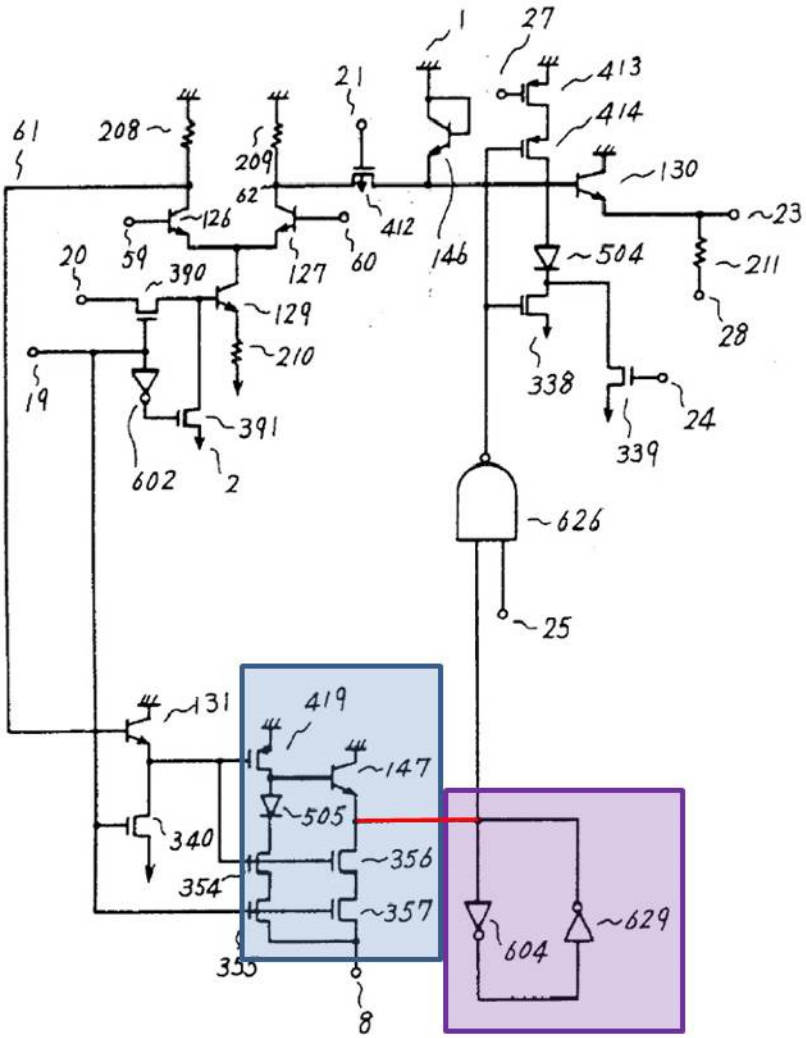
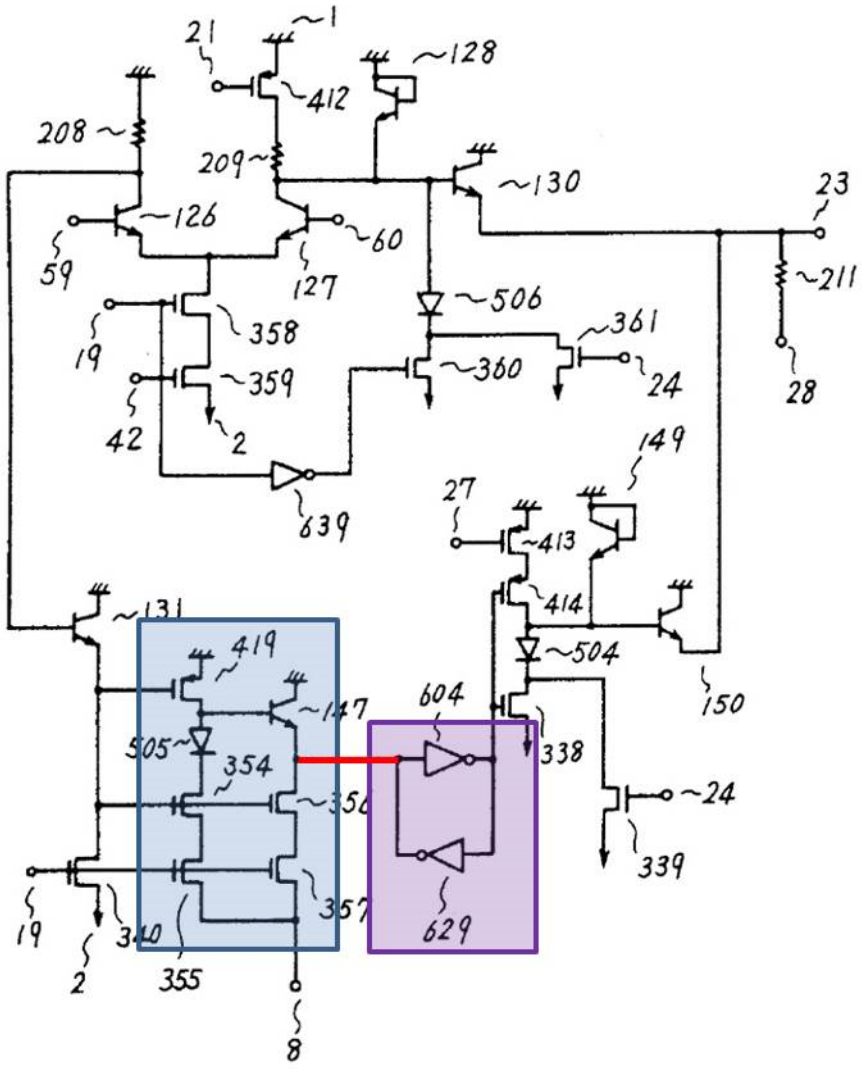


FIG. 17



10.11. Tachibana Anticipates Claim 16

10.11.1. [16.0] "The method of claim 14, further comprising the step of buffering the latched digital signal to produce an output signal."

As discussed in Section 10.9, Tachibana discloses the method of claim 14.

Tachibana further discloses buffering the latched digital signal to produce an output signal. As discussed in connection with the preamble of claim 1, Tachibana

discloses that the circuits shown in Figures 15 and 17 act as the output buffer circuit 608 in Figure 10. *See* claim [1.P]. Indeed, the latch comprised of inverters 604 and 629 itself buffers the signal. *See* Ex. 1011, p. 5 (explaining that a latch is "also called a buffer"); Ex. 1012, pp. 6-7, (explaining that in a latch, "the values on the input wires is buffered upon occurrence of some event, such as a clock pulse or riding edge of a separate latch signal"); Ex. 1003, A48. Accordingly, a POSA would have understood Tachibana to disclose that the circuits in Figures 15 and 17 buffer the digital signal latched by inverters 604 and 629 in order to produce the signal that is output on terminal 23. Ex. 1003, A48-A49.

10.12. Tachibana Anticipates Claim 20

10.12.1. [20.P] "A method of amplifying a signal to produce a latched digital signal, the method comprising the steps of:"

To the extent that the preamble is a limitation, this limitation is identical to limitation [14.P] and is disclosed by Tachibana for the same reasons discussed above. *See* claim [14.P]. Ex. 1003, A49.

10.12.2. [20.1] "amplifying and level converting a differential input to produce a level converted signal in response to a clock signal;"

This limitation is merely the union of limitations [14.1] and [14.2], and is disclosed by Tachibana for the same reasons discussed above for limitations [14.1] and [14.2]. *See* claim [14.1], [14.2]. Ex. 1003, A49.

10.12.3. [20.2] "detecting a change in impedance at an input of a clock-free latch and latching the level converted signal at the clock-free latch to produce the latched digital signal; and"

This limitation is identical to limitation [14.3] and is disclosed by Tachibana for the same reasons discussed *supra*. *See* claim [14.3]. Ex. 1003, A49.

10.12.4. [20.3] "outputting the latched digital signal."

This limitation is identical to limitation [14.4] and is disclosed by Tachibana for the same reasons discussed *supra*. *See* claim [14.4]. Ex. 1003, A49.

10.13. Tachibana Anticipates Claim 21

10.13.1. [21.P] "A memory device comprising:"

To the extent the preamble is a limitation, Tachibana discloses this limitation. Tachibana, in Figure 10, discloses a BiCMOS memory, which is a memory device. Ex. 1005, p. 117; Fig. 10. Ex. 1003, A49.

10.13.2. [21.1] "a bit cell array;"

Tachibana discloses this limitation. Tachibana discloses a memory cell array 606 in Figure 10, which is a bit cell array. Ex. 1005, Fig. 10. Ex. 1003, A50.

10.13.3. [21.2] "an amplifier module responsive to the bit cell array; and"

Tachibana discloses this limitation. Tachibana discloses a sense amp 607 in Figure 10. A POSA would have understood this to disclose an amplifier module, because a sense amp is a circuit whose purpose is to sense the signals from the

bitlines of a memory array and amplify them to recognizable logic levels. Ex. 1003, A50.

Tachibana also discloses that the sense amp 607 receives the output of memory cell array 606, thus disclosing that the sense amp 607 is responsive to the memory cell array 606 (*i.e.*, the bit cell array). Ex. 1003, A50.

10.13.4. [21.3] "an output stage responsive to the amplifier module, the output stage comprising:"

Tachibana discloses this limitation. Tachibana discloses an output buffer circuit 608, which is an output stage of the BiCMOS memory. Ex. 1005, p. 117; Fig. 10. Tachibana discloses that output buffer circuit 608 is the output buffer circuit of Figure 1. *Id*., p. 117. Further, Tachibana also discloses that Figures 15 and 17 are circuits that provide "the same operation as" the circuit in Figure 1. *Id*., pp. 119-120. Thus, Tachibana discloses that the circuits in Figures 15 and 17 are also output stages for a BiCMOS memory. Ex. 1003, A50.

Figure 10 further discloses that the output buffer circuit receives the output of sense amp 607, and is therefore responsive to the sense amp 607. Ex. 1003, A50.

Accordingly, Tachibana discloses an output stage (the circuits in Figures 15 and 17, serving as output buffer circuit 608) responsive to the amplifier module (sense amp 607).

10.13.5. [21.4] "a differential amplifier responsive to a clock signal;"

Tachibana discloses this limitation. Tachibana discloses a differential amplifier for the reasons discussed in connection with claim [1.2]. *See* claim [1.2].

Tachibana discloses that the level of the signal on terminal 19 affects the level of output signals 61 and 62 of the differential amplifiers in Figures 15 and 17. When 19 is at low-level potential, "the potential of terminal 61 attains the GND terminal's potential of 0 V." Ex. 1005, p. 111. When 19 is at high-level potential, it causes "the potential of terminal 62 to attain the low level and the potential of terminal 61 to attain the high level." *Id*., p. 113. Tachibana further discloses that terminal 19 is a "clock signal terminal[]." *Id*., p. 111. Ex. 1003, A50.

Accordingly, Tachibana discloses a differential amplifier (the differential amplifier in Figures 15 and 17) responsive to a clock signal (the signal on clock signal terminal 19).

10.13.6. [21.5] "a high impedance control circuit;"

Tachibana discloses this limitation. Tachibana discloses an impedance control circuit, PMOS transistor 412, for the reasons discussed in connection with

limitation [1.3][9]. *See* claim [1.3]. This impedance control circuit is a *high* impedance control circuit because Tachibana discloses that "PMOS transistor 412 is an element that serves to set the impedance of output element 62 of differential amplification circuit 622 to high impedance in the data held state. In the data held state, PMOS transistor 412 is in the non-conducting state, so setting the output impedance of output terminal 62 of differential amplification circuit 622 to high impedance causes differential amplification circuit 622 to cease to affect the potential of terminal 62." Ex. 1005, p. 112. Ex. 1003, A50.

10.13.7. [21.6] "a level converter responsive to the differential amplifier and responsive to the high impedance control circuit; and"

Tachibana discloses this limitation for the same reasons discussed in connection with limitation [1.4]. *See* claim [1.4]. Ex. 1003, A51.

10.13.8. [21.7] "a clock-free latch responsive to the level converter."

This limitation is identical to limitation [1.5] and is disclosed by Tachibana for the same reasons discussed *supra*. *See* claim [1.5]. Ex. 1003, A51.

[9] Additionally, transistor 340 in Figures 15 and 17 is a high impedance control circuit because it controls the impedance of the ECL-MOS level conversion circuit. Ex. 1003, A15.

11. GROUND #2: CLAIMS 4-7 ARE UNPATENTABLE AS OBVIOUS OVER TACHIBANA IN VIEW OF THE KNOWLEDGE OF A POSA

11.1. Tachibana in view of a POSA's Knowledge Renders Claim 4 Obvious

11.1.1. [4.0] "The apparatus of claim 1, wherein the timing circuit receives a clock signal."

For the reasons discussed in Section 10, Tachibana discloses the apparatus of claim 1.

As discussed above, Tachibana's timing circuit is shown in Figures 8 and 9:

FIG. 8

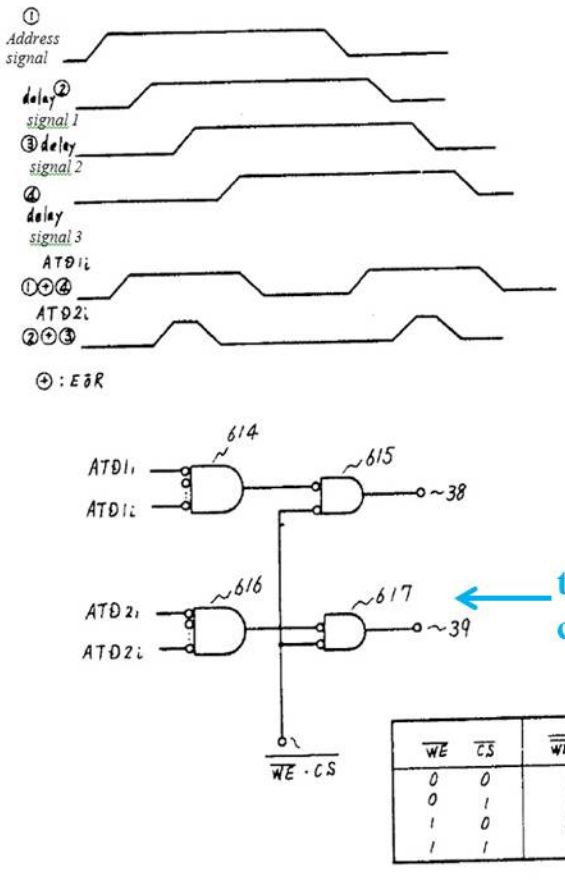
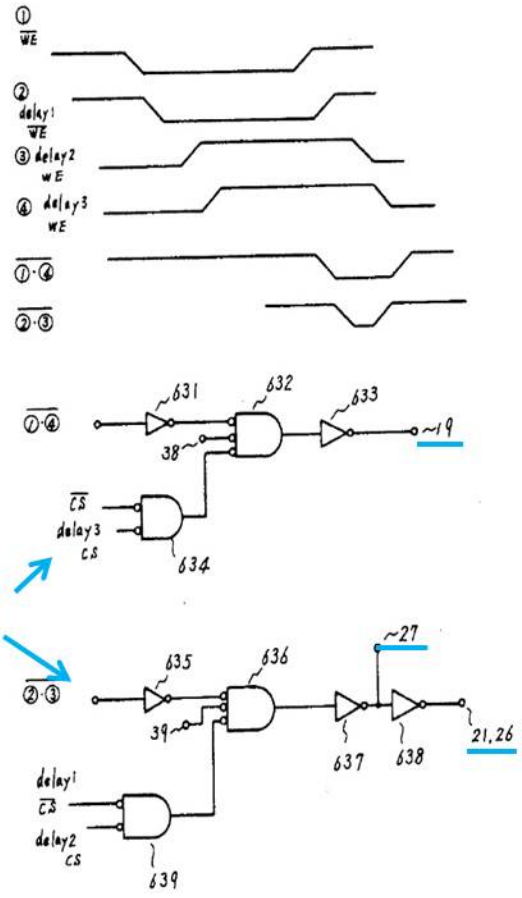


FIG. 9



See also claim [1.1]. Tachibana further describes the use of this circuit "for generating an ATD[10] signal with a different pulse width and delay time of the kind shown in FIG. 2 and FIG. 5," which includes signals 19, 21, 26, and 27. Ex. 1005, pp. 116-117. Tachibana also discloses, in Figure 10, an ATD signal generation circuit 620. *Id*., p. 117, Fig. 10. In view of Tachibana's description of using the circuit from Figures 8 and 9 to generate "an ATD signal," as well as Tachibana's description that Figure 10 illustrates "a BiCMOS memory using the output buffer circuit in FIG. 1," a POSA would have understood ATD signal generation circuit 620 to correspond to the circuit shown in Figures 8 and 9. *Id*., pp. 116-117. Ex. 1003, B1. Tachibana further discloses that the control signals generated by ATD signal generation circuit 620 can be generated either from an address signal or, "if there is a standard clock, for instance in the case of STRAM, it goes without saying that a control signal can easily be generated from the standard clock." Ex. 1005, p. 117. Ex. 1003, A1.

It was well-known in the prior art for timing circuits to receive clock signals from which to generate timing signals for controlling the operation of semiconductor memory devices. For example, STRAM—which is expressly

[10] "ATD" in this field of art refers to "address transition detection." *See, e.g.*, Ex. 1013, 2:56-65.

referenced in Tachibana, and refers to synchronous or "self-timed" RAMs (*see, e.g.*, Ex. 1014, 2:60-64)—routinely used external clock signal to generate internal control signals for reading and writing. *See, e.g.*, Ex. 1015, Figs. 4, 5, 8-11; 4:9-28, 6:59-7:66; Ex. 1016, Figs. 1, 3-11; 1:61-2:20; 4:12-49, 5:31-6:44; Ex. 1017, Figs. 1-6; Abstract; 3:36-5:15; Ex. 1018, Figs. 1, 2, 23, 25, 32, 34, 36, 40-44, 48-50, 53-60, 65, 67-74, 77-79, 81-93. Ex. 1003, A1-A2.

For the reasons discussed in Section 11.5, *supra*, it would have been obvious to a POSA to adapt Tachibana's timing circuit to receive a clock signal, as was well-known in the art, in order to use Tachibana's output stage in a synchronous memory device. Ex. 1003, B2.

Thus, Tachibana in view of the knowledge of a POSA discloses that the timing circuit (the circuit in Figures 8 and 9) receives a clock signal (the standard clock).

11.2. Tachibana in view of a POSA's Knowledge Renders Claim 5 Obvious

11.2.1. [5.0] "The apparatus of claim 4, wherein the clock-free latch performs a latching function in response to the level converter providing a modified impedance output."

For the reasons discussed in Section 11.1, Tachibana in view of a POSA's knowledge renders the apparatus of claim 4 obvious.

Tachibana in view of a POSA's knowledge further discloses this limitation. As discussed above, the latch in Figures 15 and 17 (comprised of inverters 604 and 629) performs its latching function solely in response to the output of the ECL-MOS level converter comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357. *See* claim [1.5]. Ex. 1003, B2. Further, in the "data held" state, the signal on terminal 19 is low, thereby preventing current flow to the differential amplifier and the ECL-MOS level converter, both of which take signal 19 as an input, as shown below. Ex. 1005, pp. 111-112. Ex. 1003, B2-B6.

FIG. 15

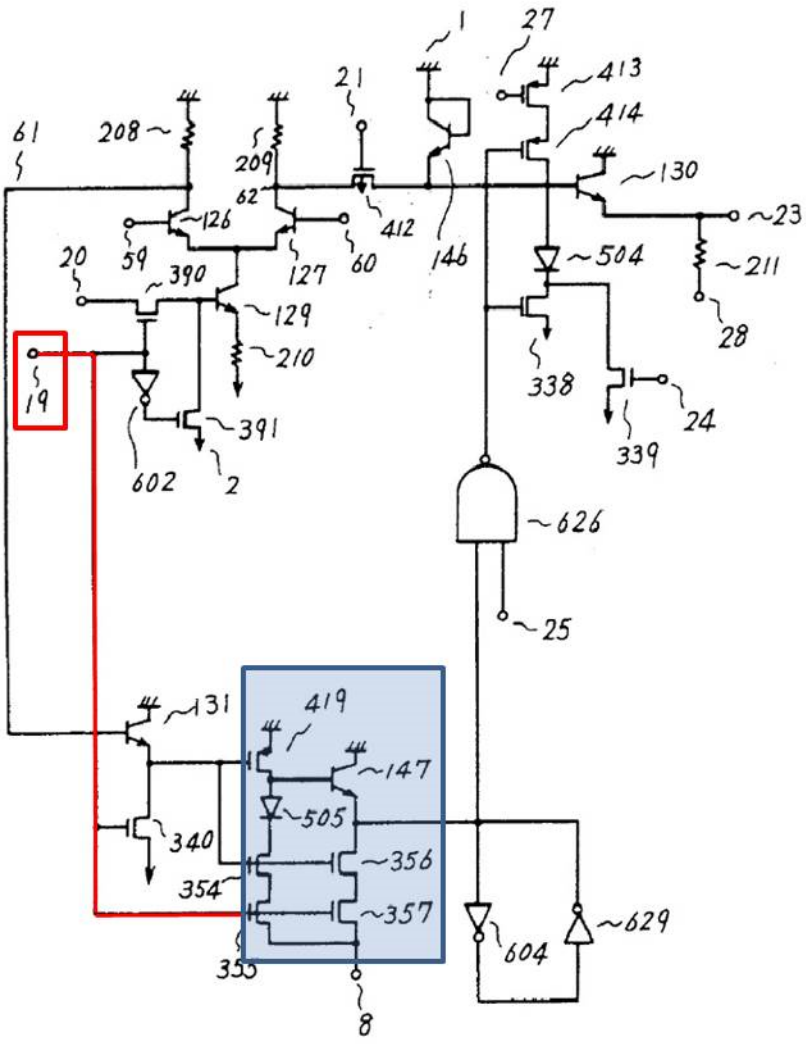
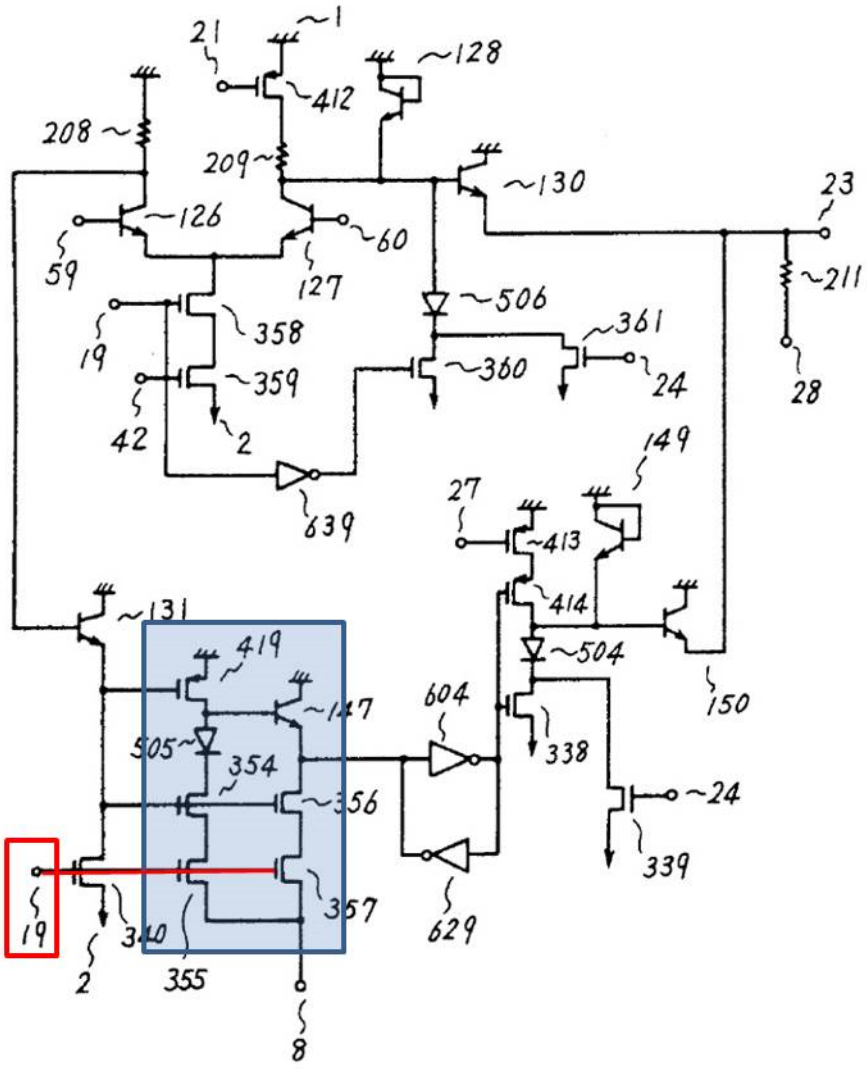

1
27
413
414
21
61
208
209
62
130
23
126
412
146
59
60
127
504
211
20
390
129
28
210
19
338
24
391
339
602
2
626
25
131
419
147
505
340
356
354
357
604
629
355
8

FIG. 17



Because the ECL-MOS level converter is not operational (*i.e.*, it is in a high impedance state), it does not output a new value into the latch comprised of inverters 604 and 629, thereby causing the latch to continue preserving the previously read value (*i.e.*, performing the latching function). When the ECL-MOS level converter becomes conductive as a result of signal 19 switching to the high level, ECL-MOS level converter passes the new output value from the

differential amplifier to the inverters 604 and 629, which latch the new value. Ex. 1003, B5-B6.

Accordingly, Tachibana in view of a POSA's knowledge discloses that the clock-free latch (comprised of inverters 604 and 629 in Figures 15 and 17) performs a latching function in response to the level converter (comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357) providing a modified impedance output (entering a high impedance state when signal 19 is low).

11.3. Tachibana in view of a POSA's Knowledge Renders Claim 6 Obvious

11.3.1. [6.0] "The apparatus of claim 5, wherein the level converter produces the modified impedance output in response to the clock signal."

For the reasons discussed in Section 11.2, Tachibana in view of a POSA's knowledge discloses the apparatus of claim 5.

Additionally, Tachibana in view of a POSA's knowledge discloses this limitation. As discussed in Section 11.2, Tachibana discloses that the ECL-MOS level conversion circuit enters the high impedance state (thereby producing a modified impedance output) in response to signal 19. *See* claim [5.0]. Ex. 1003, B6-B8. As discussed in Section 11.1, it would have been obvious to a POSA for Tachibana's timing circuit in Figures 8 and 9 to respond to a standard clock signal. *See* claim [4.0]. Ex. 1003, B8-B9. As shown in Figures 8 and 9, signal 19 to

which the ECL-MOS level conversion circuit responds is generated by the timing circuit in Figures 8 and 9. Ex. 1003, A3-A6. Accordingly, Tachibana in view of a POSA's knowledge discloses that the level converter (comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357) produces the modified impedance output (enters a high impedance state) in response to the clock signal (a standard clock).

11.4. Tachibana in view of a POSA's Knowledge Renders Claim 7 Obvious

11.4.1. [7.0] "The apparatus of claim 6, wherein the level converter produces the modified impedance output when first and second outputs of the differential amplifier have substantially the same voltage level indicating a modified impedance condition."

As discussed above, Tachibana in view of a POSA's knowledge renders obvious the apparatus of claim 6. *See* claim [6.0].

Tachibana in view of a POSA's knowledge further discloses this limitation. As discussed above, the ECL-MOS level conversion circuit in Figures 15 and 17 enters the high impedance state when signal 19 is at the low level. *See* claim [5.0]. Ex. 1003, B9. When signal 19 is low, "current does not flow to the differential amplifier comprised of bipolar transistors 126, 127, resistors 208, 209, and PMOS transistor 412." Ex. 1005, p. 111. As a result, outputs 61 and 62 of the differential amplifier (and their unlabeled equivalents in Figure 17) both have the ground voltage level, and the differential amplifier is set to output high impedance by

PMOS transistor 412. *Id*., pp. 111-12. Thus, when the first and second outputs of the differential amplifier both have the ground voltage level, it indicates that the differential amplifier is outputting high impedance and also that the ECL-MOS level conversion circuit is inactive and in the high impedance state. Ex. 1003, B9-B12.

Accordingly, Tachibana in view of a POSA's knowledge discloses that the level converter (comprised of bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357) produces the modified impedance (is in the high impedance state) when first and second outputs of the differential amplifier (outputs 61 and 62, and their unmarked equivalents in Figure 17) have substantially the same voltage level (ground voltage) indicating a modified impedance condition (set to output high impedance by PMOS transistor 412).

11.5. Motivations to Combine and Expectation of Success

It would have been obvious to a POSA to adapt Tachibana's timing circuit, disclosed in Figures 8 and 9, to accept a clock signal as an input for use in generating the internal timing and control signals for Tachibana's memory device. Tachibana provides an express teaching, suggestion, or motivation to do so, disclosing that "it goes without saying that a control signal can easily be generated from the standard clock" in instances where a clock signal is available. Ex. 1005,

p. 117; Ex. 1003, ¶70. A POSA would thus have been motivated by Tachibana to adapt the timing circuit in Figures 8 and 9 such that it could be used in clocked, or synchronous, memory devices. Ex. 1003, ¶72. Such devices were well-known in the art prior to the filing of the 274 Patent. *See, e.g.*, Ex. 1019, p. 25. In particular, they were known to be faster than asynchronous memory devices. *Id*. This was because synchronous devices are timed to the edges of the system clock, while asynchronous devices could experience internal timing delays as the various signals and inputs are established. *Id.* Thus, a POSA would have been motivated to adapt Tachibana's output buffer circuit—including the timing circuit from Figures 8 and 9—for use with synchronous memory devices by having the timing circuit accept a clock signal as an input, in order to gain the timing and speed benefits of such devices. Ex. 1003, ¶¶70-72.

A POSA would have had a reasonable expectation of success in doing so, because timing circuits for generating internal control and timing signals in synchronous memory devices were very well-known in the prior art. *See, e.g.*, Ex. 1015, Figs. 4, 5, 8-11; 4:9-28, 6:59-7:66; Ex. 1016, Figs. 1, 3-11; 1:61-2:20; 4:12-49, 5:31-6:44; Ex. 1017, Figs. 1-6; Abstract; 3:36-5:15; Ex. 1018, Figs. 1, 2, 23, 25, 32, 34, 36, 40-44, 48-50, 53-60, 65, 67-74, 77-79, 81-93; Ex. 1003, ¶¶73-74. Additionally, Tachibana itself expressly provides an expectation of success, because it explicitly discloses that "it goes without saying that a control signal can

easily be generated from the standard clock" using the signal generation circuit. Ex. 1005, p. 117; Ex. 1003, ¶75. Thus, it would have been a straightforward application of ordinary skill and knowledge for a POSA to implement a timing circuit that accepts a clock signal as an input. Ex. 1003, ¶75.

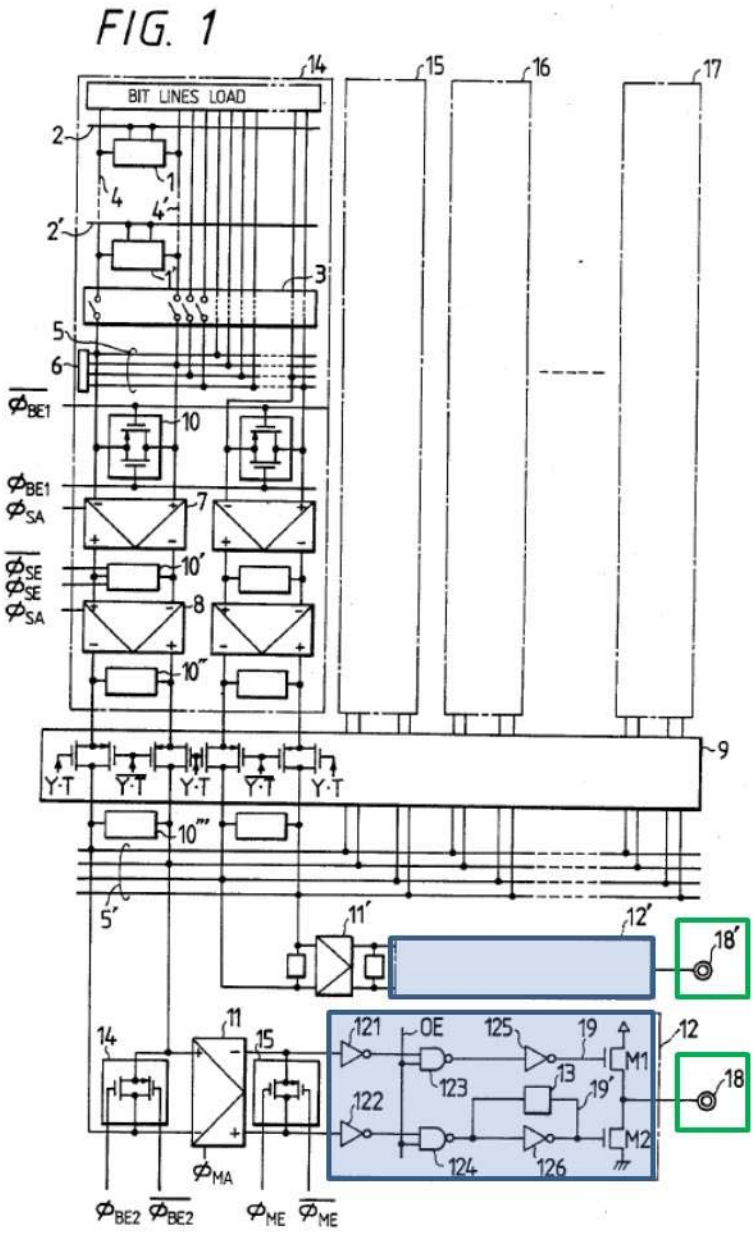
12. GROUND #3: CLAIMS 22 AND 23 ARE UNPATENTABLE AS OBVIOUS OVER TACHIBANA IN VIEW OF HANAMURA

12.1. Tachibana in View of Hanamura Renders Claim 22 Obvious

12.1.1. [22] The memory device of claim 21, further comprising a plurality of output stages and a plurality of data outputs.

For the reasons discussed above, Tachibana discloses the memory device of claim 21.

Hanamura further discloses a plurality of output stages and a plurality of data outputs. In Figure 1, Hanamura discloses a memory device comprised of four memory arrays 14, 15, 16, and 17, with memory array 14 having two output buffer circuits, 12 and 12', outputting to a respective outputs 18 and 18':



See also Ex. 1006, 5:25-45.

For the reasons discussed in Section 12.3, it would have been obvious to a POSA to apply Hanamura's teaching of multiple output stages and data outputs to Tachibana's output buffer circuit. Ex. 1003, C1-C3.

Accordingly, Tachibana in view of Hanamura discloses a plurality of output stages and a plurality of data outputs.

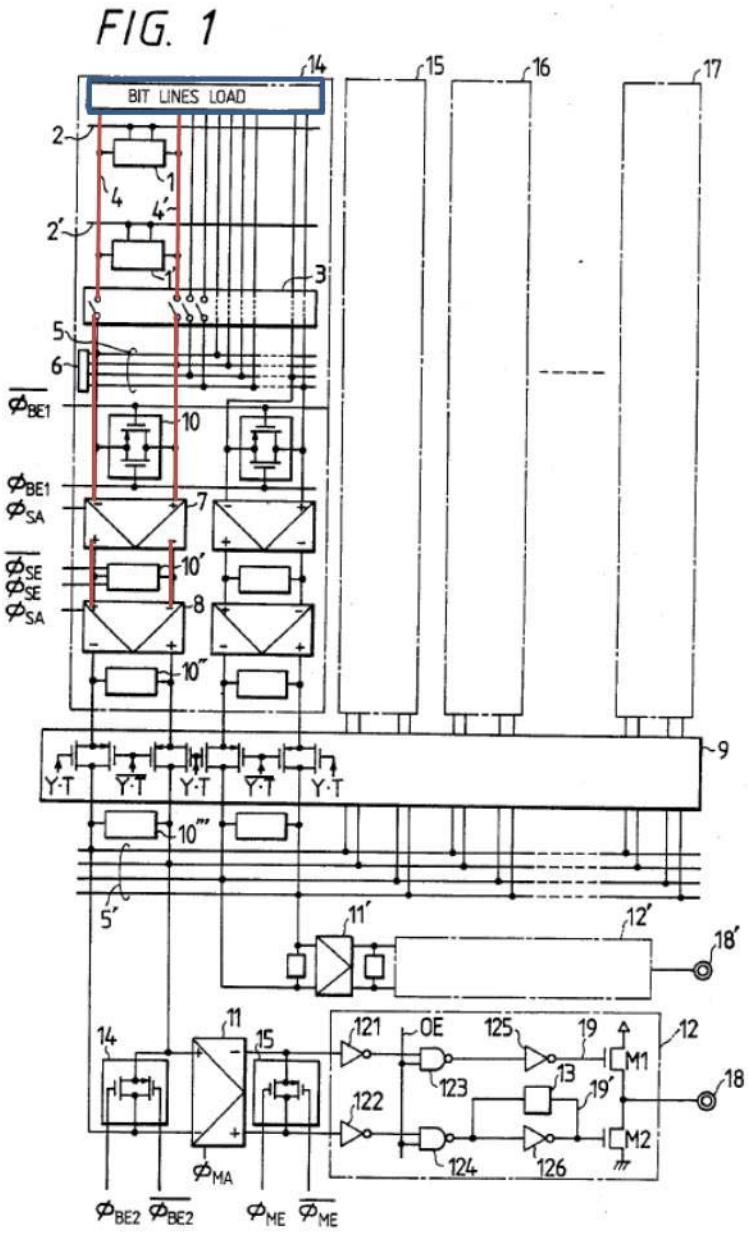
12.2. Tachibana in View of Hanamura Renders Claim 23 Obvious

12.2.1. [23] The memory device of claim 22, further comprising a bit line load array coupling the bit cell array and the amplifier module.

Tachibana in view of Hanamura discloses the memory device of claim 22 for the reasons discussed above.

Further, Tachibana in view of Hanamura discloses this limitation. First, Tachibana discloses in Figure 10 that its BiCMOS memory device includes a "data line load MOS transistor" 618 coupled to the memory cell array 606. Ex. 1005, Fig. 10, p. 117. In this context, "data line" is an alternative term for "bit line." *See, e.g.*, Ex. 1006, 1:25-29 (referring to a memory cell connected to a word line and a data line pair); Ex. 1003, C5. Thus, Tachibana discloses a bit line load array (the data line load MOS transistor 618) coupled to the bit cell array (memory cell array 606).

To the extent that Tachibana does not disclose that the data line load MOS transistor 608 couples the memory array 606 to the sense amp 607, Hanamura provides such a disclosure. Hanamura discloses a "bit lines load" structure that couples its memory array to sense amplifiers 7 and 8 via data lines 4 and 4':



For the reasons discussed in Section 12.3, it would have been obvious to a POSA to couple Tachibana's memory cell array 606 and sense amplifier 607 with a bit line load circuit, as taught in Hanamura. Ex. 1003, C3-C6.

Accordingly, Tachibana in view of Hanamura renders this limitation obvious.

12.3. Motivations to Combine and Expectation of Success

12.3.1. Including a plurality of output stages and a plurality of data outputs

It would have been obvious to a POSA to combine Tachibana's output buffer circuit with Hanamura's disclosure of a plurality of output stages and a plurality of data outputs. A POSA would have recognized that such a combination would allow faster memory accesses, which was generally recognized as a benefit for memory systems. *See, e.g.*, Ex. 1019, p. 21 ("Faster memories decrease the system access time also resulting in improved bandwidth"); Ex. 1003, ¶77. As shown in Hanamura, each column of memory cells in the memory array is coupled to a different output stage. Ex. 1006, Fig. 1; Ex. 1003, ¶78. Thus, for example, the output stage 12, which is coupled to the leftmost column of memory cells, could continue to latch the most recently read data value from that column, even while the output stage 12', which is coupled to the second column of cells, is actively reading out data stored in one of the cells in the second column. *See* Ex. 1006, Fig. 1. As a result, the previous data read from the leftmost column would still be available in the latch for output from data output 18. Similarly, when a new data read is taking place from cells in the leftmost column, the previously latched data from the second column would still be available for output from data output 18'. Ex. 1003, ¶78.

A POSA would have had a reasonable expectation of success in making this combination. First, the memory devices disclosed in Tachibana and Hanamura are structurally similar, each having a memory array (memory cell array 606 in Tachibana; memory array 14 in Hanamura) connected to sense amplifiers (sense amp 607 in Tachibana; sense amplifiers 7 and 8 in Hanamura) that output to output buffer circuits (output buffer circuit 608 in Tachibana; output buffer circuits 12 and 12' in Hanamura), which in turn output the data on a data output (output 23 in Tachibana; outputs 18 and 18' in Hanamura). Ex. 1005, Fig. 10; Ex. 1006, Fig. 1; Ex. 1003, ¶79. Additionally, both Tachibana and Hanamura disclose asynchronous memories (although, as noted above in connection with claim 4 and its dependents, Tachibana also renders obvious a synchronous system). *See, e.g.*, Ex. 1005, Figs. 5-10; Ex. 1006, Figs. 1, 2; Ex. 1003, ¶80. This structural and functional similarity would have given a POSA a reasonable expectation that using multiple instances of Tachibana's output buffer circuit, in the manner taught by Hanamura, would successfully result in a memory device capable of outputting to multiple parallel outputs. Ex. 1003, ¶81. Additionally, memory devices in which the output buffers output to multiple parallel data outputs were well-known and routine in the art. *See, e.g.*, Ex. 1020, Figs. 1-3 (disclosing data-out buffers outputting on a 4-bit parallel bus—indicated by the "4/" notation—to 4 parallel outputs DQ1 through DQ4); Ex. 1021, Fig. 25 (disclosing I/O Buffer outputting on a multiple-bit parallel

bus, indicated by the thick white arrow, to parallel I/O); Ex. 1003, ¶82. Because such parallel output paths were well-known and commonplace in the art, a POSA would have had a reasonable expectation of successfully implementing it in the combination of Tachibana with Hanamura. Ex. 1003, ¶83.

12.3.2. Coupling the bit cell array to the amplifier module using a bit line load array

It would have been obvious to a POSA to couple Tachibana's memory cell array to the sense amp using a bit line load array, as taught in Hanamura. A POSA would have found an express teaching, suggestion, or motivation in the prior art to do this, because coupling the memory array and sense amplifiers using the bit line load array in this manner permits precharging of the bit lines, which was well-known in the prior art to improve data access speeds and performance, and was therefore commonly practiced in prior art memory systems. *See, e.g.*, Ex. 1019, pp. 61, 92, 96; Ex. 1003, ¶85. It was well-known, for example, to set the potential of the bit lines to a predetermined level (typically halfway between the high and low logic levels), *i.e.*, "precharging," to avoid having to change the potential of the bit lines a large amount when a logic "1" is read out after a logic "0," for example (or vice versa). Ex. 1022, Abstract; 1:5-40; Ex. 1023, 1:48-59; Ex. 1019, p. 92; Ex. 1003, ¶85. Indeed, precharging the bit lines in memory devices was so beneficial that its common use in a variety of semiconductor memory devices was described in textbooks years prior to the filing of the 274 Patent. *See, e.g.*, Ex.

1019, pp. 31, 33, 37, 41, 43, 45, 51, 56, 57, 61, 64, 69, 75, 79, 82, 86, 90, 92, 94, 96, 104, 106, 107, describing p. 61, for example, that by 1985 "bit-line precharge was a familiar feature"); Ex. 1003, ¶85. Further, it was well-known to perform this precharging using bit line load circuitry. *See, e.g.*, Ex. 1019, pp. 96, 99; Ex. 1024, Abstract; Fig. 6; 5:35-62, 7:48-54; Ex. 1003, ¶86. Thus, a POSA would have been motivated to couple the memory array and the sense amplifiers using the bit line load array, as taught in Hanamura, to gain the well-known advantages of precharging, which is enabled by such a configuration. Ex. 1003, ¶87. Additionally, for the same reasons discussed above, this configuration would have been obvious because it involved the use of a known technique (precharging via bit line load circuitry), which was known to improve performance in a variety of memory devices, to improve a similar device (Tachibana's BiCMOS memory) in the same way. Ex. 1003, ¶88.

A POSA would have had a reasonable expectation of success in this combination, because as noted above, the use of bit line load circuitry to precharge bit lines in memory array was ubiquitous in the prior art, and extensively described in both patents and printed publications. Ex. 1003, ¶89. Additionally, Tachibana provides a reasonable expectation of success by expressly disclosing that its memory cell array is coupled to a "data line load MOS" 618, which a POSA would have understood to refer to a bit line load structure of the type disclosed in

Hanamura and the prior art. Ex. 1003, ¶90. Thus, a POSA would have reasonably expected that Tachibana's data line load MOS could successfully be coupled to the memory cell array and sense amplifiers using the conventional and routine configuration that was well-known in the art and taught in Hanamura. Ex. 1003, ¶¶89-90.

13. CONCLUSION

Petitioner respectfully requests that the Board institute an *inter partes* review and find claims 1-12, 14-16, and 20-23 of the 274 Patent unpatentable.

Respectfully submitted

Dated: April 27, 2018

By: 

Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73,604
Weil, Gotshal & Manges LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: 650-802-3000

CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 12,207 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 2010, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word 2010 in Times New Roman 14 point font.

Respectfully submitted,

WEIL, GOTSHAL AND MANGES LLP

Dated: April 27, 2018

By: 

Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73,604
Weil, Gotshal & Manges LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: 650-802-3000

CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with [37 C.F.R. § 42.105 and § 42.6(e)], that service was made on the Patent Owner as detailed below.

Date of service	April 27, 2018
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 5,943,274 with Micron's Exhibit List Power of Attorney Exhibits Ex. 1001 through Ex. 1027
Persons served	Patent Owner's Address of Record: NXP USA, Inc. Law Department 6501 William Cannon Drive West TX30/OE62 Austin TX 78735 Additional Addresses Known as Likely to Effect Service: North Star Innovations, Inc. 600 Anton Blvd., Suite 1350 Costa Mesa, CA 92626 Edward C. Flynn Cohen & Grace, LLC 105 Braunlich Drive, Suite 300 Pittsburgh, PA 15237 Robert W. Morris Eckert, Seamans, Cherin & Mellott, LLC 10 Bank St., Suite 700 White Plains, NY 10606

Dated: April 27, 2018

Jeremy Jason Lang
Lead Counsel for Petitioners
Registration No. 73,604