UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC d/b/a
ON SEMICONDUCTOR
Petitioner

v.

POWER INTEGRATIONS, INC.
Patent Owner

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Case No. Unassigned
Patent 7,239,119

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PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,239,119

TABLE OF CONTENTS

LIST OF EXHIBITS

1001	U.S. Patent No. 7,239,119 to Bäurle et al. ("the '119 Patent")
1002	Expert Declaration of Dr. R. Jacob Baker
1003	CV of Dr. R. Jacob Baker
1004	Japanese Unexamined Patent Application Publication JPA 2002-354801 by Yuu Hosoya ("Hosoya")
1005	English Translation of Hosoya
1006	U.S. Patent No. 6,294,904 to Hirst ("Hirst")
1007	U.S. Patent No. 4,479,174 to Cates ("Cates")
1008	U.S. Patent No. 5,694,305 to King et al. ("King")
1009	Declaration Regarding English Translation of Hosoya
1010	U.S. Patent No. 5,675,479 to Tani et al.
1011	U.S. Patent No. 5,390,101 to Brown
1012	U.S. Patent No. 6,713,995 to Chen
1013	U.S. Patent No. 4,013,925 to Tice
1014	U.S. Patent No. 4,586,120 to Malik et al.
1015	John O'Malley, Basic Circuit Analysis, McGraw-Hill 1992 (excerpt)
1016	Oxford American College Dictionary, G.P. Putnam Son's, 2002 (excerpt)

I. INTRODUCTION

Semiconductor Components Industries, LLC d/b/a ON Semiconductor ("ON Semiconductor" or "Petitioner") requests *inter partes* review ("IPR") under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq*. of Claims 26, 27, and 32 of U.S. Patent No. 7,239,119 ("'119 Patent").

Petitioner asserts that there is a reasonable likelihood that the challenged claims are unpatentable and requests review of, and cancellation of, the challenged claims under 35 U.S.C. §§ 102 and 103.

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices

Real Party in Interest: The real parties in interest are: (i) ON Semiconductor Corporation, (ii) Semiconductor Components Industries, LLC, doing business as ON Semiconductor, (iii) Fairchild Semiconductor International, Inc., (iv) Fairchild Semiconductor Corporation, (v) Fairchild (Taiwan) Corporation, and (vi) System-General Corporation.

Related Matters: The '119 Patent is subject to one pending lawsuit entitled *Power Integrations, Inc. v. ON Semiconductor Corporation et al*, No. 16-cv-06371-BLF (N.D. Cal.). Petitioner was first served with a complaint including the '623 Patent in the California Litigation on November 8, 2016. Petitioner notes that Patent Owner has not made proof of service with the Court as required by Fed.

R. Civ. P. 4(l)(1), and Petitioner reserves all arguments that the period provided in Section 315(b) does not begin to run until such proof of service is made pursuant to Fed. R. Civ. P. 4(l)(1).

Petitioner is concurrently filing Petitions for IPR against two additional patents held by Patent Owner (i.e., U.S. Patent Nos. 6,414,471 and 6,297,623). In addition, Petitioner previously filed petitions for IPR against other patents held by Patent Owner, including the following IPRs which have been decided or are still pending: IPR2016-00809 (Final Written Decision issued 9-22-2017); IPR2016-00995 (instituted); IPR2016-01589 (instituted); IPR2016-01590 (instituted); IPR2016-01592 (instituted); IPR2016-01594 (instituted); IPR2016-01595 (instituted); IPR2016-01597 (instituted); IPR2016-01600 (instituted).

Lead Counsel: Lead Counsel is Roger Fulghum (Reg. No. 39,678) and Back-up Counsel are Brian Oaks (Reg. No. 44,981), Nick Schuneman (Reg. 62,088), Brett Thompsen (Reg. No. 69,985), and Seth Lindner (Reg. No. 68,119), each of Baker Botts L.L.P.

Service Information: Baker Botts L.L.P., One Shell Plaza, 910 Louisiana Street, Houston, Texas 77002-4995; Tel. (713) 229-1234; Fax (713) 229-1522. Petitioner consents to service by electronic mail at: ONSemi_119IPR@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

B. Certification of Grounds for Standing

Petitioner certifies that the ’119 Patent is available for IPR. Petitioner is not barred or estopped from requesting IPR of the ’119 Patent.

C. Fees

The Office is authorized to charge any fees that become due in connection with this Petition to Deposit Account No. 02-0384.

III. OVERVIEW OF THE ’119 PATENT

A. Background of the Technology

The ’119 Patent relates to switched mode power supplies and, specifically, power supply controllers. Ex. 1001, Abstract. A switched mode power supply may include a switch coupled between a power supply input and an energy transfer element of the power supply. Ex. 1001, Abstract. A power supply controller may receive a feedback signal from an output of the power supply and turn on or off the switch in response to the feedback signal in order to regulate the output of the power supply. Ex. 1001, Abstract. A power supply controller may also include an oscillator that provides a signal that determines a maximum switching frequency of the switch. Ex. 1001, Abstract. The operation of switched mode power supplies, including regulating the output of a power supply in response to a feedback signal, was well-known in the art. Ex. 1002, ¶ 31; *see, e.g.*, Ex. 1010 & 1011.

Figure 1 of the ’119 Patent shows a block diagram of a switched mode

power supply. The power supply includes Controller **145**, Switch **120**, Feedback Signal **155**, and Energy Transfer Element **125**, configured in a "flyback" type output stage. Ex. 1001, Fig. 1, 2:30-31; Ex. 1002, ¶ 32.

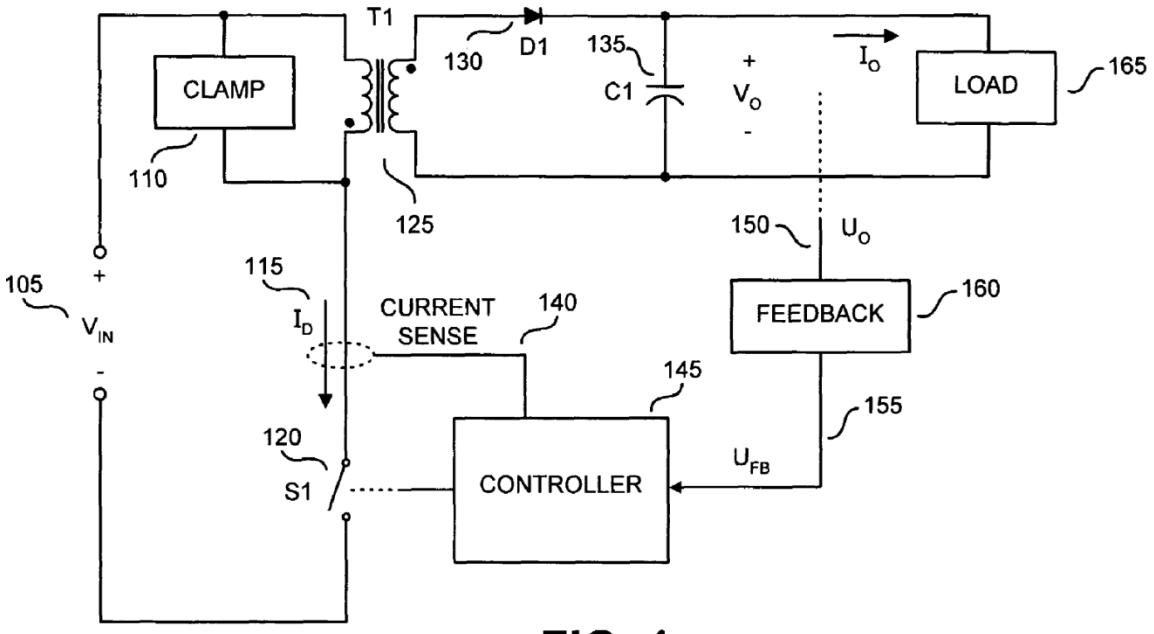


FIG. 1

Id., Fig. 1.

A switched mode power supply may regulate the amount of energy transferred from the input to the output of the power supply by modulating the duty cycle of the power switch (i.e., the ratio of the on-time of the switch to the overall period of each switching cycle). Ex. 1001, 3:7-11. The amount of power that may be delivered to a load connected to the output of a switching power supply is related to the switching frequency (how often the switch turns on and off) and the duty cycle. Ex. 1001, 4:18-38; Ex. 1002, ¶ 33.

B. Subject Matter of the '119 Patent

The specification of the '119 Patent notes that many types of electronic equipment use varying amounts of power during operation. Ex. 1001, 1:12-15. The specification also provides examples of specific devices, such as printers and DVD recorders, that require more power during brief periods of larger mechanical motion (like spinning a disk from startup to its rated speed) than they require during normal operation. Ex. 1001, 1:15-28. The '119 Patent purports to accommodate these types of high load events by temporarily increasing the maximum switching frequency of the switching regulator when an increased load demand is sensed. Ex. 1001, 3:11-16. The '119 Patent describes various methods for detecting an increase in load demand. Ex. 1001, 6:15-17. For example, Figure 7 illustrates an embodiment where load demand is determined via externally provided LOAD DEMAND signal 755. Ex. 1001, Fig. 7. Alternatively, load demand can also be determined based on measured circuit conditions. Ex. 1001, 6:17-27. Figure 8 illustrates an embodiment where load demand is determined based on a measurement of current through the primary switching transistor. *See* Ex. 1001, 6:28-7:1, Fig. 8; Ex. 1002, ¶ 34.

In response to detecting that the load has increased, the circuitry disclosed in the '119 Patent increases the maximum switching frequency of the primary switch controlling the power flow to the output. This increase in maximum switching

frequency can be discontinuous, jumping abruptly from one maximum to another (as illustrated in Figures 5A and 5B) or the increase can be continuous and gradual in response to the power requirements of the load (as illustrated in Figures 6A and 6B). Ex. 1001, 5:5-9, Figs. 5 & 6; Ex. 1002, ¶ 35.

Operating a switched mode power supply at higher switching frequencies based on higher loads was well-known in the art prior to the invention of the '119 Patent. Ex. 1002, ¶ 36. For example, U.S. Patent No. 5,675,479 to Tani et al. describes a switching power supply where the switching frequency is increased under heavy loads and decreased under light loads. Ex. 1010, Abstract. Similarly, U.S. Patent No. 5,390,101 to Brown discloses a switching power supply that includes a voltage controlled oscillator that continuously changes its switching frequency based on load conditions. *See* Ex. 1011. Other prior art references used discrete frequency settings triggered by the output of the power supply crossing a threshold voltage. *See, e.g.*, Ex. 1012; Ex. 1002, ¶ 36.

The concept of setting a limit on the amount of time a switching regulator may operate under peak loading conditions (i.e., when output current or voltage are high) was also well known in the art. Ex. 1002, ¶ 37. For example, each of U.S. Patent Nos. 4,013,925 to Tice and 4,586,120 to Malik disclose allowing temporary periods of high current prior to stopping the regulator. *See* Ex. 1013 & 1014; Ex. 1002, ¶ 37.

IV. SUMMARY OF PRIOR ART

A. Hosoya

Japanese Unexamined Patent Application Publication JPA 2002-354801 by Yuu Hosoya ("Hosoya") was published no later than December 6, 2002 (*see* Ex. 1005), and is prior art under 35 U.S.C. § 102(b). Hosoya was not considered during the prosecution. A declaration attesting to the accuracy of the English translation of Japanese Unexamined Patent Application Publication JPA 2002-354801 by Yuu Hosoya is provided at Exhibit 1009, which incorporates therein copies of the English translation of Exhibit 1005 and the original Japanese language version of Japanese Unexamined Patent Application Publication JPA 2002-354801 by Yuu Hosoya.

Hosoya is directed to a switched mode power supply whose maximum switching frequency is increased or decreased upon detection of a heavy load or a light load, respectively. Ex. 1005, Abstract, ¶ 0016, Fig. 1. Much like the '119 Patent, Hosoya recognizes the need for a switched mode power supply that can handle peak current in, for example, the context of powering a CPU, while maintaining small component size. Ex. 1005, ¶ 0010; Ex. 1002, ¶ 39. Hosoya achieves this by increasing the switching frequency during times of peak current demand, which allows the transformer to remain small. Ex. 1005, ¶ 0010. Hosoya, like the '119 Patent, detects a heavy load based on a current measurement detected

through the primary switching transistor exceeding a predetermined threshold. Ex. 1005, ¶ 0008; Ex. 1002, ¶ 39. According to Hosoya, this technique serves to improve "miniaturization and load efficiency" of the power supply. Ex. 1005, Abstract, ¶ 0040.

B. Hirst

U.S. Patent No. 6,294,904 to Hirst ("Hirst") issued on September 25, 2001 (*see* Ex. 1006), and is therefore 102(b)-type prior art. Hirst was not considered during the prosecution of the '119 Patent.

Hirst is directed to a method of operating a switching power supply wherein the maximum switching frequency is increased or decreased upon detection of a heavy load or a light load, respectively. Ex. 1006, Abstract; Ex. 1002, ¶ 41. Hirst describes several different mechanisms for detecting the need for increased power, including monitoring the output voltage, monitoring the output current, or monitoring the duty cycle. Ex. 1006, Figs. 2, 3, and 4; Ex. 1002, ¶ 41. Hirst notes the need to maintain low power consumption during times of light loading while still being able to respond "on demand" to the need for full power. Ex. 1006, 2:37-41. Note also that although Hirst refers to the mode utilized during light loading as a "standby mode," the exemplary power level of 10 Watts discussed in Hirst is identical to what the '119 Patent says is typical for the "continuous moderate output power requirement" for a DVD player, which is well above the standby

output power requirement of 0.5 Watts. Ex. 1006, 4:52-55; Ex. 1001, 3:46-49; Ex. 1002, ¶ 41.

C. Cates

U.S. Patent No. 4,479,174 to Cates ("Cates") issued on October 23, 1984 (*see* Ex. 1007), and is therefore 102(b)-type prior art. Cates was not considered during the prosecution of the '119 Patent.

Cates is directed to a method of operating a switching power supply wherein the maximum switching frequency is increased or decreased upon detection of a heavy load or a light load, respectively. Ex. 1007, 1:39-45; Ex. 1002, ¶ 43. Cates detects high and low power requirements by monitoring either the input current or the output current, each of which is representative of "the power level at which the supply operates." Ex. 1007, 3:58-4:16, Figs. 1 & 2; Ex. 1002, ¶ 43. According to Cates, the techniques disclosed therein result in an improvement in efficiency. Ex. 1007, 5:20-35.

D. King

U.S. Patent No. 5,694,305 to King et al. ("King") issued on December 2, 1997 (*see* Ex. 1008), and is therefore 102(b)-type prior art. King was not considered during the prosecution of the '119 Patent.

King is directed to a switching power supply with time-based protection circuitry that limits the duration of switching when either a high current or high

voltage is detected. Ex. 1008, 2:37-4:19; Ex. 1002, ¶ 45.

V. CLAIM CONSTRUCTION

In an IPR, claims are given their "broadest reasonable construction in light of the specification." *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Technologies, LLC*, 793 F.3d 1268, 1275-78 (Fed. Cir. 2015). Thus, the words of the claim are given their plain meaning unless inconsistent with the specification. *See In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). The construction set forth below is provided for purposes of this IPR. A personal of ordinary skill in the art ("POSITA") would have an M.S. in Electrical Engineering or related field or a B.S. with at least two years of experience in designing power electronics. Ex. 1002, ¶ 47.

A. "Temporarily increasing a maximum switching frequency"

Claims 26 and 32 each recite "temporarily increasing a maximum switching frequency." A person of ordinary skill in the art (POSITA) would understand the phrase "temporarily increasing a maximum switching frequency" to mean that the maximum switching frequency is increased for a limited period of time (i.e., non-permanently). Ex. 1002, ¶ 48. The duration of the increased maximum switching frequency may be limited either by circuit conditions, such as a measurement related to the value of the load, or by a predetermined limit (e.g., a timer).

This construction is consistent with both the plain and ordinary meaning of the word "temporarily" and the embodiments in the '119 Patent specification. Ex.

1002, ¶ 49. The plain meaning of "temporarily" is "for a limited period of time" or "not permanently." Ex. 1016, 5. In other words, "temporarily increasing a maximum switching frequency" means that the maximum switching frequency is increased and that the increase is not permanent. The '119 Patent describes at least two different mechanisms for limiting the duration of the maximum switching frequency. First, the '119 Patent describes that the maximum switching frequency may be varied in response to the load. Ex. 1001, 4:56-61 (describing that "the maximum frequency is varied depending on the output power demand"), 6:45-53 (describing a frequency shift signal that takes one of two values and establishes two discrete switching frequencies), 3:12-15 ("one embodiment of the oscillator in controller **145** is configured to switch temporarily at a higher frequency to accommodate temporary peak load conditions. . . ."); *see also id.*, Figs. 5A/B, 6A/B, 7 and associated description; Ex. 1002, ¶ 49.

The '119 Patent also describes limiting the duration of the maximum frequency using an "optional time limit circuit." Ex. 1001, 7:1-14; Fig. 8. This time limit circuit provides a logic high signal when the peak mode signal 860 goes to a logic high level and then returns to a logic low level after the maximum permitted duration of peak load event has passed. *Id.*; Ex. 1002, ¶ 50.

Accordingly, based on the plain meaning of "temporarily" and the embodiments in the specification showing that duration the maximum switching

frequency increase is limited either by circuit conditions or (optionally) by a time limit circuit, "temporarily increasing a maximum switching frequency" should be construed to mean that the maximum switching frequency is increased for a limited period of time or non-permanently (regardless of the mechanism by which the time period is limited). Ex. 1002, ¶ 51.

VI. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Hosoya Anticipates Claims 26 and 27 Under 35 U.S.C. § 102

Hosoya discloses every limitation of Claims 26 and 27 and thus anticipates those claims under 35 U.S.C. § 102.

1. Claim 26

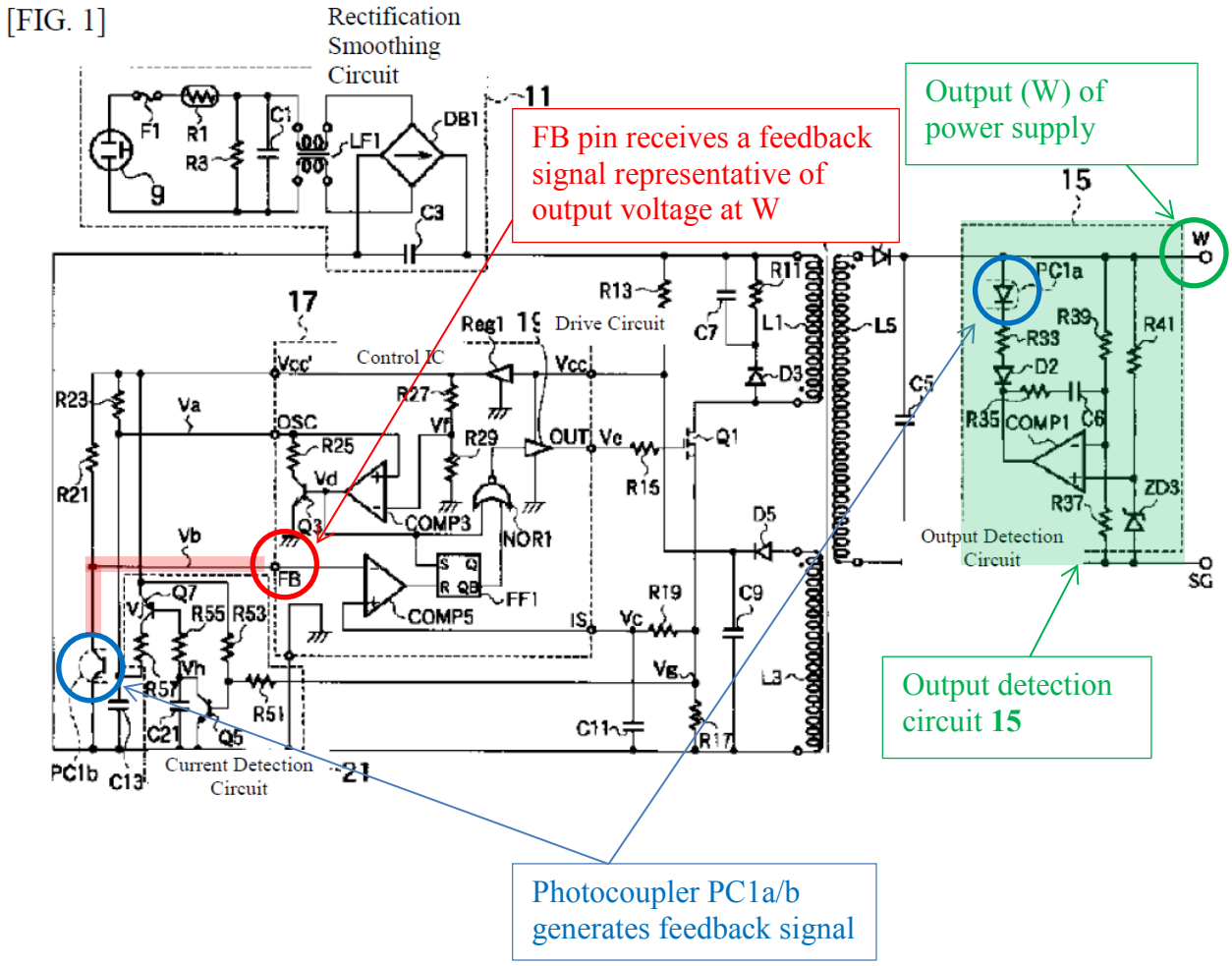
Claim 26[pre].[1] Hosoya discloses a method for regulating a power supply output. Ex. 1005, Abstract ("The present invention provides a switching power supply device that can reduce the operation frequency when at a certain power or below such as during normal operation or when at a light load, increase the operation frequency when at a high load such as when a transformer or the like reaches its limit, and contribute to the improvement of miniaturization and load efficiency."); Ex. 1002, ¶ 53. Figure 1 of Hosoya illustrates a "schematic

[1] Petitioner contends that the preambles of each of the challenged claims are non-limiting, but are nonetheless disclosed by the prior art.

configuration of the switching power supply device." Ex. 1005, ¶ 0016.

26[pre]. A method for regulating a power supply output, comprising:	**Hosoya:** Ex. 1005, Abstract: "The present invention provides a switching power supply device that can reduce the operation frequency when at a certain power or below such as during normal operation or when at a light load, increase the operation frequency when at a high load such as when a transformer or the like reaches its limit, and contribute to the improvement of miniaturization and load efficiency." *See also* Ex. 1005, ¶ 0016, Figs. 1 & 4.

Claim 26[a] receiving a feedback signal representative of an output level of a power supply output. The power supply disclosed in Hosoya uses a control scheme commonly known as current mode control to regulate output voltage W. Ex. 1005, Figs. 1 & 4; Ex. 1002, ¶ 54. The current mode control scheme in Hosoya regulates the duty cycle of the switching signal using two different feedback signals, one of which is representative of the output voltage and the other is representative of the output current. Ex. 1005, ¶ 0004, ¶ 0006, Fig. 1; Ex. 1002, ¶ 54.

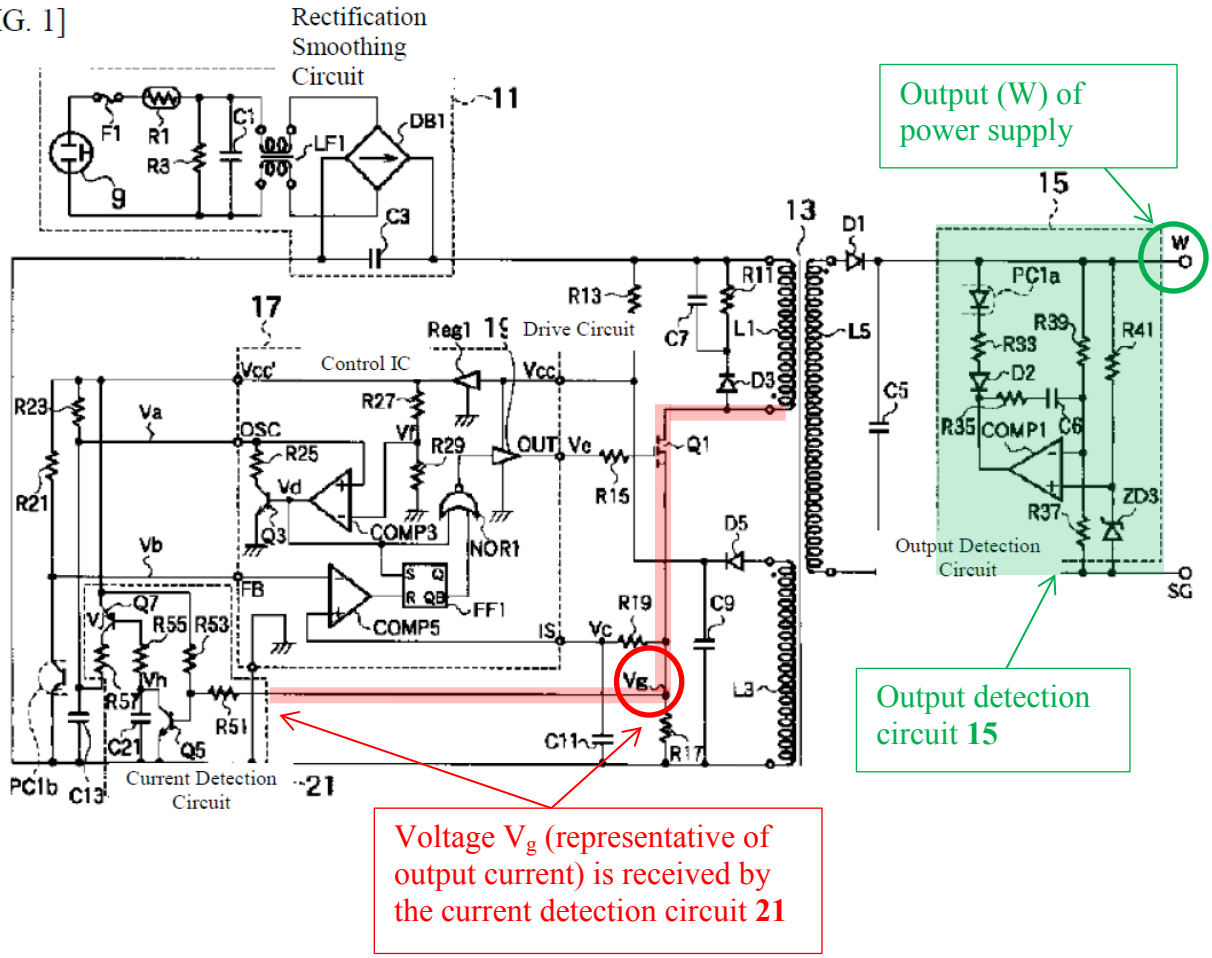


Ex. 1005, Fig. 1 (annotations added). First, Hosoya discloses an output detection circuit **15** that generates a feedback signal (FB) representative of the voltage at the power supply output W. Ex. 1005, ¶ 0004, Figs. 1 & 4. In particular, when the output voltage at W exceeds a predetermined value, the output detection circuit **15** emits light from the light emitting diode PC1a of a photocoupler, which then causes phototransistor PC1b to conduct current (through resistor R21). *Id.* Feedback signal FB, which is representative of the output voltage at W, is generated by the voltage drop across resistor R21. *Id.* Control IC 17 receives the

feedback signal at the FB pin. *Id.*; Ex. 1002, ¶ 54.

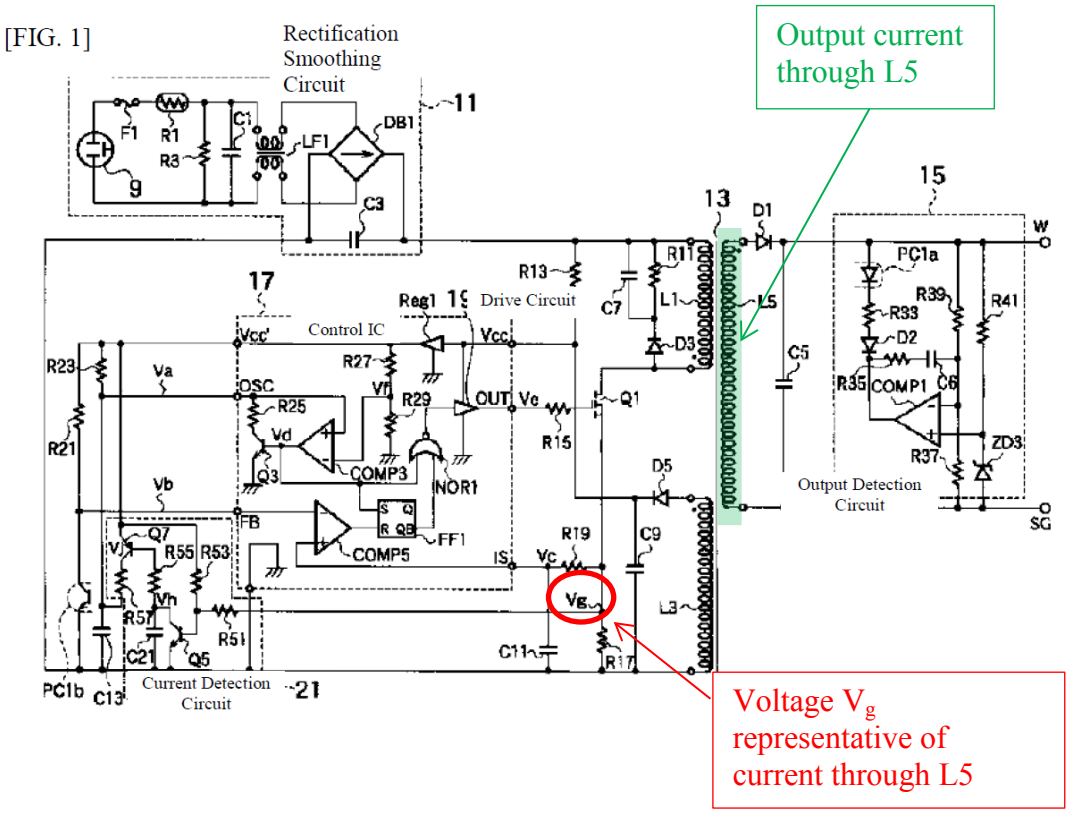
Additionally, Hosoya discloses a second feedback signal V_g used to control the behavior of the power supply. Ex. 1005, Fig. 1. Feedback signal V_g is a voltage that is proportional (based on the value of resistor R17) to the current through switch Q1 and the current through primary winding L1 of transformer **13**. Ex. 1005, ¶ 0006; Ex. 1002, ¶ 55.

[FIG. 1]



Ex. 1005, Fig. 1 (annotations added). V_g is also proportional to the current through secondary winding L5, which flows to the output W. This is because the current

through the primary and secondary windings (L1 and L5) of transformer **13** are proportional to each other based on the number of turns in the primary and secondary windings. Ex. 1002, ¶ 55; Ex. 1015, 8. It was well understood in the art that a measurement of the current through the primary winding of a transformer in a switching regulator is "representative of the power level at which the supply operates." *See* Ex. 1007, 3:66-4:4. Accordingly, Hosoya discloses receiving a feedback signal (i.e., V_g) representative of an output level (i.e., current) of a power supply output (i.e., node W).

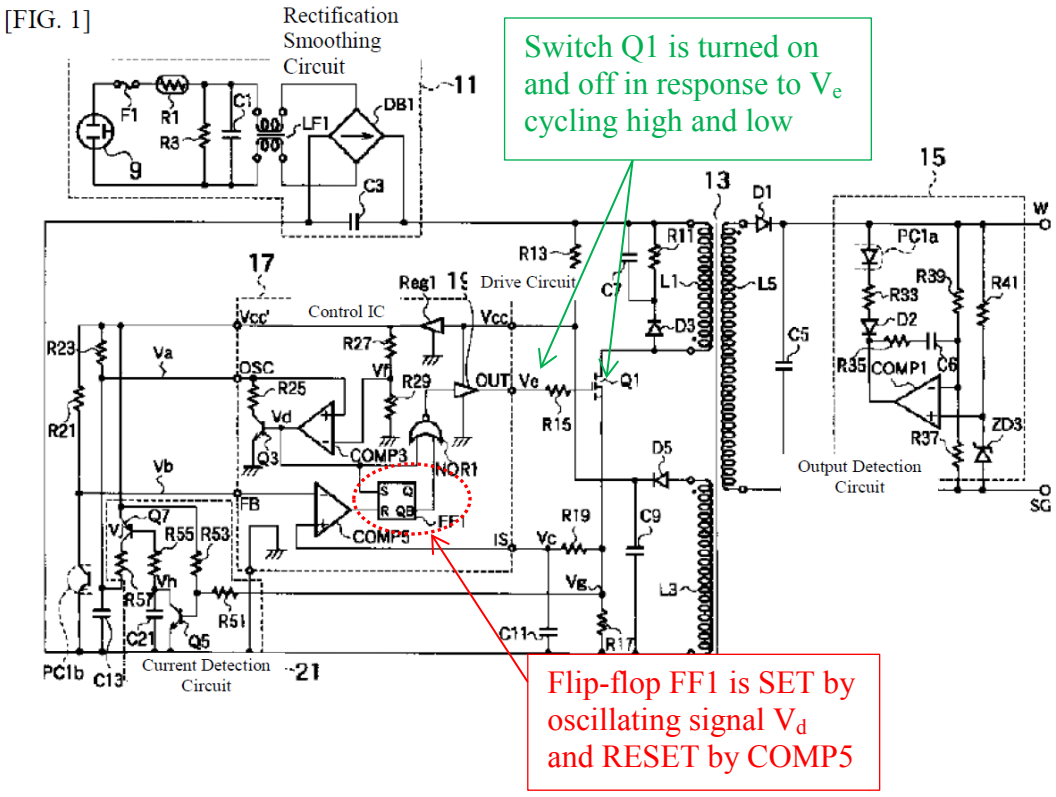


Ex. 1005, Fig. 1 (annotations added).

[26a] receiving a feedback signal representative of an output level of a power supply output;	**Hosoya:** Ex. 1005, ¶ 0004: "As the voltage that the output voltage divides by R39 and R37 becomes larger than a reference voltage as when at a light load, the output detection circuit 15 emits light from a light emitting diode PC1a of a photocoupler by outputting a low level from a comparator COMP1 based on the error signal thereof, and outputs a feedback signal to a phototransistor PC1b integrated with the light emitting diode PC1a. This signal is converted to a feedback signal FB by a resistor R21." Ex. 1005, ¶ 0013: "[A]n object of the invention described in claim 1 is to provide a current detection circuit that detects the size of current flowing into the switch element, and vary the frequency of the drive signal by superimposing current based on the output of a current detection circuit on charge or discharge current of a capacitor in a switching power supply device." *See* Ex. 1015, 8. *See also id.*, ¶ 0017, claim 1, Figs. 1 & 4.

Claim 26[b] switching a switch on and off at a switching frequency in response to the feedback signal to regulate the flow of energy from an input of the power supply to the power supply output.[2] Hosoya discloses regulating the flow of energy from an input to the output by turning on and off switch Q1. Ex. 1002, ¶ 56.

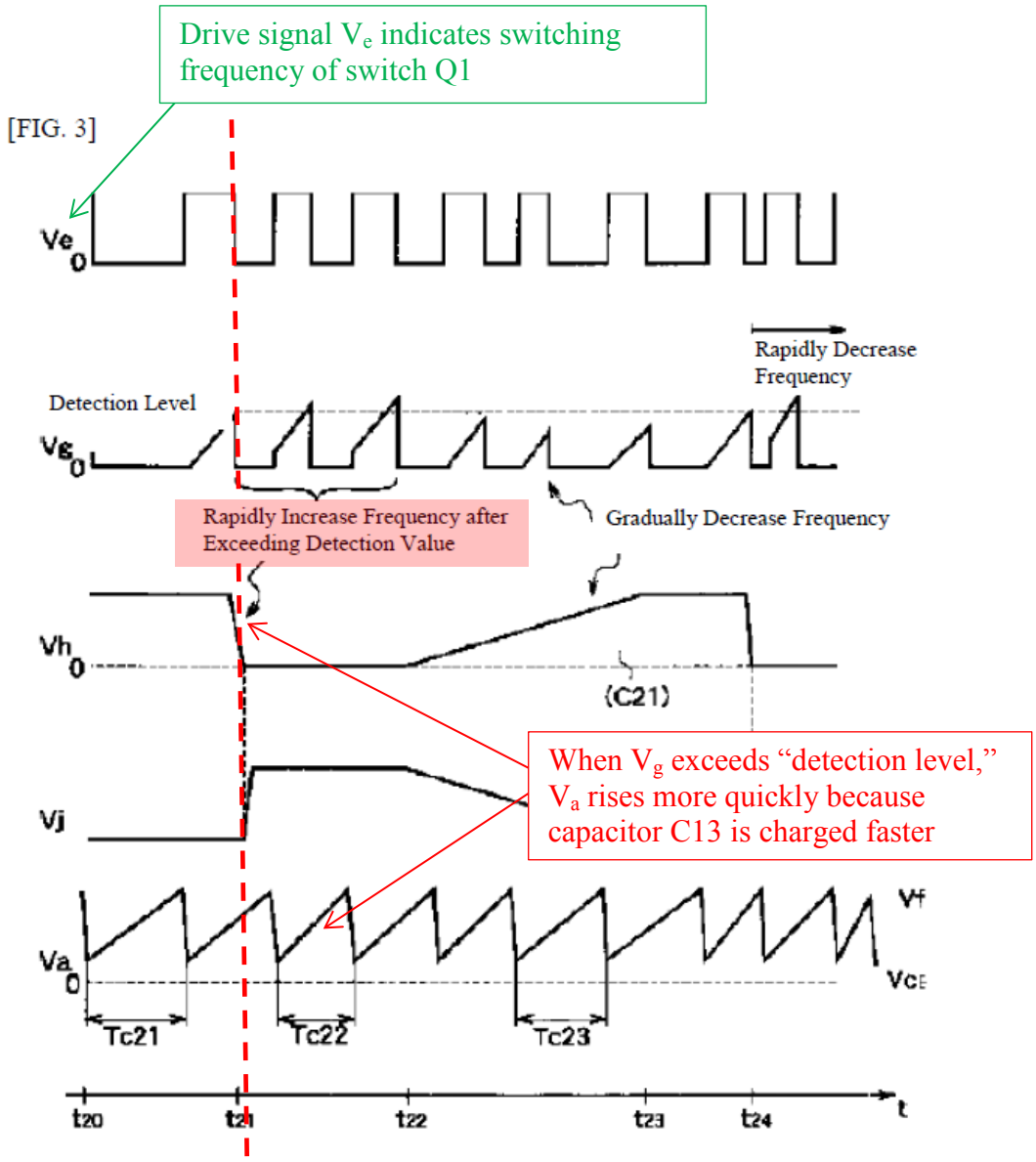
[2] The claim language is not clear as to whether the value of the switching frequency is "in response to the feedback signal," or alternatively, whether only "switching a switch on and off" must be "in response to the feedback signal." Hosoya satisfies the limitation under either interpretation.



Ex. 1005, Fig. 1 (annotations added). Hosoya describes that flip-flop FF1 is SET when the output of comparator COMP3 goes high (based on oscillation signal V_a, and RESET (by COMP5) when the voltage at the IS terminal exceeds the voltage at the FB terminal. Ex. 1005, ¶¶ 0006-0008. The output Qb of flip-flop FF1 is coupled to Drive Circuit **19**, which provides a high or low signal (V_e) to turn on or off switch Q1. Ex. 1005, ¶ 0009; Ex. 1002, ¶ 57. Accordingly, switch Q1 is turned on and off in response to both the output voltage (represented by the feedback signal FB) and the output current (represented by the voltage received at the IS pin). Ex. 1002, ¶ 57. Turning on and off switch Q1 regulates the flow of energy from an input of the power supply to the power supply output. Ex. 1005, ¶ 0003;

Ex. 1002, ¶ 57.

The switching frequency of switch Q1 varies based on the load at the output of the power supply. Ex. 1002, ¶ 58. As Hosoya describes, the switching frequency is determined by the oscillating sawtooth voltage V_a, which is charged by capacitor C13. Ex. 1005, ¶ 0022. During times of low loading, capacitor C13 charges and discharges at a steady rate. Ex. 1005, ¶ 5, Fig. 5; Ex. 1002, ¶ 58. When a high load current is detected (represented by a voltage at V_g above the threshold needed to turn on transistor Q5), Current Detection Circuit **21** acts to increase the charge current of capacitor C13. Ex. 1005, ¶ 0020-0021, Figs. 1 & 2. This causes C13 to charge more quickly, which in turn increases the frequency at which flip-flop FF1 is SET, and accordingly increases the switching frequency of switch Q1. Ex. 1005, ¶ 0014, 0017-0019. The relationship between feedback signal V_g and the switching frequency (shown by drive signal V_e) can be seen with reference to Figure 3 of Hosoya. Ex. 1002, ¶ 58.



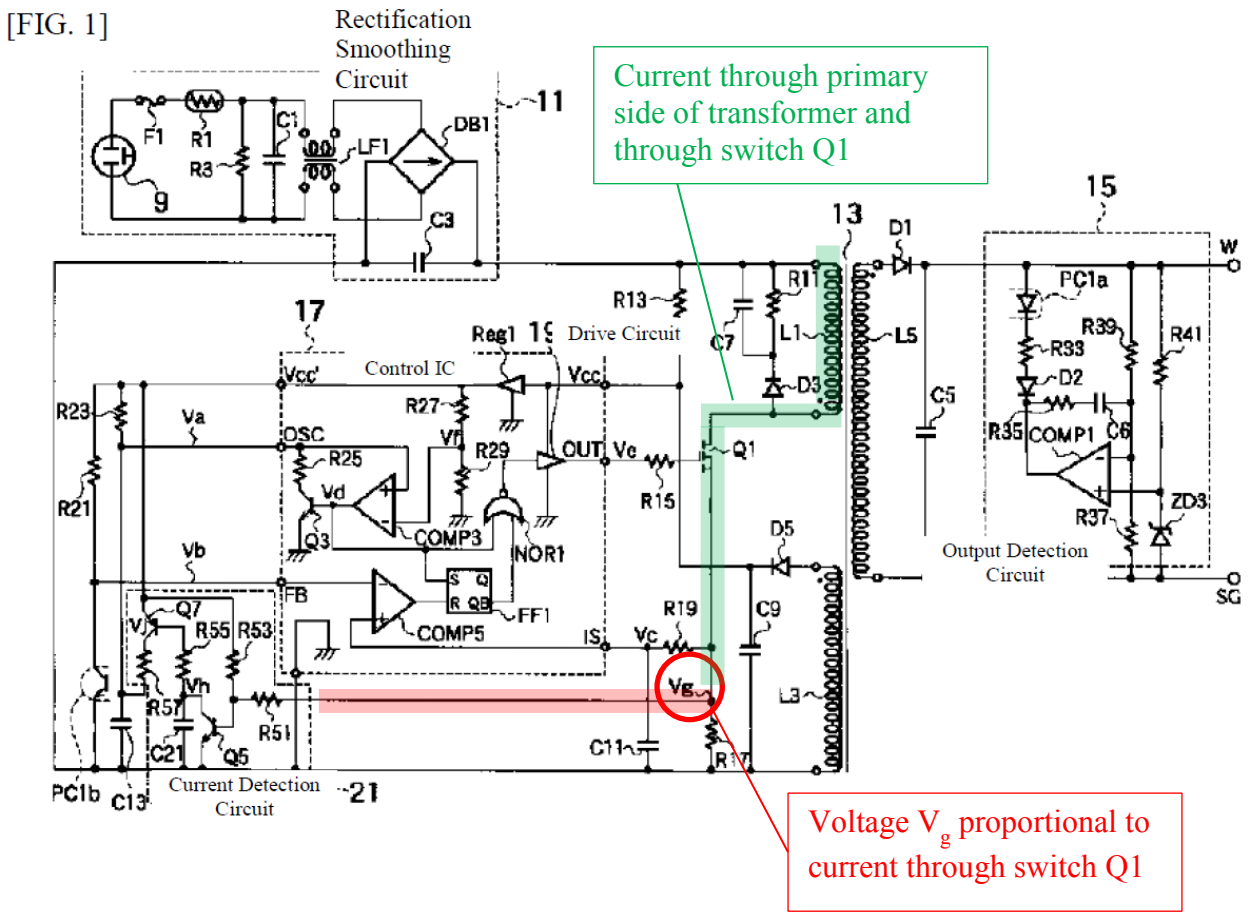
Ex. 1005, Fig. 3 (annotations added); *see id.*, Fig.1. As shown in Figure 3, the switching frequency of switch Q1 depends on the value of feedback signal V_g. When V_g crosses the "detection level," (i.e., the voltage required to turn on transistor Q5) the switching frequency is increased because capacitor C13 is

charged more quickly. Ex. 1005, ¶ 0025, Figs. 1 & 3; Ex. 1002, ¶ 59. When V_g drops below the detection level, the switching frequency decreases. *Id.* Accordingly, switch Q1 is switched on and off at a switching frequency in response to feedback signal V_g to regulate the flow of energy from an input of the power supply to the power supply output. Ex. 1002, ¶ 59.

[26b] switching a switch on and off at a switching frequency in response to the feedback signal to regulate the flow of energy from an input of the power supply to the power supply output;	**Hosoya:** Ex. 1005, ¶ 0003: "A drain of a switch element Q1 is connected to the other end of the primary winding L1 of the transformer 13, and the source of this element Q1 is connected to a GND side of the capacitor C3 of the rectification smoothing circuit 11 via a resistor R17. By this switch element Q1 being ON/OFF controlled by a control IC17 described hereafter and performing a switch operation, magnetic energy stored in the primary winding L1 of the transformer 13 is sequentially emitted to a secondary winding L5, undergoes half wave rectification by a diode D1 connected to one end of the secondary winding L5, is smoothed by the capacitor C5, and is input into an output detection circuit 15. Furthermore, the other end of the secondary winding L5 is connected to a BL terminal that becomes the output." Ex. 1005, ¶ 0009: "As a result, after timing t7, a high level on signal is output from NOR1 to a drive circuit 19, the on signal Ve is input from the drive circuit 19 to the switch element Q1 via a resistor R15, and switch element Q1 is driven. Then, the current detection signal Vc of the capacitor 11 is increased by the current flowing from the switch element Q1 to the resistor R17 via resistor R19. Because the output of the comparator COMP5 is switched from low level to high level at timing t8 when the current detection signal Vc exceeds the voltage Vb, the flip flop FF1 is reset, and as a result, the on signal output from the drive circuit 19 is turned off. Note that timings t7 and t8 are periods when the switch element is on. Meanwhile, because the voltage Vb added to one input terminal of the comparator COMP5 becomes close to 0V when the switching power supply device is at a light load, at timing t1 to t2, the on period of the switch element is shorter than when at a heavy

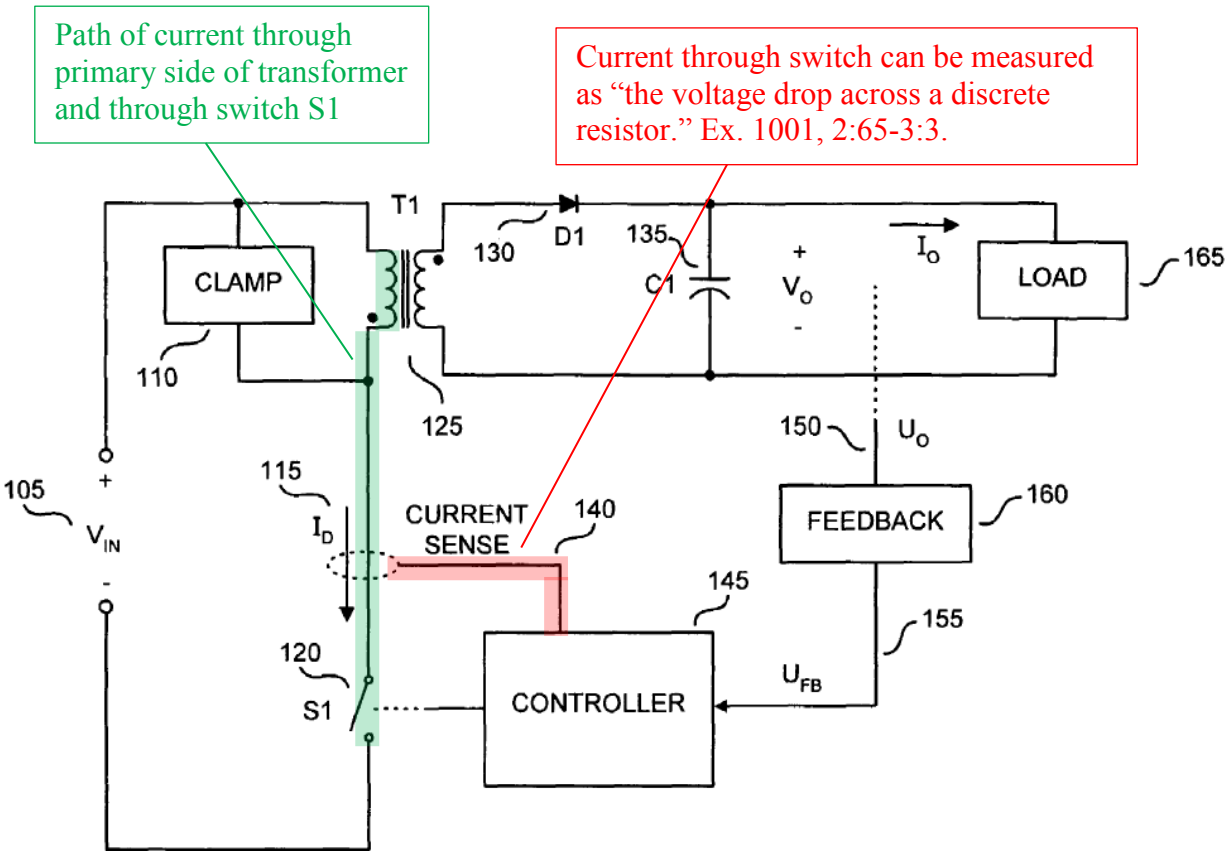
	load." *See also* Ex. 1005, Figs. 1 & 4.

Claim 26[c] detecting when a load is greater than a power level threshold value at the power supply output. Hosoya describes that "when the load of the switching power supply device becomes larger, the operation frequency rapidly increases." Ex. 1005, ¶ 0025. This rapid increase in the operation frequency is triggered when current detection circuitry **21** detects that the voltage V_g exceeds a "detection level" (i.e., the voltage required to turn on transistor Q5). Ex. 1005, ¶ 0020. As discussed above in Section VI.A.1, Vg is a feedback voltage proportional to the current through switch Q1. When V_g exceeds a detection level, it indicates that the load is greater than a power level threshold value. Ex. 1002, ¶ 60.

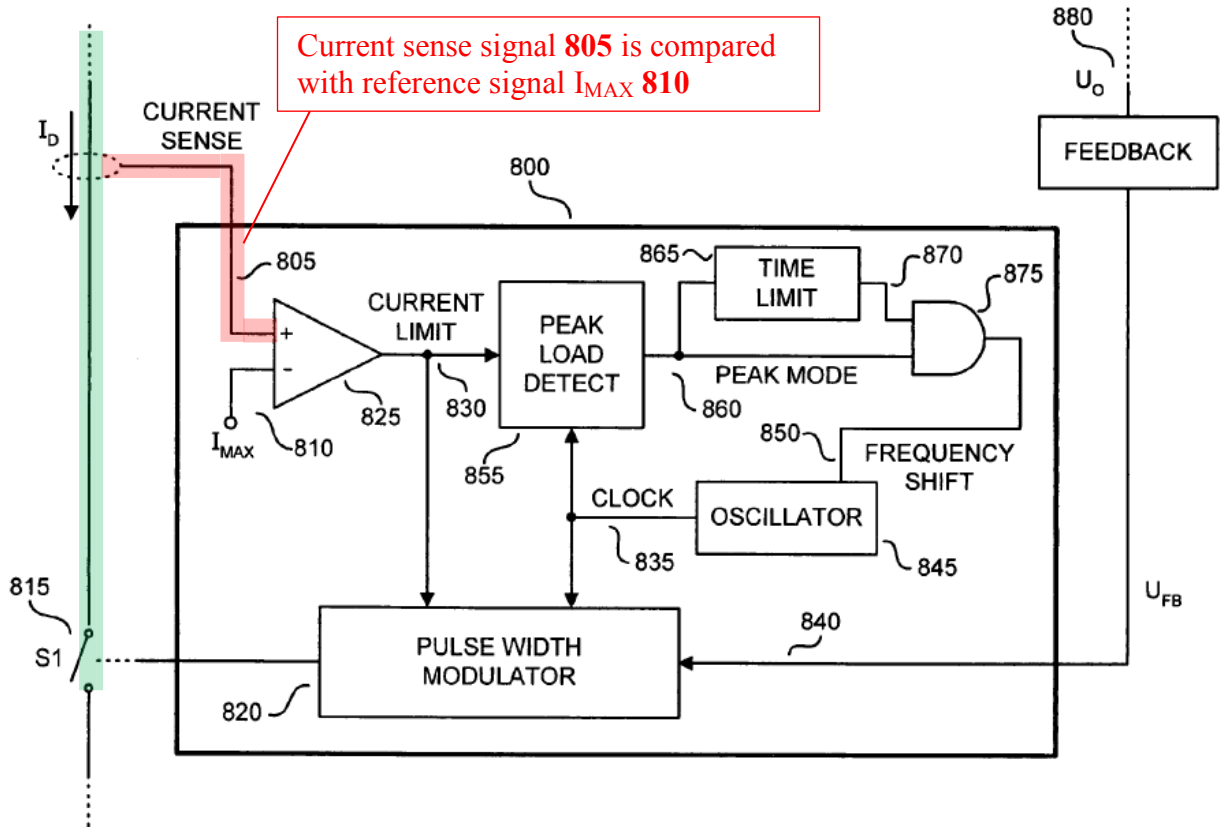


Ex. 1005, Fig. 1 (annotations added).

The method disclosed by Hosoya for detecting when a load is greater than a power level threshold is similar to the embodiment shown in Figures 1 and 8 of the '119 Patent. Ex. 1001, 6:28-7:1, Figs. 1 & 8. In that embodiment, the current through switch S**1 815** is used to determine the load demand. *Id.* ("[T]he controller 800 senses the current in the switch S**1 815** to determine the load demand."); Ex. 1002, ¶ 61.



Ex. 1001, Fig. 1 (annotations added).

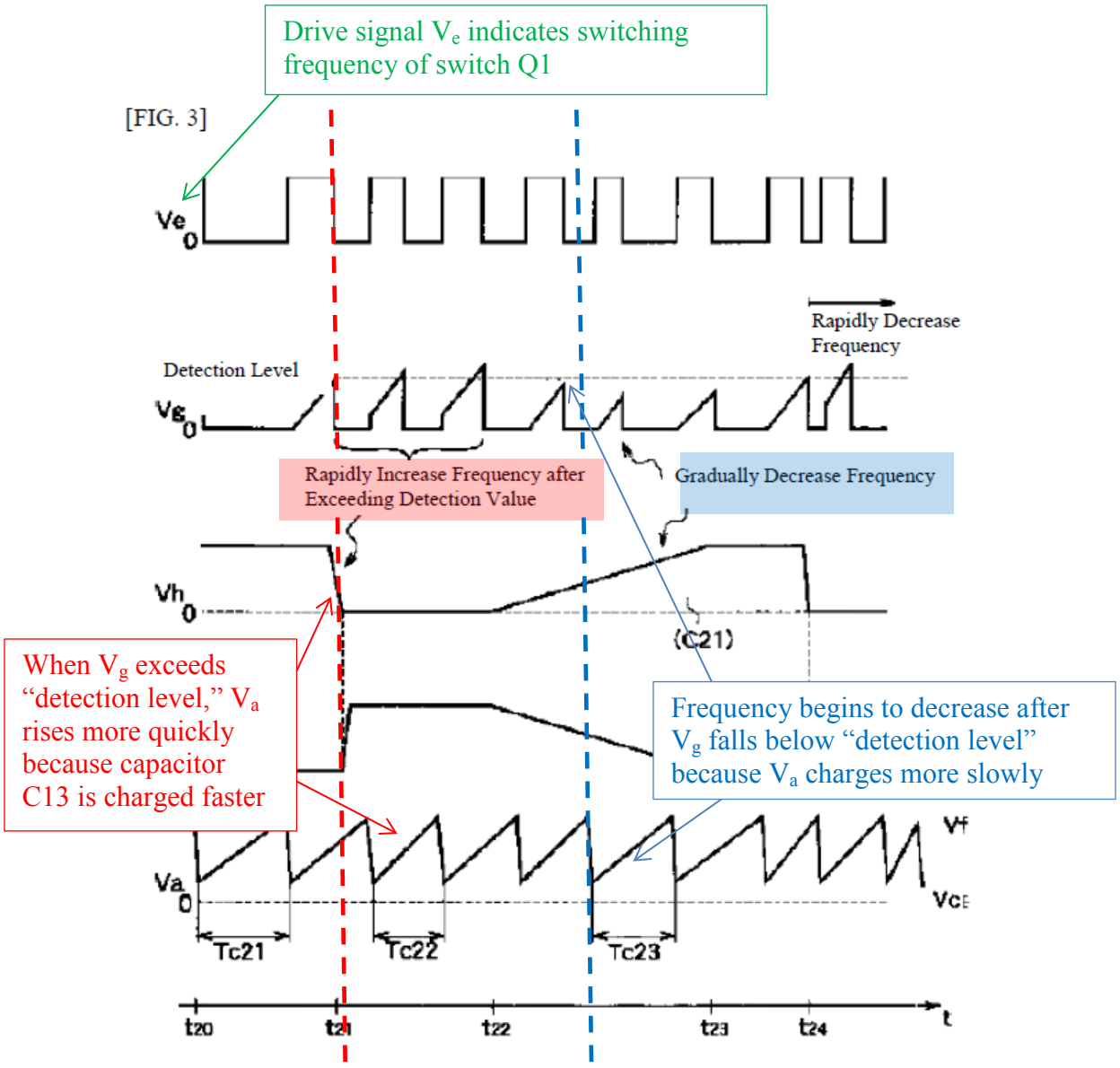


Ex. 1001, Fig. 8 (annotations added).

[26c] detecting when a load is greater than a power level threshold value at the power supply output; and	**Hosoya:** Ex. 1005, ¶ 0029: "[A]s illustrated in FIG. 3, when the base voltage of the transistor Q5 exceeds a detection level, the transistor Q5 turns on, the base voltage of the transistor Q7 is grounded to GND level via the resistor R55, and for example, as illustrated in timing t21, collector voltage Vh of the transistor Q5 rapidly becomes approximately 0V." *See also id.*, ¶¶ 0020, 0023, 0025, 0029, 0033, 0034, 0037, 0038.

Claim 26[d] temporarily increasing a maximum switching frequency of the switching frequency of the switch when the load is greater than the power level threshold value. Hosoya recognizes the necessity of increasing the switching

frequency to accommodate loads demanding a large amount of current in a short period of time. Ex. 1005, ¶ 0011. The power supply described in Hosoya increases the maximum switching frequency of switch Q1 in response to detecting a high load. Ex. 1005, ¶ 0012. The maximum switching frequency is increased via Current Detection Circuit **21** in response to the current through switch Q1 exceeding a predetermined value. Ex. 1005, ¶¶ 0020-0025. Hosoya explains that when voltage V_g exceeds a Detection Level, Current Detection Circuit **21** acts to increase the charge current of capacitor C13 and thereby increase the maximum switching frequency of switch Q1. Ex. 1005, ¶ 0014, 0017-0019; Ex. 1002, ¶ 62. The temporary increase in switching frequency can be seen with reference to Figure 3 of Hosoya.



Ex. 1005, Fig. 3 (annotations added). When V_g is below the Detection Level, switch Q1 turns on and off at a maximum switching frequency controlled by charging time Tc21. Ex. 1005, ¶ 0023, Fig. 3. Subsequently, the maximum switching frequency increases rapidly in response to the Current Detection Circuit

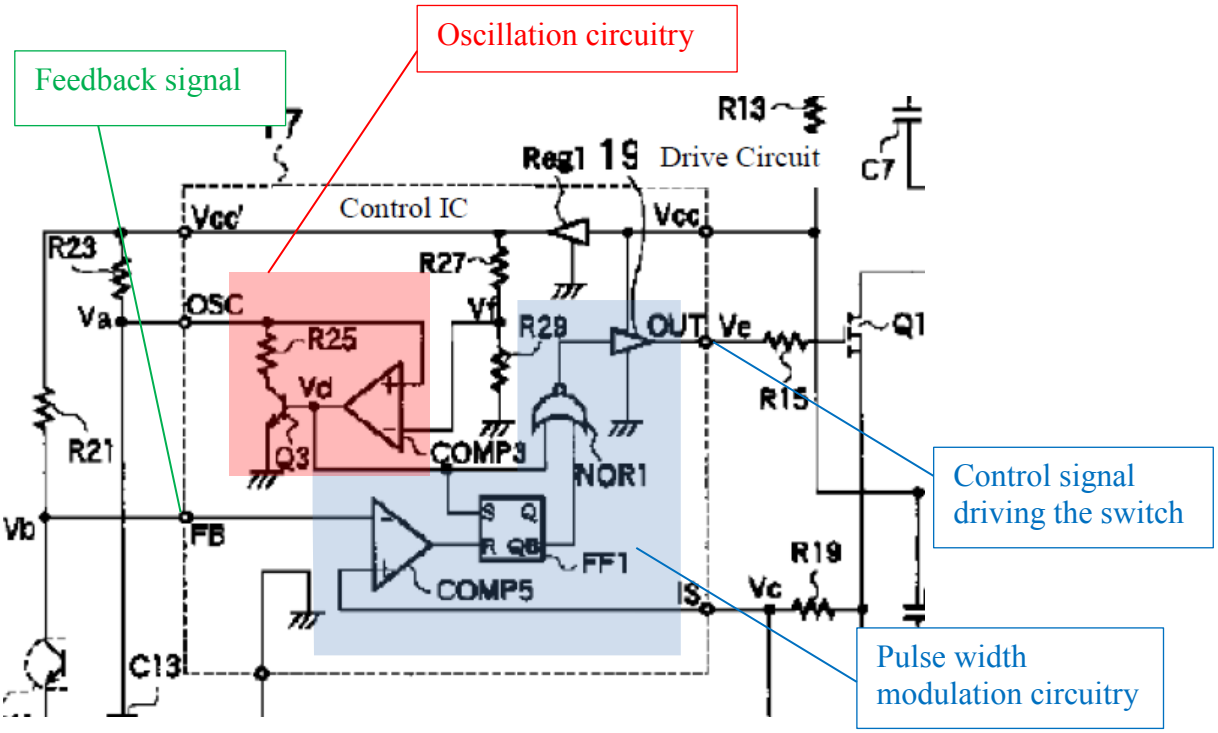
detecting that V_g has risen above the Detection Level. Ex. 1005, ¶ 0023, Fig. 3.

As discussed above in Section V.A, "temporarily increasing a maximum switching frequency" should be construed to mean that a maximum switching frequency is increased for a limited period of time or non-permanently (regardless of the mechanism by which the time period is limited). *See supra* Section V.A. The maximum switching frequency in Hosoya is temporarily increased because, as illustrated in Figure 3, when V_g falls back below the Detection Level, the maximum switching frequency begins to decrease. Ex. 1005, Fig. 3; Ex. 1002, ¶ 62.

[26d] temporarily increasing a maximum switching frequency of the switching frequency of the switch when the load is greater than the power level threshold value.	**Hosoya:** Ex. 1005, ¶ 0011 (emphasis added): "Meanwhile, when using a small transformer, it is necessary to raise the operation frequency in order to handle a load having a motor wherein a large current flows in a short time such as on startup, or an increasing peak load in a laptop computer or the like, and this becomes a problem for miniaturization." Ex. 1005, ¶ 0012 (emphasis added): "[A]n object of the present invention is to provide a switching power supply device that can reduce the operation frequency when at a certain power or below such as during normal operation or when at a light load, increase the operation frequency when at a high load such as when a transformer or the like reaches its limit, and contribute to the improvement of miniaturization and load efficiency." *See also* Ex. 1005, Figs. 1-3, Claim 2, ¶¶ 0020-0023, 0025, 0029, 0033, 0034, 0037, 0038.

2. Claim 27

"27. The method of claim 26 wherein switching the switch in response to the feedback signal to regulate the flow of energy from the power supply input to the power supply output comprises pulse width modulating a control signal driving the switch." Hosoya uses pulse width modulation of a control signal to regulate the flow of energy from the power supply input to the power supply output. Ex. 1005, ¶¶ 0013, 0017, Claim 1; Ex. 1002, ¶ 63. Hosoya describes that "the present embodiment . . . is configured to . . . control the on-duty of the switch element by a feedback signal." Ex. 1005, ¶ 0017.



Ex. 1005, Fig. 1 (annotated excerpt). The switch element is switch Q1 and the

feedback signal that controls the duty cycle of the switch through pulse width modulation is voltage V_b at the FB pin. Ex. 1005, Fig. 1; Ex. 1002, ¶ 63. What follows below is a description of how pulse width modulation occurs in Hosoya.

As illustrated in Figure 1, switch Q1 is driven by drive circuit **19**, which is coupled to NOR gate NOR1. Ex. 1005, ¶ 9, Fig. 1. V_e is the signal that turns switch Q1 on and off. NOR1 receives an input from flip flop FF1 and another input from the oscillator circuitry shown in red above. *Id.* During each switching cycle, the oscillator sets flip-flop FF1, which (via NOR gate NOR1 and driver **19**) turns on switch Q1. *Id.* The duty cycle is modulated by the resetting flip-flop FF1, which is done by COMP5. COMP5 receives feedback signal V_b at its inverting ("-") input and current detection signal V_c at its non-inverting ("+") input. Ex. 1005, ¶ 9, Fig. 1. COMP5 provides a reset signal to FF1 when V_c is greater than V_b, which ends the on-time of the cycle. *Id.* In sum, during each switching cycle, switch Q1 is turned on according to the oscillating voltage V_a, and Q1 is turned off based on a comparison of V_b (i.e., the feedback voltage) and V_c. Accordingly, the width of each on-time pulse of Q1 is controlled by the feedback signal, and the flow of energy from the power supply input to the power supply output is achieved by pulse width modulating a control signal driving the switch. Ex. 1002, ¶ 64.

B. Ground 2: The Combination of Hosoya with King Renders Obvious Claim 32 Under 35 U.S.C. § 103

The combination of Hosoya and King discloses each element of Claim 32

and thus renders that claim obvious under 35 U.S.C. § 103. Ex. 1002, ¶ 65.

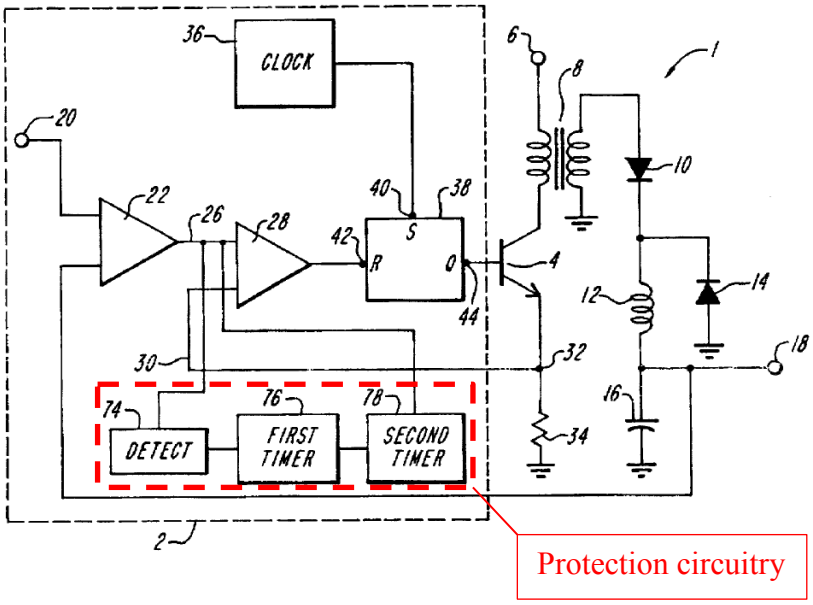
1. A POSITA would have been motivated to combine Hosoya and King

Motivation found in both Hosoya and King would have led one of ordinary skill in the art to combine Hosoya with the teachings of King to arrive at the claimed invention. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1741-42 (2007); Ex. 1002, ¶ 66.

King discloses protection circuitry designed to prevent a switching power supply from being damaged by high voltages or currents when used with variable loads. Ex. 1008, 1:6-10, 2:21-31; Ex. 1002, ¶ 67. King notes that "power supply apparatus, such as dc-to-dc converters, ac-to-dc converters, rectifiers and motor controls, typically incorporates protection circuitry to protect the apparatus from, for example, a short circuit load." Ex. 1008, 1:17-20. King describes a protection technique that offers advantages over prior known techniques. Ex. 1008, 1:21-2:17 (discussing disadvantages of heat sinks, constant-current limiting circuitry, and foldback circuitry). In particular, King notes that "miniaturization of switching power apparatus" presents difficulty for prior protection techniques, especially when dealing with variable loads like "motors and devices that have considerable input capacitance." Ex. 1008, 1:39-42, 2:1-17. To overcome these challenges, King discloses protection circuitry that "reduces the likelihood of damage to the power supply apparatus and associated circuitry from such abnormal source and load

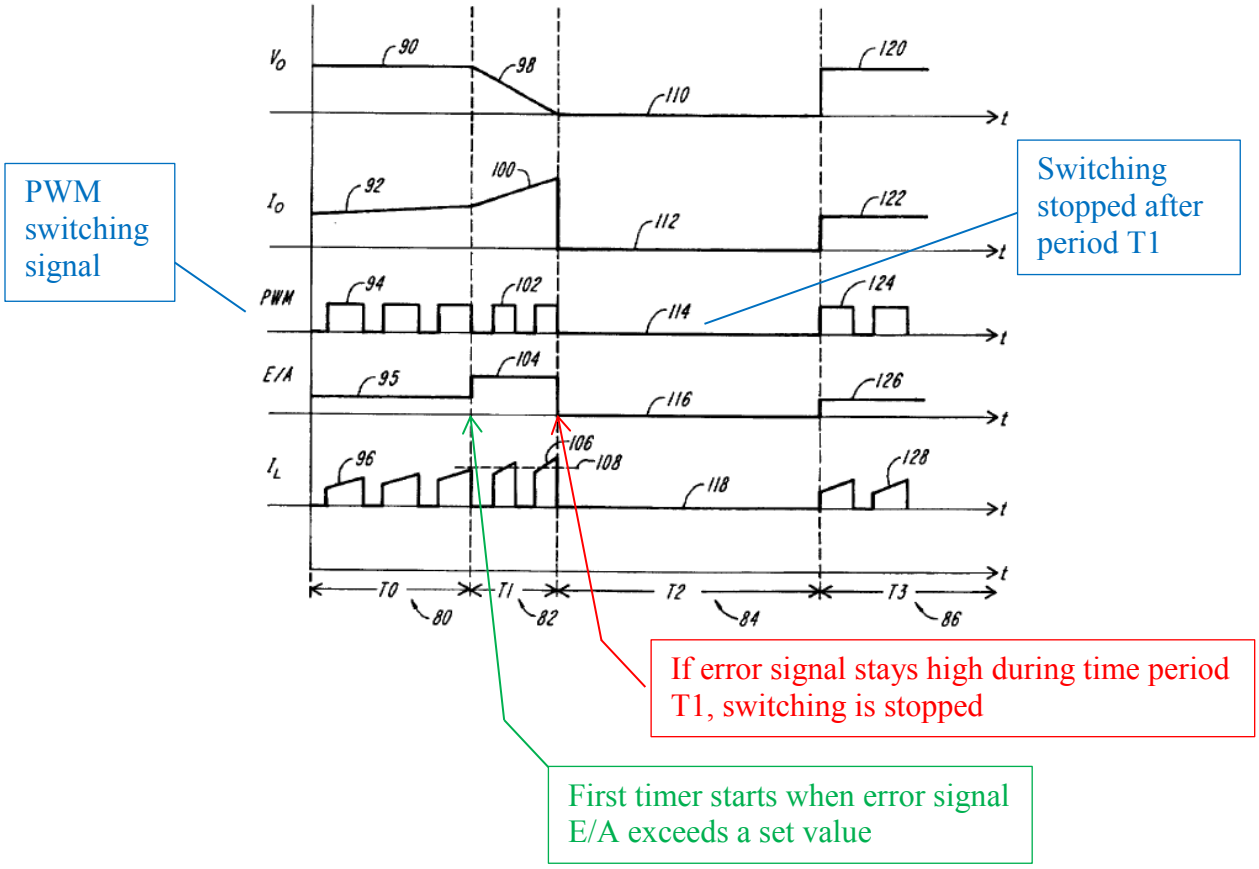
impedances, yet allows the power supply apparatus to supply adequate power to a variety of variable loads, particularly loads that vary when initially powered." Ex. 1008, 2:42-47. This protection circuitry is "particularly useful in protecting switching-type power supplies, wherein oscillator pulses periodically switch power to an energy storage component, typically an inductor, for short intervals." Ex. 1008, 2:50-53; Ex. 1002, ¶ 67.

The protection circuitry disclosed in King includes, in one embodiment, a detection circuit **74** and two timing circuits **76** and **78**. Ex. 1008, 2:61-62, 6:64-7:8.



Ex. 1008, Fig. 1. "The detection circuit monitors a first signal representative of the power delivered to the load." Ex. 1008, 2:61-63, 6:64-7:8. When the first signal exceeds a predetermined value indicative that "potentially damaging currents and/or voltages are likely present" the detection circuit generates a signal that initiates a first timer. Ex. 1008, 2:64-3:1; Ex. 1002, ¶ 68. If the first signal remains

excessive for a first period of time, the power output is reduced or terminated for a second period of time by a second timer. Ex. 1008, 3:1-6, 6:64-7:8.



Ex. 1008, Fig. 4.

A person of ordinary skill in the art would be motivated by the express teachings of King to combine the King protection circuitry with the power supply disclosed in Hosoya. Ex. 1002, ¶ 69. Hosoya is directed to a switching power supply that improves "miniaturization and load efficiency," particularly when used "to handle a load having a motor wherein a large current flows in a short time such as on startup." Ex. 1005, ¶ 0011. A POSITA would recognize that the King

circuitry would offer all of the protection advantages described in King while allowing the Hosoya power supply to maintain goals of efficiency and miniaturization. Indeed, the switching power supply of Hosoya is quite similar to the exemplary switching power supply disclosed in King, and it is designed to be used in the type of variable load conditions (e.g., a motor during startup) that King's protection technique is designed to accommodate. Ex. 1005, ¶ 11; Ex. 1008, Abstract, 2:42-48; Ex. 1002, ¶ 69. Accordingly, a POSITA would recognize that the protection circuitry from King would improve the Hosoya switching power supply in the same way that it improves the King switching power supply. Ex. 1002 ¶ 69; *see KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1731 (2007).

2. Claim 32

"32. The method of claim 26 wherein temporarily increasing the maximum switching frequency of the switch when the load is greater than the power level threshold value includes limiting a time duration that the switch may be switched at up to the increased maximum switching frequency."

The combination of switching power supply disclosed in Hosoya with the protection circuitry disclosed in King discloses each limitation of Claim 32. Ex. 1002, ¶ 70. As discussed above in Section VI.B.1, King discloses protection circuitry that includes a detection circuit that monitors a signal "representative of the power delivered to the load," and then terminates the switching when that

representative signal remains above a threshold for longer than a certain amount of time. *See supra* Section VI.B.1. As discussed above in Section VI.A.1, the switching regulator in Hosoya increases the switching frequency in response to a peak load event (i.e., when the load demand increases beyond a defined threshold). *See supra* Section VI.A.1. When used in combination with the power supply disclosed in Hosoya, the protection circuitry of King would detect the peak load event (just as Hosoya does) and then terminate the switching signal after a predetermined time has passed, thereby limiting the time duration that the switch in Hosoya may be switched at up to the increased maximum switching frequency. Ex. 1002, ¶ 70.

C. Ground 3: Hirst Anticipates Claims 26 and 27 Under 35 U.S.C. § 102

1. Claim 26

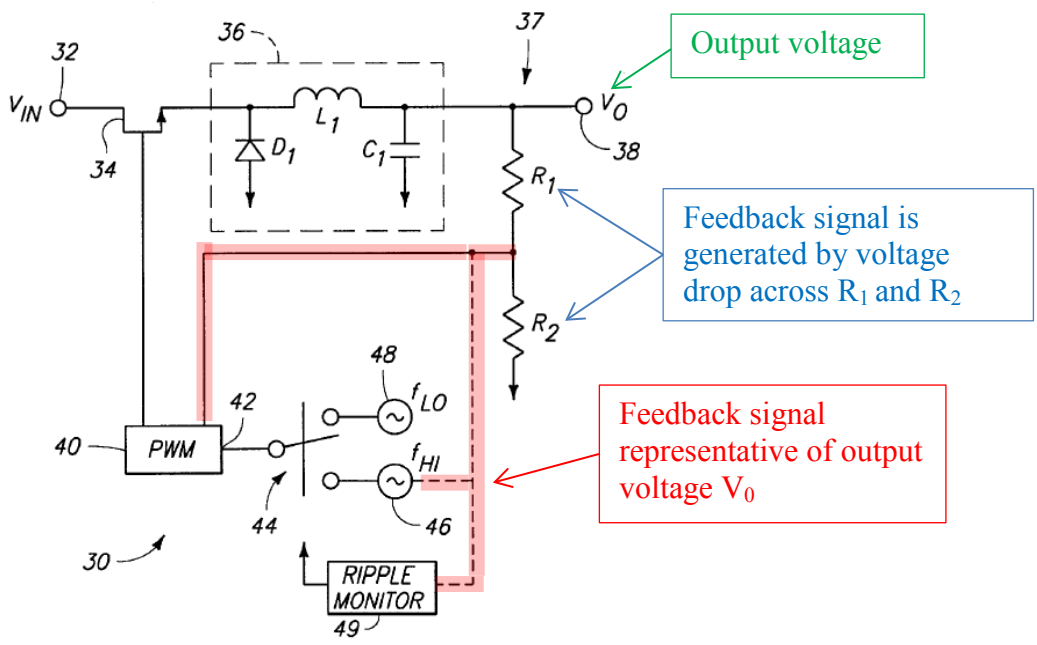
26[pre]. A method for regulating a power supply output, comprising. Hirst describes a switching power supply and several methods to regulate a switching power supply output. Ex. 1006, Abstract, 2:44-65. For example, Hirst describes a method to regulate a switching power supply involving "determining when an output current from the power supply falls below a threshold and switching from one switching frequency to another, discrete switching frequency when the output current falls below the threshold." Ex. 1006, 3:1-4. Hirst also provides schematic diagrams of switching power supplies that regulate a power supply output. *See,*

e.g., Ex. 1006, Figs. 2-6; Ex. 1002, ¶ 71.

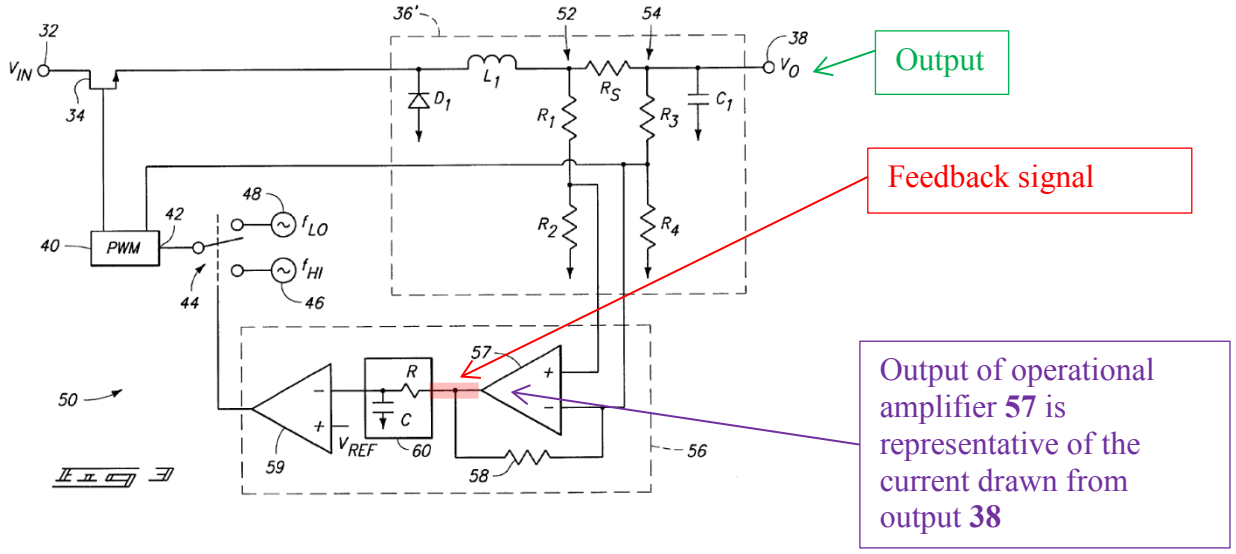
26[pre]. A method for regulating a power supply output, comprising:	**Hirst:** Ex. 1006, 2:66-3:4: "The method includes determining when an output current from the power supply falls below a threshold and switching from one switching frequency to another, discrete switching frequency when the output current falls below the threshold." Ex. 1006, Abstract: "A multiple frequency switching power supply including a pulse width modulation circuit having an output, having an input and having a clock signal input. The power supply also includes a switching transistor having first and second current-carrying electrodes and a control electrode. The first current-carrying electrode is coupled to a voltage source, the control electrode is coupled to the output of the pulse width modulation circuit and the second current-carrying electrode is coupled to a power supply output configured to provide a regulated output voltage. The power supply additionally includes a voltage sensing circuit coupled to the power supply output and having an output coupled to the pulse width modulation circuit input and a switch coupled to the clock input of the pulse width modulation circuit." *See also* Ex. 1006, Figs. 1-5.

Claim 26[a] receiving a feedback signal representative of an output level of a power supply output. Hirst discloses various power supply embodiments that each receive a feedback signal representative of an output level of a power supply. For example, in the embodiment shown in Figure 2, Hirst shows a multiple frequency power supply that includes a feedback signal representative of the output voltage V_0 (i.e., an output level) of power output port **38** (i.e., a power supply output). Ex. 1006, Figs. 1 & 2, 6:30-34. The feedback signal is received by Ripple

Monitor **49** and first oscillator **46**. *Id.*; Ex. 1002, ¶ 72. Hirst explains that the "amount of ripple that is present in the output voltage V_0 tends to increase as the amount of power being drawn from the MF [Multiple Frequency] switching power supply **30** increases." *Id.*



Ex. 1006, Fig. 2 (annotations added). An additional example of receiving a feedback signal representative of an output level of a power supply can be seen in the embodiment shown in Figure 3.



Ex. 1006., Fig. 3 (annotations added). As shown in Figure 3, operational amplifier **57** receives two signals, one from either side of sense resistor R_S. *Id.* Operational amplifier magnifies the voltage difference between its inverting ("-") and noninverting ("+") inputs to provide an indication of the current being drawn from output **38**. Ex. 1006, 7:18-22. In other words, the output of operational amplifier **57** is a feedback signal that is proportional to the current through inductor L1 and the output current at node **38**. *Id.*, Ex. 1002 ¶ 72. Coupled to operational amplifier **57** is R-C filter **60**, which receives the feedback signal from operational amplifier **57**. Ex. 1006, Fig. 3.

Figures 4 and 5 show additional embodiments that include receiving a feedback signal (i.e., the signal at the node between R_1 and R_2 coupled to PWM circuit **40)** representative of an output level of a power supply (i.e., the output voltage). Accordingly, Hirst discloses every limitation of claim element 26[a]. Ex.

1002, ¶ 73.

[26a] receiving a feedback signal representative of an output level of a power supply output;	**Hirst:** Ex. 1006, 5:62-64: "For example, the first oscillator **46** may sense power supply loading using the voltage divider **37**, as indicated by a dashed line in FIG. 2." Ex. 1006, 7:5-22: "In one embodiment, the current sensing circuit **56** includes a first operational amplifier **57**, a resistor **58** and a second operational amplifier **59**. The first operational amplifier **57** has a non-inverting input coupled to a node joining the resistors R_1 and R_2 forming the first voltage divider **52**. The first operational amplifier **57** has an inverting input coupled to a node joining the resistors R_3 and R_4 forming the second voltage divider **54**. The resistor **58** sets a gain for the first operational amplifier **57**. An output signal from the first operational amplifier **57** is coupled to an inverting input to the second operational amplifier **59**. A reference voltage V_{REF} is coupled to a non-inverting input to the second operational amplifier **59**. The reference voltage V_{REF}, together with the resistor **58**, the resistor R_S and the first and second voltage dividers **52** and **54**, determine a current level at which the current sensing circuit **56** switches from a normal operating state to a standby state and vice versa." *See, also* Ex. 1006, 5:46-51; 6:29-43; 6:54-64; 7:23-40; 7:63-8:8; Figs. 1-5.

Claim 26[b] switching a switch on and off at a switching frequency in response to the feedback signal to regulate the flow of energy from an input of the

power supply to the power supply output.[3]

In the embodiments shown in Figures 1 through 5 of Hirst, switching transistor **34** is switched on and off by PWM circuit **40** to regulate the flow of energy from power input port **32** (i.e., an input of the power supply) through filtering circuit **36** and then to power output port **38** (i.e., the power supply output). Ex. 1006, 6:1-14, Figs. 1-5. Accordingly, Figures 1-5 disclose switching the switch **34** on and off in response to the feedback signal (identified above for each embodiment in the discussion of claim element 26[a]) to regulate the energy flowing form the input of power supply (V_{IN}) to the power supply output (V_O). Ex. 1002, ¶ 75.

The switching frequency of switching transistor **34** is, in the Figure 2 embodiment, determined by Ripple Monitor **49**. Ex. 1002, ¶ 76. Based on a feedback signal (shown in red in annotated Figure 2 below), Ripple Monitor **49** couples either first oscillator **46** or second oscillator **48** to PWM circuit **40** via switch **44**. Ex. 1006, Fig. 2,6:1-14.

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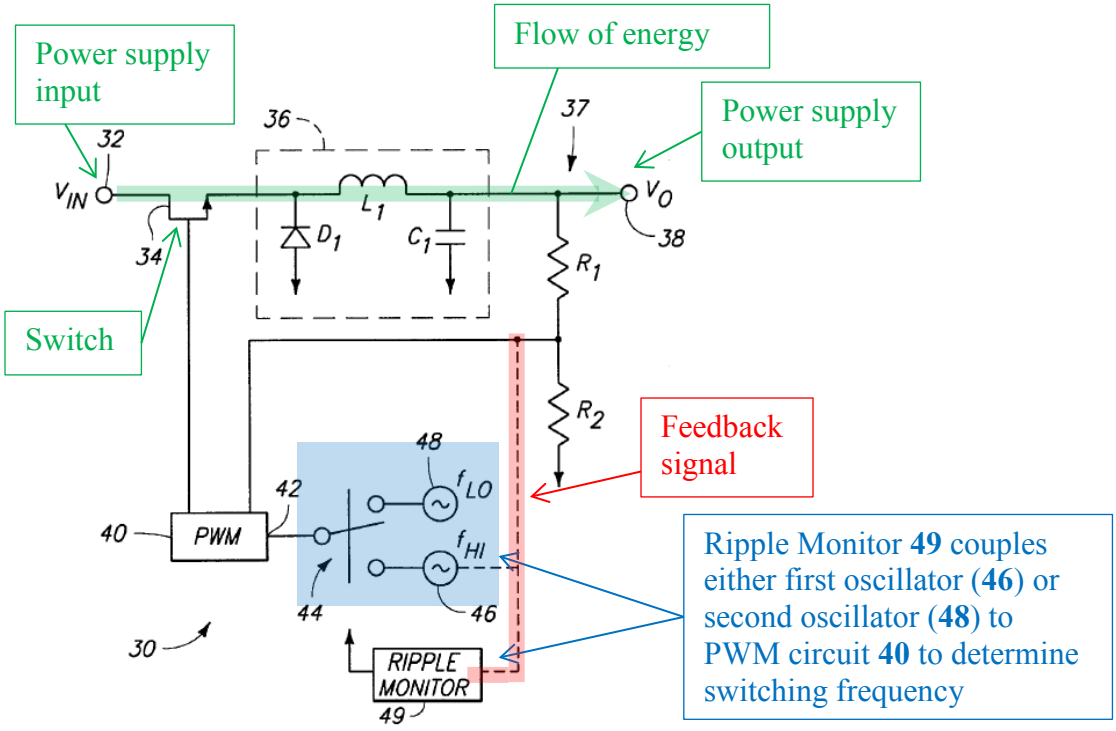
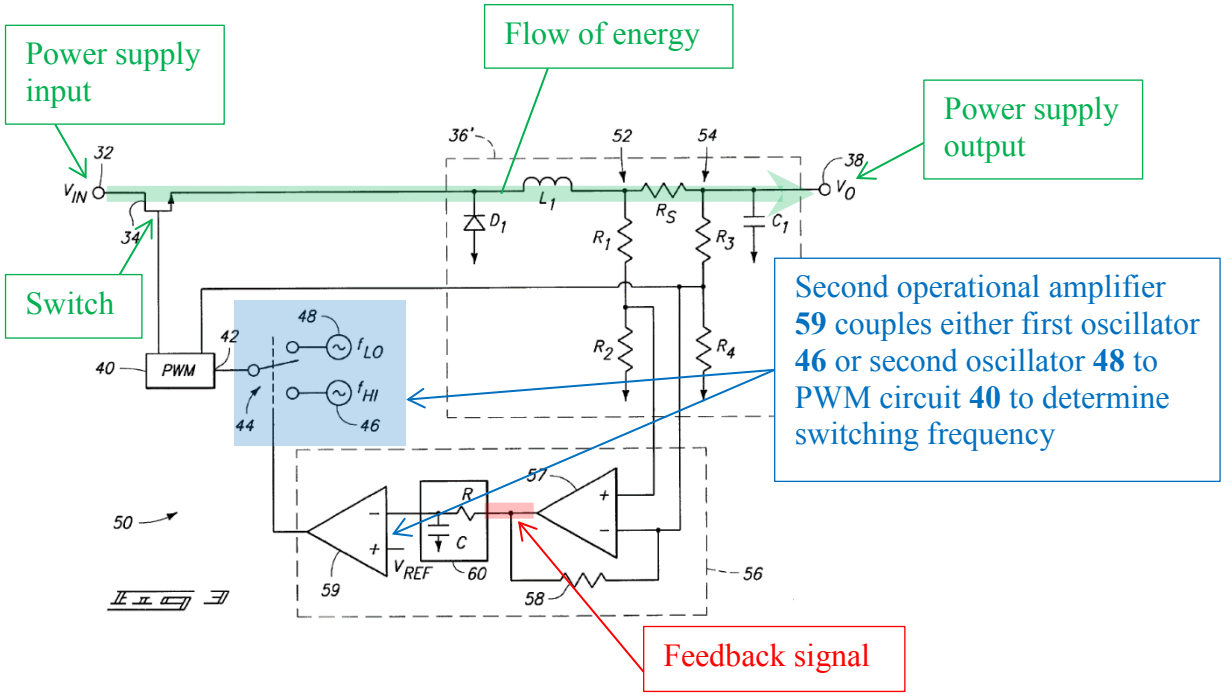
[3] The claim language is not clear as to whether the value of the switching frequency is "in response to the feedback signal," or alternatively, whether only "switching a switch on and off" must be "in response to the feedback signal." Hirst satisfies the limitation under either interpretation.



Ex. 1006, Fig. 2 (annotations added). With respect to Figure 3, Hirst discloses that the switching frequency (i.e., the value of the switching frequency) of switching transistor **34** is determined by the output of second operational amplifier **59**, which, based on a feedback signal (i.e., the output of first operational amplifier **57**), couples either first oscillator **46** or second oscillator **48** to PWM circuit **40** via switch **44**. Ex. 1006, Fig. 3, 6:54-7:40; Ex. 1002, ¶ 76.



Ex. 1006, Fig. 3 (annotations added).

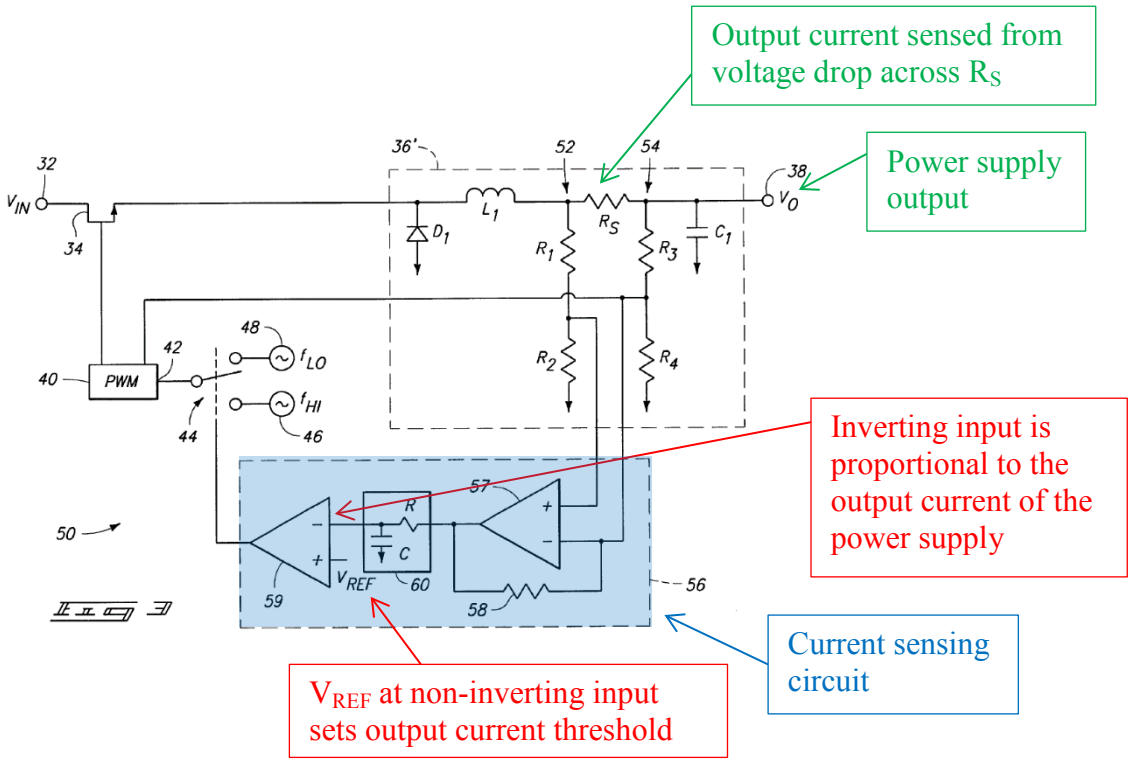
[26b] switching a switch on and off at a switching frequency in response to the feedback signal to regulate the flow of energy from an input of the power supply to the power supply output;	**Hirst:** Ex. 1006, 6:1-14 (emphasis added): "The MF switching power supply **30** operates by turning the switching transistor **34** ON and OFF to supply electrical charge from the power input port **32** to the filtering circuit **36**. The resistive voltage divider **37** is formed from two resistors R_1 and R_2 and provides a node at a junction of the two resistors R_1 and R_2 for one input of the PWM circuit **40**. A gate of the switching transistor **34** is coupled to an output of the PWM circuit **40**. A pulse width of the ON portion of the duty cycle of the switching transistor **34** is varied in a conventional manner by the PWM circuit **40** in response to voltages sensed by the voltage divider **37** to regulate the amount of charge that is transferred per cycle from the power input port **32** to the filtering circuit **36** and thus to maintain the desired output voltage V_{OUT} at the output **38**." Ex. 1006, 6:29-42: "In one embodiment, the MF switching power supply **30** includes a ripple monitor **49**. The amount of

	ripple that is present in the output voltage V_0 tends to increase as the amount of power being drawn from the MF switching power supply **30** increases. When the ripple monitor **49** determines that the ripple in the output voltage V_0 is too high, the ripple monitor **49** provides a signal to the controller **18** of FIG. 1 to increase the frequency of the MF switching power supply **30**. In one embodiment, the frequency is increased by switching to the first oscillator **46**. In one embodiment, the frequency of the first oscillator **46** is increased when the ripple monitor **49** detects unacceptably high ripple, for example by changing a control voltage controlling a VCO employed for the first oscillator **46**." *See, also id.*, 6:54-8:8, Figs. 1-5.

Claim 26[c] detecting when a load is greater than a power level threshold value at the power supply output. Hirst describes several methods of detecting when a load is greater than a power level threshold value at the power supply output. First, with respect to the simplified block diagram shown in Figure 1, Hirst describes that "[w]hen the power consumption monitor **22** detects increased power consumption, the power consumption monitor **22** causes the switch **44** to switch from the second oscillator **48** to the first oscillator **46**." Ex. 1006, 5:47-50. More specifically, Hirst notes with respect to Figure 2 that "the amount of ripple that is present in the output voltage V_0 tends to increase as the amount of power being drawn from the MF switching power supply **30** increases." Ex. 1006, 6:30-33. Ripple Monitor **49** determines the amount of ripple present in the output voltage

V_0, and when the ripple is "too high" (i.e., when the output voltage is greater than a power level threshold) the frequency of the power supply is increased. Ex. 1006, 6:30-37; Ex. 1002, ¶ 79.

Figure 3 provides an additional example of detecting when a load is greater than a power level threshold value. In this embodiment, current sensing circuit **56** serves as an exemplary power consumption monitor **22** of Figure 1. Ex. 1006, 6:67-7:4; Ex. 1002, ¶ 80.



Ex. 1006, Fig. 3 (annotations added). Hirst explains that "[t]he reference voltage V_{REF}, together with the resistor **58**, the resistor R_S and the first and second voltage dividers **52** and **54**, determine a current level at which the current sensing circuit **56**

switches from a normal operating state to a standby state and vice versa." Ex. 1006, 18-22. In other words, the value of the reference voltage V_{REF} and the above-mentioned set of resistors establish the output current (i.e., a power level threshold) at which the second operational amplifier **59** switches the PWM **40** from the second oscillator **48** to the first oscillator **46**. Ex. 1006, 7:34-40. The embodiment shown in Figure 3 of Hirst is similar to the Figure 8 embodiment in the '119 Patent. There, as in Hirst, the power supply controller senses load demand based on a current comparison. Ex. 1001, 6:28-31, Figs. 1 & 8; Ex. 1002, ¶ 80.

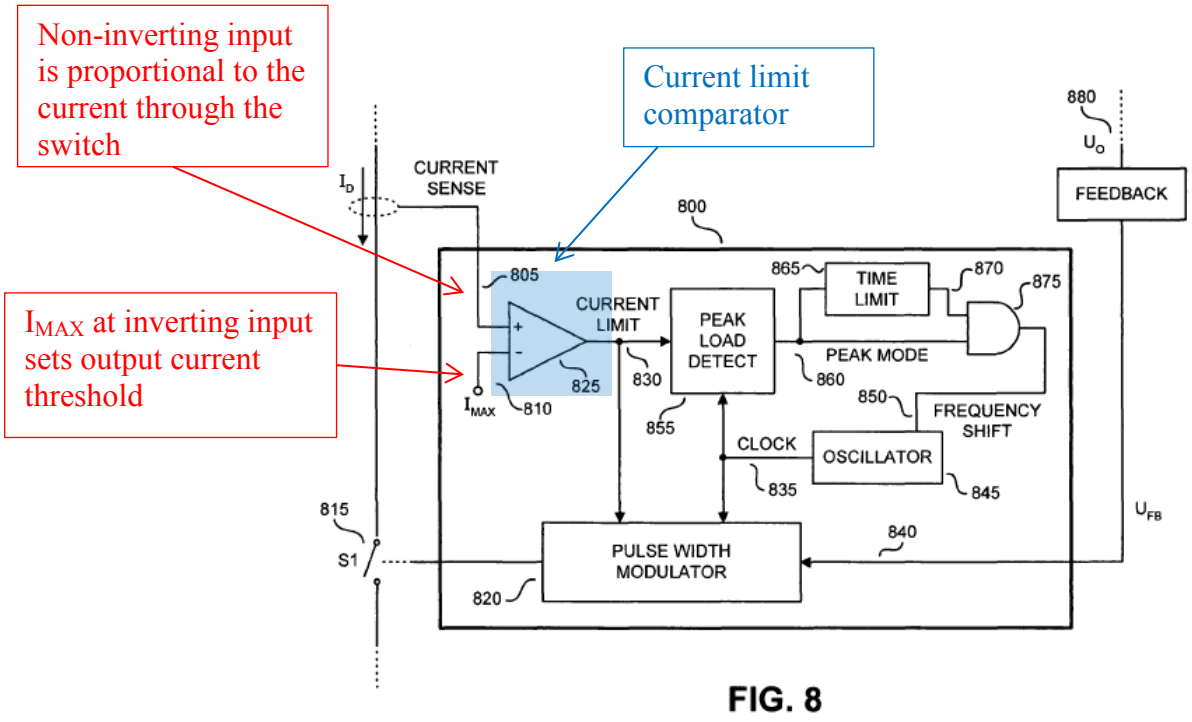


FIG. 8

Ex. 1001, Fig. 8 (annotations added).

As an additional example, the embodiment in Figure 4 of Hirst detects when a load is greater than a power level threshold value using duty cycle sense circuit

72, which "detects need for increased power output from the MF switching power supply **70**, for example due to increased duty cycle of the switching transistor **34**." Ex. 1006, 7:41-62. The duty cycle is adjusted by PWM circuit **40** based on a feedback signal proportional to the output voltage at V_O. Ex. 1006, 6:1-14. A POSITA would understand that the PWM circuit responds to a drop in output voltage by increasing the duty cycle (i.e, the on time of switch **34**) and that the duty cycle is therefore representative of the output voltage. Ex. 1002, ¶ 81. Accordingly, detecting when the duty cycle rises above a threshold is an example of detecting when the load is greater than a power level threshold value at the power supply output. Ex. 1002, ¶ 81; Ex. 1006, 7:41-62, Figs. 1 & 4.

Thus, Hirst discloses every limitation of claim element 26[c]. Ex. 1002, ¶ 82.

[26c] detecting when a load is greater than a power level threshold value at the power supply output; and	**Hirst:** Ex. 1006, 5:47-50: "When the power consumption monitor **22** detects increased power consumption, the power consumption monitor **22** causes the switch **44** to switch from the second oscillator **48** to the first oscillator **46**." Ex. 1006, 6:30-37: "The amount of ripple that is present in the output voltage V_0 tends to increase as the amount of power being drawn from the MF switching power supply **30** increases. When the ripple monitor **49** determines that the ripple in the output voltage V_0 is too high, the ripple monitor **49** provides a signal to the controller **18** of FIG. 1 to increase the frequency of the MF switching power supply **30**." Ex. 1006, 7:18-22: "The reference voltage V_{REF}, together with the resistor **58**, the resistor R_S and the first and second voltage

	dividers **52** and **54**, determine a current level at which the current sensing circuit **56** switches from a normal operating state to a standby state and vice versa." Ex. 1006, 7:55-62: "When the duty cycle sensing circuit **72** detects need for increased power output from the MF switching power supply **70**, for example due to increased duty cycle of the switching transistor **34**, the duty cycle sensing circuit 72 switches the MF switching power supply **70** from the standby mode to the normal mode by coupling the first oscillator **46** to the PWM **40** to provide the first clock signal (f_{HI}) to the PWM **40**." *See also*, Ex. 1006, Figs. 1-4.

Claim 26[d] temporarily increasing a maximum switching frequency of the switching frequency of the switch when the load is greater than the power level threshold value. In each of the embodiments discussed above for Figures 2, 3, and 4 of Hirst, the power supply responds to an increase in load demand above a power level threshold by increasing the maximum switching frequency of switching transistor **34**. Ex. 1006, 5:46-54 ("When the power consumption monitor **22** detects increased power consumption, the power consumption monitor **22** causes the switch **44** to switch from the second oscillator **48** to the first oscillator **46**"), 7:34-40 ("When the current sensing circuit **56** detects that the current being drawn from the output **38** has increased above the threshold, the second operational amplifier **59** changes state, switching the switch **44** to provide the first clock signal (f_{HI})"), 7:55-62 ("When the duty cycle sensing circuit **72** detects need for increased power output from the MF switching power supply **70**, for example due to

increased duty cycle of the switching transistor **34**, the duty cycle sensing circuit **72** switches the MF switching power supply **70** from the standby mode to the normal mode by coupling the first oscillator **46** to the PWM **40** to provide the first clock signal (f_{HI}) to the PWM **40**"). The maximum switching frequency is increased when PWM circuit **40** is coupled to first oscillator **46**, which operates at a higher frequency than second oscillator **48**. *Id.*; Ex. 1002, ¶ 83.

As discussed above in Section V.A, "temporarily increasing a maximum switching frequency" should be construed to mean that a maximum switching frequency is increased for a limited period of time or non-permanently (regardless of the mechanism by which the time period is limited). The maximum switching frequency in Hirst is increased temporarily (i.e., not permanently) because it depends upon a fluctuating load. Ex. 1006, 5:36-44, 7:26-32, 7:47-51; Ex. 1002, ¶ 84. Like the '119 Patent (*see, e.g.*, Ex. 1001, 4:56-61 (describing that "the maximum frequency is varied depending on the output power demand"), 3:12-15 ("one embodiment of the oscillator in controller **145** is configured to switch temporarily at a higher frequency to accommodate temporary peak load conditions. . . ."), Figs. 5A/B, 6A/B, 7), Hirst discloses that the maximum switching frequency is decreased when the load demand falls below the power level threshold. Ex. 1006, 5:36-44, 7:26-32, 7:47-51. Additionally, Hirst describes an embodiment where the first oscillator is comprised of a voltage controlled oscillator whose

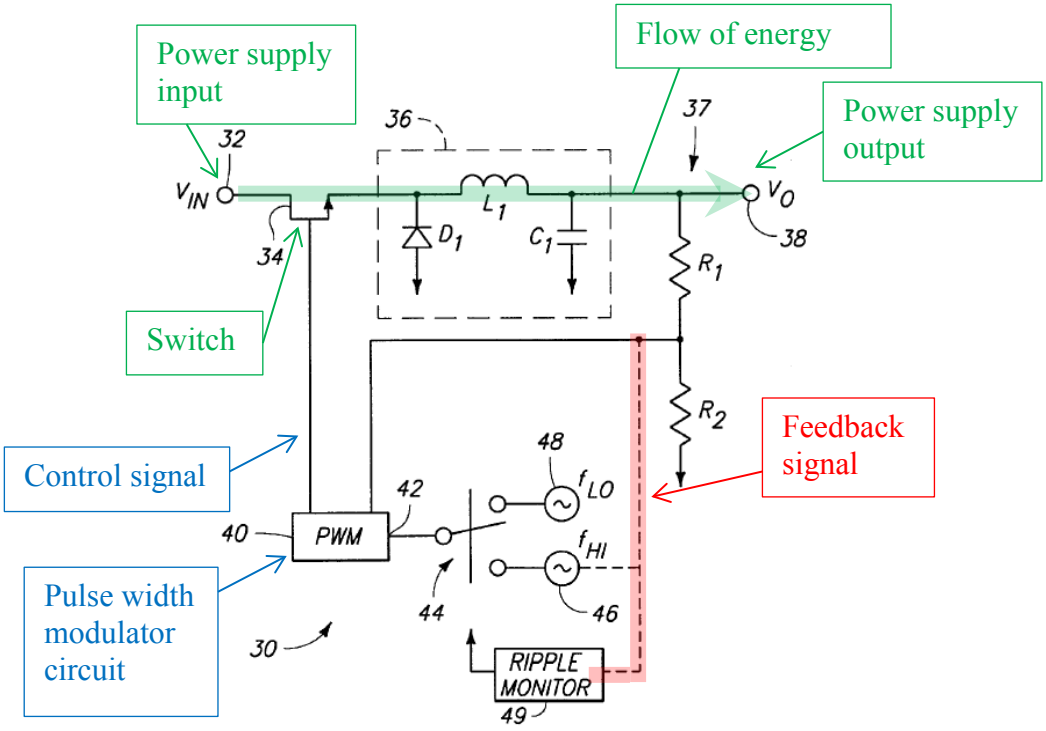
switching frequency is proportional to the output current. Ex. 1006, 5:55-61, Claim 3. In this embodiment the increase in maximum frequency is temporary because the maximum switching frequency is continually changing as the output current changes. *Id.* Accordingly, Hirst discloses every limitation of claim element 26[d]. Ex. 1002, ¶ 84.

[26d] temporarily increasing a maximum switching frequency of the switching frequency of the switch when the load is greater than the power level threshold value.	**Hirst:** Ex. 1006, 5:46-53: "When the power consumption monitor **22** detects increased power consumption, the power consumption monitor **22** causes the switch **44** to switch from the second oscillator **48** to the first oscillator **46**." Ex. 1006, 5:51-53: "In one embodiment, the first clock frequency f_{HI} is 100 kilohertz and the second clock frequency f_{LO} is 1 kilohertz." Ex. 1006, 7:34-40: "When the current sensing circuit **56** detects that the current being drawn from the output **38** has increased above the threshold, the second operational amplifier **59** changes state, switching the switch **44** to provide the first clock signal (f_{HI})." Ex. 1006, 7:55-62 "When the duty cycle sensing circuit **72** detects need for increased power output from the MF switching power supply **70**, for example due to increased duty cycle of the switching transistor **34**, the duty cycle sensing circuit **72** switches the MF switching power supply **70** from the standby mode to the normal mode by coupling the first oscillator **46** to the PWM **40** to provide the first clock signal (f_{HI}) to the PWM **40**." Ex. 1006, 5:55-61 (emphasis added): "It will be appreciated that the frequency f_{HI} of the first clock signal may be varied in a continuous fashion in order to operate the multiple frequency switching power supply **12** at high efficiency over a range of loads in the normal mode. A VCO may be used for the first oscillator **46** to allow the clock frequency f_{HI} to increase as the current output from the multiple frequency

	switching power supply **12** is increased." Ex. 1006, 9:31-38 (Claim 3) (emphasis added): "The power supply of claim 1, further comprising a voltage sensing circuit coupled to the power supply output and having an output coupled to the pulse width modulation circuit input, the first frequency is derived from a voltage controlled oscillator responsive to the voltage sensing circuit, the voltage controlled oscillator providing a first clock signal that has a frequency proportional to the output current." *See also* Ex. 1006, 5:36-44, 7:26-32, 7:47-51, Figs 1-4, Claims 1, 7, 12, 13, 14.

2. Claim 27

"27. The method of claim 26 wherein switching the switch in response to the feedback signal to regulate the flow of energy from the power supply input to the power supply output comprises pulse width modulating a control signal driving the switch." Hirst uses pulse width modulator circuit **40** to generate a control signal driving switching transistor **34**. Ex. 1006, Abstract ("The power supply additionally includes a voltage sensing circuit coupled to the power supply output and having an output coupled to the pulse width modulation circuit input and a switch coupled to the clock input of the pulse width modulation circuit."); Ex. 1002, ¶ 85.



Ex. 1006, Fig. 2 (annotations added); *see also* Figs. 3 & 4. Accordingly, Hirst discloses every limitation of claim 27.

D. Ground 4: The Combination of Hirst with King Renders Obvious Claim 32 Under 35 U.S.C. § 103

The combination of Hosoya and King discloses each element of Claim 32 and thus renders that claim obvious under 35 U.S.C. § 103. Ex. 1002, ¶ 86.

1. A POSITA would have been motivated to combine Hirst and King

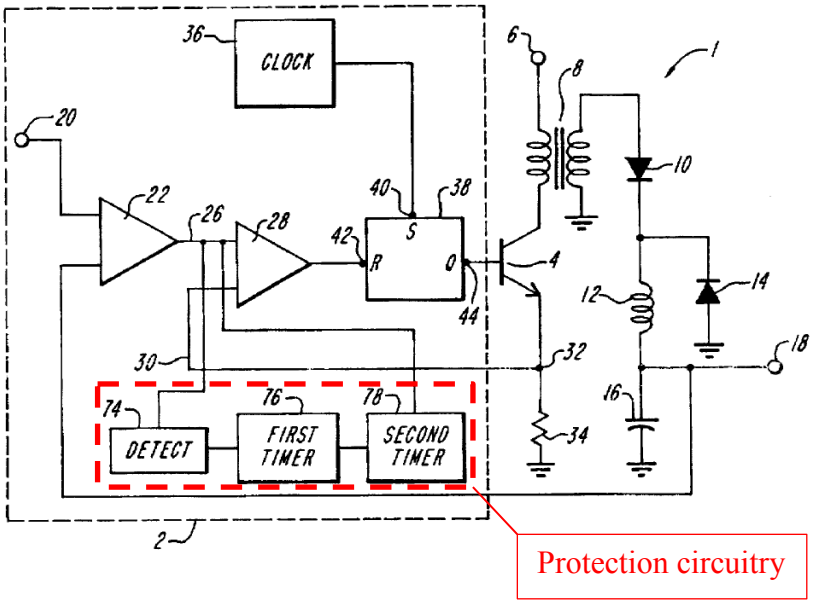
Motivation found in both Hirst and King would have led one of ordinary skill in the art to combine Hirst with the teachings of King to arrive at the claimed invention. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1741-42 (2007); Ex.

1002, ¶ 87.

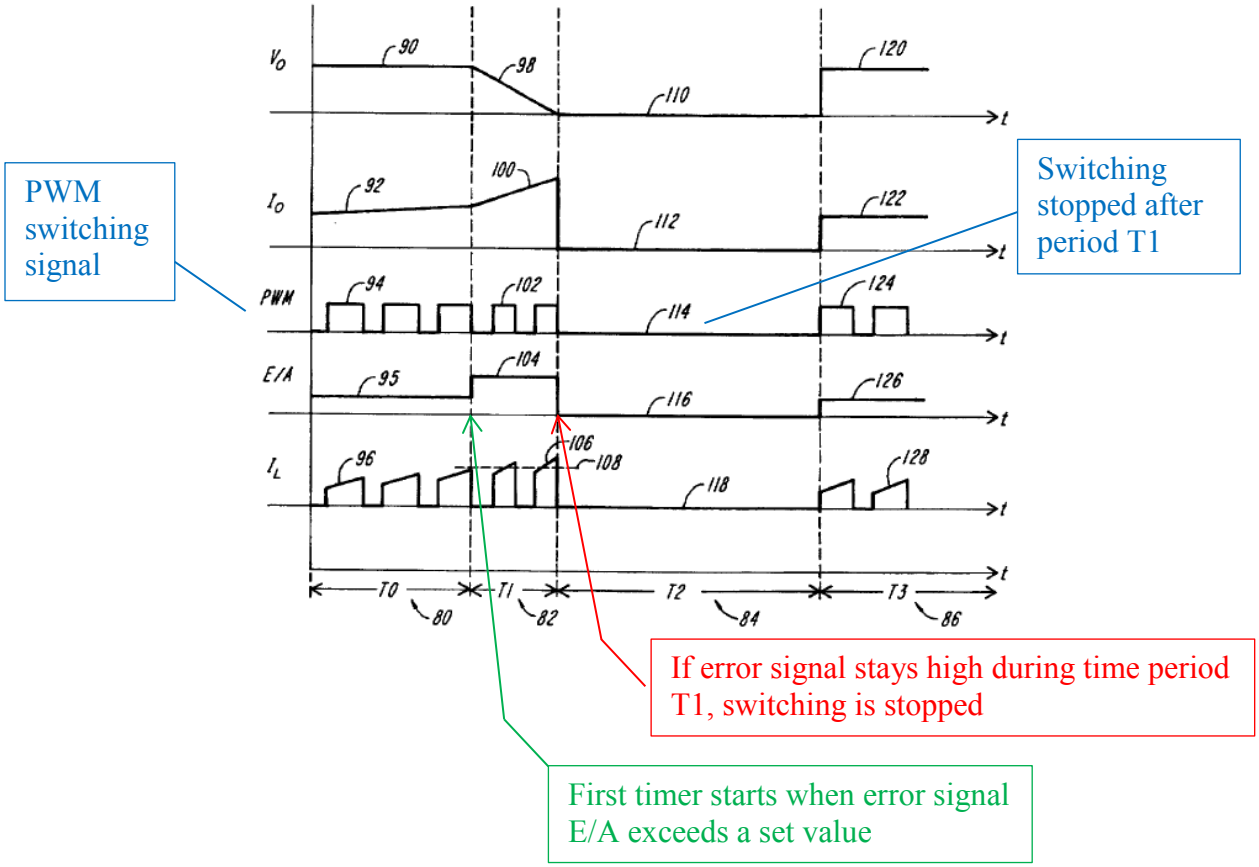
King discloses protection circuitry designed to prevent a switching power supply from being damaged by high voltages or currents when used with variable loads. Ex. 1008, 1:6-10, 2:21-31. King notes that "power supply apparatus, such as dc-to-dc converters, ac-to-dc converters, rectifiers and motor controls, typically incorporates protection circuitry to protect the apparatus from, for example, a short circuit load." Ex. 1008, 1:17-20. King describes a protection technique that offers advantages over prior known techniques. Ex. 1008, 1:21-2:17 (discussing disadvantages of heat sinks, constant-current limiting circuitry, and foldback circuitry); Ex. 1002, ¶ 88. In particular, King notes that "miniaturization of switching power supplies" presents difficulty for prior protection techniques, especially when dealing with variable loads like "motors and devices that have considerable input capacitance." Ex. 1008, 1:39-42, 2:1-17. To overcome these challenges, King discloses protection circuitry that "reduces the likelihood of damage to the power supply apparatus and associated circuitry from such abnormal source and load impedances, yet allows the power supply apparatus to supply adequate power to a variety of variable loads, particularly loads that vary when initially powered." Ex. 1008, 2:42-47. This protection circuitry is "particularly useful in protecting switching-type power supplies, wherein oscillator pulses periodically switch power to an energy storage component, typically an inductor,

for short intervals." Ex. 1008, 2:50-53; Ex. 1002, ¶ 88.

The protection circuitry disclosed in King includes, in one embodiment, a detection circuit **74** and two timing circuits **76** and **78**. *Id.*, 2:61-62, 6:64-7:8.



Ex. 1008, Fig. 1. "The detection circuit monitors a first signal representative of the power delivered to the load." Ex. 1008, 2:61-63, 6:64-7:8. When the first signal exceeds a predetermined value indicative that "potentially damaging currents and/or voltages are likely present" the detection circuit generates a signal that initiates a first timer. Ex. 1008, 2:64-3:1. If the first signal remains excessive for a first period of time, the power output is reduced or terminated for a second period of time by a second timer. Ex. 1008, 3:1-6, 6:64-7:8; Ex. 1002, ¶ 89.



Ex. 1008, Fig. 4.

A person of ordinary skill in the art would be motivated by the express teachings of King to combine the King protection circuitry with the power supply disclosed in Hirst. Ex. 1002, ¶ 90. Hirst describes a switching power supply to power a printer that may include functions like "an electromechanical drive for feeding paper through the print engine **20**, [that] require higher voltages or currents in order to operate properly." Ex. 1006, 4:24-27. Hirst also describes that power supplies for printers may operate for long periods of time at low power consumption to save energy but that they need to be capable of "switching very

rapidly to full power operation on demand (such as when the print engine is active). Ex. 1006, 2:37-41, 4:32-55. A POSITA would recognize that the King circuitry would offer all of the protection advantages described in King while allowing the Hirst power supply to maintain goals of efficiency and the ability to operate at full power on demand. Ex. 1002, ¶ 91. Indeed, the switching power supply of Hirst is quite similar to the exemplary switching power supply disclosed in King, and it is designed to be used in the type of variable load conditions (e.g., activating a print engine) that King's protection technique is designed to accommodate. Ex. 1006, 2:37-41; Ex. 1008, Abstract, 2:42-48; Ex. 1002, ¶ 91. Accordingly, a POSITA would recognize that the protection circuitry from King would improve the Hirst switching power supply in the same way that it improves the King switching power supply. Ex. 1002 ¶ 91; *see KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1731 (2007).

2. Claim 32

"32. The method of claim 26 wherein temporarily increasing the maximum switching frequency of the switch when the load is greater than the power level threshold value includes limiting a time duration that the switch may be switched at up to the increased maximum switching frequency."

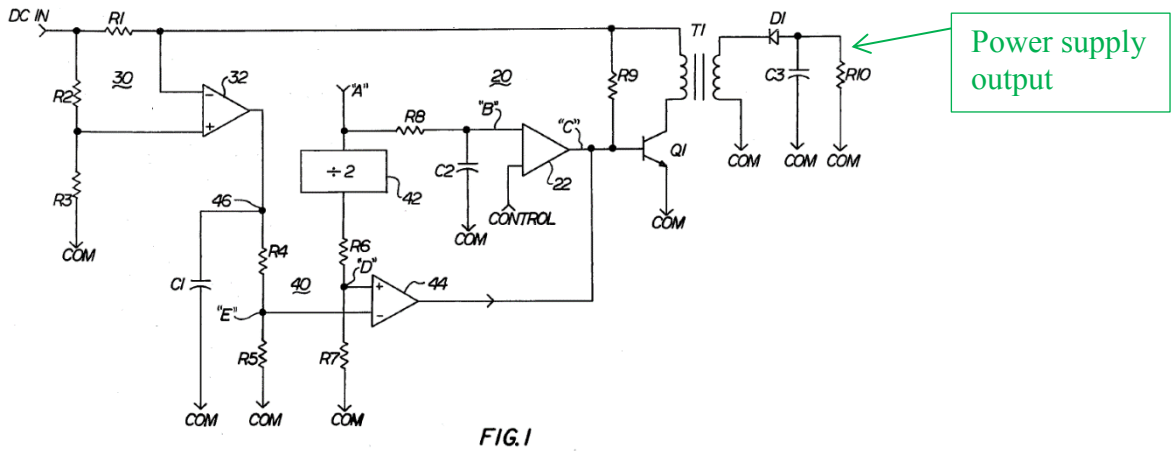
The combination of switching power supply disclosed in Hirst with the protection circuitry disclosed in King discloses each limitation of Claim 32. As

discussed above in Section VI.D.1, King discloses protection circuitry that includes a detection circuit that monitors a signal "representative of the power delivered to the load," and then terminates the switching when that representative signal remains above a threshold for longer than a certain amount of time. As discussed above in Section VI.C.1, the switching regulator in Hirst increases the switching frequency in response to a peak load event (i.e., when the load demand increases beyond a defined threshold). When used in combination with the power supply disclosed in Hirst, the protection circuitry of King would detect the peak load event (just as Hirst does) and then terminate the switching signal after a predetermined time has passed, thereby limiting the time duration that the switch in Hirst may be switched at up to the increased maximum switching frequency. Ex. 1002, ¶ 92.

E. Ground 5: Cates Anticipates Claims 26 and 27 Under 35 U.S.C. § 102

1. Claim 26

26[pre] A method for regulating a power supply output. Cates is directed to efficiently regulating the output of a switching power supply. Ex. 1007, Abstract ("A circuit for use in a p.w.m. type power supply for increasing the efficiency thereof when the supply operates a low power levels."). Figure 1 is a schematic diagram of a switching power supply whose output is regulated.

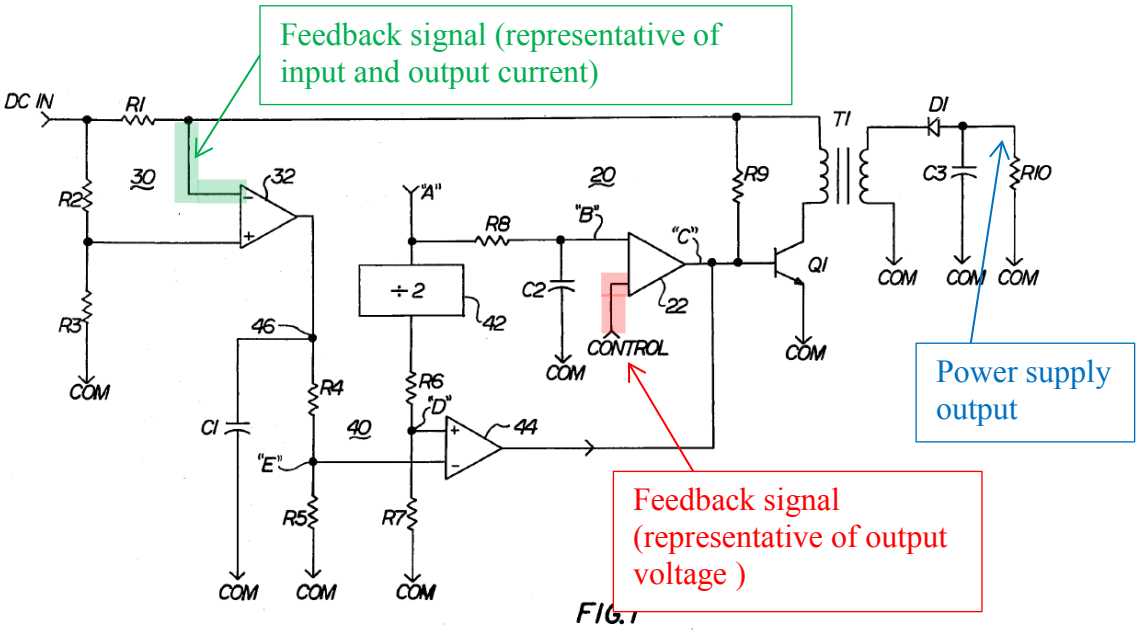


Ex. 1007, Fig. 1 (annotations added). Accordingly, Cates discloses every limitation of claim element 26[pre]. Ex. 1002, ¶ 93.

26[pre]. A method for regulating a power supply output, comprising:	**Cates:** Ex. 1007, 2:12-20: "Referring to FIG. 1 there is shown a schematic circuit diagram of a d-c to d-c switching power supply 10 in accordance with the present invention. Supply **10** includes conventional switching converter **20** which uses the well-known pulse width modulation (p.w.m.) technique to drive power switching transistor Q**1** to thereby provide from a d-c input voltage a regulated d-c output voltage across a load. The load is represented by the resistor R**10**." *See also* Ex. 1007, Abstract, 1:39-46, Figs. 1 & 2.

Claim 26[a] receiving a feedback signal representative of an output level of a power supply output. Figure 1 of Cates shows a power supply that receives a "CONTROL" signal coupled to comparator **22** (i.e., a feedback signal representative of an output level of a power supply output). Ex. 1007, Fig. 1. As Cates describes, this CONTROL signal "is derived as a result of a comparison of a

signal representative of the output voltage of the converter with a reference signal," and it determines the pulse width of the pulses of the control signal at node C based on the load. Ex. 1007, 2:29-31, 2:51-58; Ex. 1002, ¶ 94.



Ex. 1007, Fig. 1. Figure 1 shows a second feedback signal as well (shown in green above as the signal coupled between R1 and operational amplifier **32**). This second feedback signal is representative of the current through the primary side of transformer T1 and through switch Q1. As discussed above in Section VI.A.1, the current through the primary and secondary windings of transformer T1 are proportional to each other based on the number of turns in the primary and secondary windings. Ex. 1002, ¶ 94; Ex. 1015, 8. It was well understood in the art that a measurement of the current through the primary winding of a transformer in

a switching regulator is, as Cates expressly discloses, "representative of the power level at which the supply operates." *See* Ex. 1007, 3:66-4:4; Ex. 1002, ¶ 94. As Cates describes, "resistor R**1** provides a voltage representative of the input current to supply **10** to the inverting input of the comparator. The input current varies with load and decreases as the load decreases. This connection therefore provides to the comparator a signal representative of the power level at which the supply operates." Ex. 1007, 3:66-4:4 (emphasis added). Accordingly, the voltage at R1 (shown in green above) is an additional example of a feedback signal representative of an output level (i.e., current) of a power supply output (indicated in blue above). Alternatively, Cates discloses that a voltage representative of the output power "may also be obtained by the use of suitably arranged circuitry which senses current at the load." Ex. 1007, 4:14-16; Ex. 1002, ¶ 95. A POSITA would be familiar with how to suitably arrange circuitry to sense the current at the load. For example, as was depicted in Hosoya, current through the load can be sensed using a resistor coupled between the switching transistor and ground. *See supra* Section VI.A.1 (claim element 26[a]). Current through the load could also be sensed directly using a sense resistor on the secondary side of the transformer, as would be known to a POSITA. Ex. 1002, ¶ 95. Regardless of how the load current is sensed (on either the primary or secondary side of the transformer), the act of sensing current at the load as Cates describes satisfies the limitation of receiving a

feedback signal representative of an output level of a power supply output. Ex. 1002, ¶ 95.

Accordingly, Cates discloses every limitation of claim element 26[a]. Ex. 1002, ¶ 96.

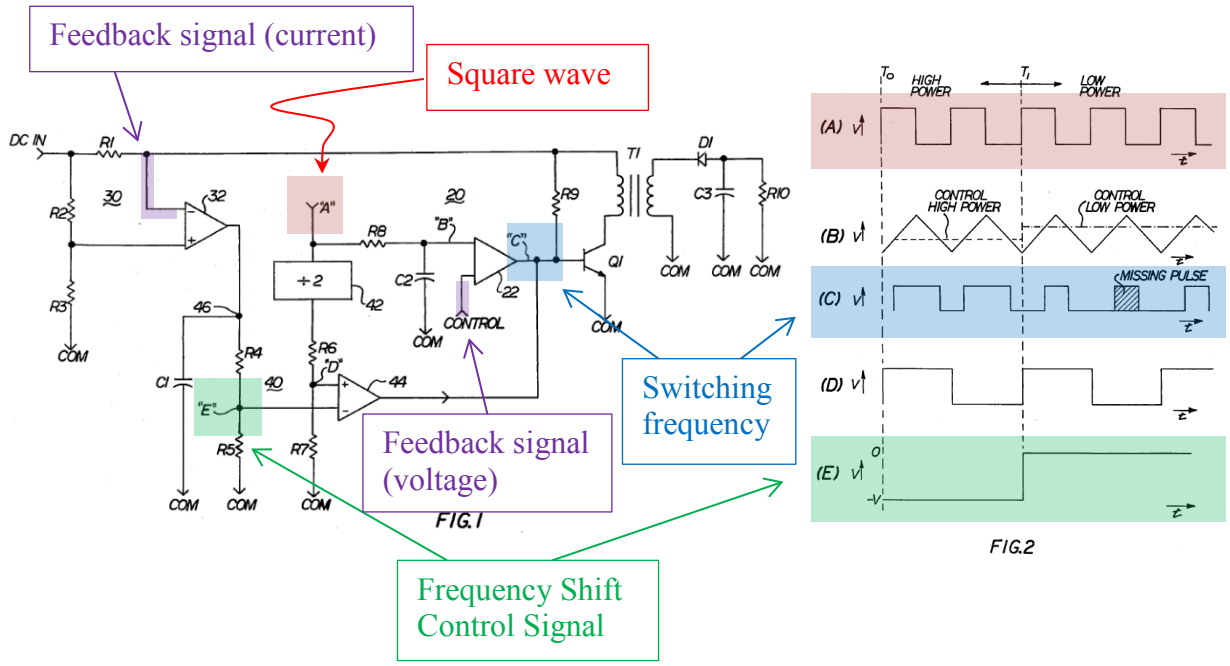
[26a] receiving a feedback signal representative of an output level of a power supply output;	**Cates:** Ex. 1007, 3:66-4:4 (emphasis added): "The resistor R**1** provides a voltage representative of the input current to supply **10** to the inverting input of the comparator. The input current varies with load and decreases as the load decreases. This connection therefore provides to the comparator a signal representative of the power level at which the supply operates." Ex. 1007, 4:10-16 (emphasis added): "While circuit **30** has been shown as including a resistor R**1** to provide from the input current a voltage representative of the power level at which the supply operates, it should be appreciated that this voltage may also be obtained by the use of suitably arranged circuitry which senses current at the load." *See also* Ex. 1007, 2:29-58, Figs. 1 & 2.

Claim 26[b] switching a switch on and off at a switching frequency in response to the feedback signal to regulate the flow of energy from an input of the power supply to the power supply output.[4] Switching transistor Q**1** (i.e., a switch)

[4] The claim language is not clear as to whether the value of the switching frequency is "in response to the feedback signal," or alternatively, whether only "switching a switch on and off" must be "in response to the feedback signal." Cates satisfies the limitation under either interpretation.

is switched on and off by comparator **22** in conjunction with comparator **44** to regulate the flow of energy from DC IN (i.e., an input of the power supply) through to load R**10** (i.e., the power supply output). Ex. 1007, 3:22-31, Figs. 1, 2(A)-(E). Comparator **22** controls the duty cycle of switch Q1 based on CONTROL signal (i.e., a voltage feedback signal) and the sawtooth signal at node B. Ex. 1007, Figs. 1, 2(B), 2(C). Accordingly, Cates discloses switching a switch (i.e., Q1) on and off at a switching frequency in response to the feedback signal (i.e., CONTROL signal) to regulate the flow of energy from an input of the power supply (i.e., DC IN) to the power supply output (i.e., to the load R10); Ex. 1002, ¶ 97.

The switching frequency of switching transistor Q**1** is determined by the square wave at input "A" (shown in Figures 1 & 2) together with the value of the current feedback signal received at the inverting ("-") input of comparator **32**. Ex. 1007, 4:45-5:2; Ex. 1002, ¶ 98.



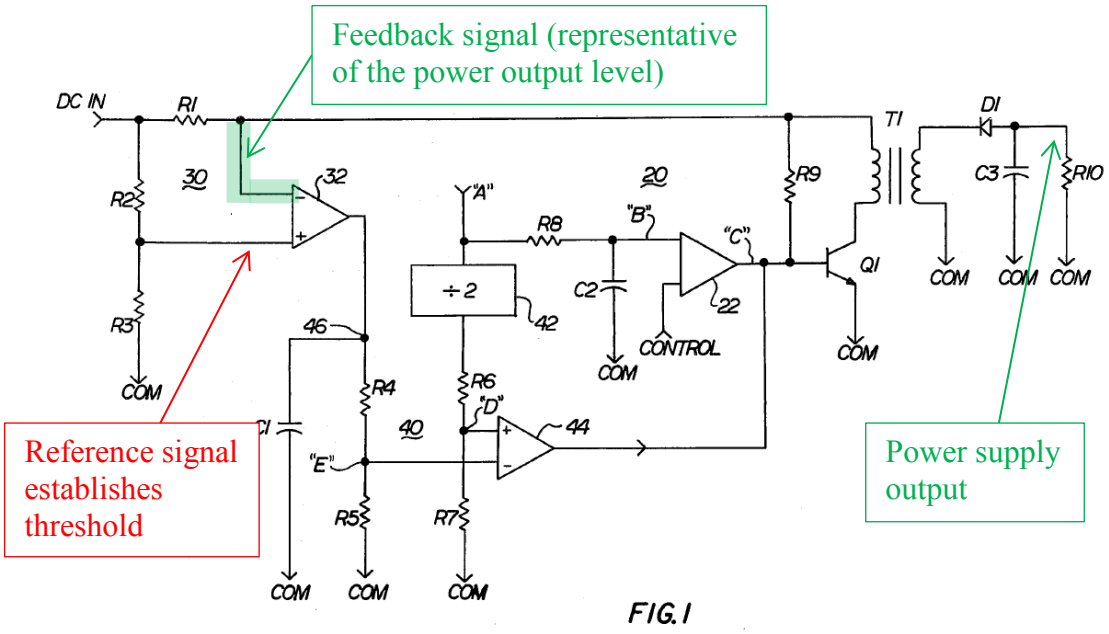
Ex. 1007, Figs. 1 & 2 (annotations added). At high power levels, the inverting input to comparator **32** is greater than the non-inverting input, and the Frequency Shift Control Signal (designated as letter "E") is held at a negative value, causing the switching frequency of Q**1** to match the frequency of square wave "A." Ex. 1007, 4:45-56, Fig. 2. At low power levels, the inverting input to comparator **32** is less than the non-inverting input, forcing the Frequency Shift Control Signal high and causing the switching frequency of Q**1** (i.e., at Node "C") to be reduced to half the frequency of square wave "A." Ex. 1007, 4:57-5:2. Accordingly, the current feedback signal disclosed in Cates is another example of a feedback signal used to switch Q1 on and off at a switching frequency and regulate the flow of energy from an input of the power supply (i.e., DC IN) to the power supply output (i.e., to

the load R10). Ex. 1007, 4:45-56, Figs. 1 & 2; Ex. 1002, ¶ 98.

[26b] switching a switch on and off at a switching frequency in response to the feedback signal to regulate the flow of energy from an input of the power supply to the power supply output;	**Cates:** Ex. 1007, 2:12-20: "Referring to FIG. 1 there is shown a schematic circuit diagram of a d-c to d-c switching power supply **10** in accordance with the present invention. Supply **10** includes conventional switching converter **20** which uses the well-known pulse width modulation (p.w.m.) technique to drive power switching transistor Q**1** to thereby provide from a d-c input voltage a regulated d-c output voltage across a load. The load is represented by the resistor R**10**." Ex. 1007, 3:64-4:1: "A resistor R**1** is connected in the manner illustrated between the input to supply **10** and the inverting input of comparator **32**. The resistor R**1** provides a voltage representative of the input current to supply **10** to the inverting input of the comparator. The input current varies with load and decreases as the load decreases." Ex. 1007, 4:45-5:2: "Circuit **40** operates in the following manner. When the supply **10** is operating at a relatively high power level, the frequency shift control signal has the negative amplitude shown in FIG. **2**(E) for the times between T**0** and T**1**. This negative amplitude appears at the inverting input of comparator **44**. As the comparator is of the type which has an open collector at its output when its inverting input is held negative, the output of the comparator remains high independent of the squarewave appearing at its noninverting input. The high output of comparator **44** has no effect on the width modulated pulses appearing at junction C. When supply **10** begins to operate at the predetermined low power level, the amplitude of the frequency shift control signal rises to become essentially zero. The output of comparator **44** is then free to switch between an open collector and a short circuit at the rate determined by the squarewave present at its noninverting input. Each time the squarewave goes low the output of the comparator goes low to thereby hold junction C low. As shown in FIG. 2(C), this going low of junction C causes the pulse which would be generated at the output of comparator **22** during that time interval to be eliminated. Therefore, only half

	of the pulses that would ordinarily appear at the base of Q**1** actually reach the base." *See also* Ex. 1007, Claim 1, Figs. 1, 2(A)-(E)

Claim 26[c] detecting when a load is greater than a power level threshold value at the power supply output. Comparator **32** detects when a load is greater than a power level threshold. It does this by comparing the voltage at its inverting input, which is "representative of the power level at which the supply operates," with a reference voltage coupled to its non-inverting input (the reference voltage determining the claimed threshold level). Ex. 1007, 3:68-4:4; Ex. 1002, ¶ 99.



Ex. 1007, Fig. 1 (annotations added). As Cates describes "circuit **30** provides at the output of the comparator a signal which has a negative amplitude at high power levels and an essentially zero amplitude at low power levels." Ex. 1007, 4:4-7. The

claimed power level threshold is the power level above which the output of comparator **32** has a negative amplitude. Ex. 1007, 4:4-7, 4:45-54; Ex. 1002, ¶ 99. Accordingly, Cates discloses every limitation of claim element 26[c].

[26c] detecting when a load is greater than a power level threshold value at the power supply output; and	**Cates:** Ex. 1007, 1:46-54: "The circuit has a first means which includes a comparator which is responsive to a signal representative of converter output power level and a signal representative of the predetermined low power level for generating a frequency shift control which has a first amplitude when the output power level is above the reference and a second amplitude when that level is at least equal to if not less than the reference." Ex. 1007, 4:45-54: "When the supply **10** is operating at a relatively high power level, the frequency shift control signal has the negative amplitude shown in FIG. 2(E) for the times between T**0** and T**1**. This negative amplitude appears at the inverting input of comparator **44**. As the comparator is of the type which has an open collector at its output when its inverting input is held negative, the output of the comparator remains high independent of the squarewave appearing at its noninverting input." Ex. 1007, 3:66-4:7 (emphasis added): "The resistor R**1** provides a voltage representative of the input current to supply **10** to the inverting input of the comparator. The input current varies with load and decreases as the load decreases. This connection therefore provides to the comparator a signal representative of the power level at which the supply operates. Thus, circuit **30** provides at the output of the comparator a signal which has a negative amplitude at high power levels and an essentially zero amplitude at low power levels."

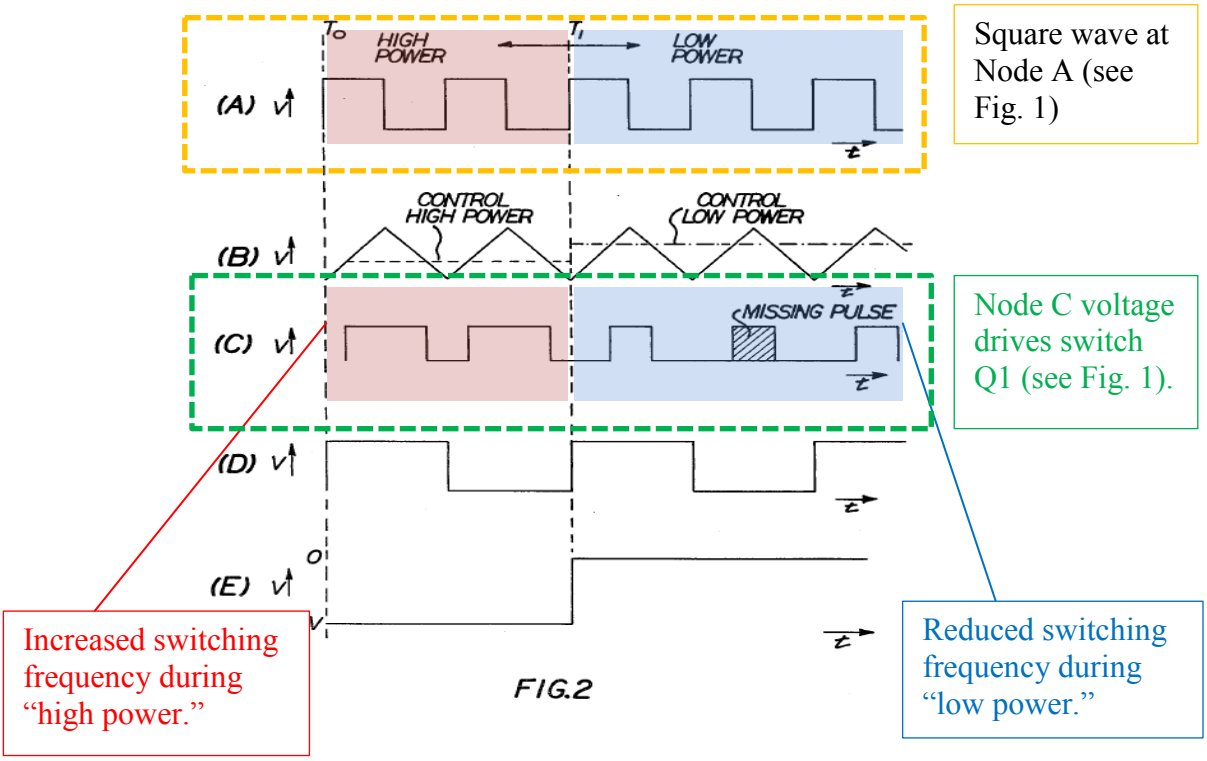
Claim 26[d] temporarily increasing a maximum switching frequency of the

switching frequency of the switch when the load is greater than the power level threshold value. When comparator **32** detects a power level below a predetermined threshold (i.e., when the inverting input is less than the non-inverting input), the Frequency Shift Control Signal ("E") is held at "essentially zero." Ex. 1007, 4:57-59. This allows comparator **44** "to switch between an open collector and a short circuit at the rate determined by the squarewave present at it noninverting input." Ex. 1007, 4:59-63; Ex. 1002, ¶ 100. As a result, junction C is held low each time the square wave goes low. Ex. 1007, 4:63-65. "As shown in FIG. 2(C), this going low of junction C causes the pulse which would be generated at the output of comparator **22** during that time interval to be eliminated. Therefore, only half of the pulses that would ordinarily appear at the base of Q**1** actually reach the base." Ex. 1007, 4:65-5:2, Fig. 2. Thus, at low power levels, the switching frequency of switch Q**1** is reduced to half of the frequency of square wave "A." Ex. 1007, 4:65-5:2, Fig. 2(C); Ex. 1002, ¶ 100.

Conversely, when comparator **32** detects a power level above the predetermined threshold (i.e., when the inverting input is greater than the non-inverting input), the Frequency Shift Control Signal ("E") is held at a negative value. Ex. 1007, 4:57-63, Fig. 2. "This negative amplitude appears at the inverting input of comparator **44**. As the comparator is of the type which has an open collector at its output when its inverting input is held negative, the output of the

comparator remains high independent of the squarewave appearing at its noninverting input." Ex. 1007, 4:49-54. In other words, when a power level above a threshold is detected, the maximum switching frequency of Q**1** increases to match the frequency of square wave "A." Ex. 1007, 4:45-56, Fig. 2; Ex. 1002, ¶ 101.

This increase in maximum switching frequency is temporary because it is responsive to the fluctuating power level of the load. Ex. 1007, 4:45-5:2, Fig. 2(E); Ex. 1002, ¶ 102. In addition, Cates describes an example in which the power level transitions from a high to a low level to generate the signals shown in Figure 2. Ex. 1007, 3:45-52 ("[I]t is assumed in FIG. 2 that for the interval of time between T0 and T1 supply **10** operates at a relatively constant high power level. Also for the purposes of illustration, it is assumed that at time T1 converter **20** instantaneously begins to operate at a low power level.") (emphasis added).



Ex. 1007, Fig. 2 (annotations added). Accordingly, Cates discloses every limitation of claim element 26[d]. Ex. 1002, ¶ 102.

[26d] temporarily increasing a maximum switching frequency of the switching frequency of the switch when the load is greater than the power level threshold value.	**Cates:** Ex. 1007, 4:45-54: "When the supply 10 is operating at a relatively high power level, the frequency shift control signal has the negative amplitude shown in FIG. 2(E) for the times between T**0** and T**1**. This negative amplitude appears at the inverting input of comparator **44**. As the comparator is of the type which has an open collector at its output when its inverting input is held negative, the output of the comparator remains high independent of the squarewave appearing at its noninverting input." *See also* Ex. 1007, 4:55-5:2, Figs. 1, 2(A)-2(E).

2. Claim 27

"27. The method of claim 26 wherein switching the switch in response to the feedback signal to regulate the flow of energy from the power supply input to the power supply output comprises pulse width modulating a control signal driving the switch." Cates describes a "conventional switching converter **20** which uses the well-known pulse width modulation (p.w.m.) technique to drive power switching transistor Q**1** to thereby provide from a d-c input voltage a regulated d-c output voltage across a load." Ex. 1007, 2:15-19. In Figure 1, node C is an example of the claimed control signal driving transistor Q**1** (i.e., the switch). Cates discloses that "[t]he width of the pulses is dependent upon the load connected to supply **10** and therefore increases to become a larger percentage of the period of the sawtooth waveform as the supply approaches essentially full load operation." Ex. 1007, 2:54-58; *see also id.*, 2:35-53, 2:65-3:2, Fig. 1. Accordingly, Cates discloses every limitation of claim element 27. Ex. 1002, ¶ 103.

VII. CONCLUSION

Petitioner respectfully requests that *inter partes* review of the '119 Patent be instituted and that claims 26, 27, and 32 be cancelled as unpatentable under 35 U.S.C. § 318(b).

Respectfully submitted,
BAKER BOTTS L.L.P.

November 7, 2017
Date

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition, exclusive of the exempted portions as provided in 37 C.F.R. § 42.24(a), contains no more than 13,717 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24(a). The word count was calculated by starting with Microsoft Word's total document word count and subtracting the words for the Table of Contents, the Exhibit List, the Mandatory Notices, the Certificate of Compliance, and the Certificate of Service.

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CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on the 7th day of November, 2017, a complete and entire copy of the **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,239,119** and any accompanying exhibits was served on the patent owner at the correspondence address of record for the subject patent,

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via Express Mail or by means at least as fast and reliable as Express Mail. Additionally, the same were also served upon counsel for the subject patent's owner, Power Integrations, Inc.,

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because that is likely to affect service.

In accordance with § 42.51(b)(1), the undersigned certify that Petitioner is not aware of, and therefore does not provide any "relevant information that is inconsistent with a position advanced by petitioner[]."

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