UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORP., UMC GROUP (USA), SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORP., SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORP., SEMICONDUCTOR MANUFACTURING INTERNATIONAL (BEIJING) CORP., and SMIC, AMERICAS
Petitioner

v.

LONE STAR SILICON INNOVATIONS LLC
Patent Owner

CASE: IPR2017-01513
U.S. PATENT NO. 5,973,372

PETITION FOR *INTER PARTES* REVIEW

Mail Stop PATENT BOARD
Patent Trial and Appeal Board
United States Patent and Trademark Office
PO Box 1450
Alexandria, Virginia 22313–1450

Table of Contents

Page

List of Exhibits

Ex. 1001: U.S. Patent No. 5,973,372 ("'372 Patent").

Ex. 1002: Declaration of R. Jacob Baker, Ph.D., P.E.

Ex. 1003: *Curriculum vitae* of R. Jacob Baker, Ph.D., P.E.

Ex. 1004: Prosecution History of U.S. Patent No. 5,973,372.

Ex. 1005: English-Language Translation of Japanese Patent Publication No. JP08-204187, Japanese-Language Version of Japanese Patent Publication No. JP08-204187, and Translation Certification ("*Saito*").

Ex. 1006: PCT Application No. WO 96/20499 ("*Chau*").

Ex. 1007: U.S. Patent No. 5,409,853 to Yu ("*Yu*").

Ex. 1008: U.S. Patent No. 4,998,150 to Rodder et al. ("*Rodder*").

Ex. 1009: English-Language Translation of Japanese Patent Publication No. JP08-018049, Japanese-Language Version of Japanese Patent Publication No. JP08-018049, and Translation Certificate ("*Ogasawara*").

Ex. 1010: R. Jacob Baker, Harry W. Li and David. E. Boyce, *CMOS Circuit Design, Layout, and Simulation* (IEEE Press, 1997).

Ex. 1011: Robert H. Dennard, Fritz H. Gaensslen, Hwa-Nien Yu, V. Leo Rideout, Ernest Bassous, and Andre R. LeBlanc, *Design of Ion-Implanted MOSFETs with Very Small Physical Dimensions*, IEEE

Journal of Solid-State Circuits, Oct. 1974, at 256.

Ex. 1012: R. W. Mann, L. A. Clevenger, P. D. Angello, and F. R. White, *Silicides and Local Interconnections for High-Performance VLSI Applications*, IBM Journal of Research Development, Vol. 39, July 1995, at 403.

Ex. 1013: S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era* (Lattice Press, 1986)[1].

Ex. 1014: Lone Star Silicon Innovation LLC's Preliminary Claim Constructions Pursuant To P.R. 4-2(a) from Case No. 2:16-cv-01170-JRG-RSP (LEAD CASE).

[1] Throughout this petition, citations to this exhibit will refer to the original textbook page number.

MANDATORY NOTICES (37 C.F.R. § 42.8)

A. Real Parties-In-Interest

The following entities are the real parties in interest:

- United Microelectronics Corporation, located at No. 3 Li-Hsin Road II, Hsinchu Science Park, Hsinchu City, Taiwan, Republic of China;
- UMC Group (USA), located at 488 De Guigne Drive, Sunnyvale, CA 94085-3903;
- Semiconductor Manufacturing International Corporation, located at 18 Zhangjiang Road, Pudong New Area, Shanghai, 201203, People's Republic of China;
- Semiconductor Manufacturing International (Shanghai) Corporation, located at 18 Zhangjiang Road, Pudong New Area, Shanghai, 201203, People's Republic of China;
- Semiconductor Manufacturing International (Beijing) Corporation, located at 18 Wenchang Avenue, Economic-Technological Development Area, Beijing 100176, People's Republic of China; and
- SMIC, Americas 1732 N. 1st Street, Suite 200, San Jose, California 95112.

B. Related Matters

Patent Owner Lone Star Silicon Innovations LLC ("PO" or "Lone Star") is presently asserting U.S. Patent No. 5,973,372 ("'372 Patent") against United Microelectronics Corporation and UMC Group (USA) in the Eastern District of Texas in Case No. 2:16-cv-01216-JRG-RSP. PO is also presently asserting the '372 Patent against Semiconductor Manufacturing International Corp., Semiconductor Manufacturing Int'l. (Shanghai) Corp., Semiconductor Manufacturing Int'l. (Beijing) Corp., and SMIC, Americas in the Eastern District of Texas in Case No. 2:16-cv-01276-JGR-RSP.

C. Lead and Backup Counsel and Service

Lead Counsel	Backup Counsel
Benjamin E. Weed Reg. No. 65,939 K&L Gates LLP 70 W. Madison Street, Suite 3100 Chicago, IL 60602 benjamin.weed.PTAB@klgates.com T: (312) 781-7166 F: (312) 827-8152	**Jay C. Chiu** Reg. No. 47,308 K&L Gates LLP 1 Park Plaza, Twelfth Floor, Irvine, CA 92614 jay.chiu@klgates.com T: (949) 253-0900 F: (949) 253-0902 **Tina Thomas** Reg. No. 75,089 K&L Gates LLP 70 W. Madison Street, Suite 3100 Chicago, IL 60602 tina.thomas@klgates.com T: (312) 807-4283 F: (312) 827-2497 **Jeffrey L. Johnson** Reg. No. 53,078 Orrick, Herrington & Sutcliffe LLP 1301 McKinney Street, Suite 4100 Houston, TX 77010-3096 3j6ptabdocket@orrick.com T: (713) 658-6450 F: (713) 658-6401

Petitioner consents to electronic service by email.

I. INTRODUCTION

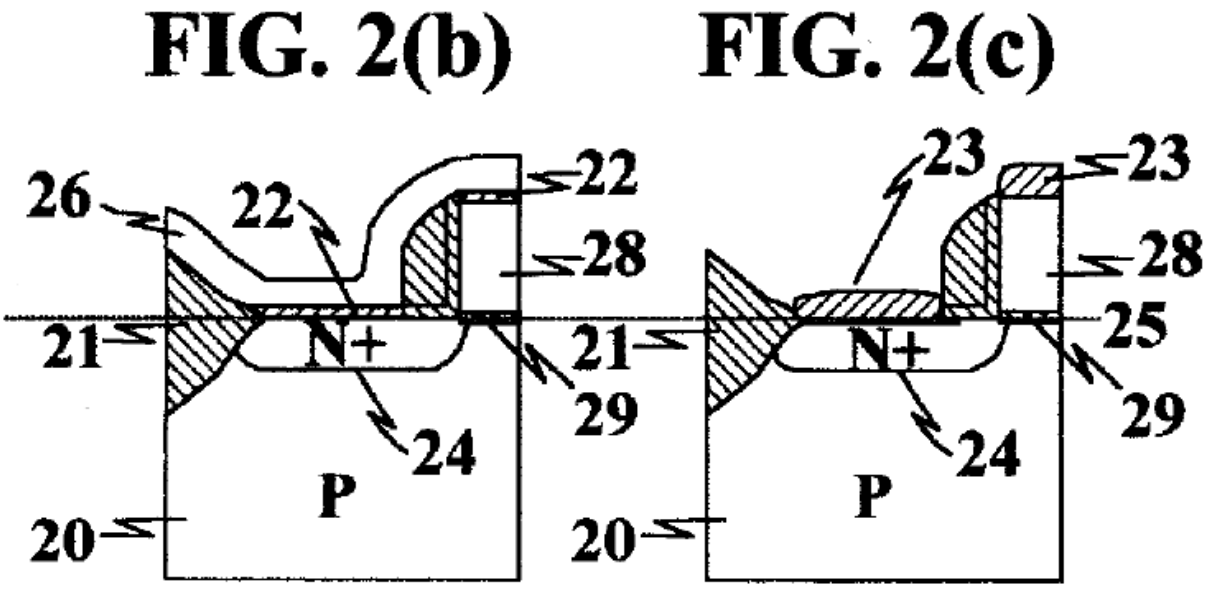
United Microelectronics Corporation, UMC Group (USA), Semiconductor Manufacturing International Corporation, Semiconductor Manufacturing International (Shanghai) Corporation, Semiconductor Manufacturing International (Beijing) Corporation, and SMIC, Americas (collectively, "Petitioner") request *Inter Partes* Review ("IPR") of claims 1 and 4-6 of U.S. Patent No. 5,973,372 ("'372 Patent") (Ex. 1001) under 35 U.S.C. §§ 311–319.

The '372 Patent describes a method of forming "a metal silicide at a shallow junction in a single crystal substrate without encroaching on the shallow junction." (Ex. 1001, Abstract). As part of this process, the '372 Patent requires a titanium silicide layer to be formed by thermally annealing amorphous silicon deposited over a titanium film. (Ex. 1001, Abstract). The '372 Patent, however, acknowledges that during this anneal, "titanium silicide 23 is formed by reacting the titanium 22 with the amorphous silicon 26 ***and slightly with the silicon substrate*** … ." (Ex. 1001, 4:38-41; emphasis added). To ensure that the silicide remains above the original surface of the silicon substrate, the '372 Patent discloses that after the first anneal to form titanium silicide, an epitaxial layer is formed *between* the silicide and the underlying substrate:

> [w]ith a thick amorphous silicon layer 26, which is sufficiently thick so as to not be totally consumed by the silicidation, silicon atoms from

> the amorphous silicon layer migrate through the titanium silicide 23 and to the single crystal silicon substrate and, in accordance with the device structure of the present invention, form a solid phase epitaxy layer as shown in the vicinity of the silicide and the N+ boundary in FIG. 2(c).

(Ex. 1001, 4:62-5:3; Ex. 1002, ¶¶34-36). FIGS. 2(b) and 2(c) of the '372 Patent illustrate this result (albeit without a clear illustration of the "solid phase epitaxy layer") and are reproduced below:



(Ex. 1001, FIGS. 2(b) and 2(c); Ex. 1002, ¶¶34-36).

Notwithstanding the fact that the '372 Patent focuses on an allegedly novel *manufacturing method*, the challenged claims of the '372 Patent are apparatus claims directed to an "integrated circuit" having a shallow junction for each of a source and drain, a metal silicide layer, and an epitaxial silicon layer between the

shallow junctions and the metal silicide layer. (Ex. 1001, 7:41-8:9). As explained herein, the *structure* of the integrated circuit is far from novel—several references unconsidered during examination disclose the recited structure. Moreover, even if certain manufacturing steps are interpreted as part of the claims (as should be the case here under the applicable district court claim construction standard), the prior art (including a Japanese patent publication referred to herein as *Saito*, Ex. 1005) plainly discloses achieving the known apparatus using the same process disclosed in the '372 Patent. Either way, the claims of the '372 Patent are invalid.

II. TECHNOLOGICAL BACKGROUND

A. Overview of Technology

The '372 Patent relates to integrated circuit fabrication and, in particular, to reducing the resistance associated with terminals of integrated transistors. (Ex. 1002, ¶19; Ex. 1001, 1:12-19). Understanding the basic technology flow for CMOS transistor formation is therefore useful; the diagram below, from a prior art textbook titled *CMOS Circuit Design, Layout, and Simulation* (Ex. 1010), summarizes this flow:

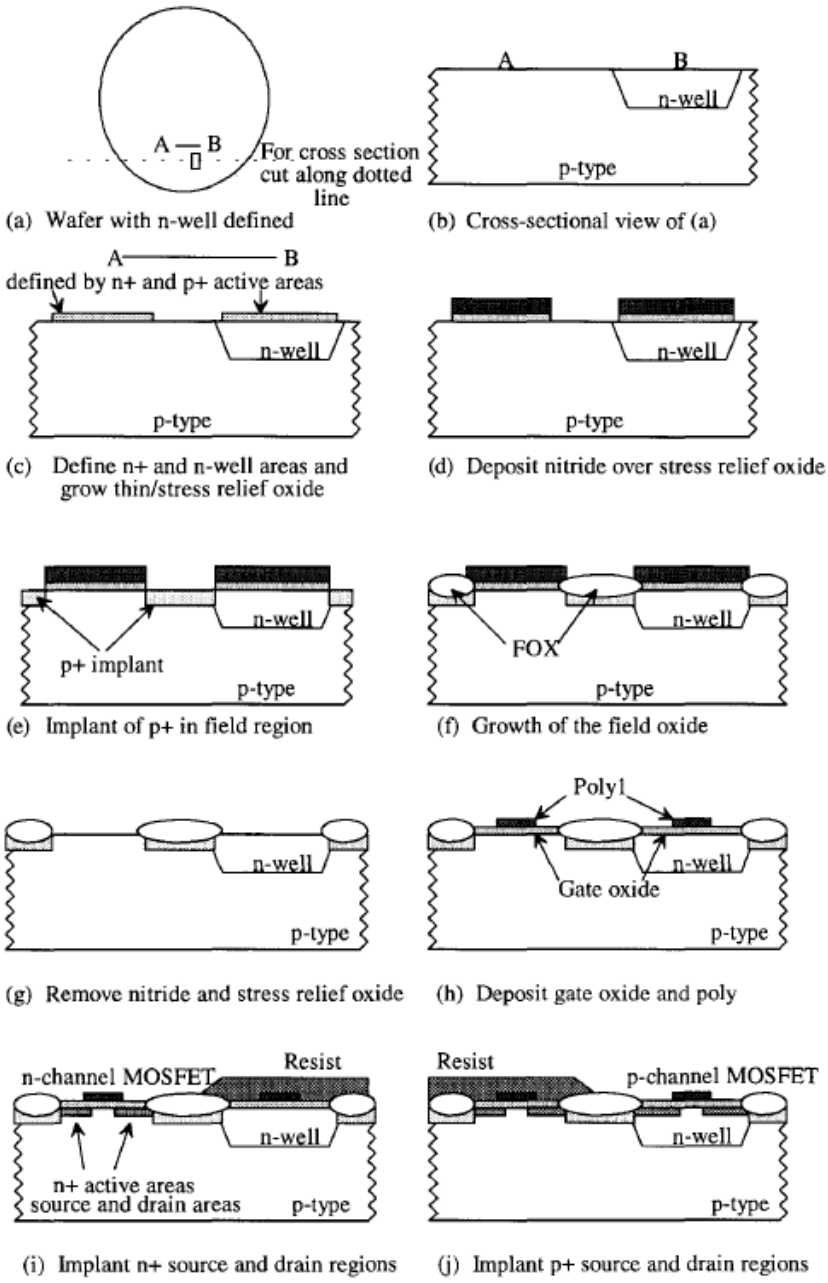


Figure 4.10 Sequence of events used in MOSFET formation.

(Ex. 1010, Figure 4.10; Ex. 1002, ¶¶20-21). An n-channel MOSFET ("NMOS") is depicted in the left of each figure and a p-channel MOSFET ("PMOS") is depicted on the right of each figure. (*Id.*). As Figure 4.10(c) suggests, the fabrication process begins when an n+ and n- well area is formed and a thin stress relief oxide

is grown on top of the active areas of the p-substrate and n-well. (*Id.*). Next, nitride is deposited on top of the stress relief oxide and areas not covered by the nitride are implanted using a p-field implant. (*Id.*). Not shown in Figure 4.10 are the steps involved in forming an n-field implant. (Ex. 1002, ¶22). After the field implants are in place, field oxide is grown and the nitride and stress relief oxides are removed. (Ex. 1010, Figure 4.10). Next, gate oxide and polysilicon are deposited and a resist is also deposited over the n-well region in order to mask the n-well region. (*Id.*). The n+ region is then implanted with dopants. (*Id.*). Next, the resist is removed from the n-well region, and the n+ region is covered with the resist in order to mask the n+ region. The wafer is again implanted with dopants. (*Id.*).

Typically, the sheet resistances for polysilicon are on the order of 20 Ω/square. (Ex. 1002, ¶23). In order to lower the sheet resistance of the polysilicon, a refractory metal and polysilicon mixture called silicide is deposited on top of the polysilicon. (*Id.*). This silicide/polysilicon sandwich is referred to as a polycide gate. The typical sheet resistances of polycide gates are 2-3 Ω/square. (*Id.*).

B. The Migration to Shallow Junction Transistors

The concept of scaling down the size of transistors is generally understood to have been first introduced in 1974. (*See* Ex. 1011, Fig. 1; Ex. 1002, ¶24). The

problems associated with this scaling, including an increase in sheet resistance due to a shorter channel length, also became known at this time. (Ex. 1002, ¶¶24-25). The higher resistance of these junctions caused an increase in the resistance in series with the MOSFET. (*Id.*). When the MOSFET was used as a switch, the increase in resistances lead to slower circuits. (*Id.*). This was highly undesirable. (*Id.*).

In order to improve issues caused by the higher sheet resistance of the source and drain, a refractory metal and polysilicon mixture could be deposited on top of the polysilicon, as well as on the source/drain regions. (Ex. 1002, ¶26). The substrate is then annealed, resulting in the formation of titanium silicide ($TiSi_2$). (*Id.*). This layer is frequently referred to as a self-aligned silicide or simply as a *salicide*. (*Id.*).

C. Silicide Formation with Amorphous Silicon

When a silicide is formed as described above, the titanium consumes the underlying silicon as part of the reaction that leads to silicide formation; in this process, after formation, the silicide generally sits below the top edge/surface of the silicon wafer due to the consumption of a portion of the silicon wafer to form the silicide. (Ex. 1002, ¶27). As MOSFETs scale to smaller dimensions, this consumption of the thinner and thinner substrate becomes undesirable. (*Id.*). One

solution to this problem is detailed in the below figure, which is taken from a survey paper published by IBM in July 1995:

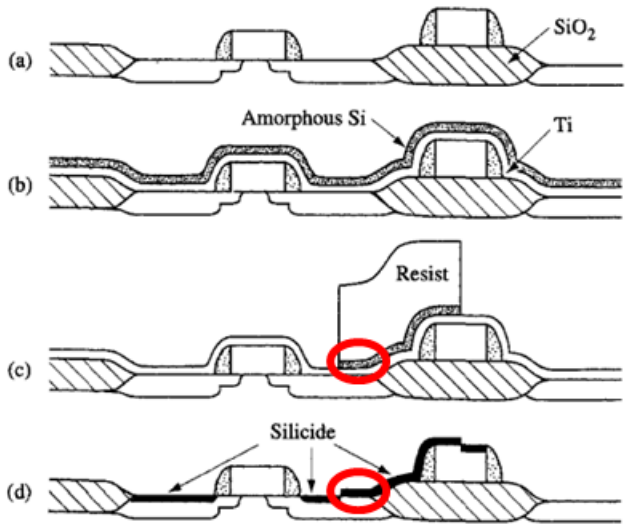


Figure 19

Process flow for forming $TiSi_2$-based local interconnections. After forming the MOSFET devices (a), a blanket layer of Ti and amorphous silicon are deposited (b). A masking resist layer is used to pattern the amorphous silicon (c). The resist is stripped, and a high-temperature annealing step is then carried out to cause the titanium which is in contact with silicon to form $TiSi_2$. Selective etching is then used to remove the TiN and unreacted titanium (d).

(Ex. 1012, 412; emphasis added).

After MOSFET formation, as shown above in Figure 19 of Ex. 1012, a layer of titanium is deposited over the devices, followed by a layer of amorphous silicon. (*Id.*). Next, a resist layer is used to mask portions of the amorphous silicon, patterning the amorphous silicon as in Figure 19(c). (*Id.*). Next, the resist is

removed and the substrate is annealed to form $TiSi_2$ (silicide). (*Id.*). Figure 19(d) demonstrates what those of skill in the art generally understand: that the titanium forms a silicide with the amorphous silicon layered above more quickly than the crystalline silicon below. (Ex. 1012, 412; Ex. 1002; ¶28). In the resulting structure, the titanium silicide does not extend as deeply into the source/drain region, as much less of the silicon substrate is consumed in formation of the titanium silicide. (*Id.*). Thus, shallower junctions can be formed when upper amorphous silicon is used to form the silicide layer. (Ex. 1002, ¶27). This technique was well known in the art at least as early as 1995 (two years before the filing of the '372 Patent). (Ex. 1002, ¶28).

D. Epitaxial Silicon Growth

In semiconductor processing, epitaxial growth of silicon refers to a process for growing silicon on another silicon material. (Ex. 1002, ¶29). In this process, the grown silicon has the same crystalline orientation as the underlying silicon. (*Id*.). In other words, if a single crystalline epitaxial layer is grown, that means the underlying substrate is also single crystalline silicon.

Those of skill in the art understand that, given the ubiquity of epitaxial silicon formation in semiconductor fabrication, drawings of fabrication processes often do not illustrate the formation of epitaxial layers. (Ex. 1002, ¶¶29-30). That is, while epitaxial layers are often necessarily formed, it is very common for those

layers not to be illustrated in drawings of semiconductor fabrication processes. (*Id*.). As illustrated below, the use of the epitaxial layer does not affect the overall function of the device, but instead it simply allows a higher impurity p-type substrate to be used. (Ex. 1010, Figure 2.1; Ex. 1002, ¶30).

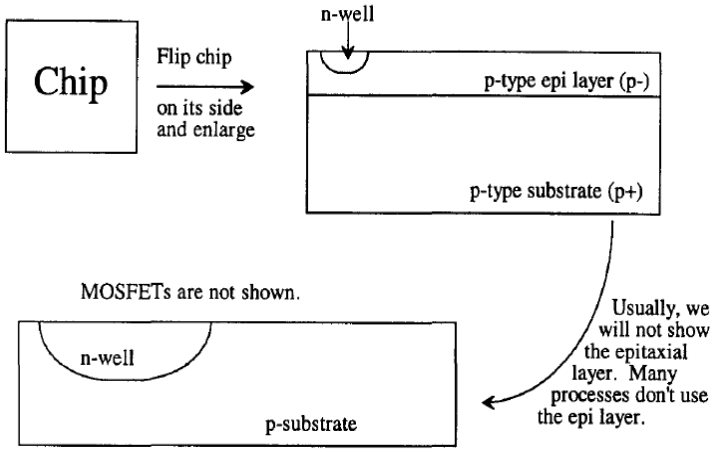


Figure 2.1 Illustration of the top and side view of a die.

(Ex. 1010, Figure 2.1; Ex. 1002, ¶30).

Those of skill in the art, therefore, are generally not surprised to read about epitaxial layer formation without seeing an illustration of such a layer in images summarizing semiconductor fabrication processes. (Ex. 1002, ¶¶29-30).

III. U.S. PATENT NO. 5,973,372

A. '372 Patent Overview

The '372 Patent, which was filed on December 6, 1997, discusses how to fabricate an integrated circuit that has a metal silicide layer formed on top of a shallow junction. (Ex. 1001, 1:64-67; Ex. 1002, ¶31). It purports to solve

problems associated with shrinking dimensions: as "the shallow junction becomes ever more shallow and the result is degrading of the integrity of the shallow junction." (Ex. 1001, 4:16-18; Ex. 1002, ¶32).

To address these problems, the '372 Patent discloses that, after junctions are formed, deposition of a refractory metal, such as titanium, is performed on the surface of the substrate. (Ex. 1001, 5:50-58; Ex. 1002, ¶32). Next, a layer of silicon-containing material, preferably amorphous silicon, is deposited on top of the titanium layer. (Ex. 1001, 5:58-65; Ex. 1002, ¶32). The substrate is then annealed at a temperature of about 650C, which initiates a silicidation process, creating a layer of titanium silicide. (Ex. 1001, 6:19-26; Ex. 1002, ¶32). The amorphous silicon is of a thickness so that the majority of the refractory metal reacts with the amorphous silicon and only a small amount of the silicon substrate is consumed during the silicide reaction. (*Id.*).

The '372 Patent states that the titanium silicide will reach the correct phase, phase C54, only after two annealing processes have been conducted. (Ex. 1001, 6:26-33; Ex. 1002, ¶33). Further, in one embodiment of the '372 Patent (illustrated in FIGS. 2(b) and 2(c)), silicon atoms from the remaining amorphous silicon (following completion of the $TiSi_2$ formation process) migrate through the newly created titanium silicide to the single crystal silicon substrate and form a solid

phase epitaxy layer in the vicinity of the N+ boundary. (Ex. 1001, 4:62-5:3; Ex. 1002, ¶33).

B. Prosecution History of the '372 Patent

The application that issued as the '372 Patent was filed on December 6, 1997. (Ex. 1004, 3). Petitioner is unaware of any patent term adjustments or extensions that apply to the term of the '372 Patent, so Petitioner believes that the '372 Patent will expire on December 6, 2017, during the pendency of this proceeding.

The Examiner issued a non-final office action on July 29, 1998, rejecting the pending claims under 35 U.S.C. §§ 112 and 102(b). (Ex. 1004, 70-72). The prior art rejection under 35 U.S.C. § 102(b) relied on U.S. Patent No. 5,225,896 to Van Roozendaal et al. (*Id.*). In response to this rejection, Applicant attempted to distinguish the pending claims from the prior art by arguing that the prior art disclosed an epitaxial layer that was part of the starting substrate, not one formed from amorphous silicon. (Ex. 1004, 84). Further, Applicant argued that its claims were distinguishable because in the prior art all of the amorphous silicon was consumed during the formation of titanium silicide; therefore, no amorphous silicon remained to create the epitaxial layer. (*Id.*).

In response, the Examiner allowed pending claim 5, and rejected the remaining claims under newly cited U.S. Patent No. 5,416,034 to Bryant.

(Ex. 1004, 86). The Applicant conducted an Examiner interview and thereafter further amended the claims and argued for patentability. (Ex. 1004, 89-97). Specifically, Applicant argued that:

> [T]he Bryant reference was discussed and the Examiner stated that if Claim 1 recited that the metal silicide and epitaxial layer structure were adjacent the shallow junctions of both a source and drain of an [sic] field effect transistor, this would patentable distinguish [the pending claims] over the Bryant reference. Further, if original Claim 5 to a bipolar transistor was written in independent form, the Examiner stated that such a claim would be patentable distinct from the Bryant reference.

(Ex. 1004, 95). The Applicant also characterized the pending claims as requiring a thin epitaxial silicon layer to provide a non-resistive path to the metal silicide for both the source and drain of the same field effect transistor and the emitter of a bipolar transistor. (Ex. 1004, 96).

Apparently agreeing with Applicant's arguments and claim amendments, the Examiner allowed the claims on May 20, 1999, and the '372 Patent issued on October 26, 1999. (Ex. 1004, 99-101).

C. The Petition Relies on Previously Unapplied Prior Art

None of the references supporting the proposed Grounds in this Petition were previously considered by the Patent Office during examination of the '372 Patent. Additionally, this Petition relies on a declaration of R. Jacob Baker, Ph.D.,

P.E., an expert in the field of the '372 Patent and the prior art, which was also not considered during examination. (*See* Ex. 1002). The Board should institute IPR in light of 35 U.S.C. § 325(d).

IV. GROUNDS FOR STANDING (37 C.F.R. § 42.104(a))

Petitioner certifies that (1) the '372 Patent is available for IPR; (2) Petitioner is not barred or estopped from requesting an IPR on the Grounds identified herein; and (3) Petitioner has not filed a complaint relating to the '372 Patent.

V. PAYMENT OF FEES (37 C.F.R. §§ 42.15 AND 42.103)

Petitioner authorizes the USPTO to charge any required fees to Deposit Account 02–1818.

VI. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (referred to herein as a "POSA") is a hypothetical person who is presumed to know the relevant prior art. (*See Gnosis S.P.A et al. v. S. Ala. Med. Sci. Foundation*, Case IPR2013-00116, Paper 68 at 9, 37 (PTAB June 20, 2014)). A POSA has ordinary creativity, is not an automaton, and is capable of combining teachings of the prior art. (*Id*. (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 420-421 (2007))).

With respect to the '372 Patent, a POSA as of December 6, 1997, would have had a bachelor's or master's degree in electrical engineering, materials science, or a closely related field and two to three years of academic or industry

experience in the field of semiconductor processing. (Ex. 1002, ¶¶17-18). A person with less education, but more relevant industry experience, or a person with more education, but less relevant industry experience, may also meet this standard. (Ex. 1002, ¶¶17-18).

VII. CLAIM CONSTRUCTION

In accordance with 37 C.F.R. § 42.100(b), the challenged claims of the '372 Patent must be given their "broadest reasonable construction in light of the specification" of the '372 Patent. (37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, No. 15-446, slip op. at 20 (U.S. June 20, 2016)).

Under this standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a POSA in the context of the entire disclosure. (*In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007)). If a special definition for a claim term is proffered, it must be described in the specification "with reasonable clarity, deliberateness, and precision." (*In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994)).

In the event PO files a motion, as it is permitted to do, certifying that the '372 Patent will expire prior to the conclusion of this proceeding, the district court claim construction standard, such as articulated in *Phillips v. AWS Corp.*, applies. 415 F.3d 1303 (Fed. Cir. 2005). Indeed, Petitioner believes that the '372 Patent *will* expire during this proceeding, as Petitioner believes the '372 Patent will expire

on December 6, 2017. Thus, Petitioner believes that the *Phillips* district-court-type claim construction standard should apply here.

Regardless of the claim construction standard applied, Petitioner believes that the constructions described below should be adopted.[2] In particular, the proposed constructions constitute the *only* reasonable way a person of skill in the art would read the claims of the '372 Patent and these constructions are thus mandated by the intrinsic record.

---

[2] Lone Star served its Preliminary Claim Constructions in a consolidated case involving the '372 Patent, on June 7, 2017. (Ex. 1014, 3-4). Petitioner asserts that for purposes of this Petition, no terms, other than those proposed herein, need construction. Further, although Lone Star proposes that the term "adjacent" requires no construction, Petitioner submits that, for the reasons articulated herein, the term adjacent does require construction. Petitioner also submits that Lone Star may still present the construction of "adjacent" described herein as a potential PO construction in this proceeding despite not proposing that construction in the district court litigation. Nonetheless, under the constructions proposed by Lone Star, the prior art presented in this petition still applies to the claim terms as construe by Lone Star, and renders obvious the claims of the '372 Patent.

Other than the terms specifically addressed below, Petitioner submits that a POSA would have understood each term of each of the challenged claims of the '372 Patent to have its ordinary and customary meaning.

A. "metal silicide layer … disposed adjacent the shallow junction" and "epitaxial silicon layer … disposed between said upper silicon surface and said lower surface of metal silicide and adjacent the shallow junction …"

Challenged claim 1 of the '372 Patent requires "a metal silicide layer having a lower surface ***disposed adjacent*** the shallow junction of each of the source and drain in the silicon substrate and above the upper surface of the silicon substrate" and "an epitaxial silicon layer ***disposed*** between the upper silicon surface and said lower surface of metal silicide and ***adjacent*** the shallow junction of the source and drain … ." (Ex. 1001, 7:51-8:6; emphasis added). In the context of claim 1, the upper surface of the silicon substrate and the upper surface of the shallow junction are the same surface. (Ex. 1002, ¶40).

Because the claim requires two layers to be both "disposed adjacent" the same surface (i.e., the upper surface of the silicon substrate/shallow junction), Petitioner submits that the claim language requires interpretation to resolve the apparent ambiguity and to ascertain the actual scope of the claims. Indeed, the plain language—requiring two layers to be both adjacent the same layer—is nonsensical. Since the claim is written as an apparatus claim, two layers cannot

both be adjacent to the shallow junction layer as the claims appear to suggest.[3] Further, the term "adjacent" is unclear. Unless the term "adjacent" is meant to mean "directly adjacent" or "in physical contact with" during the formation of each layer, the term would have an unascertainable scope to a POSA. (Ex. 1002, ¶41).

Claim 1 as originally presented in the application that issued as the '372 Patent did not require any adjacency. (Ex. 1004, 42). While it did recite a shallow junction, a metal silicide layer, and an epitaxial silicon layer, the claims as originally filed explained the relationship as follows:

> [A]n epitaxial silicon layer between said upper silicon surface and said lower surface of metal silicide whereby the metal silicide extends only slightly below the upper silicon surface and does not encroach upon the shallow junction.

(Ex. 1004, 42). This is fully consistent with the description in the '372 Patent specification regarding FIG. 2(c), wherein titanium is first layered on top of a shallow junction. (Ex. 1001, 4:33-35). Thereafter, a layer of "silicon containing material 26, such as amorphous…silicon," is formed. (Ex. 1001, 4:35-38). During

[3] Petitioner reserves the right to argue in the co-pending district court case, that the claims are invalid under 35 U.S.C. § 112 as indefinite in the event the Board (or the district court) finds that the requirement for two different layers to be adjacent to the shallow junction is not amenable to construction.

the subsequent formation of silicide, the '372 Patent discloses that some of the underlying silicon substrate is consumed, albeit at a slower rate than the amorphous silicon is consumed. (Ex. 1001, 4:38-41). This is consistent with the understanding of a POSA. (Ex. 1002, ¶35). This process mirrors the originally filed claims (Ex. 1004, 42) in the sense that the metal silicide extends "slightly below" the upper silicon surface.

During prosecution, the Examiner objected to the drawings as not showing this "slightly below" limitation and rejected the claims under 35 U.S.C. § 112 for indefiniteness. (Ex. 1004, 70-71). In response, PO (then Applicant) amended the claims to specify that the metal silicide layer is disposed adjacent the silicon substrate, but did not initially amend the claims to require the epitaxial silicon layer to also be adjacent the shallow junction. (Ex. 1004, 78). Applicant then argued that FIG. 2(c) (which is described in the specification as noted above) shows the structure recited in the claims. (Ex. 1004, 79). It argued that:

> [O]ne skilled in the art is taught the ratio of silicon and metal, such as titanium to form metal silicide, such as titanium silicide … it is the silicon that is the moving element and … if the amorphous silicon is thick enough based on the ratio of silicon to metal, the silicon from the amorphous silicon will be in sufficient supply to not only consume essentially all of the metal in forming the metal silicide but will

> migrate to the single crystal silicon and form a solid epitaxy layer ***below the metal silicide***.

(Ex. 1004, 80-81; emphasis added). Applicant reiterated that "the metal silicide only can extent [sic - extend] slightly below the original single crystal silicon surface … ." (Ex. 1004, 81). Finally, the PO (then Applicant) argued that the prior art used to reject the claims was insufficient because "no amorphous silicon remains to form an epitaxial layer with the single crystal silicon substrate." (Ex. 1004, 82). In other words, the Applicant argued that the claims were patentable because the process used to manufacture the claimed apparatus was not disclosed in the prior art of record.

Later in prosecution, the Applicant further amended the claims to specify the dual-adjacency now required. (Ex. 1004, 93-94). It clarified in the remarks that the amendments were made to clarify that "the metal silicide and epitaxial layer structure were adjacent the shallow junctions of ***both a source and drain***…." (Ex. 1004, 95; emphasis added). Applicant's remarks never addressed the nonsensical nature of the claims.

The claims were thereafter allowed. (Ex. 1004, 98-99).

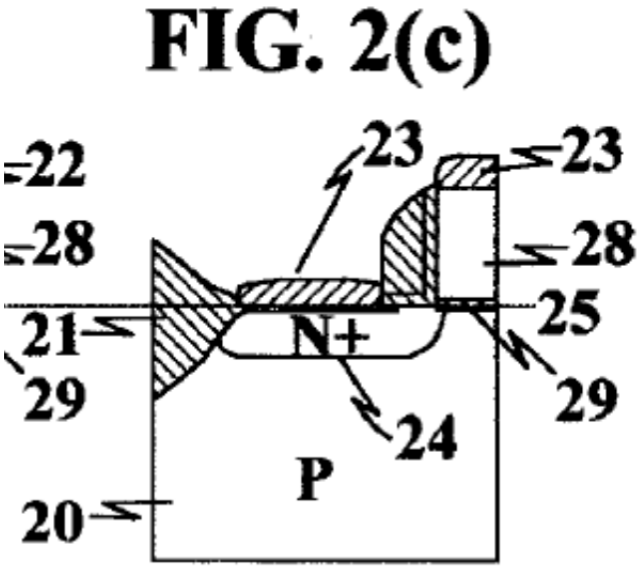
In both drafting the application and in prosecuting the claims that led to the '372 Patent, PO consistently argued that the claimed structure (and process to make the claimed structure) was the structure described and illustrated in

FIG. 2(c). Nonetheless, Petitioner submits that the claim language that was actually created by amendment (Ex. 1004, 93-94) is nonsensical by virtue of two different structures layered on top of each other both being adjacent to an underlying structure. (Ex. 1002, ¶41). Thus, for purposes of this proceeding, Petitioner submits that the only reasonable construction of this term must reflect the structure formed by the process described in connection with FIG. 2(c). (Ex. 1002, ¶44).

Petitioner proposes that the term "disposed" should be construed as "formed," such that the environmental structure existing at the time of the "formation" would be positionally relevant to the construction. This means that when the metal silicide layer is created it is disposed, or formed, adjacent to the shallow junction. Subsequent processing steps demonstrate that the metal silicide layer is not required to remain in its as-formed position indefinitely. In particular, future formation of the epitaxial layer can occur "between said upper silicon surface and said lower surface of metal silicide" and, at the time of formation, be adjacent "the shallow junction…" (Ex. 1001, Claim 1, 4:61-5:6). Therefore, the only logical interpretation of this claim is depicted in FIG. 2(c); the final structure formed after the completion of processing. (*See* Ex. 1002, ¶44).

Petitioner therefore submits that the only reasonable construction of the "disposed adjacent" terms of claim 1 is "formed adjacent" such that something is

formed at one point in the process that does not need to remain in the same relative position throughout the fabrication process. (Ex. 1002, ¶¶42-45). This construction properly reflects the claimed embodiment of FIG. 2(c).



(Ex. 1001, FIG. 2(c); Ex. 1002, ¶¶34-36, 42-45). Therefore, the claims of the '372 Patent *require* the formation of the silicide layer *before* the formation of an epitaxial layer; otherwise, the "disposed adjacent" relationship required in the claims is never met. (Ex. 1002, ¶¶42-45). Grounds 1, 2, and 6 below explain why the challenged claims of the '372 Patent are obvious under this construction.

It appears that PO may argue for a different construction unsupported by the '372 Patent specification in which the metal silicide layer can be adjacent to a layer of epitaxial silicon *previously formed* on the upper surface of the shallow junction. Though this construction is not supported by the '372 Patent specification and does

not meet the adjacency required by the claims of the '372 Patent, it is the only construction under which the silicide does not consume a portion of the shallow junction during formation (i.e., because the metal is layered on the epitaxial silicon and the silicide is thereafter formed). While Petitioner does not believe this construction is supported by the '372 Patent specification, Grounds 1, 3, 4, and 5 below address this proposed construction.

VIII. STATEMENT OF THE PRECISE RELIEF REQUESTED AND THE REASONS THEREFOR (37 C.F.R. §§ 42.22(a) AND 42.104(b))

Petitioner requests the institution of IPR and cancellation of claims 1 and 4-6 of the '372 Patent based on the Grounds listed below.

Ground	Statutory Basis	Relied-On References	Claims
1	35 U.S.C. § 103	*Saito* (Ex. 1005)	1 and 4-6
2	35 U.S.C. § 103	*Yu* (Ex. 1007)	1 and 4-5
3	35 U.S.C. § 103	*Chau* (Ex. 1006) in view of *Rodder* Ex. (1008)	1 and 4-6
4	35 U.S.C. § 103	*Rodder* (Ex. 1008)	1 and 4-6
5	35 U.S.C. § 103	*Ogasawara* (Ex. 1009)	1 and 4-6
6	35 U.S.C. § 103	*Yu* (Ex. 1007) in view of *Ogasawara* (Ex. 1009)	6

Grounds 1, 2, and 6 address claims 1 and 4-6 under Petitioner's proposed constructions. Should the Board be inclined to institute either Ground 1 or Ground 2 (and Ground 6, which addresses claim 6 based on the same primary reference as Ground 2), Petitioner submits that Ground 1 should be instituted, as it also addresses the claims under the construction Patent Owner may advocate.

Grounds 3, 4, and 5 address a construction Petitioner submits should not be adopted, but may be advocated by Patent Owner.

Per 37 C.F.R. § 42.6(c), copies of the references are filed herewith. Additionally, Petitioner provides the declaration of R. Jacob Baker, Ph.D., P.E. in support of these Grounds.[4]

A. Ground 1: Claims 1 and 4-6 Are Unpatentable Under 35 U.S.C. § 103(a) as Obvious over *Saito*

As supported by Dr. Baker's declaration, claims 1 and 4-6 of the '372 Patent are obvious in view of *Saito*.

1. Overview of the Prior Art of Ground 1

Japanese Patent Application No. JP08-204187 ("*Saito*") was published on August 9, 1996. (Ex. 1005 (foreign-language version and English-language translation, followed by declaration from translator)). *Saito* is prior art under 35 U.S.C. § 102(b). *Saito* describes a prior art technique (with regard to FIG. 6)

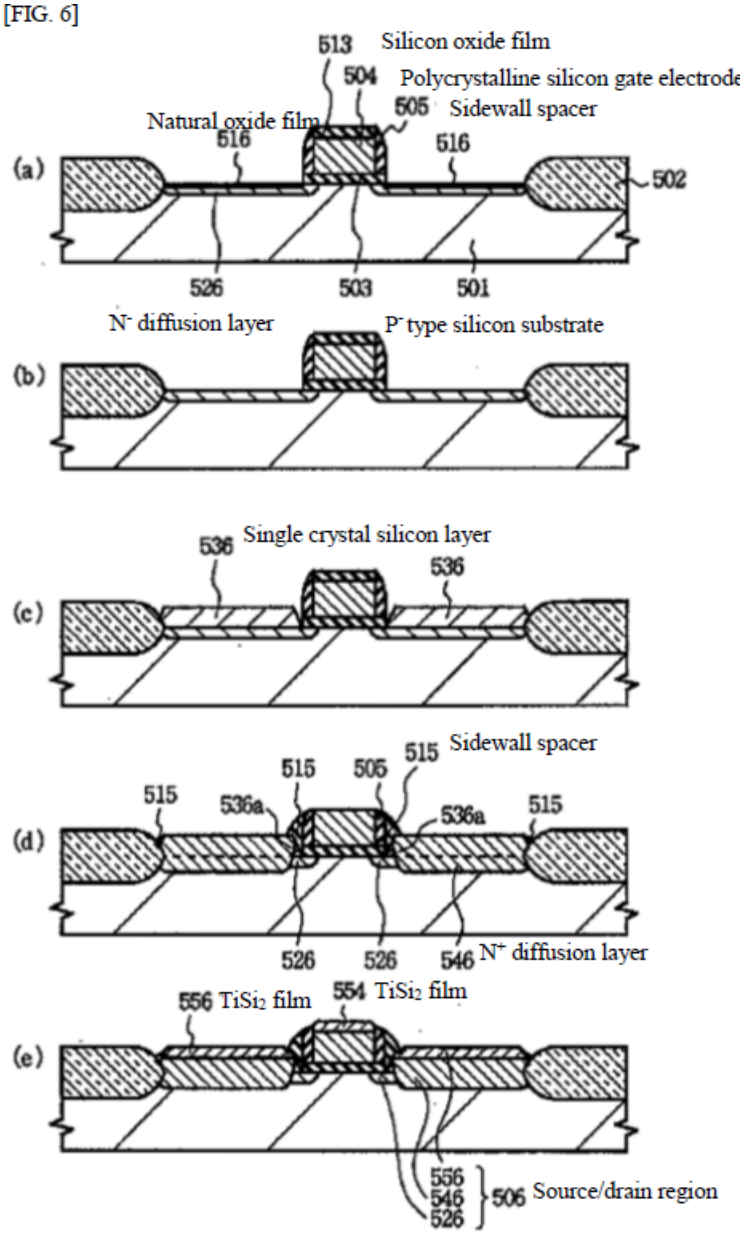
[4] Dr. Baker has a BS degree, an MS degree, and a Ph.D. in Electrical Engineering, and is a licensed Professional Engineer in the state of Idaho. He has more than 30 years of experience in circuit design and manufacture and has authored several books and other publications related to solid-state circuit design and packaging. Accordingly, Dr. Baker is an expert in the field of the '372 Patent and the prior art. (Ex. 1003).

and an allegedly inventive technique (with regard to FIG. 1) that each renders claims 1 and 4-6 obvious, depending on the construction applied.

a. *Saito*'s FIG. 6 Technique

Saito is generally directed to methods of fabricating a semiconductor device. (Ex. 1005, [0017]; Ex. 1002, ¶48). *Saito* describes a prior art process in connection with its FIG. 6, which is reproduced below:

[FIG. 6]



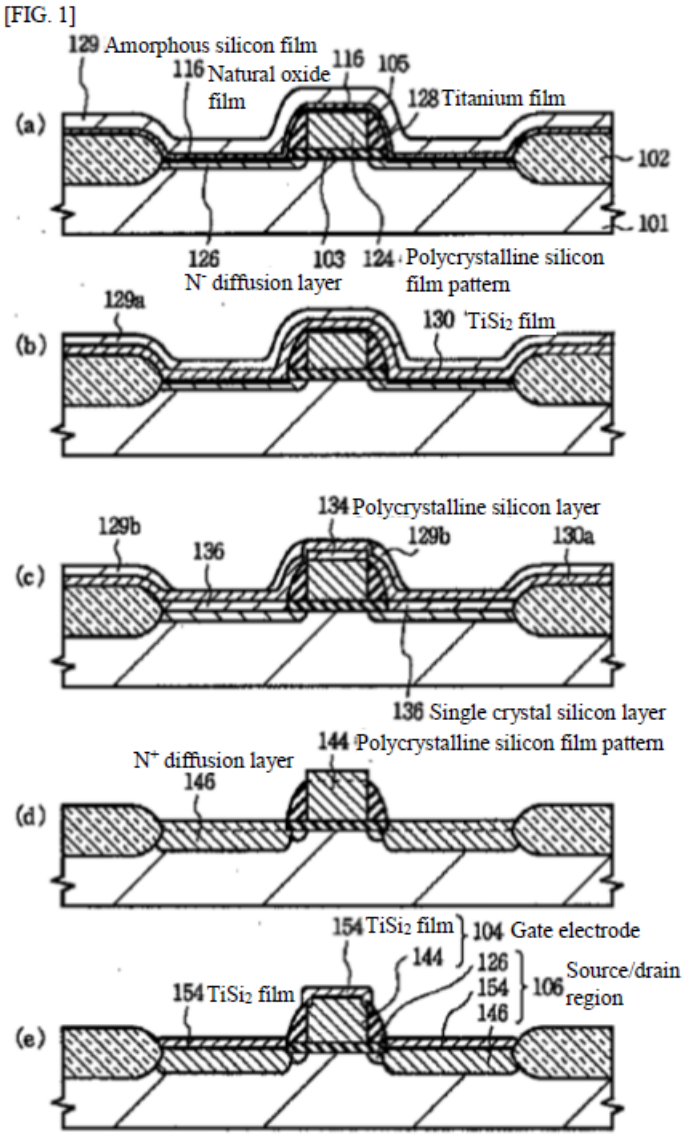
(Ex. 1005, FIG. 6, [0008]-[0013]; Ex. 1002, ¶49).

In FIG. 6, after the formation of the N- diffusion layer 526, *Saito* describes "a single crystal silicon layer 536 having a thickness of 100 to 200nm is selectively and epitaxially grown on the surface of the N- type diffusion layer 526."

(Ex. 1005, [0010]; Ex. 1002, ¶50). After the N+ diffusion layer is created, a "titanium film is formed over the entire surface, and a $TiSi_2$ film 554 and 556 are selectively formed … on the surface of the N+ type diffusion layer 546 … ." (Ex. 1005, [0011]-[0012]). This is a shallow junction. (Ex. 1005, [0013]; Ex. 1002, ¶51).

b. *Saito's* FIG. 1 Technique

One of the allegedly inventive embodiments of *Saito* discloses the deposition of titanium 128 on a silicon substrate 101 having a thin natural oxide film 116. This embodiment is described in connection with FIG. 1, which is reproduced below:



(Ex. 1005, FIG. 1, [0025]). In this embodiment, a layer of amorphous silicon 129 is deposited on top of the titanium layer 128. (Ex. 1005, FIG. 1, [0025]; Ex. 1002, ¶53). The substrate is then annealed twice: the first annealing occurring between 400-500C, and the second annealing occurring between 500-600C. (Ex. 1005, [0026]-[0028]; Ex. 1002, ¶¶53-54).

During the first annealing, the process of forming a titanium silicide film 130 begins. (Ex. 1005, [0026]; Ex. 1002, ¶¶53-54). During the second annealing, the titanium silicide's formation is completed and the thin natural oxide film 116 previously present on the silicon substrate is removed. (Ex. 1005, [0027]). *Saito* also describes that the second annealing causes the remaining amorphous silicon film 129a to pass through the titanium silicide 130 and reach the substrate's surface 126. (*Id.*). In particular, *Saito* describes that:

> When the second thermal annealing is carried out for a long time, the total energy of the system is decreased so that silicon from a portion of the amorphous silicon film 129a on the upper surface of the polycrystalline silicon film pattern 124 and on the surface of the N- diffusion layer 126 via the $TiSi_2$ film 130, respectively passes through the $TiSi_2$ film 130 and moves so as to reach the upper surface of the polycrystalline silicon film pattern 124 and the surface of the N- type diffusion layer 126. As a result, the polycrystalline silicon layer 134 having a thickness of about 70 is selectively grown in a solid phase on the surface of the polycrystalline silicon film pattern 124, the single crystal silicon layer 136 having a thickness of about 70 is selectively and epitaxially grown in a solid phase on the surface of the N- type diffusion layer 126; the $TiSi_2$ film 130 becomes the $TiSi_2$ film 130a, and the amorphous silicon film 129b is left only above the surface of the sidewall spacer 105 and above the surface of the field oxide film 102 via the $TiSi_2$ film 130a (FIG. 1 (c), FIG. 2 (c)).

(Ex. 1005, [0027]; Ex. 1002, ¶¶53-54).

The second thermal annealing is carried out at a temperature range so that the amorphous silicon film 129a is not changed into polysilicon film and the result of this anneal step is the formation of an epitaxial silicon layer 136 between the titanium silicide layer 130a and the source/drain junction. (Ex. 1005, [0027]-[0028]; Ex. 1002, ¶55). During the thermal anneal, the single crystal silicon layer at the source/drain junction also grows epitaxially, which contributes to the epitaxial silicon layer formed between the titanium silicide layer and the source/drain junction 126. (*Id.*). As explained below, this FIG. 1 embodiment of *Saito* mirrors the process and resultant structure described and claimed in the '372 Patent. (Ex. 1002, ¶72).

2. Specific Identification of Challenge

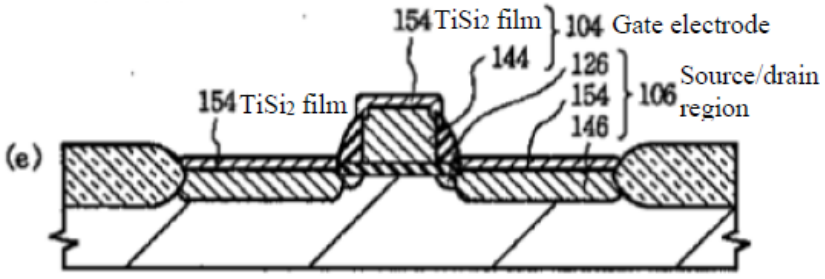
Under the construction Petitioner asserts should apply here, the challenged claims are obvious in view of *Saito* as depicted in FIGS. 1(a)-1(e). Alternatively, under a broader construction Petitioner expects PO may advocate notwithstanding its district court positions (where the epitaxial layer can be formed before silicide formation and where silicide formation can consume some of the epitaxial layer) the challenged claims are obvious in view of *Saito* as depicted in FIGS. 6(a)-6(e).

a. Claim 1

i. *Saito* FIGS. 1(a)-1(e)

The preamble of claim 1 states: "[i]n an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made."

This is disclosed in *Saito*. (Ex. 1002, ¶72). The abstract of *Saito* states a purpose for the invention as "[a] method for fabricating a MOS transistor having a salicide structure having a source/drain diffusion layer in which there is a shallow junction depth and a source/drain region with reduced resistance value." (Ex. 1005, Abstract, [0024]). A POSA would understand that a MOS transistor such as the one disclosed in *Saito* contains an active region including a field effect transistor. (Ex. 1002, ¶72). Further, FIG. 1(e) discloses a gate and a conductive contact.

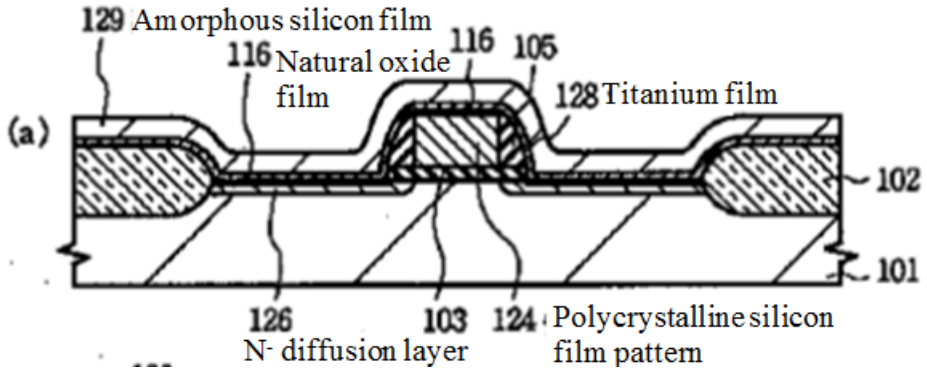


(Ex. 1005, FIG. 1(e)). *Saito* confirms this disclosure by describing the formation of a gate electrode. (Ex. 1005, [0024]).

Claim 1 of the '372 Patent requires "a single crystalline silicon substrate with a [sic] upper surface region." The silicon substrate 101 of *Saito*, depicted in FIG. 1(a), meets this limitation. Petitioner asserts that a POSA would understand that the teachings of *Saito* demonstrate the substrate 101 is a single crystalline semiconductor substrate based on a failure to indicate that it is *not* single crystalline. (Ex. 1002, ¶72). Nonetheless, to the extent a POSA would not have taken *Saito's* silence as a teaching of single crystalline silicon, a POSA would have found it obvious to use single crystalline silicon as the substrate 101 of *Saito*. (Ex. 1002, ¶72). In particular, *Saito* discloses "selectively and epitaxially growing a thin film of a single crystal silicon layer on the surface of a silicon substrate …. ." (Ex. 1005, [0007]). A POSA would understand that in order to grow a single crystalline silicon thin film epitaxially, the substrate that acts as the seed layer must also be formed of single crystalline silicon. (Ex. 1002, ¶72). The textbook *Silicon Processing for the VLSI Era* by Wolf et al. ("*Wolf*") is a seminal, mid-1980's work in the semiconductor fabrication field that confirms that the "epitaxial growth process is a means of depositing a thin layer … of single crystal material upon the surface of a single crystal substrate." (Ex. 1013, 76 (textbook page 124); Ex. 1002, ¶72). Thus, since the epitaxial growth of *Saito* is single crystalline, so too is the underlying substrate. (*Id*.). Accordingly, *Saito* renders this limitation obvious.

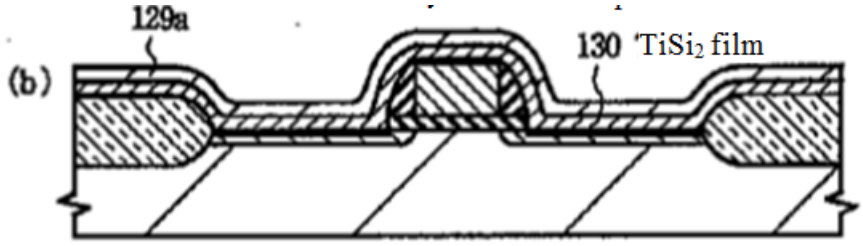
Claim 1 further requires "a shallow junction for each of the source and drain of the transistor underlying said upper surface of the silicon substrate." The shallow source and drain is depicted in *Saito* as an N- doped diffusion layer 126 in FIG. 1(a) or, alternatively, as an N+ doped diffusion layer 146 in FIG. 1(e). (*See also* Ex. 1005, [0016]). As the titanium film 128 is formed directly on the substrate 101 (and, in the process, the natural oxide film 116 is eliminated), the subsequently formed shallow junction never rises above the upper surface of the silicon substrate.

[FIG. 1]



(Ex. 1005, FIG. 1(a), [0025]). Thus, *Saito's* disclosure of either region 126 or region 146 meets this limitation. (Ex. 1002, ¶72).

Claim 1 of the '372 Patent further requires "a metal silicide layer having a lower surface disposed adjacent the shallow junction of each of the source and drain in the silicon substrate and above said upper surface of the silicon substrate." This feature can be found in FIG. 1(b) of the *Saito* reference as titanium silicide layer 130.



(Ex. 1005, FIG. 1(b), [0026]-[0027]; Ex. 1002, ¶72). The formation of this $TiSi_2$ film 130 is not complete until the second annealing. This second annealing causes the natural oxide film to react with the $TiSi_2$, causing the natural oxide to be removed, such that the formation of the titanium silicide film is adjacent to the substrate's surface. (Ex. 1005, [0027]; Ex. 1002, ¶72). To the extent PO argues that the natural oxide would *not* be removed, a POSA would have known that a natural oxide layer is not material to the fabrication process and could readily have been removed before the deposition of titanium. (Ex. 1002, ¶72). The titanium silicide layer described as layer 130 is contained within the $TiSi_2$ layers 154 and 156 at the point in fabrication illustrated in FIG. 1(e). (Ex. 1005, [0029]-[0030]). Thus, *Saito* meets this limitation.

Claim 1 of the '372 Patent further requires "an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent the shallow junction of each of the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of each of the source and the drain." The '372 Patent

describes this epitaxial silicon layer as a "solid phase epitaxy layer." (Ex. 1001, 4:62-5:3). *Saito* discloses the formation of an epitaxial layer as claimed from the remaining amorphous silicon disposed as part of the silicide formation process described above. (Ex. 1005, [0027]). In particular, *Saito* describes:

> When the second thermal annealing is carried out for a long time, the total energy of the system is decreased so that silicon from a portion of the amorphous silicon film 129a on the upper surface of the polycrystalline silicon film pattern 124 and on the surface of the N^- diffusion layer 126 via the $TiSi_2$ film 130, respectively passes through the $TiSi_2$ film 130 and moves so as to reach the upper surface of the polycrystalline silicon film pattern 124 and the surface of the N^- type diffusion layer 126. As a result, the polycrystalline silicon layer 134 having a thickness of about 70 is selectively grown in a solid phase on the surface of the polycrystalline silicon film pattern 124, ***the single crystal silicon layer 136 having a thickness of about 70 is selectively and epitaxially grown in a solid phase on the surface of the N^- type diffusion layer 126;*** the $TiSi_2$ film 130 becomes the $TiSi_2$ film 130a, and the amorphous silicon film 129b is left only above the surface of the sidewall spacer 105 and above the surface of the field oxide film 102 via the $TiSi_2$ film 130a.

(Ex. 1005, [0027], FIG. 1(c); emphasis added). Though this epitaxial layer on the surface of the N- diffusion layer is not illustrated in FIGS. 1(d) and 1(e), it is described as being positioned between layer 130 and the structure that forms the shallow junction (i.e., the N- diffusion layer 126 illustrated in FIG. 1(b)), satisfying

the claimed "epitaxial layer" having the required geometry. (*See* Ex. 1002, ¶30).

Moreover, *Saito's* discussion of FIG. 1(d) demonstrates that the epitaxial layer is still present even if not illustrated. (Ex. 1005, [0029]; Ex. 1002, ¶72). Specifically, when a second deposition of amorphous silicon is discussed, the thickness of said amorphous silicon "is determined by the required thickness of the single crystal silicon layer 136," which is the epitaxial layer formed as described above in paragraph 27 of *Saito*. (*Id.*). This demonstrates the epitaxial layer is still present, although not depicted, in FIGS. 1(d) and 1(e). (*Id.*).

For these reasons, the disclosed steps in *Saito* are identical to those described and claimed in the '372 Patent and the resulting structure is likewise identical. (Ex. 1002, ¶¶70-72). Claim 1 is obvious over this embodiment of *Saito* and its associated description under Petitioner's proposed construction of the claims.[5]

ii. *Saito* FIGS. 6(a)-6(e)

Under an alternative interpretation, in which the epitaxial layer can be formed before the silicide layer (with the silicide formation consuming part of the epitaxial layer), other figures (and associated description) of *Saito* render claim 1

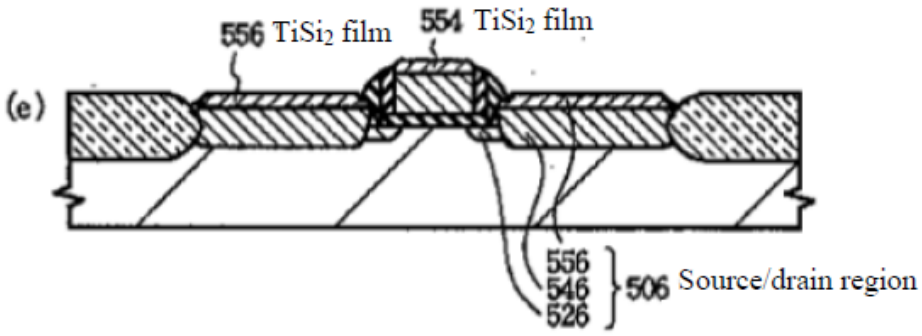
[5] A POSA would have known that a functioning transistor was created as of FIG. 1(c) and processing could stop after this step. (Ex. 1002, ¶81).

obvious. Specifically, the prior art *Saito* describes in connection with FIG. 6 renders claim 1 of the '372 Patent obvious under this alternative construction.

Saito's FIG. 6 discloses the preamble of claim 1. For example, the abstract of *Saito* states a purpose for the invention as "[a] method for fabricating a MOS transistor having a salicide structure having a source/drain diffusion layer in which there is a shallow junction depth and a source/drain region with reduced resistance value." (Ex. 1005, Abstract, [0024]). With regard to FIG. 6, *Saito* teaches "a cross sectional view of the fabricating steps for a semiconductor device." (Ex. 1005, [0008]). Further, while introducing then conventional art, *Saito* describes the decreasing sizes of MOS transistor source and drain regions, and the FIG. 6 embodiment to achieve that goal. (Ex. 1005, [0002]). Further, it explains that the result of FIG. 6 is the formation of "an N-channel MOS transistor." (Ex. 1005, [0012]). A POSA looking at FIG. 6 would have understood that this device, which *Saito* states is relevant to the alleged invention disclosed therein, is an active region that contains or could contain a field effect transistor. (Ex. 1002, ¶73).

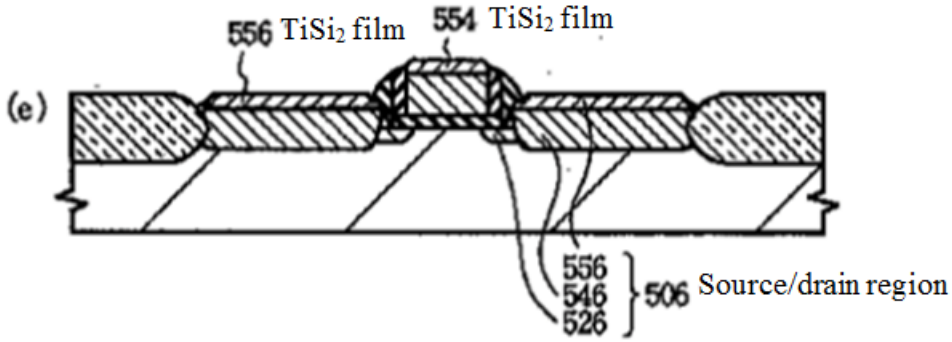
FIG. 6 illustrates a source, drain, gate, and conductive contact, as are further required. (Ex. 1005, FIG. 6). In particular, *Saito* describes that the N-channel MOS transistor formed by the FIG. 6 process includes "gate electrode 504" and "source/drain region 506." (Ex. 1005, [0012]). Claim 1 of the '372 Patent requires an integrated circuit that includes a single crystalline silicon substrate and a

shallow junction for both the source and drain. The silicon substrate 501 is depicted in FIG. 6(a). (*See also* Ex. 1005, [0009]; Ex. 1002, ¶73). A person of skill in the art would understand that this substrate is single crystalline based on the disclosure that the grown layer 536 is single crystalline. (*Id.*; *see also* Ex. 1005, [0010]). The shallow source and drain are depicted as an N+ doped diffusion layer 546 in FIG. 6(e).

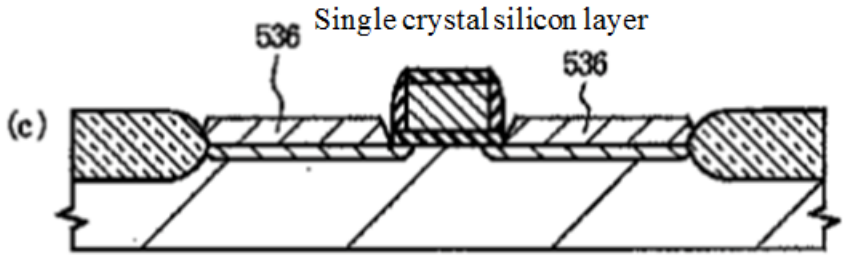


(Ex. 1005, FIG. 6(e), [0013]; Ex. 1002, ¶73).

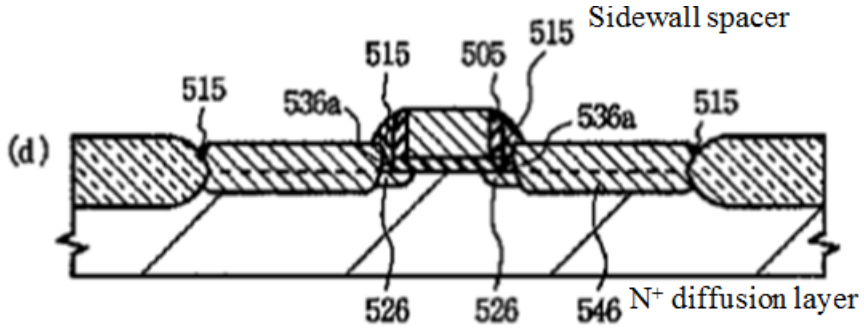
Claim 1 of the '372 Patent further requires a metal silicide layer having a lower surface disposed adjacent to the junctions. This feature can be found in FIG. 6(e) of the Saito reference as titanium silicide layer 556 formed by consuming part of the epitaxially grown silicon. (*See also* Ex. 1005, [0011]; Ex. 1002, ¶73).



Claim 1 of the '372 Patent further requires an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent to the shallow junction of each the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of each the source and drain. The '372 Patent describes this epitaxial silicon layer as a "solid phase epitaxy layer." (Ex. 1001, 4:62-5:3). *Saito* discloses the formation of this epitaxial layer as a "single crystal silicon layer 536 having a thickness of 100 to 200nm…selectively and epitaxially grown on the surface of the N- type diffusion layer 526." (Ex. 1005, [0010], FIG. 6(c)).



As the prior art process continues, the epitaxially grown crystal silicon layer can be found in FIG. 6(d) in its modified form 536a.



Although the epitaxially grown crystal silicon layer 536a is not depicted in

FIG. 6(e) under the $TiSi_2$ film 556, the N- type diffusion layer 526 is present and included as part of the source/drain. In FIG. 6(d), epitaxially grown crystal silicon layer 536a is located above the N- type diffusion layer 526. Therefore, the epitaxially grown crystal silicon layer 536a can also be considered adjacent to the shallow junction of each the source and drain in FIG. 6(d). (Ex. 1002, ¶73).

For these reasons, the disclosed steps in *Saito's* discussion of FIG. 6 render claim 1 obvious under the alternative construction PO may offer as described herein. (Ex. 1002, ¶¶52, 73).

b. Claim 4

i. *Saito* FIGS. 1(a)-1(e)

Claim 4 is obvious in view of *Saito's* FIG. 1 embodiment. Claim 4 requires that "the shallow junction is P+/N." *Saito* discloses that "[f]urthermore, although the first example is applied to the N-channel MOS transistor, the present example is not limited to that, and can be applied to the fabrication method of a P-channel MOS transistor or a CMOS transistor." (Ex. 1005, [0034]-[0035]; Ex. 1002, ¶74).

ii. *Saito* FIGS. 6(a)-6(e)

Claim 4 is obvious in view of FIG. 6 of *Saito*. Claim 4 requires that the shallow junctions must be a P+/N junction. *Saito* discloses that "[f]urthermore, although the first example is applied to the N-channel MOS transistor, the present

example is not limited to that, and can be applied to the fabrication method of a P-channel MOS transistor or a CMOS transistor." (Ex. 1005, [0034]-[0035]). A POSA would have understood this passage to be a generally applicable passage that could apply either to the alleged invention of *Saito* or to the prior art embodiments described therein (including in connection with FIG. 6). (Ex. 1002, ¶75). Thus, claim 4 is obvious over *Saito*.

c. Claim 5

i. *Saito* FIGS. 1(a)-1(e)

Claim 5 is obvious in view of *Saito's* FIG. 1 embodiment. Claim 5 requires that the "gate includes and [sic - an] upper surface and a silicide layer is disposed on said upper layer." FIG. 1(b) of *Saito* shows that the silicide layer 130 is formed over the gate portion as required by this claim. *Saito* confirms this disclosure when it states that "a first thermal annealing is carried out in a nitrogen atmosphere at 400 to 500ºC … ." (Ex. 1005, [0026]). In the temperature range of the first thermal annealing, the reaction between silicon and the titanium film, 128, constituting the N^- diffusion layer 126 and the polycrystalline silicon film pattern 124 "does not contribute to the silicidation reaction progress, and once finished, a uniform $TiSi_2$ film 130 can be obtained." (Ex. 1005, [0026]). The polysilicon film pattern 124 is "in the region in which a gate electrode is to be formed." (Ex. 1005, [0025]). Thus, claim 5 is obvious over *Saito*. (Ex. 1002, ¶76).

ii. *Saito* FIGS. 6(a)-6(e)

Alternatively, FIG. 6(e) of *Saito* shows that the silicide layer 554 is formed over the gate portion as required by this claim. *Saito* confirms this disclosure when it states that "[t]hen, a titanium film is formed over the entire surface, and a $TiSi_2$ film 554 and 556 are selectively formed on the upper surface of the polycrystalline silicon gate electrode 504 and on the surface of the N^+ type diffusion layer 546 using RTA in a nitrogen atmosphere." (Ex. 1005, [0012]). Thus, claim 5 is obvious over *Saito*. (Ex. 1002, ¶77).

d. Claim 6

i. *Saito* FIGS. 1(a)-1(e)

Claim 6 is obvious in view of *Saito's* FIG. 1 embodiment. Claim 6 requires "the depth of the shallow junction is less than about 2500Å." When converted, this requires the junction to have a depth of less than about 250nm. (Ex. 1002, ¶78). In *Saito*, N- junction has a depth of 40nm. (Ex. 1005, [0025]). The later formed N+ junction has a depth of 130nm. (Ex. 1005, [0029]). Thus, claim 6 is obvious over *Saito*. (Ex. 1002, ¶78).

ii. *Saito* FIGS. 6(a)-6(e)

Claim 6 is obvious in view of the discussion of FIG. 6 of *Saito*. Claim 6 requires that the depth of the shallow junction is less than about 2500Å. When converted, this requires the junction to have a depth of less than about 250nm.

(Ex. 1002, ¶79). With regard to FIG. 6, *Saito* states "[a]lthough the N^+ type diffusion layer 546 has an equivalently deep junction depth, the effective junction depth becomes shallow if viewed from the surface of the initial P type silicon substrate 501. From this and the presence of the $TiSi_2$ film 556, the junction depth of the source/drain diffusion layer is shallow, and the resistance value of the source/drain region itself can be reduced." (Ex. 1005, [0013]).

Given the dimensions of the relatively larger epitaxial layer (described as 100 to 200nm) to the relatively smaller shallow junction depth, as well as the fact that *Saito* discloses the junction as a "shallow junction," a POSA would have understood that, at least at the thinner range disclosed in *Saito*, the shallow junction has a depth that meets the requirements of this claim limitation. (Ex. 1002, ¶79). Thus, claim 6 is obvious over *Saito*. (*Id.*).

B. Ground 2: Claims 1 and 4-5 Are Unpatentable Under 35 U.S.C. § 103(a) as Obvious over *Yu*

As supported by Dr. Baker's declaration, claims 1 and 4-5 of the '372 Patent are obvious in view of *Yu* under the Petitioner's proposed construction.

1. Overview of the Prior Art of Ground 2

a. *Yu*

United States Patent No. 5,409,853 ("*Yu*") was filed on May 20, 1994, and issued on April 25, 1995. (Ex. 1007). *Yu* is prior art under 35 U.S.C. § 102(b).

Yu is directed to a process of fabricating a semiconductor device. (Ex. 1007, 3:10-12; Ex. 1002, ¶56). *Yu* discloses the formation of a silicide gate on a substrate. (Ex. 1007, 3:10-28; Ex. 1002, ¶57). Palladium is then deposited on the substrate. (Ex. 1007, 3:40-57; Ex. 1002, ¶57). Next, the palladium is caused to react with the silicon surface via a low temperature anneal, forming metal-rich junction silicide, specifically, palladium silicide on the surface. (Ex. 1007, 3:58-4:9; Ex. 1002, ¶57). The palladium silicide extends below the substrate surface. (*Id.*).

Next, a film or layer of amorphous silicon or fine grain silicon is deposited on the device. (Ex. 1007, 4:18-29; Ex. 1002, ¶58). As appropriate, the deposited silicon layer is then implanted with the proper dopant species; the proper dopant species depends on the polarity of the device. (Ex. 1007, 4:28-31; Ex. 1002, ¶58). The device is then annealed at a temperature of about 600C. (Ex. 1007, 4:37-46; Ex. 1002, ¶58). At this temperature, the palladium silicide acts as a transport media for the solid phase epitaxy. (*Id.*). The amorphous silicon layer is transported through the palladium silicide and epitaxially recrystallizes on the active silicon junction surface to form a doped epitaxial silicon region. (Ex. 1007, 4:37-46, FIG. 1F; Ex. 1002, ¶58). According to *Yu*, the palladium silicide that was formerly located below the substrate surface has been lifted and is now located on top of the doped epitaxial silicon region. (Ex. 1007, 4:53-58; Ex. 1002, ¶58).

2. Specific Identification of Challenge

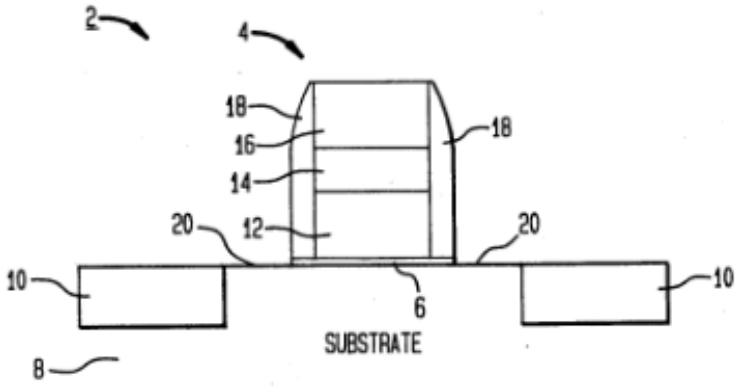
a. Claim 1

The preamble of claim 1 states "[i]n an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made." *Yu* teaches "[r]eferring initially to FIG. 1A, a semiconductor device or, more specifically, a metal-oxide-semiconductor field-effect-transistor (MOSFET), 2 is shown. The semiconductor device 2 includes a silicided gate 4 comprising a gate oxide or insulating film 6…." (Ex. 1007, 3:10-14). Further, claim 1 of *Yu* provides that the disclosure is directed to a "semiconductor device having raised source and drain regions." (Ex. 1007, 6:10-40; Ex. 1002, ¶83).

Claim 1 of the '372 Patent requires an integrated circuit that includes a single crystalline silicon substrate and a shallow junction for both the source and drain of the transistor underlying the upper surface of the silicon substrate.

The single crystalline silicon substrate is disclosed in *Yu* as semiconductor substrate 8 in FIG. 1A.

FIG. 1A

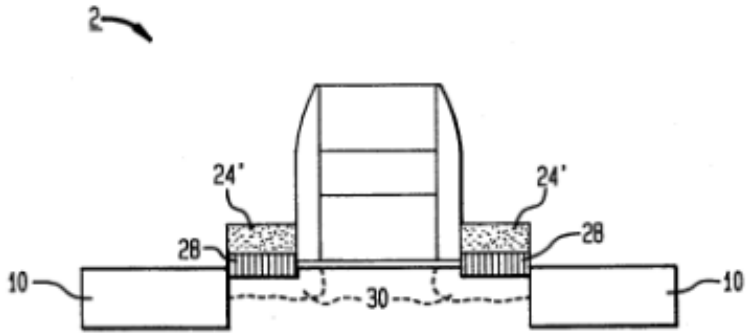


(Ex. 1007, FIG. 1A; Ex. 1002, ¶83). The fact that *Yu* refers to layer 12 as "polysilicon" indicates that the substrate, which is not specified to be polysilicon, is single crystalline silicon. (Ex. 1007, 3:15). Even if not expressly disclosed in *Yu*, it would have been obvious to a POSA that *Yu* taught or suggested the use of a single crystalline silicon substrate—the most common crystalline form of silicon substrate at the time of the filing of the '372 Patent. (Ex. 1002, ¶83). Specifically, *Yu* discloses "[a]t such a temperature, the palladium silicide 24 acts as a transport media for the solid phase epitaxy of the sputter deposited silicon 26. The amorphous, unseeded silicon layer 26 is transported through the palladium silicide 24 and epitaxially recrystallizes on the active silicon junction surfaces 20 to form doped epitaxial silicon regions 28, as shown in FIG. 1F." (Ex. 1007, 4:38-45). A POSA would understand that in order to grow a single crystalline silicon thin film epitaxially, the substrate that acts as the seed layer must also be formed of single

crystalline silicon. (Ex. 1002, ¶83). The "epitaxial growth process is a means of depositing a thin layer … of single crystal material upon the surface of a single crystal substrate." (Ex. 1013, 76 (textbook page 124); *see also* Ex. 1002, ¶83).

The shallow junctions for both the source and drain are depicted in *Yu* as shallow outdiffused junctions 30 in FIG. 1F. (Ex. 1007, 5:48-54; Ex.1002, ¶83).

FIG. 1F



Claim 1 of the '372 Patent further requires a metal silicide layer having a lower surface disposed adjacent to the junctions. This feature can be found in FIG. 1F of *Yu* as the palladium silicide contacts 24'. (Ex. 1007, FIG. 1F, 3:39-4:10; Ex. 1002, ¶83). The palladium is deposited directly onto the substrate. (Ex. 1007, FIG. 1B, 3:39-4:10).

Claim 1 of the '372 Patent further requires an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent to the shallow junction of each the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the

shallow junction of each of the source and drain. The '372 Patent describes this epitaxial silicon layer as a "solid phase epitaxy layer." (Ex. 1001, 4:62-5:3).

Yu discloses the formation of an epitaxial layer from amorphous silicon as described above. (Ex. 1007, 4:37- 46; Ex. 1002, ¶83). In particular, the palladium silicide acts as a transport media for the solid phase epitaxy. The amorphous silicon layer is transported through the palladium silicide and epitaxially recrystallizes on the active silicon junction surface to form a doped epitaxial silicon region 28. (*Id.*; *see* FIG. 1F). This doped epitaxial silicon region is located below the palladium silicide 24' and at the surface of the shallow outdiffused junctions 30. (*Id.*; Ex. 1002, ¶83). Therefore, the doped epitaxial silicon region is located between the upper silicon surface and the lower surface of the metal silicide. (*Id.*). Further, the palladium silicide 24' is raised; therefore, there is no longer metal silicide that extends below the surface of the substrate 8. (Ex. 1007, 4:53-58; Ex. 1002, ¶¶82-83).

For these reasons, *Yu* meets the Petitioner's proposed construction, where the epitaxial layer is formed between the silicide and the substrate after formation of the silicide; therefore, claim 1 is obvious over *Yu*.

b. Claim 4

Claim 4 is obvious in view of *Yu.* Claim 4 requires that the shallow junctions must be a P+/N junctions. *Yu* discloses that the amorphous silicon layer

26 "is then implanted with the proper dopant species. The proper dopant species depends on the polarity of the device 2." (Ex. 1007, 4:28-31). This means that the dopant species can be either P+ or N+ depending on the polarity already applied to the silicon substrate. (Ex. 1002, ¶84). Thus, claim 4 is obvious over *Yu*.

c. Claim 5

Claim 5 is obvious in view of *Yu*. Claim 5 requires that the "gate includes and [sic - an] upper surface and a silicide layer is disposed on said upper layer." FIG. 1A of *Yu* shows that the silicide layer 14 is disposed on the gate portion as required by this claim. *Yu* confirms this disclosure when it states that "[t]he semiconductor device 2 includes a silicided gate 4 comprising a gate oxide or insulating film 6 deposited on a semiconductor substrate 8, a polysilicon layer 12, a silicide layer 14 and a dielectric or insulating layer 16…The silicide layer 14 can be comprised, for example, of a refractory metal, such as W, Ti, Ta, or a metal silicide, such as $TiSi_2$." (Ex. 1007, 3:10-28; Ex. 1002, ¶85). Therefore, claim 5 is obvious over *Yu*.

C. Ground 3: Claims 1 and 4-6 Are Unpatentable Under 35 U.S.C. § 103(a) as Obvious over *Chau* and *Rodder*

As supported by Dr. Baker's declaration, claims 1 and 4-6 of the '372 Patent are obvious in view of *Chau* and *Rodder* under a construction where the epitaxial silicon can be grown before the silicide is formed.

1. Overview of the Prior Art of Ground 3

a. *Chau*

Published PCT application WO 96/20499 ("*Chau*") was filed on December 21, 1995, and published on July 4, 1996. Accordingly, *Chau* is prior art under 35 U.S.C. § 102(b).

Chau is directed to a method of fabricating a transistor. (Ex. 1006, 7; Ex. 1002, ¶¶59-60). One embodiment of *Chau* discloses the silicon substrate being etched to form a pair of recesses with depths of between approximately 20Å - 1000Å, with a depth of 200Å below the substrate surface being preferred. (Ex. 1006, 12; Ex. 1002, ¶60). Next, a semiconductor material is selectively deposited into the formed recesses and is formed to a thickness of between 200Å - 2000Å, with approximately 600Å being preferred. (Ex. 1006, 13; Ex. 1002, ¶60). This way, the semiconductor material is formed both above and below the surface of the semiconductor substrate. (*Id.*). Additionally, the semiconductor material deposited in the recesses is preferably in-situ doped with impurities. (*Id.*).

Next, a rapid thermal process (RTP) is carried out between 800C to 1000C. (Ex. 1006, 15; Ex. 1002, ¶61). This causes the impurities in the deposited semiconductor material to be diffused out from the semiconductor material into the semiconductor substrate, forming a diffused semiconductor region. (*Id.*). The diffusion extends below the sidewall spacers creating an ultra shallow tip, a region

directly beneath the sidewall spacers, with a depth of 500Å. (*Id.*). The substrate is then subjected to ion implantation and anneal, which implants more impurities, forming a source/drain contact region having a total thickness of 0.15-0.25μm. (Ex. 1006, 17; Ex. 1002, ¶62).

Next, a titanium layer is blanket deposited over the entire device. (Ex. 1006, 17-18; Ex. 1002, ¶63). The device is then heated, causing a reaction between the deposited titanium layer and the epitaxially grown semiconductor material to form a titanium silicide, consuming some of the silicon that had previously been formed in the etched recesses. (*Id.*).

b. *Rodder*

United States Patent No. 4,998,150 ("*Rodder*") was filed on December 22, 1988, and patented on March 5, 1991. (Ex. 1008). *Rodder* is prior art under 35 U.S.C. § 102(b).

Rodder is directed to a method of fabricating a new and improved source/drain transistor. (Ex. 1008, 1:54-58; Ex. 1002, ¶¶64-65). In one embodiment, *Rodder* discloses the formation of ultra shallow junctions by implanting either N-type or P-type material in the surface of the semiconductor substrate. (Ex. 1008, 4:6-12; Ex. 1002, ¶64). Next, raised source/drain regions are formed. The raised source/drain regions are formed by depositing epitaxial silicon onto the substrate surface. (Ex. 1008, 4:32-42; Ex. 1002, ¶64).

After this, sidewall spacers are formed and a second implantation stage occurs. (Ex. 1008, 4:58-5:33; Ex. 1002, ¶65). The second implantation will form shallow junctions. (*Id.*). Next, silicide regions are added above the raised source/drain regions. (*Id.*). The silicide regions may be created by placing a layer of titanium over the entire structure and then reacting the deposited titanium with some of the epitaxially grown silicon, thereby forming titanium silicide. (*Id.*).

2. Motivation to Combine

A POSA would understand that the epitaxial process of *Rodder* would have been used to form the semiconductor layer 314 in *Chau*. (Ex. 1002, ¶¶87-92). *Chau's* silence on the actual methodology suggests to a POSA that known methods would be used. (Ex. 1002, ¶¶91-92). Those known methods include epitaxial growth. (*Id.*). Indeed, a POSA would understand that epitaxial growth is one of the most common, if not the most common, way to form semiconductor layers such as layer 314 of *Chau*. (*Id.*). Both *Chau* and *Rodder* disclose raised source/drain transistors; therefore, it would have been obvious for a POSA to try the combination of *Rodder* with *Chau*. (Ex. 1006, 9; Ex. 1008, 1:5-8; Ex. 1002, ¶¶91-92).

Further, *Chau* discloses the use of single crystal substrate. (Ex. 1006, 11). An epitaxial layer is a silicon layer formed on another silicon layer, resulting in the two materials having the same crystalline structure. (Ex. 1002, ¶29). As a single

crystal silicon is disclosed in *Chau* as well as *Rodder*, the use of the epitaxial layer from *Rodder* combined with *Chau* is appropriate and likely to have succeeded. (Ex. 1002, ¶¶91-92). The combination is therefore proper and the use of an epitaxial process (as taught by *Rodder*) in *Chau* would have been obvious. *KSR*, 550 U.S. at 420-421.

3. Specific Identification of Challenge

a. Claim 1

The preamble of claim 1 states "[i]n an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made." *Chau* discloses each of these features in its summary. (Ex. 1006, 4; Ex. 1002, ¶92).

Claim 1 of the '372 Patent requires an integrated circuit that includes a single crystalline silicon substrate and a shallow junction for both the source and drain underlying the upper surface of the silicon substrate. In *Chau*, a silicon substrate 300 is disclosed in Figure 3f. To a POSA, *Chau* also depicts that the substrate 300 is a single crystalline substrate. (Ex. 1006, 11; Ex. 1002, ¶92). Further, *Rodder* teaches a silicon substrate "wherein said substrate comprises crystalline silicon." (Ex. 1008, 7:24-25). The combination of *Chau* and *Rodder* therefore renders obvious the requisite single crystalline silicon substrate.

Chau also discloses a shallow junction in the form of item 316 and portion of 322 (semiconductor material) under 316 in Figure 3f. (Ex. 1006, 7-8; Ex. 1002, ¶92).

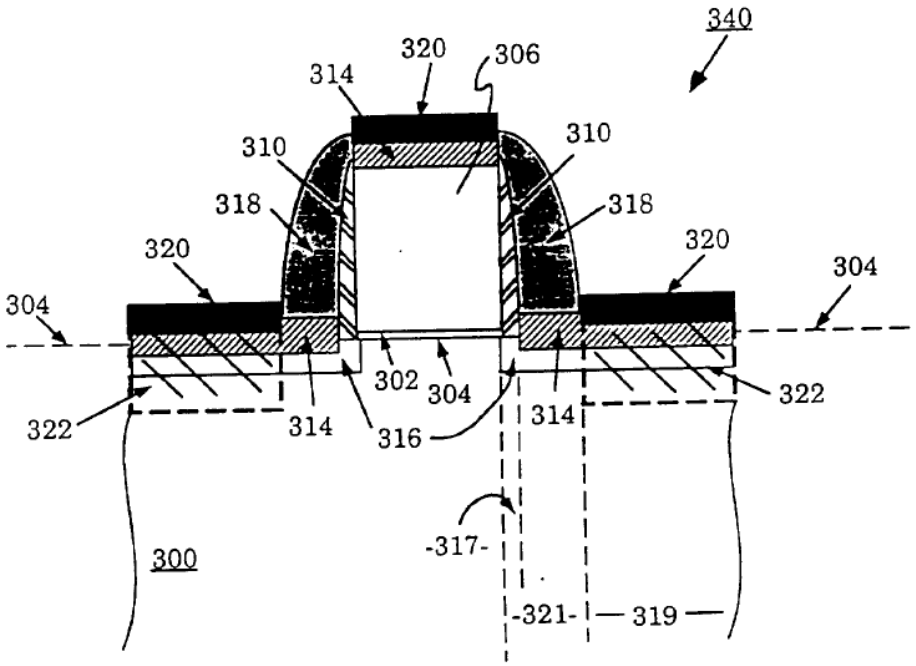


Figure 3f

Claim 1 of the '372 Patent further requires a metal silicide layer having a lower surface disposed adjacent to the junctions described above. *Chau* discloses a titanium silicide layer 320 as required under the appropriate claim construction, as can be seen in Figure 3f above. (Ex. 1002, ¶92).

Claim 1 of the '372 Patent further requires an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent to the shallow junction of each the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the

shallow junction of each the source and drain. The '372 Patent describes this epitaxial silicon layer as a "solid phase epitaxy layer." (Ex. 1001, 4:62-5:3).

Chau discloses a semiconductor material 314 in Figure 3f that is deposited onto the semiconductor substrate 300. (Ex. 1006, Figure 3f, 17). However, *Chau* does not expressly disclose that this semiconductor material 314 is formed by an epitaxial process. (Ex. 1002, ¶92).

Rodder discloses an epitaxial layer deposited onto a semiconductor substrate. (Ex. 1008, 4:30-40; Ex. 1002, ¶92). *Rodder* discloses an epitaxial silicon layer in FIG. 2D as the raised source/drain 60. (Ex. 1008, 5:19-24; Ex. 1002, ¶92). This raised source/drain 60 is disposed below the lower surface of the silicide region 72. Further, the raised source/drain 60 is disposed above the shallow junction 68. (*Id.*). Therefore, the epitaxial layer is disposed between the upper silicon surface and the lower surface of the metal silicide. (*Id.*). The epitaxial layer is disposed adjacent to the source/drain as it is located above the shallow junctions 68. (*Id.*). Further, the metal silicide 72 does not encroach upon the shallow junctions as the silicide region 72 is located above the raised source/drain 60. (*Id.*).

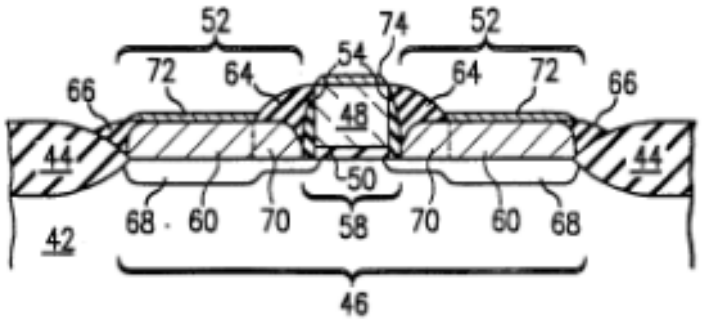


FIG. 2D

A POSA would understand that it would have been obvious to use the epitaxial process of *Rodder* to form the semiconductor layer 314 in *Chau*. (Ex. 1002, ¶92). Accordingly, the required "epitaxial silicon layer" is obvious in view of the prior art.

Chau and *Rodder* render claim 1 obvious under an interpretation where the epitaxial silicon layer can be formed prior to silicide layers being formed. (Ex. 1002, ¶92).

b. Claim 4

Claim 4 is obvious over *Chau* in view of *Rodder*. Claim 4 requires that the shallow junctions must be a P+/N junction. *Chau* discloses that "[t]he preferred method of fabrication will be described with respect to the fabrication of a PMOS transistor. It is to be appreciated that the preferred method is equally applicable to the fabrication of NMOS devices wherein the conductivity types are simply reversed. As shown in Figure 3a, a PMOS transistor of the present invention is preferably fabricated on an n-type substrate or well 300 … ." (Ex. 1006, 9-10; Ex.

1002, ¶93). Thus, claim 4 is obvious over *Chau* in view of *Rodder*.

c. Claim 5

Claim 5 is obvious over *Chau* in view of *Rodder*. Claim 5 requires that the

> [G]ate includes and [sic - an] upper surface and a silicide layer is disposed on said upper layer." Figure 3f of *Chau* discloses a silicide layer 320 formed on top of the gate. Further, *Chau*'s specification states "[i]n the preferred salicide process a titanium layer is first blanket deposited over the entire device. The device is then temperature cycled to cause a reaction between the deposited titanium layer and any exposed silicon surface (i.e., semiconductor material 314 on gate electrode 306 and semiconductor material 314 on source/drain contact region 319) to form titanium silicide 320 (i.e. $TiSi_x$).

(Ex. 1006, 17-18; Ex. 1002, ¶94). Therefore, Claim 5 is obvious over *Chau* in view of *Rodder*.

d. Claim 6

Claim 6 is obvious over *Chau* in view of *Rodder*. Claim 6 requires that the depth of the shallow junction is less than about 2500Å. When converted, this requires the junction to have a depth of less than about 250nm. (Ex. 1002, ¶95). The *Chau* reference discloses "a source/drain contact region 319 having a total thickness of between 0.15-0.25 μm." (Ex. 1006, 17). 0.15-0.25 μm, when converted, is equivalent to 150-250nm. (Ex. 1002, ¶95). Therefore, Claim 6 is

obvious over *Chau* in view of *Rodder*.

D. Ground 4: Claims 1 and 4-6 Are Unpatentable Under 35 U.S.C. § 103(a) as Obvious over *Rodder*

As supported by Dr. Baker's declaration, claims 1 and 4-6 of the '372 Patent are obvious in view of *Rodder* under an interpretation where the epitaxial silicon can be grown before the formation of a silicide.

1. Overview of the Prior Art of Ground 4

a. *Rodder*

Rodder's teachings are summarized above in Section VIII.C.1.b.

2. First Specific Identification of Challenge

a. Claim 1

The preamble of claim 1 states "[i]n an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made." *Rodder* discloses this limitation by its teaching of a "raised source/drain transistor indicated generally at 10. … A gate 18 is formed in moat 16 and separated from semiconductor substrate 12 by a gate insulator 20. Formation of gate 18 defines interim areas 22 for the formation of source/drain regions. An initial implantation step is used to form ultra-shallow junctions 24 which electrically connect the source/drain regions to the channel region 26 underlying gate 18." (Ex.1008, 3:11-23; Ex. 1002, ¶97).

Claim 1 of the '372 Patent requires an integrated circuit that includes a single crystalline silicon substrate and a shallow junction for both the source and drain of the transistor underlying the upper surface of the silicon substrate. The single crystalline silicon substrate is depicted in *Rodder* as the semiconductor substrate 42 in FIG. 2A. (Ex. 1002, ¶97). Further, *Rodder* discloses "wherein said substrate comprises crystalline silicon." (Ex. 1008, 7:24-25).

The shallow source and drain is depicted as an ultra shallow junction 56 in FIG. 2A or, alternatively, as a shallow junction 68 in FIG. 2D. (Ex. 1008, 4:3-29, 5:4-18; Ex. 1002, ¶97).

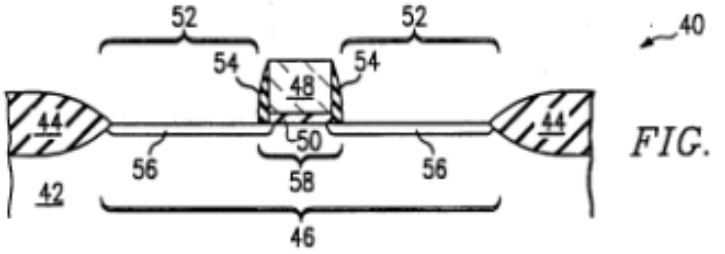


FIG. 2A

Claim 1 of the '372 Patent further requires a metal silicide layer having a lower surface disposed adjacent to the junctions. This feature can be found in FIG. 2D of *Rodder* as silicide regions (72 and 74). (Ex. 1002, ¶97). Further, the specification of the *Rodder* reference describes these silicide regions as "low resistance," and may be created by placing a layer of titanium over the entire structure. (Ex. 1008, 5:19-26; Ex. 1002, ¶97).

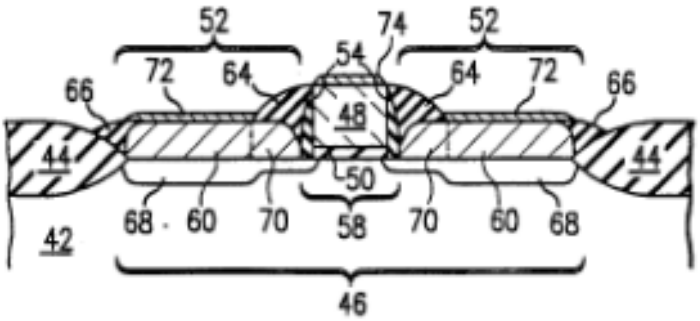


FIG. 2D

Claim 1 of the '372 Patent further requires an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent to the shallow junction of each the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of each the source and drain. The '372 Patent describes this epitaxial silicon layer as a "solid phase epitaxy layer." (Ex. 1001, 4:62-5:3).

Rodder discloses an epitaxial silicon layer in FIG. 2D as the raised source/drain 60. (Ex. 1008, 4:34-36; Ex. 1002, ¶97). This raised source/drain 60 is disposed below the lower surface of the silicide region 72. (Ex. 1008, 5:4-33). Further, the raised source/drain 60 is disposed above the shallow junction 68. (Ex. 1002, ¶97). Therefore, the epitaxial layer is disposed between the upper silicon surface and the lower surface of the metal silicide. (*Id.*). The epitaxial layer is disposed adjacent to the source/drain as it is located above the shallow junctions 68. (*Id.*). Further, the metal silicide 72 does not encroach upon the shallow junctions as the silicide region 72 is located above the raised source/drain 60. (*Id.*).

Rodder renders claim 1 obvious under an interpretation where the epitaxial silicon layer can be formed prior to silicide layers being formed. (Ex. 1002, ¶¶96-97).

b. Claim 4

Claim 4 is obvious in view of *Rodder.* Claim 4 requires that the shallow junctions must be a P+/N junction. *Rodder* discloses that "[j]unctions 56 are formed by implanting either N-type (e.g. arsenic, phosphorus or antimony) or P-type (e.g., boron) material ... ." (Ex. 1008, 4:9-12). This means that the junctions can be doped P+/N if desired. (Ex. 1002, ¶98). Thus, claim 4 is obvious over *Rodder*.

c. Claim 5

Claim 5 is obvious in view of *Rodder*. Claim 5 requires that the "gate includes and [sic - an] upper surface and a silicide layer is disposed on said upper layer." FIG. 2D of *Rodder* shows that the silicide layer 74 is formed over the gate portion as required by this claim. *Rodder* confirms this disclosure when it states that "[l]ow resistance silicide regions 72 and 74 are formed over raised source/drain regions 60 and gate 48, respectively. The formation of silicide regions 72 and 74 may be effected by placing a layer of titanium over the entire structure and then reacting the same in a nitrogen ambient. Silicon from raised source/drain regions 60 will react with the titanium layer thereby forming titanium

silicide ($TiSi_2$) over the exposed silicon regions." (Ex. 1008, 5:19-26; Ex. 1002, ¶99). Thus, claim 5 is obvious over *Rodder*.

d. Claim 6

Claim 6 is obvious in view of *Rodder*. Claim 6 requires that the depth of the shallow junction is less than about 2500Å. When converted, this requires the junction to have a depth of less than about 250nm. (Ex. 1002, ¶100). FIG. 2A discloses an ultra shallow junction 5. (Ex. 1008, FIG. 2A). Therefore, one of skill in the art would have understood, at the time of the disclosure, that ultra shallow junctions are less than 250 nm. (Ex. 1002, ¶100).

E. Ground 5: Claims 1 and 4-6 Are Unpatentable Under 35 U.S.C. § 103(a) as Obvious over *Ogasawara*

As supported by Dr. Baker's declaration, claims 1 and 4-6 of the '372 Patent are obvious in view of *Ogasawara* under an interpretation where the epitaxial silicon can be grown before the formation of a silicide layer.

1. Overview of the Prior Art of Ground 5

a. *Ogasawara*

Japanese Patent Application No. JP08-018049 ("*Ogasawara*") was published on January 19, 1996. (Ex. 1009 (foreign-language version and English-language translation, followed by declaration from translator)). *Ogasawara* is prior art under 35 U.S.C. § 102(b).

Ogasawara is directed to a method of fabricating a semiconductor device. (Ex. 1009, [0001]; Ex. 1002, ¶¶66-67). *Ogasawara* discloses, after the formation of the polysilicon gate electrode, amorphous silicon deposited along the entire substrate. (Ex. 1009, [0020]-[0028]; Ex. 1002, ¶67). Through a heat treatment at about 600C, the amorphous silicon is crystallized and forms an epitaxial layer on top of the silicon substrate. (Ex. 1009, [0025]-[0027]; Ex. 1002, ¶67). The remaining amorphous silicon may be removed and the newly formed epitaxial layer forms the raised source/drain region. (Ex. 1009, [0027]-[0028]; Ex. 1002, ¶67).

Next, a heat treatment is conducted and low-concentration diffusion zone n-layers are created from an impurity diffusion that resulted in impurities being located in the raised source/drain. (Ex. 1009, [0027]-[0028]; Ex. 1002, ¶68). Next, a metal film is deposited on top of the raised source/drain region. (Ex. 1009, [0029]-[0030]; Ex. 1002, ¶69). Then a heat treatment is conducted, causing a silicide to form on top of the raised source/drain regions. (*Id.*).

2. First Specific Identification of Challenge

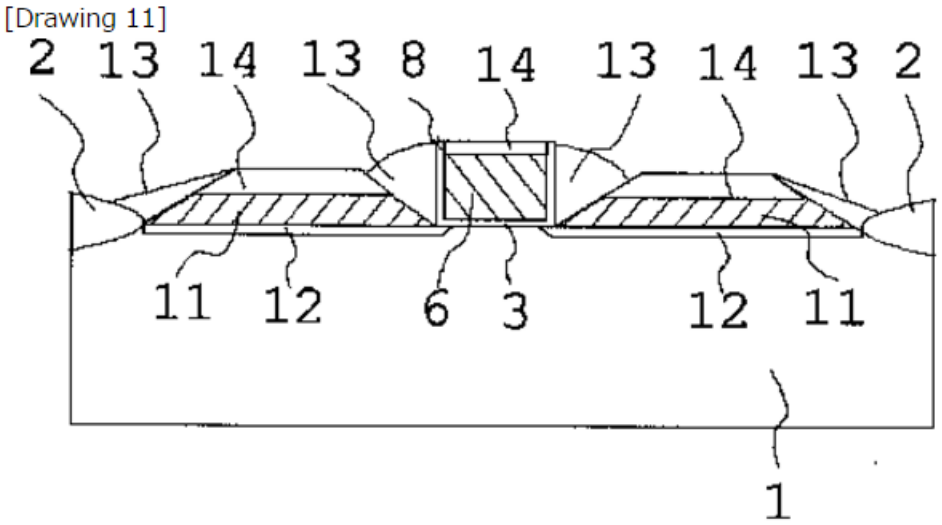
a. Claim 1

The preamble of claim 1 requires "[i]n an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made."

Ogasawara discloses the "industrial application" of the disclosure "relates to the manufacturing method of a semiconductor device, and relates to the manufacturing method of the MOS transistor of raised source/drain structure in detail." (Ex. 1009, [0001]; Ex. 1002, ¶102).

Claim 1 of the '372 Patent requires an integrated circuit that includes a single crystalline silicon substrate and a shallow junction for both the source and drain of the transistor underlying the upper surface of the silicon substrate.

The single crystal silicon is depicted in *Ogasawara* as single crystal silicon 1 in Fig. 11. (Ex. 1009, [0016]; Ex. 1002, ¶102). The shallow junctions for both the source and drain are depicted in Fig. 11 of *Ogasawara* as diffusion zone n- layers 12. (Ex. 1009, [0027]-[0028]; Ex. 1002, ¶102).



Claim 1 of the '372 Patent further requires a metal silicide layer having a lower surface disposed adjacent to the junctions. This feature can be found in

Fig. 11 of *Ogasawara* as silicide 14, which is created from a metal film. (Ex. 1009, [0028]-[0029]; Ex. 1002, ¶102).

Claim 1 of the '372 Patent further requires an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent to the shallow junction of each the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of each the source and drain. The '372 Patent describes this epitaxial silicon layer as a "solid phase epitaxy layer." (Ex. 1001, 4:62-5:3). *Ogasawara* discloses a structure of an epitaxial layer grown from amorphous silicon, as raised source/drain region 11. (Ex. 1009, [0025]-[0027], FIG. 7; Ex. 1002, ¶102). This epitaxial layer is disposed above the junction, diffusion zone n-layers 12. (Ex. 1002, ¶102). This epitaxial layer is disposed below metal silicide 14. (*Id.*).

Further, FIG. 11 of *Ogasawara* depicts that the metal silicide layer 14 does not extend below the upper silicon surface and encroach upon the shallow junction of the source and drain. (*See* Ex. 1009, [0029]-[0030]; Ex. 1002, ¶102). Therefore, the epitaxial silicon layer is disposed between the silicon surface and said lower surface of metal silicide and adjacent to the shallow junction of each the source and drain whereby the metal silicide does not extend below the upper

silicon surface and encroach upon the shallow junction of each the source and drain. (*Id.*).

Ogasawara renders claim 1 obvious under an interpretation where the epitaxial silicon layer can be formed prior to silicide layers being formed. (Ex. 1002, ¶¶101-102).

b. Claim 4

Claim 4 is obvious in view of *Ogasawara.* Claim 4 requires that the shallow junctions must be P+/N junctions. *Ogasawara* discloses that

> Incidentally, the present invention is not limited to the above embodiment, and may be carried out as described below. (1) A P channel MOS transistor with a raised source-drain structure is also manufactured in the same manner as the embodiment above. In this case, the P type single crystal silicon substrate 1 is replaced with an N type single crystal silicon substrate or N well layer, the N type impurities are replaced with P type impurities (for example, boron ion), and the N type amorphous silicon 9 is replaced with a P type amorphous silicon. The other steps are the same as in the embodiment described above. By this, a high concentration raised source-drain and a low concentration p^- layer can by formed on an N type single crystal silicon substrate.

(Ex. 1009, [0034]; Ex. 1002, ¶103). Thus, claim 4 is obvious over *Ogasawara*.

c. Claim 5

Claim 5 is obvious in view of *Ogasawara*. Claim 5 requires that the "gate

includes and [sic - an] upper surface and a silicide layer is disposed on said upper layer." Fig. 11 of *Ogasawara* shows that the silicide layer 14 is formed over the gate portion as required by this claim. (Ex. 1009, [0029]; Ex. 1002, ¶104). Therefore, Claim 5 is obvious over *Ogasawara*.

d. Claim 6

Claim 6 is obvious in view of *Ogasawara*. Claim 6 requires that the depth of the shallow junction is less than about 2500Å. When converted, this requires the junction to have a depth of less than about 250nm. (Ex. 1002, ¶105). In *Ogasawara*, diffusion zone n- layers 12 have a depth of 0.05 micrometers, which, when converted, is 50 nm. (Ex. 1009, [0028]; Ex. 1002, ¶105). This is less than 250 nm; therefore, claim 6 is obvious in light of *Ogasawara.*

F. Ground 6: Claim 6 is Unpatentable Under 35 U.S.C. § 103(a) as Obvious over *Yu* in view of *Ogasawara*

As supported by Dr. Baker's declaration, claim 6 of the '372 Patent is obvious over *Yu* in view of *Ogasawara* under a proper claim interpretation, wherein the silicide is formed before the epitaxial silicon layer is grown.

1. Motivation to Combine

A POSA would have been motivated to combine *Yu* with *Ogasawara*. (Ex. 1002, ¶¶106-108). *Yu* is directed to "ultra-shallow junctions." (Ex. 1007, 1:11-16; Ex. 1002, ¶107). And *Yu* further discloses that "[t]he sidewall spacers 18 should be of a thickness which is sufficiently thin to allow dopants associated with

the junctions to advance a sufficient distance laterally so as to provide an electrical connection between the junctions and the transistor channel region, while still maintaining the shallow junction requirements." (Ex. 1007, 5:54-60). Thus, a POSA reading *Yu* would understand *Yu*'s intent to create shallow junctions to improve on prior art. (Ex. 1002, ¶¶106-108). A POSA reading *Yu* would take *Yu's* silence on the actual dimensions of its shallow junctions as a motivation to look to the dimension of other, contemporaneous shallow junction techniques to ascertain what dimensions could be achieved. (Ex. 1002, ¶107). *Ogasawara*, a reference having a very similar device fabrication structure to that of *Yu*, confirms that such devices could be manufactured having shallow junctions with depth less than 2500Å. (Ex. 1009, [0028]; Ex. 1002, ¶107). A POSA would therefore have understood reading *Yu* that its structures could be formed with dimensions in the range of those disclosed in *Ogasawara*. (Ex. 1002, ¶107). Such a POSA would have had an expectation of success, because he or she would have understood a shallow junction to mean less than 2500 Å. (Ex. 1002, ¶107). *KSR*, 550 U.S. at 420-421.

2. Specific Identification of Challenge

a. Claim 6

Claim 6 recites "[t]he integrated circuit of claim 1 wherein the depth of the shallow junction is less than about 2500 Å."

Yu does not disclose a particular junction depth for a shallow junction. Therefore, a POSA would look to another reference to determine the depth of the shallow junction. (Ex. 1002, ¶¶106-108). *Ogasawara* teaches or suggests "[t]he integrated circuit of claim 1 wherein the depth of the shallow junction is less than about 2500 Å."

When Angstroms (Å) are converted to nanometers (nm), the '372 Patent requires a junction having a depth of less than about 250nm. (Ex. 1002, ¶108). In *Ogasawara*, diffusion zone n- layers 12 have a depth of 0.05 micrometers, which is 50 nm. (Ex. 1009, [0028]; Ex. 1002, ¶108). This is less than 250 nm, and therefore, claim 6 is obvious over *Yu* in view of *Ogasawara*.

IX. SECONDARY CONSIDERATIONS

Petitioner is unaware of any secondary considerations of non-obviousness with regard to the '372 Patent (*see KSR*, 550 U.S. at 414-15 (2007)) and particularly is unaware of any considerations that have the requisite nexus to the claims such that the considerations support a finding of non-obviousness. *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995).

X. CONCLUSION

This Petition demonstrates a reasonable likelihood that claims 1 and 4-6 of the '372 Patent are unpatentable under 37 C.F.R. § 42.208(c). Petitioner requests the institution of IPR and cancellation of claims 1 and 4-6 of the '372 Patent.

Respectfully submitted by

K&L Gates LLP

By: /Benjamin E. Weed/
Benjamin E. Weed
Reg. No. 65,939

Certification of Service Under 37 C.F.R. § 42.6(e)(4)

A copy of this Petition for *Inter Partes* Review and supporting materials has been served at the following correspondence address of record for the subject patent via Federal Express Priority Overnight® on this 20th day of July, 2017:

FOLEY & LARDNER
777 East Wisconsin Ave.
Milwaukee, WI 53202

By: /Benjamin E. Weed/
Reg. No. 65,939
K&L Gates LLP
70 W. Madison Street, Suite 3100
Chicago, IL 60602
benjamin.weed.PTAB@klgates.com
T: (312) 781-7166
F: (312) 827-8152

Certification of Word Count Under 37 C.F.R. § 42.24(d)

The undersigned hereby certifies that the foregoing Petition for *Inter Partes* Review contains 13,569 words according to the word count of the word-processing software used to prepare the petition.

By: /Benjamin E. Weed/

Reg. No. 65,939
K&L Gates LLP
70 W. Madison Street, Suite 3100
Chicago, IL 60602
benjamin.weed.PTAB@klgates.com
T: (312) 781-7166
F: (312) 827-8152