Paper No. __
Filed: May 12, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 6,172,554

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,172,554

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-3, 14-16, 22, and 28-36 of U.S. Patent No. 6,172,554 ("the '554 patent") (Ex.1001), which, according to PTO records, is assigned to Promos Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Austin Semiconductor, LLC, and Samsung Semiconductor, Inc.

Related Matters: Patent Owner has asserted the '554 patent against Petitioner and the other real parties-in-interest in *Promos Technologies Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 1:16-cv-00335-SLR (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 6,069,507 ("the '507 patent"), 7,375,027 ("the '027 patent"), 6,208,574 ("the '574 patent"), 6,559,044 ("the '044 patent"), and 6,562,714 ("the '714 patent") in this action. Petitioner is also concurrently filing IPR petitions on the '507, '027, '574, '044, and '714 patents. Petitioner also previously filed several IPR petitions involving additional patents asserted by Patent Owner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Specifically, on October 7, 2016,

Petitioner filed IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. All of these proceedings were instituted and remain pending except for the 00033 and 00035 proceedings.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel is (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '554 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1-3, 14-16, 22, and 28-36

("challenged claims") of the '554 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following grounds:

Ground 1: Claim 22 is unpatentable under pre-AIA 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,744,998 ("*Ito*") (Ex.1005);

Ground 2: Claims 28 and 29 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Ito* (Ex.1005) and U.S. Patent No. 5,602,506 ("*Kim*") (Ex.1006);

Ground 3: Claims 1-3, 14-16, 30, 31, and 36 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,886,567 ("*Park*") (Ex.1007) and Baker, R. J., CMOS Circuit Design, Layout, and Simulation, First Edition ("*Baker*") (Ex.1008);

Ground 4: Claims 32-34 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Park* (Ex.1007), *Baker* (Ex.1008), and U.S. Patent No. 5,818,290 ("*Tsukada*") (Ex.1009); and

Ground 5: Claim 35 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over *Park* (Ex.1007), *Baker* (Ex.1008), and U.S. Patent No. 4,710,647 ("*Young*") (Ex.1012).

The ’554 patent issued from U.S. Application No. 09/160,363 (“the ’363 application”) filed September 24, 1998. (Ex.1001, Cover). *Kim* issued on February 11, 1997. *Baker* was published in August 1997 and was available in August 1997 to those interested in the technologies to which *Baker* is directed to. (Ex.1002, ¶¶16-17.) Indeed, *Baker* was received by the Library of Congress on August 19, 1997 (Ex.1008, 8) and the Internet Archive has a record of the IEEE’s website documenting “New & Bestselling IEEE Books in Circuits & Systems” as of July 12, 1997, and indicating to its readers that *Baker* will be available in August 1997 and providing a link for ordering *Baker*. (Ex.1013, 4-5.) *Young* issued on December 1, 1987. Thus, *Kim*, *Baker*, and *Young* qualify as prior art at least under pre-AIA 35 U.S.C. § 102(b) with respect to the ’554 patent.

Ito issued on April 28, 1998 from U.S. Patent Application No. 760,010 filed December 3, 1996. *Park* issued on March 23, 1999 from U.S. Patent Application No. 890,601 filed July 9, 1997. *Tsukada* issued on October 6, 1998 from U.S. Patent Application No. 601,242 filed February 14, 1996. Thus, *Ito*, *Park*, and *Tsukada* qualify as prior art at least under pre-AIA 35 U.S.C. § 102(e) with respect to the ’554 patent.

None of the references relied upon in this Petition, except for *Ito*, were considered by the Patent Office during prosecution of the ’554 patent. (*See generally* Ex.1001, References Cited.) *Ito* was considered by the Patent Office

during prosecution, but Petitioner presents *Ito* in a new light never considered by the Office. (*See infra* Sections IX.A-IX.B.) For example, the prosecution history of the '554 patent does not include substantive discussion of *Ito* relating to patentability of the '554 patent claims. Although the Examiner stated that *Ito* "is cited as of interest because it discloses an internal voltage circuit having superior responsibility" (Ex.1004, 65), *Ito* was not the basis for any claim rejections. Here, Petitioner presents testimony from R. Jacob Baker, Ph.D., P.E. (Ex.1002), an expert in the field of the '554 patent, who confirms that the relevant teachings of *Ito* alone or in combination with *Kim* disclose or suggest what is claimed by challenged claims 22, 28, and 29 of the '554 patent. (*See* Ex.1002.) As such, consideration of *Ito* by the Patent Office during prosecution of the '554 patent should not preclude the Board from considering and adopting the grounds in this petition that involve *Ito*.

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '554 patent ("POSITA"), which for purposes of this proceeding is the mid-to-late 1990s (including September 24, 1998, the filing date of the U.S. Application maturing into the '554 patent), would have had at least a bachelor's degree in electrical engineering or a similar field, and at least two to three years of

experience in integrated circuit design. (Ex.1002, ¶20.)[1] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '554 PATENT AND PRIOR ART

A. The '554 Patent

The '554 patent issued from U.S. Application No. 09/160,363 filed on September 24, 1998 (Ex.1001, Cover) and is entitled "Power Supply Insensitive Substrate Bias Voltage Detector Circuit." The '554 patent is directed to a method of providing a bias voltage. (Ex.1001, 1:6 ("providing voltages"), Abstract; Ex.1002, ¶¶40-43; *see also* Ex.1002, ¶¶22-39 (citing Exs. 1008, 1011).)

During prosecution, the Examiner indicated that, in then-pending claims 7, 27, and 51 (which issued as independent claims 1, 15, and 30, respectively), the limitation "an inverter (12) having an input terminal connected to a first node (11), the inverter possessing a trip point which is substantially insensitive to power supply voltage (Vcc) variations, whereby the bias voltage is obtained when the node voltage and the trip point of the inverter are substantially the same" was the basis for allowance. (Ex.1004, 87 (Notice of Allowability dated June 13, 2000).) In addition, in then-pending claim 34 (which issued as independent claim 22), the

[1] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '554 patent. (Ex. 1002, ¶¶4-14; Ex. 1003.)

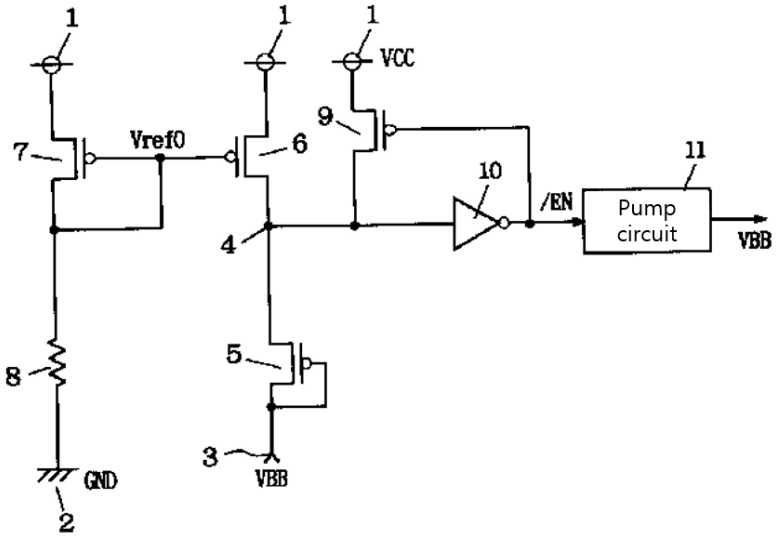
limitation "detector circuit . . . allowing the bias voltage V1 to get arbitrarily close to the ground voltage but not allowing the bias voltage V1 to become positive" was the basis for allowance. (*Id.*)

As discussed below, the features which the Examiner found to be allowable are actually disclosed by the prior art cited in this petition. (Ex.1002, ¶¶64-221.)

B. *Ito*

Ito relates to "a substrate voltage detecting circuit for detecting a substrate voltage in a semiconductor memory device such as a DRAM (Dynamic Random Access Memory) and activating a substrate voltage generation circuit." (Ex.1002, ¶¶46-48.) (Ex.1005, 1:6-12.) *Ito* discloses that a "substrate voltage detecting circuit … is connected to charge pumping circuit 11 in order to retain the substrate voltage VBB at a prescribed level." (*Id.*, 1:15-22, FIG. 9.) In particular, *Ito*'s "charge pumping circuit 11 [] generat[es] a negative substrate voltage VBB to be supplied to a semiconductor substrate." (*Id.*)

[FIG. 9]

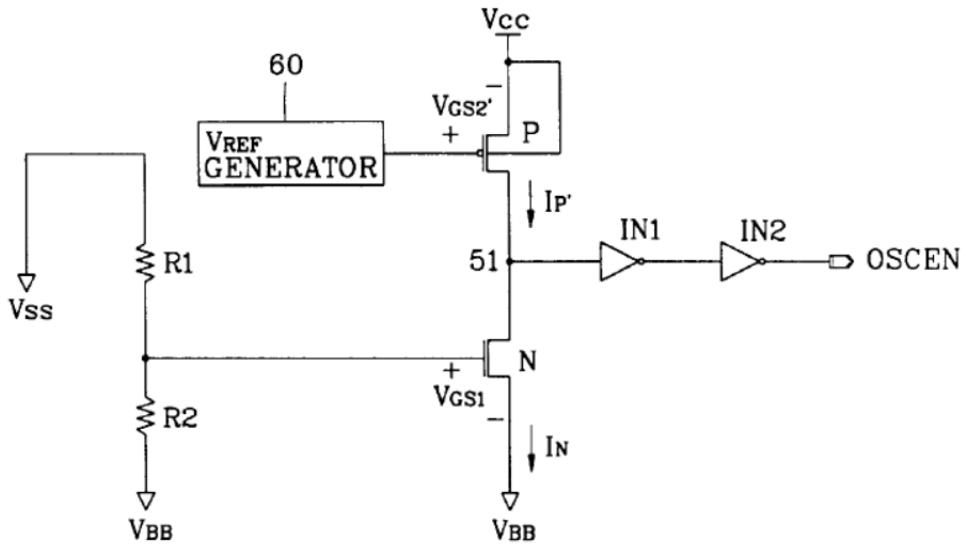


(Ex.1005, FIG. 9.)

C. *Park*

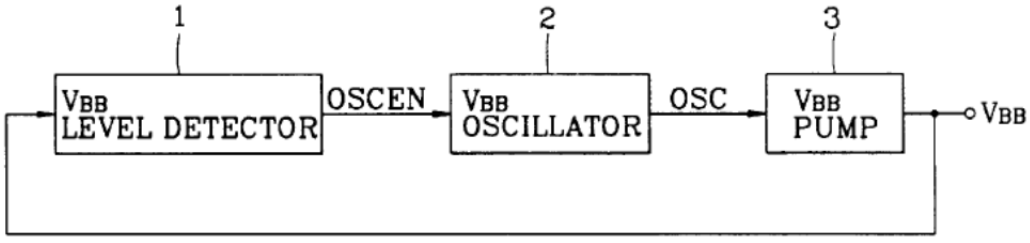
Park discloses "a back bias voltage level detector," which is illustrated in figure 5. (Ex.1002, ¶¶53-55.) (Ex.1007, 4:44-45; FIG. 5.) The "back bias voltage level detector" generates an oscillator enable signal OSCEN. (Ex.1007, FIG. 5, 4:58-5:45.) *Park* further discloses that when "OSCEN becomes a high electrical potential, … the back bias voltage oscillator 2, as shown in FIG. 1, outputs a pulse OSC." (Ex.1007, 5:26-28, FIG. 1.) "OSC is inputted to the back bias voltage pump 3," which in turn generates the back bias voltage V_{BB}. (*Id*., 5:40-45, FIG. 1.)

FIG. 5



(*Id.*, FIG. 5.)

FIG. 1
CONVENTIONAL ART

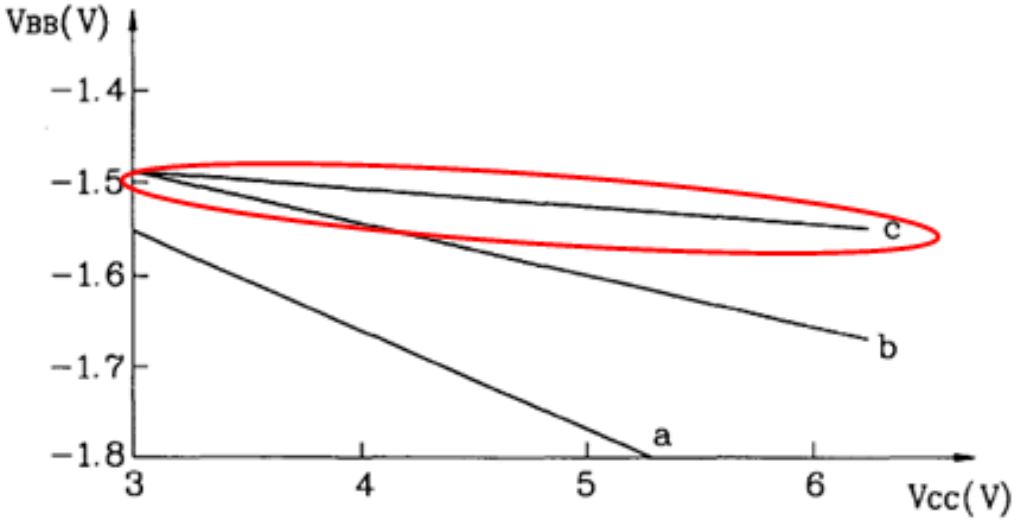


(*Id.*, FIG. 1.)

Park discloses "[a]s shown in c of FIG. 8, the circuit of FIG. 5 according to the present invention has more stable back bias voltage [V_{BB}] level with respect to

the variation of the external voltage V_{CC} compared to the conventional circuits." (*Id.*, 5:12-14, 6:32-35.) *Park* discloses that "even if the external voltage V_{CC} is varied … the back bias voltage V_{BB} is stable." (*Id.*, 6:39-42.)

FIG. 8



(Ex.1002, ¶55, citing Ex.1007, FIG. 8 (annotated to show V_{BB} is stable even when there are variations in V_{CC}).)

VIII. CLAIM CONSTRUCTION

Should the Board institute *inter partes* review, the '554 patent will expire on September 24, 2018, i.e., during the pendency of the instituted proceeding. Accordingly, the claims of the '554 patent should be construed under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See,*

e.g., *Square Inc. v. J. Carl Cooper*, IPR2014-00156, Paper No. 38 at 7 (May 14, 2015) (citing *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). Under *Phillips*, claim terms are given their ordinary and customary meanings, as would be understood by a POSITA having taken into consideration the language of the claims, the specification, and the prosecution history of record. *See, e.g.*, *Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 20 at 2-3 (July 10, 2014).

The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Petitioner submits that for purposes of this proceeding, the terms of the challenged claims should be given their ordinary and customary meaning consistent with *Phillips*.[2] (Ex.1002, ¶45.)

[2] Petitioner does not concede that the challenged claims are not invalid under one or more sections of 35 U.S.C. § 112, which is something that cannot be pursued in this proceeding under the Rules.

IX. DETAILED EXPLANATION OF GROUNDS

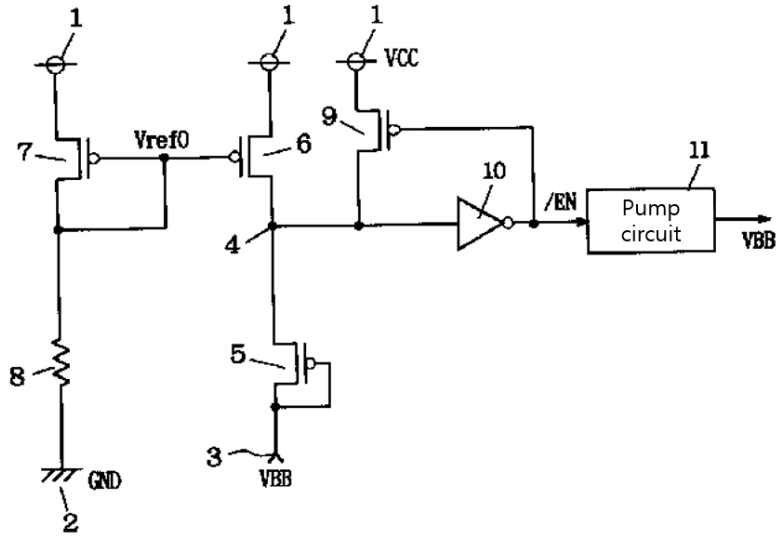
A. Ground 1: *Ito* Anticipates Claim 22

1. Claim 22

a) **"A circuit comprising:"**

To the extent the preamble is limiting, *Ito* discloses this feature. (Ex.1002, ¶65-66.) For instance, figure 9 of *Ito* discloses a "substrate voltage detecting circuit." (Ex.1005, 1:19-22.) *Ito* discloses that the circuit illustrated in figure 9 is used in a semiconductor memory device such as a DRAM. (*Id*. 1:15-18.) The DRAM memory device disclosed in *Ito*, which includes the circuit illustrated in figure 9, is a "circuit," as claimed. (Ex.1002, ¶66.) (*See also* citations and analysis below for the remaining elements of this claim.)

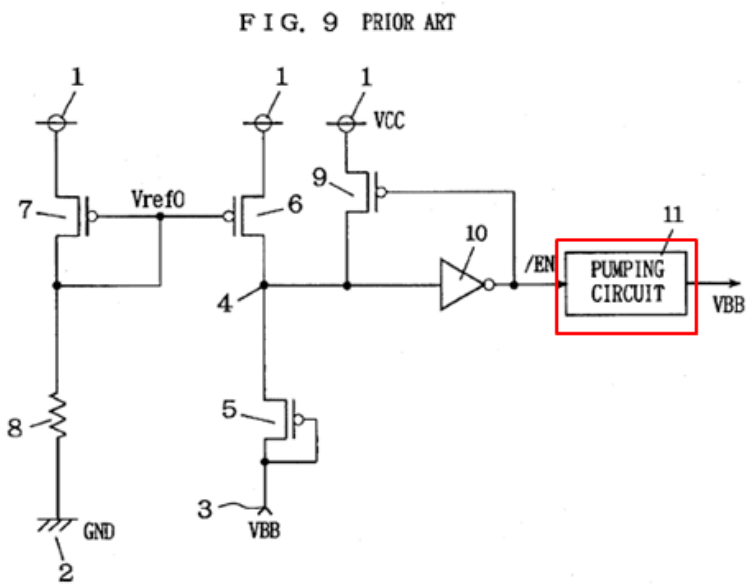
[FIG. 9]



(Ex.1005, FIG. 9.)

b) **"a voltage generator for generating a bias voltage V1; and"**

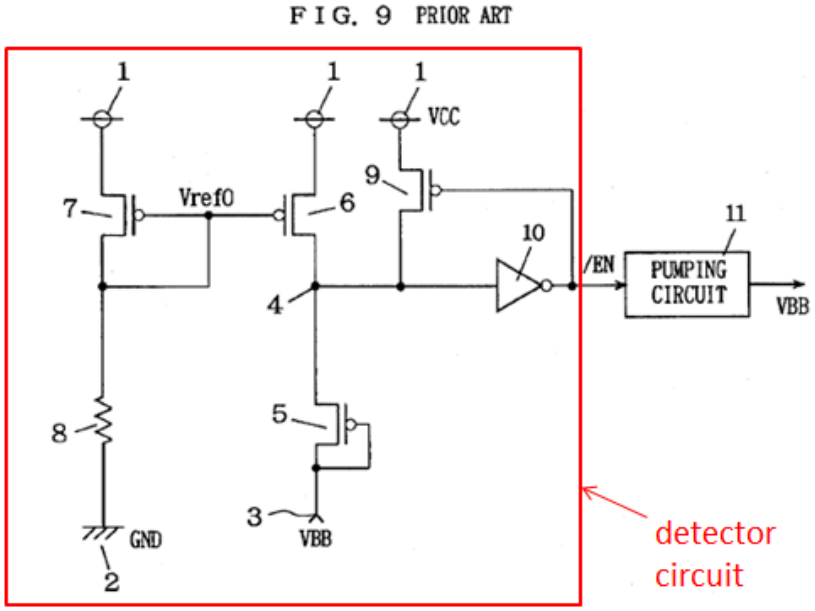
Ito discloses this feature. For instance, *Ito* discloses "[a] charge pumping circuit 11 for generating a negative substrate voltage VBB to be supplied to a semiconductor substrate." (Ex.1005, 1:15-17; *see also id.*, 1:55-57, 1:61-63, 1:64-66; Ex.1002, ¶¶67-68.) A POSITA would have understood "BB" in the label "VBB" refers to "back bias" and that voltage VBB, which is supplied to the semiconductor substrate, is a "bias" voltage that biases the substrate. (Ex.1002, ¶69.) The charge pumping circuit 11 ("voltage generator") for generating the voltage VBB ("bias voltage V1") is shown below in red.



(Ex.1002, ¶69, citing Ex.1005, FIG. 9 (annotated).)

c) **"a detector circuit for detecting the bias voltage V1 and regulating the voltage generator to maintain the bias voltage V1 at a substantially constant negative level,"**

Ito discloses this feature. For instance, *Ito* discloses that the "substrate voltage detecting circuit … is connected to charge pumping circuit 11" (Ex.1005, 1:19-21), so a POSITA would have understood that *Ito*'s substrate voltage detecting circuit ("detector circuit") corresponds to the portion of figure 9 shown in red below. (Ex.1002, ¶¶70-71.)

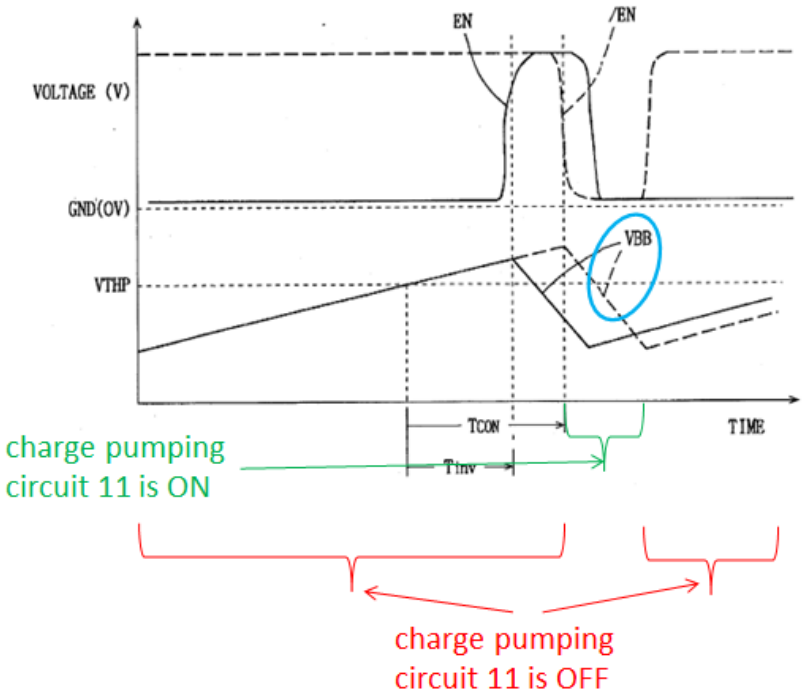


(Ex.1002, ¶71, citing Ex.1005, FIG. 9 (annotated).)

Ito discloses that the detector circuit is for detecting the substrate voltage VBB and generating an enable signal /EN which controls charge pumping circuit 11. (Ex.1002, ¶72.) When VBB is detected as more negative than the negative

threshold voltage of PMOS transistor 5, the /EN signal is generated high such that the charge pumping circuit is off. (Ex.1005, 1:38-45.) When VBB is detected as higher than the threshold voltage VTHP, the /EN signal is generated low such that the charge pumping circuit is turned on to pull VBB more negative. (*Id.*, 1:50-57; Ex.1002, ¶¶72-74.)

FIG. 2



(Ex.1002, ¶72, citing Ex.1005, FIG. 2 (annotated to show VBB in blue, and ON and OFF time periods for charge pumping circuit 11 corresponding to dotted line VBB in green and red, respectively).)

Thus, *Ito*'s "substrate voltage detecting circuit" (*id.*, 1:1-20) (shown in red in FIG. 9 above) detects whether VBB is lower or higher than voltage VTHP.

(Ex.1002, ¶75.) That is, *Ito*'s "substrate voltage detecting circuit" is "a detector circuit for detecting the bias voltage V1." (*Id.*) Moreover, *Ito*'s detecting circuit controls charge pumping circuit 11 to either operate (which causes voltage VBB to decrease, *see* Ex.1005, 1:55-57) or not operate (*see id.*, 2:1-4). (Ex.1002, ¶75.) A POSITA would have understood that controlling *Ito*'s charge pumping circuit 11 in this manner constitutes "regulating the voltage generator." (*Id.*)

Ito discloses that the detector circuit controls the charge pump such that VBB is maintained at a prescribed level, which is a negative voltage ("regulating the voltage generator to maintain the bias voltage V1 at a substantially constant negative level"). (Ex.1002, ¶76.) For instance, *Ito* discloses controlling the charge pumping circuit 11 "in order to retain the substrate voltage VBB at a prescribed level." (Ex.1005, 1:21-22.) Specifically, *Ito* discloses that "when the substrate voltage VBB attains a prescribed level, charge pumping circuit 11 will not generate the substrate voltage VBB." (*Id*., 1:46-48.) This "prescribed level" is a voltage "lower than threshold voltage VTHP (***negative***) of p channel MOS transistor 5" because charge pumping circuit will be activated when VBB "increases to be higher than . . . VTHP" and will stop operating "[w]hen the substrate voltage VBB is made sufficiently lower than the threshold voltage VTHP . . . ." (*Id*., 1:37-2:4 (emphasis added); Ex.1002, ¶76.) Because VBB is maintained at a "prescribed level," which *Ito* discloses is below VTHP that is a "negative" level (*id.*, 1:29

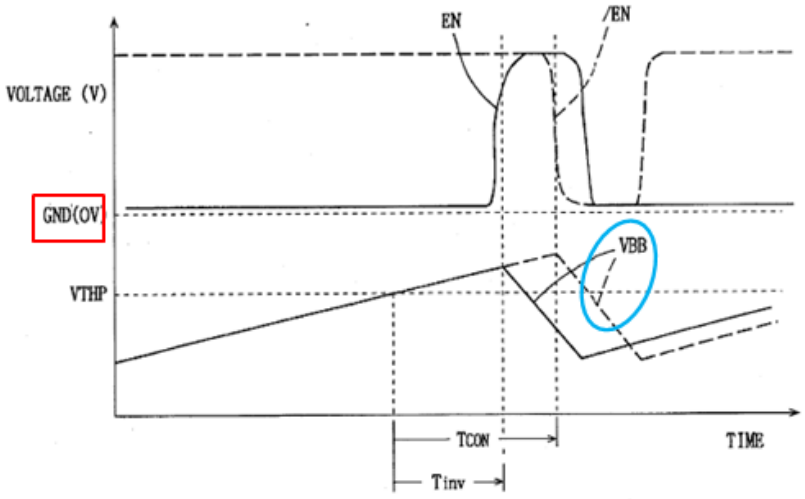
("threshold voltage VTHP (negative)", 1:15-21), *Ito* discloses maintaining VBB "at a substantially constant negative level," as claimed. (Ex.1002, ¶76.) Indeed, as shown in figure 2 of *Ito*, VTHP is less than 0V, and thus the "prescribed level" is also a "negative" value. (Ex.1005, FIG. 2; Ex.1002, ¶76.)

d) **"the detector circuit allowing the bias voltage V1 to get arbitrarily close to the ground voltage but not allowing the bias voltage V1 to become positive."**

Ito discloses this feature. For instance, figure 2 of *Ito* (annotated below) discloses the detector circuit allowing substrate voltage VBB ("the bias voltage V1") to get arbitrarily close to the level indicated in FIG. 2 as "GND (0V)" ("arbitrarily close to the ground voltage") but not allowing VBB to rise above 0V ("but not allowing the bias voltage V1 to become positive"). (Ex.1005, FIG. 2; *see also supra* Section IX.A.1(c) regarding "the detector circuit"; Ex.1002, ¶77.) Indeed, *Ito* discloses that the circuit of figure 9 "generate[s] a negative substrate voltage VBB" and "retain[s] the substrate voltage VBB at a prescribed level." (Ex.1005, 1:19-22.) As shown in FIG. 2 of *Ito*, the dotted line version of VBB, which corresponds to the prior art noted in *Ito*, becomes less negative (closer to 0V) than the threshold voltage VTHP. The solid line version of VBB corresponding to the embodiment of *Ito* in which a differential amplifier allows for reduced response time for turning on the charge pumping circuit to reduce VBB

after it crosses VTHP also becomes less negative than VTHP, but by less of a margin than the dotted line version. (Ex.1005, 5:7-18, FIG. 2; Ex.1002, ¶77.)

FIG. 2



(Ex.1002, ¶77, citing Ex.1005, FIG.2 (annotated to show ground voltage (0V) in red, and VBB in blue).)

B. Ground 2: *Ito* and *Kim* Render Obvious Claims 28 and 29

1. Claim 28

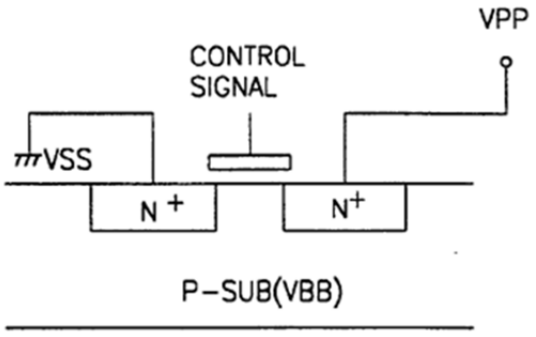
a) **"The circuit of claim 22 wherein the bias voltage V1 biases a P-type region that makes junction with at least one N-type region, and the bias voltage V1 is operable to make the junction reverse biased."**

Ito in combination with *Kim* discloses or suggests this feature. (Ex.1002, ¶¶78-85.) *Ito* does not provide details regarding the DRAM memory device for which the substrate voltage detecting circuit disclosed in *Ito* is used, and therefore *Ito* does not explicitly disclose that the substrate voltage VBB ("bias voltage V1") biases a P-type region that makes junction with at least one N-type region, and the

bias voltage V1 is operable to make the junction reverse biased. However, *Kim* discloses the details of this feature in the general context of a memory device, and it would have been obvious to combine the details of *Kim* with *Ito* to enable *Ito*'s circuit to be configured and implemented according to known configurations and memory designs, like those disclosed by *Kim*. (Ex.1002, ¶79.)

Kim discloses a back bias voltage generator for generating a back bias voltage (VBB) having a constant level. (Ex.1002, ¶80; Ex.1006, 1:6-12.) The back bias voltage VBB in *Kim* is applied, for example, to the substrate of a memory device. (Ex.1006, 1:6-12, 4:6-15.) *Kim* discloses that memory devices generally comprise circuits that include a transistor such as that shown in FIG. 6 of *Kim*. (Ex.1006, FIG. 6, 4:6-15.) *Kim* further discloses that "[a]s shown in FIG. 6, the transistor includes a P-type substrate to which the back bias voltage VBB is applied," (*see id.*) and therefore, *Kim* discloses that "the bias voltage V1 biases a P-type region," as recited in claim 28. (Ex.1002, ¶80.) The P-type substrate ("P-type region") is in contact with "N+ diffusion region having a drain for inputting the voltage Vpp." (Ex.1006, 4:6-15, FIG. 6; Ex.1002, ¶80.) Therefore, *Kim* discloses a "P-type region that makes junction with at least one N-type region." (Ex.1002, ¶80.)

FIG.6
PRIOR ART

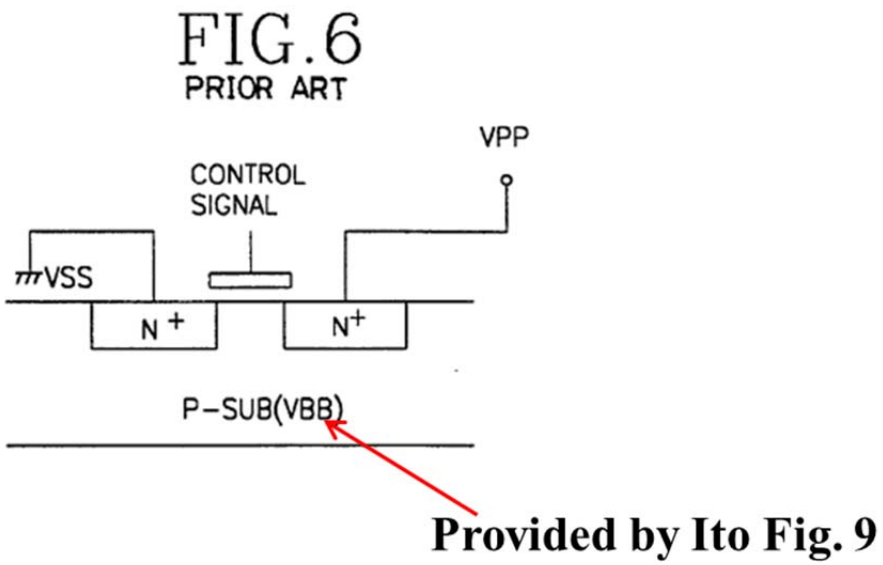


(Ex.1006, FIG. 6; Ex.1002, ¶80.)

Ito's charge pumping circuit 11, used in a memory device such as DRAM, "generat[es] a negative substrate voltage VBB to be supplied to a semiconductor substrate (***not shown***)." (Ex.1005, 1:15-18 (emphasis added).) It would have been obvious for a POSITA to combine the teachings of *Ito* and *Kim* such that *Ito*'s figure 9 circuit generates a bias voltage VBB for a P-type region that makes a junction with an N-type region, like that disclosed by *Kim*, where the negative bias voltage VBB is operable to make the junction reverse biased. (Ex.1002, ¶¶81-82.) Both *Ito* and *Kim* are directed to generating back bias voltages (VBB), and both *Ito* and *Kim* disclose using such a back bias voltage to bias the substrate for a memory device. A POSITA would have known at the time of the alleged invention to include a transistor such as that shown in figure 6 of *Kim* in the DRAM semiconductor memory device of *Ito* as such transistors were generally included in

memory devices, including DRAM memory devices. (Ex.1002, ¶¶35-39, 83.)

Biasing the substrate with a negative back bias voltage VBB generated by *Ito's* figure 9 circuit in such a combination would have been obvious as both *Ito* and *Kim* disclose applying a back bias voltage to the substrate in a memory device. (Ex.1006, FIG. 6, 4:9-15; Ex.1005, 1:15-22) Moreover, using a negative substrate bias was common in DRAMs as such biasing was known to provide many benefits, including preventing forward biasing of n+ to p-substrate pn junctions. (Ex.1002, ¶¶81-84, citing Ex.1008 at 368.) An exemplary demonstrative of the combined *Ito-Kim* features that may have been achieved is below:



(Ex.1006 at FIG. 6, annotated; Ex.1002 at ¶83.)

In such a combination, the junction between the P-type substrate biased by a negative VBB (as disclosed in *Ito*) and the N+ diffusion region that receives a

positive voltage Vpp[3] will be reverse-biased. (Ex.1001, 2:7-11; Ex.1002, ¶84.) Therefore, the combined *Ito-Kim* system further discloses that "the bias voltage V1 is operable to make the junction reverse biased." (Ex.1002, ¶84.)

In addition, the above modification of *Ito* based on *Kim* merely constitutes a combination of known prior art components (*Ito*'s substrate voltage detecting circuit of figure 9 connected to the charge pumping circuit 11 which are parts of a memory device and *Kim*'s figure 6 transistor which is also part of a memory device) according to known methods (providing a connection from *Ito*'s charge pumping circuit 11 to *Kim*'s substrate in figure 6 such that the back bias voltage VBB output from charge pumping circuit 11 is supplied to *Kim*'s figure 6 substrate) to yield predictable results (an operational memory device that is responsive to the back bias voltage being supplied by the charge pumping circuit 11) and hence, would have been obvious. (Ex.1002, ¶85.) *KSR Int'l Co. v. Teleflex, Inc.* ("*KSR*"), 550 U.S. 398, 416 (2007).

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[3] *Kim* discloses that "the voltage Vpp … is higher than the external voltage Vcc," and therefore a POSITA would have understood that Vpp will be a positive value while VBB is negative. (Ex. 1006 at 4:8-9; Ex. 1002, ¶84.)

2. Claim 29

a) **"The circuit of claim 28 wherein the circuit is a dynamic random access memory (DRAM) device."**

Ito in combination with *Kim* discloses or suggests this feature. For instance, *Ito* discloses that the figure 9 circuit is for use in a "semiconductor memory device such as a DRAM." (Ex.1005, 1:19-22.) Therefore, the DRAM of *Ito*, which includes the circuitry depicted in figure 9 of *Ito*, is a circuit that is a "dynamic random access memory (DRAM) device." (Ex.1002, ¶86.) (*Supra* Section IX.A.1(a).)

C. Ground 3: *Park* and *Baker* Render Obvious Claims 1-3, 14-16, 30, 31, and 36

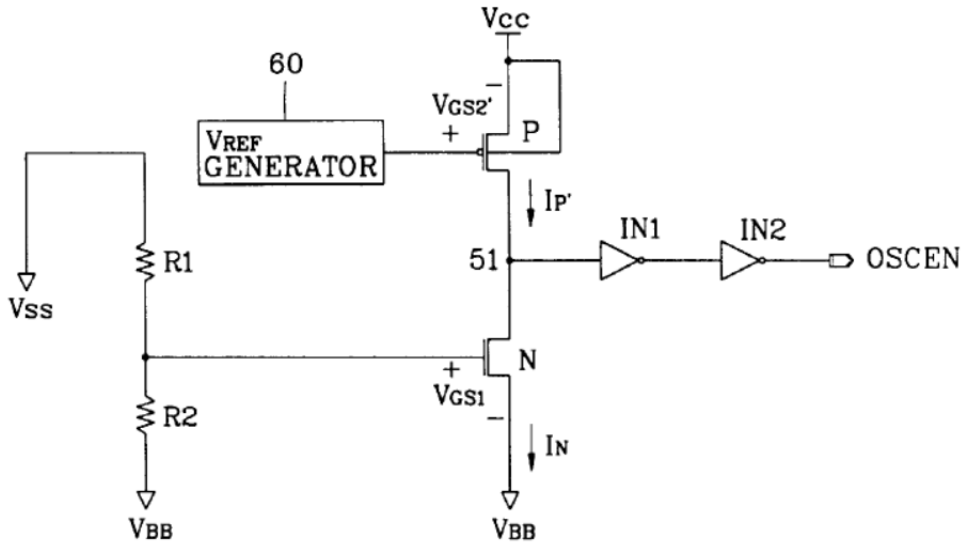
1. Claim 1

a) **"A circuit for providing a bias voltage V1 which is substantially insensitive to variations of a power supply voltage powering the circuit, the circuit comprising:"**

To the extent the preamble is limiting, *Park* discloses this feature. (Ex.1002, ¶¶87-91.) *Park* discloses "a back bias voltage level detector," which is illustrated in figure 5. (Ex.1007, 4:44-45; FIG. 5.) The "back bias voltage level detector" generates a signal OSCEN. (*Id.*, FIG. 5, 4:58-5:45; *see supra* Section VII.C.) *Park* further discloses that when "OSCEN becomes a high electrical potential, … the back bias voltage oscillator 2, as shown in FIG. 1, outputs a pulse OSC." (Ex.1007, 5:26-28.) "OSC is inputted to the back bias voltage pump 3," which in turn generates the back bias voltage V_{BB}. (*Id.*, 5:40-45, FIG. 1.) The combination

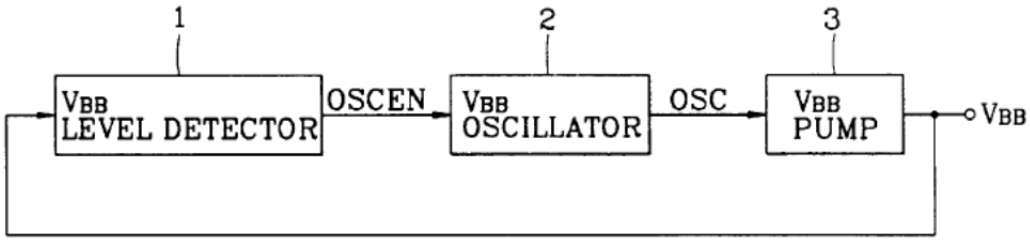
of the "back bias voltage level detector," "back bias voltage oscillator 2," and "back bias voltage pump 3" corresponds to the claimed "circuit." (Ex.1002, ¶88.)

FIG. 5



(Ex.1007, FIG. 5.)

FIG. 1
CONVENTIONAL ART

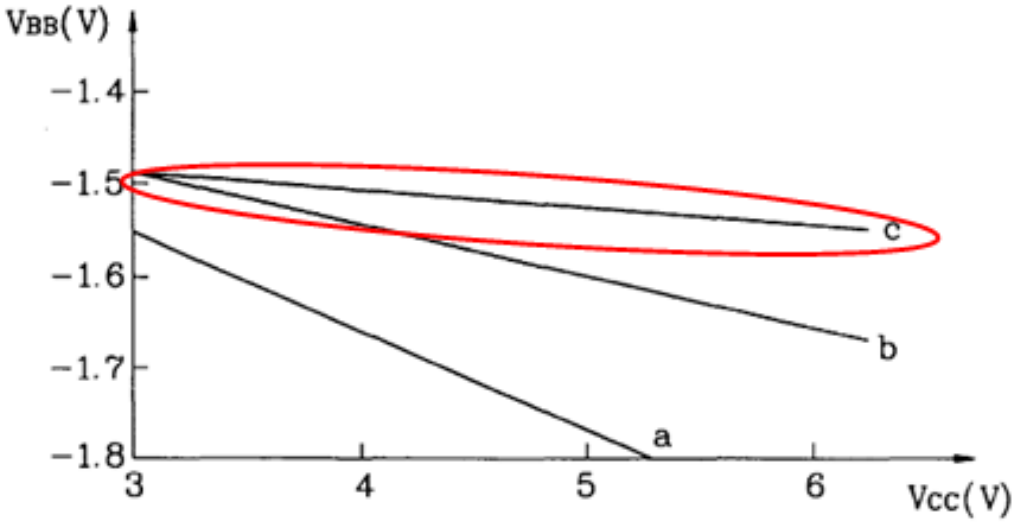


(*Id*., FIG. 1.)

Park discloses that the above "circuit" provides a back bias voltage V_{BB} ("bias voltage V1"). (Ex.1002, ¶89.) For instance, *Park* discloses that when "OSCEN becomes a high electrical potential, … the back bias voltage oscillator 2, as shown in FIG. 1, outputs a pulse OSC." (Ex.1007, 5:26-28.) "OSC is inputted to the back bias voltage pump 3," as a result of which "negative potential is applied to the substrate by a pumping operation" thereby increasing the "absolute value of the back bias voltage V_{BB}." (*Id.*, 5:29-32.)

Park discloses that the above "circuit" provides a "back bias voltage V_{BB}" ("a bias voltage V1") that is substantially insensitive to variations of an external voltage V_{CC} ("power supply voltage powering the circuit"). (Ex.1002, ¶90.) A POSITA would have readily understood that voltage V_{CC} applied to the circuit of figure 5 is "a power supply voltage powering the circuit." (*Id.*, ¶90.) The back bias voltage V_{BB} is substantially insensitive to variations of the external voltage V_{CC}. (Ex.1007, 5:12-14, 6:32-35.) Indeed, *Park* discloses that "even if the external voltage V_{CC} is varied … the back bias voltage V_{BB} is stable." (*Id.*, 6:39-42.)

FIG. 8

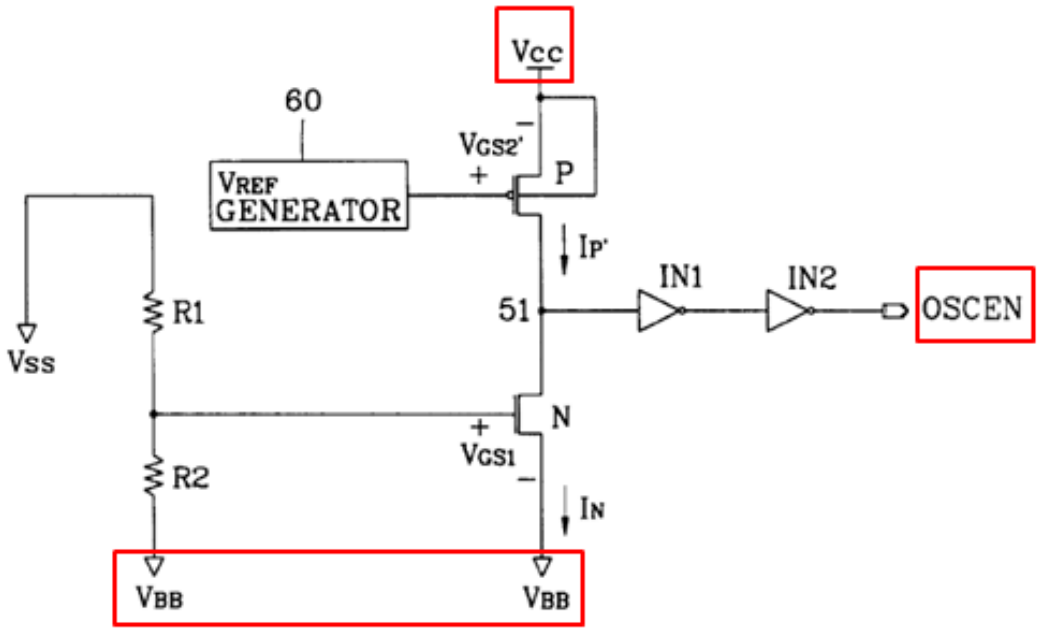


(Ex.1002, ¶91, citing Ex.1007, FIG. 8 (annotated to show V_{BB} is substantially insensitive to variations of V_{CC}).) (*See also* citations and analysis below for the remaining limitations of this claim.)

b) **"a detector circuit for generating a signal from the power supply voltage and the bias voltage V1,"**

Park discloses this feature. (Ex.1002, ¶¶92-96.) For instance, *Park* discloses a back bias voltage level detector ("detector circuit") shown in figure 5 for generating an oscillation enable signal OSCEN ("for generating a signal") from V_{CC} ("power supply voltage") and V_{BB} ("bias voltage V1"). (*Id.*) The OSCEN signal is generated based on the voltage at node 51, which is generated using both V_{CC} and V_{BB}. (Ex.1002, ¶92.)

FIG. 5



(Ex.1002, ¶92, citing Ex.1007, FIG. 5 (annotated to show V_{CC}, V_{BB}, and OSCEN), 4:44-45).)

Park's disclosure of "the operation of the back bias voltage level detector" with reference to figure 5 explains how signal OSCEN ("a signal") is generated from power supply V_{CC} and back bias voltage V_{BB}. (Ex.1007, 4:58-5:45, FIG. 5.) For example, *Park* discloses that signal OSCEN is generated from a current I_P' supplied by V_{CC} through transistor P. (Ex.1007, 4:58-5:45, FIG. 5; Ex.1002, ¶93.) Therefore, voltage V_{CC} is used by the detector circuit to generate signal OSCEN ("generating a signal from the power supply voltage"). (Ex.1002, ¶¶93-94.)

Park also discloses that signal OSCEN is generated by the detector circuit from V_{BB}. (*Id.*, ¶95-96.) For instance, *Park* discloses that "when the absolute value of the back bias voltage V_{BB} is increased, … the node 51 becomes a low electric potential." (Ex.1007, 5:33-39.) The voltage signal at node 51 is then used by inverter IN1 to generate a high or low output, and the output of inverter IN1 is inverted by inverter IN2 to generate signal OSCEN. (*Id.*, FIG. 5; Ex.1002, ¶96.)

c) **"wherein said signal is substantially insensitive to variations in the power supply voltage while being responsive to the bias voltage V1; and"**

Park in combination with *Baker* discloses or suggests this feature. *Park* discloses that OSCEN is generated from, and thus, responsive to the back bias voltage V_{BB} ("bias voltage V1"). (*See supra* citations and analysis for claim limitation 1(b); Ex.1002, ¶¶95-97.) As discussed immediately below, the OSCEN ("signal") is substantially insensitive to variations in the power supply voltage because the voltage at node 51 is substantially insensitive to variations in Vcc and OSCEN is generated using the voltage at node 51. (Ex.1002, ¶97, ¶¶104-106.)

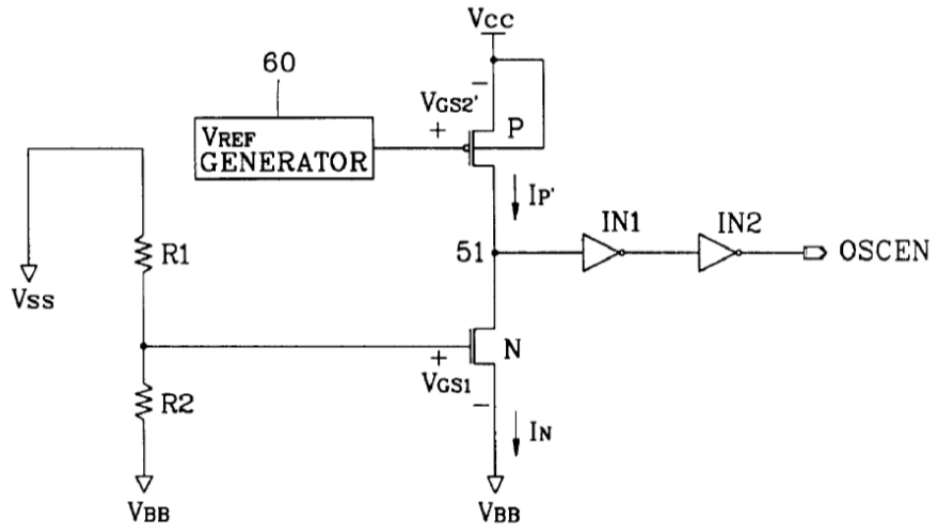
The voltage at node 51 is substantially insensitive to variations in V_{CC}

A POSITA would have understood that the voltage at node 51 in *Park* is affected by the current I_P' flowing into node 51 and current I_N flowing out of node 51. (*See* Ex.1007, FIG. 5; Ex.1002, ¶105.) But both these currents are substantially insensitive to variations in V_{CC}. (Ex.1002, ¶105.) For instance, *Park*

discloses that "[s]ince the difference V_{CC} -V_{REF} is constant, **it is possible to obtain constant current I_P' irrespective of the external voltage V_{CC}.**" (*Id.*, 5:12-14 (emphasis added).)

Similarly, current I_N is also substantially insensitive to variations in V_{CC} because I_N depends on V_{GS1}, which is the difference between the gate voltage of NMOS pull-down transistor N and V_{BB}. (*See* Ex.1007, FIG. 5, 5:18-20; Ex.1002, ¶106.) Both the gate voltage and V_{BB} are insensitive to variations in V_{CC}. (Ex.1002, ¶106.) As discussed above with respect to limitation 1(a), *Park* discloses that back bias voltage V_{BB} is insensitive to variations in V_{CC}. (See *supra* Section IX.C.1(a); Ex.1002, ¶106.) Moreover, the gate voltage of NMOS pull-down transistor N is also insensitive to variations in V_{CC} because resistors R1 and R2 connected in series divide the back bias voltage V_{BB} and bias the NMOS pull-down transistor N (Ex.1007, 5:14-16) and V_{BB} itself is "substantially insensitive" to variations in V_{CC} as discussed above. (Ex.1002, ¶106.)

FIG. 5



(Ex.1007, FIG. 5.)

A POSITA would have modified Park based on Baker to ensure that the "trip" point of inverter IN1 is substantially insensitive to variations in V_{CC}

A POSITA would have recognized that while the OSCEN signal in the circuit of figure 5 is quite insensitive to power supply variations (*see* discussion above), the switching or "trip" point of the inverter IN1 is a factor that could contribute to some power supply sensitivity for OSCEN.[4] (Ex.1002, ¶¶98-103 (see hypotheticals).) *Park* does not disclose that the "trip" point of inverter IN1 is

[4] The output of inverter IN1 is driven to either a "high" or a "low" and therefore the trip point of inverter IN2 does not impact generation of the OSCEN signal in the manner of the trip point of inverter IN1. (Ex. 1002, ¶100.)

substantially insensitive to variations in V_{CC}, but *Baker* discloses various details regarding inverters (Ex.1008, 201-228), including details regarding the trip point of an inverter, which *Baker* refers to as a "switching point" (*id*., 204-05; Ex.1002, ¶107.) *Baker* discloses the following equation for the switching point of an inverter comprising an NMOS transistor and a PMOS transistor (*see infra*, Section IX.C.2 (discussing that a typical and well-known construction of an inverter includes an NMOS transistor and a PMOS transistor).):

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

(Ex.1008, 205 (equation 11.4, where β_n and β_p are transconductance parameters of the NMOS and PMOS transistors, respectively, in the inverter, V_{THN} and V_{THP} are threshold voltages of the NMOS and PMOS transistors, respectively, and VDD is the power supply voltage); Ex.1002, ¶107.)

Based on *Baker*'s above equation regarding the switching point (trip point) of an inverter, a POSITA would have understood that the trip point will be "substantially insensitive" to variations in VDD (the label in *Baker* for the power supply voltage) if β_n is set much larger than β_p by sizing the NMOS and PMOS

transistors of the inverter suitably, which was a task within the capability and skill of an ordinary artisan at the time of the alleged invention. (Ex.1002, ¶¶108-109.)

Thus, *Baker* teaches or suggests to a POSITA how to configure an inverter such that its trip point is substantially insensitive to power supply voltage variations, and in view of *Baker* and the knowledge of an ordinary artisan, such a person would have been motivated to configure *Park*'s circuit (e.g., inverter IN1 therein) to have such a feature, especially given *Park*'s objective of "constantly maintaining a back bias voltage with respect to the variation of an external voltage." (Ex 1007, 3:45-57; Ex.1002, ¶110.)

A POSITA would have recognized that it was desirable for the inverter IN1, which serves as a buffer that converts the voltage at node 51 to a digital signal (high or low), to have a stable trip point. (Ex.1002, ¶¶111-113.) This understanding was within the knowledge of a POSITA, as exemplified by *Lovett*.[5] (*Id.*) For example, *Lovett* discloses that "the trip point of … an ideal input buffer

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[5] Petitioner refers to *Lovett* (U.S. Patent 6,278,295) (Ex. 1010) to demonstrate the knowledge of a POSITA at the time of the alleged invention, but does not rely on *Lovett* as part of this invalidity ground. *Int'l Bus. Machines Corp. v. Intellectual Ventures II, LLC*, IPR2015-00089, Paper No. 44 at 15 (Apr. 25, 2016), citing *Cont'l Can Co. USA v. Monsanto Co*., 948 F.2d 1264, 1268–69 (Fed.Cir.1991).

would be utterly stable and would be insensitive to . . .variations in the supply voltage V_{CC}" but that "[a] number of factors … act alone and in combination to cause the trip point to vary from its nominal value of $V_{CC}/2$." (Ex.1010, 1:20-22, 1:26-29; Ex.1002, ¶111.)

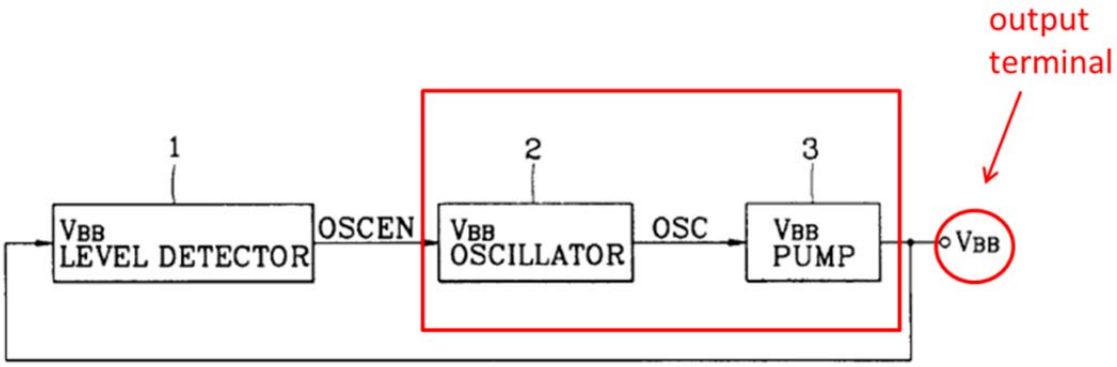
A POSITA would have recognized that it would have been desirable for inverter IN1 to have a stable trip point to ensure that the oscillation enable signal OSCEN is not detrimentally affected by variations in power supply variations. (Ex.1002, ¶¶98-103, 111-113 (*see* hypotheticals).) This is because OSCEN affects the back bias voltage V_{BB} generated by *Park*'s circuit (Ex.1007, 5:26-32) and *Park* touts that its figure 5 level detector circuit provides a more stable back bias voltage V_{BB} even if V_{CC} is varied. (Ex.1002, ¶113.) Thus, a POSITA would have had reason to look to *Baker* to address such issues because, like *Park*, *Baker* is directed to semiconductor devices and explains well-known considerations regarding the design and operation of semiconductor components, like those found in *Park*'s circuit. (*Id.*) Having looked to *Baker*, a POSITA would have been motivated to configure the inverter IN1 in *Park*'s back bias voltage level detector of figure 5 to possess a trip point that is substantially insensitive to power supply voltage variations by sizing transistors in the inverter appropriately in accordance with *Baker*'s teachings, in order to ensure more consistent performance. (*Id.*)

A POSITA would have recognized that implementing such features would have been straightforward and had a reasonable expectation of success in the providing the desired outcome. (*Id.*, ¶114.) Indeed, because *Park* discloses a circuit including inverters and *Baker* discloses details of inverters including details regarding the trip point of inverters, implementing the above modification to *Park*'s circuit would have been merely a combination of known components (*Park*'s figure 5 level detector circuit with *Baker*'s improved inverter), according to known methods (e.g., sizing transistors in the inverters appropriately in accordance with *Baker*'s teachings), to achieve predictable results (e.g., the inverter having a trip point that is substantially insensitive to power supply voltage variations). (*Id.*) *See KSR*, 550 U.S. at 416. Furthermore, as discussed above, implementing this configuration would not have negatively impacted the performance of *Park*'s circuit but rather would have enhanced it. (Ex.1002, ¶114.)

The OSCEN signal in the combined *Park-Baker* system would have been even more insensitive to variations in V_{CC} in view of the modification to *Park*'s inverter IN1 based on *Baker*. (Ex.1002, ¶115.)

d) **"a voltage generator for generating the bias voltage V1 on an output terminal, wherein the voltage generator is responsive to said signal such that the detector circuit and the voltage generator are operable to maintain the bias voltage V1 at a substantially constant value over power supply voltage variations;"**

Park in combination with *Baker* discloses this feature. For instance, *Park* discloses a back bias voltage oscillator 2 and a back bias voltage pump 3 (collectively, "a voltage generator") for generating back bias voltage V_{BB} ("bias voltage V1") on an output terminal. (Ex.1002, ¶¶116-117.) *Park* discloses that when "OSCEN becomes a high electrical potential, … the back bias voltage oscillator 2, as shown in FIG. 1, outputs a pulse OSC." (Ex.1007, 5:26-28; Ex.1002, ¶116.) "OSC is inputted to the back bias voltage pump 3," which in turn generates the back bias voltage V_{BB}. (Ex.1007, 5:40-45.) Further, a POSITA would have understood that the back bias voltage V_{BB} is generated "on an output terminal," because "voltage pump 3" generates the back bias voltage V_{BB}. (*Id*., 5:40-45; Ex.1002, ¶116.) This is confirmed by *Park*, which describes that V_{BB} is an output of the back bias voltage pump 3 as shown in FIG. 1 of *Park* (reproduced below with annotations). (Ex.1002, ¶116.)



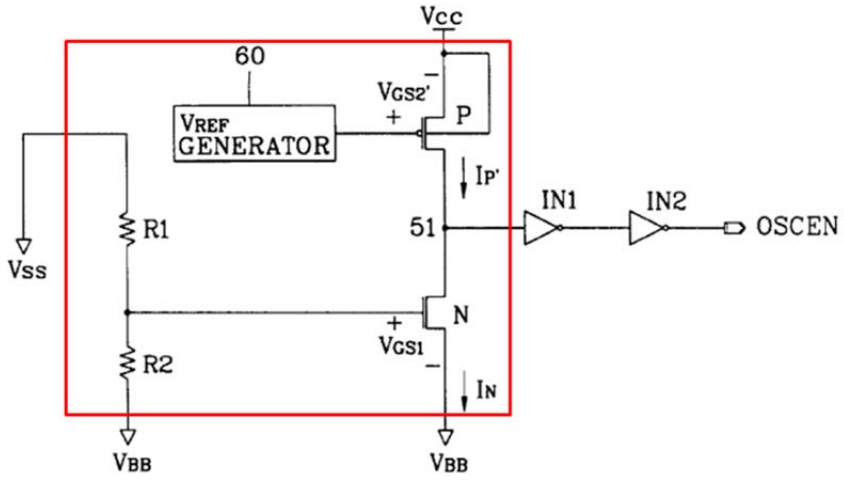
(Ex.1002, ¶116, citing Ex.1007, FIG. 1 (annotated).)

Park further discloses that oscillator 2 and pump 3 (collectively, "voltage generator") are responsive to the OSCEN signal ("said signal"), because when "OSCEN becomes a high electrical potential, … the back bias voltage oscillator 2, as shown in FIG. 1, outputs a pulse OSC." (Ex.1007, 5:26-28; Ex.1002, ¶117.) "OSC is inputted to the back bias voltage pump 3," which in turn generates the back bias voltage V_{BB}. (Ex.1007, 5:40-45.) Moreover, the back bias voltage level detector ("detector circuit") of the combined *Park-Baker* system and *Park*'s oscillator 2 and pump 3 (collectively, "voltage generator") are operable to maintain V_{BB} ("the bias voltage V1") at a substantially constant value over power supply voltage (V_{CC}) variations, for the reasons discussed above at limitations 1(a) and 1(c). (*See supra* Sections IX.C.1(a),(c); Ex.1002, ¶117.)

e) **"wherein the detector circuit comprises: a bias circuit for biasing a first node to a node voltage, the bias circuit receiving the power supply voltage and the bias voltage V1; and"**

Park in combination with *Baker* discloses or suggests this feature. As shown in figure 5 of *Park*, the back bias voltage level detector ("detector circuit") comprises a reference voltage generator 60, PMOS pull-up transistor P, resistor divider R1/R2, and NMOS pull-down transistor N (collectively, "bias circuit") (annotated below in red) for biasing node 51 ("a first node") to a voltage ("node voltage"). (Ex.1002, ¶118.)

FIG. 5



(Ex.1002, ¶118, citing Ex.1007, FIG. 5 (annotated); *see also id.*, 4:66-5:5:39.)

A POSITA would have understood that *Park*'s disclosure of providing a node voltage at node 51 discloses "biasing a first node to a node voltage," as recited in this claim element. (Ex.1002, ¶119.) *Park* discloses that the above-

annotated "biasing circuit" establishes or biases the node 51 to either a high or low electric potential. (*Id.*) For instance, "when the drain current I_N of the NMOS pull-down transistor is increased up to a predetermined level of the current I_P', the node 51 becomes a low electric potential." (Ex.1007, 5:36-39.) Similarly, "when the drain current I_N of the NMOS pull-down transistor is decreased, the current I_P' is also decreased" as a result of which **"**node 51 becomes the high electric potential." (*Id*. at 5:18-39, FIG. 5.)

The above-annotated bias circuit therefore includes PMOS pull-up transistor P and NMOS pull-down transistor N because currents I_N and I_P' flow through these transistors and set the node voltage 51. (Ex.1002, ¶119.) The bias circuit also includes reference voltage generator 60 because it controls current I_P'. (*See supra* Section IX.C.1(b); Ex.1007, 5:5-13 (explaining that I_P' depends on V_{REF}); Ex.1002, 119.) The bias circuit also includes voltage divider R1/R2 because they "bias the NMOS pull-down transistor N." (*Id.*, 5:14-16, FIG. 5; Ex.1002, ¶119.)

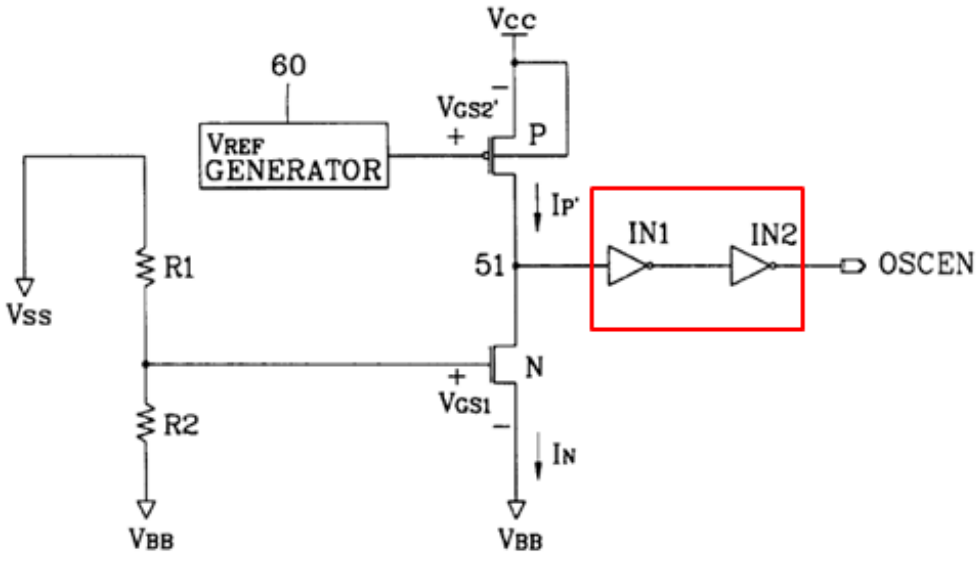
Park further discloses that "the bias circuit receiv[es] the power supply voltage and the bias voltage V1." (Ex.1002, ¶120.) For example, as can be readily seen above in annotated figure 5 of *Park*, the above annotated "bias circuit" receives the external voltage V_{CC} ("power supply voltage") and the back bias voltage V_{BB} ("bias voltage V1"). (*Id.*) In particular, the PMOS pull-up transistor P

is coupled to external voltage V_{CC} and the NMOS pull-down transistor N is coupled to back bias voltage V_{BB}. (*Id.*)

f) **"[wherein the detector circuit comprises:] a sensing circuit for generating said signal in response to the node voltage at the first node;"**

Park in combination with *Baker* discloses or suggests this feature. For instance, the combined *Park-Baker* system discloses that the back bias voltage level detector of figure 5 ("detector circuit") includes inverters IN1 (as modified by *Baker*'s teachings) and IN2 (collectively, "a sensing circuit") for generating the oscillation enable signal OSCEN ("signal") in response to the node voltage at node 51 ("the node voltage at the first node"), as shown in FIG. 5. (Ex.1002, ¶121; *See supra*, Section IX.C.1(c); Ex.1007, 5:24-27, 5:39-41.)

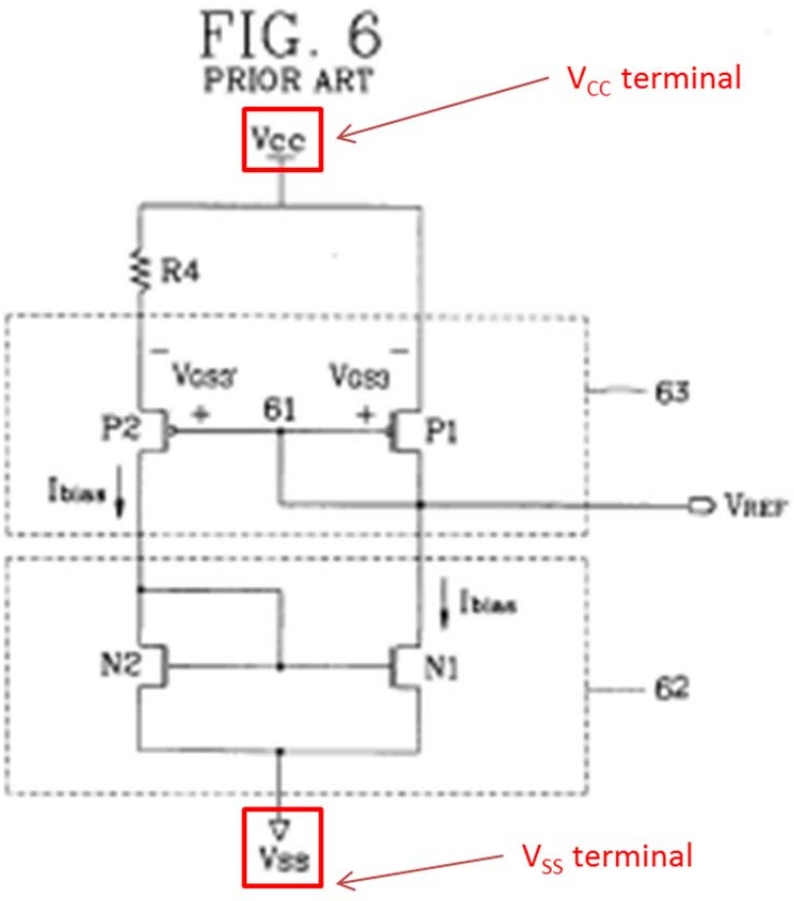
FIG. 5



(Ex.1002, ¶121, citing Ex.1007, FIG. 5 (annotated).)

g) **"wherein the power supply voltage is provided across a power supply terminal and a reference terminal, and"**

Park in combination with *Baker* discloses or suggests this feature. For instance, *Park* discloses that the external voltage V_{CC} ("power supply voltage") is provided across a "V_{CC}" terminal ("a power supply terminal") and a "V_{SS}" terminal ("a reference terminal").



(Ex.1002, ¶122, citing Ex.1007, FIG. 6 (annotated).)

Figure 6 shows the detailed implementation of the reference voltage generator 60 shown in figure 5. (Ex.1002, ¶123; Ex.1007 at 4:46-47.) A POSITA would have understood that V_{CC} in figure 6 corresponds to a "power supply terminal" because it supplies power to the circuit(s) shown in figures 5-6 and furthermore, it was commonplace terminology to label a power supply terminal "V_{CC}." (*Id.*) A POSITA would have similarly understood that Vss in figure 6 corresponds to a "reference terminal." (*Id.*) This understanding would have been consistent with how a POSITA would have understood the "VSS" terminal shown in the '554 patent to be a "reference terminal." For example, a POSITA would have understood from claims 10-13 and figure 5a of the '554 patent that the "reference terminal" refers to VSS. (*Id.*, ¶¶123-124.)

A POSITA would have further understood that the external voltage V_{CC} ("power supply voltage") in *Park* is provided ***across*** the V_{CC} terminal ("power supply terminal") and V_{SS} terminal ("reference terminal") because the external voltage V_{CC} can be measured across the V_{CC} terminal and V_{SS} terminal. (*Id.*, ¶124.) Indeed, as shown in figure 5A of the '554 patent, the same terminals VCC and VSS are terminals across a circuit just like figure 6 in *Park*. (*Id.*)

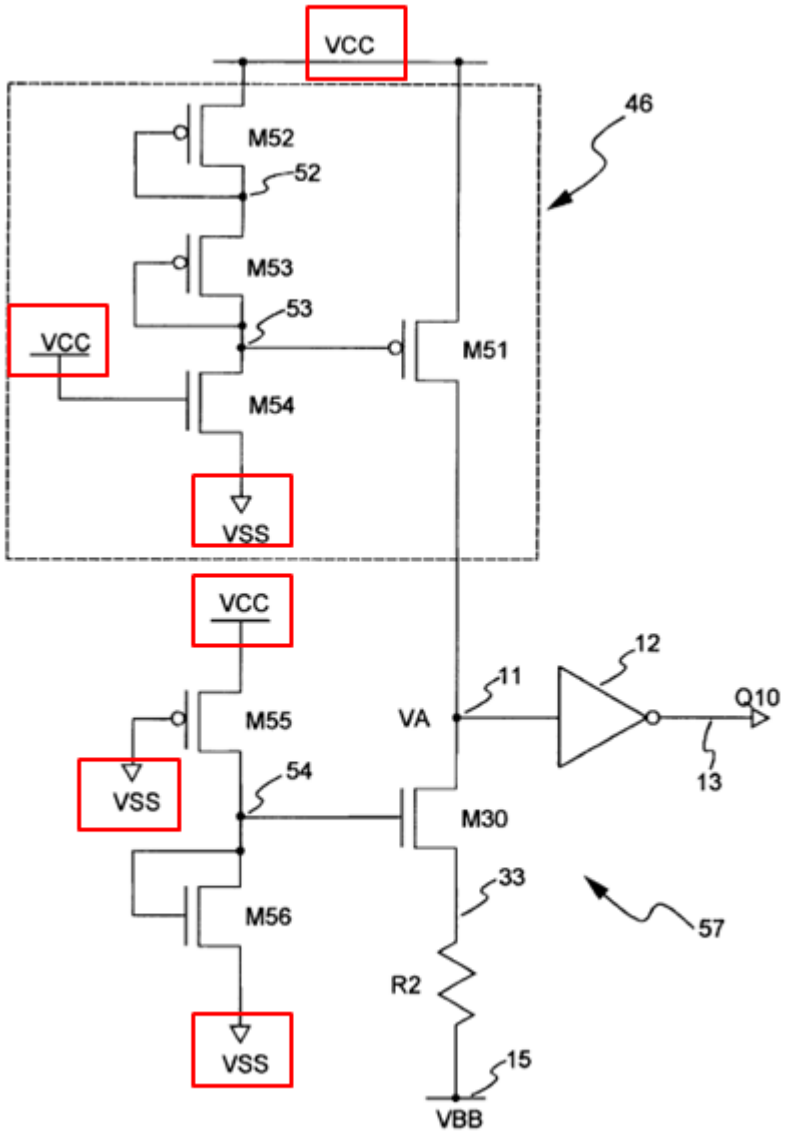


FIG. 5A

(Ex.1002, ¶124, citing Ex.1001, FIG. 5A (annotated).)

a) **"the bias circuit comprises: a current source connected between the power supply terminal and the first node, the current source being substantially insensitive to power supply voltage variations; and"**

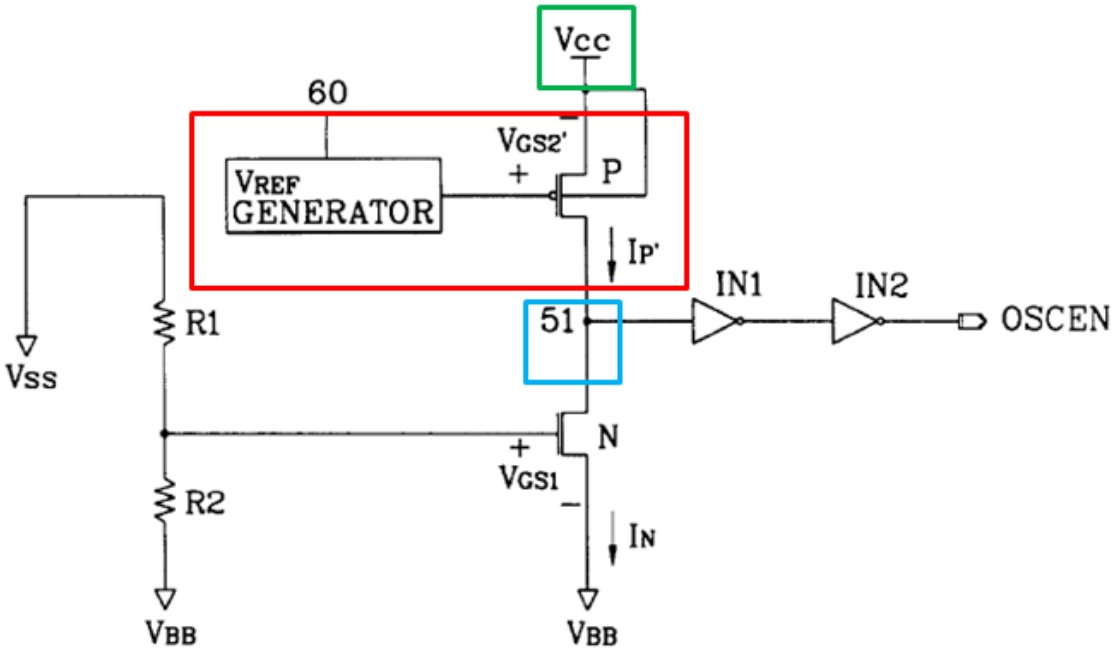
Park in combination with *Baker* discloses or suggests this feature. For instance, as discussed above with respect to claim limitation 1(e), *Park* discloses

that the combination of reference voltage generator 60, PMOS pull-up transistor P, resistor divider R1/R2 and NMOS pull-down transistor N is a "bias circuit." (Ex.1002, ¶125.) In this "bias circuit," reference voltage generator 60 and a PMOS pull-up transistor P constitute a "current source," as claimed because they form an electrical circuit that delivers a current. (Ex.1007, FIG. 5, 4:66-5:13; Ex.1002, ¶125.)

The reference voltage generator 60 works in tandem with the PMOS pull-up transistor P to deliver the current I_P'. (Ex.1007, 4:66-5:10, FIG. 5; Ex.1002, ¶126.) For example, the transistor P delivers the current I_P' based on a voltage provided by the reference voltage generator 60. (Ex.1007, 5:12-14.); Ex.1002, ¶126.) (*See also* analysis above with respect to claim limitations 1(b) and 1(e) (discussing equation for current I_P').)

Park discloses that the reference voltage generator 60 and the PMOS pull-up transistor P (collectively, "current source") are connected between the V_{CC} terminal ("power supply terminal") and node 51 ("first node"). (*Id.*, FIG. 5; Ex.1002, ¶127.) This can be readily seen in the annotated version of *Park*'s figure 5 below.

FIG. 5



(Ex.1002, ¶127, citing Ex.1007, FIG. 5 (annotated).)

Park further discloses that the combination of the reference voltage generator 60 and the PMOS pull-up transistor P (collectively, "current source") is substantially insensitive to the external voltage V_{CC} variations ("power supply voltage variations"). (Ex.1002, ¶128.) In particular, as discussed above with respect to claim limitations 1(a), 1(c), and 1(e), *Park* discloses that the current I_P' output from the transistor P is substantially insensitive to variations in the external voltage V_{CC}. (*See* analysis above with respect to claim limitations 1(a), 1(c), and 1(e); Ex.1002, ¶129.) *Park* discloses that "[s]ince the difference V_{CC} -V_{REF} is

constant, **it is possible to obtain constant current I_P ' irrespective of the external voltage V_{CC}.**" (Ex.1007, 5:12-14, emphasis added.)

b) **"[wherein the bias circuit comprises:] a resistor connected between the first node and the output terminal of the voltage generator circuit;"**

Park in combination with *Baker* discloses or suggests this feature. As discussed above with respect to claim limitation 1(e), *Park* discloses that the combination of the reference voltage generator 60, PMOS pull-up transistor P, resistor divider R1/R2, and NMOS pull-down transistor N corresponds to the claimed "bias circuit." (*Supra* Section IX.C.1.e.) Moreover, as discussed above with respect to claim limitation 1(e), the terminal corresponding to back bias voltage V_{BB} is an "output terminal of the voltage generator circuit." (*Id.*) As illustrated below, in the "bias circuit," NMOS pull-down transistor N ("resistor") (shown below in red) is connected between node 51 ("the first node") (shown below in blue) and the output terminal for the back bias voltage V_{BB} ("the output terminal of the voltage generator circuit") (shown below in green).[6] (Ex.1007, FIG. 5, 5:18-25, 5:33-39; *see also supra* Section IX.C.1(d) regarding output terminal of voltage generator; Ex.1002, ¶130.)

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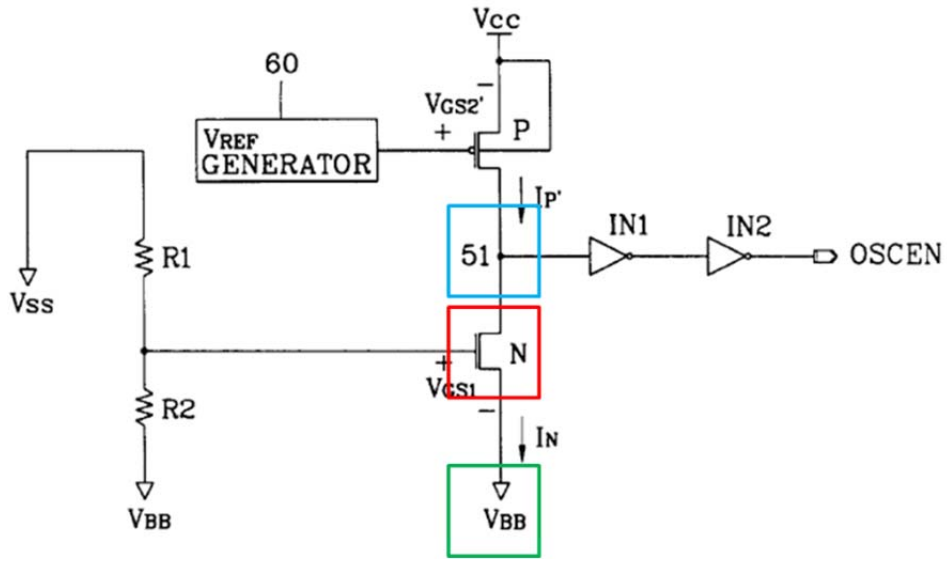
[6] While the phrase "voltage generator circuit" lacks antecedent basis, Petitioner assumes for the purpose of this proceeding that the "voltage generator" recited in limitation 1(d) is intended.

FIG. 5



(Ex.1002, ¶130, citing Ex.1007, FIG. 5 (annotated).)

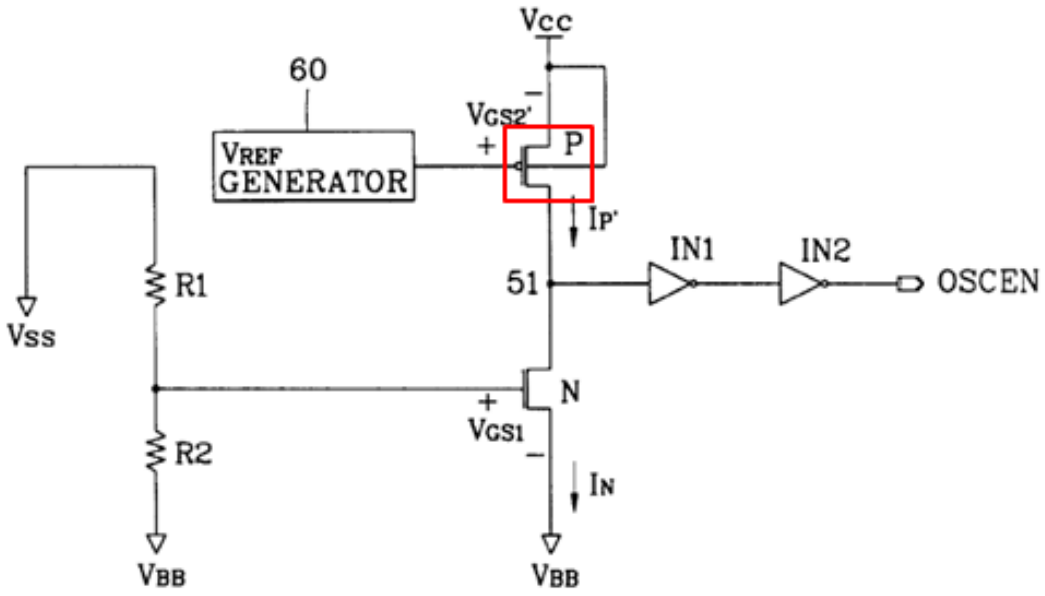
A POSITA would have understood that the NMOS pull-down transistor N is a resistor consistent with the context of the '554 patent. (Ex.1002, ¶131, citing Ex.1001, 3:50-51.)

c) **"wherein the current source comprises a first transistor connected between the power supply terminal and the first node, the first transistor being biased such that a current through the first transistor is substantially insensitive to power supply voltage variations;"**

Park in combination with *Baker* discloses or suggests this feature. In particular, *Park* discloses that the combination of the reference voltage generator 60 and PMOS pull-up transistor P (collectively, "current source") includes the PMOS pull-up transistor P ("first transistor") connected between the V_{CC} terminal

("power supply terminal") and the node 51 ("first node"). (*See* analysis above regarding claim limitations 1(e), 1(g), and 1(h).)

FIG. 5



(Ex.1002, ¶132, citing Ex.1007, FIG. 5 (annotated).)

Park further discloses that the PMOS pull-up transistor P ("first transistor") is biased such that the current I_P' ("current") through the PMOS pull-up transistor P is substantially insensitive to variations in the external voltage V_{CC} ("power supply voltage"). (*See* analysis above with respect to claim limitations 1(h); Ex.1002, ¶133.)

d) **"wherein the gate to source voltage of the first transistor is made substantially insensitive to power supply voltage variations;"**

Park in combination with *Baker* discloses or suggests this feature. For instance, *Park* discloses that the gate to source voltage V_{GS2} of the PMOS pull-up transistor P ("the gate to source voltage of the first transistor") is made substantially insensitive to variations in the external voltage V_{CC} ("power supply voltage"). (Ex.1002, ¶134.) *Park* discloses that the "gate-source voltage V_{GS2} [ ] of the PMOS pull-up transistor P is thus constantly maintained irrespective of the external voltage V_{CC}." (Ex.1007, 4:66-5:4.)

e) **"wherein the first transistor is a field effect transistor biased in the saturation mode;"**

Park in combination with *Baker* discloses or suggests this feature. In particular, a POSITA would have understood that PMOS pull-up transistor P is a "field effect transistor" because a PMOS is a type of MOSFET. (Ex.1002, ¶¶23-26, 135-136; Ex.1007, 4:60.) Moreover, as discussed above at limitation 1(j), the PMOS pull-up transistor P provides a "constant current I_P' irrespective of the external voltage V_{CC}." (Ex.1007, 5:12-14; *see supra* Section IX.C.1(j).) *Park* discloses that the constant current has a value I_P' as follows:

$$I'_P = \frac{\beta}{2}(V'_{GS2} - V_T)^2 = \frac{\beta}{2}(V_{CC} - V_{REF} - V_T)^2$$

(Ex.1007, 5:8-9.)

A POSITA would have understood based on the above equations for a constant current I_P' provided by PMOS pull-up transistor P that transistor P is biased in the saturation mode. (Ex.1002, ¶¶137-138.) For example, *Baker* explains the fundamental principles of CMOS transistors, including the following equation for the drain current of "a MOSFET … **operating in the saturation region**." (Ex.1008, 96 (emphasis added).)[7]

$$I_D = \frac{\beta}{2}(V_{GS} - V_{THN})^2$$

(*Id.*, 96 (equation 5.39, V_{GS} is gate-to-source voltage and V_{THN} is threshold voltage of an NMOS transistor); Ex.1002, ¶138.) A POSITA would have understood that *Baker*'s I_D equation for a MOSFET in the saturation mode is the same form as *Park*'s corresponding I_P' equation (e.g., compare the leftmost equality above regarding I_P' in *Park* ($I'_P = \frac{\beta}{2}(V'_{GS2} - V_T)^2$) with *Baker*'s I_D equation). (Ex.1002, ¶138.) While *Baker*'s I_D equation is for an NMOS, a POSITA would have known that the same equation is applicable for a PMOS transistor except that V_{THN} is replaced by V_{THP} (the threshold voltage of the PMOS) and the polarity of V_{GS} is

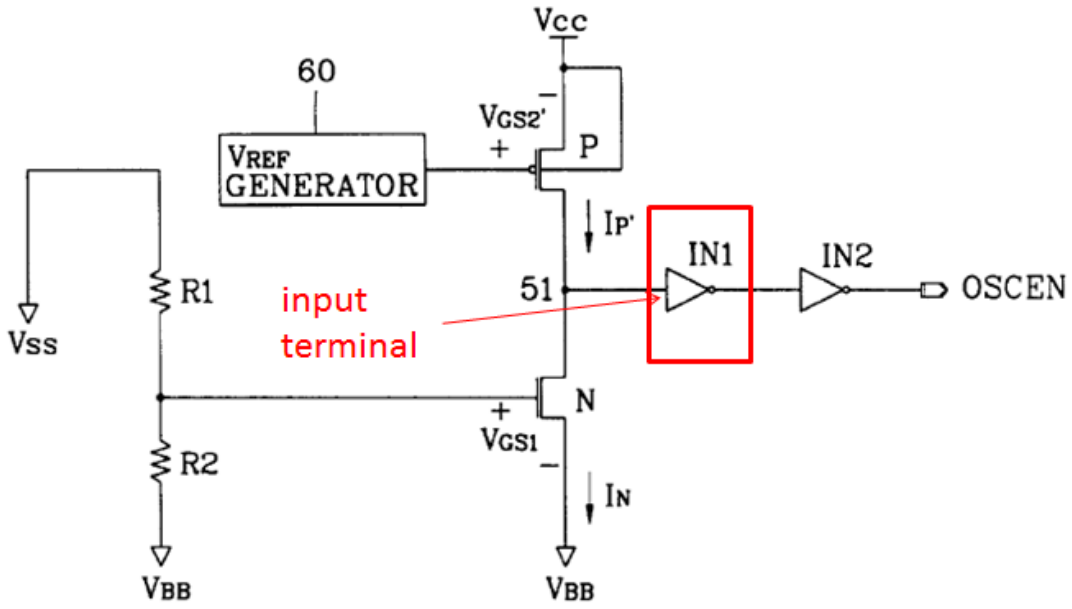
[7] As *Baker* describes, a MOS transistor has various modes of operation including a cutoff mode, a triode mode, and a saturation mode. (Ex. 1008, 94, 96, 113; Ex. 1002, ¶138.)

reversed. (*Id.*) Thus, *Park* discloses that its PMOS pull-up transistor P is biased in the saturation mode. (*Id.*)

f) **"wherein the sensing circuit comprises an inverter having an input terminal connected to the first node, the inverter possessing a trip point which is substantially insensitive to power supply voltage variations, whereby the bias voltage V1 is obtained when the node voltage and the trip point of the inverter are substantially the same."**

Park in combination with *Baker* discloses or suggests this feature. For example, the combined *Park-Baker* system discloses that the inverter IN1, as modified by *Baker*'s teachings, and inverter IN2 (collectively, "a sensing circuit") comprise an inverter IN1 ("inverter") having an input terminal connected to the node 51 ("first node"). (*See supra* Section IX.C.1(f); annotated figure below; Ex.1002, ¶139.)

FIG. 5



(Ex.1002, ¶139, citing Ex.1007, FIG. 5 (annotated to show inverter IN1 and its input terminal).)

Moreover, as discussed above with respect to claim limitation 1(c), a POSITA would have been motivated to configure the inverter IN1 in *Park*'s back bias voltage level detector of figure 5 to possess a trip point that is substantially insensitive to power supply voltage variations by sizing transistors in the inverter appropriately in accordance with *Baker*'s teachings. (*See supra* Section IX.C.1(c); Ex.1002, ¶140.) Therefore, the combined *Park-Baker* system discloses an "inverter [IN1] possessing a trip point which is substantially insensitive to power supply voltage variations." (Ex.1002, ¶140.)

Park also discloses "whereby the bias voltage V1 is obtained when the node voltage and the trip point of the inverter are substantially the same." For instance, *Park* discloses that once the value of VBB decreases (i.e., the absolute value of VBB increases), "the oscillation enable signal OSCEN becomes a low electric potential … so that the back bias voltage pump 3 does not pump the negative electric charge to the substrate." (Ex.1007, 5:33-44.) But as VBB starts to increase, "the gate-source voltage VGS1 of the NMOS pull-down transistor N is decreased … node 51 becomes the high electric potential" as a result of which "OSCEN becomes a high electric potential." (*Id*., 5:18-28.) At that time, voltage pump 3 applies a "negative electric potential … to the substrate by a pumping

operation" to generate VBB. (*Id*., 5:26-32.) That is, VBB is generated when OSCEN becomes a high electric potential from a low electric potential. A POSITA would have understood that OSCEN would switch from low to high when the voltage at node 51 ("the node voltage") reaches the trip point of inverter IN1 thereby tripping/switching IN1's output from high to low. (Ex.1002 at ¶141.) That is, VBB in the combined *Park-Baker* circuit is generated "when the node voltage [of node 51] and the trip point of the inverter [IN1] are substantially the same."

2. Claim 2

a) **"The circuit of claim 1 wherein the inverter comprises: a pull up transistor; and a pull down transistor,"**

Park in combination with *Baker* discloses or suggests this feature. In particular, while *Park* does not disclose internal details regarding the implementation of inverter IN1 in the back bias voltage level detector of figure 5, *Baker* discloses it was well known prior to the alleged invention to implement an inverter using a pull up transistor and a pull down transistor, like that shown in figure 11.1 (reproduced below with annotations). (Ex.1002, ¶¶142-143.)

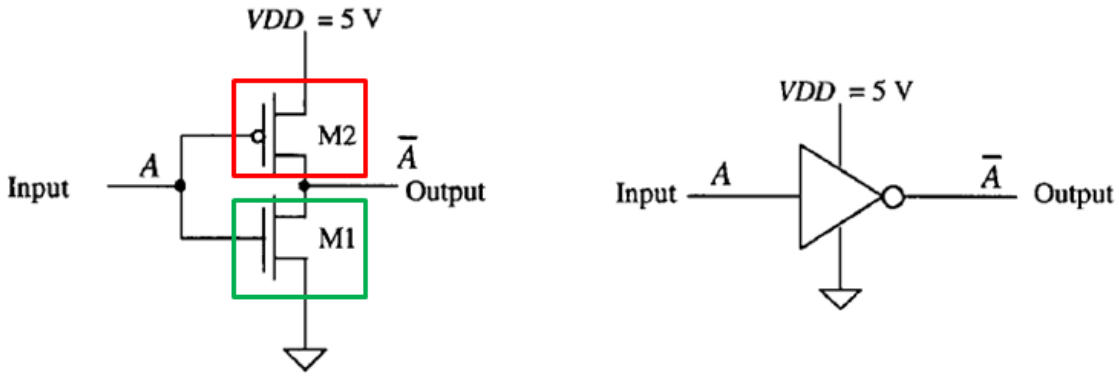


Figure 11.1 The CMOS inverter, schematic, and logic symbol.

(Ex.1002, ¶143, citing Ex.1008, 201 (FIG. 11.1, annotated to show pull up transistor M2 in red and pull down transistor M1 in green).)

Baker's transistors M2 and M1 of figure 11.1 are a PMOS "pull up transistor" and an NMOS "pull down transistor," respectively. (Ex.1008, 151, 201), FIG. 11.1; Ex.1002, ¶144.) Indeed, *Baker*'s PMOS pull up transistor M2 and NMOS pull down transistor M1 are arranged in the same configuration as the PMOS pull-up transistor M48 and NMOS pull-down transistor M49 shown in FIG. 4B of the '554 patent:

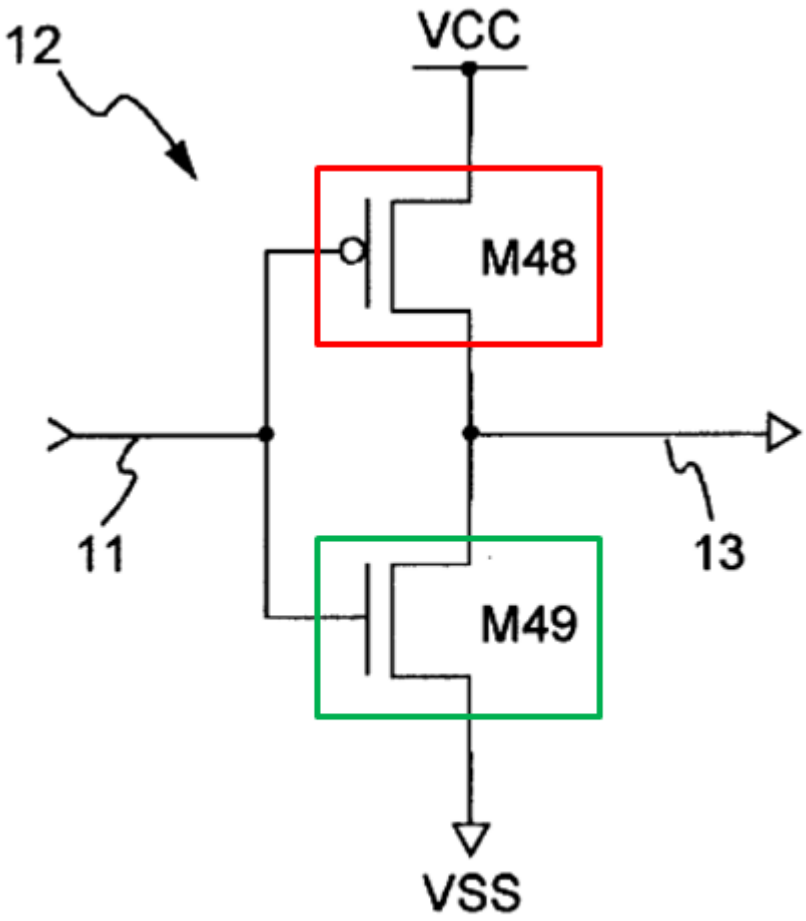


FIG. 4B

(Ex.1002, ¶145, citing Ex.1001, FIG. 4B.)

It would have been obvious to a POSITA in view of *Baker* to implement *Park*'s inverter IN1 ("the inverter") to comprise a pull up transistor, like *Baker*'s pull up transistor M2, and a pull down transistor, like *Baker*'s pull down transistor M1, to enable *Park*'s circuit to be configured and implemented according to known configurations and circuitry designs, like those disclosed by *Baker*. (Ex.1002, ¶146.) Indeed, a POSITA would have been motivated to implement *Park*'s

inverter IN1 in this manner because the implementation taught at figure 11.1 of *Baker* was a well-known, standard CMOS implementation of an inverter. (Ex.1008, 201; Ex.1002, ¶146.) Because this was a standard CMOS implementation, it was well within the capability of an ordinary artisan, who would have had a reasonable expectation of success in the result of the outcome of this implementation. (Ex.1002, ¶146.) Indeed, such an implementation of the inverter IN1 would have been merely a combination of known components (e.g., inverter as in *Park*, implemented using *Baker*'s pull up and pull down transistors), according to known methods (*Baker* teaches how to implement the CMOS inverter as described above), to achieve a predictable outcome (*Baker* confirms that logic inversion as required by *Park*'s inverter IN1 will be achieved by the above implementation). (*Id.*) *See KSR*, 550 U.S. at 416.

b) **"wherein the pull down transistor size is substantially larger than the pull up transistor size."**

Park in combination with *Baker* discloses or suggests this feature. In particular, as discussed above at limitation 1(c), in order for the inverter IN1 to have an inverter trip point that is substantially insensitive to variations in the external voltage V_{CC}, a POSITA would have been motivated and had the capability to configure the size of an NMOS transistor of the inverter IN1 much larger than the size of the PMOS transistor of the inverter IN1 in the combined *Park-Baker* system. (*See supra* Section IX.C.1(c); Ex.1002, ¶¶147-148.) As discussed above

with respect to limitation 2(a), the combined *Park-Baker* system would have included an inverter IN1 with a PMOS pull up transistor M2 ("pull-up transistor") and an NMOS pull down transistor M1 ("pull-down transistor"). (*See supra* Section IX.C.2(a); Ex.1002, ¶148.)

Therefore, given the above-discussed configuration of inverter IN1 in the combined *Park-Baker* system and the reasons discussed above for claim limitation 1(c), a POSITA would have been motivated to size the NMOS pull down transistor M1 much larger than the PMOS pull up transistor M2 in the combined *Park-Baker* system. (*See supra* Section IX.C.1(c); Ex.1002, ¶149.)

3. Claim 3

a) **"The circuit of claim 1 wherein the first transistor is a PMOS transistor having its gate biased to a voltage equal to the power supply voltage minus a predesignated voltage."**

Park in combination with *Baker* discloses or suggests this feature. For instance, *Park* discloses the transistor P ("first transistor") is a PMOS pull-up transistor P ("PMOS transistor.") (Ex.1007, 5:2, FIG. 5; *see supra* Section IX.C.1(j); Ex.1002, ¶150.)

Park further discloses that the "reference voltage V_{REF} … is connected to the gate of … transistor P." (Ex.1007, 4:66-5:1.) The reference voltage V_{REF} is set to the power supply voltage V_{CC} minus a constant voltage ("predesignated voltage"), because "the difference $V_{CC} - V_{REF}$" is a constant. (*Id*., 5:11; Ex.1002, ¶151.) So,

a POSITA would have understood that if $V_{CC} - V_{REF}$ = constant K, then V_{REF} = V_{CC} – constant K. (Ex.1002, ¶151.) Accordingly, transistor P ("first transistor") has its gate biased to V_{REF}, which is set to a voltage equal to V_{CC} ("power supply voltage") minus a constant voltage K ("predesignated voltage"). (*Id.*)

4. Claim 14

a) **"The circuit of claim 1 wherein the resistor is implemented using a MOS transistor, or a strip of polysilicon, or a strip of diffusion."**

Park in combination with *Baker* discloses or suggests this feature. For instance, as discussed above at limitation 1(i), *Park* discloses that the NMOS pull-down transistor N ("resistor") is implemented using a NMOS transistor N ("a MOS transistor"). (*See supra* Section IX.C.1(i); Ex.1002, ¶152.)

5. Claim 15

a) **"A method for providing a bias voltage V1 which is substantially insensitive to variations of a power supply voltage powering a circuit, the method comprising:"**

To the extent the preamble is limiting, *Park* discloses this feature. As discussed above with respect to limitation 1(a), *Park* discloses a circuit for providing a back bias voltage V_{BB} ("bias voltage V1") which is substantially insensitive to variations of an external voltage V_{CC} ("power supply voltage powering the circuit"). (*See supra* Section IX.C.1(a); Ex.1002, ¶153.) *Park* also discloses how that circuit functions, and thus discloses the "method" of claim 15 and the corresponding method steps as discussed below. (Ex.1007, 4:58-5:45;

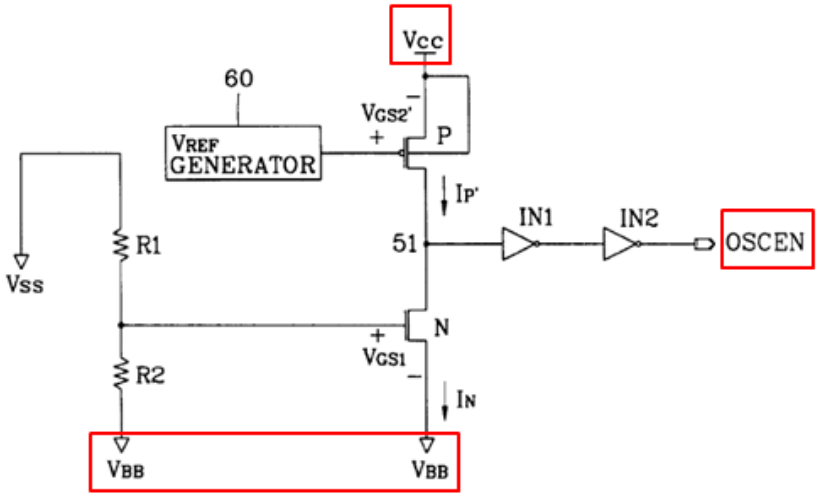
Ex.1002, ¶153.) (*See also* citations and analysis below for the remaining limitations of this claim.)

b) **"(A) generating on an output terminal of a detector circuit a signal from the power supply voltage and the bias voltage V1, wherein said signal is substantially insensitive to variations in the power supply voltage while being responsive to the bias voltage V1; and"**

Park in combination with *Baker* discloses or suggests this feature. For instance, as discussed above with respect to limitation 1(b), *Park* discloses generating an oscillation enable signal OSCEN ("generating … a signal") from V_{CC} ("power supply voltage") and V_{BB} ("bias voltage V1"), and as discussed above at limitation 1(c), *Park* in combination with *Baker* discloses or suggests that signal OSCEN ("said signal") is substantially insensitive to variations in V_{CC} ("power supply voltage") while being responsive to V_{BB} ("bias voltage V1"). (*See supra* Section IX.C.1(b)-(c); Ex.1002, ¶154.)

As discussed above with respect to limitation 1(b), *Park* discloses that signal OSCEN ("a signal") is generated by a back bias voltage level detector ("detector circuit") shown in figure 5. (Ex.1002, ¶155.)

FIG. 5



(Ex.1002, ¶155, citing Ex.1007, FIG. 5 (annotated), 4:44-45).)

A POSITA would have understood, based on *Park*'s figure 5 (above), that *Park* discloses generating signal OSCEN "on an output terminal" of the back bias voltage level detector ("detector circuit") shown in figure 5. (Ex.1002, ¶156.)

c) **"(B) generating the bias voltage V1 on an output terminal of a voltage generator, wherein the voltage generator is responsive to said signal such that the detector circuit and the voltage generator are operable to maintain the bias voltage V1 at a substantially constant value over power supply voltage variations;"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above for limitation 1(d). (*See supra* Section IX.C.1(d); Ex.1002, ¶157.)

d) **"wherein step (A) comprises: (C) biasing a first node to a node voltage by a bias circuit, the bias circuit receiving the power supply voltage and the bias voltage V1; and"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(e). (*See supra* Section IX.C.1(e); Ex.1002, ¶158.)

e) **"[wherein step (A) comprises:] (D) generating said signal in response to the node voltage at the first node by a sensing circuit;"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(f). (*See supra* Section IX.C.1(f); Ex.1002, ¶159.)

f) **"the method further comprising: (E) preventing the bias voltage V1 from exceeding a predesignated voltage;"**

Park in combination with *Baker* discloses or suggests this feature. As discussed above with respect to limitation 1(m), when V_{BB} starts to increase, "the gate-source voltage V_{GS1} of the NMOS pull-down transistor N is decreased … node 51 becomes the high electric potential," as a result of which "OSCEN becomes a high electric potential." (Ex.1007, 5:18-28.) At that time, voltage pump 3 applies a "negative electric potential … to the substrate by a pumping operation" to generate V_{BB}. (*Id*., 5:26-32.) A POSITA would have understood that the back bias voltage V_{BB} at which "node 51 becomes the high electric potential" is at or near the maximum voltage to which V_{BB} can rise, because once V_{BB} reaches

the voltage at which node 51 becomes a "high" voltage, OSCEN becomes a high electric potential and voltage pump 3 begins to start pumping negative charge to the substrate to decrease V_{BB}. (*See* analysis for claim limitation 1(m).) (Ex.1002, ¶160-161.) Accordingly, the circuit of figure 5 in *Park* prevents V_{BB} ("the bias voltage V1") from exceeding a certain maximum value ("exceeding a predesignated voltage"). (*Id.*)

g) **"wherein: the power supply voltage is provided across a power supply terminal and a reference terminal, and"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(g). (*See supra* Section IX.C.1(g); Ex.1002, ¶162.)

h) **"the bias circuit includes a current source which is substantially insensitive to power supply voltage variations, the current source being connected between the power supply terminal and the first node, and"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(h). (*See supra* Section IX.C.1(h); Ex.1002, ¶163.)

i) **"[the bias circuit] also includes a resistor connected between the first node and the output terminal of the voltage generator;"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(i). (*See supra* Section IX.C.1(i); Ex.1002, ¶164.)

j) **"wherein the current source includes a first transistor biased such that a current through the first transistor is substantially insensitive to power supply voltage variations, the first transistor being connected between the power supply terminal and the first node;"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(j). (*See supra* Section IX.C.1(j); Ex.1002, ¶165.)

k) **"wherein the gate to source voltage of the first transistor is made substantially insensitive to power supply voltage variations and"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(k). (*See supra* Section IX.C.1(k); Ex.1002, ¶166.)

l) **"the first transistor is a field effect transistor biased in the saturation mode;"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(l). (*See supra* Section IX.C.1(l); Ex.1002, ¶167.)

m) **"wherein the sensing circuit includes an inverter having an input terminal connected to the first node, the inverter possessing a trip point which is substantially insensitive to power supply voltage variations, whereby the bias voltage V1 is obtained when the node voltage and the trip point of the inverter are substantially the same."**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitation 1(m). (*See supra* Section IX.C.1(m); Ex.1002, ¶168.) (*See supra* Section IX.C.1(m).)

6. Claim 16

a) **"The method of claim 15 wherein the inverter includes a pull up transistor and a pull down transistor, the pull down transistor size being substantially larger than the pull up transistor size."**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at claim 2. (*See supra* Section IX.C.2; Ex.1002, ¶169.)

7. Claim 30

a) **"An integrated circuit comprising a semiconductor region and also comprising a circuit C1 for providing a bias voltage V1 to bias the semiconductor region such that the bias voltage V1 is substantially insensitive to variations of a power supply voltage powering the circuit C1, the circuit C1 comprising:"**

To the extent the preamble is limiting, *Park* discloses this feature. As discussed above at limitation 1(a), *Park* discloses a circuit (e.g., "circuit C1") for providing a back bias voltage V_{BB} ("bias voltage V1") which is substantially insensitive to variations of an external voltage V_{CC} ("power supply voltage powering the circuit C1"). (*See supra* Section IX.C.1(a); Ex.1002, ¶170.)

Limitation 30(a) requires the following additional elements:

(i) an "integrated circuit" comprising the circuit C1;

(ii) the integrated circuit comprising a semiconductor region; and

(iii) that the bias voltage V1 provided by the circuit C1 biases the semiconductor region.

Park discloses each of these additional limitations. First, with respect to limitations (ii) and (iii) above, a POSITA would have understood that *Park* discloses a substrate ("semiconductor region") to which a back bias voltage V_{BB} is applied. (Ex.1007, 5:29-32 (describing negative electric potential applied to the substrate by a pumping operation from voltage pump 3, where the negative electric potential corresponds to the back bias voltage V_{BB} output from the pump 3); *see also id*., 5:40-44; Ex.1002, ¶¶171-172.) As such, *Park* discloses that the bias voltage V1 provided by the voltage pump 3 (part of *Park*'s components constituting the "circuit C1") biases the substrate ("semiconductor region"). (Ex.1002, ¶172.)

As for limitation (i) above, a POSITA would have understood that *Park* discloses an "integrated circuit" comprising the substrate ("semiconductor substrate") along with the back bias voltage level detector, voltage oscillator 2, and voltage pump 3 (collectively, "circuit C1"), as required by limitation 1(a). (Ex.1002, ¶173.) For example, a POSITA would have understood that an integrated circuit is a circuit formed on semiconductor material such as the substrate of *Park*. (*Id.*) Accordingly, because *Park* discloses a substrate to which the voltage pump 3 applies the back bias voltage V_{BB}, a POSITA would have understood that *Park* discloses an integrated circuit. (*Id.*)

b) **"a bias voltage terminal for providing the bias voltage V1;"**

Park discloses this feature, for the reasons discussed above at limitation 1(d). (*See supra* Section IX.C.1(d); Ex.1002, ¶174.) In particular, as discussed above with respect to limitation 1(d), *Park* discloses that the combination of back bias voltage oscillator 2 and back bias voltage pump 3 generates the back bias voltage V_{BB} ("bias voltage V1") on an output terminal ("bias voltage terminal"). (Ex.1002, ¶174.)

c) **"a voltage generator for generating the bias voltage V1 on the bias voltage terminal;"**

Park discloses this feature, for the reasons discussed above with respect to limitations 1(d) and 30(b). (*See supra* Sections IX.C.1(d), IX.C.7(b); Ex.1002, ¶175.)

d) **"a power supply terminal for receiving the power supply voltage;"**

Park discloses this feature, for the reasons discussed above with respect to limitation 1(g). (*See supra* Section IX.C.1(g); Ex.1002, ¶176.) In particular, as shown above with respect to limitation 1(g), the V_{CC} terminal ("power supply terminal") receives the external voltage V_{CC} ("power supply voltage"). (Ex.1002, ¶176.)

e) **"a node;"**

Park discloses this feature, for the reasons discussed above with respect to limitation 1(e). (*See supra* Section IX.C.1(e); Ex.1002, ¶177.) In particular, as discussed at limitation 1(e), *Park* discloses a node 51 ("node"). (Ex.1002, ¶177.)

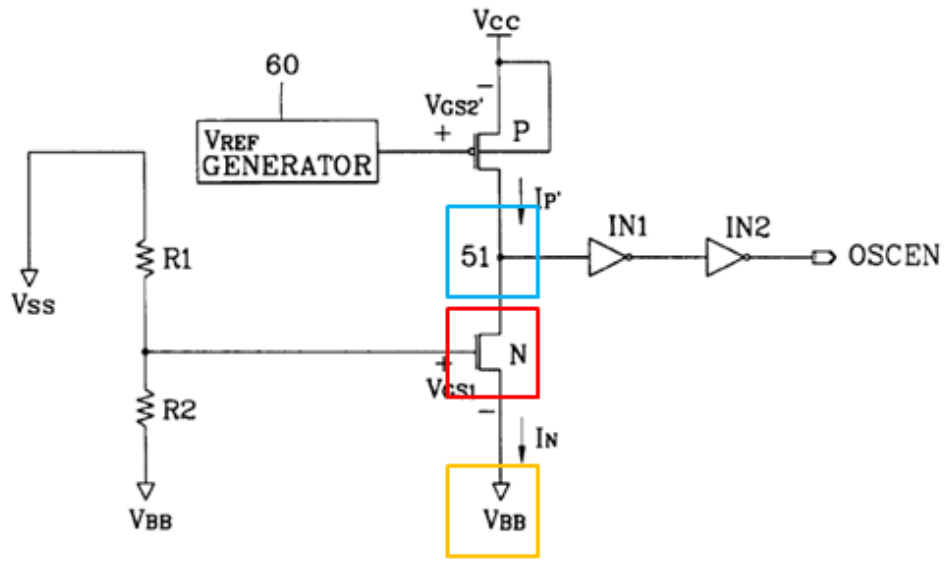
f) **"a current source connected between the power supply terminal and the node, for providing current substantially insensitive to the power supply voltage variations;"**

Park discloses this feature, for the reasons discussed above at limitation 1(h). (*See supra* Section IX.C.1(h); Ex.1002, ¶178.)

g) **"a first circuit for providing a conductive path between the node and the bias voltage terminal, such that the current source and the first circuit bias the node to a voltage which is a function of the bias voltage V1; and"**

Park discloses this feature. (Ex.1002, ¶¶179-183.) Figure 5 of *Park* discloses an NMOS pull-down transistor N ("first circuit") for providing a conductive path between node 51 ("node") and the V_{BB} node, as shown below. (*Id*., ¶180.)

FIG. 5



(Ex.1002, ¶180, citing Ex.1007, FIG. 5 (annotated to show NMOS pull-down transistor N in red, node 51 in blue, and back bias voltage V_{BB} in orange).)

Park further discloses that the claimed first circuit provides a conductive path between the node and the bias voltage terminal "such that the current source and the first circuit bias the node to a voltage which is a function of the bias voltage V1." For example, as discussed above with respect to claim limitations 1(b) and 1(c), the voltage at node 51 ("node") is affected by both (i) current I_P', which is generated by reference voltage generator 60 and PMOS pull-up transistor P (collectively, "current source") to flow into node 51, and (ii) current I_N, which flows across the source and drain terminals of NMOS pull-down transistor N ("a first circuit") and out of node 51. (*See supra* Sections IX.C.1(b)-(c); Ex.1002,

¶181.) Thus, *Park*'s voltage generator 60 and PMOS pull-up transistor P (collectively, "current source") and NMOS pull-down transistor N ("first circuit") affect the voltage of node 51 ("such that the current source and the first circuit bias the node to a voltage"). (Ex.1002, ¶181.) For example, as discussed above, *Park* discloses that "when the absolute value of the back bias voltage V_{BB} is increased" sufficiently, "the node 51 becomes a low electric potential." (Ex.1007, 5:33-39; *see also supra* Section IX.C.1(b); Ex.1002, ¶181.)

Park further discloses that "[w]hen the gate-source voltage V_{GS1} of the NMOS pull-down transistor N is decreased, … node 51 becomes the high electric potential." (*Id.*, 5:18-25.) Because a decrease in the gate-source voltage V_{GS1} occurs when there is an increase in the back bias voltage V_{BB} (due to back bias voltage V_{BB} being the voltage at the source of NMOS pull-down transistor N), *Park* thus discloses that an increase in the back bias voltage V_{BB} (i.e., moving it closer to 0V) results in a decrease in the voltage at node 51. (Ex.1002, ¶182.)

Therefore, a decrease in back bias voltage V_{BB} (i.e., an increase in its magnitude, because it is negative, *see* Ex.1007, FIG. 8) or an increase in back bias voltage V_{BB} result in node 51 becoming a "low electric potential" or "high electric potential," respectively. (Ex.1002, ¶183.) As such, the voltage to which node 51 ("the node") is biased is a function of the back bias voltage V_{BB} ("bias voltage V1"), as claimed. (*Id.*)

h) **"an inverter for inverting a voltage signal on the node, the inverter possessing a trip point which is substantially insensitive to the power supply voltage variations,"**

Park in combination with *Baker* discloses this feature, for the reasons discussed above at limitations 1(m) and 1(c). (*See supra* Section IX.C.1(m); IX.C.1(c); Ex.1002, ¶184.)

i) **"wherein the voltage generator turns on and off in response to an output signal of the inverter."**

Park in combination with *Baker* discloses this feature. (Ex.1002, ¶185-187.) For example, *Park* discloses that the back bias voltage oscillator 2 and back bias voltage pump 3 (collectively, "voltage generator") turn on and off in response to an output signal of the inverter IN1 ("inverter"). (*Id.*)

In particular, *Park* discloses that the inverter IN2 outputs an oscillation enable signal depending upon the signal ("output signal") output from inverter IN1. (Ex.1002, ¶186; Ex.1007, FIG. 5.) Further, in response to the inverter IN2 outputting an oscillation enable signal OSCEN having a **high** electric potential, the voltage oscillator 2 outputs a pulse signal whereas in response to the inverter IN2 outputting an oscillation enable signal OSCEN having a **low** electric potential, the voltage oscillator does not output a pulse signal. (Ex.1007, 5:26-44, FIG. 5; Ex.1002, ¶186.) Consequently, the voltage pump 3 either applies or does not apply the negative electric potential to the substrate in response to the presence or

absence of a pulse signal from the voltage oscillator 2. (Ex.1007, 5:26-44, FIG. 5; Ex.1002, ¶186.)

A POSITA would have understood based on the disclosure of *Park* that if the voltage oscillator 2 is not outputting a pulse signal and consequently the voltage pump 3 is not applying the negative electrical potential to the substrate, then they are effectively turned off. (Ex.1002, ¶187.) On the other hand, if the voltage oscillator 2 is outputting a pulse signal and consequently the voltage pump 3 is applying the negative electrical potential to the substrate, then they are effectively turned on. (*Id.*) Therefore, *Park* discloses that the back bias voltage oscillator 2 and back bias voltage pump 3 (collectively, "voltage generator") turn on and off in response to an output signal of the inverter IN1 ("inverter"). (*Id.*)

8. Claim 31

a) **"The integrated circuit of claim 30 wherein the inverter comprises: a first transistor connected to a ground voltage terminal and to an output of the inverter; and a second transistor connected to the output of the inverter in series with the first transistor,"**

Park in combination with *Baker* discloses or suggests this feature. For example, as discussed above with respect to limitation 2(a) above, the combined *Park-Baker* system discloses that the inverter IN1 ("inverter') includes an NMOS transistor M1 ("first transistor") and a PMOS transistor M2 ("second transistor"). (*See supra* Section IX.C.2; Ex.1002, ¶188.)

In particular, while *Park* does not disclose internal details regarding the implementation of inverter IN1 in the back bias voltage level detector of figure 5, *Baker* discloses it was known prior to the alleged invention to configure an inverter using a PMOS transistor M2 and a NMOS transistor M1 having features like those recited in this claim, as shown in figure 11.1. (Ex.1002, ¶189.)

For example, as shown in figure 11.1 of *Baker* (reproduced below with annotations), the combined *Park-Baker* system discloses that the inverter IN1 ("inverter') includes an NMOS transistor M1 ("a first transistor") connected to ground ("a ground voltage terminal") and to the node located at the output of the inverter IN1 ("an output of the inverter"), and further includes a PMOS transistor M2 ("second transistor") connected to the node located at the output of the inverter IN1 ("the output of the inverter") in series with transistor M1 ("the first transistor"). (Ex.1002, ¶190.)

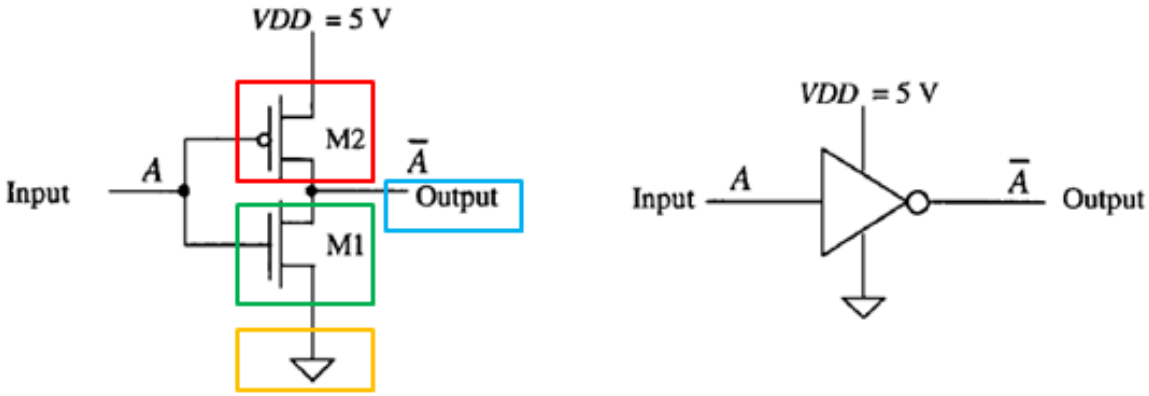


Figure 11.1 The CMOS inverter, schematic, and logic symbol.

(Ex.1002, ¶190, citing Ex.1008, 201 (FIG. 11.1, annotated to show transistor M1 in green, transistor M2 in red, ground node in orange, and output of the inverter in blue).)

Baker discloses that transistor M1 ("first transistor") is connected to ground ("a ground voltage terminal") because figure 11.1 (above) shows the source terminal of transistor connected to a node designated by an inverted triangle, which a POSITA would have understood to be the circuit symbol for ground. (Ex.1008, 201 (FIG. 11.1); Ex.1002, ¶191.) Transistor M1 ("first transistor") is also connected at its drain terminal to a node labeled "Output" in figure 11.1 ("an output of the inverter"). (Ex.1002, ¶191.)

Baker further discloses at figure 11.1 that transistor M2 ("second transistor") is also connected at its drain terminal to the node labeled "Output" ("the output of the inverter"). (Ex.1002, ¶192.) The drain terminal of the transistor M2 is also connected to the drain terminal of transistor M1, a configuration that a POSITA would have understood to be a series coupling of transistors M1 and M2 ("second transistor connected … in series with the first transistor"). (*Id.*)

For reasons similar to those discussed above with respect to limitation 2(a), it would have been obvious to a POSITA in view of *Baker* to implement *Park*'s inverter IN1 ("the inverter") to comprise *Baker*'s NMOS transistor M1 ("first

transistor") and PMOS transistor M2 ("second transistor"). (*See supra*, Section IX.C.2(a); Ex.1002, ¶193.)

b) **"wherein the first transistor size is substantially greater than the second transistor size."**

Park in combination with *Baker* discloses or suggests this feature. (Ex.1002, ¶194.) For example, the combined *Park-Baker* system discloses that the size of transistor M1 ("first transistor size") is substantially greater than the size of transistor M2 ("second transistor size"), for the reasons discussed above at limitation 2(b). (*See supra* Section IX.C.2(b); Ex.1008, 201 (FIG. 11.1); Ex.1002, ¶194.)

9. Claim 36

a) **"The integrated circuit of claim 30 wherein the current source comprises a transistor connected between the power supply terminal and the node,"**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitations 1(j) and 15(j). (*See supra* Sections IX.C.1(j), IX.C.5(j); Ex.1002, ¶195.)

b) **"the transistor being a field effect transistor biased in the saturation mode."**

Park in combination with *Baker* discloses or suggests this feature, for the reasons discussed above at limitations 1(l) and 15(l). (*See supra* Sections IX.C.1(l), IX.C.5(l); Ex.1002, ¶196.)

D. Ground 4: *Park, Baker,* and *Tsukada* Render Obvious Claims 32-34

1. Claim 32

a) **"The integrated circuit of claim 30 further comprising a memory wherein the bias voltage V1 is applied to a silicon substrate region in which memory cells reside."**

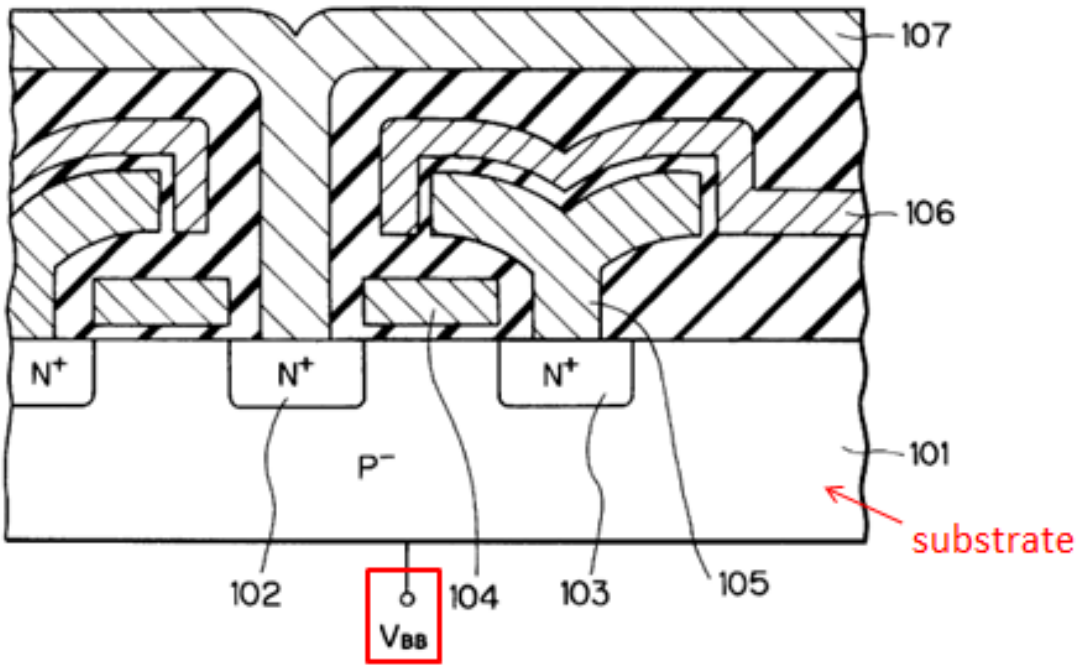
Park in combination with *Baker* and *Tsukada* discloses or suggests this feature. While the combined *Park-Baker* system discloses an integrated circuit comprising a substrate to which a back bias voltage V_{BB} ("bias voltage V1") is applied as discussed above with respect to claim limitation 30(a), the combined *Park-Baker* system does not disclose the integrated circuit comprises a memory wherein the back bias voltage V_{BB} ("bias voltage V1") is applied to a silicon substrate region in which memory cells reside. (See *supra* Section IX.C.7(a); Ex.1002, ¶¶197-198.) However, *Tsukada* discloses these elements, and in view of *Tsukada* it would have been obvious to a POSITA to modify the *Park-Baker* system so that the integrated circuit of the *Park-Baker* system further comprises a memory wherein the back bias voltage V_{BB} ("bias voltage V1") is applied to a silicon substrate region in which memory cells reside. (Ex.1002, ¶198.)

For example, Tsukada discloses a DRAM device ("memory") wherein a substrate bias voltage V_{BB} ("bias voltage V1") is applied to silicon a semiconductor substrate ("substrate region") in which a DRAM cell ("memory cell[]") resides. (Ex.1002, ¶199.) In particular, Tsukada discloses that "[i]n FIG. 1A, which

illustrates a conventional stacked-capacitor type **DRAM cell**, reference numeral 101 designates a P- type monocrystalline **silicon** substrate" (Ex.1009, 2:46-49 (emphasis added)) and that a "**substrate bias voltage V_{BB} is applied** by a substrate bias voltage controlling apparatus **to the substrate** 101" (id., 2:62-64 (emphasis added)). (Ex.1002, ¶199; see also Ex.1009, 1:11-14.)

As discussed above, a DRAM cell ("memory cell[]") is shown in figure 1A of *Tsukada* (reproduced below with annotations). (Ex.1002, ¶200.)

Fig. 1A PRIOR ART



(Ex.1002, ¶200, citing Ex.1009, FIG. 1A (annotated).)

Although a single DRAM cell ("memory cell[]") is shown in *Tsukada*'s figure 1A, *Tsukada* discloses a DRAM device ("memory") having multiple DRAM cells ("memory cells"). (Ex.1002, ¶201.) For example, *Tsukada* discloses that "in a DRAM device mounted in a portable personal computer, … improved hold characteristics of the **memory cells** must be strictly required." (Ex.1009, 4:18-25 (emphasis added); *see also id.*, 3:9, 4:45, 6:14-24.)

Thus, a POSITA would have understood *Tsukada* to disclose that multiple DRAM cells ("memory cells") reside in *Tsukada*'s substrate 101 ("silicon substrate region"). (Ex.1002, ¶202.) *Tsukada* is directed to the same field (e.g., semiconductor devices) as *Park* and *Baker*, so a POSITA would have looked to *Tsukada* when considering how and in what contexts to implement and apply the combined *Park-Baker* system discussed above with respect to claim 30. (Ex.1007, 5:30-31 (disclosing negative electric potential applied to substrate), Ex.1009, 1:11-15 (disclosing substrate bias voltage applied to semiconductor substrate); Ex.1002, ¶203.)

Having looked to *Tsukada*, a POSITA would have recognized that the integrated circuit of the combined *Park-Baker* system described claim 30 provides a back bias voltage V_{BB} that is usable for biasing *Tsukada*'s substrate 101 and therefore would have been motivated to modify the *Park-Baker* combination in the above manner to bias *Tsukada*'s substrate 101, because *Tsukada* discloses that the

substrate 101 is biased by a "negative substrate bias voltage" similar to the back bias voltage V_{BB} of the *Park-Baker* system. (*See supra* Section IX.C.7(a) regarding back bias voltage V_{BB} provided by *Park-Baker* combination; Ex.1007, FIG. 8 (disclosing negative back bias voltage V_{BB}); Ex.1009, 1:12-13 ("negative substrate bias voltage"); Ex.1002, ¶204.)

A POSITA would have recognized that modifying the *Park-Baker* combination in the above manner based on the teachings of *Tsukada* would have constituted a mere combination of known components (circuitry of the *Park-Baker* combination as discussed above with respect to claim 30, and *Tsukada*'s DRAM, silicon substrate 101, and DRAM cells), according to known methods (e.g., *Park-Baker* combination discloses applying a back bias voltage V_{BB} to a substrate, and *Tsukada* discloses where to apply a substrate bias voltage in the context of a DRAM device), to achieve predictable results (e.g., *Tsukada*'s substrate of the DRAM device will be biased in the same way that the substrate of the *Park-Baker* combination is biased). (Ex.1002, ¶205.) *See KSR*, 550 U.S. at 416.

Thus, *Tsukada* teaches a particular type of device (DRAM device) in which to implement the techniques and circuitry of the *Park-Baker* combination, and a POSITA would have known that combining *Park*, *Baker*, and *Tsukada* in the above manner would not only have beneficially provided a useful application

(DRAM) for substrate biasing but would have done so in a predictable manner with a reasonable expectation of success. (Ex.1002, ¶206.)

2. Claim 33

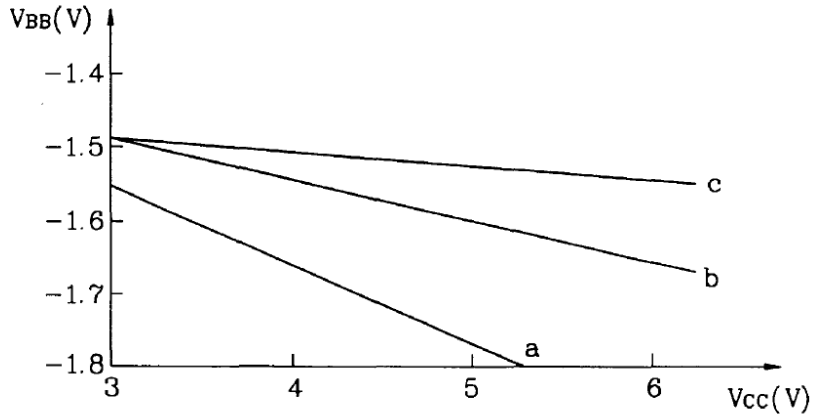
a) **"The integrated circuit of claim 32 wherein the memory is a dynamic random access memory (DRAM)."**

Park in combination with *Baker* and *Tsukada* discloses or suggests this feature. (Ex.1002, ¶207.) For instance, the combined *Park-Baker-Tsukada* system discloses that the DRAM device ("memory") is a dynamic random access memory (DRAM), as discussed above with respect to claim 32. (*See supra* Section IX.D.1; Ex.1002, ¶207.)

3. Claim 34

a) **"The integrated circuit of claim 32 wherein the bias voltage is less than or equal to 0 volt."**

Park in combination with *Baker* and *Tsukada* discloses or suggests this feature. (Ex.1002, ¶208.) For instance, *Park* discloses that the back bias voltage V_{BB} ("bias voltage") is less than or equal to 0 volt. (*Id.*) In particular, *Park* discloses by way of its figure 8 that the back bias voltage V_{BB} ("the bias voltage") is less than 0 volts:



(Ex.1007, FIG. 8; Ex.1002, ¶208.)

A POSITA would have understood given the values of the back bias voltage V_{BB} ("bias voltage") in *Park*'s figure 8 that the back bias voltage V_{BB} is **less than** or equal to **0 volt**. (Ex.1002, ¶209; *see also supra* Section IX.C.5(f).)

E. Ground 5: *Park, Baker,* and *Young* Render Obvious Claim 35

1. Claim 35

a) **"The integrated circuit of claim 30 further comprising a memory wherein the bias voltage is applied to a well region in which memory cells reside, the well region being formed in a silicon substrate of a conductivity type opposite that of the well region."**

Park in combination with *Baker* and *Young* discloses or suggests this feature. (Ex.1002, ¶¶210-211.) The combined *Park-Baker* system discloses an integrated circuit comprising a substrate to which a back bias voltage V_{BB} ("bias voltage V1") is applied. (Ex.1002, ¶211; *see supra* Section IX.C.7(a).) While the combined *Park-Baker* system does not disclose the integrated circuit comprises a memory wherein the back bias voltage V_{BB} ("bias voltage V1") is applied to a well

region in which memory cells reside and where the well region is formed in a silicon substrate of a conductivity type opposite that of the well region, it would have been obvious in view of *Young* to configure the *Park-Baker* system to implement this feature. (Ex.1002, ¶211.) A POSITA would have recognized that such an application of the circuit of *Park-Baker* was well known, as evidenced by *Young*, and would have been motivated to configure the *Park-Baker* system in this manner. (*Id.*)

At the time of the alleged invention of the '554 patent, it was well-known that "[m]emory arrays processed using CMOS technology often include memory cells formed in a well of a P [] conductivity type." (*Id*., ¶212; Ex.1012, 1:14-16.) It was further well-known that P-wells were formed in an N-type silicon substrate. (Ex.1002, ¶213, citing Ex.1014.) Therefore, *Young* is evidence that it was well-known to form a memory array in which memory cells reside in a P-well formed on an N-type silicon substrate ("a well region in which memory cells reside, the well region being formed in a silicon substrate of a conductivity type opposite that of the well region"). (*Id*., ¶¶212-215.)

Young is further evidence that the P-well would have been biased by a negative voltage. (Ex.1012, 1:14-21 ("bias this well to . . . below the power supply ground for P-well CMOS arrays."); *see also id*. at 2:51-56.) A POSITA would

have known that the reason for such biasing is to prevent forward biasing pn junctions formed by n+ implant regions in the P-well. (Ex.1002, ¶¶216-217.)

As discussed above, the *Park-Baker* bias circuit generates **a negative** back bias voltage that is insensitive to power supply variations. (*Supra* Section IX.C.7; IX.C.1; VII.C; Ex.1007, 5:29-32, 5:12-14, 6:32-35, FIG. 8.) Thus, a POSITA would have recognized in view of *Young* that the *Park-Baker* bias circuit could be used to bias a P-well in a memory array, where the P-well includes memory cells and is formed on an N-type silicon substrate. Such a POSITA would have been motivated to do so because it was well known to provide a negative bias to such P-wells, as evidenced by *Young*, and doing so would have increased the utility of the *Park-Baker* circuit while providing the P-well with a stable negative bias voltage. (Ex.1002, ¶218.) A POSITA would have had a high likelihood of success regarding the combined system, as the combination would have constituted a mere combination of known components (the well-known memory cell arrays and the *Park-Baker* back bias generator), according to known methods (providing the VBB output of the *Park-Baker* circuit to a P-well in which the memory cells reside), to achieve predictable results (an operational memory with properly biased P-well). (Ex.1002, ¶¶218-221.) *See KSR*, 550 U.S. at 416.

Young is directed to the same field (e.g., semiconductor devices) as *Park* and *Baker*, so a POSITA would have had reason to look to the teachings of *Young*

when considering how and in what contexts to implement and apply the combined *Park-Baker* system discussed above for claim 30. (Ex.1007, 5:30-31, 5:46-48; Ex.1008, Title; Ex.1012, 1:9-12; Ex.1002, ¶219.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of *inter partes* review and cancellation of claims 1-3, 14-16, 22, and 28-36 of the '554 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: May 12, 2017 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,172,554 contains, as measured by the word processing system used to prepare this paper, 13,951 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: May 12, 2017

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on May 12, 2017, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,172,554 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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