Paper No. __
Filed: May 12, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,208,574

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,208,574

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 4-18 and 21-27 of U.S. Patent No. 6,208,574 ("the '574 patent") (Ex.1001), which is currently assigned to ProMOS Technologies, Inc. ("Patent Owner") according to USPTO records. For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Austin Semiconductor, LLC, and Samsung Semiconductor, Inc.

Related Matters: Patent Owner has asserted the '574 patent against Petitioner and the above real parties-in-interest in *ProMOS Technologies, Inc. v. Samsung Electronics, Ltd., Co.*, Case No. 1:16-cv-00335-SLR-SRF (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 6,069,507 ("the '507 patent"), 6,172,554 ("the '554 patent"), 6,562,714 ("the '714 patent"), 7,375,027 ("the '027 patent"), and 6,559,044 ("the '044 patent") in this action. Petitioner is concurrently filing another IPR petition challenging claims 1-3 and 30-39 of the '574 patent as well as additional IPR petitions challenging certain claims of the '507, '554, '714, '027, and '044 patents. Petitioner also previously filed several

IPR petitions involving additional patents asserted by Patent Owner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Specifically, on October 7, 2016, Petitioner filed IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. All of these proceedings were instituted and remain pending except for the 00033 and 00035 proceedings. Moreover, the '574 patent is in the same family as U.S. Patent No. 6,088,270 ("the '270 patent"), which is at issue in IPR2017-00036 in which the Board recently instituted *inter partes* review.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '574 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

A. Claims for Which Review is Requested

Petitioner respectfully requests review of claims 4-18 and 21-27 ("challenged claims") of the '574 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following grounds:

Ground 1: Claims 4-10, 14-16, and 21-27 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Japanese Patent Publication JPS58-128087 to Inoue *et al.* ("*Inoue*") (Ex.1007),[1] UK Patent Application Publication No. G.B. 2246005A to Min *et al.* ("*Min*") (Ex.1008), and U.S. Patent No. 5,323,349 to

[1] Ex.1007 is a compilation containing the English-language translation of *Inoue* (Ex.1007, 1-5), followed by the Japanese language version (*id.*, 6-10). An affidavit required by 37 C.F.R. § 42.63(b) (in the form of a declaration as permitted by 37 C.F.R. § 42.2) follows the Japanese-language version (*id.*, 11), and a certification of correction to the certified translation follows the declaration (*id.*, 12.).

Hamade *et al.* ("*Hamade*") (Ex.1009);

Ground 2: Claims 11-13 are unpatentable under 35 U.S.C. § 103(a) as being obvious over of *Inoue, Min*, *Hamade* and U.S. Patent No. 5,293,347 ("*Ogawa*") (Ex.1010);

Ground 3: Claim 17 is unpatentable under 35 U.S.C. § 103(a) as being obvious over *Inoue, Min*, and *Hamade*; and

Ground 4: Claim 18 is unpatentable under 35 U.S.C. § 103(a) as being obvious over *Inoue, Min*, *Hamade*, and *Ogawa*.[2]

The '574 patent issued from U.S. Application No. 08/432,884 filed May 2, 1995, which claims priority to U.S. Application No. 07/976,312 filed on November 12, 1992. *Inoue* was published on July 30, 1983, and thus is prior art to the '574 patent at least under pre-AIA 35 U.S.C. § 102(b). *Min* was published on January 15, 1992, and is thus prior art to the '574 patent at least under pre-AIA 35 U.S.C. § 102(a). *Hamade* issued June 21, 1994, from U.S. Application No. 936,454 filed August 28, 1992. *Ogawa* issued on March 8, 1994, from U.S. Application No. 814,174 filed December 30, 1991. Therefore, *Hamade* and *Ogawa* are prior art to the '574 patent at least under pre-AIA 35 U.S.C. § 102(e). *Inoue*, *Min*, *Hamade*,

[2] Grounds 3 and 4 are presented separately from Grounds 1 and 2 because they rely on different disclosures from the references.

and *Ogawa* were never considered by the Patent Office during prosecution of the '574 patent. (*See* Ex.1001, 1 (References Cited).)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA at the time of the alleged invention of the '574 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in design of semiconductor memory circuits. (Ex.1002, ¶20.)[3] More education can supplement practical experience and vice versa. (*Id*.)

VII. OVERVIEW OF THE '574 PATENT AND PRIOR ART

A. The '574 Patent

The '574 patent relates to a "sense amplifier for a very high density integrated circuit memory using CMOS technology." (Ex.1001, Abstract; Ex.1002, ¶¶38-42.) The '574 patent acknowledges that sense amplifiers were known at the time of the alleged invention. (Ex.1001, Title, FIG. 1, 1:47-2:13.) The '574 patent discloses a preferred embodiment of a sense amplifier 100 in connection with figure 5. (Ex.1001, 1:46-62, 6:3-9, 6:32-63, 6:66-7:13, 7:43-46, FIGS. 1, 5; Ex.1002, ¶¶39-41.)

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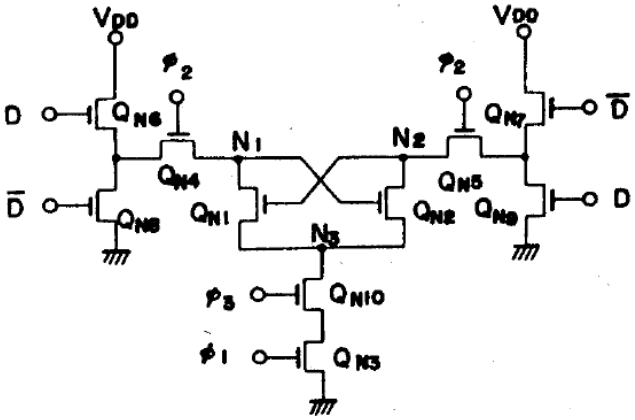
[3] Petitioner submits the declaration of Dr. R. Jacob Baker (Ex.1002), an expert in the field of the '574 patent. (Ex.1002, ¶¶5-15; Ex.1003.)

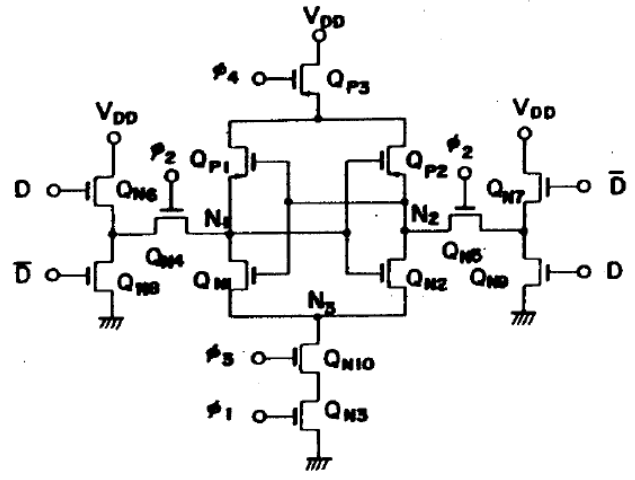
B. *Inoue*

Inoue discloses a semiconductor device including a sense amplifier with internal nodes and a flip-flop circuit capable of latching into two states (states I and II). (Ex.1007, 1 (Claim 1), 3; Ex.1002, ¶¶52-55.) *Inoue* discloses two configurations in figures 4 and 6 that are designed to consume a small amount of transient power when writing to a flip-flop. (Ex.1007, 3; Ex.1002, ¶52.)

第 4 図



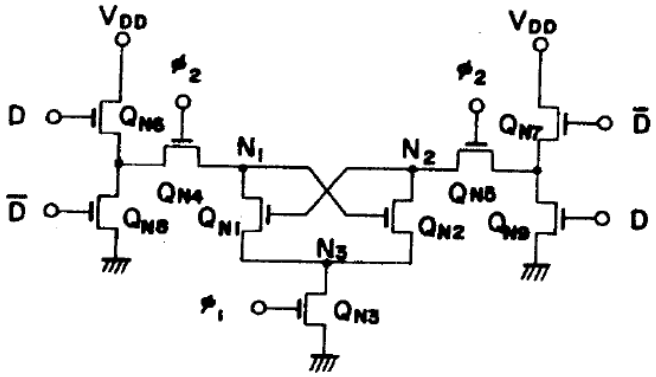
第 6 図



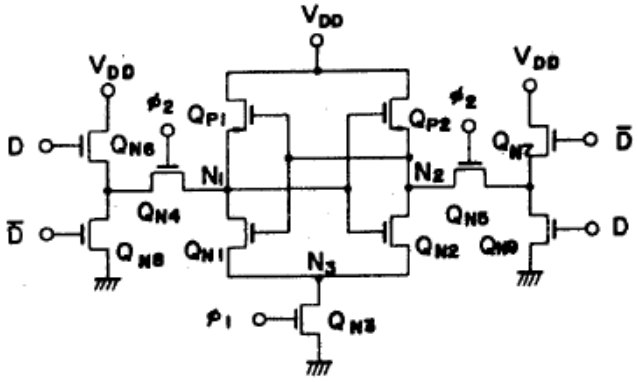
(Ex.1007, FIGS. 4, 6.[4])

The two embodiments in figures 4 and 6 of *Inoue* build on conventional flip-flops shown in figures 1 and 3, respectively. (Ex.1002, ¶53.)

第 1 図



第 3 図



[4] In this Petition, Petitioner refers to the text of the English translation of *Inoue*, but sometimes may show figures from the Japanese version because those figures are clearer.

(*Id.*, 5, FIGS. 1, 3; Ex.1002, ¶53.)

Inoue's first embodiment in figure 4 adds to the conventional flip-flop of figure 1 a transistor Q_{N10} for pulling down node N_3. (*Id.*, 4, 5, FIGS. 1, 4; Ex.1002, ¶54.) The "embodiment [of FIG. 6] differs from FIG. 4 in the addition of a P-channel transistor Q_{P3}, which is controlled by clock ϕ_4, and also in the addition of PMOS transistors Q_{P1} and Q_{P2} as in the circuit of figure 3. (Ex.1007, 4, 5, FIGS. 3, 4, 6; Ex.1002, ¶54.) Much of the functionality of figure 6 is described at the portion of *Inoue* pertaining to figure 4, so *Inoue* does not repeat that description when describing FIG. 6. (Ex.1007, 4; Ex.1002, ¶54.) Figure 6 of *Inoue* differs from the circuit of figure 3 in the addition of pull-up transistor Q_{P3} and pull-down transistor Q_{N10}. (Ex.1007, 5, FIGS. 3, 6; Ex.1002, ¶54.) Like figure 3, figure 6 contains P channel transistors Q_{P1} and Q_{P2} and N channel resistors Q_{N1} and Q_{N2} within the flip-flop. (Ex.1002, ¶54.)

Inoue discloses that the flip-flop of figure 6 latches into one of two stable states, corresponding to node N_1 at a level 'H' and node N_2 at a level 'L' in a first state or vice-versa in the second state. (Ex.1007, 3; Ex.1002, ¶55.) A POSITA would have understood that a flip-flop such as in figure 6 of *Inoue* is a latch circuit, which is consistent with the understanding of such circuitry as discussed in the '574 patent. (Ex.1002, ¶55; Ex.1001, 1:58-62, 2:6-14, 6:5-13, FIGS. 1, 5.)

VIII. CLAIM CONSTRUCTION

The '574 patent is set to expire on March 27, 2018. Therefore, the '574 patent will expire within 18 months from entry of any notice of filing date issued in this proceeding should the Board institute review. *See* 37 C.F.R. § 42.100(b). Accordingly, the claims of the '574 patent should be construed under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See, e.g.*, *Square Inc. v. J. Carl Cooper*, IPR2014-00156, Paper No. 38 at 7 (May 14, 2015) (citing *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)). Under *Phillips*, claim terms are given their ordinary and customary meanings, as would be understood by a POSITA, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *See, e.g.*, *Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 20 at 2-3 (July 10, 2014). The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Below, Petitioner discusses the construction of two terms. Any term not construed below should be interpreted in accordance with its plain and ordinary

meaning.[5] Petitioner has applied these understandings in its analysis of the '574 patent.

A. "local data write driver circuit"

For purposes of this proceeding, the phrase "local data write driver circuit," which appears in each independent claim (claims 1, 4, and 30), should be construed as "a data write driver circuit that is associated with only one latch circuit." The Board previously adopted this construction for this same claim term in an IPR pertaining to the '270 patent, which is in the same family as the '574 patent. *Samsung Elecs. Co., Ltd. v. ProMOS Techs., Inc.*, IPR2017-00036, Paper No. 6 at 8 (Apr. 6, 2017). The intrinsic record supports Petitioner's construction. (Ex.1002, ¶¶44-47.)

The plain language of the claims supports this construction. Claim 1, for instance, states that "***each*** said sense amplifier is coupled to a pair of said local data write driver circuits" where "each sense amplifier compris[es] a latch circuit."

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[5] Petitioner reserves all rights to raise claim construction and other arguments in other proceedings, including the pending district court litigation (*see supra* Section II). For example, Petitioner has not necessarily raised all challenges to the '574 patent, including challenges to the claims under 35 U.S.C. § 112, given the limitations placed by the Rules.

(Ex.1001, 13:24-25, 12:61.) Similarly, claim 4 recites that "a local data write drive circuit" is provided for "each of a plurality of sense amplifiers" having a "sense amplifier latch circuit." (*Id*., 13:46-58.) Claim 30 also recites that "first and second local data write drive circuits" are provided for "each of a plurality of sense amplifiers" having a "sense amplifier latch circuit." (*Id*., 15:52-16:5.)

The specification supports Petitioner's construction. Throughout the specification, a local write driver circuit or its constituent components are described as being connected to, or associated with, a single latch circuit. For instance, figure 5 of the '574 patent discloses a sense amplifier 100 including data write driver circuits ("local" data write transistors 128/130 and 132/134) connected to a single latch circuit (transistors 112, 114, 118, 120). (Ex.1001, 6:5-13, 7:15-16; *see also id*., FIG. 5 (annotated below), *id*., 4:62-64 ("[t]he present invention provides a CMOS sense amplifier with local write driver transistors . . . ."), 5:29-36.)

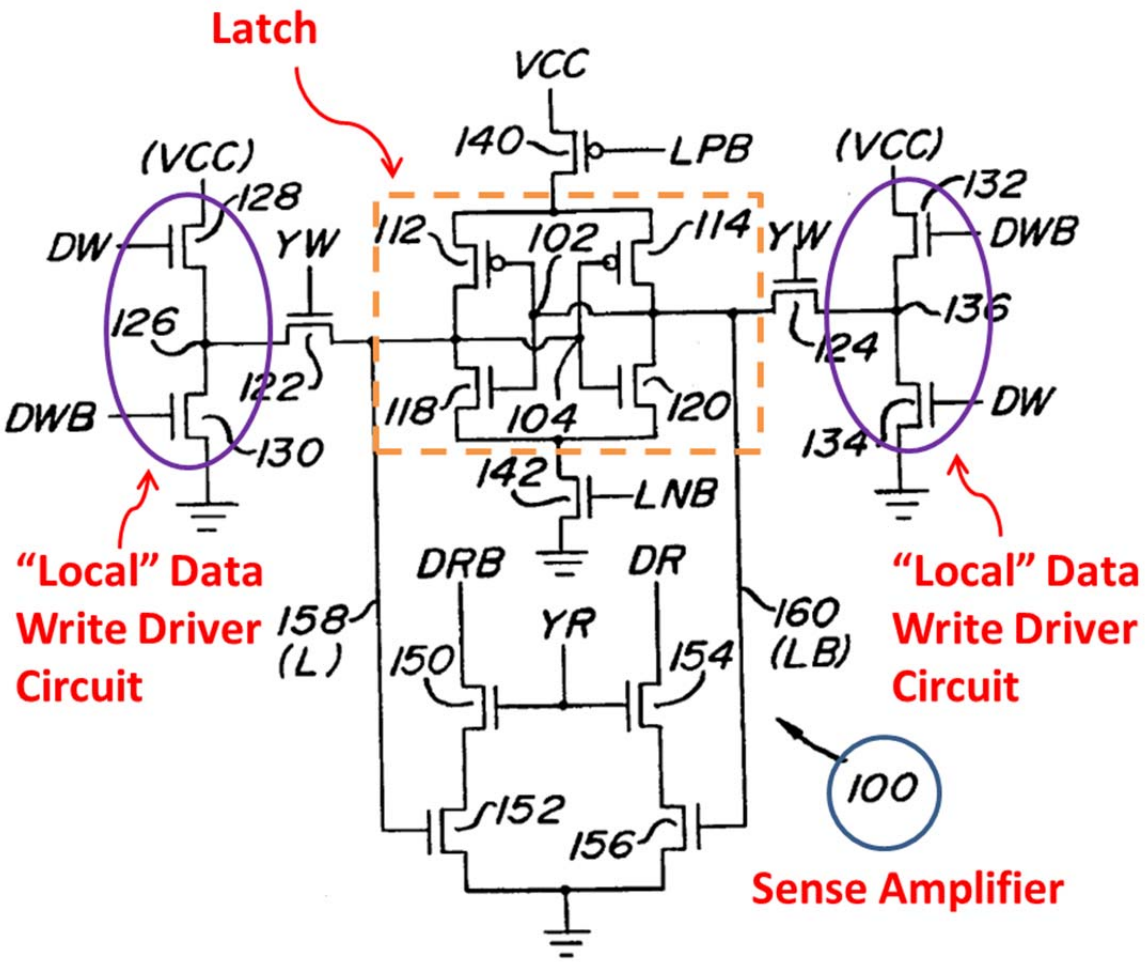

FIG. 5

(Ex.1002, ¶46, citing Ex.1001, FIG. 5 (annotated).)

The '574 patent also defines the term "global" as "connected to **several** sense amps," which suggests that "local" should denote an association with only **one** sense amplifier (and thereby, a single latch circuit). (Ex.1001, 11:25-31 (emphasis added); Ex.1002, ¶47.)

Because each sense amplifier includes a latch circuit (*see* Ex.1001., 1:46-62, FIGS. 1, 2) and each independent claim recites "a latch circuit," Petitioner's

proposed construction includes the phrase "only one latch circuit" rather than "only one sense amplifier" for consistency with the claim language.

The patentee unequivocally confirmed this interpretation of "local" data write driver circuits during the prosecution history of a related patent to the '574 patent. (*See* Ex.1006, 274 ("the pair of data write circuits in the present application is associated with only one latch circuit and is clearly local to that one latch circuit").) The prosecution history of the parent '312 application is also consistent with Petitioner's proposed construction. There, the patentee clarified the difference between "local" and "global" and explained that a transistor is "local" when it is associated with only *one* sense amplifier. (Ex.1005, 166-68.) Thus, the prosecution history shows a clear and intentional disavowal of claim scope regarding a data write driver circuit that is associated with more than one latch circuit.[6] [7] *See Abbott Laboratories v. Sandoz, Inc.*, 566 F.3d 1282, 1290 (Fed. Cir.

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[6] Patent Owner may argue against Petitioner's construction because in an *ex parte* appeal of the '183 application, the Board stated that "local" means something that has "a definite spatial form or location." (Ex.1006, 299 (Decision on Appeal dated Nov. 30, 1999 at 7).) But the Board found in IPR2017-00036 that Petitioner's construction, which is under *Phillips*, is "not inconsistent with the Board's prior

2009) (en banc).

B. "local column read amplifier"

For purposes of this proceeding, the phrase "local column read amplifier," which appears in each independent claim (claims 1, 4, and 30), should be construed as "a column read amplifier that is associated with only one latch circuit." The intrinsic record supports Petitioner's construction. (Ex.1002, ¶¶48-51.)

The plain language of the claims supports Petitioner's construction. For instance, claim 1 recites that each local column read amplifier is "responsively coupled to said internal nodes of **said** latch circuit of a corresponding sense amplifier." (Ex.1001, 13:22-24 (claim 1) (emphasis added).) Similarly, claim 4 recites that "a local column read amplifier responsively coupled to the sense

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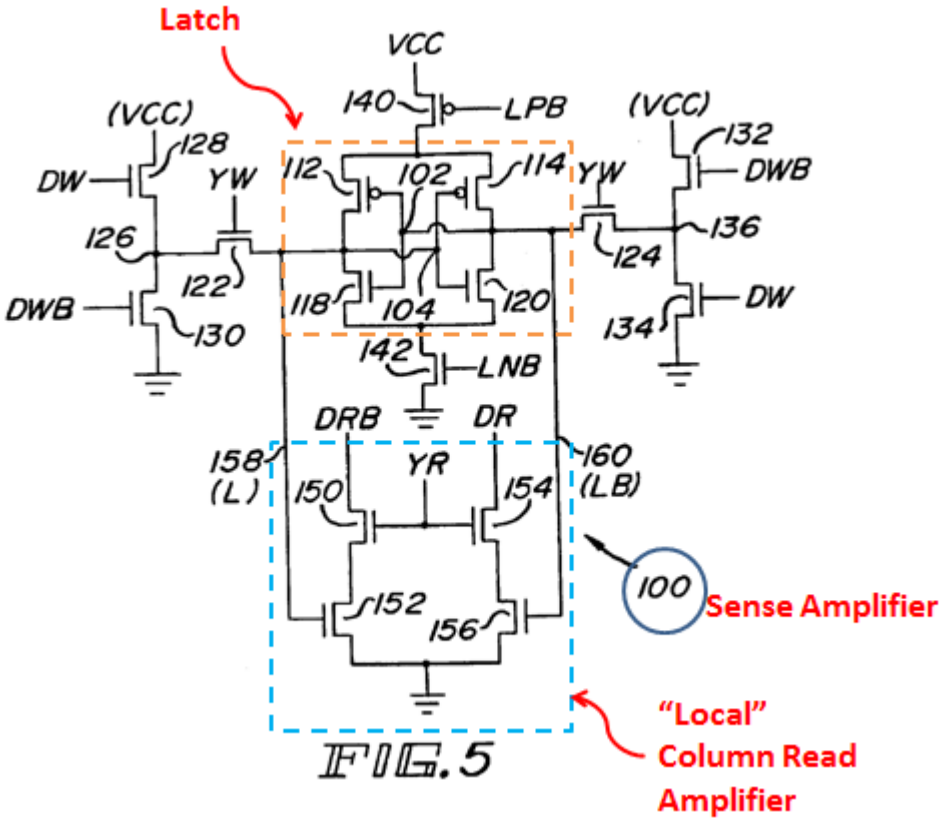
construction, which was made under a broadest reasonable interpretation standard." IPR2017-00036, Paper No. 6 at 8.

[7] Further, while the specification discloses that the local data write driver transistors 128-134 can be shared with other column circuits (Ex.1001, 7:55-57), the patentee's unequivocal characterization of "local" data write driver circuit during prosecution confirms the above proposed interpretation and is consistent with the specification's description of "global."

amplifier" having a "sense amplifier latch circuit." (*Id.*, 13:46-58.) Claim 30 also recites that "a sense amplifier latch circuit having first and second latch nodes" to which "a local column read amplifier" is coupled. (*Id.*, 15:52-16:1.)

Additionally, throughout the specification, a local column read amplifier is described as being connected to, or associated with, a single latch circuit. For instance, figure 5 of the '574 patent "includes a local column read amplifier which includes four N channel transistors 150, 152, 154, and 156" connected to a single latch circuit (transistors 112, 114, 118, 120). (*Id.*, 6:66-7:1; *see also id.*, FIG. 5 (annotated below); *id.*, 4:64-65, 5:29-36.)



(Ex.1002, ¶50, citing Ex.1001, FIG. 5 (annotated).)

Furthermore, as discussed above regarding the claim term "local data write driver circuit," the definition of "global" in the '574 patent suggests that "local" should denote an association with only one sense amplifier, and that argument also applies to support Petitioner's proposed construction of "local column read amplifier." (*See supra* Section VIII.A; Ex.1002, ¶¶47,51.) Because each sense amplifier includes a latch circuit (*see* Ex.1001, 1:46-62, FIGS. 1, 2) and each independent claim recites "a latch circuit," Petitioner's proposed construction includes the phrase "only one latch circuit" rather than "only one sense amplifier" for consistency with the claim language.

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: *Inoue*, *Min and Hamade Render* Obvious Claims 4-10, 14-16 and 21-27 of the '574 Patent

Grounds 1 and 2 in this petition focus on the disclosure of figure 6 in *Inoue*. The disclosure of figure 6 builds on the circuits disclosed in figures 1, 3, and 4 of *Inoue*. (Ex.1002, ¶¶52-55.) For instance, when describing figure 6, *Inoue* does not repeat details previously discussed for common aspects between figures 1, 3, 4, and 6. (*Id*.) Below, Petitioner refers to the common aspects of figures 1, 3, 4, and 6 when describing aspects of figure 6. (*See supra* Section VII.B.)

1. Claim 4

a) "A sense amplifier arrangement for an integrated circuit memory comprising,"

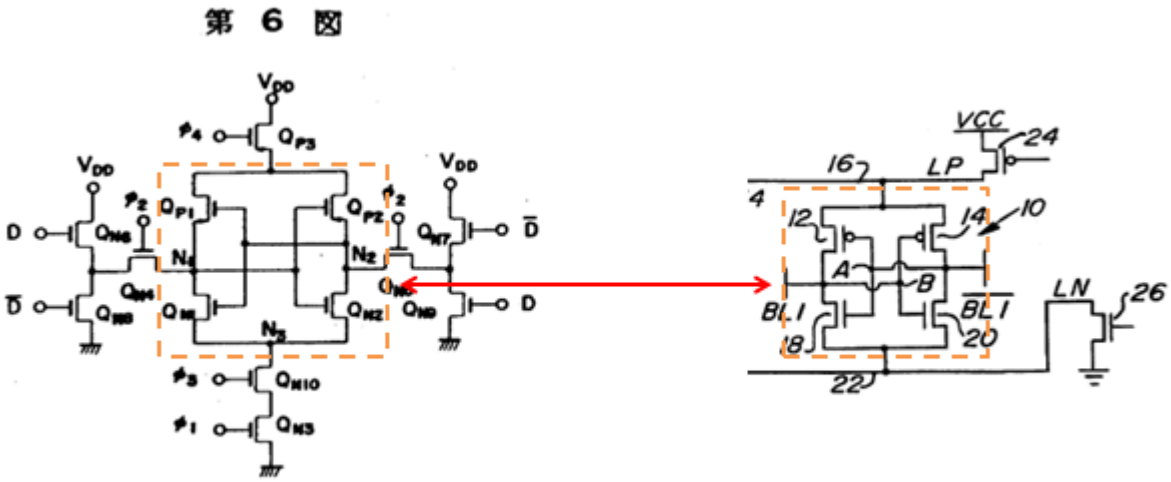
To the extent the preamble is limiting, *Inoue* discloses this feature. (Ex.1002, ¶68.) For example, *Inoue* discloses "a semiconductor device" comprising a sense amplifier with a flip-flop circuit. (*Id.*; Ex.1007, 1 (Claim 1).) The circuit in figure 6 of *Inoue* is for a sense amplifier in a dynamic memory. (Ex.1007, 4; Ex.1002, ¶68; *see also supra* Section VII.B.) A POSITA would have understood that "dynamic memory" in *Inoue* refers to a dynamic random access memory (DRAM), which is an integrated circuit memory. (*See* Ex.1002, ¶68; *see also* citations and analysis below for the remaining elements of this claim.)

b) "for each of a plurality of sense amplifiers: a sense amplifier latch circuit having a pair of nodes to which respective bit lines may be coupled;"

To the extent "may be coupled" does not render claim 4 indefinite[8], the combined *Inoue-Min* system discloses this feature. (Ex.1002, ¶¶69-83.) Figure 6 of *Inoue* "shows a CMOS F/F," where the "F/F" includes a pair of internal nodes "N_1 and N_2 corresponding to bit lines." (Ex.1007, 4, FIG. 6.) In particular, the "CMOS F/F" in figure 6 of *Inoue* includes transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}.

[8] For purposes of this proceeding, Petitioner assumes "may be coupled" specifies a required coupling, but does not concede the definiteness of the claim.

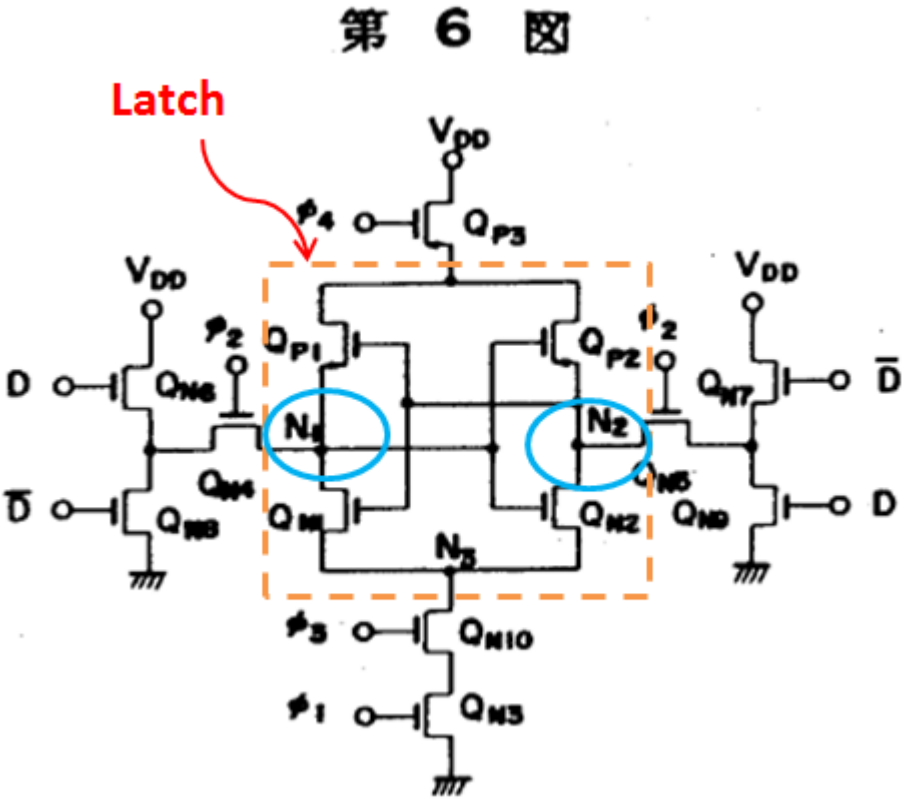
(Ex.1002, ¶69.; Ex.1007, 3-4, FIG. 6.) The flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} would have been readily recognized by a POSITA as a "latch." (Ex.1002, ¶70.) The '574 patent confirms this because it shows the exact same configuration with transistors 12, 14, 18, and 20 and states that "[t]hese transistors form a latch." (*Id*.; *compare* Ex.1007, FIG. 3 (transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}), *with* Ex.1001, 1:61-62, FIG. 1 (transistors 12, 14, 18, and 20).) Moreover, the flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} would also have been readily recognized by a POSITA as a "sense amplifier." (Ex.1002, ¶71.) The '574 patent again confirms this as it shows the exact same configuration and acknowledges that such a configuration was the well-known configuration for a "sense amplifier." (*Id*.; *compare* Ex.1007, FIG. 3 (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}), *with* Ex.1001, 1:47-62, FIG. 1, illustrating "sense amplifier 10" that includes P-channel transistors 12, 14 and N-channel transistors 18, 20.) A POSITA would have thus recognized that the transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} in figure 6 of *Inoue* constitute a "sense amplifier latch circuit" as recited in claim 4. (Ex.1002, ¶71.) The demonstrative below shows the correspondence between the circuit in figure 6 of *Inoue* and "sense amplifier 10" shown in figure 1 of the '574 patent.



Inoue, FIG. 6 '574 Patent, FIG. 1 (excerpt)

(Ex.1002, ¶71, citing Ex.1007, FIG. 6, Ex.1001, FIG. 1 (annotated).)

The "sense amplifier latch circuit" shown in figure 6 of *Inoue* includes a pair of internal nodes "N_1 and N_2 corresponding to bit lines" that constitute "a pair of nodes to which respective bit lines are coupled." (Ex.1007, 4, FIG. 6; Ex.1002, ¶72.)

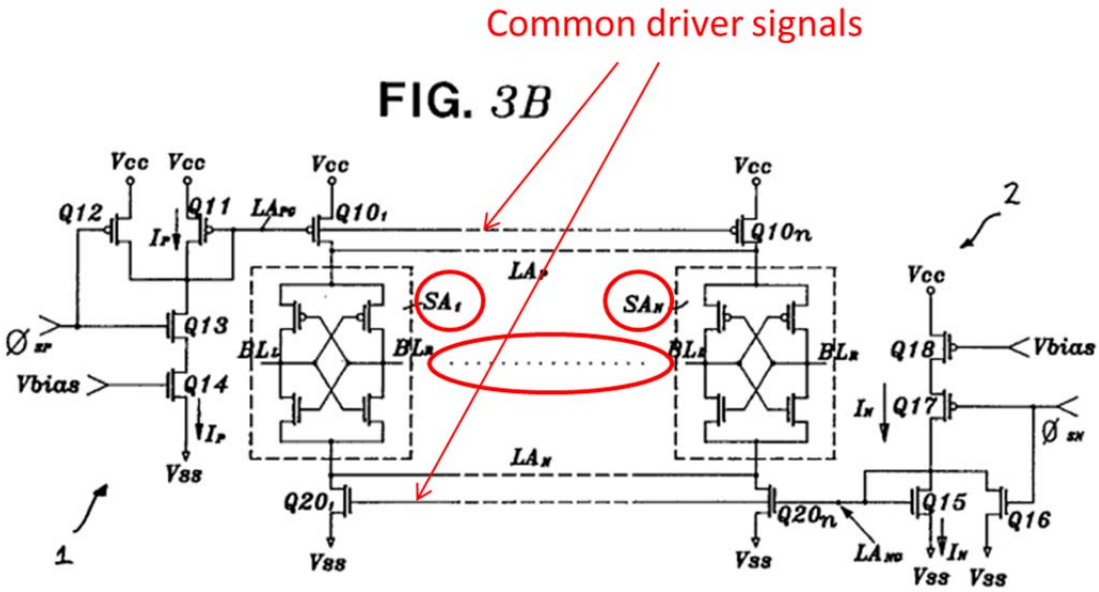


(Ex.1002, ¶72, citing Ex.1007, FIG. 6 (annotated to show internal nodes (blue) of the latch circuit (orange).)

A POSITA would have understood that the flip-flop of figure 6 is part of one sense amplifier and that other sense amplifiers are also present in *Inoue*'s dynamic memory. (Ex.1007, 4; Ex.1002, ¶73.) Therefore, a POSITA would have understood that *Inoue* discloses a "plurality of sense amplifiers." While *Inoue* does not expressly show the multiple sense amplifiers in any figure, nor does *Inoue* expressly show a figure with a plurality of such sense amplifiers having a pair of nodes to which respective bit lines are coupled, *Min* provides such disclosure. (*Id.*)

Min discloses the replication of sense amplifiers in a memory device where each sense amplifier is associated with respective bit lines in the form of a bit line pair for each sense amplifier. (*Id*.) In view of *Min*, a POSITA would have been motivated to implement *Inoue*'s figure 6 circuit in a multi-column memory system to create a dynamic memory having a plurality of bit line pairs with each of bit line pairs coupled to a respective sense amplifier. (*Id*.)

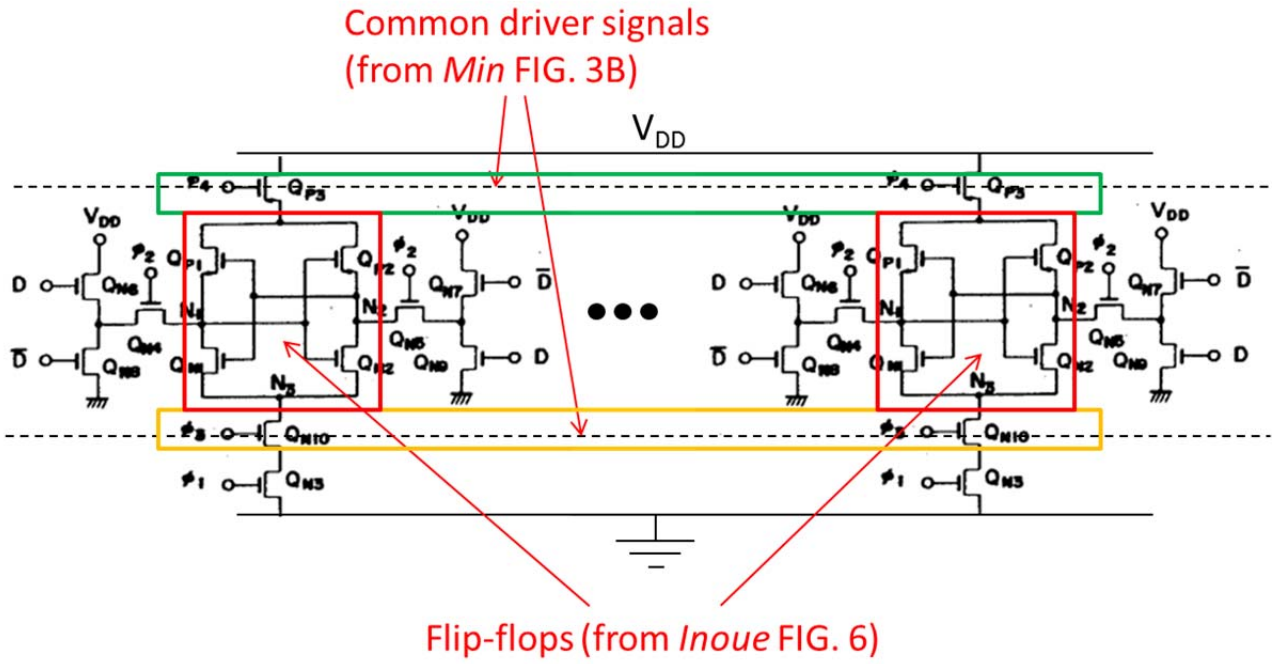
Min, which like *Inoue* is in the field of semiconductor memory, discloses a semiconductor memory device having a plurality of sense amplifiers SA_1-SA_N. (*Id*.; Ex.1008, 1:4-8, 21:1-13, FIG. 3B.) Each sense amplifier SA_i (where i is an integer between 1 and N) in figure 3B of *Min* is coupled to a corresponding bit line pair (BL_L and BL_R) and is coupled to a positive power supply (Vcc) and to ground (Vss) via driving transistors $Q10_i$ and $Q20_i$, respectively. (Ex.1008, 2:5-15, 21:1-13, FIG. 3B; Ex.1002, ¶74.) *Min* teaches the use of a common driver signal for driving PMOS transistors $Q10_i$ of respective columns and another common driver signal for driving NMOS transistors $Q20_i$ of respective columns. (Ex.1008, FIG. 3B; Ex.1002, ¶74.)



(Ex.1002, ¶74, citing Ex.1008, FIG. 3B (annotated to show plurality of sense amplifiers and common driver signals).)

A POSITA would have looked to *Min* for guidance regarding implementing the circuit of figure 6 of *Inoue* in a practical DRAM having multiple bit line pairs, particularly because *Min* and *Inoue* are references in the same field. (Ex.1002, ¶¶75-81.) Having looked to *Min*, such a person would have been motivated to replicate *Inoue*'s circuitry of figure 6 based on *Min* to implement a multi-column DRAM. (*Id*.) In such a multi-column DRAM, the circuit of figure 6 of *Inoue* would have been present for each of a plurality of columns, and the driver transistors (e.g., exemplified below as Q_{P3} (annotated in green) and Q_{N10} (annotated in orange)) of respective columns would have been driven by respective common

driver signals. (Ex.1002, ¶¶75,80.)[9] Specifically, a common clock ϕ_4 signal would have been provided to each of transistors Q_{P3} and a common clock ϕ_3 signal would have been provided to each of transistors Q_{N10}. Below is a non-limiting example showing a generalized illustration of a modified circuit.



(Ex.1002, ¶75, annotated to show, for respective columns, transistors Q_{P3} in green

[9] A POSITA would have been motivated to replicate the entire circuit of figure 6 instead of replicating just the latch portion (i.e., Q_{P1} and Q_{P2} and NMOS transistors Q_{N1} and Q_{N2}). (Ex.1002, ¶78.) A POSITA would have also known the benefit of not coupling together the drains of transistors Q_{P3} and Q_{N10} across multiple columns. (Ex.1002, ¶79.)

and transistors Q_{N10} in orange).)

A POSITA would have been motivated to combine the teachings of *Inoue* and *Min* as described above to implement a multi-column DRAM, which was a known benefit because practical DRAMs had multiple columns.[10] (Ex.1002, ¶76.) *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 ("*KSR*"). Moreover, a POSITA would have found it beneficial to use common driver signals for the driver transistors of respective columns because using the same clock signals ϕ_4 and ϕ_3 to drive transistors Q_{P3} and Q_{N10} would have resulted in a reduction of circuitry (and therefore, use of the chip area) as opposed to case in which different clock signals were provided for transistors Q_{P3} and Q_{N10} of each latch circuit. (Ex.1002, ¶80.) *KSR*, 550 U.S. at 416-17.

Such a modification of *Inoue*'s disclosed apparatus would have been straightforward for a POSITA to implement because *Inoue* discloses an approach (e.g., regarding figure 6) in the context of a single bit line pair corresponding to a sense amplifier, and *Min* discloses a plurality of sense amplifiers coupled to respective bit line pairs. (Ex.1007, 3, FIG. 6; Ex.1008, FIG. 3B; Ex.1002, ¶77.)

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[10] A POSITA would have known at the time of the alleged invention that a practical DRAM device typically had multiple bit line pairs where each bit line pair corresponds to a column. (Ex.1002, ¶76; *see also* Ex.1001, 1:35-41, 2:15-16.)

Moreover, the sense amplifier in figure 6 of *Inoue* includes a flip-flop with internal nodes N_1, N_2 coupled to a bit line pair, and *Min* likewise discloses that each sense amplifier SA_i[11] is coupled to a bit line pair. (Ex.1007, FIG. 6; Ex.1008, FIG. 3B; Ex.1002, ¶77.) *Min* also teaches the use of a common driver signal for driving PMOS transistors $Q10_i$ of respective columns and another common driver signal for driving NMOS transistors $Q20_i$ of respective columns that are similar to transistors Q_{P3} and Q_{N10} in *Inoue* in that they couple the sense amplifier circuits to VDD and ground. (Ex.1008, FIG. 3; Ex.1002, ¶77.) A POSITA would have thus had reason and the capability to modify *Inoue* based on *Min* as noted above. (Ex.1002, ¶78.) A POSITA would have known how to modify *Inoue*'s circuit in ways that would ensure operation of the memory. (*Id.*)

Extending the teachings of *Inoue* to a context with a plurality of bit line pairs would not have negatively impacted the disclosed apparatus of *Inoue*, would have been a predictable combination of known components according to known methods (e.g., replication of *Inoue*'s approach of figure 6 across multiple columns as taught by *Min* at figure 3B), and would have been consistent with the known

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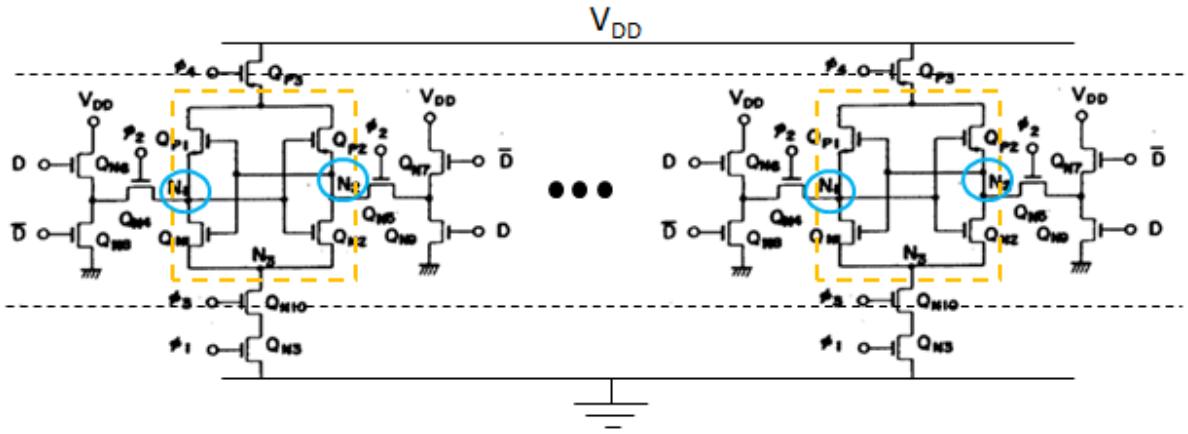
[11] *Min*'s sense amplifier SA_i has the same circuit configuration as the flip-flop in figure 6 of *Inoue*, i.e., the latch constituted by PMOS transistors Q_{P1} and Q_{P2} and NMOS transistors Q_{N1} and Q_{N2}. (Ex.1002, ¶76, n.7.)

features of working DRAMs that included multiple columns and multiple pairs of bit lines. (Ex.1002, ¶81.) *KSR*, 550 U.S. at 416.

In the above combined *Inoue-Min* system, there would have been a plurality of sense amplifiers with one sense amplifier corresponding to each column, where each sense amplifier ("for each of the plurality of sense amplifiers") is constituted by a latch circuit ("sense amplifier latch circuit") (orange below) having nodes N_1 and N_2 ("pair of nodes") (blue below) to which respective bit lines may be (and are) coupled. (Ex.1002, ¶82.)



(*Id.*, ¶82.)

The '574 patent discloses a similar configuration for a single column.

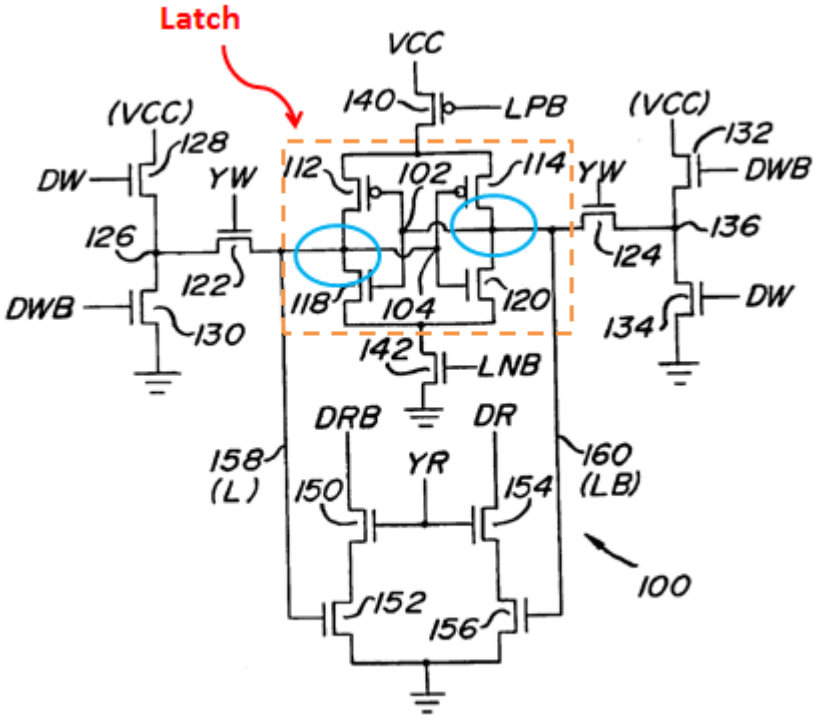


FIG. 5

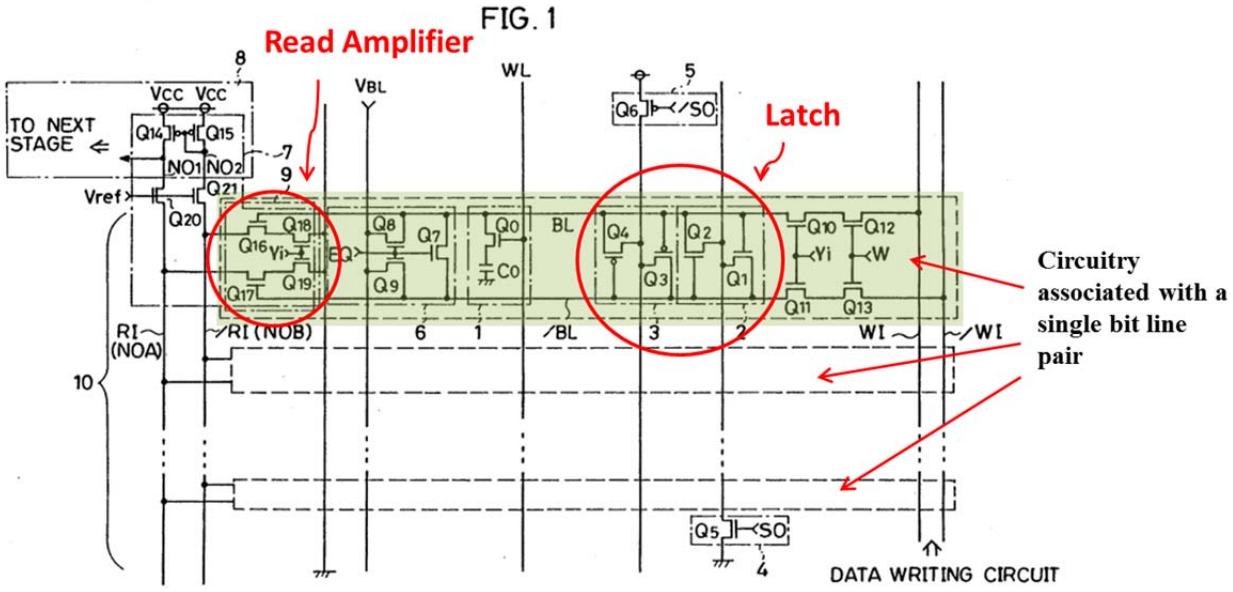
(Ex.1002, ¶83, citing Ex.1001, FIG. 5 (annotated).)

c) "[for each of the plurality of sense amplifiers,] a local column read amplifier responsively coupled to the sense amplifier, and receiving at least one data read signal; and"

The combined *Inoue-Min* system does not expressly disclose this feature. However, such a feature would have been obvious in view of *Hamade*. (Ex.1002, ¶¶84-99.)

Hamade, which is in the same field (semiconductor memory) as *Inoue* and *Min*, discloses circuitry for "implementing a high speed operation of semiconductor memory devices." (Ex.1009, 1:17-19.) Figure 1 of *Hamade* discloses a "main part of a semiconductor memory device." (Ex.1009, 7:10-12.)

The broken line in figure 1 of *Hamade* illustrates a "pair of bit lines BL and /BL," and circuitry associated with each bit line pair BL and /BL. (*Id.*, 3:1-5, 7:4-12, FIG. 1.)



(Ex.1002, ¶85, citing Ex.1009, FIG. 1 (annotated).)

The circuitry associated with each bit line pair in figure 1 includes an n-type sense amplifier 2 and a p-type sense amplifier 3. (Ex.1009, FIG. 1, 7:4-9, 1:47-52; Ex.1002, ¶¶26-33,86.) A POSITA would have understood that the sense amplifiers 2 and 3 collectively form a latch circuit like in *Inoue's* figure 6. (Ex.1002, ¶86.) Moreover, *Hamade* discloses that "a drive circuit 9 [] is provided for each bit line pair." (Ex.1009, 7:14-18, FIG. 1.) As explained immediately below, a POSITA would have also understood that drive circuit 9 (consisting of transistors Q16-Q19, *see id.*, FIG. 1) constitutes a "column read amplifier."

(Ex.1002, ¶¶87-89.) Because *Hamade* discloses that each bit line pair includes a drive circuit 9 associated with a single latch circuit (combination of sense amplifiers 2 and 3 in figure 1), *Hamade* discloses a "**local** column read amplifier" (emphasis added). (Ex.1009, FIG. 1 (annotated below), 7:4-23, 1:47-52, 3:1-5; *see supra* Section VIII.B; Ex.1002, ¶87.)

A POSITA would have understood that *Hamade*'s drive circuit 9 is a "column read amplifier" in the context of the '574 patent. (Ex.1002, ¶88.) Drive circuit 9 is part of a "read amplifier means 7" and "***amplifies*** the potentials of the associated bit lines." (Ex.1009, 7:14-19 (emphasis added); Ex.1002, ¶88.) Specifically, a POSITA would have understood that the combination of transistors Q16-Q19 (i.e., drive circuit 9) constitutes a "read amplifier" because they operate to amplify the potentials on bit lines BL and /BL during a read operation, and allow one of read only data lines Rl and /Rl to be discharged to ground during a read operation. (Ex.1009, 3:61-4:10, 8:8-31, 8:52-54; Ex.1002, ¶88.) Moreover, drive circuit 9 is provided for each ***column*** because it is provided for each bit line pair (Ex.1009, 7:22-23), which "is related to memory cells in one ***column*** of the memory cell array." (*Id*., 1:36-39 (emphasis added), 7:4-9.) Indeed, the "column read amplifier" in the '574 patent is a circuit similar to drive circuit 9 because it has two transistors 152 and 156 coupled to bit lines 158 and 160, and two other

transistors 150 and 154 whose conduction is controlled by a column read signal Y_R. (Ex.1001, 6:66-7:11; Ex.1002, ¶89.)

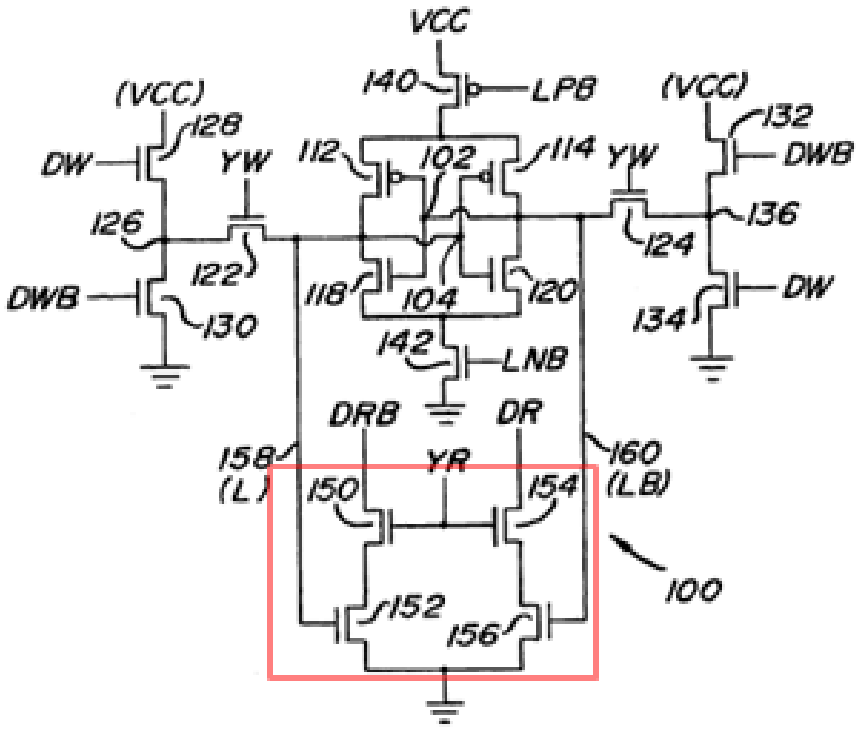
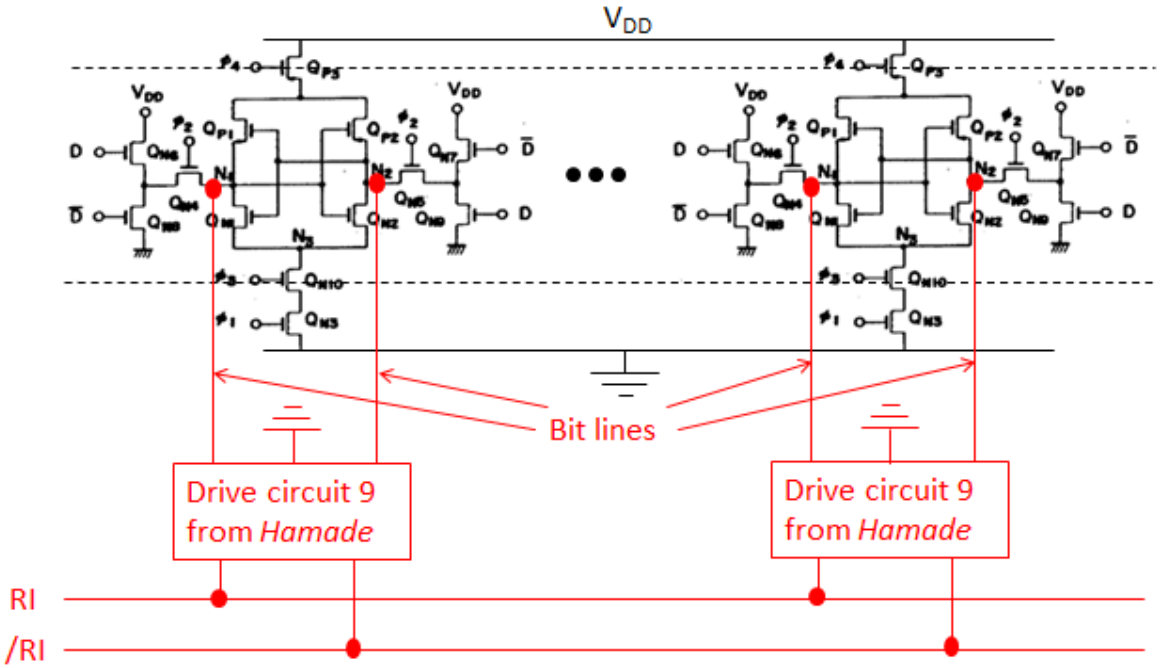


FIG. 5

(Ex.1002, ¶89, citing Ex.1001, FIG. 5 (annotated to show transistors 150, 152, 154, 156 which constitute a read amplifier).)

Based on the teachings of *Hamade*, a POSITA would have been motivated to modify the combined *Inoue-Min* system to implement *Hamade*'s drive circuit 9 at **each** column for **each** sense amplifier because *Hamade* discloses that "drive circuit 9 [ ] is provided for each bit line pair." (Ex.1009, 7:17-18; Ex.1002, ¶90.) In view of *Hamade*, a POSITA would have been motivated to implement read only data lines RI and /RI in the combined system in a manner similar to how they are

configured in figure 1 of *Hamade* (i.e., coupled to transistors Q17 and Q16, respectively), to support the functionality of the read amplifiers of respective columns. (Ex.1009, FIG. 1, 5:12-16; Ex.1002, ¶90.) As a non-limiting example, below is a demonstrative showing certain aspects of the combined *Inoue-Min-Hamade* system that a POSITA would have found to be consistent with the above modification. (Ex.1002, ¶90.)



(*Id.*, ¶90, citing Ex.1007, FIG. 6; Ex.1008, FIG. 3B; Ex.1009, FIG. 1 (annotated).)

Although not shown in the above demonstrative for visual simplicity, a POSITA would have also been motivated to implement in the combined *Inoue-Min-Hamade* system other circuitry associated with *Hamade*'s figure 1 configuration (e.g., transistors Q20/Q21, Q14/Q15), to ensure proper operation of

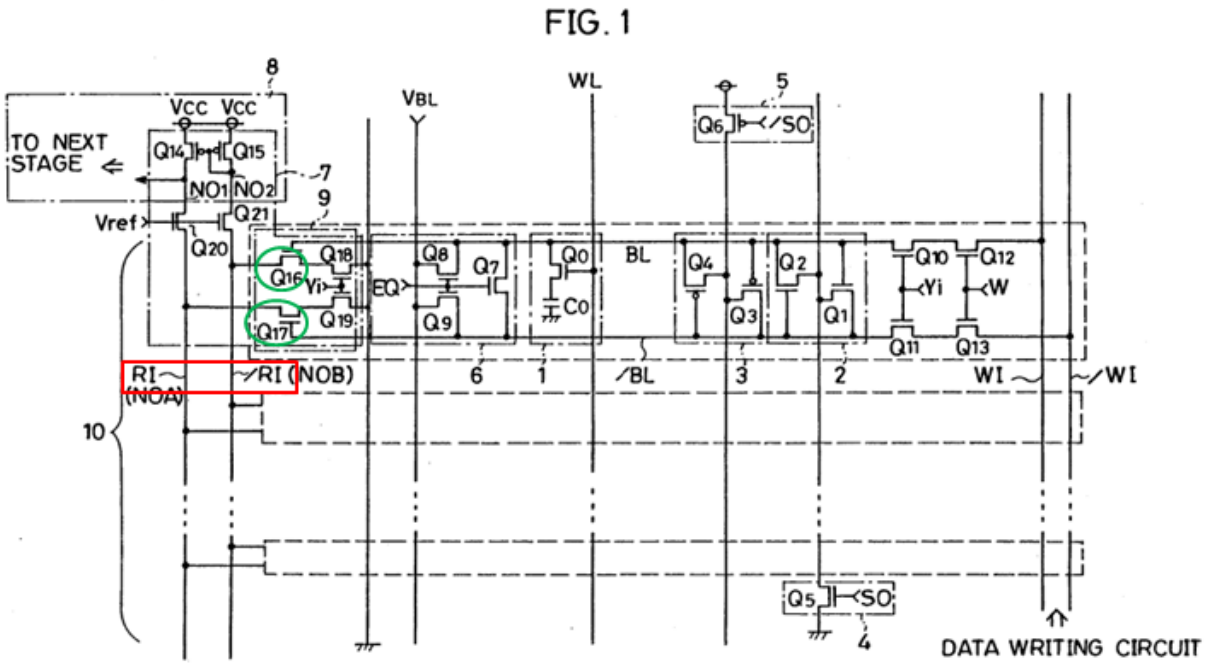
the memory in accordance with *Hamade*'s description of the figure 1 circuit. (Ex.1009, FIG. 1, 8:8-9:10; Ex.1002, ¶93.)

As shown in the above exemplary demonstrative, the combined *Inoue-Min-Hamade* system discloses, a "local column read amplifier" "for each of a plurality of sense amplifiers," as there is a read amplifier (drive circuit 9) for each sense amplifier and corresponding column, and each column read amplifier is associated with only one latch circuit. (*See supra* Section VIII.B.; Ex.1002, ¶94.)

A POSITA would have further understood that drive circuit 9, as implemented in the combined *Inoue-Min-Hamade* system at each column, would have included the gates of NMOS transistors Q16 and Q17 (green below) coupled to nodes N_1 and N_2 of figure 6 of *Inoue*, respectively, because gates of transistors Q17 and Q16 in drive circuit 9 receive the bit line signals (Ex.1009, FIG. 1), and *Inoue*'s N_1 and N_2 correspond to bit lines for each sense amplifier in the *Inoue-Min-Hamade* system. (Ex.1009, FIG. 1; Ex.1007, 3, 4, FIG. 6; *See supra* Section IX.A.1(b); Ex.1002, ¶95.) Therefore, the combined system further discloses, for each sense amplifier of the plurality of sense amplifiers, "a local column read amplifier **responsively coupled to the sense amplifier**" (emphasis added). (Ex.1002, ¶95.)

Moreover, as is again shown in the demonstrative above, the drive circuit 9 ("local column read amplifier") would receive signals on read only data lines RI

and /RI ("receiving at least one data read signal") in the combined system. (*See* Ex.1009, FIG. 1 (annotated below), 7:35-39; Ex.1002, ¶96.)



(Ex.1002, ¶96, citing Ex.1009, FIG. 1 (annotated to illustrate the connection between read only data lines RI and /RI with transistors Q16 and Q17 of drive circuit 9).)

A POSITA would have found it obvious to combine the teachings of *Inoue*, *Min*, and *Hamade* as discussed above. A POSITA would have looked to *Hamade* to augment and improve the capabilities of the combined *Inoue-Min* system, because *Hamade* is in the same field as *Inoue* and *Min* and teaches circuitry and functionality applicable to a column of a memory such as in the combined *Inoue-Min* system. (Ex.1002, ¶97.) A POSITA would have recognized the

configurations of these references are similar and conducive to combination with one another as described herein. (*Id*.)

A POSITA would have been motivated to modify the combined *Inoue-Min* system to implement circuitry from *Hamade*'s figure 1 because the combined *Inoue-Min* system does not disclose read circuitry for reading data carried by the bit lines that would typically be found in a practical DRAM. (Ex.1002, ¶98.) Therefore, in the interest of making a practical DRAM, a POSITA would have found it advantageous to include in the combined *Inoue-Min* system circuitry similar to *Hamade*'s circuitry that allows for reading of the data carried by the bit lines, and hence, the combination would have been obvious. *See KSR*, 550 U.S. at 416-17. The benefit of doing so would have been allowing fast reading of the data carried by the bit lines as disclosed by *Hamade*. (Ex.1009, 1:24-30, 5:11-16, 8:37-42; Ex.1002, ¶98.)

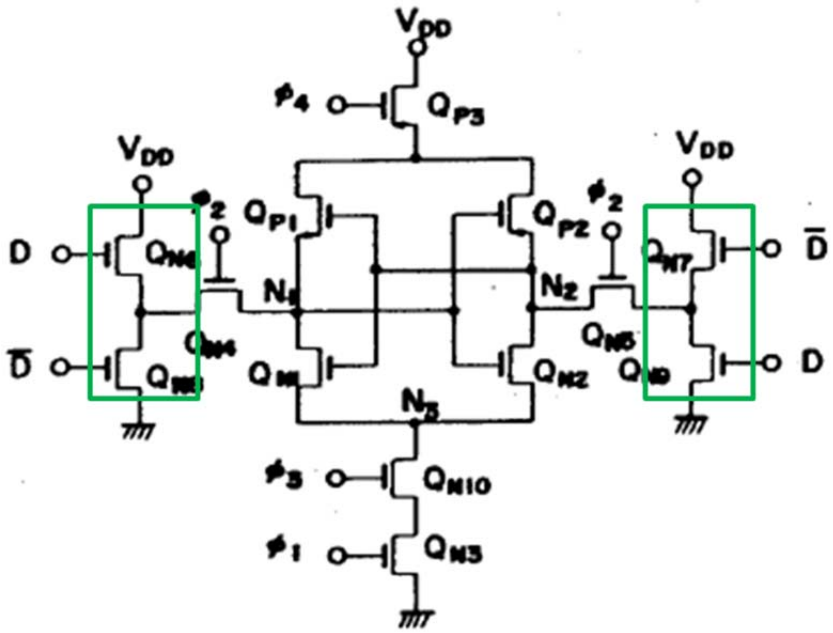
Moreover, a POSITA would have understood that the above modification of the *Inoue-Min* system based on *Hamade* would have been merely a combination of known components (e.g., circuitry for a multi-column memory as in the combined *Inoue-Min* system, and a drive circuit 9 for a given column and related circuitry such as read only data lines RI, /RI as taught by *Hamade*) according to known methods (e.g., *Hamade* teaches how to implement the drive circuit 9 for a given column because it shows how to connect the drive circuit to a latch circuit at bit

lines corresponding to that column) to yield predictable results (e.g., faster read operations as taught by *Hamade*). (Ex.1002, ¶99.) *See KSR*, 550 U.S. at 416.

d) **"**[for each of the plurality of sense amplifiers,] a local data write driver circuit coupled to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶100.) *Inoue* discloses that "Q_{N5}, Q_{N7}, Q_{N9} and Q_{N4}, Q_{N6}, Q_{N8} are write circuits that determine the state of the F/F." (*Id*.; Ex.1007, 3, FIG. 6.) The inputs to circuits Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9}, i.e., "D, $\overline{D}$ [are] write data input terminals used to write data to F/F," where F/F refers to a flip-flop. (Ex.1007, 3; Ex.1002, ¶100.) Therefore, a POSITA would have understood that transistor pairs Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} each constitute a data write driver circuit. (Ex.1002, ¶100.)

第 6 図



(Ex.1002, ¶100, citing Ex.1007, FIG. 6 (annotated to show data write driver circuits (green).)

The ’574 patent discloses a similar configuration. (Ex.1002, ¶101.)

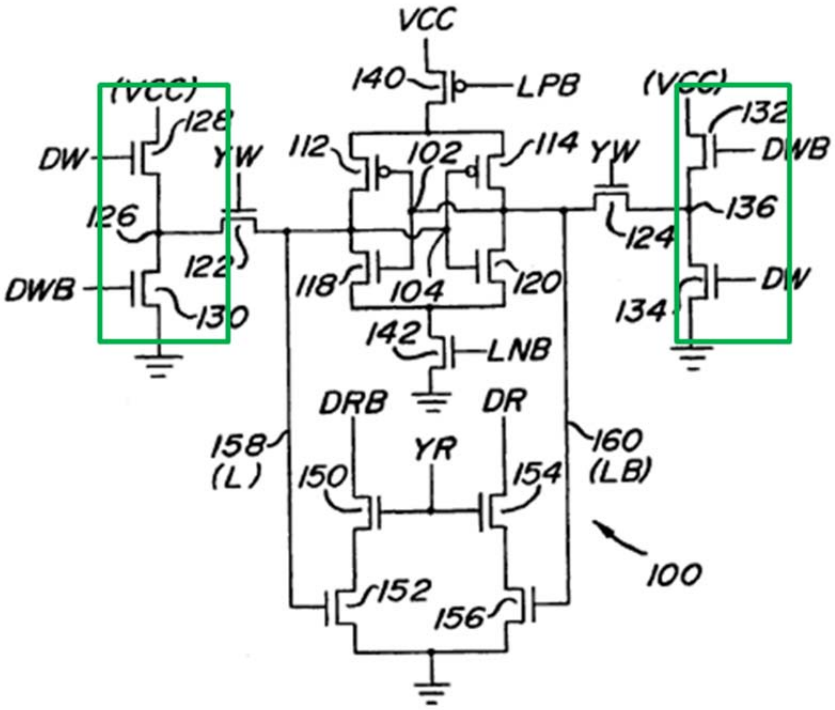
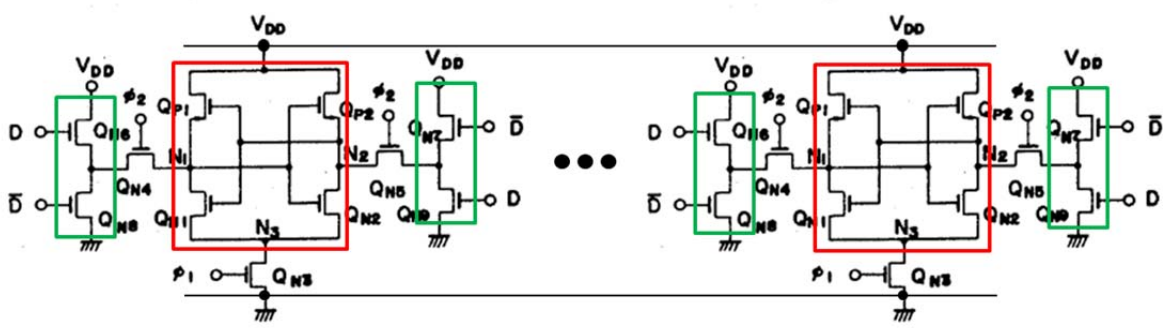


FIG. 5

(*Id*., ¶101, citing Ex.1001, FIG. 5 (annotated to show data write driver circuits (green).)

Moreover, as seen in the annotated figure below, in the combined *Inoue-Min-Hamade* system discussed above for limitation 4(c), each latch circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) and therefore, each "sense amplifier," is coupled to only one pair of data write driver circuits that includes Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9}. (*See* annotated figure below.) (Ex.1002, ¶102.) Thus, the combined *Inoue-Min-Hamade* system includes a plurality of sense amplifiers and each sense amplifier has a corresponding pair of data write driver circuits. (*Id*.) Therefore, transistor

pairs Q_{N6}, Q_{N8}, and Q_{N7}, Q_{N9} each constitute "a **local** data write driver circuit." (*Id.*; *see also supra* Section VIII.A.)



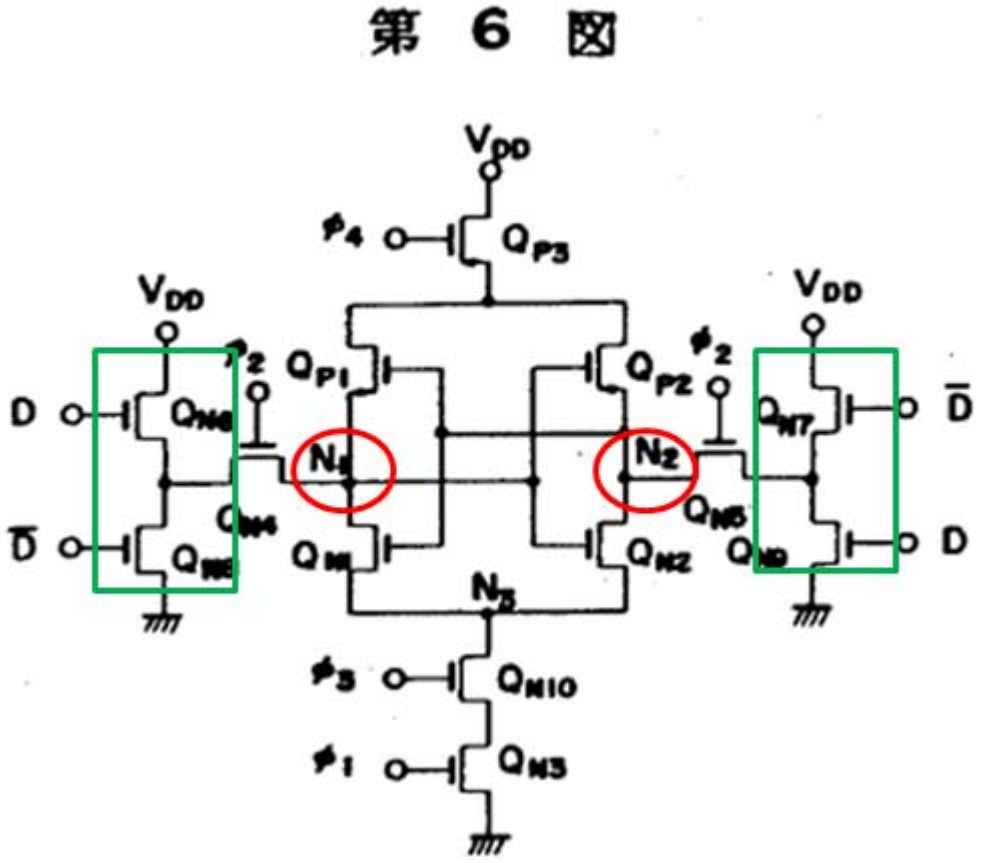
(Ex.1002, ¶102, annotated to show sense amplifiers (each of which is constituted by a "latch circuit") in red and circuitry corresponding to claimed local data write driver circuits in green.[12])

Each of the local data write driver circuits at each column in the combined *Inoue-Min-Hamade* system would have been coupled to (1) receive data at their gate terminals D and $\overline{D}$ ("receive write data") during a write operation at a gate electrode of a transistor Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("a transistor in said data write driver circuit") in said data write driver circuit, and (2) apply a signal corresponding to a level 'H' or 'L' ("apply a signal") based upon receiving data D or $\overline{D}$ ("based upon

[12] The read amplifier circuitry for each column is not shown for visual simplicity. here and in other sections where the combined *Inoue-Min-Hamade* system is referenced.

receiving said write data") to node N_1 or N_2 of the latch circuit ("one of said latch circuit nodes") (red below). (Ex.1007, FIG. 6; Ex.1002, ¶103.)

Referring to figure 6 of *Inoue* (shown below) for a given column of the combined *Inoue-Min-Hamade* system, terminals D and $\overline{D}$ are "write data input terminals used to write data to [the flip-flop]" (Ex.1007, 3), with D coupled to the gate of transistors Q_{N6} and Q_{N9}, and with $\overline{D}$ coupled to the gate of transistors Q_{N8} and Q_{N7}. (Ex.1002, ¶104.) Accordingly, the combined *Inoue-Min-Hamade* system discloses, for each sense amplifier of a plurality of sense amplifiers, "a local data write driver circuit coupled to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit." (*Id*.)



(*Id.*, ¶104, citing Ex.1007, FIG. 7 (annotated).)

In addition, *Inoue* discloses that "terminals D and $\overline{D}$ write to the nodes N_1 and N_2" based on the signal received at terminal D and $\overline{D}$. (Ex.1002, ¶105; Ex.1007, 3.) Accordingly, the combined *Inoue-Min-Hamade* system discloses "a local data write driver circuit coupled . . . to apply a signal based upon receiving said write data to one of said latch circuit nodes." (Ex.1002, ¶105.)

The '574 patent discloses a similar configuration for a given column. (Ex.1001, 6:38-52, 7:50-52, FIG. 5; Ex.1002, ¶106.)

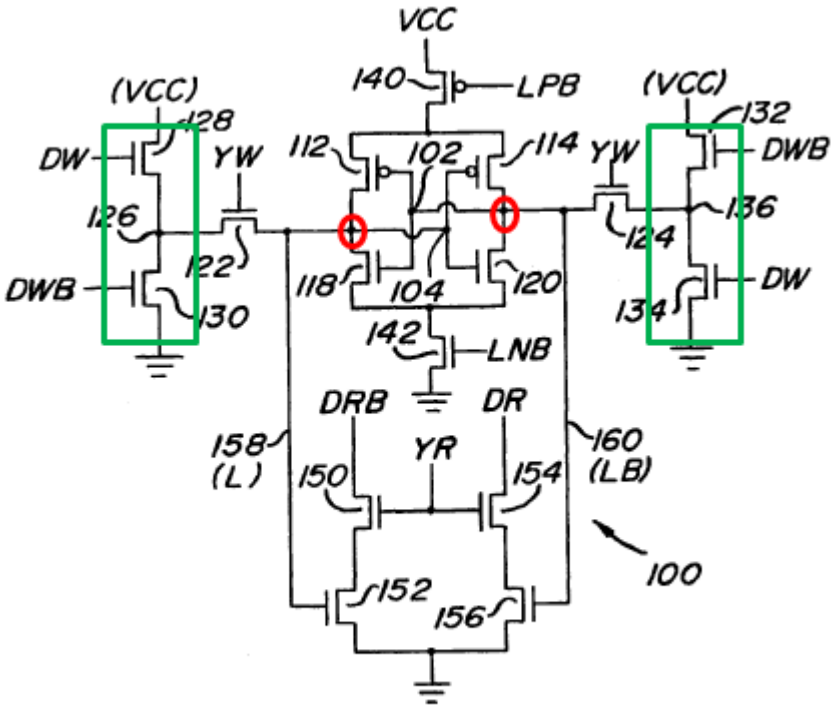


FIG. 5

(Ex.1002, ¶106, citing Ex.1001, FIG. 5 (annotated).)

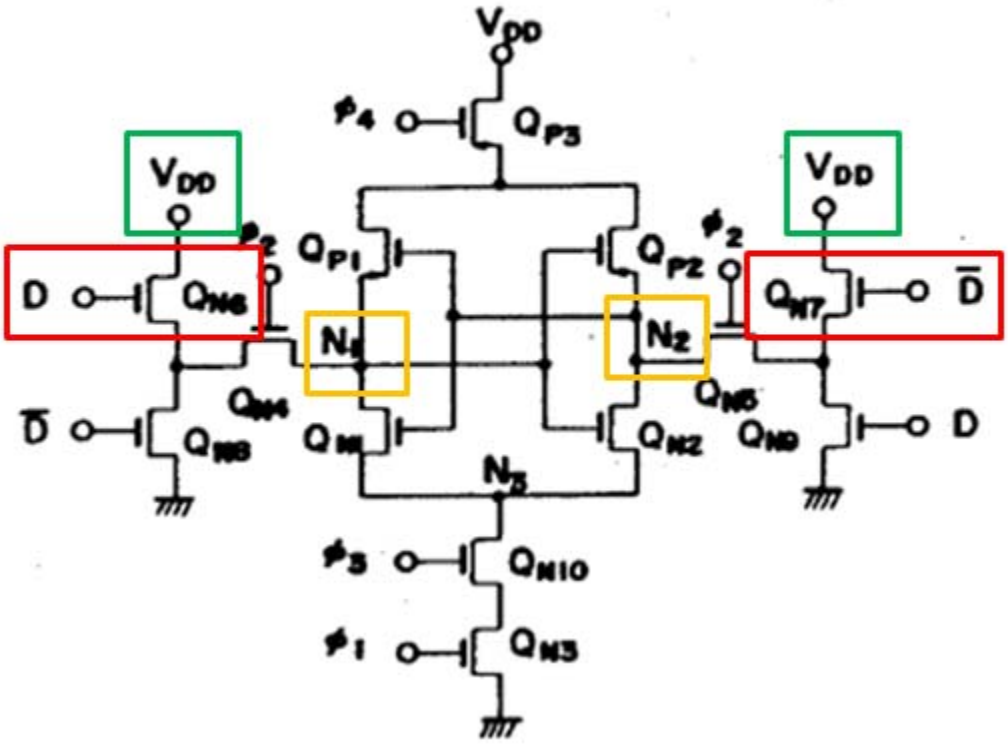
2. Claim 5

a) "The sense amplifier arrangement of claim 4 wherein said local data write driver circuit includes a first transistor coupled between a power supply voltage and one of said latch circuit nodes, said transistor being responsively coupled to a first data write signal."

In the combined *Inoue-Min-Hamade* system discussed above for limitation 4(d), transistor pairs Q_{N6} and Q_{N8}, and Q_{N7} and Q_{N9} from *Inoue* figure 6 constitute a "local data write driver circuit." The "local data write driver circuit" includes a transistor Q_{N6} or Q_{N7} (each of which is "a first transistor") (red below) coupled between V_{DD} ("a power supply voltage") (green below) and node N_1 or N_2 ("one of

said latch circuit nodes") (orange below), where transistors Q_{N6} and Q_{N7} ("said transistor") have their gate terminals coupled ("responsively coupled") to write data input terminals D and $\overline{D}$ (each of which receives "a first data write signal") (red below), respectively. (*See supra* Sections IX.A.1(c),(d); Ex.1002, ¶107; Ex.1007, 3, FIG. 6.)

第 6 図



(Ex.1002, ¶107, citing Ex.1007, FIG. 6 (annotated).)

Inoue discloses that transistors Q_{N6}/Q_{N7} ("said transistor") are each "responsively coupled to a first data write signal" because the gate terminals of transistors Q_{N6} and Q_{N7} are coupled to signals D and $\overline{D}$, respectively, which are

"write data input terminal[] used to write data." (Ex.1007, 3, FIG. 6; Ex.1002, ¶¶108-109.)

The '574 patent discloses a similar configuration. (Ex.1002, ¶110.)

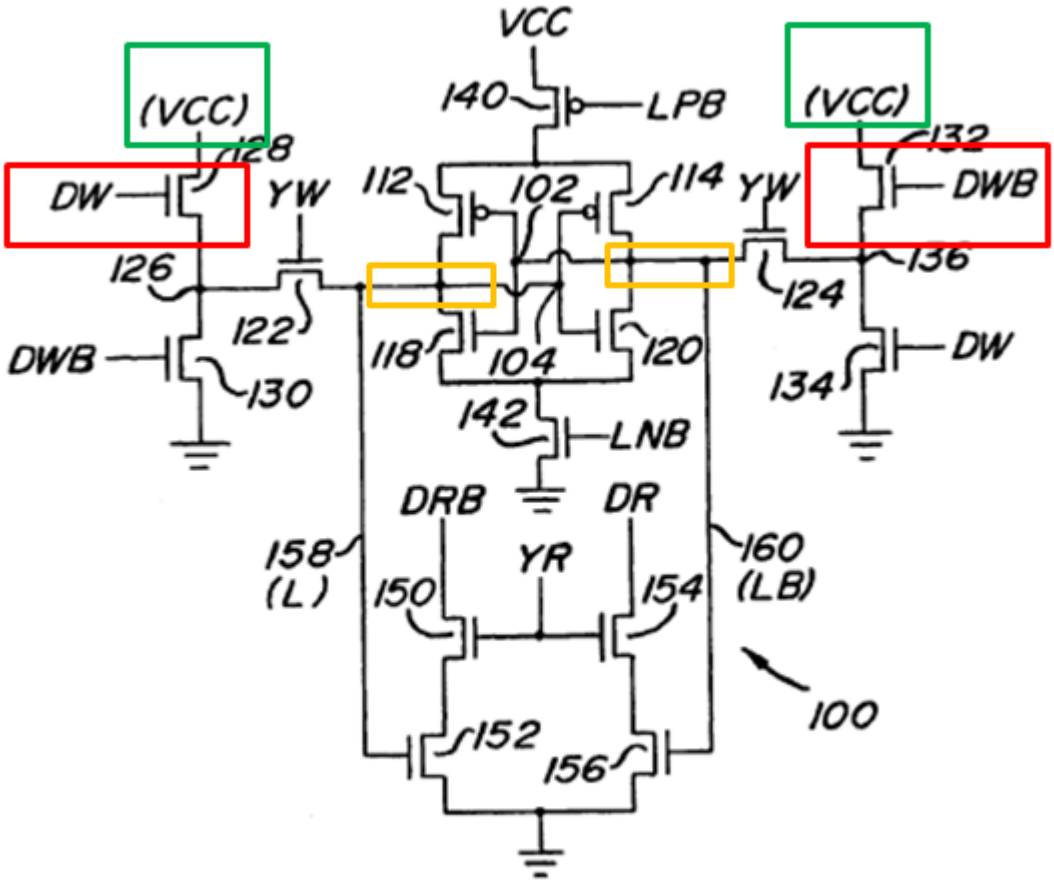


FIG. 5

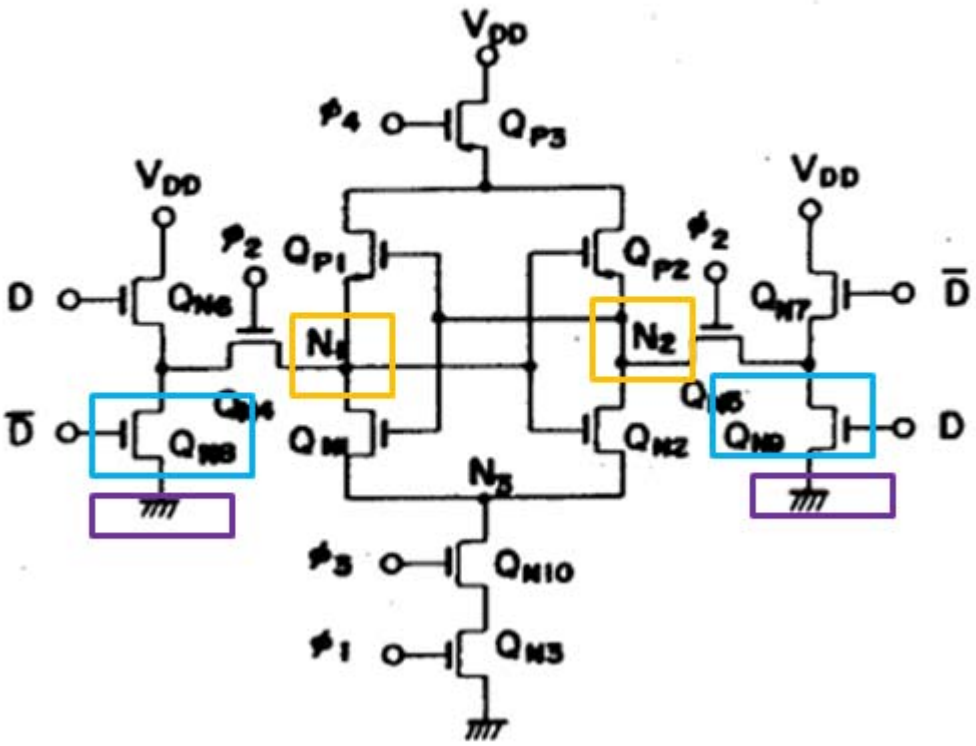
(*Id*., ¶110, citing Ex.1001, FIG. 5 (annotated).)

3. Claim 6

a) "The sense amplifier arrangement according to claim 5 wherein said local data write driver circuit further comprises a second transistor connected between another power supply voltage and said one latch node."

In the combined *Inoue-Min-Hamade* system discussed above for limitation 4(d), transistor pairs Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} from *Inoue* figure 6 constitute a "local data write driver circuit." The "local data write driver circuit" includes a transistor Q_{N8} or Q_{N9} (each of which is "a second transistor") (blue below) connected between a ground node ("another power supply voltage") and one of nodes N_1/N_2 ("said one latch node"). (*See supra* Sections IX.A.1(c),(d),IX.A.2; Ex.1002, ¶111; Ex.1007, 3, FIG. 6.)

第 6 図



(Ex.1002, ¶111, citing Ex.1007, FIG. 6 (annotated).)

The ’574 patent discloses a similar configuration. (Ex.1002, ¶112.)

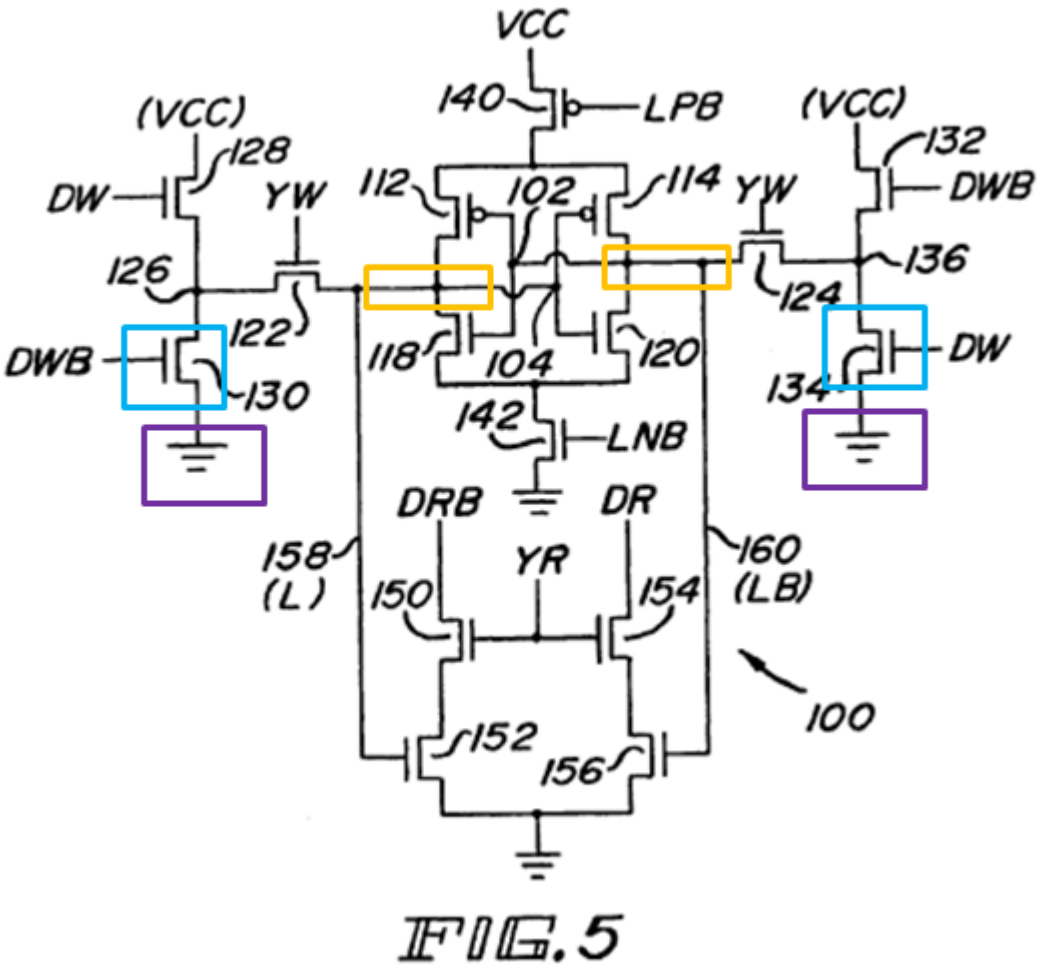


FIG. 5

(*Id.*, ¶112, citing Ex.1001, FIG. 5 (annotated).)

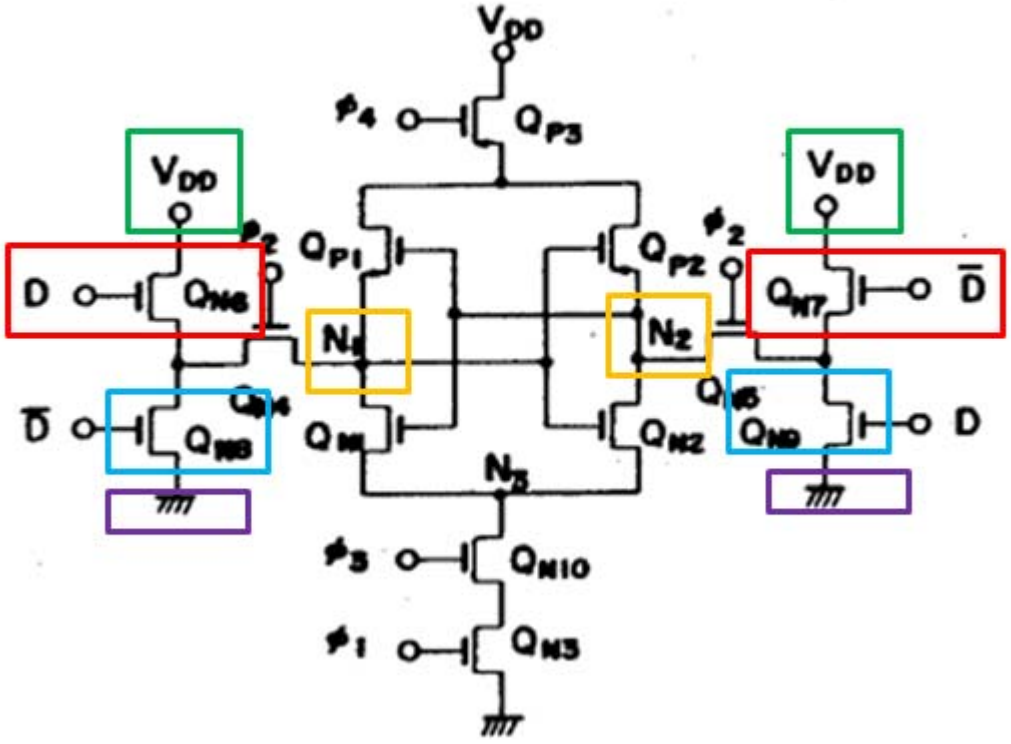
4. Claim 7

a) "The sense amplifier arrangement of claim 4 wherein said local data write driver circuit includes first and second transistors each coupled between a corresponding node of the latch and a respective power supply voltage."

In the combined *Inoue-Min-Hamade* system discussed above for limitation 4(d), transistor pairs Q_{N6} and Q_{N8}, and Q_{N7} and Q_{N9} from *Inoue* figure 6 constitute a "local data write driver circuit." The "local data write driver circuit" includes a

transistor Q_{N6} or Q_{N7} ("first . . . transistor[]") (red below) and a transistor Q_{N8} or Q_{N9} ("second transistor[]") (blue below) each coupled between node N_1 or N_2 ("a corresponding node of the latch") (orange below) and either V_{DD} (green below) or ground (purple below) ("a respective power supply voltage"). (*See Supra*, Sections IX.A.1(c),(d),IX.A.2-3; Ex.1007, 3, FIG. 6; Ex.1002, ¶113.)

第 6 図



(Ex.1002, ¶113, citing Ex.1007, FIG. 6 (annotated).)

The '574 patent discloses a similar configuration.

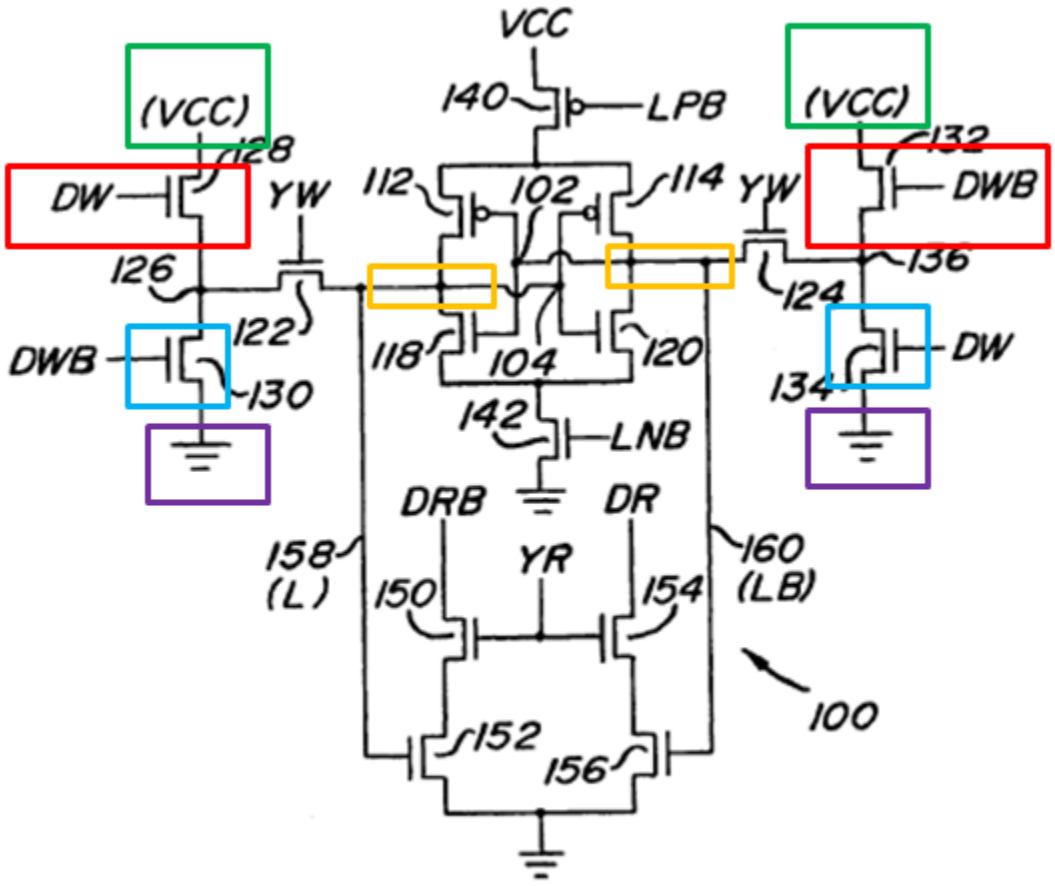


FIG. 5

(Ex.1002, ¶114, citing Ex.1001, FIG. 5 (annotated).)

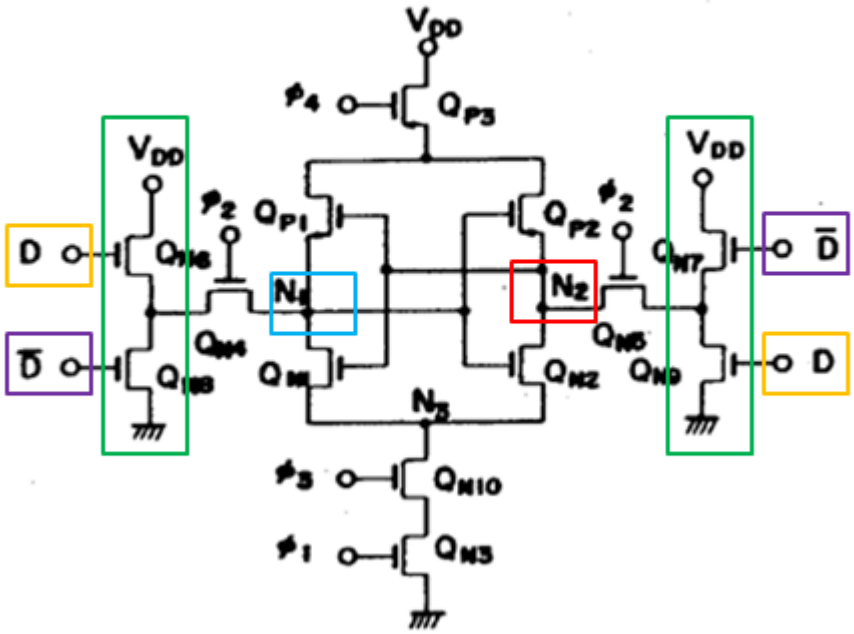
5. Claim 8

a) "The sense amplifier arrangement of claim 4 wherein said local data write driver circuit comprises a pair of local data write driver circuits, each coupled to a respective node of said latch, each data write driver circuit being responsively coupled to a corresponding data write signal."

In the combined *Inoue-Min-Hamade* system discussed above for limitation 4(d), each sense amplifier is coupled to a first pair of transistors Q_{N6}/Q_{N8} (a first "local data write driver circuit") and a second pair of transistors Q_{N7}/Q_{N9} (a second

"local data write driver circuit") (collectively, "a pair of local data write driver circuits"; green below), each coupled to a node N_1 (blue below) or N_2 (red below) of the flip-flop ("respective node of said latch"), each "data write driver circuit" including a transistor coupled at its gate to write data input terminal D (orange below) or $\overline{D}$ (purple below) ("responsively coupled to a corresponding data write signal"). (*See supra*, Sections IX.A.1(d), IX.A.2, IX.A.3; Ex.1007, 3, FIG. 6.)

第 6 図



(Ex.1002, ¶115, citing Ex.1007, FIG. 6 (annotated).)

For a given column in the combined *Inoue-Min-Hamade* system, *Inoue* discloses the "responsively coupled" and "corresponding data write signal" limitations for the reasons discussed above for claim 5. (Ex.1002, ¶116; *see Supra*, Section IX.A.2.)

The '574 patent discloses a similar configuration.

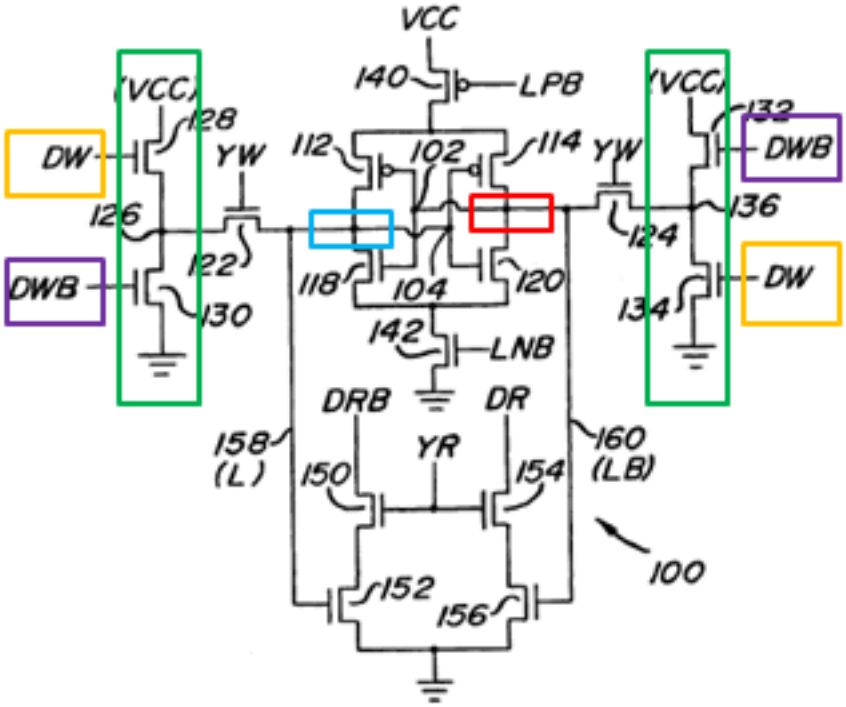


FIG. 5

(Ex.1002, ¶117, citing Ex.1001, FIG. 5 (annotated).)

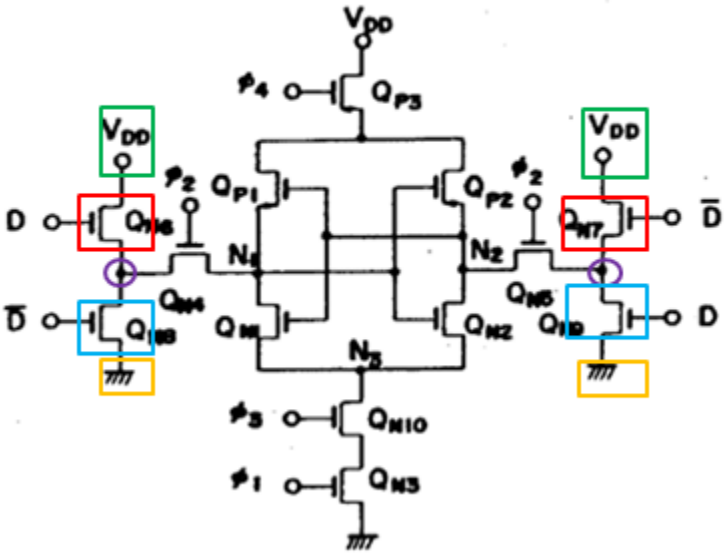
6. Claim 9

a) "The sense amplifier arrangement according to claim 8 wherein each of said local data write driver circuits comprises a pull-up transistor and a pull-down transistor having their source-drain paths coupled in series and forming an output node therebetween, said output node being coupled to the corresponding node of the latch circuit, said source-drain paths being coupled between first and second voltages."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶¶118-120.) Each of the first and second "local data write driver

circuits" include a transistor Q_{N6} or Q_{N7} ("pull-up transistor") (red below), and a transistor Q_{N8} or Q_{N9} ("pull-down transistor") (blue below) having their source-drain paths coupled in series and forming an output node (purple below) therebetween, the output node being coupled to the node N_1 or N_2 ("the corresponding node") of the flip-flop ("latch circuit"), and the source-drain paths of the pull-up and pull-down transistors being coupled between V_{DD} and ground ("first and second voltages"; shown below in green and orange, respectively). (Ex.1007, 3, FIG. 6; *see also Supra*, Section IX.A.5.)

第 6 図



(Ex.1002, ¶118, citing Ex.1007, FIG. 6 (annotated).)

One of ordinary skill in the art would have understood that Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} have their source-drain paths connected in series just like the source-drain paths are connected in series for transistors 128 and 130 in the '574 patent. (*See*

Ex.1001, 6:35-36.) Moreover, the output node (purple above) of circuits Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} is connected to nodes N1 and N2 when Q_{N4} and Q_{N5} become conducting. (Ex.1007, 3; Ex.1002, ¶¶26-33,119-120.)

The '574 patent discloses a similar configuration.

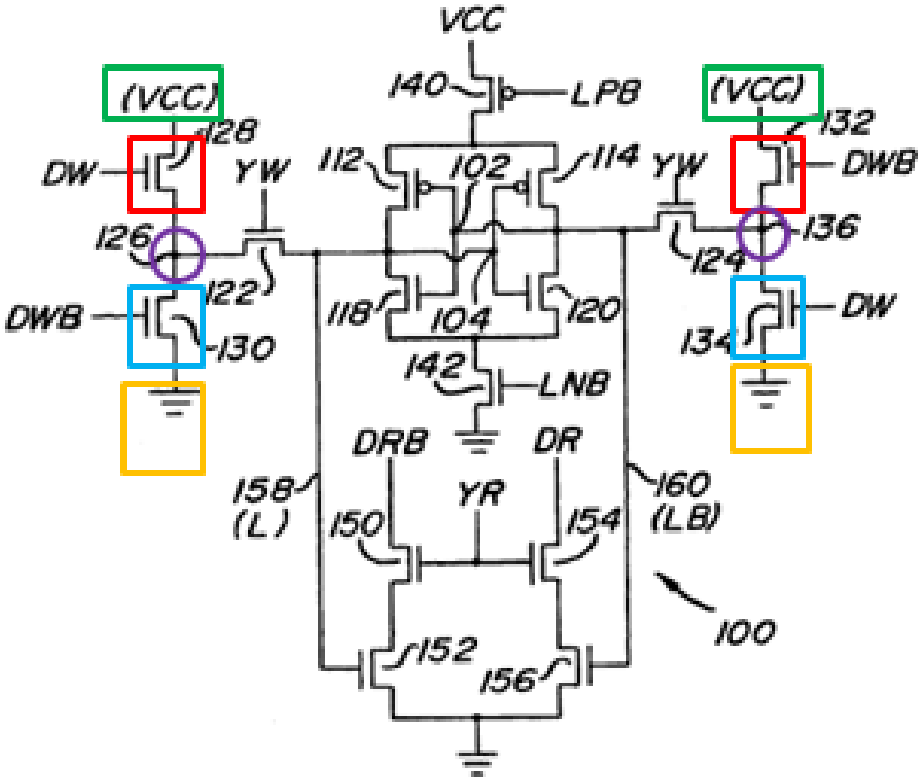


FIG. 5

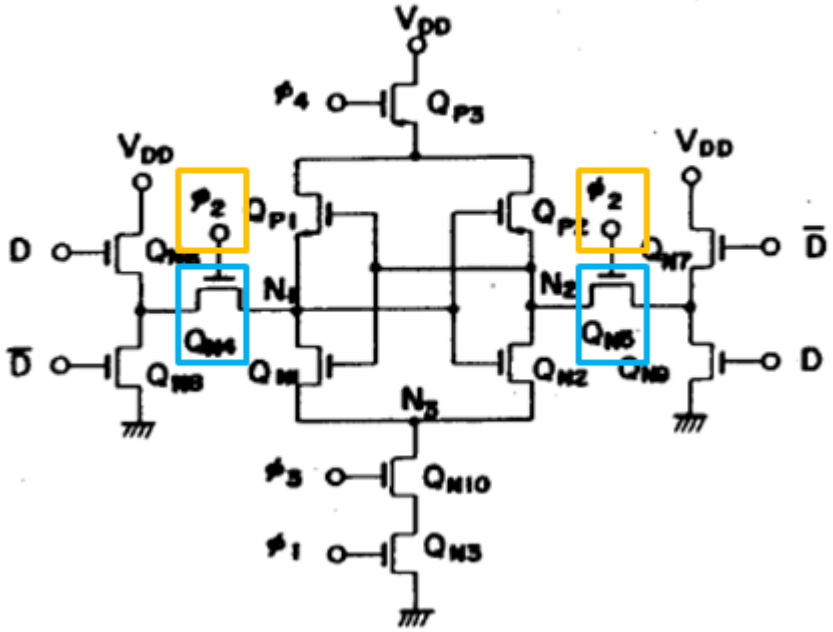
(Ex.1002, ¶121, citing Ex.1001, FIG. 5 (annotated).)

7. Claim 10

a) "The sense amplifier arrangement according to claim 9, further comprising: first and second pass transistors, said first pass transistor being coupled between one said latch circuit node and one said local data write driver circuit, said second pass transistor being coupled between another said latch circuit node and the other said local data write driver circuit of the pair of write driver circuits; each said pass transistor being responsively coupled to a write control signal."

In the combined *Inoue-Min-Hamade* system discussed above for limitation 4(d), the circuit of figure 6 in *Inoue* is replicated for each column. (*See Supra*, Sections IX.A.1(b),(c),(d).) The circuit of figure 6 in *Inoue* includes transistors Q_{N4} and Q_{N5} ("first and second pass transistors") (green below), with transistor Q_{N4} ("said first pass transistor") being coupled between node N_1 ("one said latch node") and the circuit comprising transistors Q_{N6} and Q_{N8} ("one said local data write driver circuit"), and with transistor Q_{N5} ("said second pass transistor") being coupled between node N_2 ("another said latch circuit node") and the circuit comprising transistors Q_{N7} and Q_{N9} ("the other said local data write driver circuit of the pair of write driver circuits"), wherein each of transistors Q_{N4}/Q_{N5} ("each said pass transistor") is coupled at its gate ("responsively coupled") to "write control clock ϕ_2." (Ex. 1002, ¶122; Ex.1007, 4; s*upra*, Section IX.A.1(d).)

第 6 図



(Ex.1002, ¶122, citing Ex.1007, FIG. 6 (annotated.)

A POSITA would have understood that with respect to each column above, each of transistors Q_{N4}/Q_{N5} is a "pass transistor" because, for example, when operating in a conducting state, each of transistors Q_{N4}/Q_{N5} would have allowed current to flow (pass) into and out of nodes N_1 (Q_{N4}) or N_2 (Q_{N5}). (Ex.1007, 3; Ex.1002, ¶123.) *Inoue* discloses that clock ϕ_2, which is provided to the gate terminal of transistors Q_{N4} and Q_{N5} as shown in figure 6, controls the conductivity of those transistors and is used for writing to nodes N_1 and N_2. (Ex.1007, 3.) Therefore, a POSITA would have understood that ϕ2 is a "write control signal" to which each of transistors QN4/QN5 is "responsively coupled." (Ex.1002, ¶124.)

The '574 patent discloses a similar configuration.

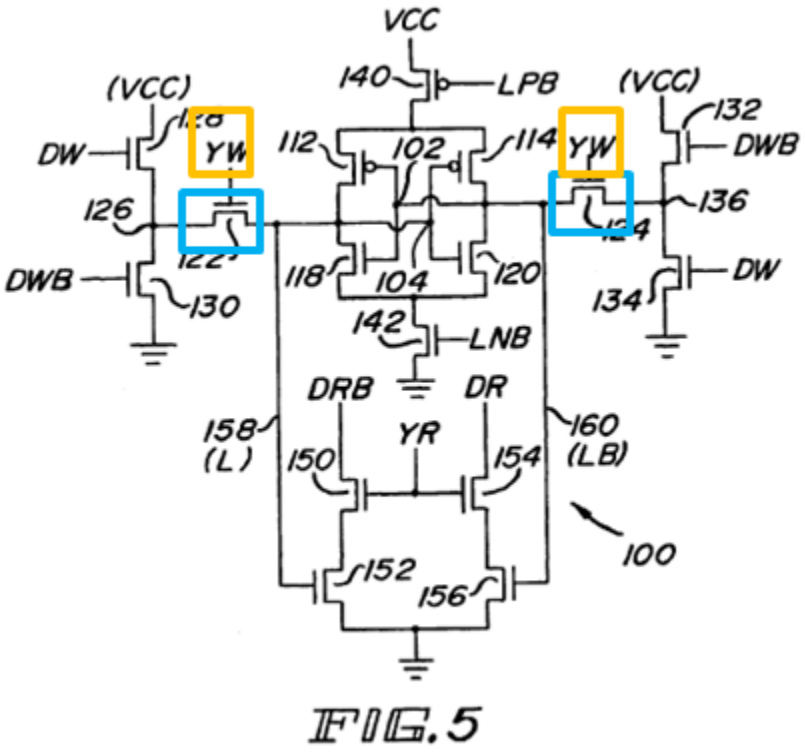


FIG. 5

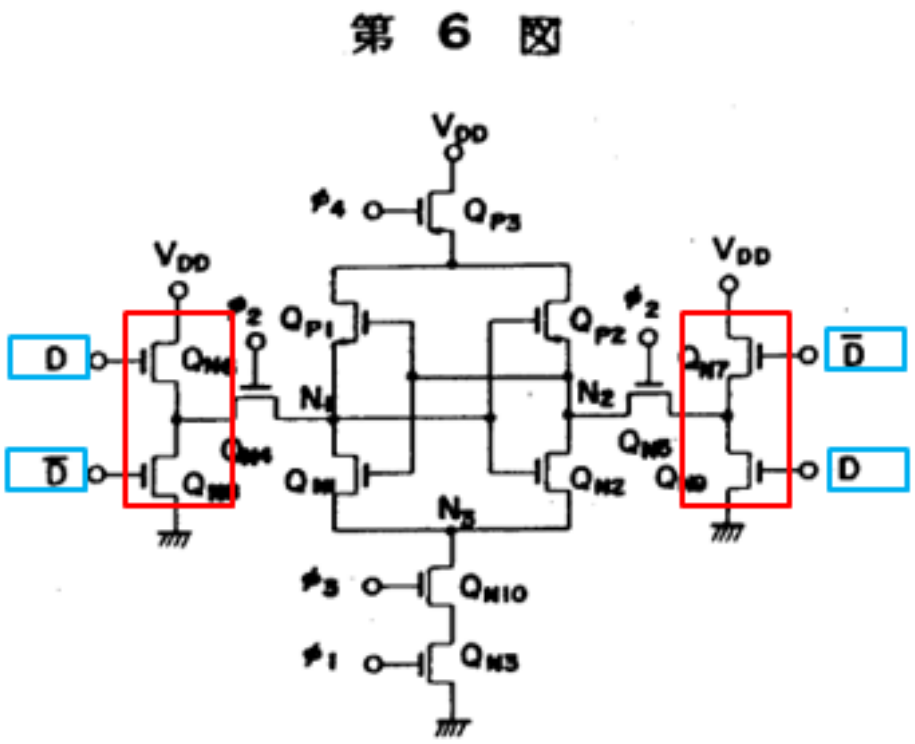
(Ex.1002, ¶125, citing Ex.1001, FIG. 5 (annotated).)

8. Claim 14

a) "The sense amplifier arrangement according to claim 9 wherein said local data write driver circuits receive said data write signals at control terminals of said pull-up and pull-down transistors."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶126.) For instance, the data write driver circuit comprising transistors Q_{N6}/Q_{N8} and the data write driver circuit comprising transistors Q_{N7}/Q_{N9} ("said local data write driver circuits") (red below) receive write signals D and $\overline{D}$ ("said data write signals") (blue below) at the gates ("control terminals") of transistors

Q_{N6} or Q_{N7} ("said pull-up [transistors]") and transistors Q_{N8} or Q_{N9} ("[said] pull-down transistors"). (Ex.1007, 3, FIG. 6; *supra*, IX.A.6.)



(Ex.1002, ¶126, citing Ex.1007, FIG. 6 (annotated).)

The '574 patent discloses a similar configuration.

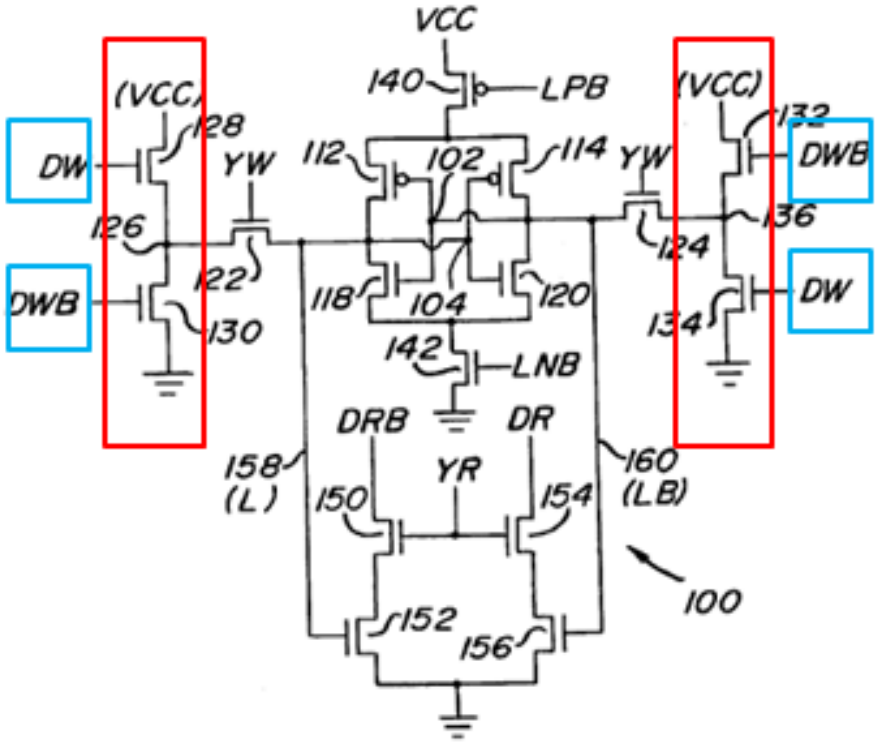


FIG. 5

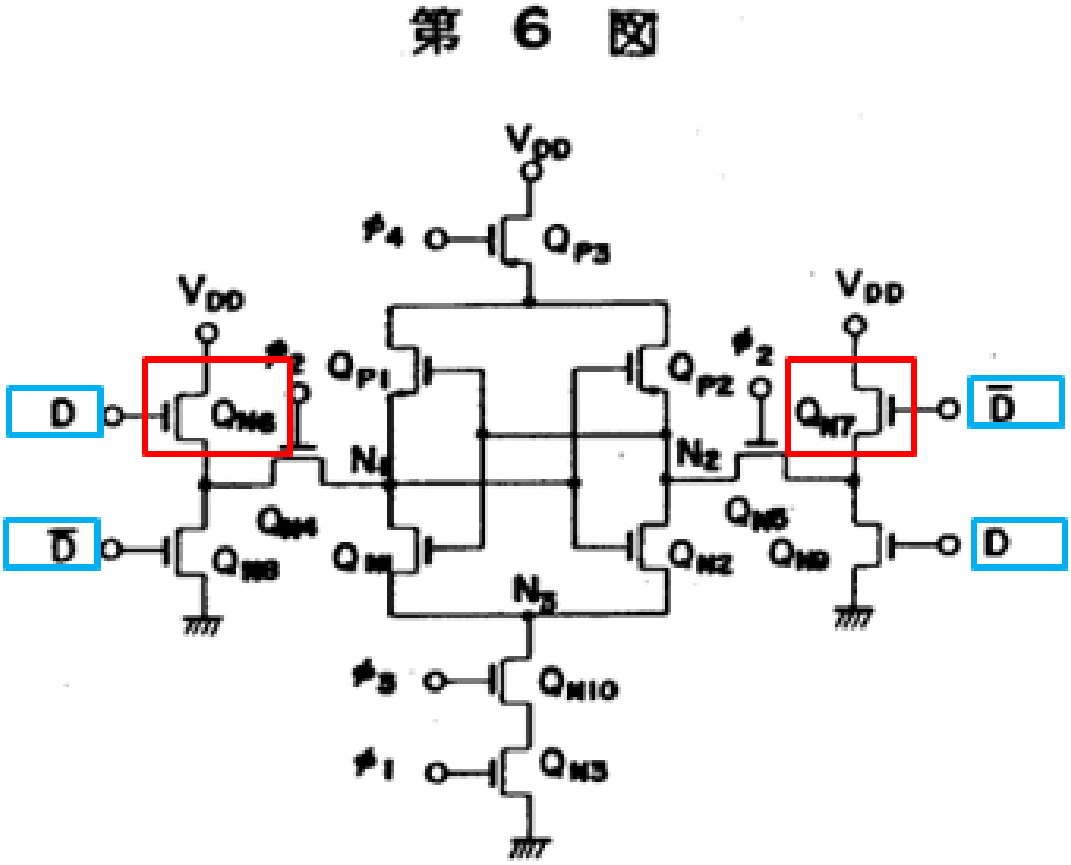
(Ex.1002, ¶127, citing Ex.1001, FIG. 5 (annotated).)

9. Claim 15

a) "The sense amplifier arrangement according to claim 14 wherein said data write signals comprise first and second data write signals; and wherein one said pull-up transistor in the local data write circuits for the corresponding latch circuit receives the first data write signal and the other said pull-up transistor receives the second data write signal."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶128.) *Inoue* discloses, for example, signals D and $\overline{D}$ ("first and second data write signals," respectively) (blue below) that are received by transistors Q_{N6}

("one said pull-up transistor in the local data write circuits for the corresponding latch circuit") and Q_{N7} ("the other said pull-up transistor"), respectively (red below). (*Supra*, Sections IX.A.1(c),(d),IX.A.6,8; Ex.1007, 3, FIG. 6.)



(Ex.1002, ¶128, citing Ex.1007, FIG. 6 (annotated).)

The '574 patent discloses a similar configuration.

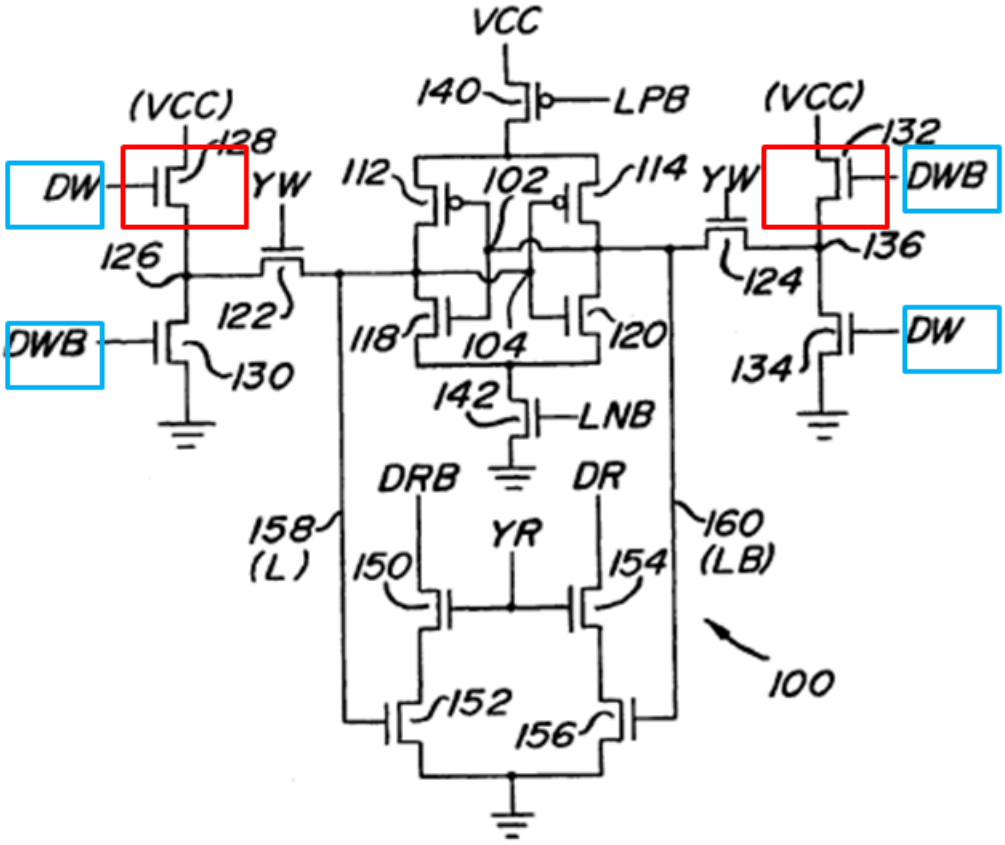


FIG. 5

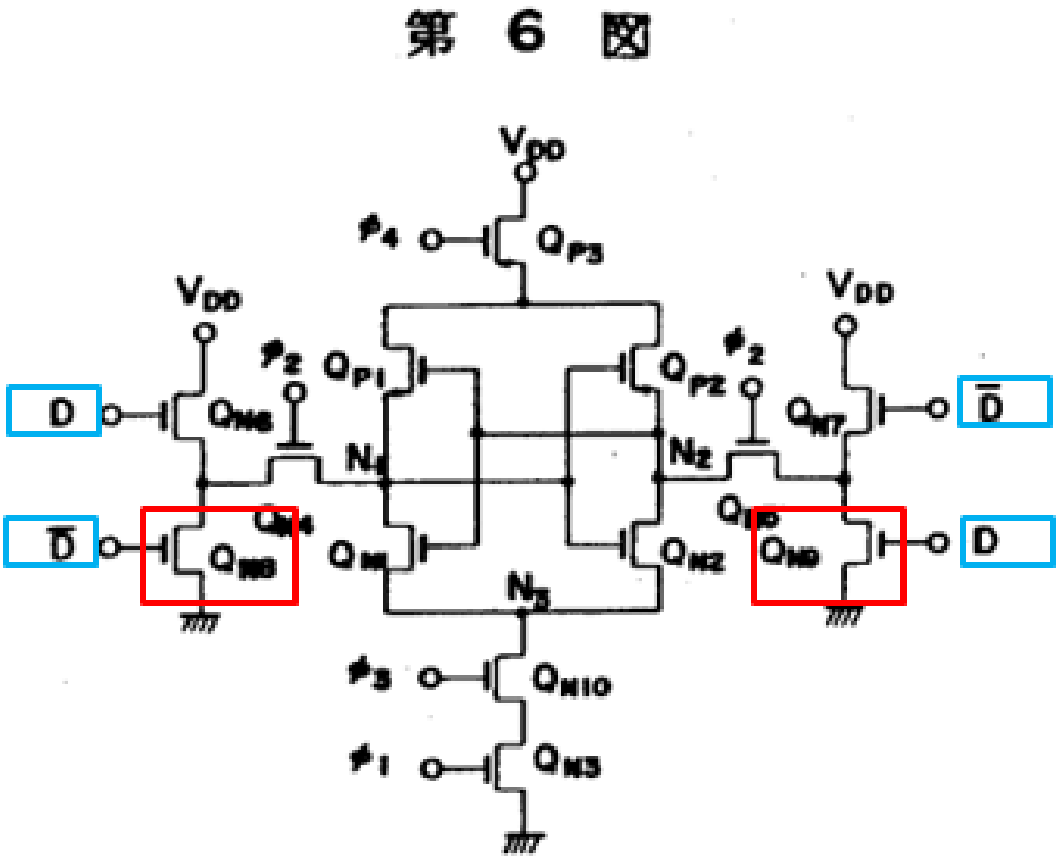
(Ex.1002, ¶129, citing Ex.1001, FIG. 5 (annotated).)

10. Claim 16

a) "The sense amplifier arrangement of claim 15 wherein one said pull-down transistor in the local data write circuits for the corresponding latch circuit receives the first data write signal and the other said pull-down transistor receives the second data write signal."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶130.) *Inoue* discloses that Q_{N9} ("one said pull-down transistor in the local data write driver circuits for the corresponding latch circuit") receives D ("the

first data write signal") and Q_{N8} ("the other said pull-down transistor") receives $\overline{D}$ ("the second data write signal"). (*Supra*, Sections IX.A.1(c),(d),IX.A.6,8-9; Ex.1007, 3, FIG. 6.)



(Ex.1002, ¶130, citing Ex.1007, FIG. 6 (annotated to show transistor Q_{N8} in red at left, transistor Q_{N9} in red at right, and signals D and $\overline{D}$ in blue).)

The '574 patent discloses a similar configuration.

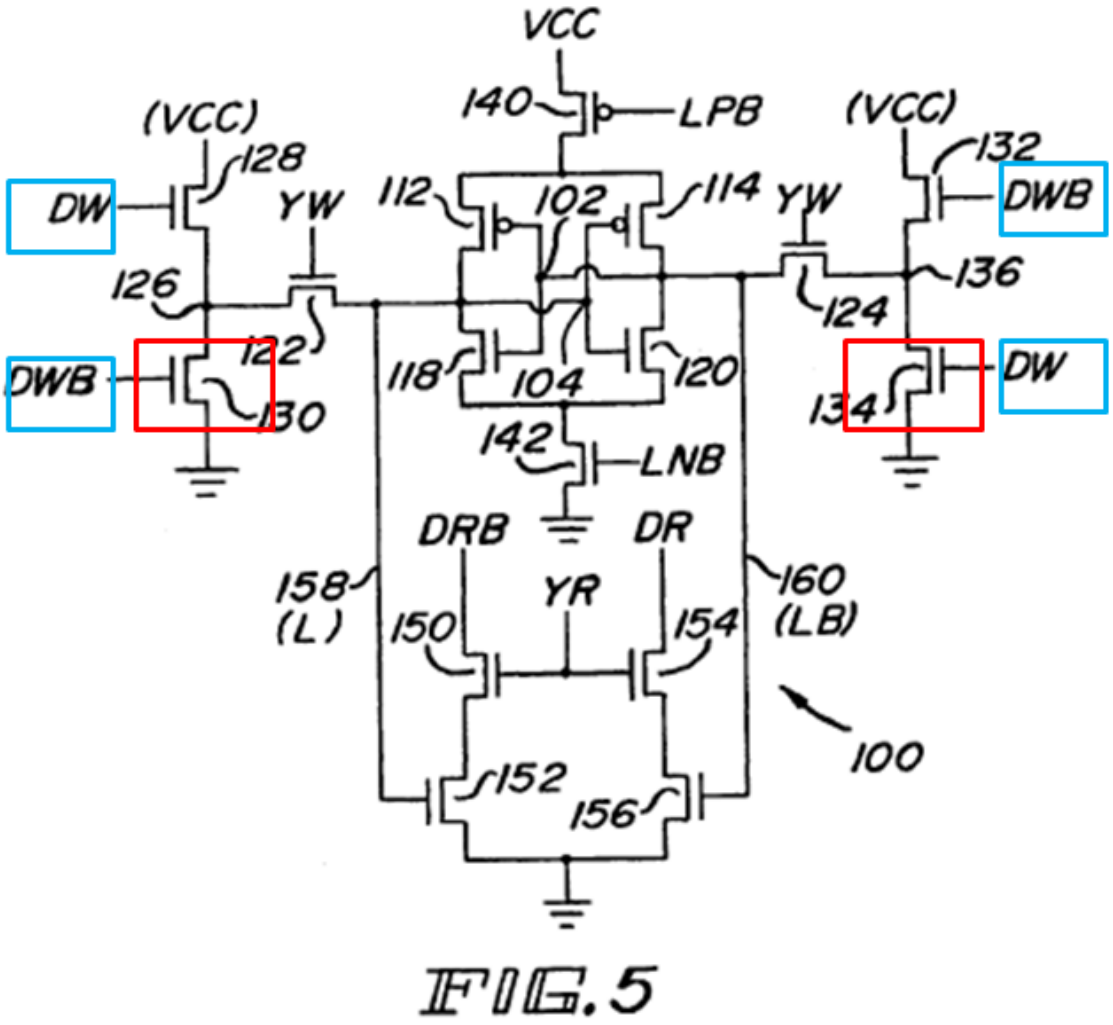


FIG. 5

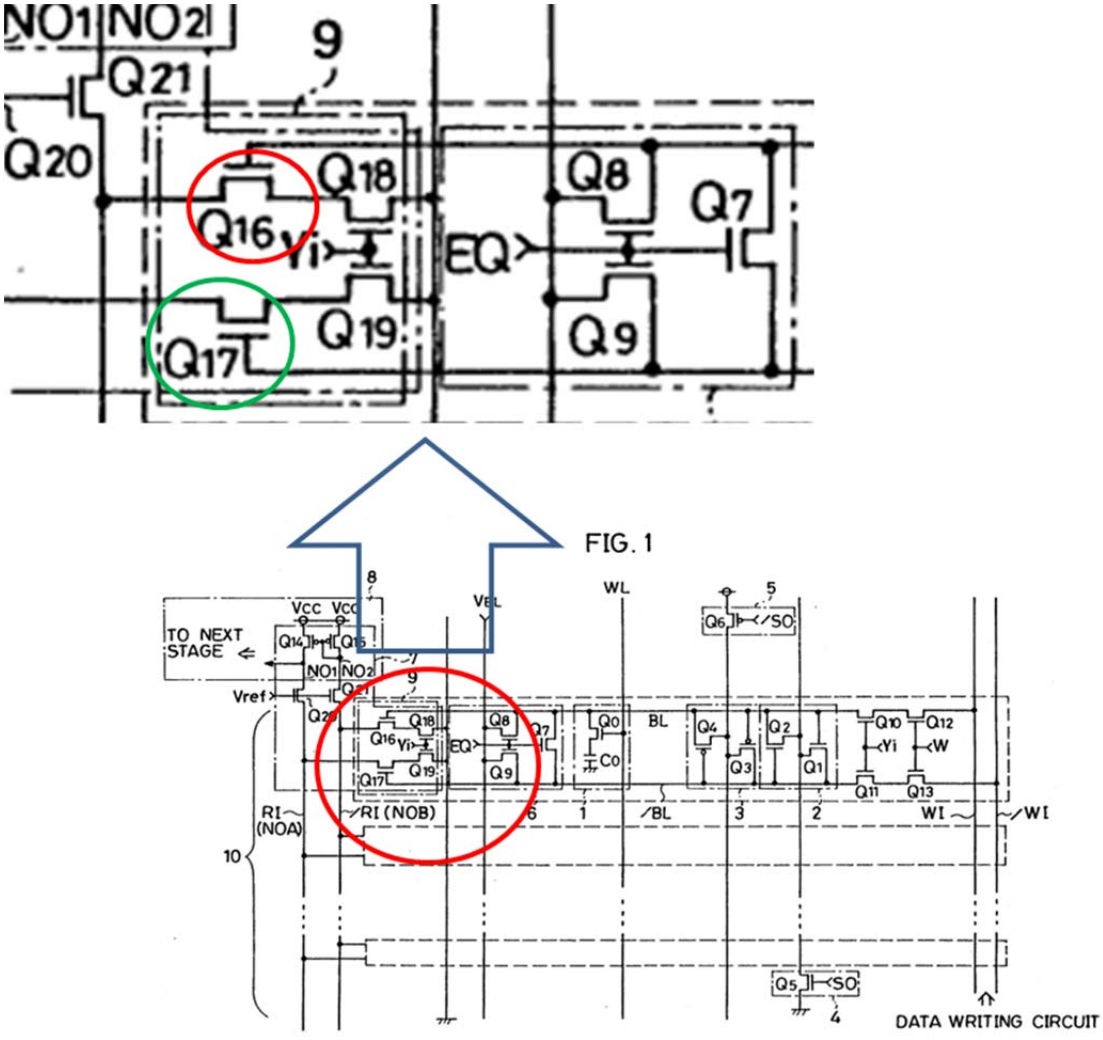
(Ex.1002, ¶131, citing Ex.1001, FIG. 5 (annotated).)

11. Claim 21

a) "The sense amplifier arrangement of claim 4 wherein said local column read amplifier comprises: first and second transistors each having respective control electrodes;"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶132.) As discussed above with respect to claim limitation 4(c), *Hamade*'s drive circuit 9 corresponds to the claimed "local column read

amplifier." (*See Supra*, Section IX.A.1(c).) Drive circuit 9 ("said local column read amplifier") includes drive transistors Q17 and Q16 ("first and second transistors," respectively) (shown below in green and red, respectively) each having respective gate terminals ("respective control electrodes"). (*See Supra*, Section IX.A.1(c); Ex.1009, FIG. 1, 7:32-39.)



(Ex.1002, ¶132, citing Ex.1009, FIG. 1, annotated.)

b) "the control electrode of the first transistor being coupled to one of said pair of latch nodes; the control electrode of the second transistor being coupled to the other one of said pair of latch nodes."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶133.) For example, as discussed above, in the combined system the gates of NMOS transistors Q16 and Q17 would have been coupled to nodes N_1 and N_2 of figure 6 of *Inoue*, respectively. (*Supra*, Section IX.A.1(c).)

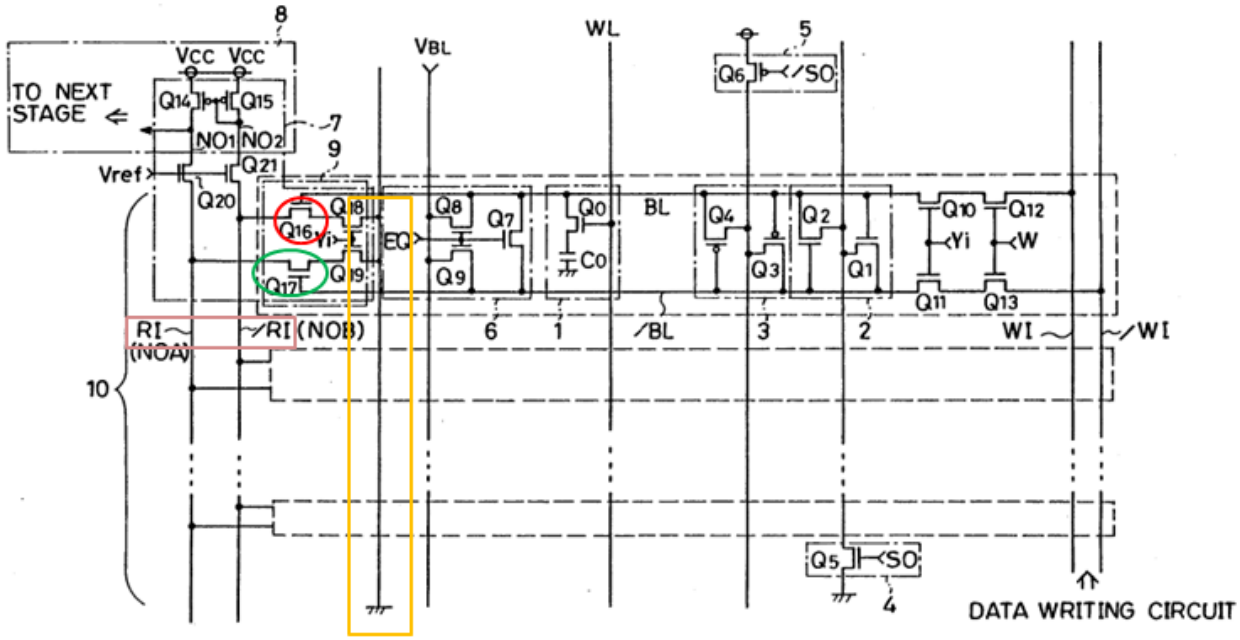
12. Claim 22

a) "The sense amplifier arrangement of claim 21 wherein said column read amplifier is coupled to receive first and second data read signals; wherein said first transistor is coupled between said first data read signal and a first power supply; wherein said second transistor is coupled between said second data read signal and said first power supply."

The combined *Inoue-Min-Hamade* system includes the read circuitry from *Hamade*. (*See Supra*, Section IX.A.1(c).) *Hamade* discloses that the drive circuit 9 as implemented at a given column ("said column read amplifier") is coupled to receive signals at read only data lines RI and /RI ("first and second data read signals," respectively) (pink below), wherein transistor Q17 ("said first transistor") (green below) is coupled between read only data line RI ("said first data read signal") and the ground node ("a first power supply"), and transistor Q16 ("said second transistor") (red below) is coupled between read only data line /RI ("said second data read signal") and the ground node ("said first power supply") (orange

below). (*Supra*, Sections IX.A.1(c),IX.A.11; Ex.1009, FIG. 1 (reproduced below with annotations).) Specifically, *Hamade* discloses that transistors Q16 and Q17 pass current from read only data lines /RI and RI to ground, respectively. (Ex.1002, ¶¶134-135; Ex.1009, 7:32-39, 8:8-27, 8:24-31, 8:52-54.)

FIG. 1



(Ex.1002, ¶134, citing Ex.1009, FIG. 1 (annotated).)

The '574 patent discloses a similar configuration.

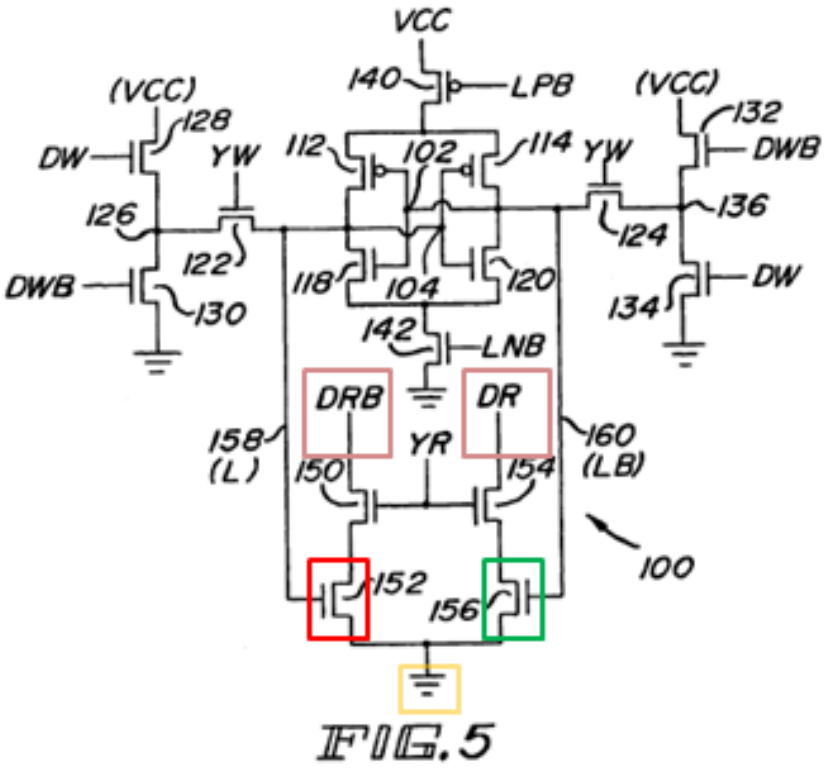


FIG. 5

(Ex.1002, ¶136, citing Ex.1001, FIG. 5 (annotated).)

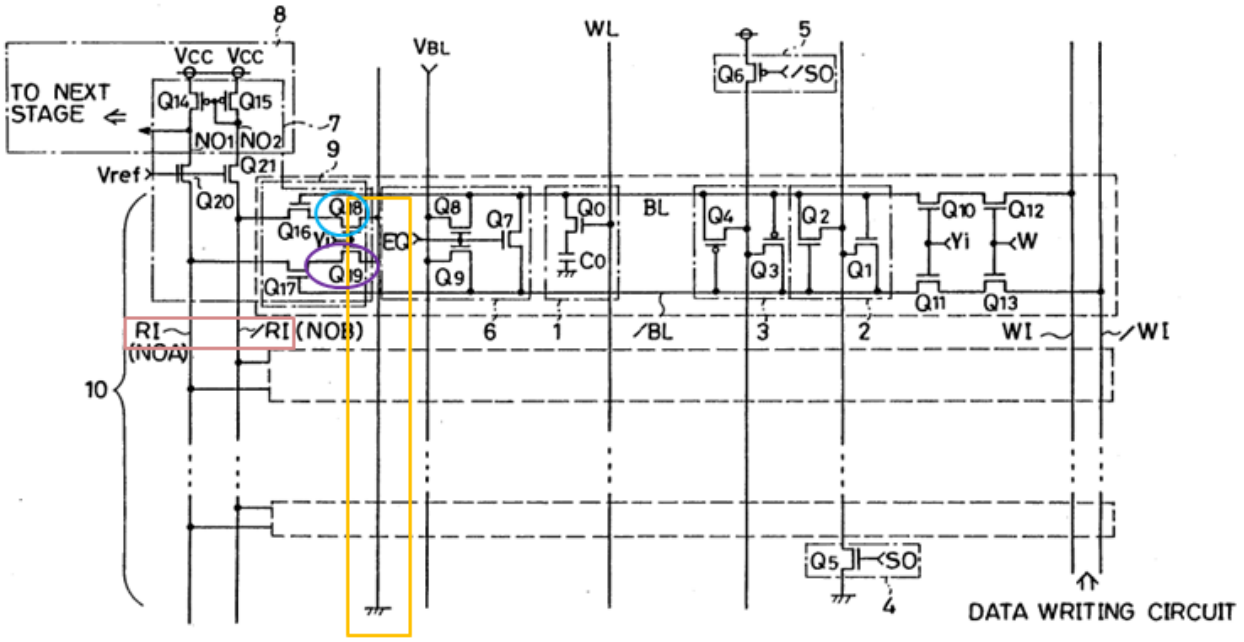
13. Claim 23

a) "The sense amplifier arrangement of claim 22 wherein said local column read amplifier further comprises: a third transistor coupled between said first data read signal and said first power supply; and a fourth transistor coupled between said second data read signal and said first power supply."

The drive circuit of *Hamade* implemented at a given column ("said local column read amplifier") in the combined *Inoue-Min-Hamade* system further includes transistor Q19 ("a third transistor") (purple below) coupled between read only data line RI ("said first data read signal") (pink below) and the ground node

("said first power supply") (orange below), and transistor Q18 ("a fourth transistor") (blue below) coupled between read only data line /RI ("said second data read signal") (pink below) and the ground node ("said first power supply") (orange below). (Ex.1002, ¶137-138; *see Supra*, Sections IX.A.1(c),IX.A.11-12; Ex.1009, FIG. 1, 8:24-31, 8:52-54.)

FIG. 1



(Ex.1002, ¶137, citing Ex.1009, FIG. 1 (annotated).)

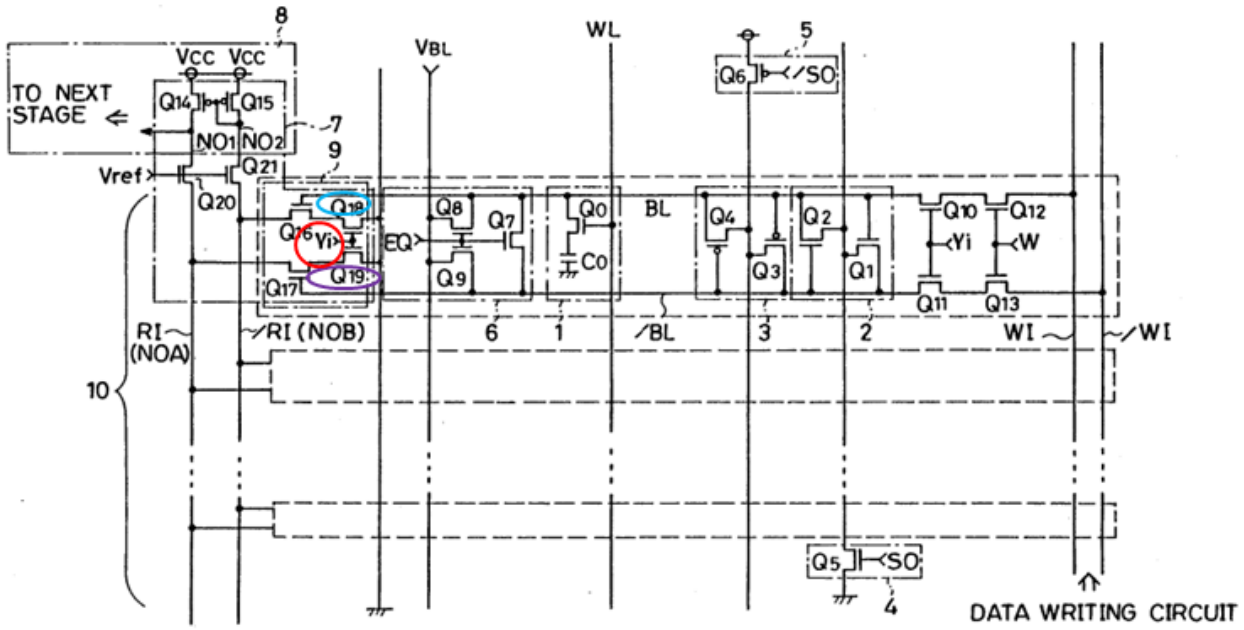
14. Claim 24

a) "The sense amplifier arrangement of claim 23 wherein said third and fourth transistors are coupled to receive a column read control signal."

In the *Inoue-Min-Hamade* combination discussed above for limitation 4(c), the drive circuit 9 as implemented at a given column includes transistors Q19 (purple below) and Q18 (blue below) ("said third and fourth transistors") coupled

to receive, at their respective gate terminals, a column selecting signal Yi (red below) ("coupled to receive a column read control signal"). (*See Supra*, Sections IX.A.1(c),IX.A.11-13.)

FIG. 1



(Ex.1002, ¶140, citing Ex.1009, FIG. 1.)

A POSITA would have found it obvious to incorporate the column selecting signal Yi associated with drive circuit 9 in *Hamade* in the combined *Inoue-Min-Hamade* system because the column selecting signal Yi would have allowed the selection of a particular column for reading and hence, would have made possible operation of the multi-column memory device in the combined *Inoue-Min-Hamade* system. (*See Supra*, Section IX.A.1(c); Ex.1009, FIG. 1; Ex.1002, ¶141.) *KSR*, 550 U.S. at 416-17. Therefore, a POSITA would have provided, in the combined *Inoue-Min-Hamade* system, the column selecting signal to the gates of transistors

Q18 and Q19 as illustrated in figure 1 of *Hamade* so that "[w]hen column selecting signal Yi rises from the low level to the high level, transistors Q18 and Q19 are turned on." (Ex.1009, 8:24-26, FIG. 1; Ex.1002, ¶142.) A POSITA would have understood that *Hamade*'s column selecting signal Yi is a "column read signal" because it is used for selecting a column during a read operation. (Ex.1009., 8:8-26; Ex.1002, ¶142.)

15. Claim 25

a) "The sense amplifier arrangement of claim 24 wherein said third and fourth transistors include respective control electrodes coupled to receive said column read control signal."

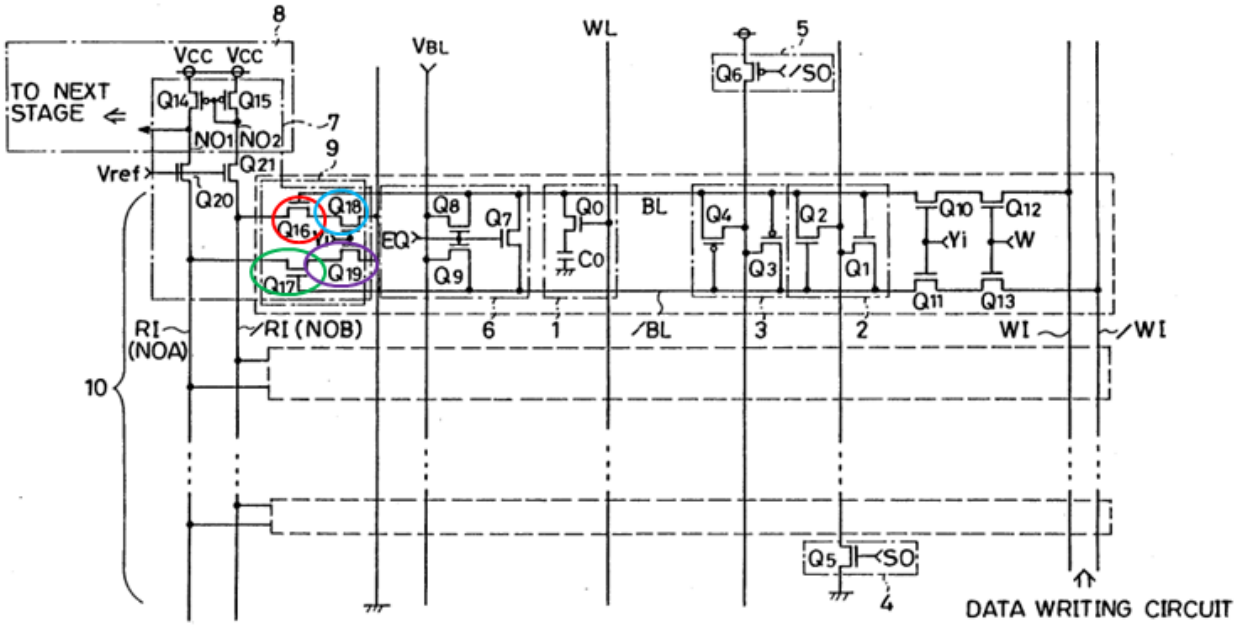
The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶143.) For instance, with respect to a given column of the combined *Inoue-Min-Hamade* system discussed above for limitation 4(c), *Hamade* discloses transistors Q19 and Q18 (annotated in blue and purple above at Sections IX.A.13-14) ("third and fourth transistors") in figure 1 have their respective gate terminals ("respective control electrodes") coupled to column selecting signal Yi ("coupled to receive said column read signal"). (*See* Ex.1009, FIG. 1; *see also Supra*, Sections IX.A.1(c), IX.A.11-14.)

16. Claim 26

a) "The sense amplifier arrangement of claim 25 wherein said third transistor is coupled in series with said first transistor, and wherein said fourth transistor is coupled in series with said second transistor."

The combined *Inoue-Min-Hamade* system includes the read circuitry from *Hamade*. (*See Supra*, Section IX.A.1(c).) *Hamade* discloses that the drive circuit 9 as implemented at a given column ("said column read amplifier") includes transistor Q19 ("said third transistor") (purple below) is coupled in series with transistor Q17 ("said first transistor") (green below), and transistor Q18 ("said fourth transistor") (blue below) is coupled in series with transistor Q16 ("said second transistor") (red below). (*See supra*, Sections IX.A.1(c), IX.A.11-15; Ex.1009, FIG. 1; *see also* Ex.1001, 7:1-8, FIG. 5.)

FIG. 1



(Ex.1002, ¶144, citing Ex.1009, FIG. 1 (annotated).)

The '574 patent discloses a similar configuration.

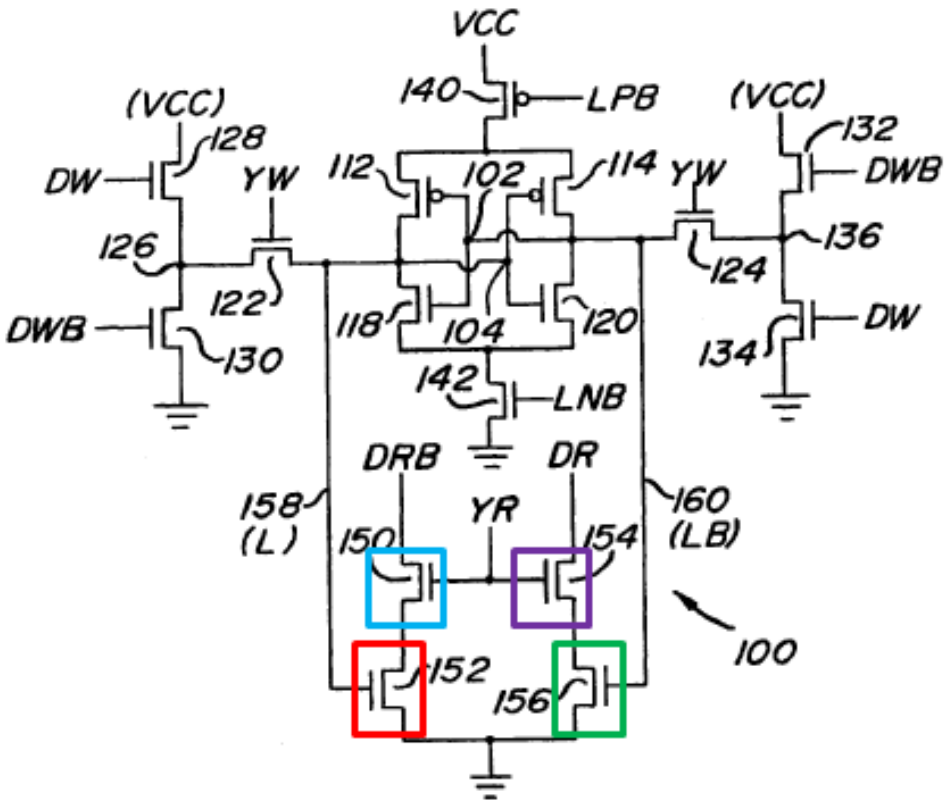


FIG. 5

(Ex.1002, ¶145, citing Ex.1001, FIG. 5 (annotated).)

17. Claim 27

a) "The sense amplifier arrangement of claim 24 wherein said third transistor is coupled in series with said first transistor, and wherein said fourth transistor is coupled in series with said second transistor."

The combined *Inoue-Min-Hamade* system discloses this feature for the same reasons discussed above for claim 26. (*Supra*, Sections IX.A.1(c), IX.A.11-16; Ex.1009, FIG. 1, 1:44-47; Ex.1002, ¶146.)

B. Ground 2: *Inoue*, *Min*, *Hamade*, and *Ogawa* Render Obvious Claims 11-13 of the '574 Patent

Inoue in combination with *Min*, *Hamade*, and *Ogawa* discloses or suggests all of the features of claims 11-13 of the '574 patent.

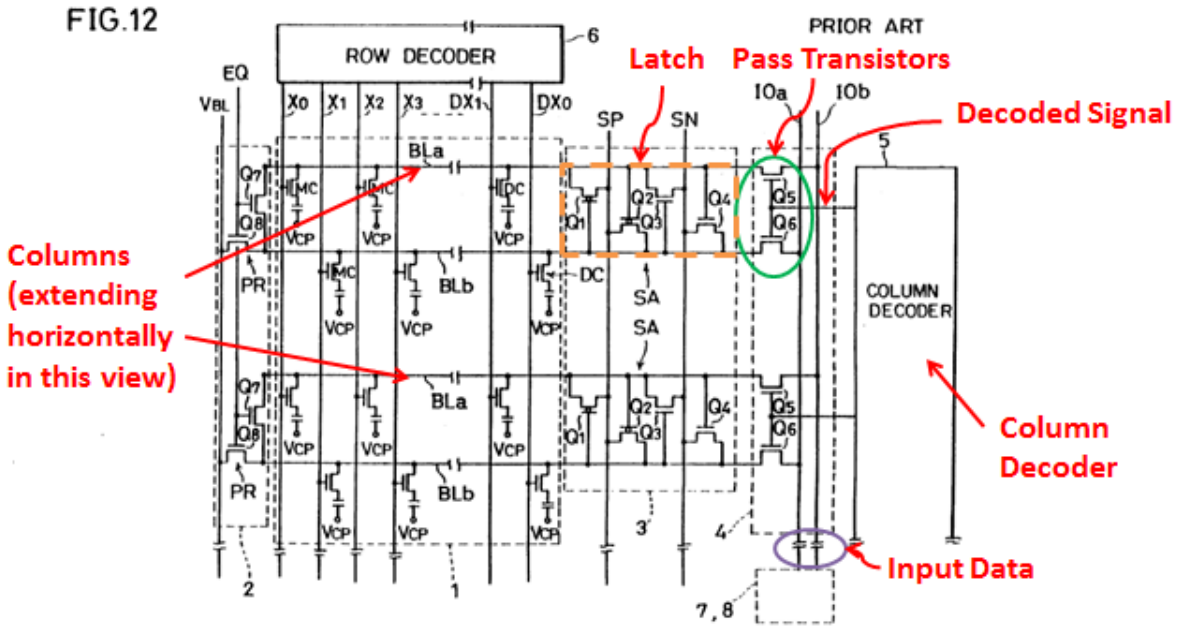
1. Claim 11

a) "The sense amplifier arrangement according to claim 10 wherein said write control signal is a column write signal."

Inoue in combination with *Min*, *Hamade*, and *Ogawa* discloses this feature. (Ex.1002, ¶¶148-156.) In the *Inoue-Min-Hamade* combined system discussed above, clock ϕ_2 is a write control clock ("a write control signal") that is received by the pass transistors Q_{N4} and Q_{N5}. (*See Supra*, Sections IX.A.1(c), IX.A.7.) *Inoue*, *Min*, and *Hamade* do not expressly disclose that clock ϕ_2 is a "***column*** write signal," but as discussed below, *Ogawa* discloses this feature, and a POSITA would have been motivated, in light of *Ogawa*, to utilize a column write signal as the write control signal in a combined *Inoue-Min-Hamade* system. (Ex.1002, ¶148.)

Ogawa explains that in the conventional memory writing technique a "column decoder 5" is provided a column address, which decodes the address and selects "a desired bit line pair." (Ex.1010, 1:18-19, 1:24-27, FIGS. 2, 12, 3:1-13.) To select a bit line pair (column) for writing data (which is provided on data buses

IOa and IOb), the column decoder turns on transistors Q5 and Q6 corresponding to that bit line pair. (Ex.1002, ¶¶149-150; Ex.1010, 2:17-26, FIG. 12.)

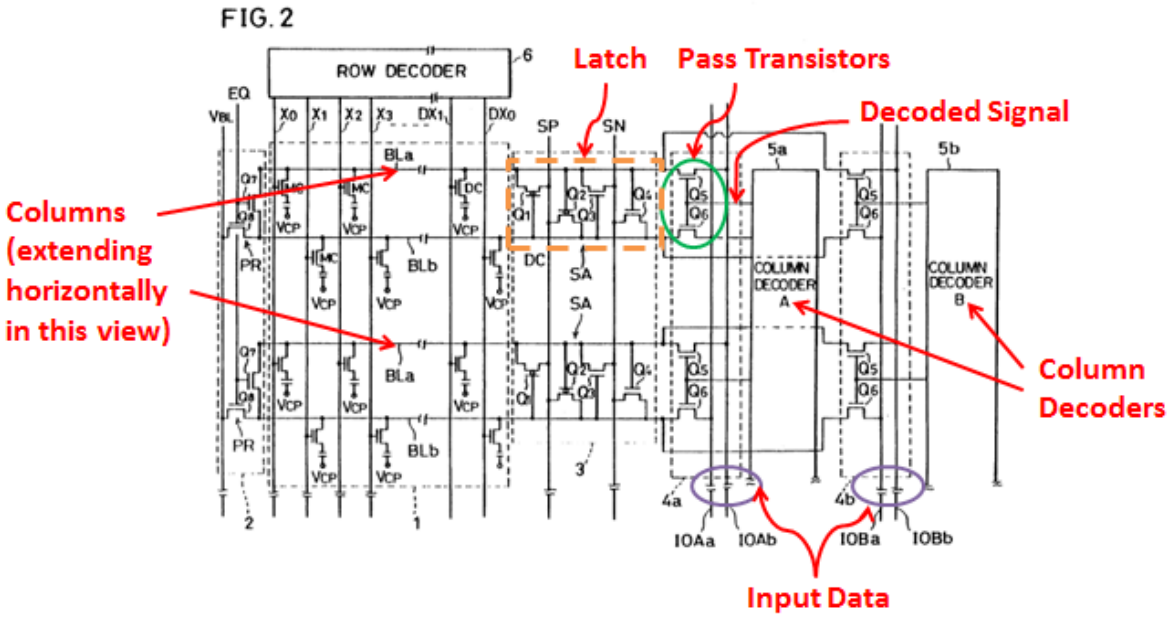


(Ex.1002, ¶149, citing Ex.1010, FIG. 12 (annotated).)

Annotated *Ogawa*'s figure 12 above also shows the correspondence between *Inoue*'s figure 6 and *Ogawa*'s circuitry. As shown, transistors Q5 and Q6 are the corresponding "pass transistors" in *Ogawa*'s circuit because, like *Inoue*'s transistors Q_{N4} and Q_{N5} of figure 6, transistors Q5 and Q6 must be turned ON to access the latch circuit for writing. (Ex.1002, ¶151; Ex.1010, 2:17-26, FIG.12 (showing transistors Q5 and Q6); Ex.1007, 3, 4.)

Ogawa's embodiments (e.g., figure 12) retain the above basic functionality during a write operation but modify the conventional arrangement by providing

two column decoders (e.g., decoders 5A and 5B in FIG. 2) instead of one (decoder 5 in FIG. 12). (Ex.1010, 8:16-36; *compare id.*, FIG. 12, *with* FIG. 2.)



(Ex.1002, ¶152, citing Ex.1010, FIG. 2 (annotated).)

Based on the foregoing disclosures, a POSITA would have understood that *Ogawa*'s signal provided from any of column decoders 5/5a/5b to pass transistors Q5 and Q6 is a "column write signal" as in claim 11 of the '574 patent when the decoder(s) select(s) a column (bit line pair) for writing. (Ex.1002, ¶153.) Indeed, at the time of writing to a given column, the decoded signal output from decoders 5A/5B/5 turns on transistors Q5 and Q6 "connected to the select bit line pair" to allow data on the data buses to be written to each bit line. (Ex.1010, 2:17-33, 8:16-36.)

In view of *Ogawa*, it would have been obvious to a POSITA to implement the write control clock ϕ_2 of each column of the *Inoue-Min-Hamade* system as a "column write signal" that is provided by a decoder as disclosed in *Ogawa*. (Ex.1002, ¶154.) A POSITA would have looked to *Ogawa* to refine or improve the combined *Inoue-Min-Hamade* system, because *Inoue* discloses that its figure 6 circuit configuration may be applied to a sense amplifier in dynamic memory and *Ogawa* teaches how to operate a dynamic memory with multiple rows and columns of memory cells. (*Id.*)

A POSITA would have been motivated to use *Ogawa*'s teachings to configure the combined *Inoue-Min-Hamade* system to work with a memory array containing rows and columns of memory cells, particularly because in the early 1990's a typical way to arrange memory cells in dynamic memory was by columns and rows, as explained by *Ogawa*. (Ex.1010, 1:24-27; Ex.1002, ¶155.) *Min* describes a memory with multiple columns having respective sense amplifiers, and *Hamade* describes a memory with multiple rows and columns, but a POSITA would have also looked to *Ogawa* for additional details regarding implementing a column decoder in a memory having multiple rows and columns. (*See, e.g.*, Ex.1008, FIG. 3B; Ex.1009, FIG. 1; Ex.1002, ¶155.) Such a person would have recognized that modifying the write control clock ϕ_2 in the combined *Inoue-Min-Hamade* system to be a "column write signal" that is provided by a decoder as

disclosed in *Ogawa* would have provided the benefit of allowing a column of memory cells to be selected and would have been a necessary feature to enable *Inoue*'s figure 6 circuit to be implemented in a dynamic memory, which would have included many memory cells. (Ex.1002, ¶155.) *KSR*, 550 U.S. at 416-17.

The above modification would have been the result of combining prior art elements (e.g., a sense amplifier and pass transistors as discussed above in the combined *Inoue-Min-Hamade* system for claim 10 (*see Supra*, Section IX.A.7), and *Ogawa*'s column decoder that drives pass transistors (Ex.1010, FIGS. 2, 12)) according to known methods (e.g., driving a pass transistor with the column write signal as in *Ogawa*) to yield predictable results (e.g., turn on pass transistors using the column write signal to select a column in memory for writing). (Ex.1002, ¶156.) *KSR*, 550 U.S. at 416.

2. Claim 12

a) "The sense amplifier arrangement according to claim 11 wherein said column write signal is a decoded column write signal."

As discussed above for claim 11, the combined *Inoue-Min-Hamade-Ogawa* system discloses a column write signal that is provided by a decoder, which decodes a column address. (*See Supra*, Section IX.B.1.) Therefore, the column write signal in the combined *Inoue-Min-Hamade-Ogawa* system is a "decoded" column write signal. (Ex.1002, ¶157.)

3. Claim 13

a) "The sense amplifier arrangement according to claim 12 wherein said integrated circuit memory has a plurality of columns and wherein said decoded column write control signal is decoded for a subset of said plurality of columns."

The combined *Inoue-Min-Hamade-Ogawa* system includes a plurality of columns, for the reasons discussed above for limitation 4(b) regarding the *Inoue-Min* combination. (*See Supra*, Section IX.A.1(b), citing Ex.1008, FIG. 3B and providing demonstratives of the combined *Inoue-Min* system.) As discussed above for claim 11, *Ogawa*'s decoded column select signal selects "a desired bit line pair," i.e., it selects one column from the plurality of columns. (Ex.1010, 1:24-27, FIGS. 2, 12, 3:1-13.) A single column is a "subset" of a plurality of columns. Therefore, the combined *Inoue-Min-Hamade-Ogawa* system discloses "said decoded column write control signal is decoded for a subset of said plurality of columns." (Ex.1002, ¶158.)

C. Ground 3: *Inoue*, *Min*, and *Hamade* Render Obvious Claim 17 of the '574 Patent

Claim 17 depends from dependent claims 16, 15, 14, 9, and 8, and dependent claim 8 depends from independent claim 4. Thus, Petitioner demonstrates below how *Inoue* discloses the limitations of claims 4, 8, 9, and 14-16 (Sections IX.C.1-C.6) before addressing the limitations of claim 17 (Section IX.C.7). The analysis in this section is based on the disclosure of figure 3 of *Inoue*

in combination with FIG. 6, in part because FIG. 3 of *Inoue* explicitly discloses the "active memory block" limitation of claim 17, as discussed below. Because the disclosure of figure 6 (as discussed above) builds on the circuits disclosed in figures 1, 3, and 4 of *Inoue*, the analysis in this section overlaps with the analysis above in section IX.A. (Ex.1002, ¶¶159-161.) When describing the operation and composition of FIG. 3, *Inoue* does not repeat the details it previously discusses for common aspects between figures 1 and 3. (*See* Ex.1007, 3.) Therefore, in this section the common aspects of figures 1, 2, and 3 of *Inoue* are referenced when describing the configuration of figure 3.

1. Claim 4[13]

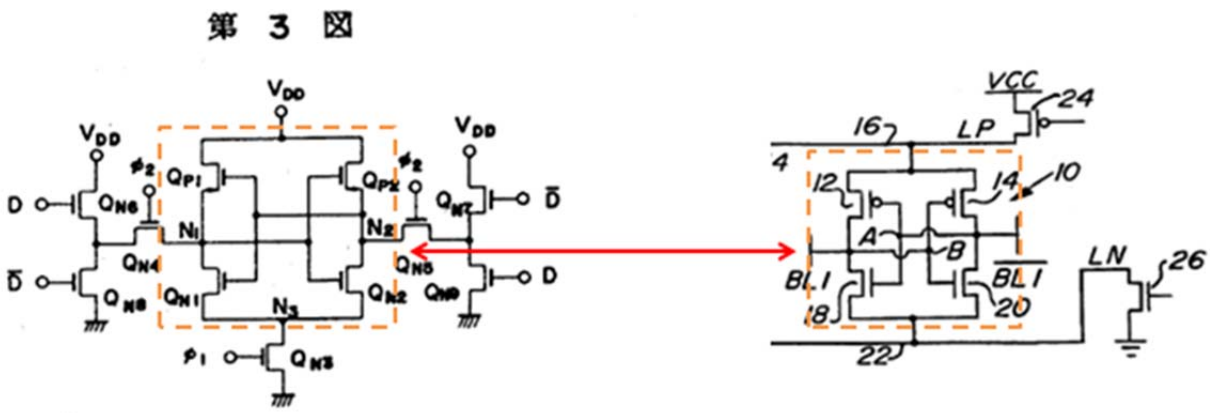
a) Claim Element 4(a)

To the extent the preamble is limiting, *Inoue* discloses this feature. (Ex.1002, ¶¶162-168.) For example, *Inoue* discloses "a semiconductor device" comprising a sense amplifier with a flip-flop circuit. (Ex.1007, 1 (Claim 1).)

Moreover, figure 3 of *Inoue* discloses a CMOS flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, and Q_{N2}. (Ex.1007, 3, FIG. 3.) *Inoue* discloses that in figure 1, N-channel transistors Q_{N1}, Q_{N2} constitute a flip-flop and that "FIG. 3

[13] The limitations of claims 4, 8, 9, and 14-16 are provided above in ground 1 (Section IX.A) and are not repeated here.

illustrates an example of a CMOS F/F" similar to figure 1 except that the F/F also includes "P-channel transistors Q_{P1}, Q_{P2}" in addition to the N-channel transistors Q_{N1}, and Q_{N2}. (*Id.*, 3, FIGS. 1, 3.) As discussed above in Section IX.A.1(b), the flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, and Q_{N2} would have been readily recognized by a POSITA as a "sense amplifier" and a "latch." (*See Supra*, Section IX.A.1(b).) The demonstrative below shows the correspondence between the circuit in figure 3 of *Inoue* and "sense amplifier 10" shown in figure 1 of the '574 patent.



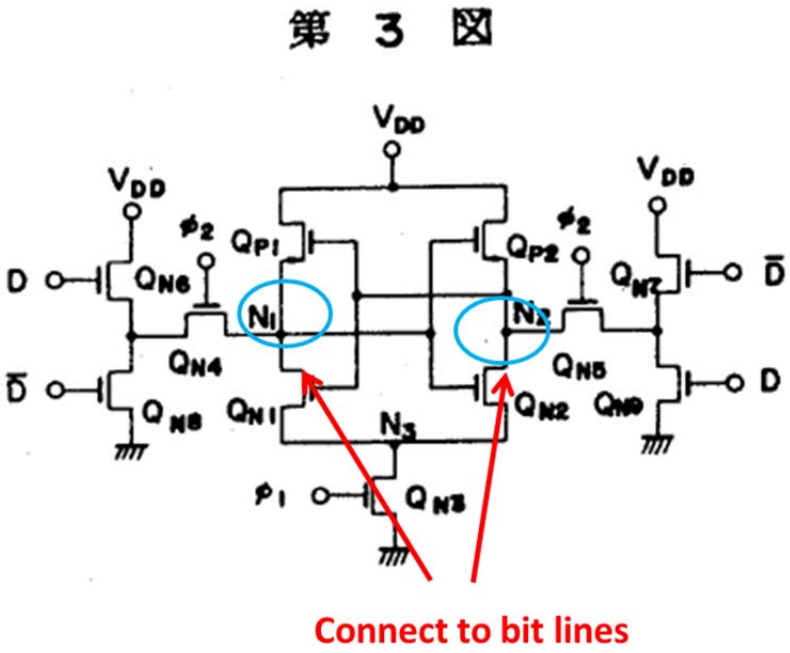
Inoue, FIG. 3 '574 Patent, FIG. 1 (excerpt)

(Ex.1002, ¶163, citing Ex.1007, FIG. 3 (annotated), Ex.1001, FIG. 1 (annotated).)

Accordingly, figure 3 of *Inoue* discloses a "sense amplifier arrangement" because it discloses a flip-flop (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) that one of ordinary skill in the art would have recognized to be a "sense amplifier." (Ex.1002, ¶164.)

Figure 3 of *Inoue*, however, does not explicitly disclose that the sense amplifier "is for an integrated circuit memory." (Ex.1002, ¶165.) But figure 6 of *Inoue* discloses that the same flip-flop configuration as shown in figure 3 can be applied to "a sense amp in . . . dynamic memory." (Ex.1007, 4, FIG. 6.) For instance, figure 6 discloses the same circuit configuration as figure 3 except for the addition of transistors Q_{P3} and Q_{N10} above and below the flip-flop circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}). (*Compare id.*, FIG. 3, *with id.*, FIG. 6.) *Inoue* further discloses that the circuit of figure 6 can be "applied to a sense amp in the dynamic memory" (i.e., DRAM) where "for example, N_1 and N_2 correspond to bit lines." (*Id.*, 4; *see* Section IX.A.1(a).)

In view of figure 6 in *Inoue*, one of ordinary skill in the art would have been motivated to utilize the sense amplifier configuration disclosed in figure 3 in a DRAM, which is a type of "integrated circuit memory." (Ex.1002, ¶166.) For instance, one of ordinary skill in the art would have been motivated to combine the teachings of figures 3 and 6 in *Inoue* such that nodes N_1 and N_2 in figure 3 also correspond to bit lines of a DRAM like nodes N_1 and N_2 in figure 6 in *Inoue*. (Ex.1007, FIG. 3.)



(Ex.1002, ¶166, citing Ex.1007, FIG. 3 (annotated to show the modification of FIG. 3 based on FIG. 6).)

Configuring the figure 3 circuit in the manner described above would have allowed the figure 3 circuit (as configured in this manner) to be used for reading and writing data to memory cells of a DRAM, thereby enhancing the utility of the circuit. (Ex.1002, ¶167.) *KSR*, 550 U.S. at 416-17. Furthermore, one of ordinary skill in the art would have recognized that the above modification of the circuit of figure 3 would have been merely the result of combining prior art elements (*e.g.*, *Inoue*'s figure 3 circuit and bit lines coupled to nodes N_1, N_2 in figure 3) according to known methods (*e.g.*, connecting nodes N_1, N_2 in figure 3 to bit lines in a DRAM) to yield predictable results (*e.g.*, sensing and amplifying of data read and

written to memory cell by the sense amplifier of figure 3). (Ex.1002, ¶168.) *KSR*, 550 U.S. at 416.

b) Claim Element 4(b)

Inoue in combination with *Min* discloses or suggests this feature. As discussed above in Section IX.C.1(a), the transistors Q_{P1}, Q_{P2}, Q_{N1}, and Q_{N2} included in figure 3 of *Inoue* would have been understood by a POSITA to constitute a "sense amplifier" that is a "latch." Therefore, transistors Q_{P1}, Q_{P2}, Q_{N1}, and Q_{N2} constitute a "sense amplifier latch circuit." Moreover, as discussed above in Section IX.C.1(a), one of ordinary skill in the art would have been motivated to combine the teachings of figures 3 and 6 in *Inoue* such that nodes N_1 and N_2 in figure 3 also correspond to bit lines of a DRAM like nodes N_1 and N_2 in figure 6 in *Inoue.* Therefore, the "sense amplifier latch circuit" in such a modified figure 3 circuit would have included "a pair of nodes to which respective bit lines are coupled." (Ex.1002, ¶169.)

A POSITA would have understood that a practical DRAM would have included several of such sense amplifiers coupled to bit line pairs but that *Inoue* does not expressly show multiple sense amplifiers in any figure, nor does *Inoue* expressly show a figure with a plurality of sense amplifier latch circuits each having a pair of nodes to which respective bit lines are coupled. (*See* Section IX.A.1(b).) *Min* provides such disclosure. (Ex.1002, ¶170.) As discussed above

in Section IX.A.1(b), a POSITA would have looked to *Min* for teachings on a multi-column memory system having a plurality of bit line pairs, each of which is coupled to a respective sense amplifier. (*See Supra*, Section IX.A.1(b).) As such, for the same reasons provided in Section IX.A.1(b) with respect to *Inoue's* circuit of figure 6, a POSITA looking at *Min* would have been motivated to implement *Inoue's* modified figure 3 circuit[14] in a multi-column memory system to create a dynamic memory having a plurality of bit line pairs (like in a practical DRAM), each of which is coupled to a respective sense amplifier. Such a person would have been motivated to combine *Inoue's* modified figure 3 circuit and *Min* in a manner similar to that discussed above with respect to figure 6 of *Inoue* and *Min* in Section IX.A.1.b. For instance, a POSITA would have been motivated to replicate the modified figure 3 circuit across various columns to create a practical DRAM. (Ex.1002, ¶171.)

Below is a non-limiting example showing a generalized illustration of such a modified circuit.

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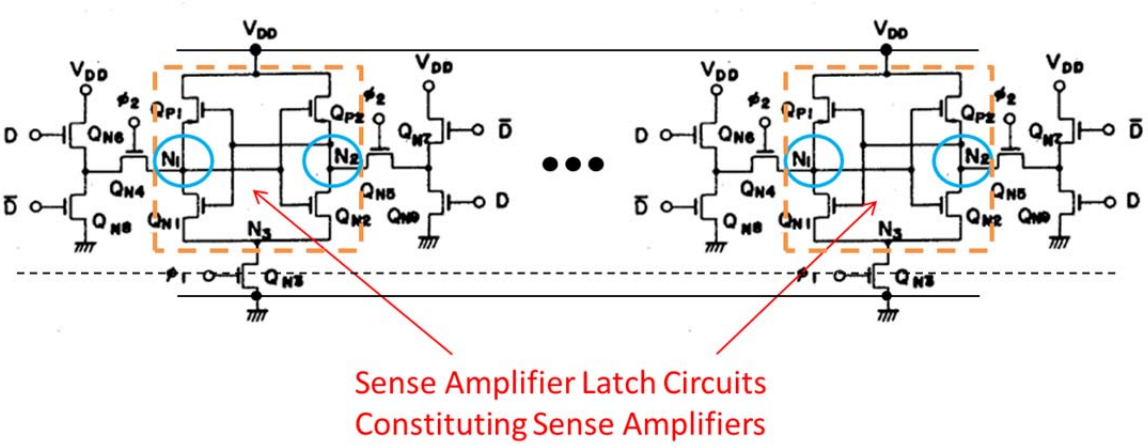
[14] The modified figure 3 circuit is the circuit of figure 3 modified based on figure 6 of *Inoue*. (Ex.1002, ¶171.)



(Ex.1002, ¶172, citing Ex.1007, FIG. 3; 1008, FIG. 3B (annotated to show in orange flip-flop ("sense amplifier latch circuit") for M respective columns (M an integer), and to show in blue nodes N_1/N_2).)

As is apparent from the above illustration and as explained above, the combined *Inoue-Min* system discloses a plurality of sense amplifier latch circuits each having a pair of nodes (N_1, N_2) to which respective bit lines are coupled. The '574 patent discloses a similar configuration for a single column, as shown below, where the same colors are used to annotate corresponding components as the ones described above.

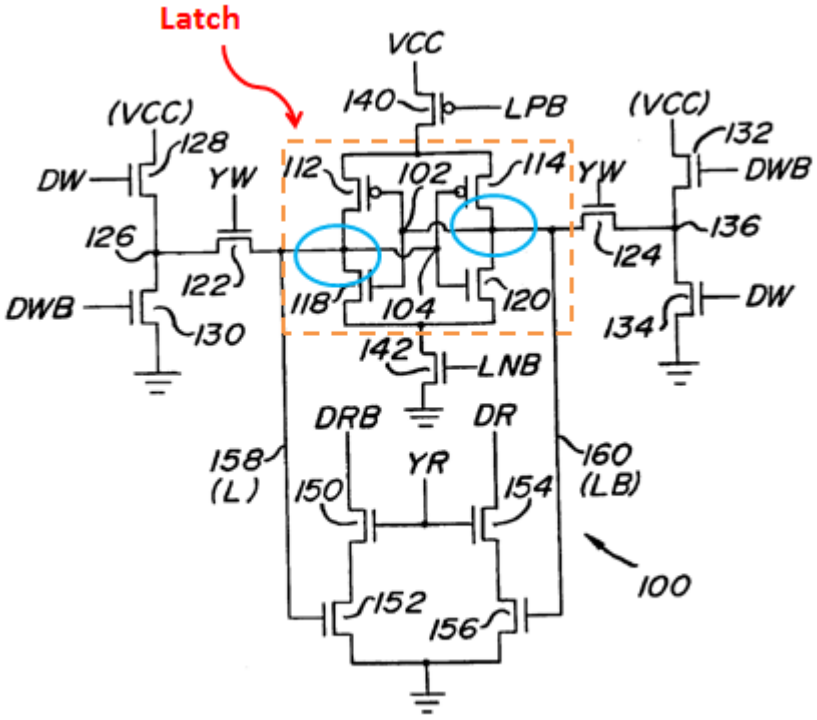


FIG. 5

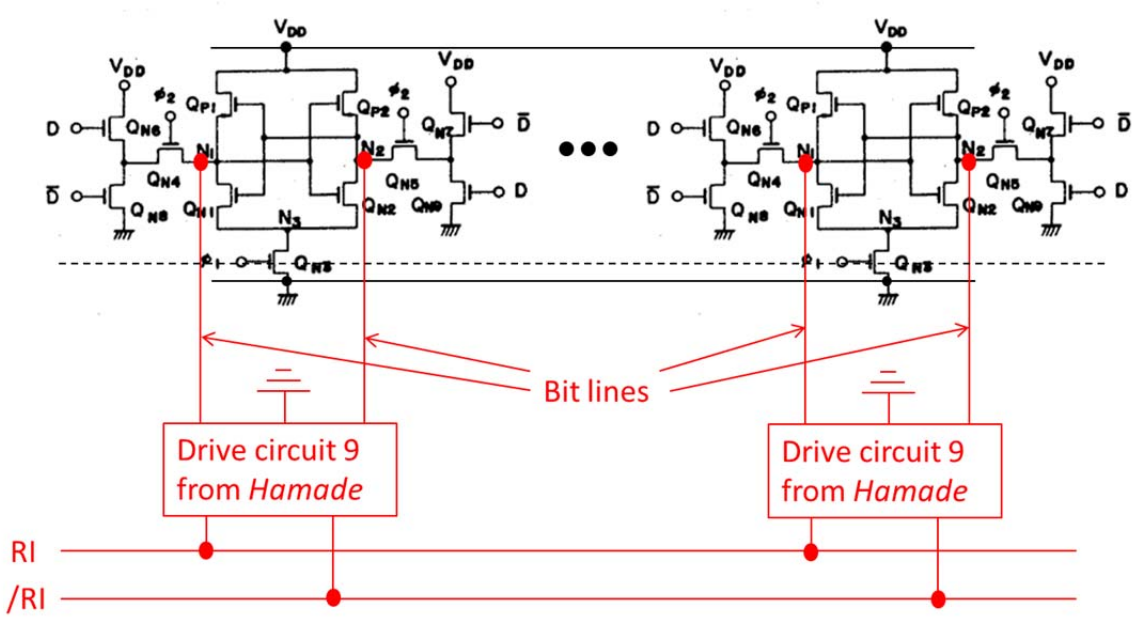
(Ex.1002, ¶173, citing Ex.1001, FIG. 5 (annotated).)

c) Claim Element 4(c)

The combined *Inoue-Min* system discussed in Section IX.C.1(b) does not expressly disclose this feature. However, *Hamade* discloses this feature, and a POSITA would have been motivated, in view of *Hamade*, to modify the combined *Inoue-Min* system discussed in Section IX.C.1(b) to include a plurality of read amplifiers at respective columns of the memory, with each column read amplifier being associated with only one latch circuit ("a local column read amplifier"). (*See Supra*, Section VIII.B; Ex.1002, ¶174.)

For reasons similar to those discussed above in Section IX.A.1(c), a POSITA would have looked to *Hamade* to augment and improve the capabilities of

the combined *Inoue-Min* system that includes the circuit of figure 3 of *Inoue*. (Ex.1002, ¶175.) Having looked to *Hamade*, a POSITA would have been motivated to modify the combined *Inoue-Min* system discussed above in Section IX.C.1(b) to implement *Hamade*'s drive circuit 9 at *each* column for reasons similar to those discussed above in Section IX.A.1(c). As a non-limiting example, below is a demonstrative showing certain aspects of the combined *Inoue-Min-Hamade* system that a POSITA would have found to be consistent with the above modification. (*Id*.)



(Ex.1002, ¶175, citing Ex.1007, FIG. 6; Ex.1008, FIG. 3B; Ex.1009, FIG. 1 (annotated).)

A POSITA would have been motivated to configure the drive circuit 9 of each column in the combined system in a similar manner as discussed above in

Section IX.A.1(c) to ensure proper operation of the memory in accordance with the disclosure of *Hamade*. Based on the disclosures of *Inoue*, *Min*, and *Hamade*, a POSITA would have known how to assemble and implement all the above circuitry into the combined system without undue experimentation. (Ex.1002, ¶176.)

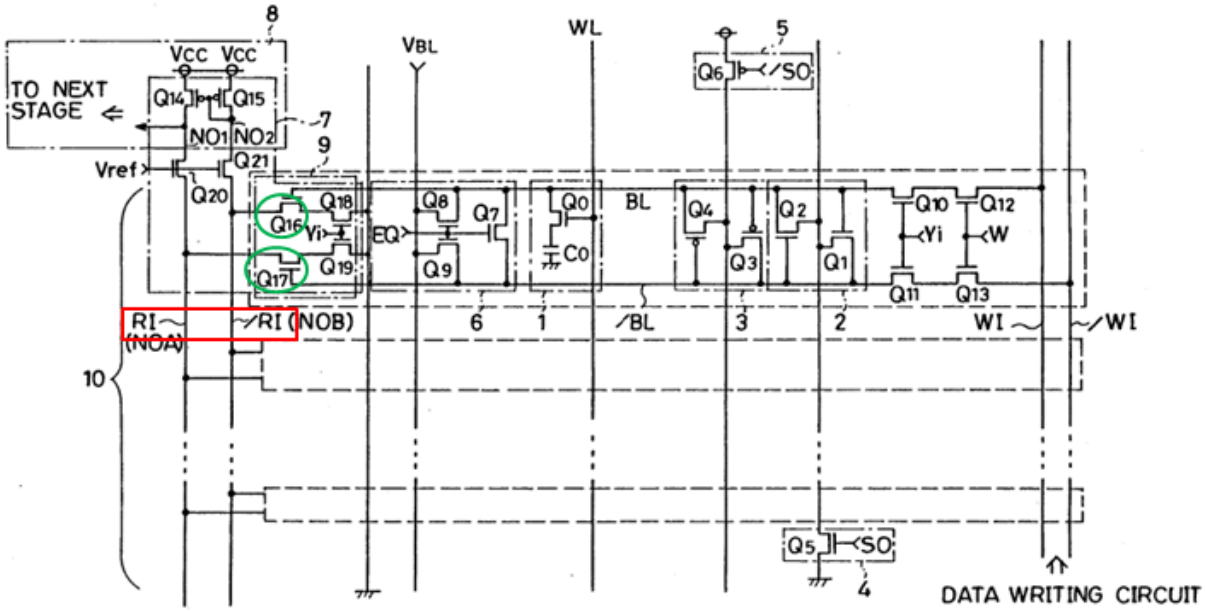
As is apparent from the above exemplary demonstrative, the combined *Inoue-Min-Hamade* system discloses a "local column read amplifier" "for each of a plurality of sense amplifiers," as there is a read amplifier (drive circuit 9) for each sense amplifier and corresponding column, and each column read amplifier is associated with only one latch circuit. (Ex.1002, ¶177; *see Supra*, Sections VIII.B, IX.A.1(c).)

A POSITA would have further understood that drive circuit 9, as combined with *Inoue-Min* as discussed in Section IX.C.1(b), would have included the gates of NMOS transistors Q16 and Q17 (green below) coupled to nodes N_1 and N_2 of figure 3 of *Inoue*, respectively, because gates of transistors Q17 and Q16 in drive circuit 9 receive the bit line signals (Ex.1009, FIG. 1), and *Inoue*'s N_1 and N_2 correspond to bit lines for each sense amplifier in the *Inoue-Min-Hamade* system (Ex.1007, 3, 4, FIG. 6; *see Supra*, Sections IX.A.1(c),IX.C.1(a) (regarding nodes N_1 and N_2 of *Inoue*'s figure 3 being the same as nodes N_1 and N_2 of figure 6); Ex.1002, ¶178.). Therefore, the combined system discloses "a local column read

amplifier **responsively coupled to the sense amplifier**" (emphasis added). (*See* similar analysis above in Section IX.A.1(c)).

Moreover, as is again apparent from the demonstrative above, the drive circuit 9 ("local column read amplifier") would have received signals on read only data lines RI and /RI ("receiving at least one data read signal") in the combined system. (*See Supra*, Section IX.A.1(c); *see also* Ex.1009, FIG. 1 (annotated below), 7:35-39.)

FIG. 1



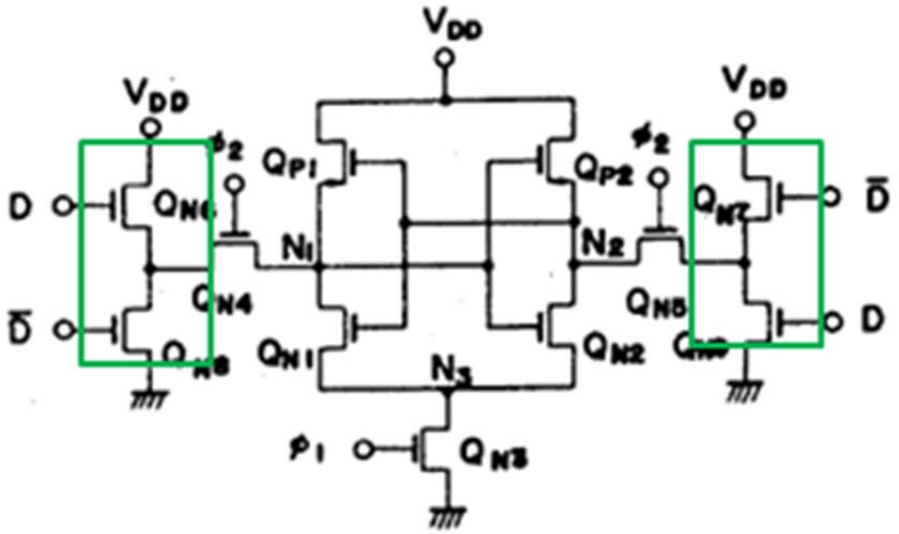
(Ex.1002, ¶179, citing Ex.1009, FIG. 1 (annotated).)

d) Claim Element 4(d)

The combined *Inoue-Min-Hamade* system as set forth in Section IX.C.1(c) discloses or suggests this feature. (Ex.1002, ¶¶180-181.) The local data write

driver circuits identified for figure 6 of *Inoue* in Section IX.A.1(d) above are the same in figure 3 of *Inoue*. Both figures 3 and 6 of *Inoue* include two data write circuits Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} (each of which corresponds to "a local data write driver circuit") that are associated with only a single latch circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}). (Ex.1007, 3, FIGs. 3, 6.) The data write circuits receive the same inputs and each data write circuit is coupled to the latch in figure 3 of *Inoue* in the same manner as in figure 6 of *Inoue*. Therefore, for the same reasons set forth in Section IX.A.1(d) above, the *Inoue-Min-Hamade* combination of Section IX.C.1(c) discloses a pair of local data write driver circuits for each sense amplifier as shown highlighted in green in the annotated figure 3 of *Inoue* below:

第 3 図



(Ex.1002, ¶180, citing Ex.1007, FIG. 3 (annotated to show local data write driver

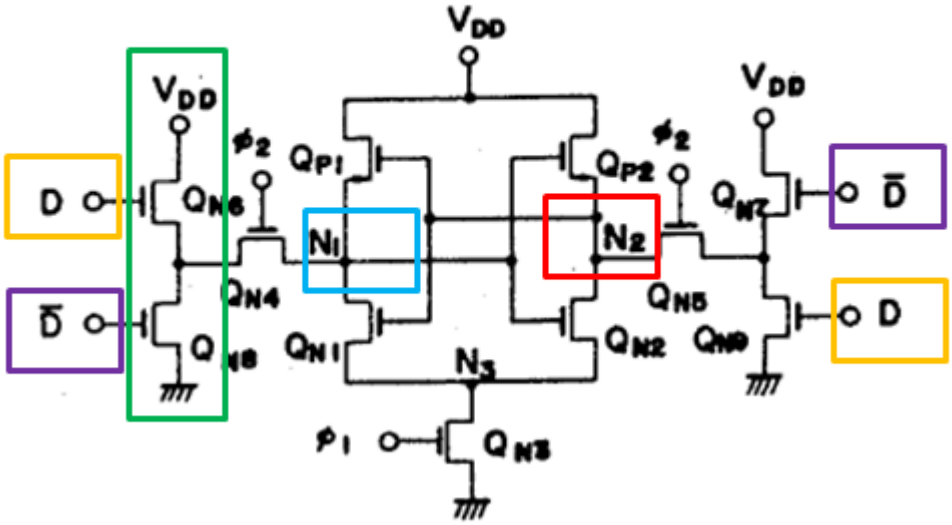
circuits (green)).)

Moreover, also for the same reasons presented above in Section IX.A.1(d), the combined *Inoue-Min-Hamade* system of Section IX.C.1(c) discloses the remaining aspects of this feature in claim 4. (Ex.1002, ¶181*; see Supra*, Sections IX.A.1(d),IX.C.1(c).)

2. Claim 8

As discussed above in Section IX.C.1(d), the local write driver circuits disclosed in figure 3 of *Inoue* are the same as those disclosed in figure 6. As such, for the same reasons provided in Section IX.A.5, the *Inoue-Min-Hamade* system discussed in Section IX.C.1(c) discloses the features of this claim. (Ex.1002, ¶¶182-184.)

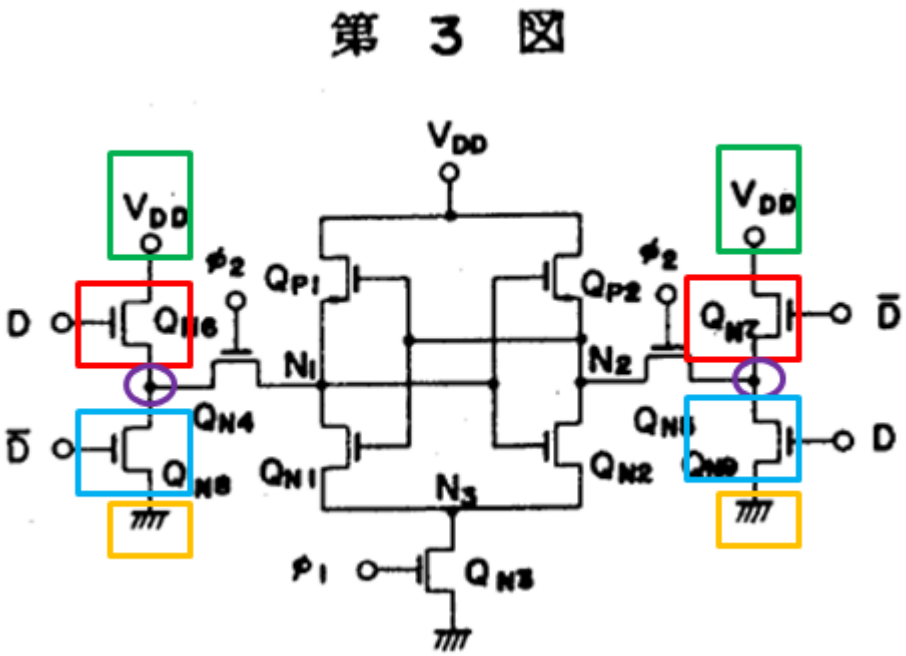
第 3 図



(Ex.1002, ¶183, citing Ex.1007, FIG. 3 (annotated).)

3. Claim 9

As discussed above in Section IX.C.1(d), the local write driver circuits disclosed in figure 3 of *Inoue* are the same as those disclosed in figure 6. As such, for the same reasons provided in Section IX.A.6, the *Inoue-Min-Hamade* system discussed in Section IX.C.1(c) discloses the features of this claim. (Ex.1002, ¶¶185-187.)

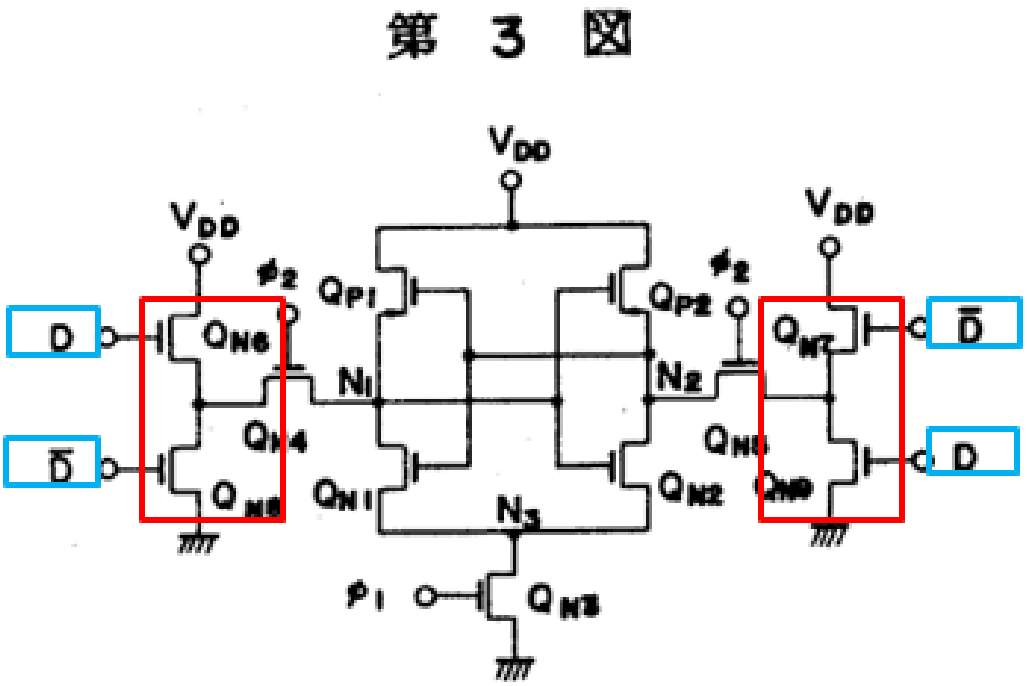


(Ex.1002, ¶186, citing Ex.1007, FIG. 3 (annotated).)

4. Claim 14

As discussed above in Section IX.C.1(d), the local write driver circuits disclosed in figure 3 of *Inoue* are the same as those disclosed in figure 6. As such, for the same reasons provided above in Section IX.A.8 the *Inoue-Min-Hamade*

system discussed in Section IX.C.1(c) discloses the features of this claim. (Ex.1002, ¶¶188-190.)

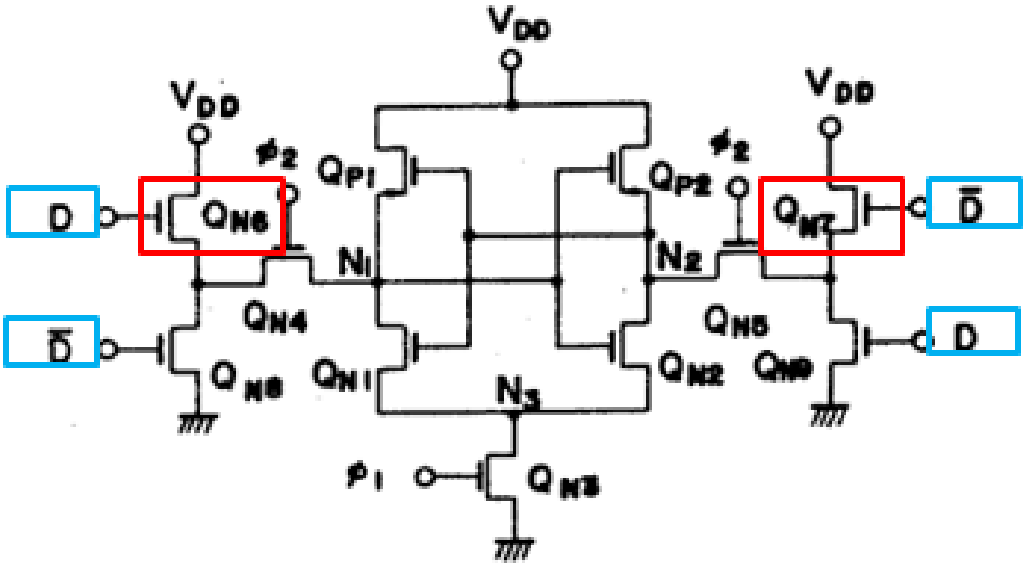


(Ex.1002, ¶189, citing Ex.1007, FIG. 3 (annotated).)

5. Claim 15

As discussed above in Section IX.C.1(d), the local write driver circuits disclosed in figure 3 of *Inoue* are the same as those disclosed in figure 6. As such, for the same reasons provided in Section IX.A.9, the *Inoue-Min-Hamade* system discussed in Section IX.C.1(c) discloses the features of this claim. (Ex.1002, ¶¶191-193.)

第 3 図

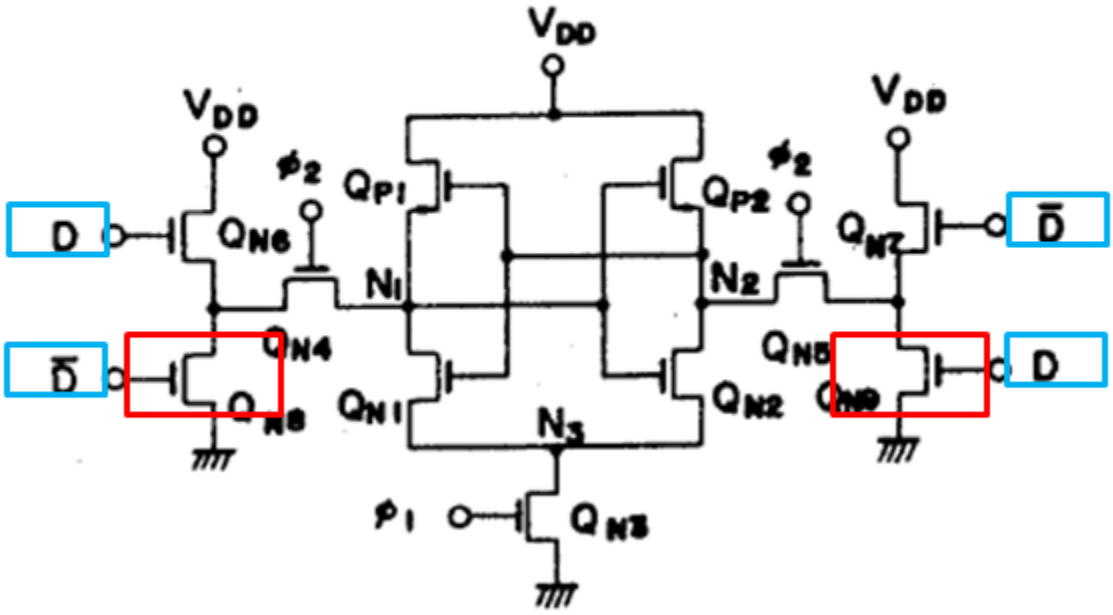


(Ex.1002, ¶192, citing Ex.1007, FIG. 3 (annotated).)

6. Claim 16

As discussed above in Section IX.C.1(d), the local write driver circuits disclosed in figure 3 of *Inoue* are the same as those disclosed in figure 6. As such, for the same reasons provided in Section IX.A.10, the *Inoue-Min-Hamade* system discussed in Section IX.C.1(c) discloses the features of this claim. (Ex.1002, ¶¶194-196.)

第 3 図



(Ex.1002, ¶195, citing Ex.1007, FIG. 3 (annotated to show transistor Q_{N9} in red at right, transistor Q_{N8} in red at left, and signals D and $\overline{D}$ in blue).)

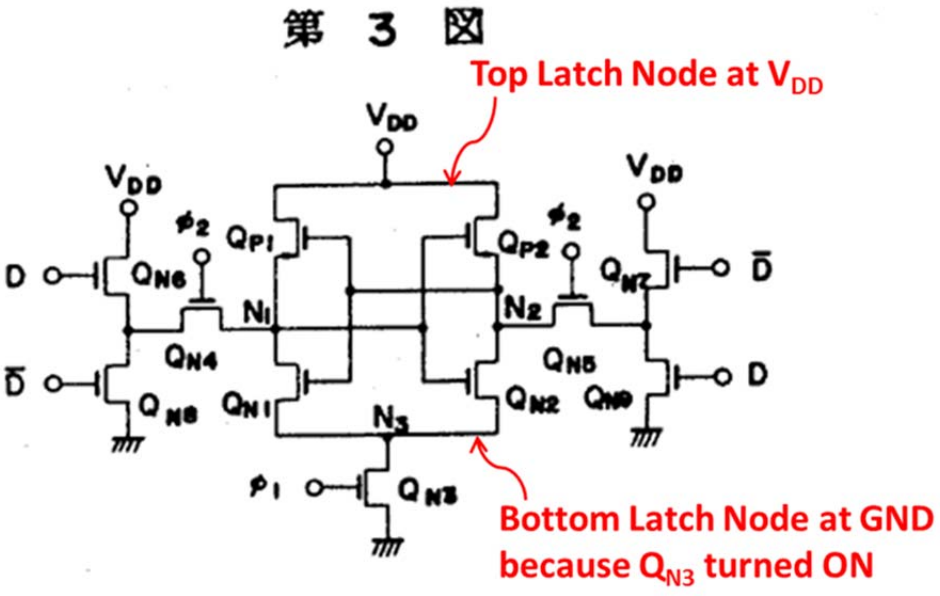
7. Claim 17

a) "The sense amplifier arrangement of claim 16 wherein said first and second data write signals are complementary signals for writing data into an active block."

The combined *Inoue-Min-Hamade* system discussed in Section IX.C.1(c) discloses or suggests this feature. (Ex.1002, ¶¶197-199.) *Inoue* discloses that the circuit of figure 3 operates in a manner similar to figure 1. (Ex.1007, 3.) *Inoue* discloses with respect to figure 1, which also applies to figure 3, that the signals at write data input terminal D ("said first data write signal") and write data input

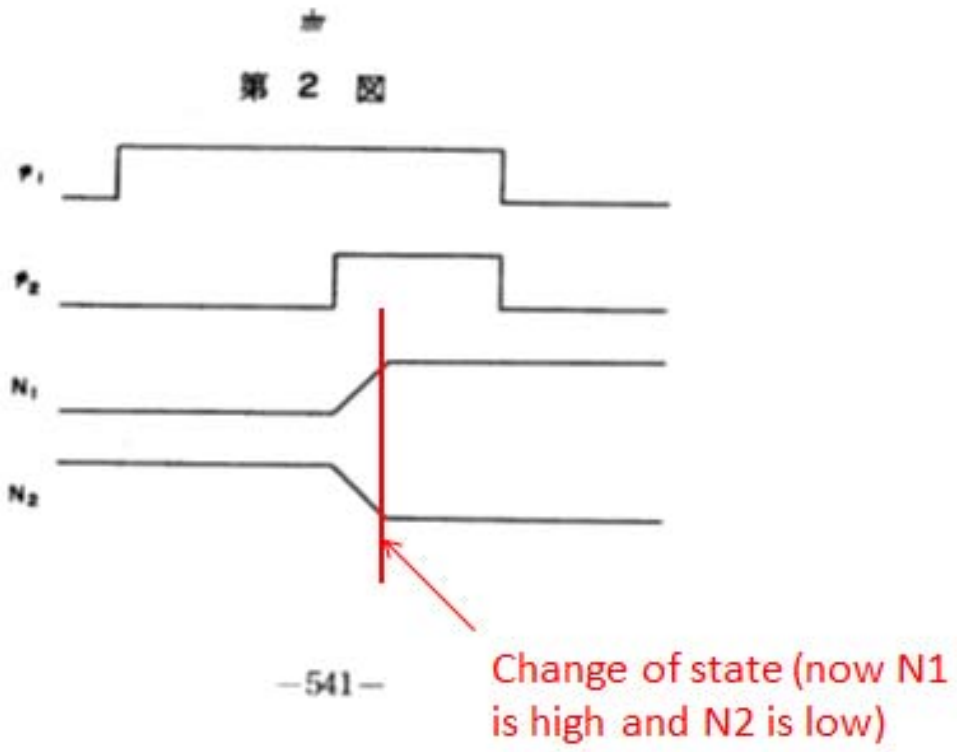
terminal $\overline{D}$ ("second data write signal") are complementary signals at the time of writing because when D is a high, $\overline{D}$ is a low. (*Id.*)

Furthermore, *Inoue* discloses that when data is written to nodes N1 and N2, the latch (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) is active, *i.e.*, D and $\overline{D}$ are complementary signals for writing data "into an active memory block." (Ex.1002, ¶198.) According to the '574 patent, an active memory block refers to a latch circuit whose top and bottom nodes are connected to Vcc and GND, respectively. (Ex.1001, 4:32-34, 6:24-26, FIG. 4.) In *Inoue*, when node N1 transitions from state I ("L") to state II ("H"), *i.e.*, during writing, the top latch node and the bottom latch node are at VDD and GND, respectively. (Ex.1007, 3; *see id.*, FIG. 3 (annotated below).)



(Ex.1002, ¶198, citing Ex.1007, FIG. 3 (annotated).)

Figure 2 further confirms that when N1 and N2 change state, Q_{N3} is turned ON because ϕ_1 is high ("H"), which indicates that node N_3 is pulled down to ground. (Ex.1007, FIG. 2; Ex.1002, ¶¶26-33, 199.)



(Ex.1002, ¶199, citing Ex.1007, FIG. 2 (annotated).)

D. Ground 4: *Inoue*, *Min*, *Hamade*, and *Ogawa* Render Obvious Claim 18 of the '574 Patent

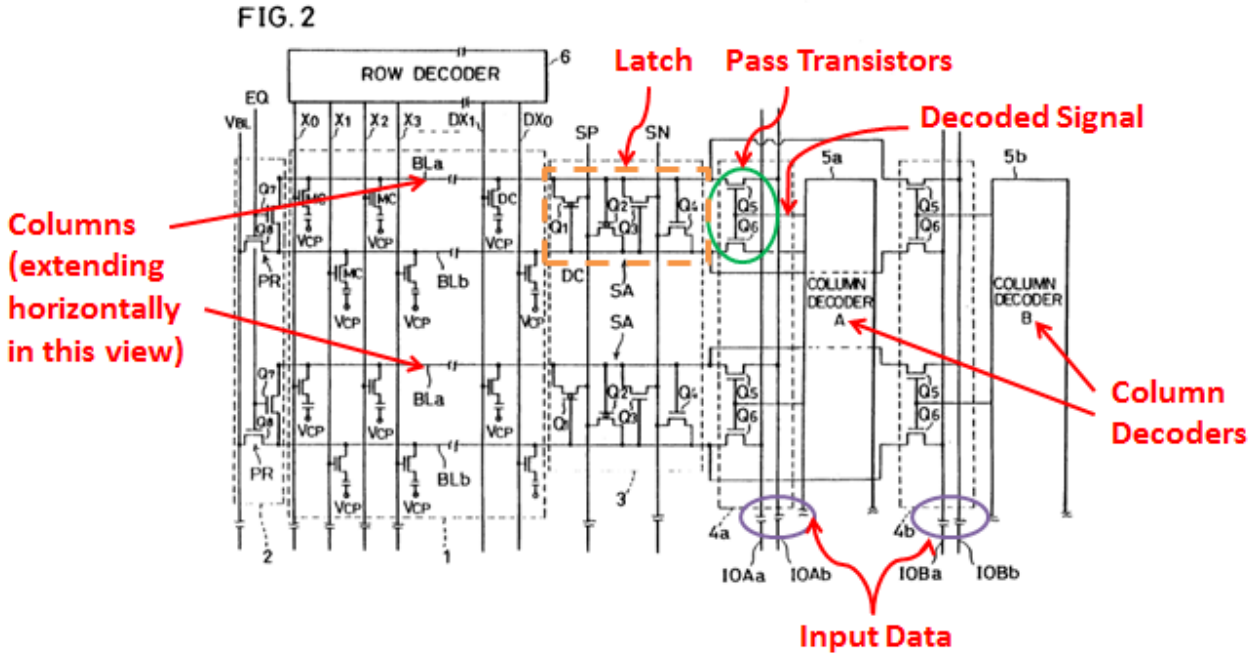
Inoue in combination with *Min*, *Hamade*, and *Ogawa* discloses or suggests all of the features of claim 18 of the '574 patent.

1. Claim 18

a) "The sense amplifier arrangement of claim 17 wherein said first and second data write signals are controlled to have a same value when no write is to occur to a memory cell for the sense amplifier."

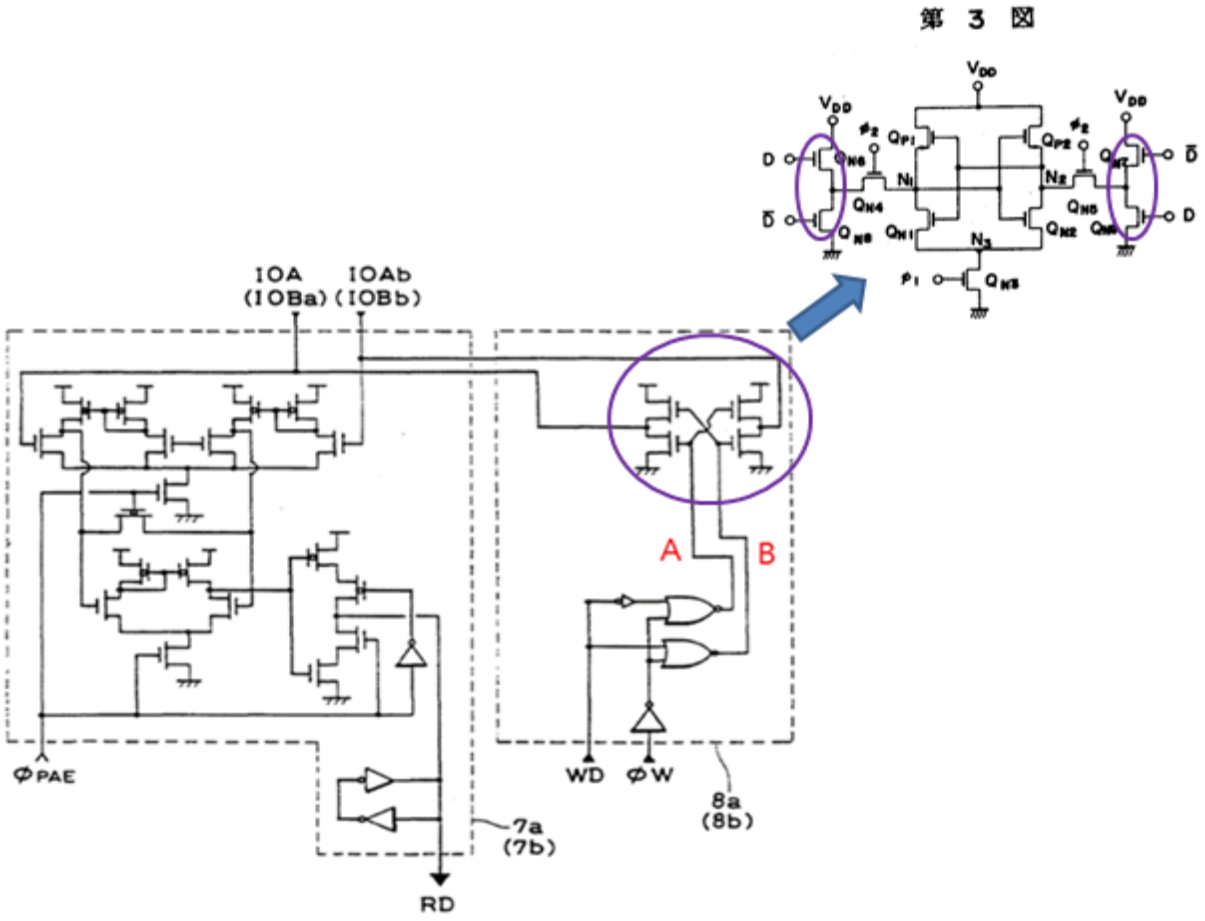
Inoue in combination with *Min*, *Hamad*e, and *Ogawa* discloses this feature. (Ex.1002, ¶201-208.) *Inoue*, in the context of figure 3, discloses that D and $\overline{D}$ (the data write terminals) control writing of data into the sense amplifier latch. (*See Supra,* Sections IX.C.1(d), IX.C.2-7.) However, the combined *Inoue-Min-Hamade* system discussed above with respect to claim 17 does not disclose how input data (e.g., from an I/O line) is presented to D and $\overline{D}$. For instance, if a '1' has to be written to the latch, *Inoue*, *Min*, and *Hamade* do not disclose how D and $\overline{D}$ are driven by the input data. *Ogawa* discloses this feature as discussed below.

Ogawa discloses that the input data for writing to the latch is provided along I/O buses IOA or IOB. (Ex.1010, 8:1-4, FIG. 2.)



(Ex.1002, ¶202, citing Ex.1010, FIG. 2 (annotated).)

The data on I/O buses IOA and IOB is generated by a write driver 8a (8b). (Ex.1010, 7:66-8:4, FIG. 5.) The circuitry in the lower half (i.e., the two NOR gates and inverter) of write driver 8a and 8b provides the inputs (annotated as "A" and "B" below) to the data write circuits (the four NMOS transistors in the top half of 8a) based on input data. (Ex.1010, FIG. 5, 8:59-62.) The correspondence between *Inoue*'s data input buffer transistors Q_{N6}-Q_{N9} (Ex.1007, 4) and *Ogawa*'s data write circuits (the four NMOS transistors in the top half of 8a) is illustrated in *Ogawa*'s FIG. 5 below that includes *Inoue*'s FIG. 3. A POSITA would have understood that "A" and "B" (as shown below) would correspond to D and $\overline{D}$ in FIG. 3 of *Inoue* when combined. (Ex.1002, ¶203.)



(Ex.1002, ¶203, citing Ex.1010, FIG. 5 (annotated) with superimposed Ex.1007, FIG. 3 (annotated).)

Based on the FIG. 5 configuration of *Ogawa*, the signals indicated by "A" and "B" would have the following values based on the values of write data WD and ϕW:

WD	**ϕW**	**A**	**B**
0	0	0	0
0	1	0	1
1	0	0	0

1 1 1 0

(Ex.1002, ¶204, citing Ex.1010, 8:59-62.)

As seen from the table, when ϕW is low, which a POSITA would have understood means that no write is to occur, A and B (i.e., the signals corresponding to D and $\overline{D}$ in *Inoue*) have the same value ('0'). (Ex.1002, ¶205.)

In view of *Ogawa*, a POSITA would have been motivated to modify the combined *Inoue-Min-Hamade* system discussed with respect to claim 17 above to include first and second signals that are controlled to have a same value when no write is to occur to a memory cell for the sense amplifier. (Ex.1002, ¶¶206-207.) A POSITA would have found it obvious to *Ogawa* to refine the combined *Inoue-Min-Hamade* system, e.g., regarding setting values for signals disclosed in *Inoue*. (*Id*.)

First, combining the teachings of the *Inoue-Min-Hamade* combination (discussed above in Section IX.C.1(c)) and *Ogawa* would have constituted no more than a combination of familiar elements by known methods where the combined elements continue to perform the same function they did separately. (Ex.1002, ¶207.) *KSR*, 550 U.S. at 416. *Inoue* discloses that D and $\overline{D}$ (the data write terminals) control writing of data into the sense amplifier latch. But *Inoue*, *Min*, and *Hamade* do not disclose how input data (e.g., from an I/O line) is presented to

D and $\overline{D}$. Accordingly, the addition of circuitry from *Ogawa*, which performs the same function of generating data write signals, to the combined *Inoue-Min-Hamade* system constitutes a combination of known elements where the known elements perform the same functions they did prior to their combination. In the combined *Inoue-Min-Hamade-Ogawa* system, the data write signals have the same value ('0') when no write is to occur. (Ex.1002, ¶207.)

Second, the combination of *Ogawa* with the *Inoue-Min-Hamade* combination would have reduced erroneous data writes into the latch. For instance, in *Inoue*, data can only be written to the latch when clock ϕ_2 goes high. (Ex.1007, 3.) But if the metal line that carries ϕ_2 in the DRAM is shared between many sense amplifiers or if ϕ_2 becomes high due to transients on neighboring metal lines, data can be written out of turn into the latch based on the voltages at D and $\overline{D}$. (Ex.1002, ¶208.) Such problems can be avoided by shutting off Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} when the latch does not have to be written to, which is exactly what *Ogawa* does by controlling ϕW to be a '0' when no writing is to occur. (*Id*.) *KSR*, 550 U.S. at 416-17.

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 4-18 and 21-27 of the ’574 patent based on the grounds specified in this petition.

Respectfully submitted,

Dated: May 12, 2017 By: /Naveen Modi/
Naveen Modi (Reg. No. 46224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,208,574 contains, as measured by the word-processing system used to prepare this paper, 13,829 words. This word count does not include the items excluded by 37 C.F.R. § 42.24(a).

Respectfully submitted,

Dated: May 12, 2017

By: /Naveen Modi/
Naveen Modi (Reg. No. 46224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on May 12, 2017, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,208,574 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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