Paper No. __
Filed: May 12, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,208,574

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,208,574

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Ex.1001	U.S. Patent No. 6,208,574
Ex.1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex.1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex.1004	Prosecution History of U.S. Patent Application No. 08/432,884
Ex.1005	Prosecution History of U.S. Patent Application No. 07/976,312
Ex.1006	Prosecution History of U.S. Patent Application No. 08/284,183
Ex.1007	Japanese Patent Publication JPS58-128087 ("*Inoue*") including English-language translation, Japanese Publication English Abstract, Japanese-language version, translation certification, and certification of correction to certified translation
Ex.1008	UK Patent Application G.B. 2246005A ("*Min*")
Ex.1009	U.S. Patent No. 5,323,349 ("*Hamade*")
Ex.1010	RESERVED
Ex.1011	Taur *et al.*, Fundamentals of Modern VLSI Devices, 1998, including title page, copyright page, and chapters 1, 3, and 4 ("*Taur*")
Ex.1012	U.S. Patent No. 4,980,799 to Tobita et al. ("*Tobita*")

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-3 and 30-37 of U.S. Patent No. 6,208,574 ("the '574 patent") (Ex.1001), which is currently assigned to ProMOS Technologies, Inc. ("Patent Owner") according to PTO records. For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Austin Semiconductor, LLC, and Samsung Semiconductor, Inc.

Related Matters: Patent Owner has asserted the '574 patent against Petitioner and the other above real parties-in-interest in *ProMOS Technologies, Inc. v. Samsung Electronics, Ltd., Co.*, Case No. 1:16-cv-00335-SLR-SRF (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 6,069,507 ("the '507 patent"), 6,172,554 ("the '554 patent"), 6,562,714 ("the '714 patent"), 7,375,027 ("the '027 patent"), and 6,559,044 ("the '044 patent") in this action. Petitioner is concurrently filing another IPR petition challenging claims 4-18 and 21-27 of the '574 patent as well as additional IPR petitions challenging certain claims of the '507, '554, '714, '027, and '044 patents. Petitioner also previously filed several

IPR petitions involving additional patents asserted by Patent Owner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Specifically, on October 7, 2016, Petitioner filed IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. All of these proceedings were instituted and remain pending except for the 00033 and 00035 proceedings. Moreover, the '574 patent is in the same family as U.S. Patent No. 6,088,270 ("the '270 patent"), which is at issue in IPR2017-00036 in which the Board recently instituted *inter partes* review.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '574 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

A. Claims for Which Review is Requested

Petitioner respectfully requests review of claims 1-3 and 30-37 ("challenged claims") of the '574 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following ground:

Ground 1: Claims 1-3 and 30-37 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Japanese Patent Publication JPS58-128087 to Inoue *et al.* ("*Inoue*") (Ex.1007),[1] UK Patent Application Publication No. G.B. 2246005A to Min *et al.* ("*Min*") (Ex.1008), and U.S. Patent No. 5,323,349 to Hamade *et al.* ("*Hamade*") (Ex.1009).

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[1] Ex.1007 is a compilation containing the English-language translation of *Inoue* (Ex.1007, 1-5), followed by the Japanese language version (*id.*, 6-10), an affidavit required by 37 C.F.R. § 42.63(b) (in the form of a declaration as permitted by 37 C.F.R. § 42.2) (*id.*, 11), and a certification of correction to the certified translation (*id.*, 12).

The '574 patent issued from U.S. Application No. 08/432,884 filed May 2, 1995, which claims priority to U.S. Application No. 07/976,312 filed on November 12, 1992. *Inoue* was published on July 30, 1983. Thus, *Inoue* is prior art to the '574 patent at least under pre-AIA 35 U.S.C. § 102(b). *Min* was published on January 15, 1992, and is thus prior art to the '574 patent at least under pre-AIA 35 U.S.C. § 102(a). *Hamade* issued June 21, 1994 from U.S. Application No. 936,454 filed August 28, 1992. Thus, *Hamade* is prior art to the '574 patent at least under pre-AIA 35 U.S.C. § 102(e). *Inoue, Min*, and *Hamade* were never considered by the Patent Office during prosecution of the '574 patent. (Ex.1001, 1 (References Cited).)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '574 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in design of semiconductor memory circuits. (Ex.1002, ¶20.)[2] More education can supplement practical experience and vice versa. (*Id*.)

[2] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex.1002), an expert in the field of the '574 patent. (Ex.1002, ¶¶5-15; Ex.1003.)

VII. OVERVIEW OF THE '574 PATENT AND PRIOR ART

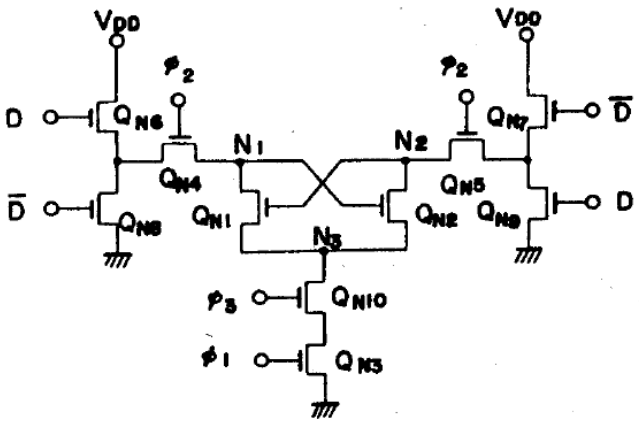
A. The '574 Patent

The '574 patent relates to a "sense amplifier for a very high density integrated circuit memory using CMOS technology." (Ex.1001, Abstract; Ex.1002, ¶¶38-42.) The '574 patent acknowledges that sense amplifiers were known at the time of the alleged invention. (Ex.1001, Title, FIG. 1, 1:47-2:13.) The '574 patent further acknowledges that it was known for integrated circuit memories to be organized into rows and columns and for a sense amplifier to be connected to each column of the memory. (*Id.*, 1:14-41, 1:47-48, 2:12-14, FIG. 1; Ex.1002, ¶38.) The '574 patent discloses a preferred embodiment of a sense amplifier 100 in connection with figure 5. (Ex.1001, 1:46-62, 6:3-9, 6:32-63, 6:66-7:13, 7:42-46, FIGS. 1, 5; Ex.1002, ¶39.) As discussed in detail in Section IX, however, all of these features described and claimed in the '574 patent were known in the prior art.

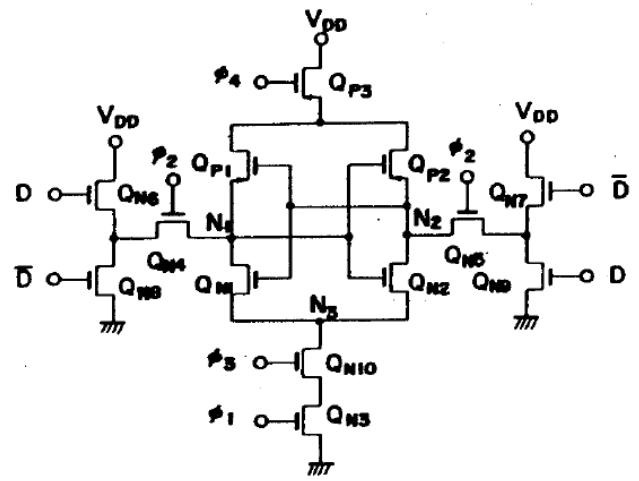
B. *Inoue*

Inoue discloses a semiconductor device including a sense amplifier with internal nodes and a flip-flop circuit capable of latching into two states (states I and II). (Ex.1007, 1 (Claim 1), 3; Ex.1002, ¶¶57-60.) *Inoue* discloses two configurations in figures 4 and 6 that are designed to consume a small amount of transient power when writing to a flip-flop. (Ex.1007, 3; Ex.1002, ¶57.)

第 4 図



第 6 図

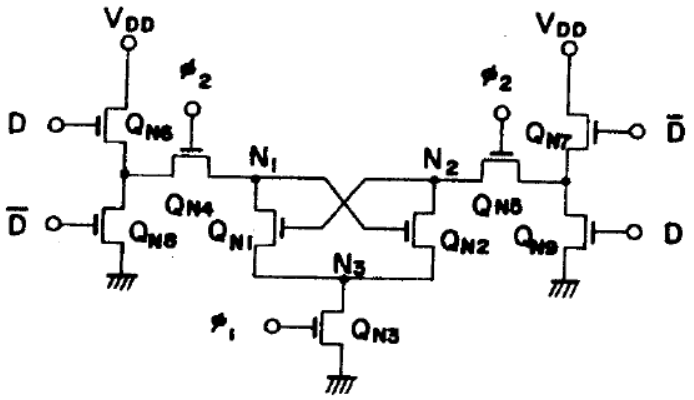


(Ex.1007, FIGS. 4, 6.[3])

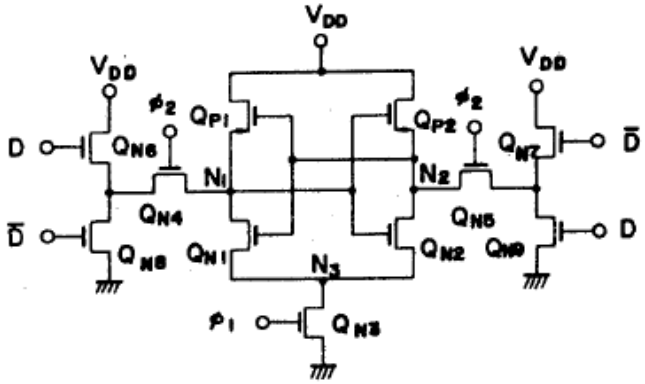
[3] In this Petition, Petitioner refers to the text of the English translation of *Inoue*, but sometimes may show figures from the Japanese version because those figures are clearer.

The two embodiments in figures 4 and 6 of *Inoue* build on conventional flip-flops shown in figures 1 and 3, respectively.

第 1 図



第 3 図



(Ex.1007, 5, FIGS. 1, 3; Ex.1002, ¶58.)

Inoue's first embodiment in figure 4 adds to the conventional flip-flop of figure 1 a transistor Q_{N10} for pulling down node N_3. (Ex.1007, 3-5, FIGS. 1, 4; Ex.1002, ¶59.) The "embodiment [of FIG. 6] differs from FIG. 4 in the addition of a P-channel transistor Q_{P3}," which is controlled by clock ϕ_4, and also in the addition

of PMOS transistors Q_{P1} and Q_{P2} as in the circuit of figure 3. (Ex.1007, 4, 5, FIGS. 3, 4, 6; Ex.1002, ¶59.) Much of the functionality of figure 6 is described at the portion of *Inoue* pertaining to figure 4, so *Inoue* does not repeat that description when describing figure 6. (Ex.1007, 4; Ex.1002, ¶59.) Figure 6 of *Inoue* differs from the circuit of figure 3 in the addition of pull-up transistor Q_{P3} and pull-down transistor Q_{N10}. (Ex.1007, 3-5, FIGS. 3, 6; Ex.1002, ¶59.) Like figure 3, figure 6 contains P channel transistors Q_{P1} and Q_{P2} and N channel transistors Q_{N1} and Q_{N2} within the flip-flop. (Ex.1007, 5, FIGS. 3, 6; Ex.1002, ¶59.)

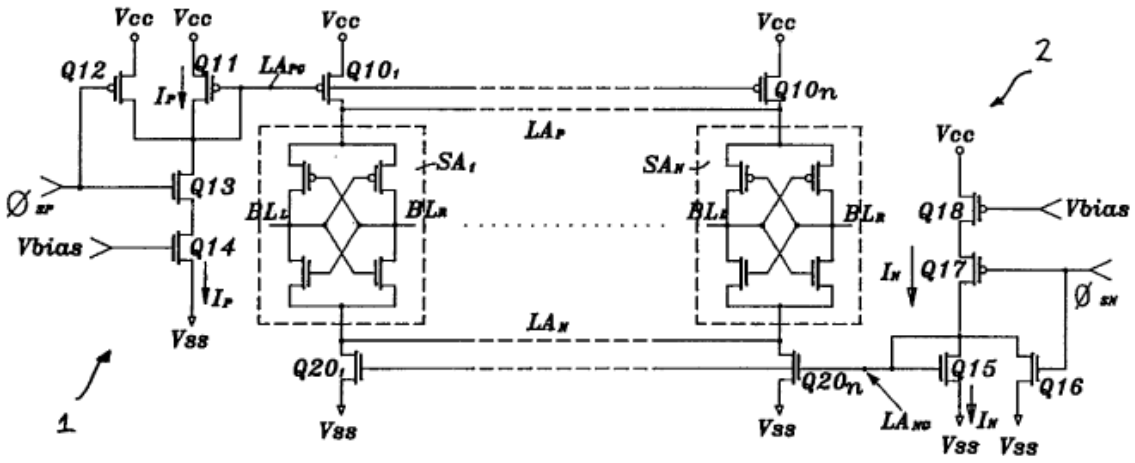
Inoue discloses that the flip-flop of figure 6 latches into one of two stable states, corresponding to node N_1 at a level 'H' and node N_2 at a level 'L' in a first state or vice-versa in the second state. (Ex.1007, 3; Ex.1002, ¶60.) A POSITA would have understood that a flip-flop such as in figure 6 of *Inoue* is a latch circuit, which is consistent with the understanding of such circuitry as discussed in the '574 patent. (Ex.1002, ¶60; Ex.1001, 1:58-62, 2:6-14, 6:5-13, FIGS. 1, 5.)

C. *Min*

Min, which like *Inoue* is in the field of semiconductor memory (Ex.1002, ¶61), discloses a semiconductor memory device having a plurality of sense amplifiers SA_1-SA_N. (Ex.1008, FIG. 3B.) Each sense amplifier SA_i in figure 3B of *Min* is coupled to a corresponding bit line pair and is coupled to a positive

power supply (Vcc) and to ground (Vss) via driving transistors $Q10_i$ and $Q20_i$, respectively. (*Id.*, 21:1-13, FIG. 3B; Ex.1002, ¶61.)

FIG. 3B



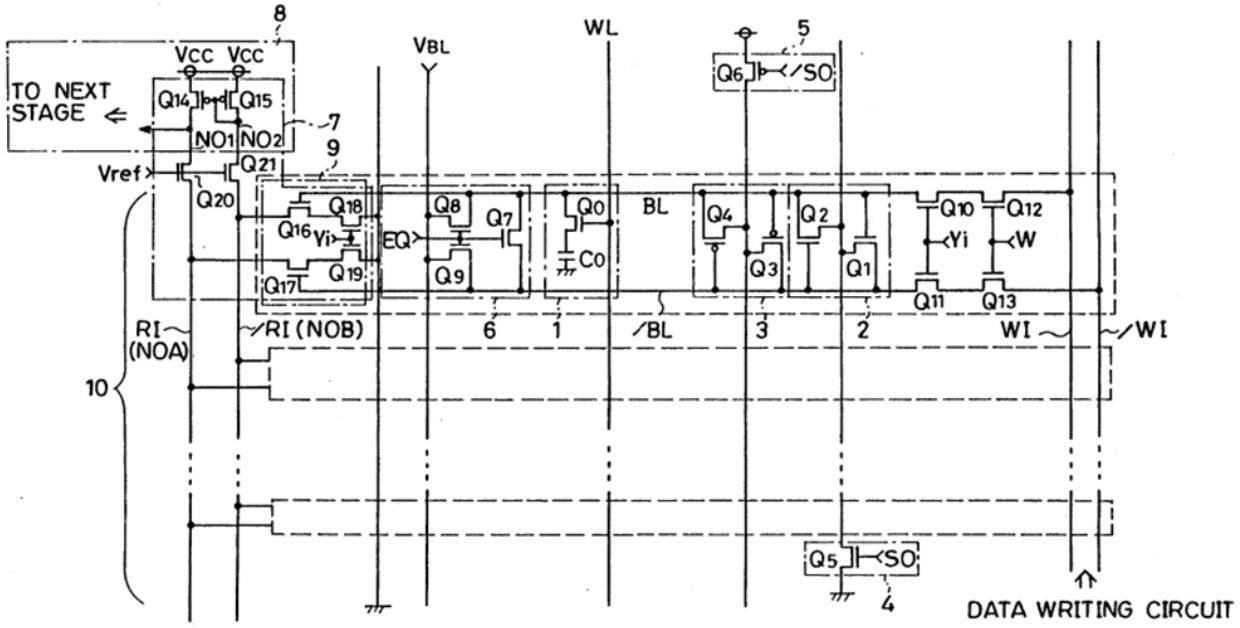
(Ex.1002, FIG. 3B.)

D. *Hamade*

Hamade discloses circuitry for "implementing a high speed operation of semiconductor memory devices." (Ex.1009, 1:8-14, 1:17-19; Ex.1002, ¶¶62-65.) *Hamade*'s figure 1 embodiment includes drive circuit 9 "provided for each bit line pair and amplifies the potentials of the associated bit lines." (Ex.1009, 7:17-19; Ex.1002, ¶62.) Various other components (e.g., sense amplifiers 2 and 3, bit line pair BL, /BL, read only data lines RI, /RI, and word line WL) are also included. (Ex.1009, FIG. 1, 7:10-8:27; Ex.1002, ¶65.) *Hamade* discloses that "[w]hen column selecting signal Yi rises from the low level to the high level, transistors

Q18 and Q19 are turned on, and amplifier 7 of the current mirror type formed of transistors Q14-Q19 is activated" and "[t]hus, the potential of each of nodes NOB and N02 on read only data line /RI is discharged toward the ground potential in order to amplify a minute potential difference appearing between bit lines BL and /BL." (Ex.1009, 8:24-31.)

FIG. 1



(*Id.*, FIG. 1; *see also* Ex.1002, ¶64.)

VIII. CLAIM CONSTRUCTION

The '574 patent is set to expire on March 27, 2018. Therefore, the '574 patent will expire within 18 months from entry of any notice of filing date issued in this proceeding should the Board institute review. *See* 37 C.F.R. § 42.100(b). Accordingly, the claims of the '574 patent should be construed under the standard

set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See, e.g.*, *Square Inc. v. J. Carl Cooper*, IPR2014-00156, Paper No. 38 at 7 (May 14, 2015) (citing *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)). Under *Phillips*, claim terms are given their ordinary and customary meanings, as would be understood by a POSITA, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *See, e.g.*, *Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 20 at 2-3 (July 10, 2014). The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Below, Petitioner discusses the construction of three terms. Any term not construed below should be interpreted in accordance with its plain and ordinary meaning.[4] Petitioner has applied these understandings in its analysis of the '574

[4] Petitioner reserves all rights to raise claim construction and other arguments in other proceedings, including the pending district court litigation (*supra* Section II). For example, Petitioner has not necessarily raised all challenges to the '574 patent, including challenges to the claims under 35 U.S.C. § 112, given the limitations placed by the Rules.

patent.

A. "local data write driver circuit"

For purposes of this proceeding, the phrase "local data write driver circuit," which appears in each independent claim (claims 1, 4, and 30), should be construed as "a data write driver circuit that is associated with only one latch circuit." The Board previously adopted this construction for this same claim term in an IPR pertaining to the '270 patent, which is in the same family as the '574 patent. *Samsung Elecs. Co., Ltd. v. ProMOS Techs., Inc.*, IPR2017-00036, Paper No. 6 at 8 (Apr. 6, 2017). The intrinsic record supports Petitioner's construction. (Ex.1002, ¶¶44-47.)

The plain language of the claims supports this construction. (*Id.*, ¶45.) Claim 1, for instance, states that "**each** said sense amplifier is coupled to a pair of said local data write driver circuits" where "each sense amplifier compris[es] a latch circuit." (Ex.1001, 13:24-25, 12:61.) Similarly, claim 4 recites that "a local data write drive circuit" is provided for "each of a plurality of sense amplifiers" having a "sense amplifier latch circuit." (*Id*., 13:46-58.) Claim 30 also recites that "first and second local data write drive circuits" are provided for "each of a plurality of sense amplifiers" having a "sense amplifier latch circuit." (*Id*., 15:52—16:5.)

The specification supports Petitioner's construction. (Ex.1002, ¶46.)

Throughout the specification, a local write driver circuit or its constituent components are described as being connected to, or associated with, a single latch circuit. For instance, figure 5 of the '574 patent discloses a sense amplifier 100 including data write driver circuits ("local" data write transistors 128/130 and 132/134) connected to a single latch circuit (transistors 112, 114, 118, 120). (Ex.1001, 6:5-13, 7:15-16; *see also id*., FIG. 5 (annotated below), 4:61-63 ("The present invention provides a CMOS sense amplifier with local write driver transistors . . . ."), 5:29-36.)

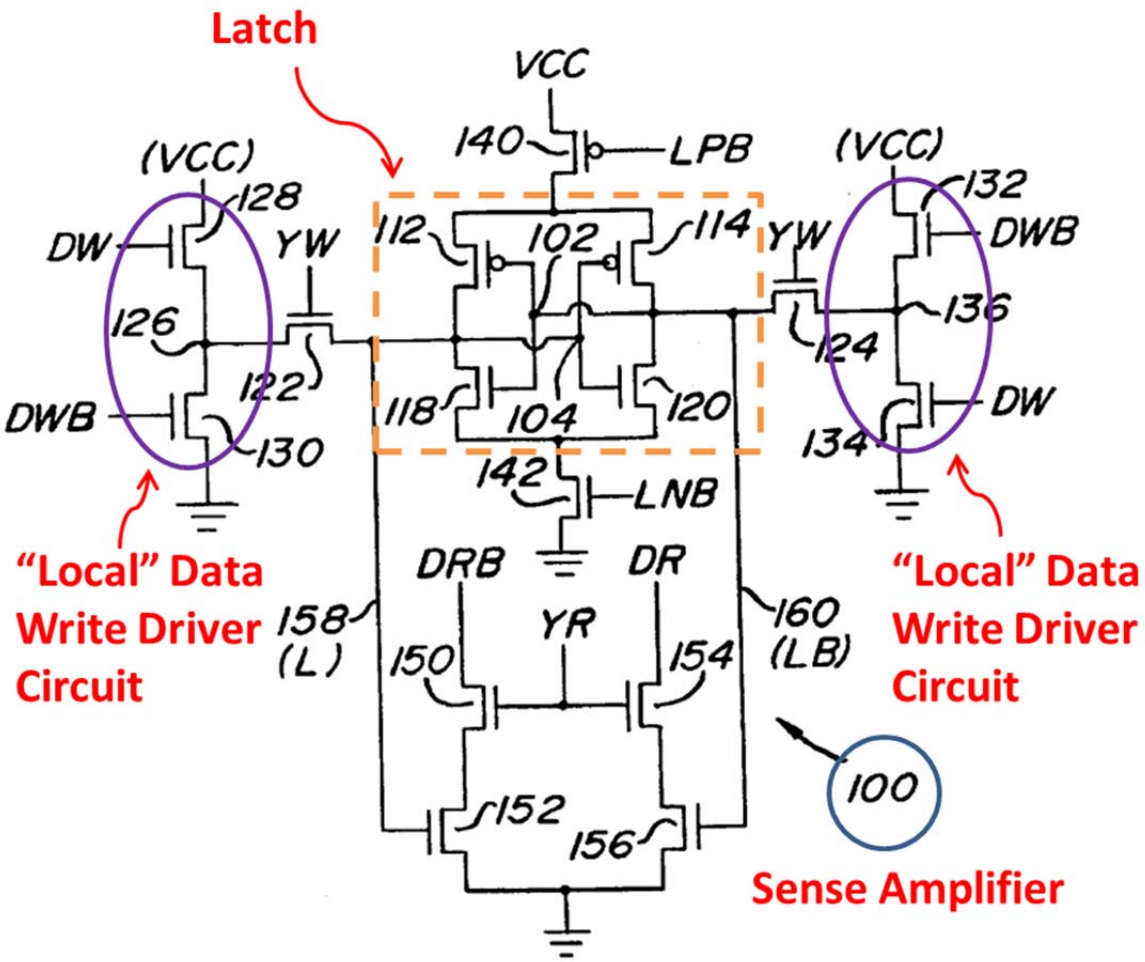


FIG. 5

(Ex.1002, ¶46, citing Ex.1001, FIG. 5 (annotated).)

The '574 patent also defines the term "global" as "connected to **several** sense amps," which suggests that "local" should denote an association with only **one** sense amplifier (and thereby, a single latch circuit). (Ex.1001, 11:25-31 (emphasis added); Ex.1002, ¶47.)

Because each sense amplifier includes a latch circuit (Ex.1001., 1:46-62, FIGS. 1, 2) and each independent claim recites "a latch circuit," Petitioner's

proposed construction includes the phrase "only one latch circuit" rather than "only one sense amplifier" for consistency with the claim language.

The patentee unequivocally confirmed this interpretation of "local" data write driver circuits during the prosecution history of a related patent to the '574 patent. (Ex.1006, 274 ("the pair of data write circuits in the present application is associated with only one latch circuit and is clearly local to that one latch circuit").) The prosecution history of the parent '312 application is also consistent with Petitioner's proposed construction. There, the patentee clarified the difference between "local" and "global" and explained that a transistor is "local" when it is associated with only **one** sense amplifier. (Ex.1005, 166-68.) Thus, the prosecution history shows a clear and intentional disavowal of claim scope regarding a data write driver circuit that is associated with more than one latch circuit.[5] [6] *See Abbott Laboratories v. Sandoz, Inc.*, 566 F.3d 1282, 1290 (Fed. Cir.

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[5] Patent Owner may argue against Petitioner's construction because in an *ex parte* appeal of the '183 application, the Board stated that "local" means something that has "a definite spatial form or location." (Ex.1006, 299 (Decision on Appeal dated Nov. 30, 1999 at 7).) But the Board found in IPR2017-00036 that Petitioner's construction, which is under *Phillips*, is "not inconsistent with the Board's prior

2009) (en banc).

B. "local column read amplifier"

For purposes of this proceeding, the phrase "local column read amplifier," which appears in each independent claim (claims 1, 4, and 30), should be construed as "a column read amplifier that is associated with only one latch circuit." The intrinsic record supports Petitioner's construction. (Ex.1002, ¶¶48-51.)

The plain language of the claims supports Petitioner's construction. (Ex.1002, ¶49.) For instance, claim 1 recites that each local column read amplifier is "responsively coupled to said internal nodes of **said** latch circuit of a corresponding sense amplifier." (Ex.1001, 13:22-24 (claim 1) (emphasis added).) Similarly, claim 4 recites that "a local column read amplifier responsively coupled

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construction, which was made under a broadest reasonable interpretation standard." IPR2017-00036, Paper No. 6 at 8.

[6] Further, while the specification discloses that the local data write driver transistors 128-134 can be shared with other column circuits (Ex.1001, 7:55-57), the patentee's unequivocal characterization of "local" data write driver circuit during prosecution confirms the above proposed interpretation and is consistent with the specification's description of "global."

to the sense amplifier" having a "sense amplifier latch circuit." (*Id.*, 13:46-58.) Claim 30 also recites that "a sense amplifier latch circuit having first and second latch nodes" to which "a local column read amplifier" is coupled. (*Id.*, 15:52-16:1.)

Additionally, throughout the specification, a local column read amplifier is described as being connected to, or associated with, a single latch circuit. (Ex. 1002, ¶50.) For instance, figure 5 of the '574 patent "includes a local column read amplifier which includes four N channel transistors 150, 152, 154, and 156" connected to a single latch circuit (transistors 112, 114, 118, 120). (Ex. 1001, 6:66-7:1; *see also id.*, FIG. 5 (annotated below); *id.* at 4:64-65, 5:29-36.)

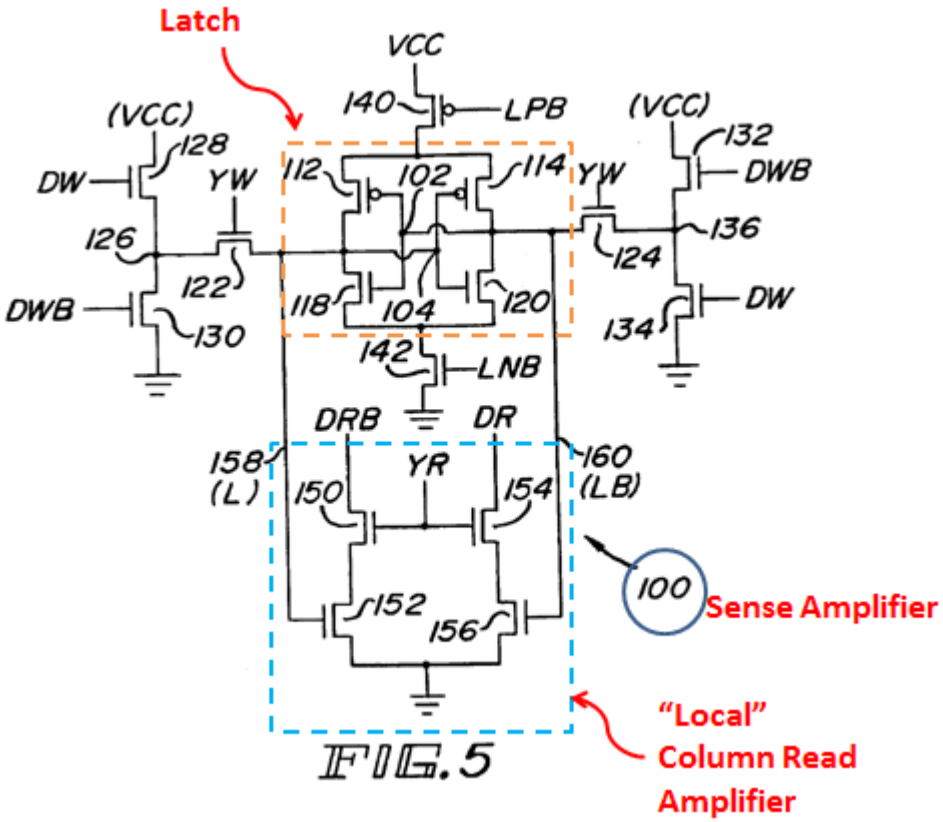


FIG. 5

(Ex.1002, ¶50, citing Ex.1001, FIG. 5 (annotated).)

Furthermore, as discussed above regarding the claim term "local data write driver circuit," the definition of "global" in the '574 patent suggests that "local" should denote an association with only one sense amplifier, and that argument also applies to support Petitioner's proposed construction of "local column read amplifier." (*Supra* Section VIII.A; Ex.1002, ¶¶47, 51.) Because each sense amplifier includes a latch circuit (Ex.1001., 1:46-62, FIGS. 1, 2) and each independent claim recites "a latch circuit," Petitioner's proposed construction includes the phrase "only one latch circuit" rather than "only one sense amplifier" for consistency with the claim language.

C. "local sense amplifier drive transistor(s)"

For purposes of this proceeding, the phrase "local sense amplifier drive transistor(s)," which appears in independent claim 1, should be construed as "sense amplifier drive transistor(s) associated with only one latch circuit." (Ex. 1002, ¶¶52-56.)

The intrinsic record supports Petitioner's construction. (*Id.*, ¶¶53-54.) For instance, according to the plain language of claim 1, "each sense amplifier is connected to a first said local sense amplifier drive transistor having a source-drain path coupled to said P channel transistors of **the** latch circuit [of said sense amplifier]," and "each sense amplifier is connected to a second said local sense

amplifier drive transistor having a source-drain path coupled to said N channel transistors of **said** latch circuit." (Ex.1001, 12:66—13:8 (emphases added).) Thus, according to the plain language of claim 1, the first and second "said local sense amplifier drive transistor[s]" are each associated with only one latch circuit.

Additionally, in the specification, local sense amplifier drive transistors 140 and 142 are described as being connected to, or associated with, a single latch circuit. For instance, the specification discloses that "[t]he source electrodes of P channel transistors 112 and 114 within amplifier 100," which are part of the latch circuit shown in figure 5, are coupled to local sense amplifier drive transistor 140, and that "the source electrodes of the N channel transistors 118 and 120 within amplifier 100," which are also part of the latch circuit of figure 5, are coupled to local sense amplifier drive transistor 142. (*Id.*, 6:53-55, 6:59-63; *see also id.*, 7:16-18, 7:35-41, FIG. 5 (annotated below).)

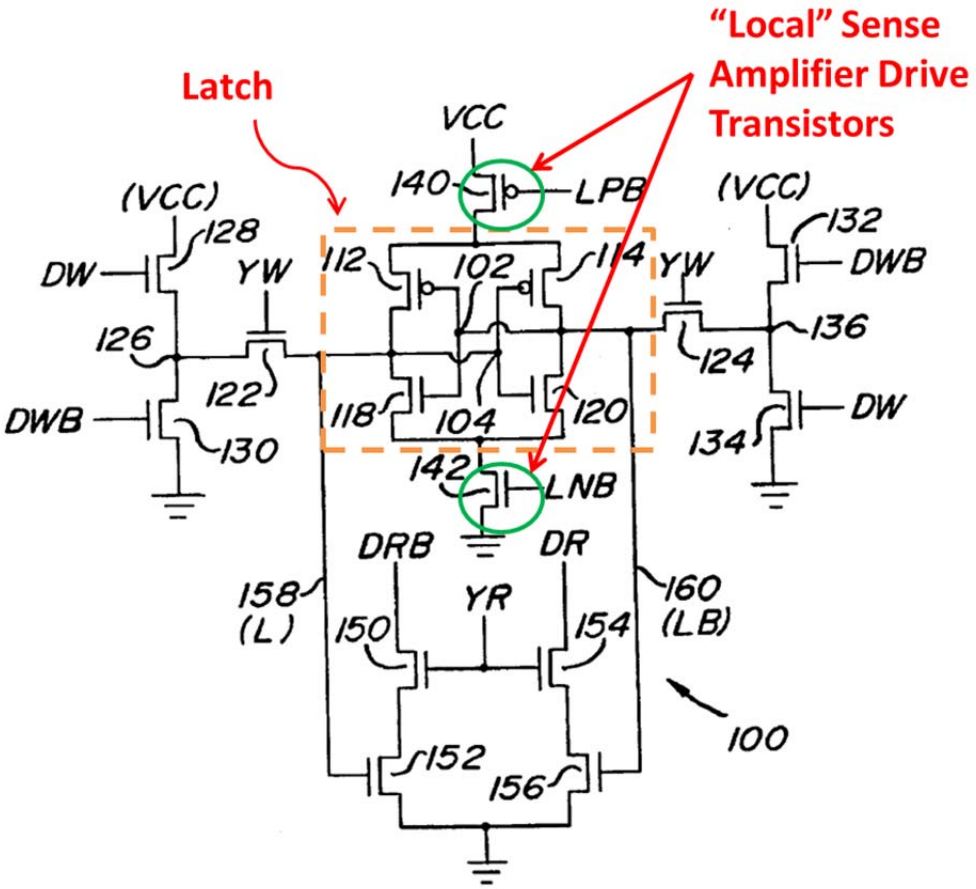


FIG. 5

(Ex.1002, ¶54, citing Ex.1001, FIG. 5 (annotated).)

Local sense amplifier drive transistors 140 and 142 cause "each sense amplifier [to be] decoupled from other sense amplifiers," so that "[e]ach sense amplifier 100 is isolated from the others." (Ex.1001, 7:35-40, 8:41.) Therefore, each local sense amplifier drive transistor is necessarily associated with only one latch circuit. (Ex.1002, ¶55.)

Furthermore, as discussed above regarding the claim term "local data write driver circuit," the definition of "global" in the '574 patent suggests that "local"

should denote an association with only one sense amplifier, and that argument also applies to support Petitioner's proposed construction of "local sense amplifier drive transistor(s)." (*Supra* Section VIII.A; Ex.1002, ¶¶47, 56.)

Because each sense amplifier includes a latch circuit (Ex.1001, 1:46-62, FIGS. 1, 2) and each independent claim recites "a latch circuit," Petitioner's proposed construction includes the phrase "only one latch circuit" rather than "only one sense amplifier" for consistency with the claim language.

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: *Inoue, Min and Hamade* Render Obvious Claims 1-3 and 30-37

Ground 1 in this petition focuses on the disclosure of figure 6 in *Inoue*. The disclosure of the circuit relating to figure 6 builds on the circuits disclosed in connection with figures 1, 3, and 4 of *Inoue*. (Ex.1002, ¶¶66-67.) For instance, when describing figure 6, *Inoue* does not repeat details previously discussed for common aspects between figures 1, 3, 4, and 6. (*Id*.) Below, at Sections IX.A.1-11, Petitioner refers to the common aspects of figures 1, 3, 4, and 6 when describing aspects of figure 6. (*Supra* Section VII.B.)

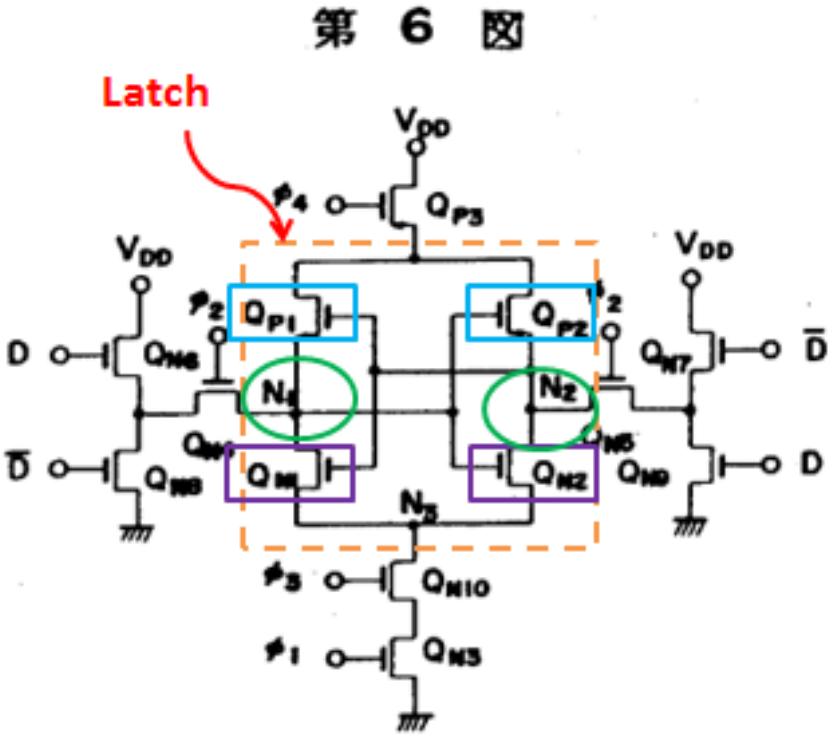
1. Claim 1

a) "In an integrated circuit memory having a plurality of bit line pairs,"

To the extent the preamble is limiting, *Inoue* in combination with *Min* discloses or suggests this feature. (Ex. 1002, ¶¶68-78.) For example, *Inoue*

discloses "a semiconductor device" in a "dynamic memory." (Ex.1007, 3-4; *see also id.*, 1 ("a semiconductor device comprising a sense amp with a flip-flop circuit").) A POSITA would have understood that "dynamic memory" in *Inoue* refers to a dynamic random access memory (DRAM), which is an integrated circuit memory. (Ex.1002, ¶68.)

Inoue discloses an embodiment shown in figure 6 that "shows a CMOS F/F," where the "F/F" (or latch) includes a pair of internal nodes "N_1 and N_2 corresponding to bit lines." (Ex.1007, 4, FIG. 6; Ex.1002, ¶69; *see also infra* Section IX.A.1(f).) A POSITA would have understood from *Inoue*'s disclosure that the "bit lines" described in *Inoue* are not shown in figure 6 but are connected to nodes N_1 and N_2. (Ex.1002, ¶69; Ex.1007, 4, FIG. 6.) Figure 6 further discloses transistors Q_{P3} and Q_{N10} that selectively connect the flip-flop (latch circuit) comprising P-channel transistors Q_{P1}, Q_{P2}, and N-channel transistors Q_{N1}, Q_{N2} to VDD and ground. (*Infra* Sections IX.A.1(f)-(h).) *Inoue* discloses that clock ϕ_4 and clock ϕ_3 control the turning ON/OFF of transistors Q_{P3} and Q_{N10}, respectively. (*Infra* Sections IX.A.1(i)-(j).)

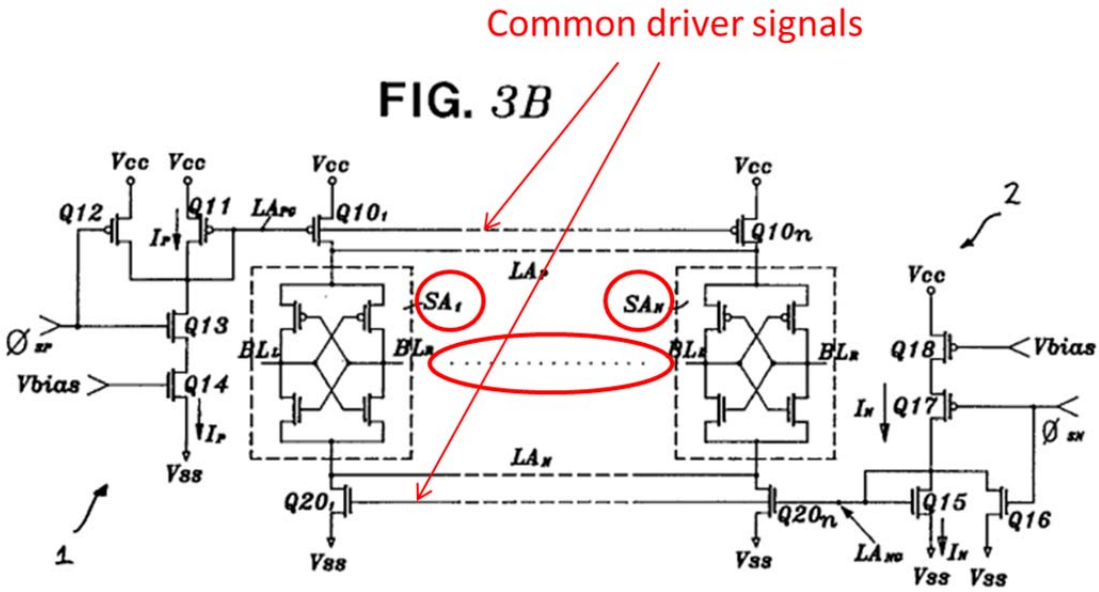


(Ex. 1002, ¶69, citing Ex. 1007, FIG. 6 (annotated to show flip-flop ("latch circuit") in orange, internal nodes N_1 and N_2 in green, PMOS transistors Q_{P1} and Q_{P2} in blue, and NMOS transistors Q_{N1} and Q_{N2} in purple).)

Based on *Inoue*'s disclosure that the embodiment of figure 6 "is applied to a sense amp in the dynamic memory" and that there are multiple "sense amps in the memory" (Ex.1007, 4), a POSITA would have understood that the flip-flop of figure 6 is part of one sense amplifier and that other sense amplifiers are also present in *Inoue*'s dynamic memory. (Ex.1002, ¶70.) Therefore, a POSITA would have understood that *Inoue* discloses a "plurality of bit line pairs" because the bit line pair represented by nodes N_1 and N_2 would be replicated given that *Inoue*

discloses multiple "sense amps in the memory." (*Id.*) While *Inoue* does not expressly show the multiple sense amplifiers in any figure, nor does *Inoue* expressly show a figure with a plurality of bit line pairs corresponding to such sense amplifiers, *Min* provides such disclosure. (*Id.*) In view of *Min*, it would have been obvious to a POSITA to implement *Inoue*'s figure 6 circuit in a multi-column memory system to create a dynamic memory having a plurality of bit line pairs, each of which is coupled to a respective sense amplifier. (*Id.*)

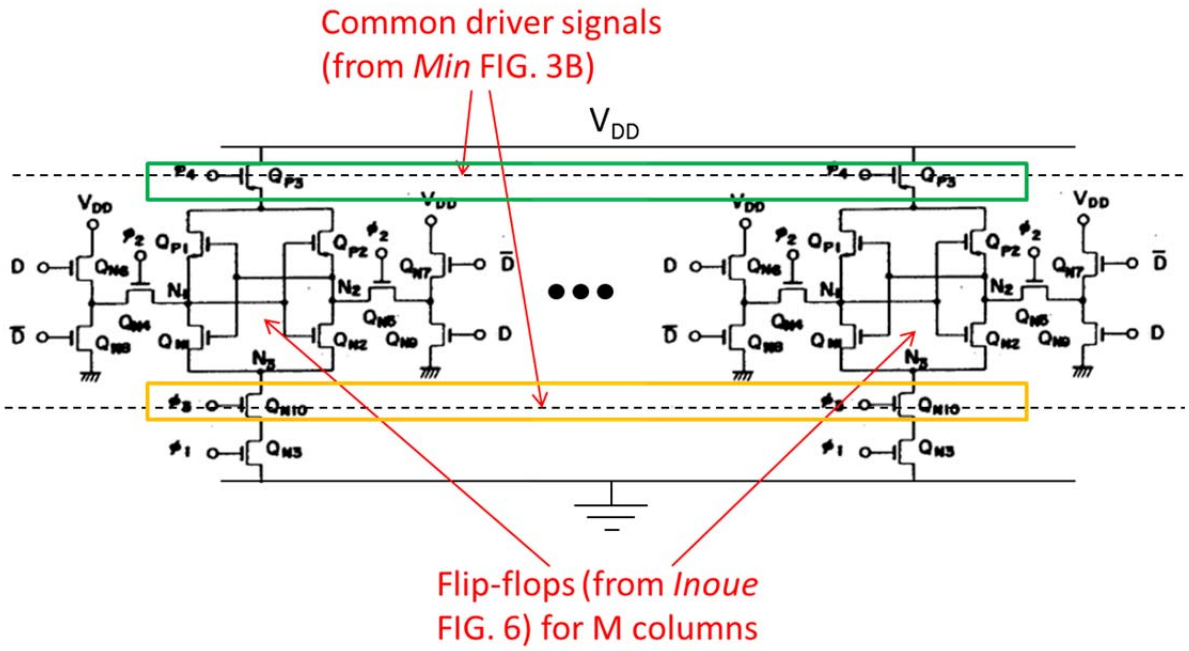
Min, which like *Inoue* is in the field of semiconductor memory, discloses a semiconductor memory device having a plurality of sense amplifiers SA_1-SA_N. (*Id.*, ¶71; Ex.1008, 1:4-8, 21:1-13, FIG. 3B.) Each sense amplifier SA_i (where i is an integer between 1 and N) in figure 3B of *Min* is coupled to a corresponding bit line pair (BL_L and BL_R) and is coupled to a positive power supply (Vcc) and to ground (Vss) via driving transistors $Q10_i$ and $Q20_i$, respectively. (Ex.1008, 2:5-15, 21:1-13, FIG. 3B.) *Min* teaches the use of a common driver signal for driving PMOS transistors $Q10_i$ of respective columns and another common driver signal for driving NMOS transistors $Q20_i$ of respective columns. (*Id.*, FIG. 3B; Ex.1002, ¶71.)



(Ex.1002, ¶71, citing Ex.1008, FIG. 3B (annotated to show plurality of sense amplifiers and common driver signals).)

A POSITA would have looked to *Min* for guidance regarding implementing the circuit of figure 6 of *Inoue* in a practical DRAM having multiple bit line pairs, particularly because *Min* and *Inoue* are references in the same field. (Ex.1002, ¶72.) Having looked to *Min*, such a person would have been motivated to replicate *Inoue*'s circuitry of figure 6 based on *Min* to implement a multi-column DRAM. (*Id.*) In such a multi-column DRAM, the circuit of figure 6 of *Inoue* would have been present for each of a plurality of columns, and the driver transistors (e.g., exemplified below as Q_{P3} (annotated in green) and Q_{N10} (annotated in orange)) of respective columns would have been driven by respective common driver signals.

(*Id.*)[7] Specifically, a common clock ϕ_4 signal would have been provided to each of transistors Q_{P3} and a common clock ϕ_3 signal would have been provided to each of transistors Q_{N10}. (*Id.*) Below is a non-limiting example showing a generalized illustration of a modified circuit.



(Ex.1002, ¶72, citing Ex.1007, FIG. 6; Ex. 1008, FIG. 3B (annotated).)

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[7] A POSITA would have been motivated to replicate the entire circuit of figure 6 instead of replicating just the latch portion (i.e., Q_{P1} and Q_{P2} and NMOS transistors Q_{N1} and Q_{N2}). (Ex.1002, ¶75.) A POSITA would have also known the benefit of not coupling together the drains of transistors Q_{P3} and Q_{N10} across multiple columns. (*Id.*, ¶76.)

A POSITA would have been motivated to combine the teachings of *Inoue* and *Min* as described above to implement a multi-column DRAM, which was a known benefit because practical DRAMs had multiple columns.[8] (*Id.*, ¶¶34-37, 73.) Moreover, a POSITA would have found it beneficial to use common driver signals for the driver transistors (e.g., exemplified above as Q_{P3} (annotated in green) and Q_{N10} (annotated in orange)) of respective columns because using the same clock signals ϕ_4 and ϕ_3 to drive transistors Q_{P3} and Q_{N10} would have resulted in a reduction of circuitry (and therefore, use of the chip area) as opposed to a case in which different clock signals were provided for transistors Q_{P3} and Q_{N10} of each latch circuit. (*Id.*, ¶77.)

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[8] A POSITA would have known at the time of the alleged invention that a practical DRAM device typically had multiple bit line pairs where each bit line pair corresponds to a column. (Ex.1002, ¶73.) The '574 patent also acknowledges this point. For instance, the '574 patent states in its background section that "[a] column is . . . ordinarily [associated with] . . . a collection of memory cells along (coupled to) a bit line or a bit line pair" and that "[i]n any large memory, such as a 16 megabit DRAM, there will be thousands of columns . . . ." (Ex.1001, 1:35-41, 2:15-16; Ex.1002, ¶73.)

Such a modification of *Inoue*'s disclosed apparatus would have been straightforward for a POSITA to implement because *Inoue* discloses an approach (e.g., regarding figure 6) in the context of a single bit line pair corresponding to a sense amplifier, and *Min* discloses a plurality of sense amplifiers coupled to respective bit line pairs. (Ex.1007, 3, FIG. 6; Ex.1008, FIG. 3B; Ex.1002, ¶74.) Moreover, the sense amplifier in figure 6 of *Inoue* includes a flip-flop with internal nodes N_1, N_2 coupled to a bit line pair, and *Min* likewise discloses that each sense amplifier SA_i[9] is coupled to a bit line pair. (Ex.1007, FIG. 6; Ex.1008, FIG. 3B; Ex.1002, ¶74.) *Min* also teaches the use of a common driver signal for driving PMOS transistors $Q10_i$ of respective columns and another common driver signal for driving NMOS transistors $Q20_i$ of respective columns that are similar to transistors Q_{P3} and Q_{N10} in *Inoue* in that they couple the sense amplifier circuits to VDD and ground. (Ex.1008, FIG. 3; Ex. 1007, FIG. 6; Ex.1002, ¶74.) A POSITA would have thus had reason and the capability to modify *Inoue* based on *Min* as noted above. (Ex.1002, ¶74.) A POSITA would have known how to modify *Inoue*'s circuit in ways that would ensure operation of the memory. (*Id.*)

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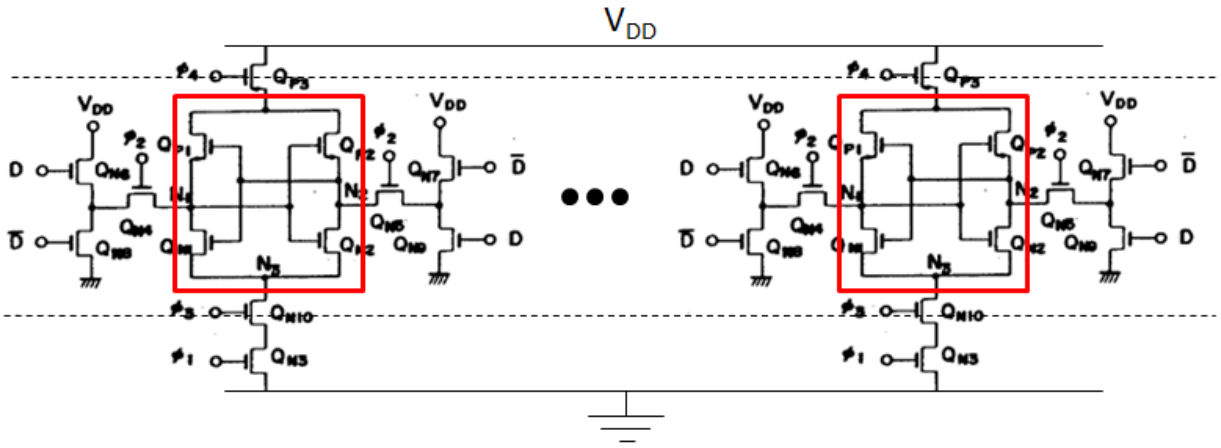
[9] *Min*'s sense amplifier SA_i has the same circuit configuration as the flip-flop in figure 6 of *Inoue*, i.e., the latch constituted by PMOS transistors Q_{P1} and Q_{P2} and NMOS transistors Q_{N1} and Q_{N2}. (Ex.1002, ¶73, n.7.)

Extending the teachings of *Inoue* to a context with a plurality of bit line pairs would not have negatively impacted the disclosed apparatus of *Inoue*, would have been a predictable combination of known components according to known methods (e.g., replication of *Inoue*'s approach of figure 6 across multiple columns as taught by *Min* at figure 3B), and would have been consistent with the known features of working DRAMs that included multiple columns and multiple pairs of bit lines. (Ex.1002, ¶78.) *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 ("*KSR*") ("The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.").

b) "a combination comprising a plurality of sense amplifiers;"

The combined *Inoue-Min* system discloses or suggests this feature. (Ex.1002, ¶¶79-80.) For instance, as discussed above at limitation 1(a) and shown below using the exemplary figure discussed above, the combined *Inoue-Min* system discloses a combination comprising a plurality of sense amplifiers ("plurality of sense amplifiers"). (*Supra* Section IX.A.1(a); Ex.1002, ¶79.)

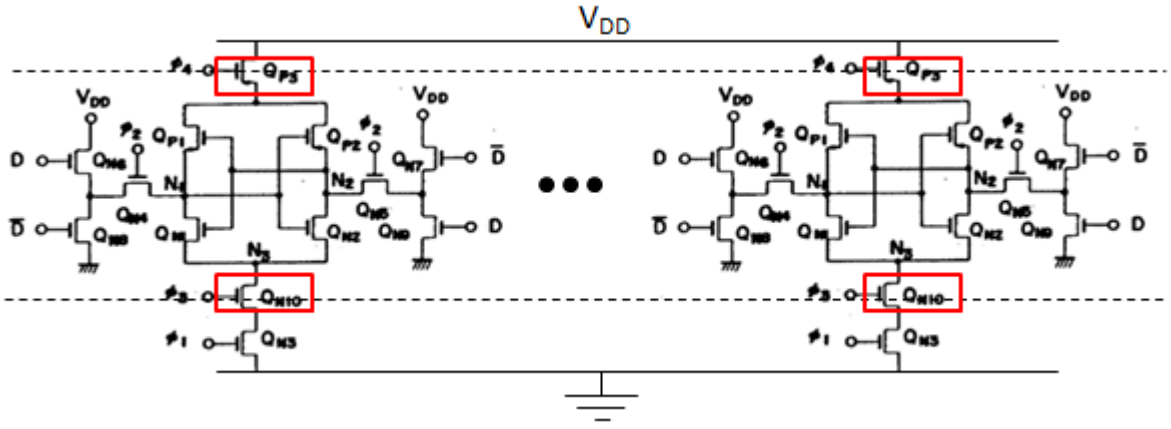


(Ex.1002, ¶79, citing Ex.1007, FIG. 6; Ex.1008, FIG. 3B (annotated).)

For reasons similar to those discussed above for limitation 1(a), it would have been obvious to replicate the circuit of figure 6 in *Inoue* based on *Min*. (Ex.1002, ¶80.) Moreover, the circuit of figure 6 in *Inoue* includes "a sense amplifier" (annotated in red above), which is the latch constituted by PMOS transistors Q_{P1} and Q_{P2} and NMOS transistors Q_{N1} and Q_{N2}. (*Id.*, ¶80; *see also infra* Section IX.A.1(f).)

c) "[the combination comprising] a plurality of local sense amplifier drive transistors;"

The combined *Inoue-Min* system discloses this feature. (Ex.1002, ¶81.) For example, the combined *Inoue-Min* system discussed above for limitation 1(a) discloses a combination comprising a plurality of local sense amplifier drive transistors Q_{P3}/Q_{N10} ("plurality of local sense amplifier drive transistors"), as shown below. (*Id.*)



(*Id.*, ¶81, citing Ex.1007, FIG. 6; Ex.1008, FIG. 3B (transistors Q_{P3}/Q_{N10} ("local sense amplifier drive transistors") annotated in red).)

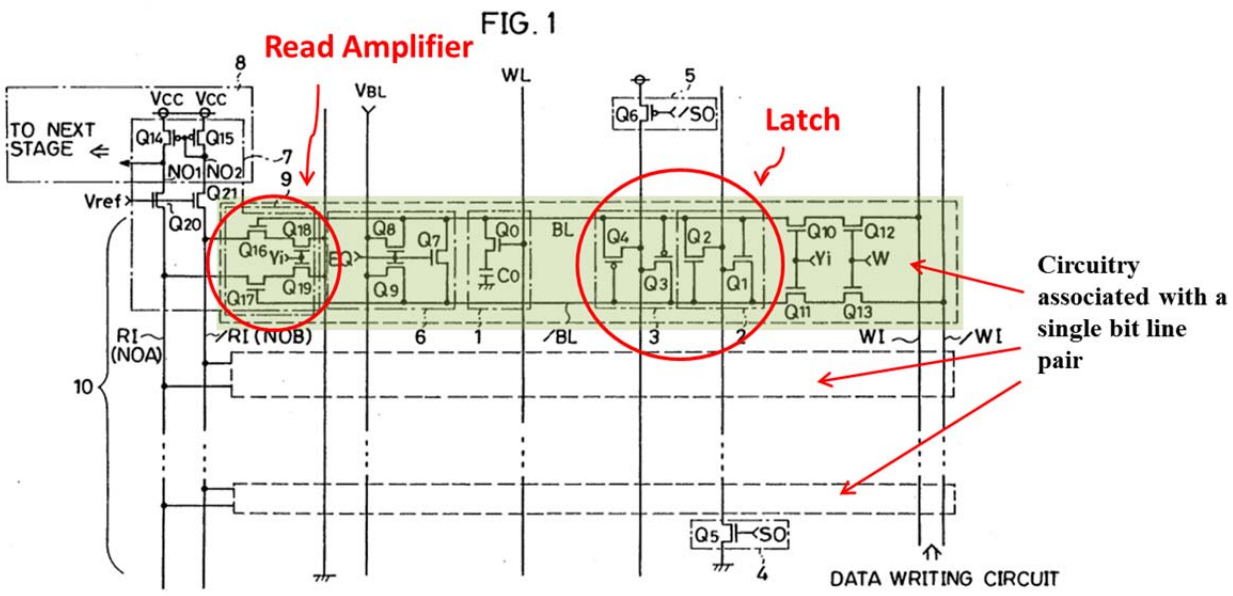
In the combined *Inoue-Min* system, each column has its own driving transistors Q_{P3} and Q_{N10} as shown above, and these transistors in respective columns constitute "a plurality of local sense amplifier drive transistors." (Ex.1002, ¶81; *see also infra* Sections IX.A.1(g),(h) (explaining that each of Q_{P3} and Q_{N10} is a "local sense amplifier drive transistor").)

d) **"**[the combination comprising] a plurality of local column read amplifiers; and"

The combined *Inoue-Min* system does not expressly disclose "a plurality of local column read amplifiers." However, it would have been obvious in view of *Hamade* to modify the combined *Inoue-Min* system to implement a combination comprising a plurality of read amplifiers at respective columns of the memory, with each column read amplifier being associated with only one latch circuit

("plurality of local column read amplifiers"). (Ex.1002, ¶82; *see also* Section VIII.B.)

Hamade, which is in the same field (semiconductor memory) as *Inoue* and *Min*, discloses circuitry for "implementing a high speed operation of semiconductor memory devices." (Ex.1009, 1:17-19; Ex.1002, ¶83; *supra* Section VII.D.) Figure 1 of *Hamade* discloses a "main part of a semiconductor memory device." (Ex.1009, 7:10-12.) The broken line in figure 1 of *Hamade* illustrates a "pair of bit lines BL and /BL" and circuitry associated with each bit line pair BL and /BL. (*Id.*, 3:1-5, 7:4-12, FIG. 1.)



(Ex.1002, ¶83, citing Ex.1009, FIG. 1 (annotated).)

The circuitry associated with each bit line pair in figure 1 includes an n-type sense amplifier 2 and a p-type sense amplifier 3. (Ex.1009, FIG. 1, 7:4-9, 1:47-

52.) A POSITA would have understood that the sense amplifiers 2 and 3 collectively form a latch circuit like in *Inoue* figure 6. (Ex.1002, ¶¶26-33, 84.) Moreover, *Hamade* discloses that "a drive circuit 9 [] is provided for each bit line pair." (Ex.1009, 7:14-18, FIG. 1.) As explained immediately below, a POSITA would have also understood that the drive circuit 9 (consisting of transistors Q16-Q19, *see id*., FIG. 1) constitutes a "column read amplifier." Because *Hamade* discloses a plurality of bit line pairs, and each bit line pair includes a drive circuit 9 associated with a single latch circuit (combination of sense amplifiers 2 and 3 in figure 1), *Hamade* discloses a "plurality of **local** column read amplifiers" (emphasis added). (*Id.*, FIG. 1 (annotated above), 7:4-23, 1: 47-52, 3:1-5; *supra* Section VIII.B.)

A POSITA would have understood that *Hamade*'s drive circuit 9 is a "column read amplifier" in the context of the '574 patent. (Ex.1002, ¶86.) Drive circuit 9 is part of a "read amplifier means 7" and "**amplifies** the potentials of the associated bit lines." (Ex.1009, 7:14-19 (emphasis added); Ex.1002, ¶86.) Specifically, a skilled artisan would have understood that the combination of transistors Q16-Q19 (i.e., drive circuit 9) constitutes a "read amplifier" because they operate to amplify the potentials on bit lines BL and /BL during a read operation, and allow one of read only data lines RI and /RI to be discharged to ground during a read operation. (Ex.1009, 3:61-4:10, 8:8-31, 8:52-54; Ex.1002,

¶86.) Moreover, drive circuit 9 is provided for each **column** because it is provided for each bit line pair (Ex.1009, 7:22-23), which "is related to memory cells in one **column** of the memory cell array." (*Id*., 1:36-39 (emphasis added), 7:4-9; Ex.1002, ¶87.) Indeed, the "column read amplifier" in the '574 patent is a circuit similar to drive circuit 9 because it has two transistors 152 and 156 coupled to bit lines 158 and 160, and two other transistors 150 and 154 controlled by a column read signal Y_R. (Ex.1002, ¶87; Ex.1001, 6:66—7:11.)

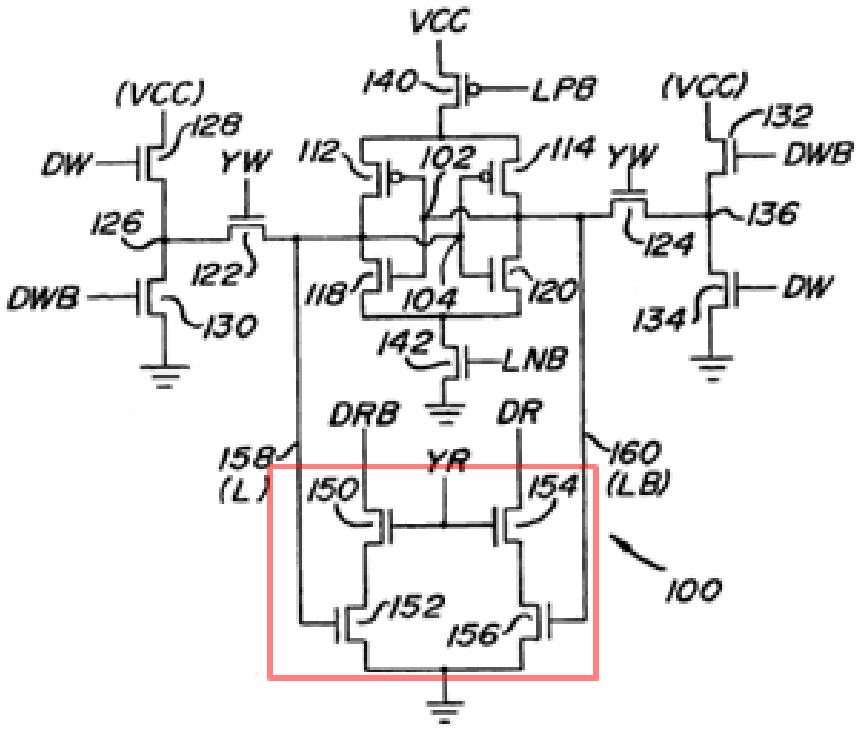
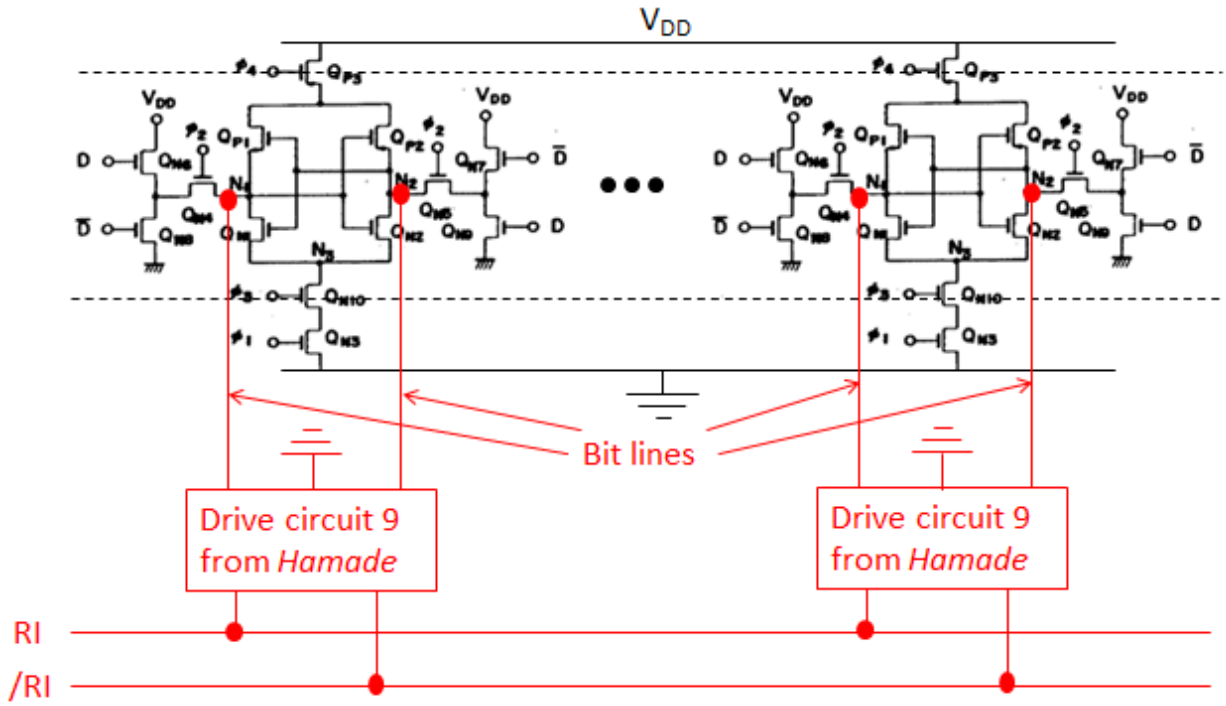


FIG. 5

(Ex.1002, ¶87, citing Ex.1001, FIG. 5 (annotated).)

A POSITA would have been motivated to modify the combined *Inoue-Min* system to implement *Hamade*'s drive circuit 9 at *each* column because *Hamade* discloses that "drive circuit 9 [ ] is provided for each bit line pair." (Ex.1009, 7:17-18; Ex.1002, ¶88.) A POSITA would have been motivated to implement read only data lines RI and /RI in the combined system in a manner similar to how they are configured in figure 1 of *Hamade* to support the functionality of the read amplifiers of respective columns. (Ex.1009, FIG. 1, 5:12-16; Ex.1002, ¶88.) As a non-limiting example, below is a demonstrative showing certain aspects of the combined *Inoue-Min-Hamade* system that a POSITA would have found to be consistent with the above modification. (Ex.1002, ¶88.) Although not shown in the below demonstrative for visual simplicity, a POSITA would have also been motivated to implement in the combined *Inoue-Min-Hamade* system other circuitry associated with *Hamade*'s figure 1 configuration (e.g., transistors Q20/Q21, Q14/Q15), to ensure proper operation of the memory in accordance with *Hamade*'s description of the figure 1 circuit. (Ex.1009, FIG. 1, 8:8—9:10; Ex.1002, ¶¶89-91.) Based on the disclosures of *Inoue*, *Min*, and *Hamade*, a POSITA would have known how to assemble and implement all the above circuitry into the combined system without undue experimentation. (Ex.1002, ¶91.)



(Ex.1002, ¶88, showing the combined *Inoue-Min-Hamade* system.)

As is apparent from the above exemplary demonstrative, the combined *Inoue-Min-Hamade* system discloses a "plurality of local column read amplifiers," because there is a read amplifier (drive circuit 9) for each column ("plurality of . . . column read amplifiers"), and each column read amplifier is associated with only one latch circuit. (*Id.*, ¶92; *supra* Section VIII.B.) Thus, the combined *Inoue-Min-Hamade* system discloses a "plurality of **local** column read amplifiers" (emphasis added). (Ex.1002, ¶92.)

A POSITA would have found it obvious to combine the teachings of *Inoue*, *Min*, and *Hamade* as discussed above. (*Id.*, ¶93.) A POSITA would have looked to *Hamade* to augment and improve the capabilities of the combined *Inoue-Min*

system, because *Hamade* is in the same field as *Inoue* and *Min* and teaches circuitry and functionality applicable to a column of a memory such as in the combined *Inoue-Min* system. (*Id.*, ¶93.) A POSITA would have recognized that the combined *Inoue-Min* system does not disclose read circuitry for reading data carried by the bit lines that would typically be found in a practical DRAM. (*Id.*) Given that *Hamade* discloses circuitry for reading data carried by the bit lines in a practical DRAM at a high rate of speed, a POSITA would have looked to *Hamade*. (*Id.*) A POSITA would have recognized that (1) *Inoue* discloses a sense amplifier implemented as a flip-flop coupled to a pair of bit lines (Ex.1007, 4 ("N_1 and N_2 correspond to bit lines"), (2) *Min* teaches a multi-column approach compatible with *Inoue* as discussed above (*supra* Section IX.A.1(a)), and (3) *Hamade* similarly discloses a latch circuit including sense amplifiers 2 and 3 coupled to a pair of bit lines BL and /BL for a given column (Ex.1009, 1:47—2:4, FIGS. 1, 7; Ex.1002, ¶93) such that the configurations of these references are similar and conducive to combination with one another as described herein. (Ex.1002, ¶93.)

As discussed above, a POSITA would have been motivated to modify the combined *Inoue-Min* system to implement circuitry from *Hamade*'s figure 1 because the combined *Inoue-Min* system does not include read circuitry for reading data carried by bit lines that would typically be found in a practical DRAM. (Ex.1002, ¶94.) Therefore, in the interest of making a practical functional DRAM

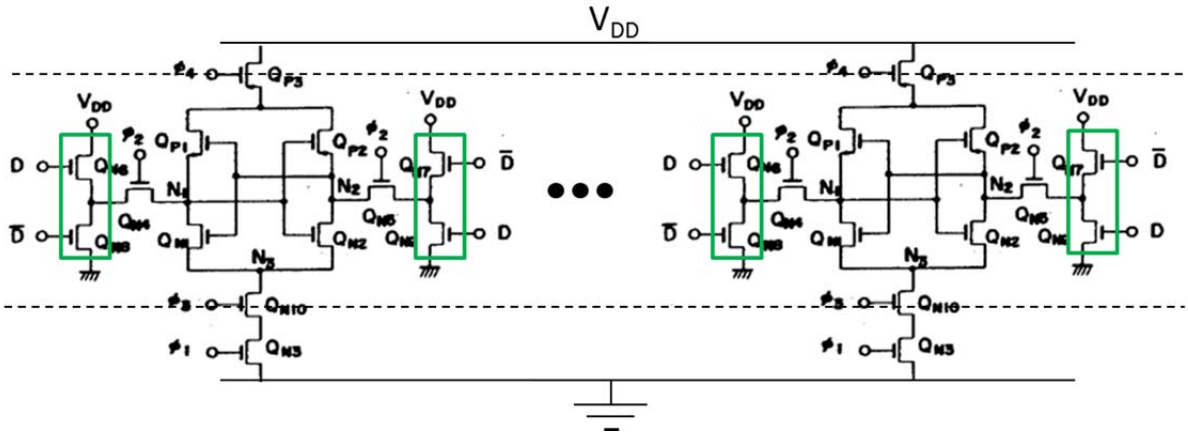
a POSITA would have found it advantageous to include in the combined *Inoue-Min* system circuitry similar to *Hamade*'s circuitry that allows for reading of the data carried by the bit lines, and hence, the combination would have been obvious. *See KSR*, 550 U.S. at 416-18. The benefit of doing so would have been allowing fast reading of the data carried by the bit lines as disclosed by *Hamade*. (Ex.1009, 1:24-30, 5:11-16, 8:37-42; Ex.1002, ¶94.)

Moreover, a POSITA would have understood that the above modification of the *Inoue-Min* system based on *Hamade* would have been merely a combination of known components (e.g., circuitry for a multi-column memory as in the combined *Inoue-Min* system, and a drive circuit 9 for a given column and related circuitry such as read only data lines RI, /RI as taught by *Hamade*) according to known methods (e.g., *Hamade* teaches how to implement the drive circuit 9 for a given column because it shows how to connect the drive circuit to a latch circuit at bit lines corresponding to that column) to yield predictable results (e.g., faster read operations as taught by *Hamade*). (Ex.1009, ¶95.) *See KSR*, 550 U.S. at 416.

e) "[the combination comprising] a plurality of local data write driver circuits;"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶96.) For example, in the *Inoue-Min-Hamade* combination (discussed above for limitation 1(d)), each column would have had a configuration as shown below (the read amplifier circuitry for each column is not shown for visual

simplicity here and throughout). (*Id.*) In the combined system, each of the circuits annotated in green is a "local data write driver circuit." (Ex.1002, ¶96; *infra*, Sections IX.A.1(n),(o).) Therefore, the combined *Inoue-Min-Hamade* system discloses across the various columns "a plurality of local data write driver circuits." (Ex.1002, ¶96.)

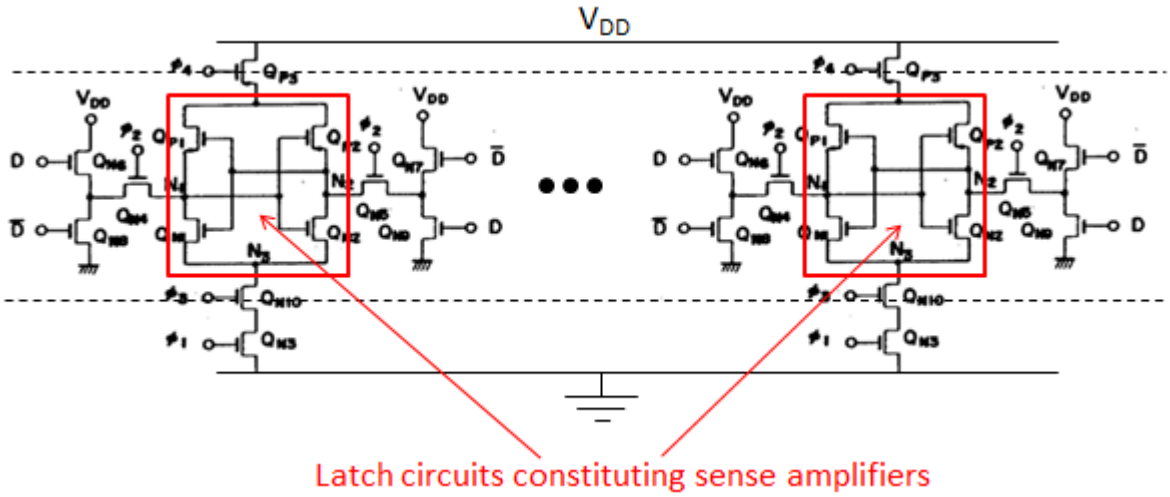


(Ex.1002, ¶96, citing Ex.1007, FIG. 6; Ex.1008, FIG. 3B (annotated).)

f) "each sense amplifier comprising a latch circuit having a pair of internal nodes coupled to a corresponding pair of bit lines, the latch circuit including a pair of P channel transistors and a pair of N channel transistors;"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶97.) In the *Inoue-Min-Hamade* combination, each column would have had a corresponding sense amplifier ("each sense amplifier") comprising a flip-flop ("latch circuit") having a pair of internal nodes N_1 and N_2 ("a pair of internal nodes") coupled to a corresponding pair of bit lines, the flip-flop including PMOS transistors Q_{P1} and Q_{P2} ("a pair of P channel transistors") and NMOS transistors

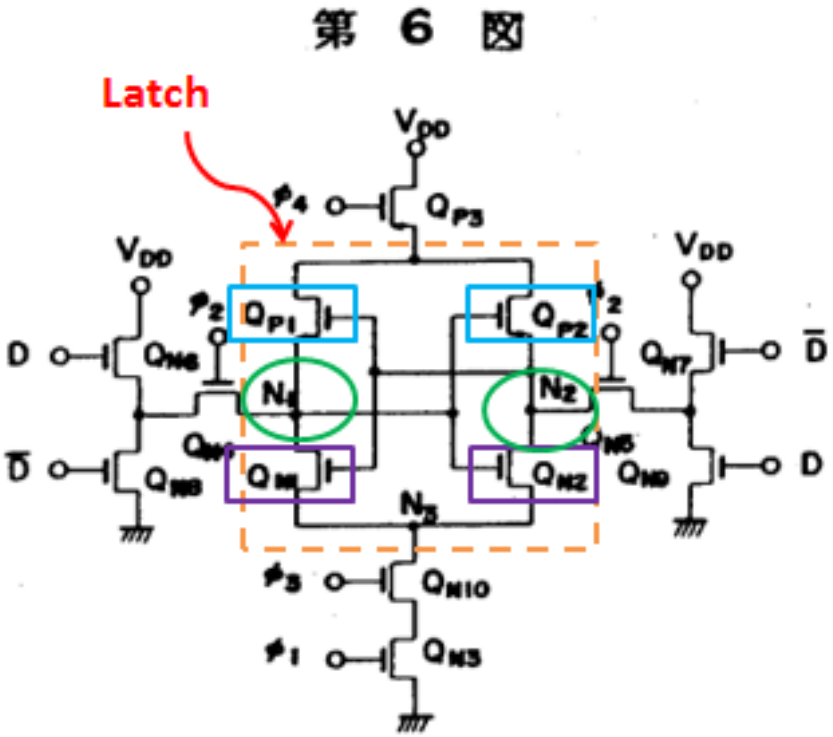
Q_{N1} and Q_{N2} ("a pair of N channel transistors"). (*Supra* Sections IX.A.1(a), (d); Ex.1007, FIG. 6; Ex.1002, ¶97.)



(Ex.1002, ¶97.)

The latch circuit of each column of the *Inoue-Min-Hamade* combination is described in *Inoue* with respect to figure 6. (Ex.1002, ¶98.) *Inoue* discloses that PMOS or P-channel transistors Q_{P1}, Q_{P2}, and NMOS or N-channel transistors Q_{N1}, Q_{N2} form a flip-flop ("latch circuit"). (Ex.1007, 3.) Additionally, *Inoue* discloses that the embodiment of figure 6 "is applied to a sense amp," which includes a "CMOS F/F" (i.e., flip-flop). (*Id.*, 4.) Moreover, a flip-flop is a "latch circuit" as acknowledged by the '574 patent and as would have been readily understood by a POSITA. (Ex.1002, ¶98; Ex.1001, 1:58-62, 2:6-14, 6:5-13, FIGS. 1, 5.) A POSITA would have understood that the "latch circuit" in *Inoue* is a "sense amplifier" because *Inoue* discloses that the embodiment of figure 6 "is applied to a

sense amp," which includes a "CMOS F/F" (i.e., flip-flop). (Ex.1007, 4; Ex.1002, ¶98.) Moreover, the '574 patent acknowledges that a "latch circuit" such as the one shown in figure 6 of *Inoue* constitutes a "sense amplifier." (Ex.1001, 1:47-57, FIG. 1.) Therefore, the combined *Inoue-Min-Hamade* combination discloses that "each sense amplifier comprising a latch circuit . . . the latch circuit including a pair of P channel transistors and a pair of N channel transistors," as claimed.



(Ex.1002, ¶98, citing Ex.1007, FIG. 6 (annotated to show flip-flop ("latch circuit") in orange, internal nodes N_1 and N_2 in green, PMOS transistors Q_{P1} and Q_{P2} in blue, and NMOS transistors Q_{N1} and Q_{N2} in purple).)

Figure 6 of *Inoue* further discloses that the flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} has nodes N_1 and N_2 and when the embodiment of figure 6 is applied to a sense amp in the memory, "**N_1 and N_2 correspond to bit lines**." (Ex.1007, 4 (emphasis added); Ex.1002, ¶99.) Therefore, the combined *Inoue-Min-Hamade* combination discloses that "each sense amplifier comprising a latch circuit having a pair of internal nodes coupled to a corresponding pair of bit lines," as claimed.

As shown below, the configuration of *Inoue*'s latch circuit in the combined system is similar to the configuration of the latch circuit disclosed by the '574 patent. (Ex.1002, ¶100.)

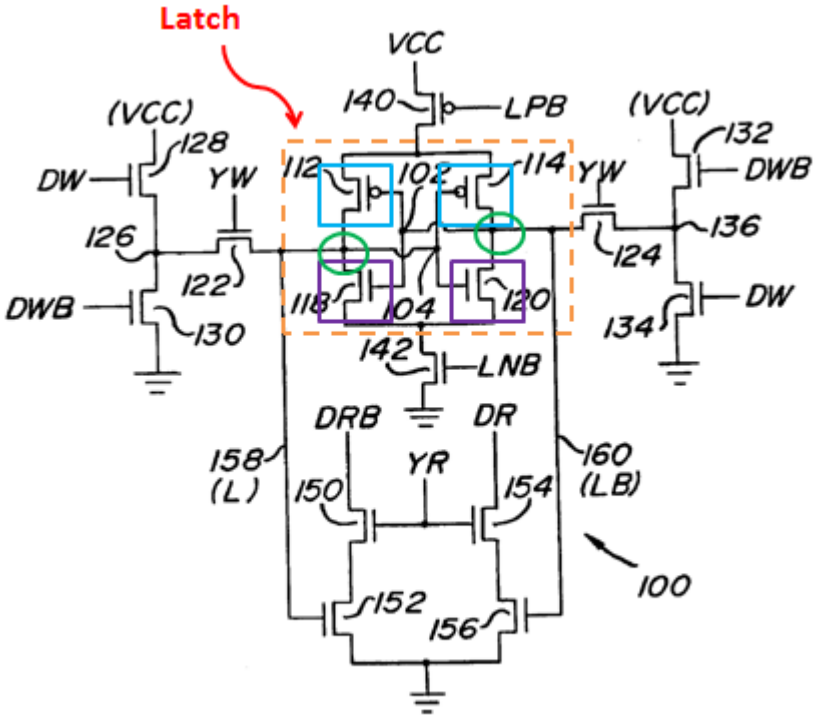


FIG. 5

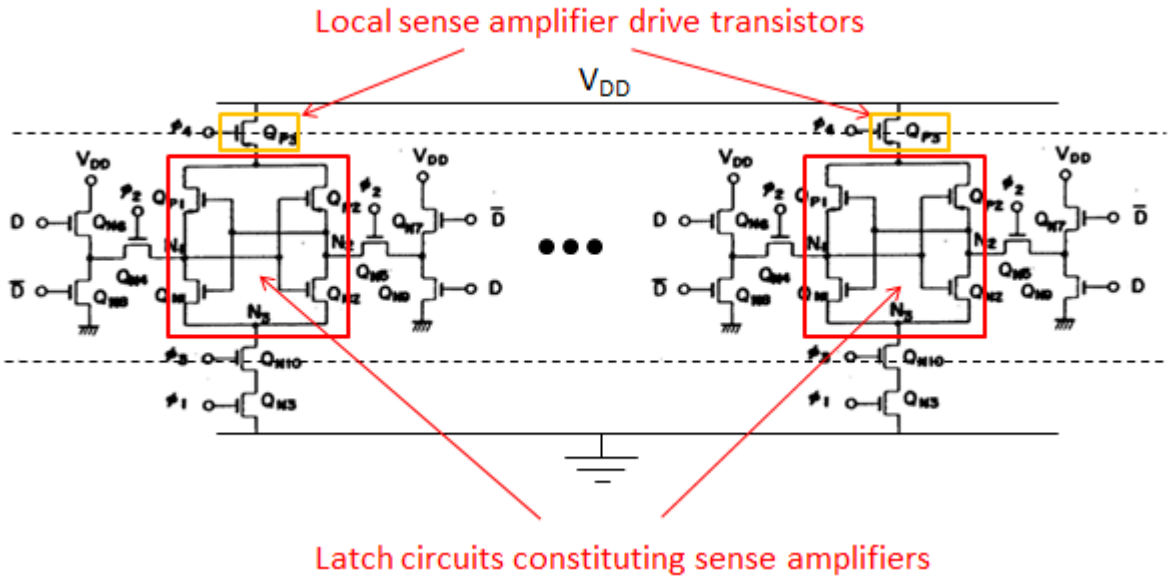
(Ex.1002, ¶100, citing Ex.1001, FIG. 5 (annotated).)

g) "wherein each sense amplifier is connected to a first said local sense amplifier drive transistor having a source-drain path coupled to said P channel transistors of the latch circuit, said first local sense amplifier drive transistor selectively coupling said P channel transistors to a first voltage source;"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶101.) In the combined *Inoue-Min-Hamade* system, each column would have had a corresponding sense amplifier ("each sense amplifier") that is connected to a corresponding transistor Q_{P3} ("a first said local sense amplifier drive transistor") having a source-drain path coupled to the transistors Q_{P1}, Q_{P2} ("said P channel transistors of the latch circuit"), transistor Q_{P3} selectively coupling the transistors Q_{P1}, Q_{P2} to V_{DD} ("a first voltage source"). (*Supra* Sections IX.A.1(a),(d); Ex.1007, FIG. 6; Ex.1002, ¶101.)

Inoue discloses that transistor Q_{P3} is a "sense amplifier drive transistor" because it controls the activation of the sense amplifier (i.e., latch circuit comprising P-channel transistors Q_{P1}, Q_{P2}, and N-channel transistors Q_{N1}, Q_{N2}). (Ex.1002, ¶102.) Specifically, *Inoue* discloses that when "Q_{P3} is rendered non-conducting . . . no current path is formed from V_{DD} to GND." (Ex.1007, 4.) Indeed, transistor Q_{P3} is no different from transistor 140 in the '574 patent, which the '574 patent refers to as a "local sense amplifier drive transistor." (Ex.1001,

FIG. 5, 6:53-59; Ex.1002, ¶102.) As is apparent from the figure below, the combined *Inoue-Min-Hamade* system discloses that each sense amplifier (which is a "latch circuit", *supra* Section IX.A.1(f)) is connected to a transistor Q_{P3}, which is provided for each latch circuit in the combined *Inoue-Min-Hamade* system. (Ex.1002, ¶102.) Therefore, transistor Q_{P3} is a "local sense amplifier drive transistor" and the combined system discloses that "each sense amplifier is connected to a first said local sense amplifier drive transistor." (*Id.*, ¶102; *supra* Section VIII.C.)

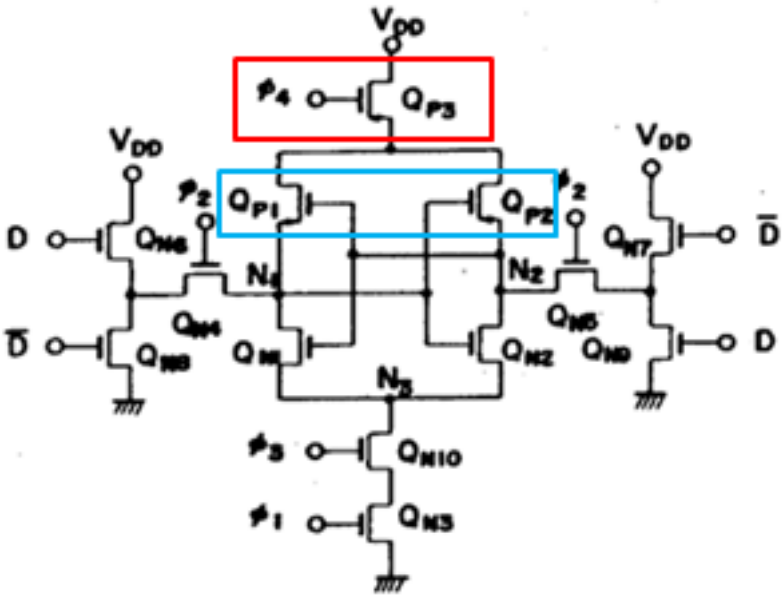


(Ex.1002, ¶102, transistor Q_{P3} in orange).)

As would have been apparent to a POSITA from figure 6 in *Inoue*, transistor Q_{P3} has a path across its source and drain ("source-drain path") coupled to transistors Q_{P1} and Q_{P2} ("said P channel transistors") because the drain of transistor

Q_{P3} is coupled to the source of transistors Q_{P1} and Q_{P2}. (Ex.1007, FIG. 6; Ex.1002, ¶103.) *Inoue* additionally discloses that transistor Q_{P3} selectively couples (based on the signal ϕ_4 applied to the gate of transistor Q_{P3}) transistors Q_{P1} and Q_{P2} to V_{DD} ("a first voltage source"). (Ex.1007, 4, FIG. 6; Ex.1002, ¶103.) Therefore, the combined system discloses "said local sense amplifier drive transistor having a source-drain path coupled to said P channel transistors of the latch circuit, said first local sense amplifier drive transistor selectively coupling said P channel transistors to a first voltage source," as claimed. (Ex.1002, ¶103.)

第 6 図



(*Id.*, ¶103, citing Ex.1007, FIG. 6 (annotated to show transistor Q_{P3} in red, and P-channel transistors Q_{P1} and Q_{P2} in blue).)

The '574 patent discloses a similar configuration, as shown below.

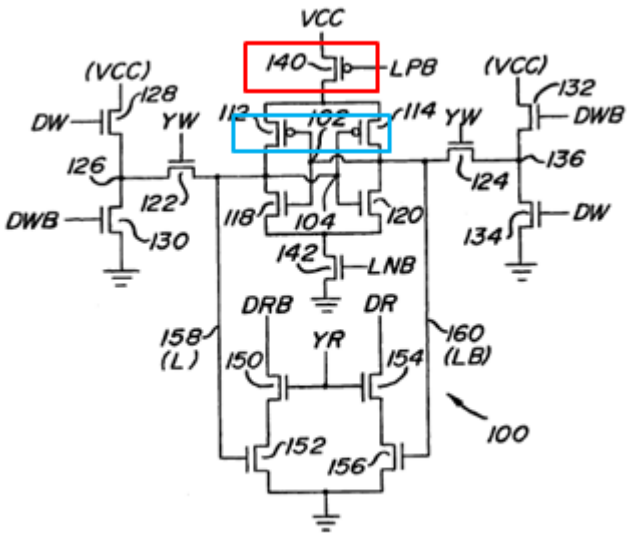


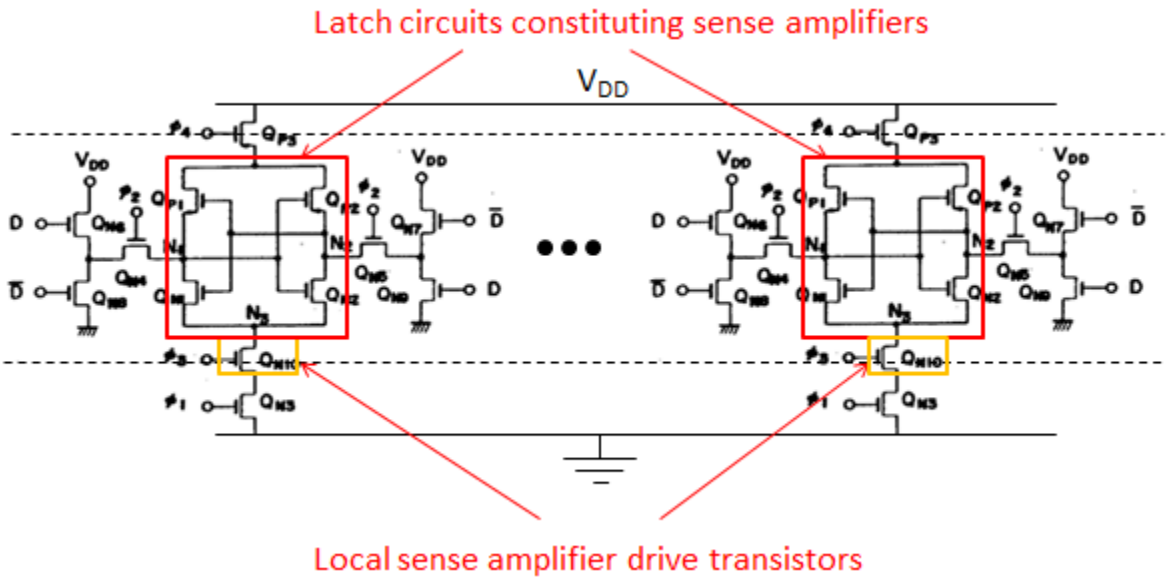
FIG. 5

(Ex.1002, ¶104, citing Ex.1001, FIG. 5 (annotated).)

h) "wherein each sense amplifier is connected to a second said local sense amplifier drive transistor having a source-drain path coupled to said N channel transistors of said latch circuit, said second local sense amplifier drive transistor selectively coupling said N channel transistors to a second voltage;"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶105.) In the combined *Inoue-Min-Hamade* system, each column would have had a corresponding sense amplifier ("each sense amplifier") that is connected to a corresponding transistor Q_{N10} ("a second said local sense amplifier drive transistor") having a source-drain path coupled to the transistors Q_{N1} and Q_{N2} ("said N channel transistors of said latch circuit"), transistor Q_{N10} selectively coupling the transistors Q_{N1}, Q_{N2} to ground ("a second voltage"). (*Supra* Sections IX.A.1(a),(d); Ex.1007, FIG. 6; Ex.1002, ¶105.)

Inoue discloses that transistor Q_{N10} is a "sense amplifier drive transistor" because it controls the activation of the sense amplifier (i.e., latch circuit comprising P-channel transistors Q_{P1}, Q_{P2}, and N-channel transistors Q_{N1}, Q_{N2}). (Ex.1002, ¶106.) Specifically, *Inoue* discloses that when "Q_{N10} is made non-conducting . . . no current path is formed from V_{DD} to GND." (Ex.1007, 4.) Indeed, transistor Q_{N10} is very similar to the "local sense amplifier drive transistor 142" in the '574 patent. (Ex.1001, FIG. 5, 6:53-59; Ex.1002, ¶106.) As is apparent from the figure below, the combined *Inoue-Min-Hamade* system discloses that each sense amplifier (which is a "latch circuit", *supra* Section IX.A.1(f)) is connected to a transistor Q_{N10}, which is provided for each latch circuit in the combined *Inoue-Min-Hamade* system. Therefore, transistor Q_{N10} is a "**local** sense amplifier drive transistor" and the combined system discloses that "each sense amplifier is connected to a second said local sense amplifier drive transistor." (Ex.1002, ¶106; *supra* Section VIII.C.)



(Ex.1002, ¶106.)

As would have been apparent to a POSITA from figure 6 in *Inoue*, transistor Q_{N10} ("said second local sense amplifier drive transistor") has a path across its source and drain ("source-drain path") coupled to transistors Q_{N1} and Q_{N2} ("said N channel transistors") because the drain of transistor Q_{N10} is coupled to the source of transistors Q_{N1} and Q_{N2}. (Ex.1007, FIG. 6; Ex.1002, ¶107.) *Inoue* additionally discloses that transistor Q_{N10} selectively couples (based on the signal ϕ_3 applied to the gate of transistor Q_{N10}) transistors Q_{N1} and Q_{N2} of that column to GND ("a second voltage"). (Ex.1007, 4, FIG. 6; Ex.1002, ¶107.) Therefore, the combined system discloses "second said local sense amplifier drive transistor having a source-drain path coupled to said N channel transistors of said latch circuit, said

second local sense amplifier drive transistor selectively coupling said N channel transistors to a second voltage," as claimed. (Ex.1002, ¶108.)

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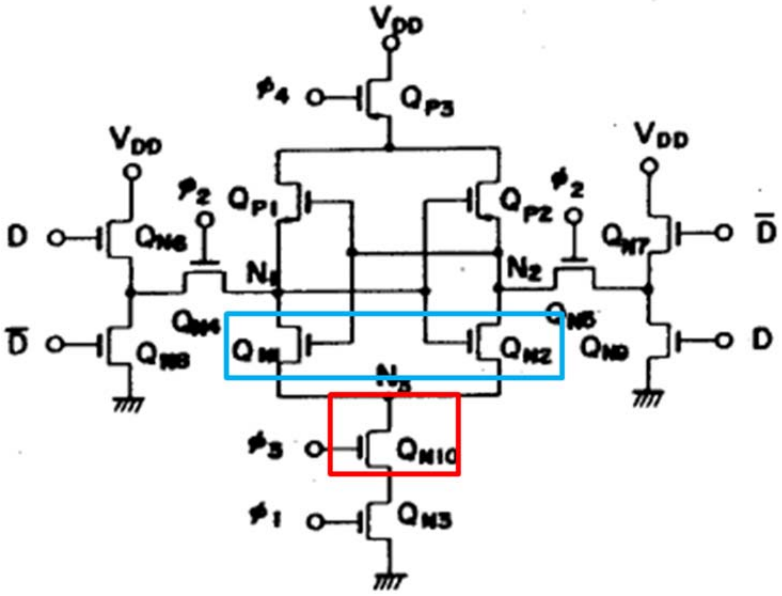


(Ex.1002, ¶108, citing Ex.1007, FIG. 6 (annotated to show transistor Q_{N10} in red, and N channel transistors Q_{N1} and Q_{N2} in blue).)

The '574 patent discloses a similar configuration, as shown below.

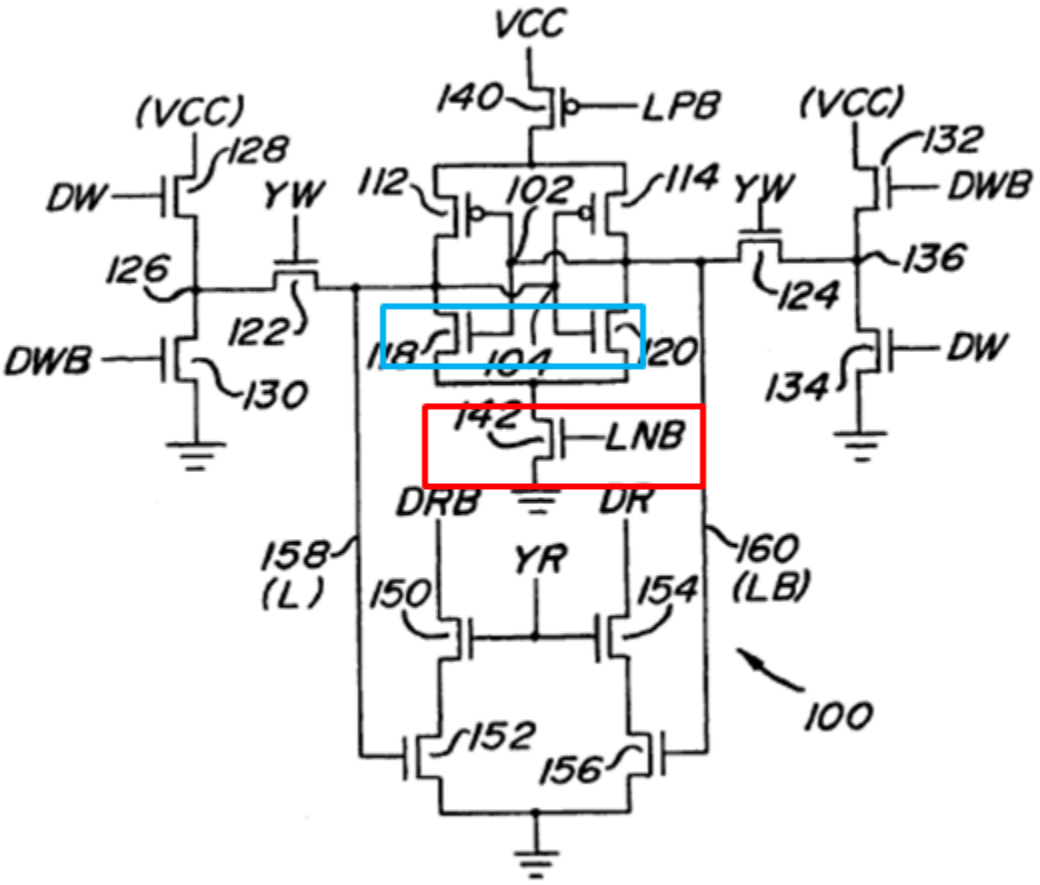


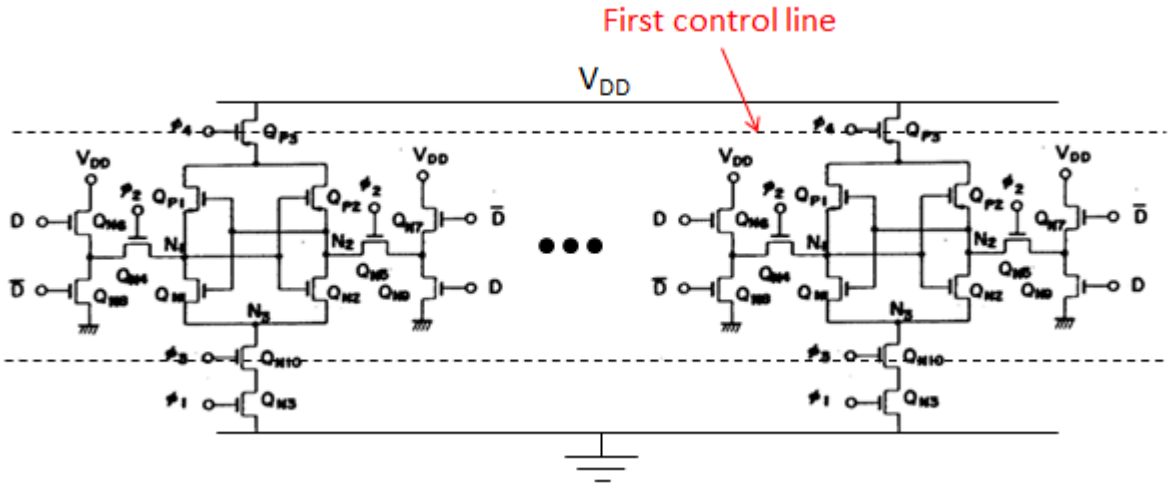
FIG. 5

(Ex.1002, ¶109, citing Ex.1001, FIG. 5 (annotated).)

i) "a first control line coupled to control the operation of a plurality of said first local sense amplifier drive transistors;"

In the combined *Inoue-Min-Hamade* system, clock ϕ_4 ("a first control line") would have been coupled to control the operation of transistor Q_{P3} in each column ("control the operation of a plurality of said first local sense amplifier drive transistors"). (*Supra* Sections IX.A.1(a),(c),(d); Ex.1002, ¶110.) Specifically,

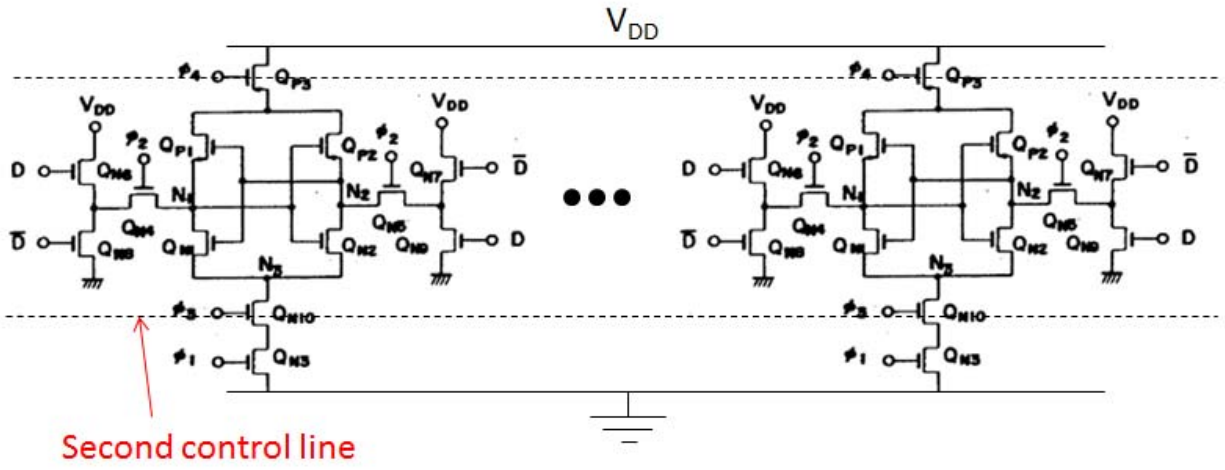
clock ϕ_4 would have controlled the turning ON/OFF for each transistor Q_{P3} because when "clock ϕ_4 is made to rise, . . . Q_{P3} is rendered non-conducting." (Ex.1007, 4.)



(Ex.1002, ¶110.)

j) "a second control line coupled to control the operation of a plurality of said second local sense amplifier drive transistors;"

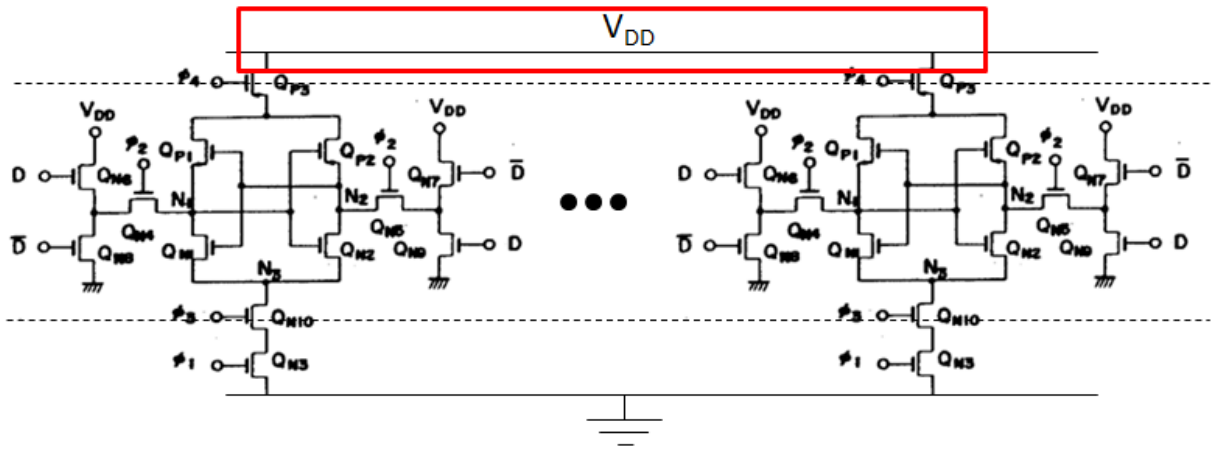
In the combined *Inoue-Min-Hamade* system, clock ϕ_3 ("a second control line") would have been coupled to control the operation of transistor Q_{N10} in each column ("control the operation of a plurality of said second local sense amplifier drive transistors"). (*Supra* Sections IX.A.1(a),(c),(d); Ex.1002, ¶111.) Specifically, clock ϕ_3 would have controlled the turning ON/OFF for each transistor Q_{N10} because when "clock ϕ_3 is made to fall, Q_{N10} is made non-conducting." (Ex.1007, 4, 12 (explaining typographical error on page 4).)



(Ex.1002, ¶111; *supra* Sections IX.A.1(a),(c),(d).)

k) "a first voltage supply line coupled to said plurality of said first local sense amplifier drive transistors;"

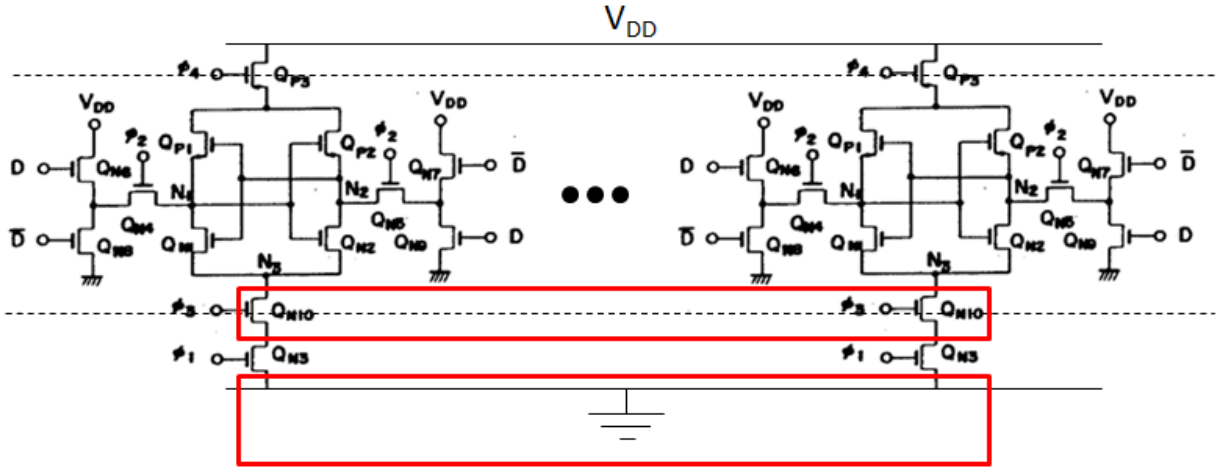
The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶112.) In the combined *Inoue-Min-Hamade* system, V_{DD} ("a first voltage supply line") would have been coupled to transistors Q_{P3} of respective columns ("said plurality of said first local sense amplifier drive transistors"). (*Supra* Sections IX.A.1(a),(c),(d); Ex.1002, ¶112.)



(Ex.1002, ¶112.)

l) "a second voltage line coupled to said plurality of second local sense amplifier drive transistors;"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶113.) In the *Inoue-Min-Hamade* combination, the ground node ("a second voltage supply line") would have been coupled to transistors Q_{N10} of respective columns ("said plurality of second local sense amplifier drive transistors"). (*Supra* Sections IX.A.1(a),(c),(d); Ex.1002, ¶113.)



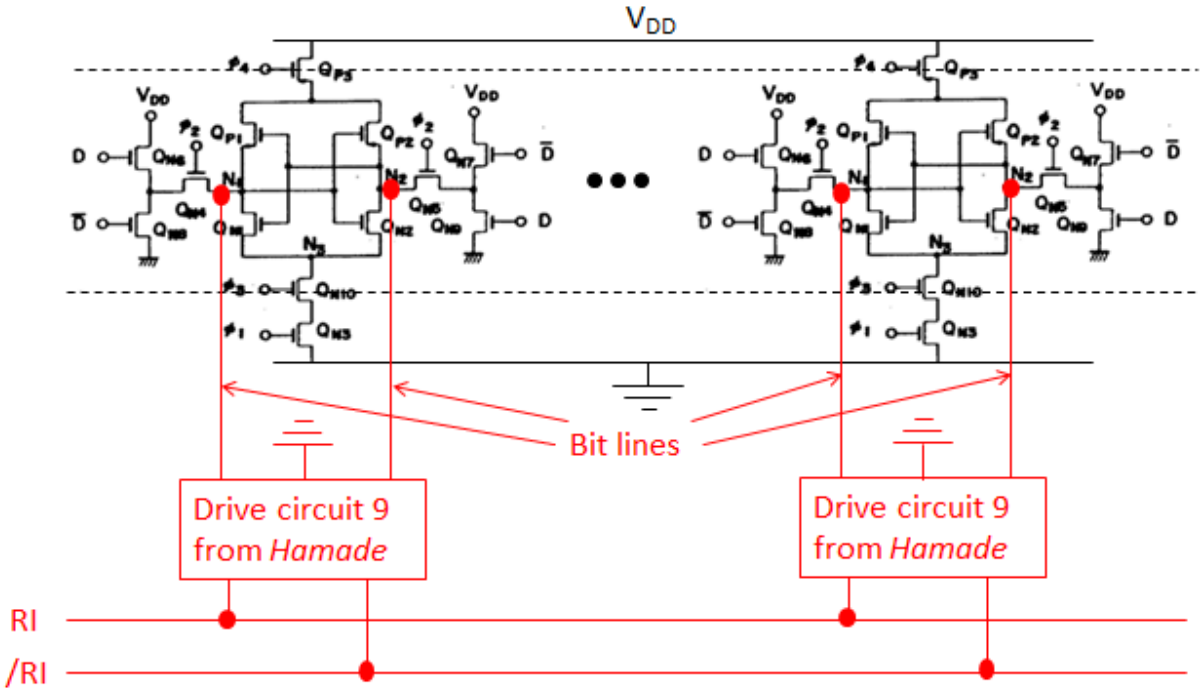
(Ex.1002, ¶113.)

At each column, transistor Q_{N3}, which is between transistors Q_{N10} and ground, facilitates this coupling. (*Supra* Section IX.A.1(h); Ex.1002, ¶113.) Claim limitation 1(p) supports this understanding, as that limitation recites "each said local data write driver circuit is coupled to . . . a respective one of said internal nodes" and figure 5 of the '574 patent shows that a pass transistor 122/124 facilitates that claimed coupling. (Ex.1001, FIG. 5; Ex.1002, ¶113.)

m) "wherein each said column read amplifier is responsively coupled to said internal nodes of said latch circuit of a corresponding sense amplifier; and"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶114.) As is apparent from the annotated figure below, in the combined *Inoue-Min-Hamade* system, each drive circuit 9 (from *Hamade)* as implemented in the combined system would have been responsively coupled to nodes N_1, N_2 for

each latch circuit (P-channel transistors Q_{P1}, Q_{P2}, and N-channel transistors Q_{N1}, Q_{N2}) of a corresponding sense amplifier. (*Id.*, ¶114; *supra* Sections IX.A.1(a),(d).)



(Ex.1002, ¶114 (non-limiting illustration of the combined *Inoue-Min-Hamade* system.)

Inoue's internal nodes N_1 and N_2 of the latch circuit of figure 6 "correspond to bit lines." (Ex.1007, 4) Moreover, the drive circuit 9 of *Hamade*'s figure 1 includes transistors Q16 and Q17 having their gates coupled to bit lines BL and /BL. (Ex.1009, FIG. 9, 2:60-63[10].) Therefore, a skilled artisan would have

[10] The configuration of drive circuit 7b in figure 7 of *Hamade* is identical to the configuration of drive circuit 9 in figure 1. (Ex.1002 at ¶115.)

understood that nodes N_1 and N_2 would have been connected to transistors Q16 and Q17 of drive circuit 9 in the *Inoue-Min-Hamade* combination. (*Supra* Section IX.A.1(d); Ex.1002, ¶¶82-95 for reasons to combine *Inoue-Min* with *Hamade*.) Hence, the column read amplifier in each column in the *Inoue-Min-Hamade* combination ("each said column read amplifier") would have been "responsively coupled to said internal nodes of said latch circuit of a corresponding sense amplifier" because transistors Q16 and Q17 will conduct current based on the potentials at nodes N_1 and N_2. (Ex.1002, ¶115.)

The '574 patent discloses a similar configuration, as shown below.

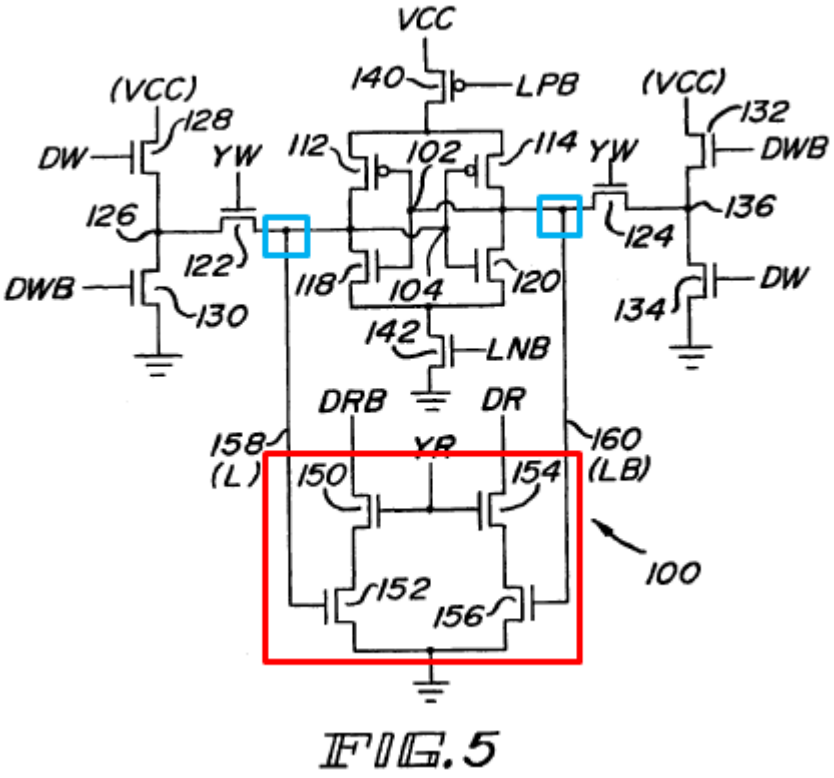


FIG. 5

(Ex.1002, ¶116, citing Ex.1001, FIG. 5 (annotated).)

n) "wherein each said sense amplifier is coupled to a pair of said local data write driver circuits,"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶117.) *Inoue* discloses that "Q_{N5}, Q_{N7}, Q_{N9} and Q_{N4}, Q_{N6}, Q_{N8} are write circuits that determine the state of the F/F." (Ex.1007, 3, FIG. 6.) The inputs to circuits Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9}, i.e., "D, $\overline{D}$ [are] write data input terminals used to write data to F/F," where F/F refers to a flip-flop. (*Id.*, 3; Ex.1002, ¶117.) Therefore, a POSITA would have understood that Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} constitute a pair of "data write driver circuits." (Ex.1002, ¶117.)

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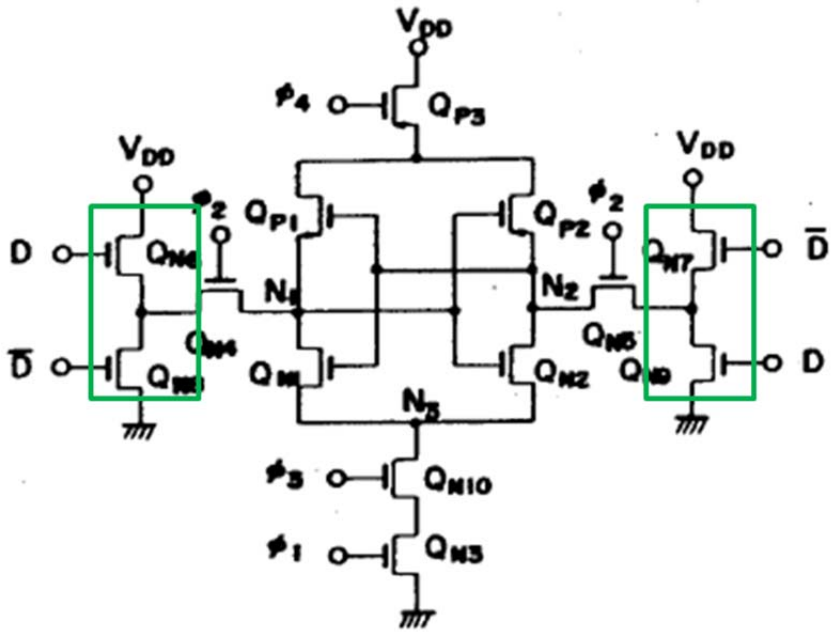


(Ex.1002, ¶117, citing Ex.1007, FIG. 6 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

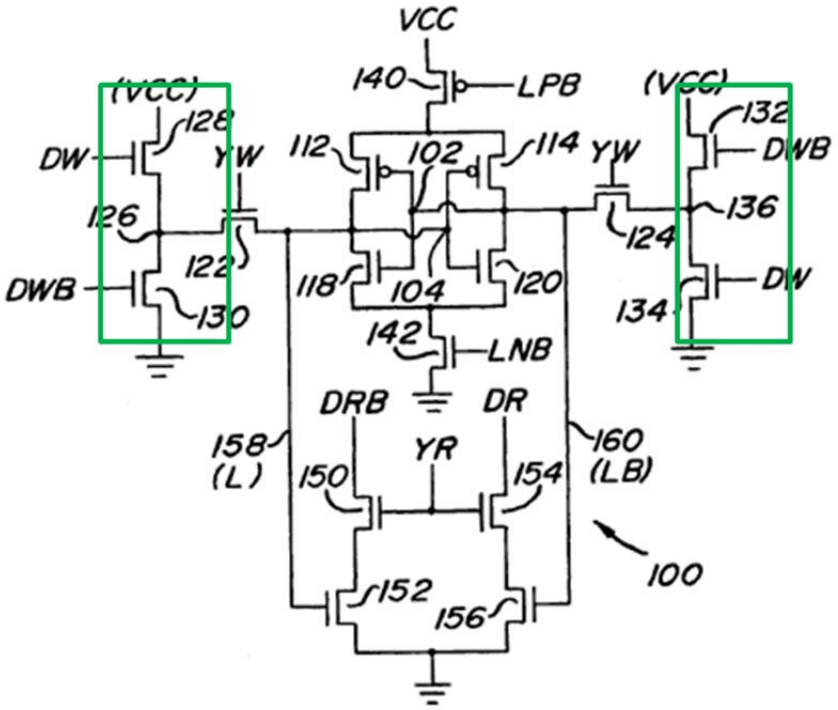
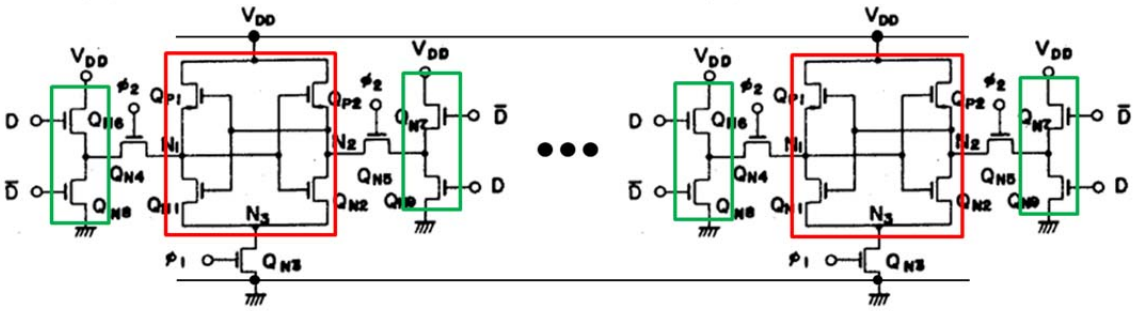


FIG. 5

(Ex.1002, ¶118, citing Ex.1001, FIG. 5 (annotated).)

Moreover, as seen in the annotated figure below, in the combined *Inoue-Min-Hamade* system, each latch circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) and therefore, each "sense amplifier," is coupled to only one pair of data write driver circuits that includes transistors Q_{N6} and $Q_{N8,}$ or Q_{N7} and Q_{N9}. (*See* annotated figure below; Ex.1002, ¶119.) Therefore, Q_{N6}, $Q_{N8,}$ and $Q_{N7,}$ Q_{N9} constitute "a pair of **local** data write driver circuits." (Ex.1002, ¶44-47, 117; *see also supra* Section VIII.A)



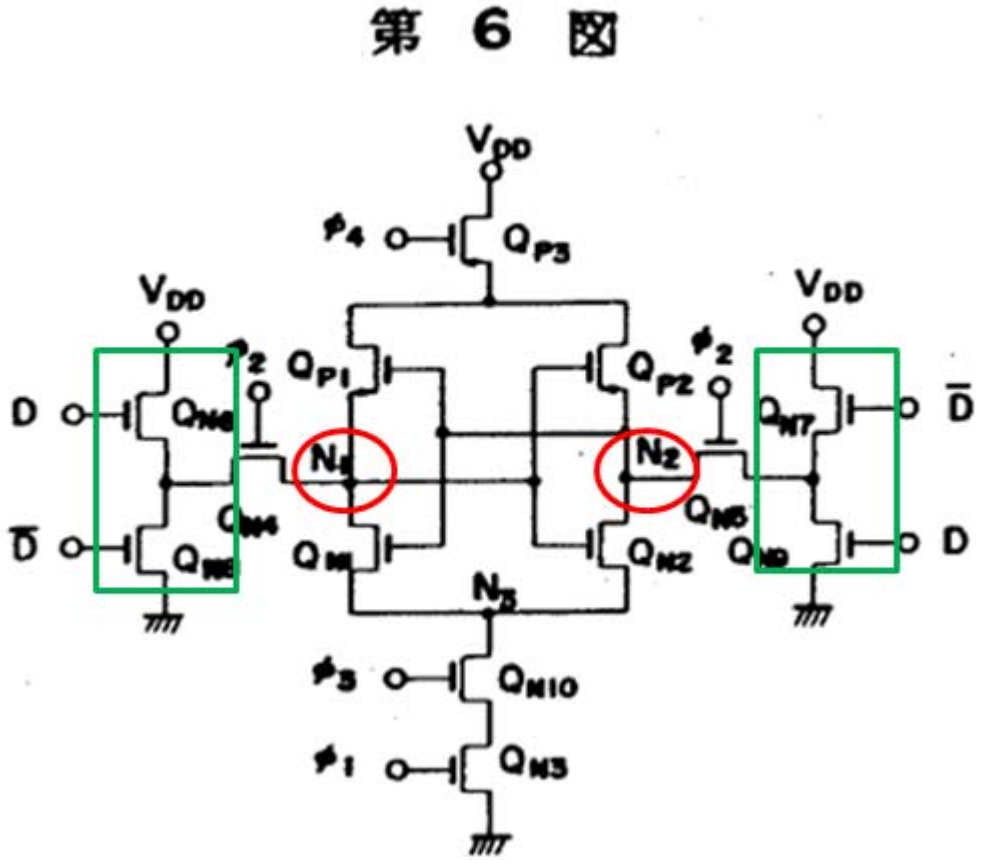
(Ex.1002, ¶119, annotated to show sense amplifiers (each of which is constituted by a "latch circuit") in red and circuitry corresponding to claimed pairs of local data write driver circuits in green.)

o) "each local data write driver circuit being configured to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes;"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶120.) In the *Inoue-Min-Hamade* combination, each pair of transistors Q_{N6}/Q_{N8} or transistors Q_{N7}/Q_{N9} ("each local data write driver circuit") (green below) would have been configured to (1) receive data at their gate terminals D and $\overline{D}$ ("receive write data") during a write operation at a gate electrode of a transistor Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("a transistor in said data write driver circuit") in said data write driver circuit, and (2) apply a signal corresponding to a level 'H' or 'L' ("apply a signal") based upon receiving data D or $\overline{D}$ ("based upon receiving said write data") to node N_1 or N_2 of the latch circuit ("one of said latch circuit

nodes") (red below). (*Supra* Sections IX.A.1(a),(d),(e),(f); Ex.1007, FIG. 6; Ex.1002, ¶120.)

Referring to figure 6 of *Inoue* (shown below) for a given column of the combined *Inoue-Min-Hamade* system, terminals D and $\overline{D}$ are "write data input terminals used to write data to [the flip-flop]" (Ex.1007, 3), with D coupled to the gate of transistors Q_{N6} and Q_{N9}, and with $\overline{D}$ coupled to the gate of transistors Q_{N8} and Q_{N7}. Accordingly, the combined *Inoue-Min-Hamade* system discloses "each local data write driver circuit being configured to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit." (Ex.1002, ¶121.)



(Ex.1002, ¶121, citing Ex.1007, FIG. 7 (annotated).)

In addition, *Inoue* discloses that "terminals D and $\overline{D}$ write to the nodes N_1 and N_2." (Ex.1007, 3.) For instance, in one example the local data write driver circuit comprising transistors Q_{N6} and Q_{N8} is configured to apply a signal corresponding to level 'H' to node N_1 of the latch circuit shown in figure 6 based upon receiving data 'H' at terminal D and data 'L' at terminal $\overline{D}$, and the local data write driver circuit comprising transistors Q_{N7} and Q_{N9} is configured to apply a signal corresponding to level 'L' to node N_2 of the latch circuit based upon receiving data 'H' at terminal D and data 'L' at terminal $\overline{D}$. (*Id.*; Ex.1002, ¶122.)

Accordingly, the combined *Inoue-Min-Hamade* system discloses "each local data write driver circuit being configured . . . to apply a signal based upon receiving said write data to one of said latch circuit nodes." (Ex.1002, ¶122.)

The '574 patent discloses a similar configuration, as shown below.

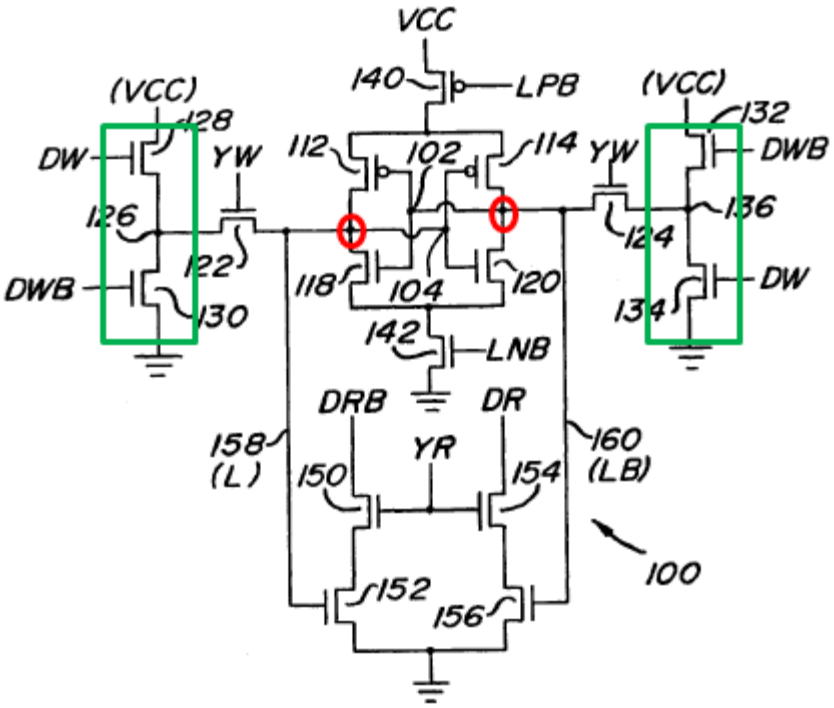


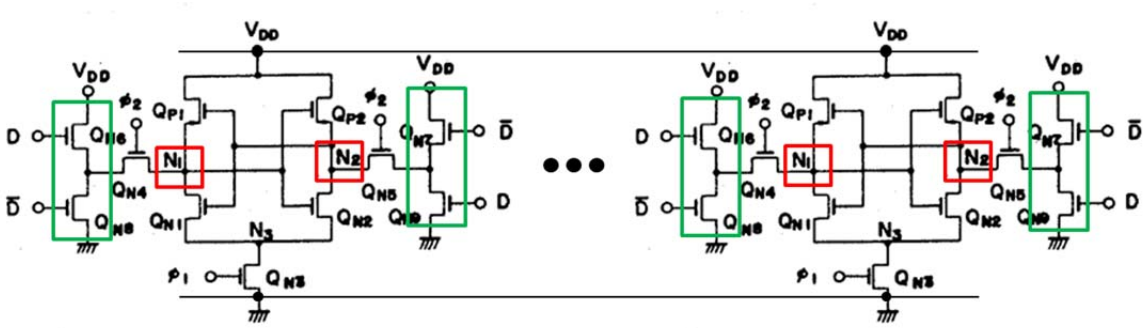
FIG. 5

(*Id.*, ¶123, citing Ex.1001, FIG. 5 (annotated).)

p) "wherein each said local data write driver circuit is coupled to both a respective one of said internal nodes of its corresponding sense amplifier and a corresponding bit line."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶124.) In the *Inoue-Min-Hamade* combination, each pair of transistors Q_{N6}/Q_{N8} or transistors Q_{N7}/Q_{N9} ("each said local data write driver circuit") for each

column would have been coupled to both: 1) one of the internal nodes N_1/N_2 of the sense amplifier of that column ("a respective one of said internal nodes of its corresponding sense amplifier"), and 2) a corresponding bit line of the pair of bit lines associated with that column. (*Supra* Sections IX.A.1(a),(d),(e),(f); Ex.1007, FIG. 6; Ex.1002, ¶124.) Although the bit lines are not explicitly shown in figure 6 of *Inoue*, a POSITA would have understood that *Inoue* discloses the above coupling with respect to "a corresponding bit line" based on *Inoue*'s disclosure that "N_1 and N_2 correspond to bit lines." (Ex.1007, 4; Ex.1002, ¶124; *see also supra* Section IX.A.1(a).)



(Ex.1002, ¶124, annotated to show components constituting claimed local data write driver circuits in green, and nodes N_1 and N_2 in red).)

The '574 patent discloses a similar configuration, as shown below.

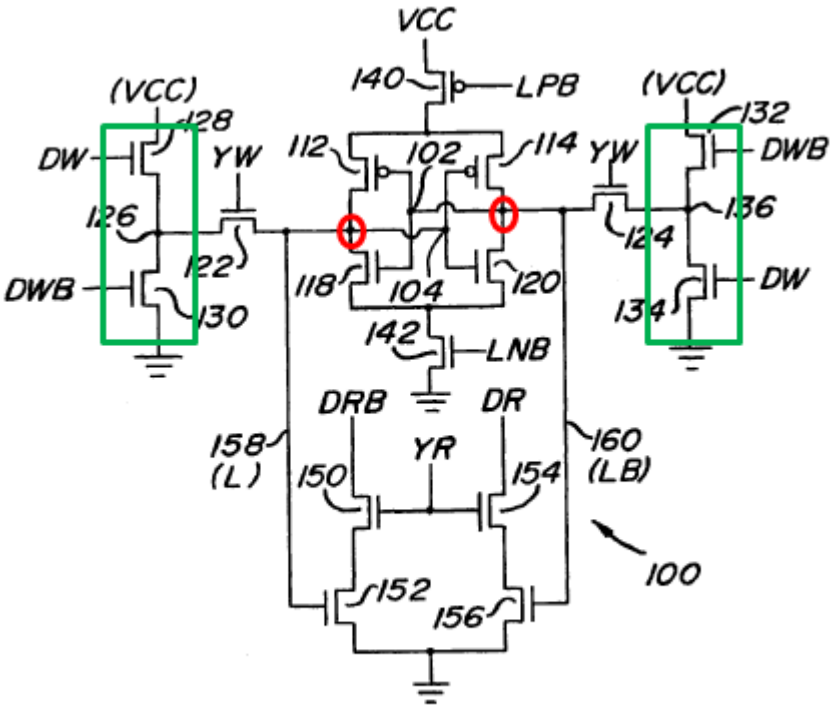


FIG. 5

(Ex.1002, ¶125, citing Ex.1001, FIG. 5 (annotated).)

2. Claim 2

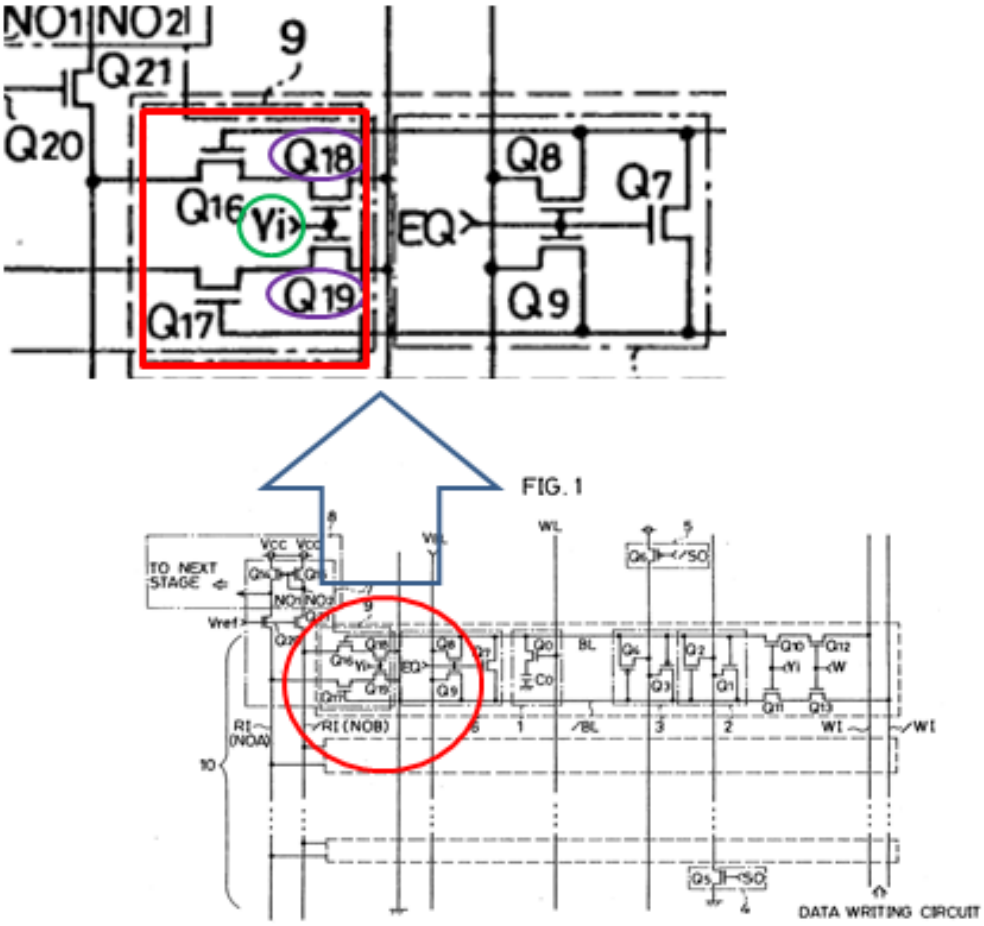
a) "The circuit combination according to claim 1 wherein said read amplifier is also responsively coupled to read control signals and"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶126.) As discussed above with respect to claim limitation 1(d), a POSITA would have found it obvious to modify the combined *Inoue-Min* system to include, for each of the plurality of sense amplifiers, a drive circuit 9 and related circuitry (e.g., read only data lines RI, /RI) associated with operation of drive circuit 9 as disclosed in *Hamade*. (*Supra* Section IX.A.1(d); Ex.1002, ¶126.) A

POSITA would have also understood that it would have been advantageous to incorporate the column selecting signal Yi associated with drive circuit 9 in *Hamade* in the combined *Inoue-Min-Hamade* system because the column selecting signal Yi would have allowed the selection of a particular column for reading and hence would have made possible operation of the multi-column memory device in the combined *Inoue-Min-Hamade* system. (Ex.1002, ¶126.)

Therefore, the POSITA would have been motivated to provide, in the combined *Inoue-Min-Hamade* system, the column selecting signal Yi to the gates of transistors Q18 and Q19 as illustrated in figure 1 of *Hamade* so that "[w]hen column selecting signal Yi rises from the low level to the high level, transistors Q18 and Q19 are turned on." (Ex.1009, 8:24-26, FIG. 1; Ex.1002, ¶127.) Hence, in the *Inoue-Min-Hamade* combination, the drive circuit 9 (Ex.1009, FIG. 1) ("said read amplifier") would have been responsively coupled to receive a column selecting signal Yi ("read control signals"). (Ex.1002, ¶127.) A POSITA would have understood that Yi is a "read control signal" because it is used for selecting a column during a read operation. (*Id.*; Ex.1009, 8:8-26.) Indeed, column selecting signal Yi is no different from "column read signal Y_R" (Ex.1001, 7:8, FIG. 5), which Patent Owner explained corresponds to the claimed "read control signals." (Ex.1004, 171 (stating that claim 11 (which issued as claim 2) "recites that said read amplifier (150, 152, 154, 156) is also responsively coupled to **read control**

signals (YR)") (emphasis added); Ex.1002, ¶127.) Finally, a skilled artisan would have understood that each column in the combined system would have its own column selecting signal Yi to address the selected column in the memory array and therefore, there exists a plurality of column selecting signals Y_i. (Ex.1002, ¶129.) Hence, column selecting signal Yi reads on the claimed "read control signals." (*Id*. (emphasis added).)



(*Id*., ¶127, citing Ex.1009, FIG. 1, annotated to show transistors Q18 and Q19 (purple) of drive circuit 9 ("said read amplifier") (shown with red rectangle), and to show Yi ("read control signals") in green).)

The '574 patent discloses a similar configuration, as shown below.

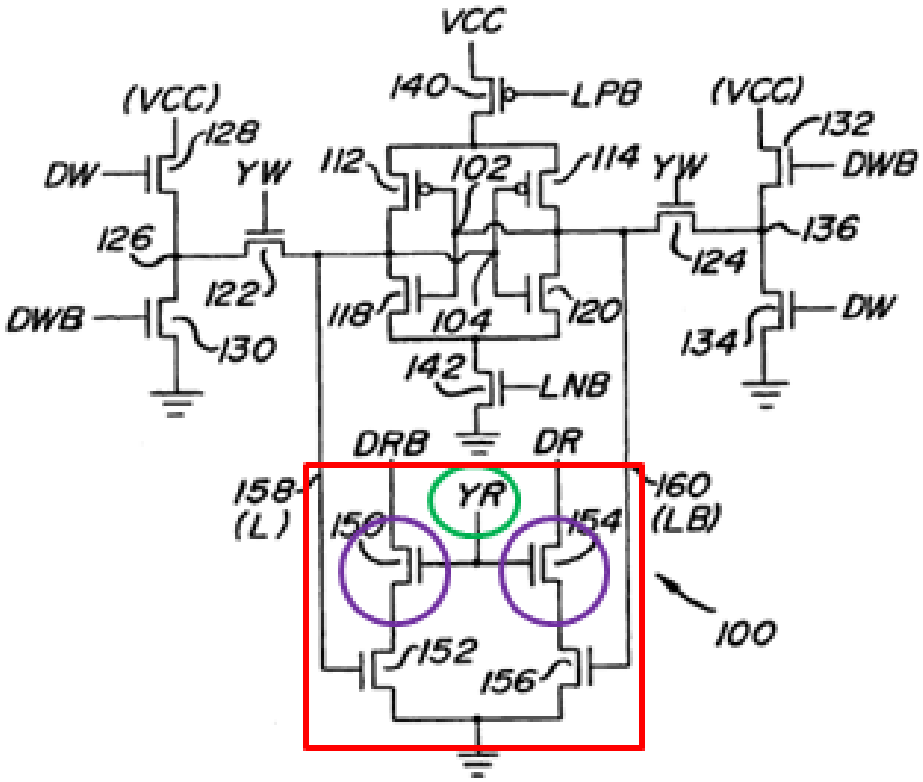


FIG. 5

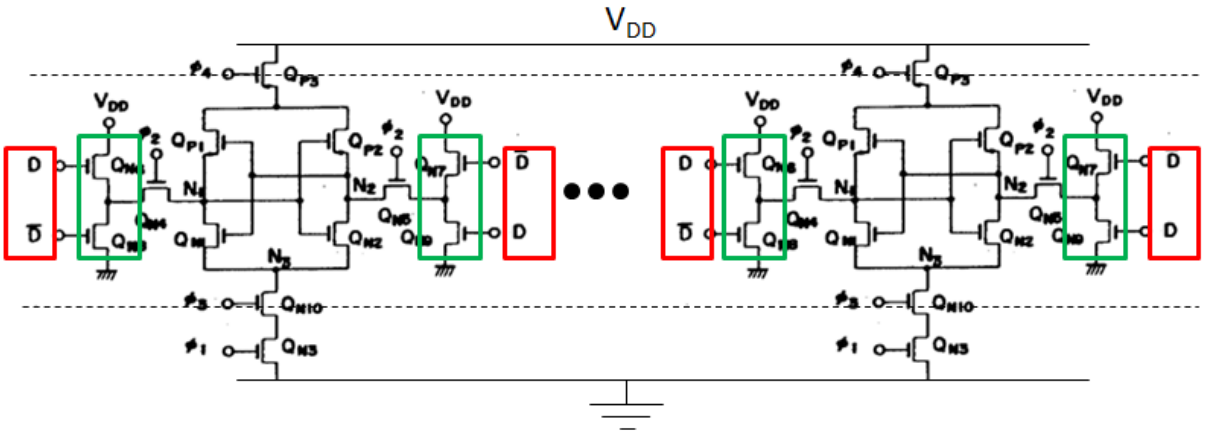
(Ex.1002, ¶128, citing Ex.1001, FIG. 5 (annotated).)

b) "wherein said local data write driver transistors are responsively coupled to data write control signals."

The combined *Inoue-Min-Hamade* system discloses this feature.[11] (Ex.1002, ¶130.) For example, in the combined *Inoue-Min-Hamade* combination, each column would have had a corresponding pair of circuits comprising transistors Q_{N6}/Q_{N8} and transistors Q_{N7}/Q_{N9} ("said local data write driver circuits")

[11] There is no antecedent basis for "said local data write driver transistors," and Petitioner assumes "said local data write driver circuits" was intended in claim 2.

(green) responsively coupled to "write data input terminals" D and $\overline{D}$ ("data write control signals") (red), as shown below. (*Supra* Sections IX.A.1(a),(d),(e); Ex.1002, ¶130.)



(Ex.1002, ¶130.)

Inoue discloses that "D, $\overline{D}$ [are] write data input terminals used to write data to F/F" where F/F refers to a flip-flop. (Ex.1007, 3.) Terminal D is the gate terminal of Q_{N6} and Q_{N9}, and terminal $\overline{D}$ is the gate terminal of Q_{N8} and Q_{N7}. (*Id.*, FIG. 6; Ex.1002, ¶131.) Thus, Q_{N6}, Q_{N8}, Q_{N7} and Q_{N9} are responsively coupled to the signals received at write data input terminals D and $\overline{D}$. (Ex.1002, ¶131.)

The '574 patent discloses a similar configuration, as shown below.

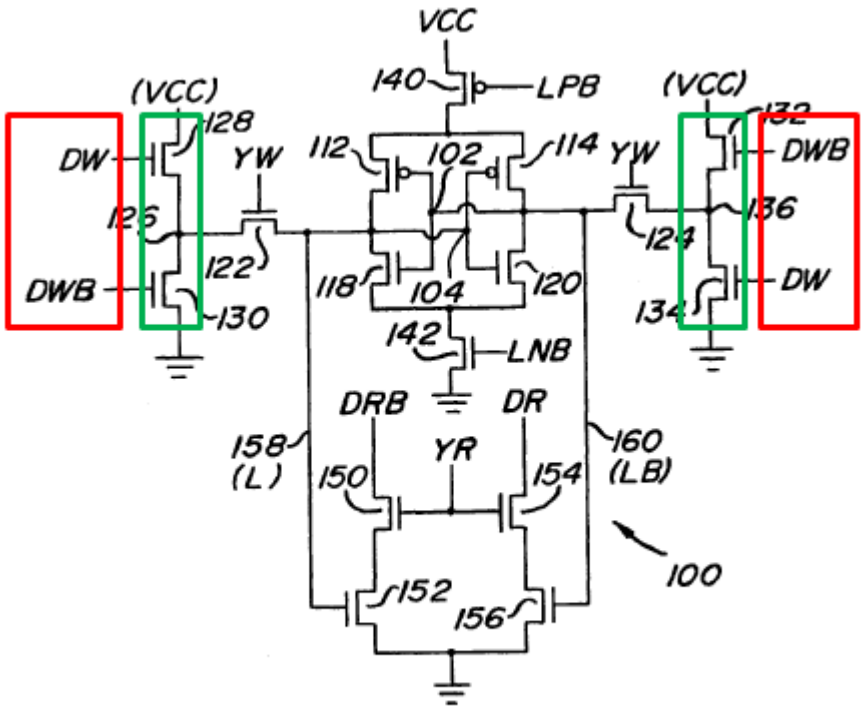


FIG. 5

(Ex.1002, ¶132, citing Ex.1001, FIG. 5 (annotated).)

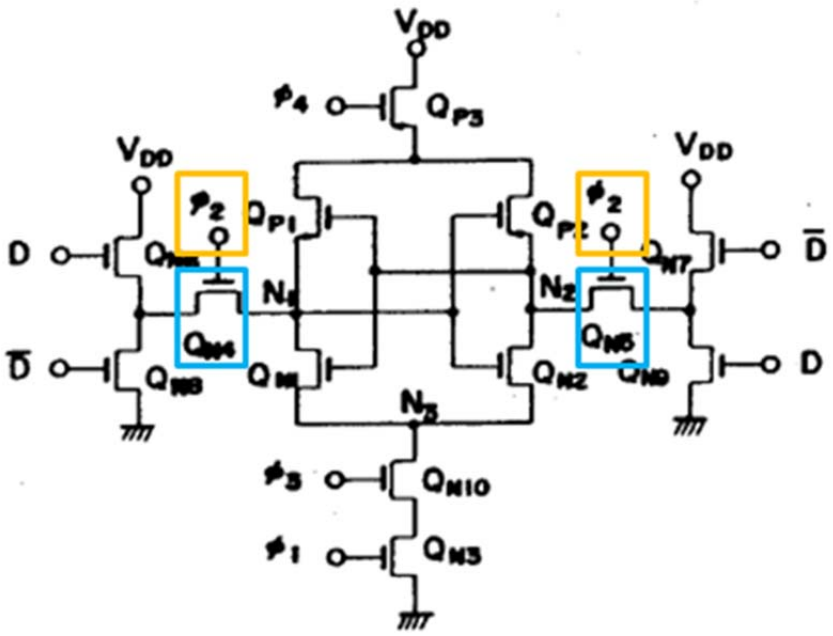
3. Claim 3

a) "The circuit combination according to claim 2 further comprising a pass transistor selectively coupling a corresponding internal node of a said latch circuit to its respective local data write driver circuit, said pass transistor being responsively coupled to a further write control signal."

The combined *Inoue-Min-Hamade* system discloses this feature. (Ex.1002, ¶133.) As discussed above, in the combined *Inoue-Min-Hamade* system discussed above, the circuit of figure 6 in *Inoue* is replicated for each column. (*Supra* Sections IX.A.1(b), IX.A.1(d).) The circuit of figure 6 in *Inoue* includes transistor Q_{N4} or Q_{N5} (each of which is "a pass transistor") selectively coupling node N_1 or

N_2 of the latch circuit of that column ("a corresponding internal node of a said latch circuit") to transistors Q_{N6} and Q_{N8}, or to transistors Q_{N7} and Q_{N9} ("its respective local data write driver circuit"), with transistor Q_{N4} or Q_{N5} ("said pass transistor") being responsively coupled to write control clock ϕ_2 (Ex.1007, 4) ("a further write control signal"), as shown below. (Ex.1007, 4, FIG. 6; Ex.1002, ¶133.)

第 6 図



(Ex.1002, ¶133, citing Ex.1007, FIG. 6 (annotated to show clock ϕ_2 ("further write control signal") in orange and transistors Q_{N4} and Q_{N5} ("pass transistor") in blue).)

A POSITA would have understood that each of transistors Q_{N4}/Q_{N5} is a "pass transistor" and would have "selectively coupl[ed]" a corresponding one of nodes

N_1/N_2 to transistors Q_{N6} and Q_{N8}, or to transistors Q_{N7} and Q_{N9}, because, for example, when operating in a conducting state each of transistors Q_{N4}/Q_{N5} would have allowed current to flow into and out of nodes N_1 (Q_{N4}) or N_2 (Q_{N5}). (Ex.1007, 3, FIG. 6; Ex.1002, ¶134.)

Inoue discloses that clock ϕ_2, which is provided to the gate terminal of transistors Q_{N4} and Q_{N5} as shown in figure 6, controls the conductivity of those transistors and is, therefore, a "control signal" to which each of those transistors is "responsively coupled." (Ex.1007, 3; Ex.1002, ¶135.) *Inoue* further discloses that clock ϕ_2 is used for writing to nodes N_1 and N_2. (Ex.1007, 3-4; Ex.1002, ¶135.) Therefore, a POSITA would have understood that ϕ_2 is a "further write control signal" to which each of transistors Q_{N4}/Q_{N5} is "responsively coupled." (Ex.1002, ¶135.)

The '574 patent discloses a similar configuration, as shown below.

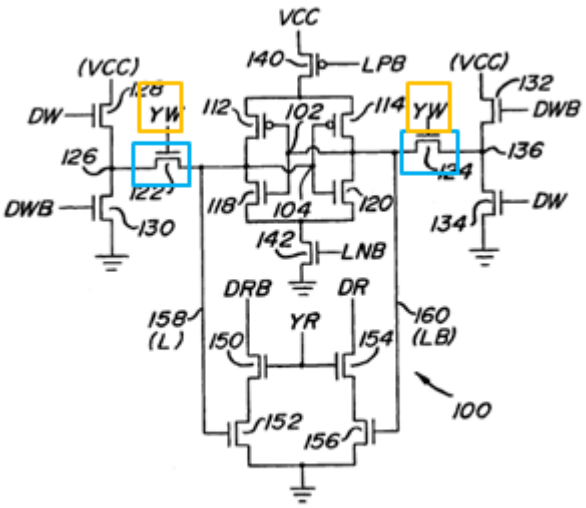


FIG. 5

(Ex.1002, ¶136, citing Ex.1001, FIG. 5 (annotated).)

4. Claim 30

a) "A sense amplifier arrangement for an integrated circuit memory comprising,"

To the extent the preamble is limiting, *Inoue* discloses this feature. (Ex.1002, ¶137.) For example, *Inoue* discloses "a semiconductor device" comprising a sense amplifier with a flip-flop circuit. (Ex.1007, 1 (Claim 1).) The circuit in figure 6 of *Inoue* is for a sense amplifier in a dynamic memory. (*See id.*, 4; IX.A.1(a); Ex.1002, ¶137.) A POSITA would have understood that "dynamic memory" in *Inoue* refers to a DRAM, which is an integrated circuit memory. (*See* Ex.1002, ¶137; citations and analysis below for the remaining elements of this claim.)

b) "for each of a plurality of sense amplifiers: a sense amplifier latch circuit having first and second latch nodes to which respective bit lines may be coupled;"

To the extent "may be coupled" does not render claim 30 indefinite[12], *Inoue* in combination with *Min* discloses or suggests this feature. (Ex.1002, ¶138.) As discussed above with respect to claim element 1(a), *Inoue*'s figure 6 embodiment discloses a CMOS flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} having nodes

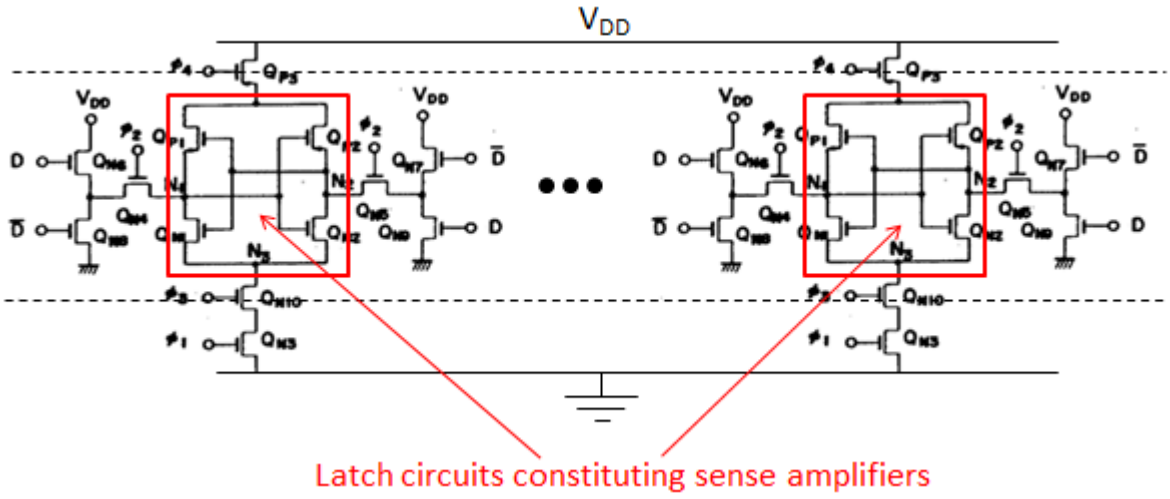
[12] For purposes of this proceeding, Petitioner assumes "may be coupled" specifies a required coupling, but does not concede the definiteness of the claim.

N_1 and N_2 to which respective bit lines are coupled. (*Supra* Section IX.A.1(a), Ex.1007, 3, 4, FIG. 6; Ex.1002, ¶138.) As further discussed above with respect to claim element 1(a), a POSITA would have understood that the flip-flop of figure 6 is part of one sense amplifier and that other sense amplifiers are also present in *Inoue*'s dynamic memory. (*Supra* Section IX.A.1(a); Ex.1002, ¶138.) While *Inoue* does not expressly show the multiple sense amplifiers in any figure, nor does *Inoue* expressly show a figure with a plurality of bit line pairs corresponding to such sense amplifiers[13], a POSITA would have found it obvious to implement *Inoue*'s figure 6 circuit in a multi-column memory system to create a dynamic memory based on the teachings of *Min*. (Ex.1002, ¶138.) The resulting *Inoue-Min* combined system discloses the features of claim limitation 30(b). (*Id*.)

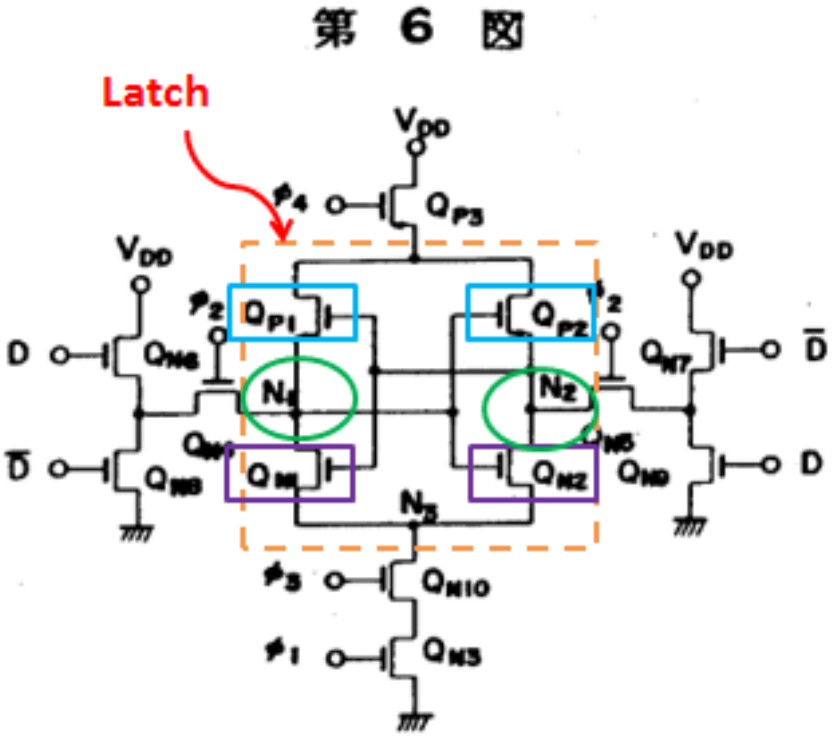
Specifically, as discussed above with respect to claim limitation 1(b), the combined system includes a replication of *Inoue*'s figure 6 circuit, which includes a latch circuit constituted by PMOS transistors Q_{P1} and Q_{P2} and NMOS transistors Q_{N1} and Q_{N2}. (Ex.1002, ¶139; *see also supra* Section IX.A.1(f).) Given that a POSITA would have understood that the "latch circuit" in *Inoue* is the same as a "sense amplifier" in the context of the '574 patent, the combined *Inoue-Min* system thus discloses "a plurality of sense amplifiers" where each "sense amplifier" is the latch circuit constituted by PMOS transistors Q_{P1} and Q_{P2} and NMOS transistors

[13] Claim element 30(b) requires a plurality of bit line pairs.

Q_{N1} and Q_{N2}. (*Supra* Sections IX.A.1(b),(f); Ex.1002, ¶139.) Hence, the combined *Inoue-Min* system discloses "for each of a plurality of sense amplifiers," a latch circuit ("sense amplifier latch circuit") constituted by PMOS transistors Q_{P1} and Q_{P2} and NMOS transistors Q_{N1} and Q_{N2}. (Ex.1002, ¶139.) Each such latch circuit includes nodes N_1 and N_2 ("first and second latch nodes") to which respective bit lines are coupled. (Ex.1002, ¶139; *supra* Section IX.A.1(a); *see also supra* Section IX.A.1(f).) The above features are evident from the following figures.



(Ex.1002, ¶139.)



(Ex.1002, ¶139, citing Ex.1007, FIG. 6.)

The ’574 patent discloses a similar configuration, as shown below.

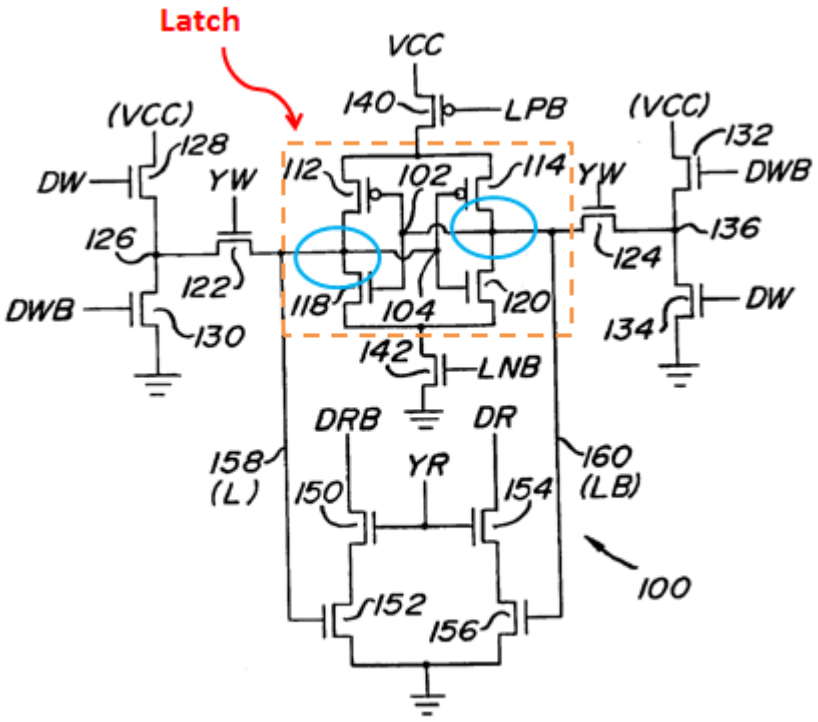


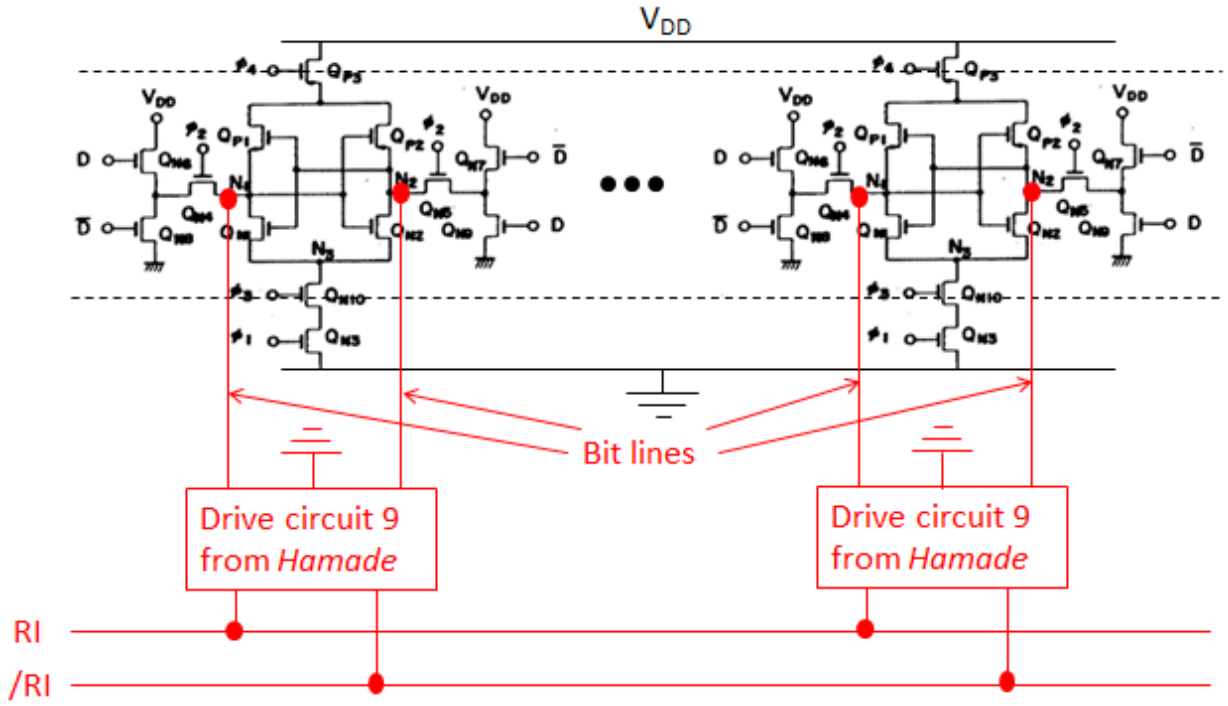
FIG. 5

(Ex.1002, ¶140, citing Ex.1001, FIG. 5 (annotated).)

c) "[for each of the plurality of sense amplifiers:] a local column read amplifier having transistors responsively coupled to at least one of said first and second latch nodes, and receiving at least one data read signal, said local read amplifier being configured to control the current of said data read signal based on the state of said one latch node; and"

The combined *Inoue-Min* system discussed above for limitation 30(b) does not expressly disclose this feature. But as discussed above with respect to claim limitation 1(d), a POSITA would have found it obvious to modify the combined *Inoue-Min* system to include, for each of the plurality of sense amplifiers, a drive circuit 9 and related circuitry (e.g., read only data lines RI, /RI) associated with

operation of drive circuit 9 as disclosed in *Hamade*. (*Supra* Section IX.A.1(d); Ex.1002, ¶141.) In the combined *Inoue-Min-Hamade* system according to these modifications, at each column the drive circuit 9 and read only data lines RI and /RI as implemented in the combined system would have been configured in the manner described above for limitation 1(d). (*Supra* Section IX.A.1(d); Ex.1002, ¶141.)



(Ex.1002, ¶141, illustrating a non-limiting visual demonstrative of the combined *Inoue-Min-Hamade* system; *supra* section IX.A.1(d).)

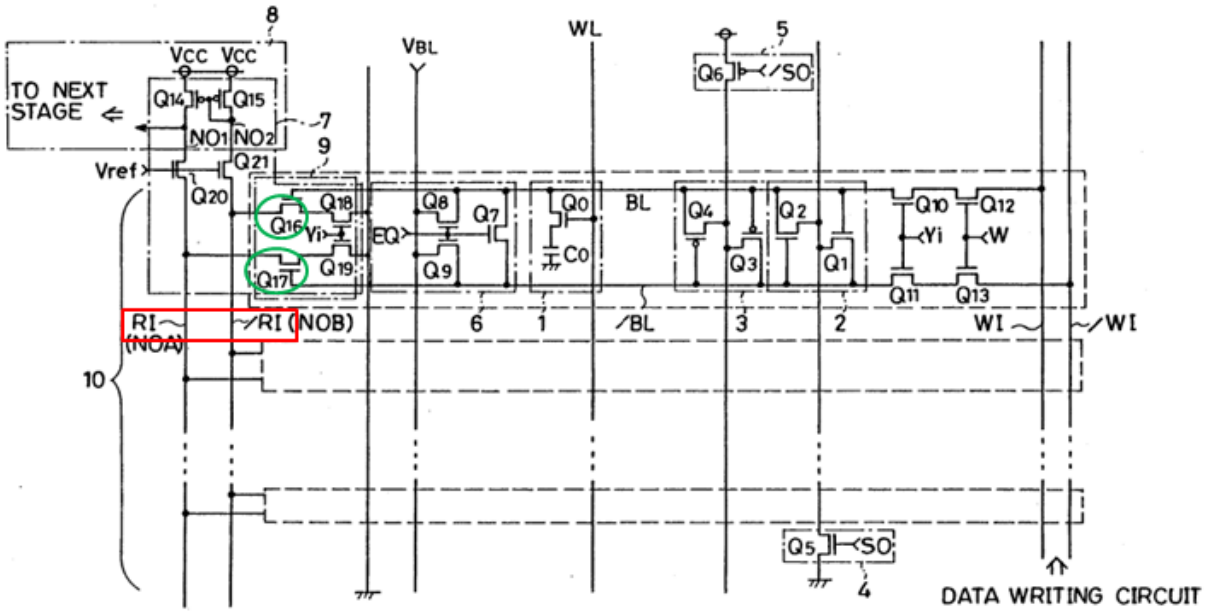
The resulting combined *Inoue-Min-Hamade* system discloses claim element 30(c). (Ex.1002, ¶142.) For instance, as is apparent from the above demonstrative of the combined system, for each sense amplifier in a respective column, there is a

corresponding drive circuit 9 ("local column read amplifier"). (*Supra* Section IX.A.1(d) (explaining that drive circuit 9 constitutes a "local column read amplifier"); Ex.1002, ¶142.)

A POSITA would have further understood that drive circuit 9, as combined with *Inoue-Min*, would have included the gates of NMOS transistors Q16 and Q17 (green below) coupled to nodes N_1 and N_2 of figure 6 of *Inoue*, respectively, because gates of transistors Q17 and Q16 in drive circuit 9 receive the bit line signals (Ex.1009, FIG. 1), and *Inoue*'s N_1 and N_2 correspond to bit lines. (*Id.*; Ex.1007, 3, 4, FIG. 6; Ex.1002, ¶143.) Therefore, the combined system discloses "a local column read amplifier **having transistors responsively coupled to at least one of said first and second latch nodes**" (emphasis added). (Ex.1002, ¶143.)

Moreover, the drive circuit 9 ("local column read amplifier") would receive signals on read only data lines RI and /RI ("receiving at least one data read signal") in the combined system. (*Supra* Sections IX.A.1(d) (explaining reasons to include read only data lines RI and /RI in the combined system); *see also* Ex.1009, FIG. 1 (annotated below), 7:35-39; Ex.1002, ¶144.)

FIG. 1

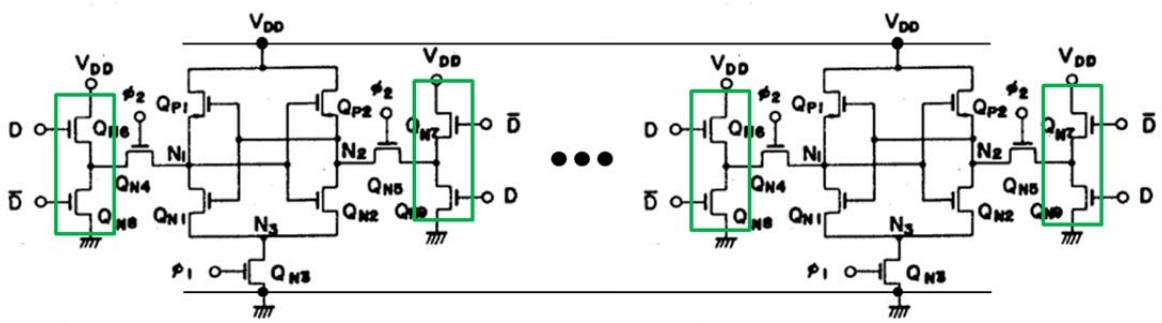


(Ex.1002, ¶144, citing Ex.1009, FIG. 1.)

Because the combined *Inoue-Min-Hamade* system incorporates the drive circuit 9 and read only data lines /RI and RI from *Hamade* and the latch nodes N_1 and N_2 from *Inoue* would have been coupled to the gates of transistors Q16 and Q17 (*see* discussion above), the drive circuit 9 ("local column read amplifier") would have controlled the current of read only data lines /RI and RI ("said data read signal") based on the state of nodes N_1 and N_2 ("said one latch node"). (Ex.1002, ¶145.) This is because based on the potentials of the bit lines (i.e., the potentials at nodes N_1 and N_2), transistors Q16 and Q17 would have discharged RI and /RI to ground, respectively. (*Id.*; *supra* Section IX.A.1(d).)

d) "[for each of the plurality of sense amplifiers:] first and second local data write driver circuits, each being configured to receive a respective data signal at a respective gate electrode of first write driver transistors in said first and second local data write driver circuits,"

The combined *Inoue-Min-Hamade* discloses this feature. (Ex.1002, ¶146.) For instance, in the combined *Inoue-Min-Hamade* system discussed above for limitation 30(c), each column of the memory array (and thus each of the plurality of sense amplifiers) would have had a circuit comprising transistors Q_{N6} and Q_{N8}, and a circuit comprising transistors Q_{N7} and Q_{N9} (collectively, "first and second local data write driver circuits") (green below). (*Supra* Sections IX.A.1(e), IX.A.4(c); Ex.1007, FIG. 6; Ex.1002, ¶146.) Each of those data write driver circuits at each column in the combined *Inoue-Min-Hamade* system would have been configured to receive data at terminals D and $\overline{D}$ (either of which is "a respective data signal") coupled to a respective gate electrode of transistors Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("at a respective gate electrode of first write driver transistors in said first and second local data write driver circuits") as shown in figure 6 of *Inoue*. (*Supra* Sections IX.A.1(o), IX.A.4(a),(c); Ex.1007, FIG. 6; Ex.1002, ¶146.)



(Ex.1002, ¶146, citing Ex.1007, FIG. 6; Ex.1008, FIG. 3B (annotated).)

The '574 patent discloses a similar configuration, as shown below.

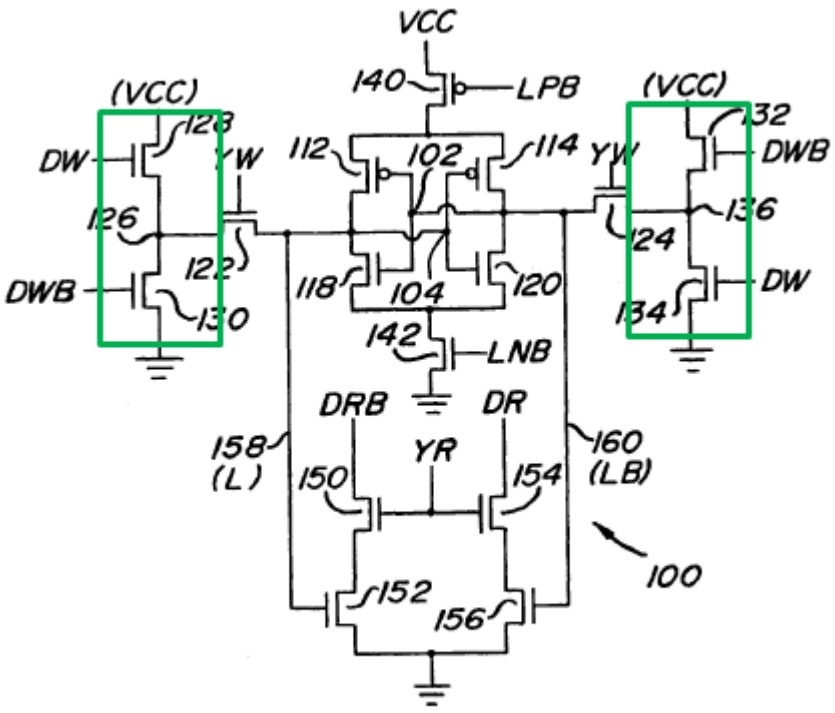


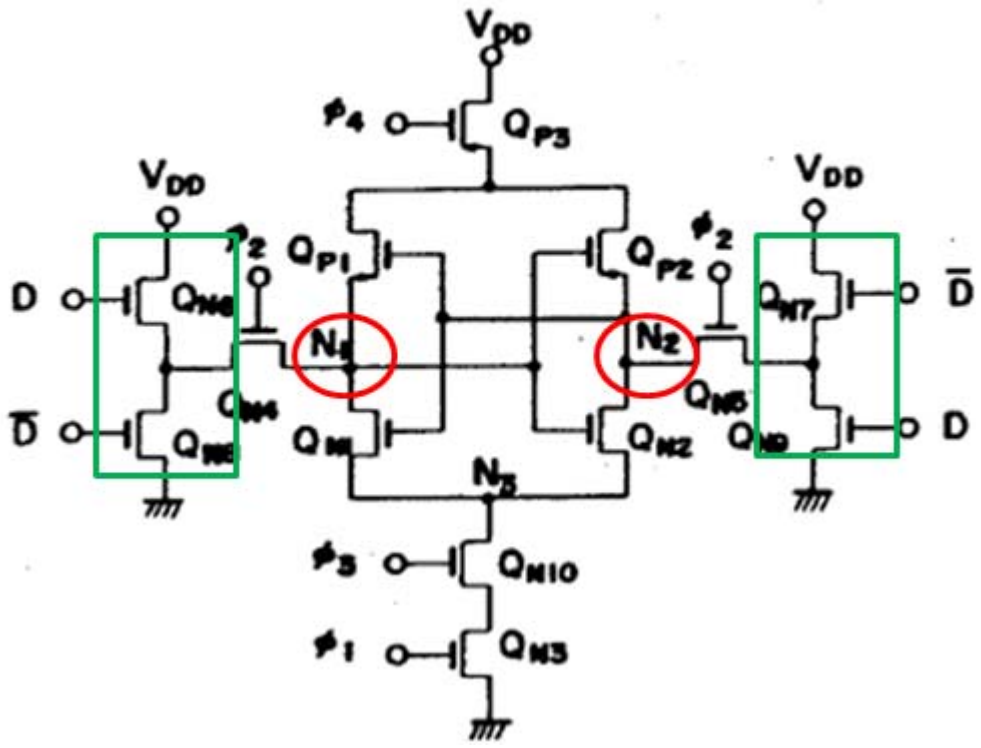
FIG. 5

(Ex.1002, ¶147, citing Ex.1001, FIG. 5 (annotated).)

e) "said first and second data write driver circuits being coupled to said first and second latch nodes to provide signals based on said respective data signal to said first and second latch nodes during a writing operation."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶148.) For example, in the combined *Inoue-Min-Hamade* system discussed above for limitation 30(c), for each sense amplifier, the circuit comprising transistors Q_{N6} and Q_{N8} and the circuit comprising transistors Q_{N7} and Q_{N9} ("said first and second data write driver circuits") (green below) would have been coupled to nodes N_1 and N_2 ("said first and second latch nodes") (red below) to provide signals corresponding to level 'H' and level 'L' ("signals") based on data at terminals D and $\overline{D}$ ("based on said respective data signal") to nodes N_1 and N_2, respectively, ("to said first and second latch nodes") during a writing operation, as shown below in figure 6 of *Inoue*. (*Supra* Sections IX.A.1(o), IX.A.4(a),(c); Ex.1007, 3, FIG. 6; Ex.1002, ¶148.)

第 6 図



(Ex.1002, ¶148, citing Ex.1007, FIG. 7 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

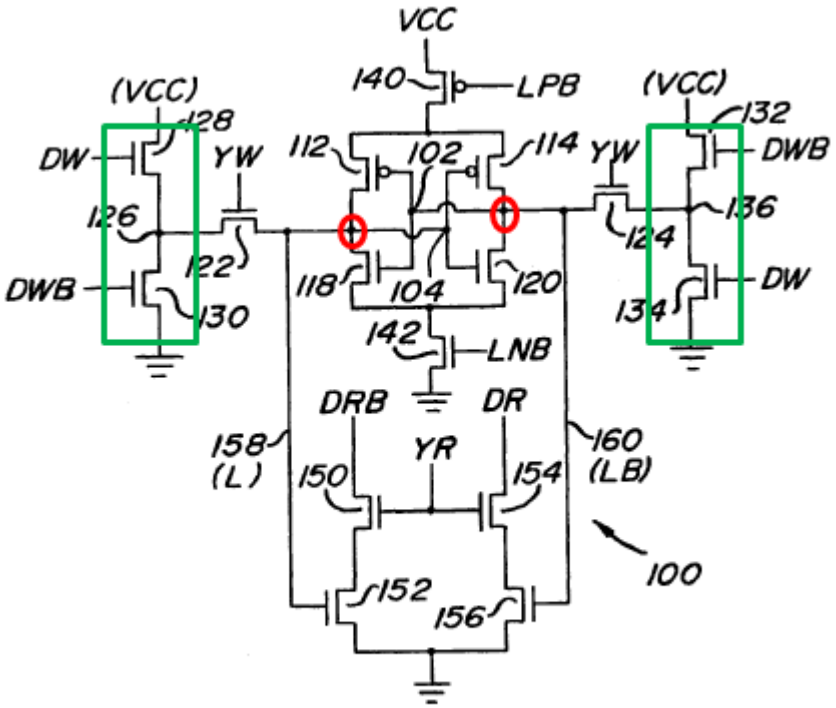


FIG. 5

(Ex.1002, ¶149, citing Ex.1001, FIG. 5 (annotated).)

5. Claim 31

a) "The sense amplifier arrangement according to claim 30 wherein said local column read amplifier is coupled to receive first and second data read signals, and"

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶150.) For example, in the combined *Inoue-Min-Hamade* system discussed above for limitation 30(c), the drive circuit 9 ("said local column read amplifier") as implemented at a given column would have been coupled to receive signals at read only data lines RI and /RI ("first and second data read signals," respectively). (*Supra* Sections IX.A.4(c) (explaining that transistors Q16 and Q17

in driving circuit 9 would have been connected to read only data lines RI and /RI; Ex.1009, FIG. 1; Ex.1002, ¶150.)

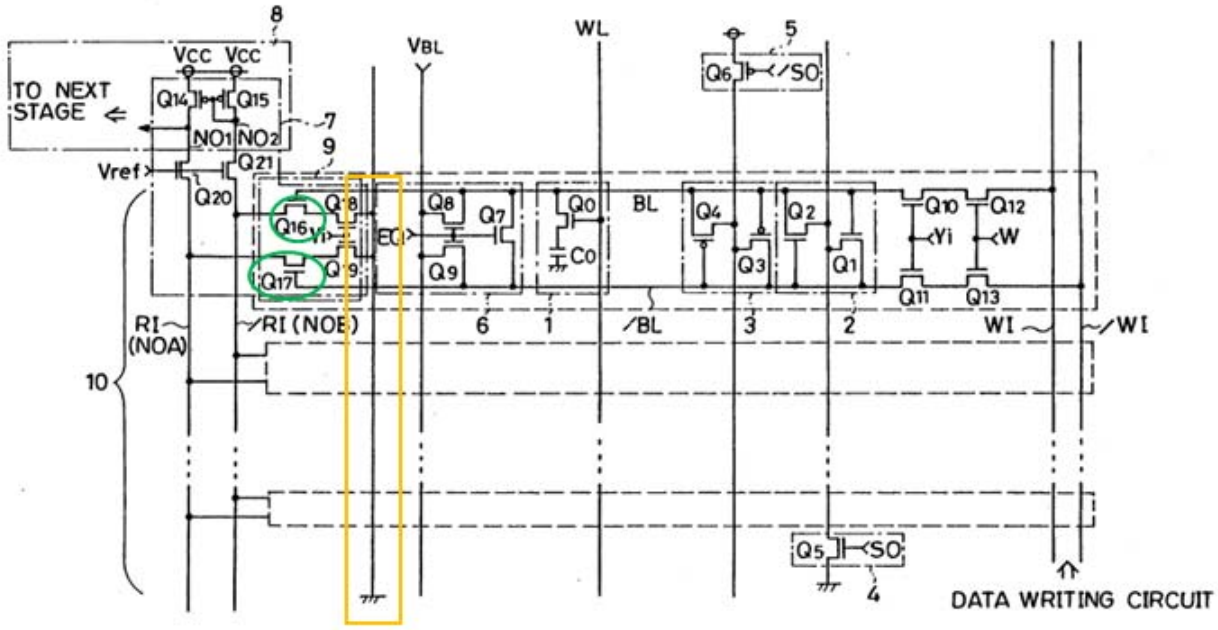
b) "[said local column read amplifier] is configured to connect said first and second data read signals selectively to a first power supply based on conditions of said first and second latch nodes."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶151.) As discussed above with respect to claim element 30(c), in the combined *Inoue-Min-Hamade* system, based on the potentials of the bit lines (i.e., the potentials at nodes N_1 and N_2 ("based on conditions of said first and second latch nodes")), transistors Q16 and Q17 of drive circuit 9 ("local column read amplifier") would have selectively discharged RI and /RI ("connect said first and second data read signals selectively to") ground ("a first power supply"), based on conditions of said first and second latch nodes. (*Supra* Sections IX.A.4(c); Ex.1002, ¶151.) Such operation of the combined system is evident from *Hamade*, which describes the operation of drive circuit 9. (Ex.1002, ¶151.) *Hamade* explains that during a "reading operation" of a memory cell storing a "1," "[w]hen column selecting signal Yi rises from the low level to the high level, **transistors Q18 and Q19 are turned on**." (Ex.1009, 8:8-27 (emphasis added).) As a result, "read only data line /RI is discharged toward the ground potential in order to amplify a minute potential difference appearing between bit lines BL and /BL."

(*Id*., 8:28-31.) A skilled artisan would have understood that this discharging operation would have required transistor Q16 to turn ON and pass current from read only data line /RI to ground. (Ex.1002, ¶151; Ex.1009, 3:62—4:10[14].) Similarly, if the memory cell stored a '0,' read only data line RI would have been discharged to ground by the turning ON of transistor Q17 because the potential on bit line /BL would have been higher than the potential on bit line BL. (Ex.1002, ¶151; Ex.1009, 8:52-54.)

[14] The primary difference between the operation of figure 1 and figure 7 is the provision of transistors Q20 and Q21, which does not change the operation of drive circuit 9, which is identical to drive circuit 7b. (Ex.1002 at ¶151; Ex.1009, FIGS. 1, 7, 2:60-67, 8:11-13, 8:31-41.)

FIG. 1



(Ex.1002, ¶151, citing Ex.1009, FIG. 1 (annotated to show in orange the ground node ("first power supply) and to show in green transistors Q16 and Q17 which perform the selective connection of limitation 31(b)).)

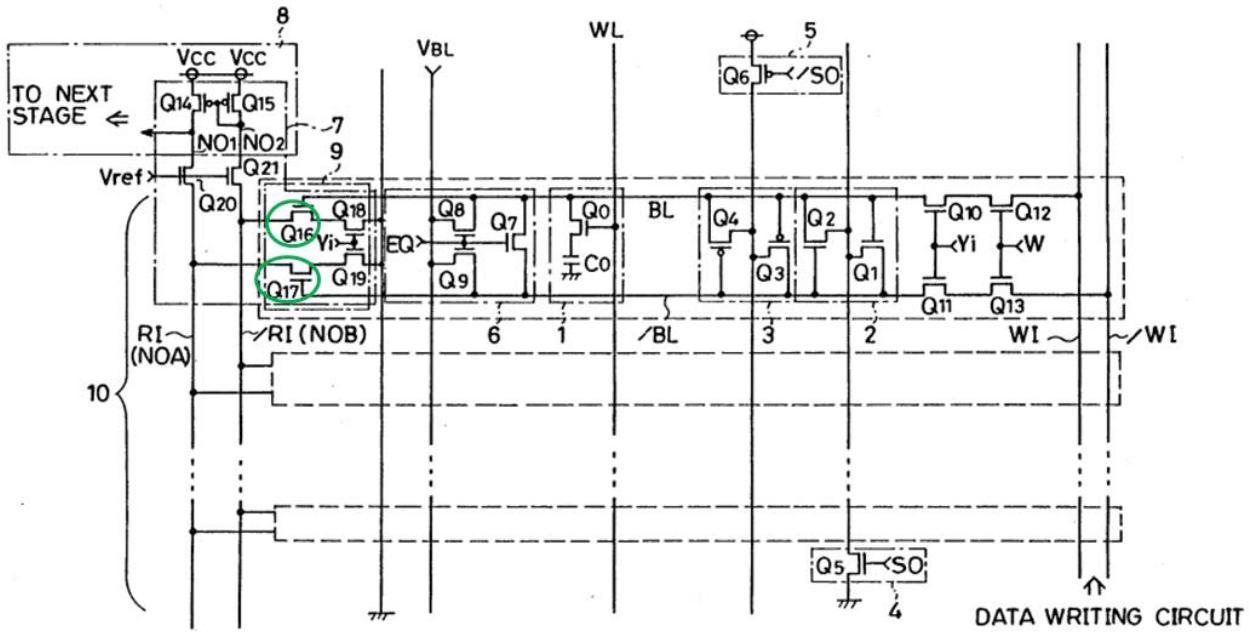
6. Claim 32

a) "The sense amplifier arrangement of claim 31 wherein said local column read amplifier includes first and second read amplifier transistors responsively coupled to said first and second latch nodes,"

In the combined *Inoue-Min-Hamade* system, drive circuit 9 ("local column read amplifier") would have included the gates of NMOS transistors Q16 and Q17 (green below) ("first and second read amplifier transistors") responsively coupled to nodes N_1 and N_2 ("said first and second latch nodes") of figure 6 of *Inoue*,

respectively, because gates of transistors Q17 and Q16 in drive circuit 9 receive the bit line signals (Ex.1009, FIG. 1, 2:60-63), and *Inoue*'s nodes N_1 and N_2 correspond to bit lines (Ex.1007, 3, 4, FIG. 6). (Ex.1002, ¶152; *supra* SectionsIX.A.4(c).)

FIG. 1



(Ex.1002, ¶152, citing Ex.1009, FIG. 1 (annotated to show transistors Q17 and Q16 ("first and second read amplifier transistors," respectively) in green.)

b) "wherein said first and second read amplifier transistors selectively couple said first and second data read signals to said first power supply."

The combined *Inoue-Min-Hamade* system discloses or suggests this feature. (Ex.1002, ¶153.) This is because based on the potentials of the bit lines (i.e., the potentials at nodes N_1 and N_2), transistors Q16 and Q17 would have selectively

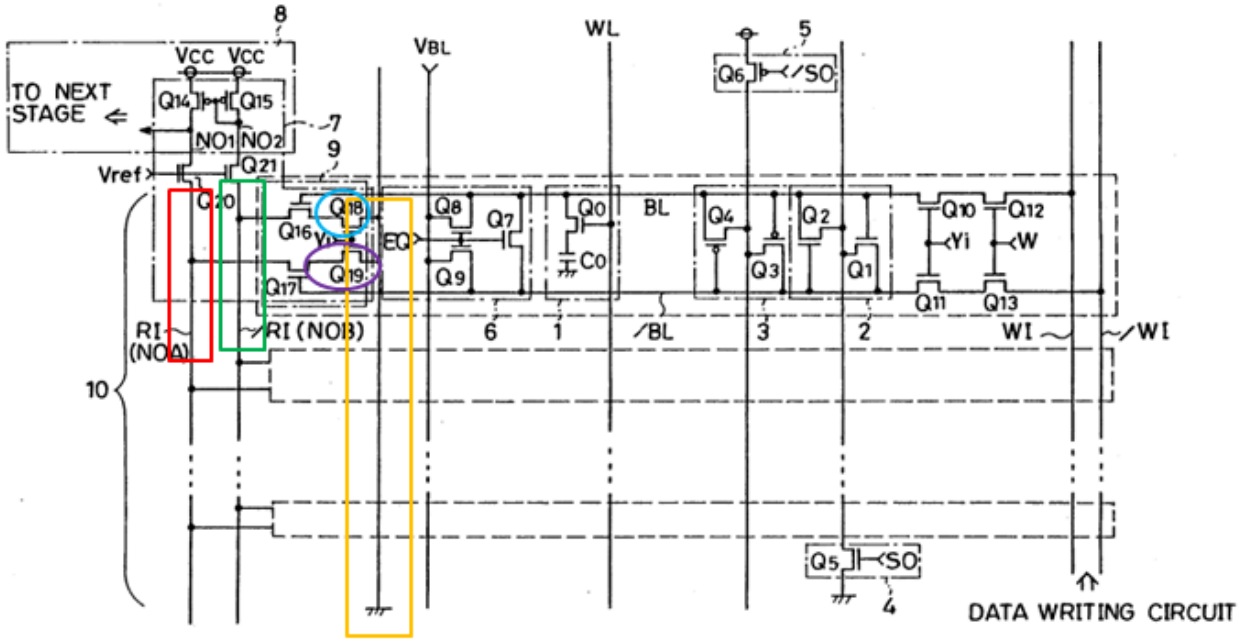
discharged RI and /RI ("first and second data read signals") to ground ("said first power supply"). (*Id.*; *supra* Sections IX.A.4(c), IX.A.5(b).)

7. Claim 33

a) "The sense amplifier arrangement of claim 32 wherein said read amplifier further includes: a third read amplifier transistor coupled between said first power supply and said first data read signal; and a fourth read amplifier transistor coupled between said first power supply and said second data read signal."

In the *Inoue-Min-Hamade* combination discussed above for limitation 30(c), the drive circuit 9 corresponding to each sense amplifier ("said read amplifier") would have further included transistor Q19 ("third read amplifier transistor") (purple below) coupled between the ground node ("said first power supply") (orange below) and read only data line RI ("said first data read signal") (red below), and transistor Q18 ("fourth read amplifier transistor") (blue below) coupled between the ground node and read only data line /RI ("said second data read signal") (green below). (*Supra* Sections IX.A.4(c); Ex.1009, FIG. 1; Ex.1002, ¶¶154-155.)

FIG. 1



(Ex.1002, ¶154, citing Ex.1009, FIG. 1 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

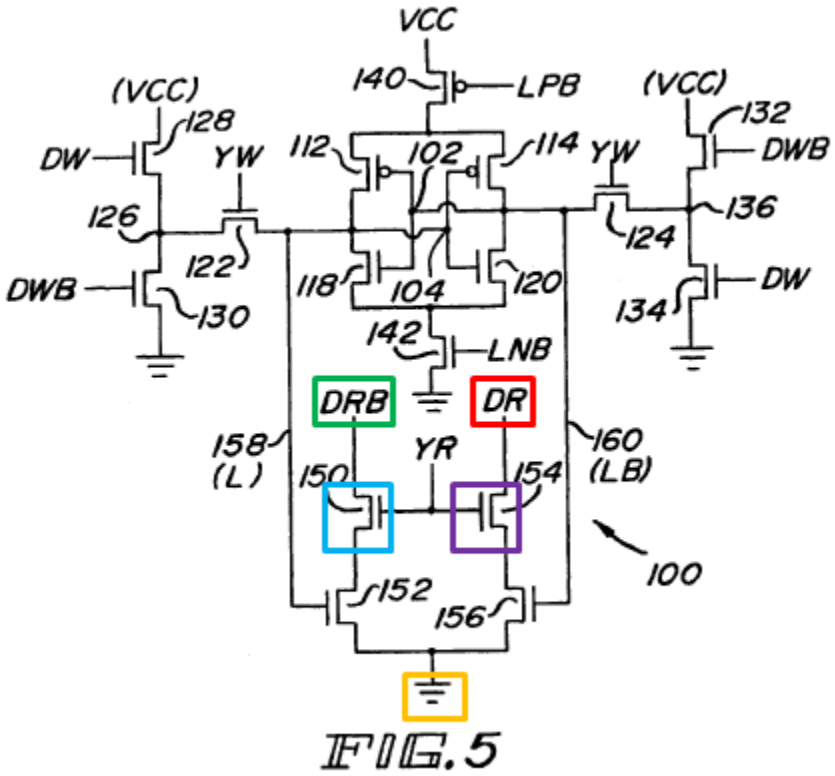


FIG. 5

(Ex.1002, ¶156, citing Ex.1001, FIG. 5 (annotated).)

8. Claim 34

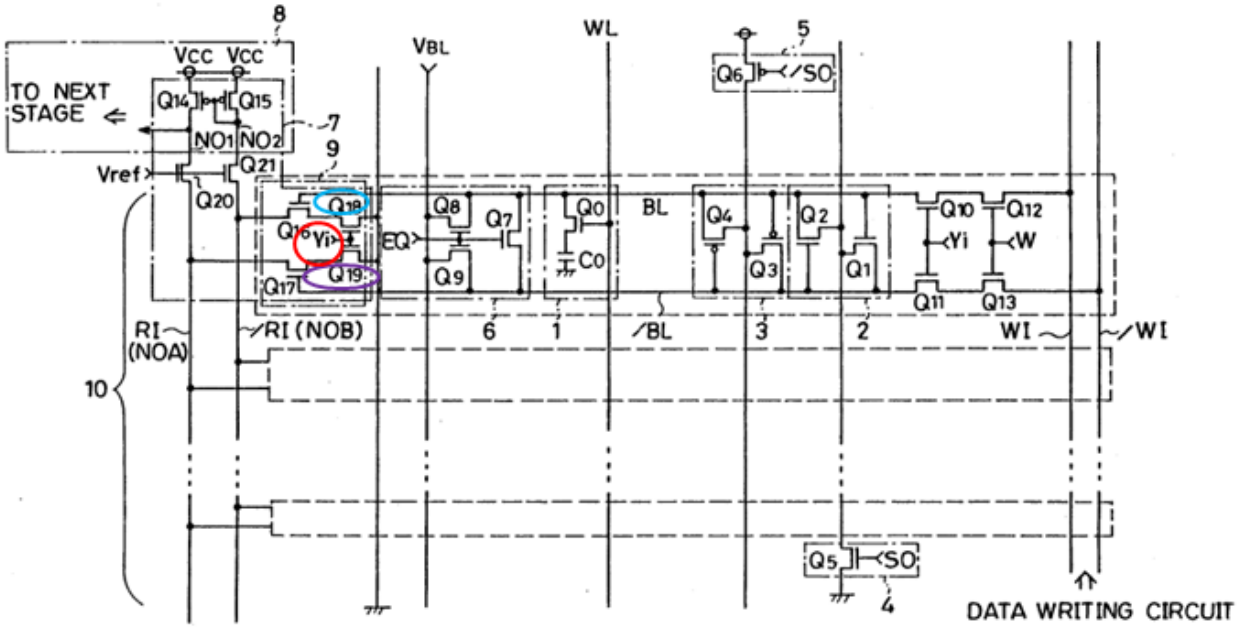
a) "The sense amplifier arrangement of claim 33 wherein said third and fourth read amplifier transistors have control electrodes coupled to receive a column read signal."

As discussed above with respect to claim limitation 30(c), a POSITA would have found it obvious to modify the combined *Inoue-Min* system to include, for each of the plurality of sense amplifiers, a drive circuit 9 and related circuitry (e.g., read only data lines RI, /RI) associated with operation of drive circuit 9 as disclosed in *Hamade*. (*Supra* Sections IX.A.1(d); IX.A.4(c); Ex.1002, ¶157.) A

POSITA would have also found it obvious to incorporate the column selecting signal Yi associated with drive circuit 9 in *Hamade* in the combined *Inoue-Min-Hamade* system. (*Supra* Section IX.A.1(d); Ex.1002, ¶157.)

Therefore, the POSITA would have provided, in the combined *Inoue-Min-Hamade* system, the column selecting signal Yi to the gates of transistors Q18 and Q19 as illustrated in figure 1 of *Hamade*. (Ex.1009, 8:24-26, FIG. 1; Ex.1002, ¶158-159.) Hence, in the *Inoue-Min-Hamade* combination discussed above for limitation 30(c), the drive circuit 9 (Ex.1009, FIG. 1) corresponding to each sense amplifier would have had transistors Q19 and Q18 ("said third and fourth read amplifier transistors") (purple and blue below, respectively) with their gate terminals ("control electrodes") coupled to receive a column selecting signal Yi ("column read signal"). (Ex.1002, ¶158.) A POSITA would have understood that *Hamade*'s column selecting signal Yi is a "column read signal" because it is used for selecting a column during a read operation. (*Id.*; Ex.1009, 8:8-26.)

FIG. 1



(Ex.1002, ¶158, citing Ex.1009, FIG. 1 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

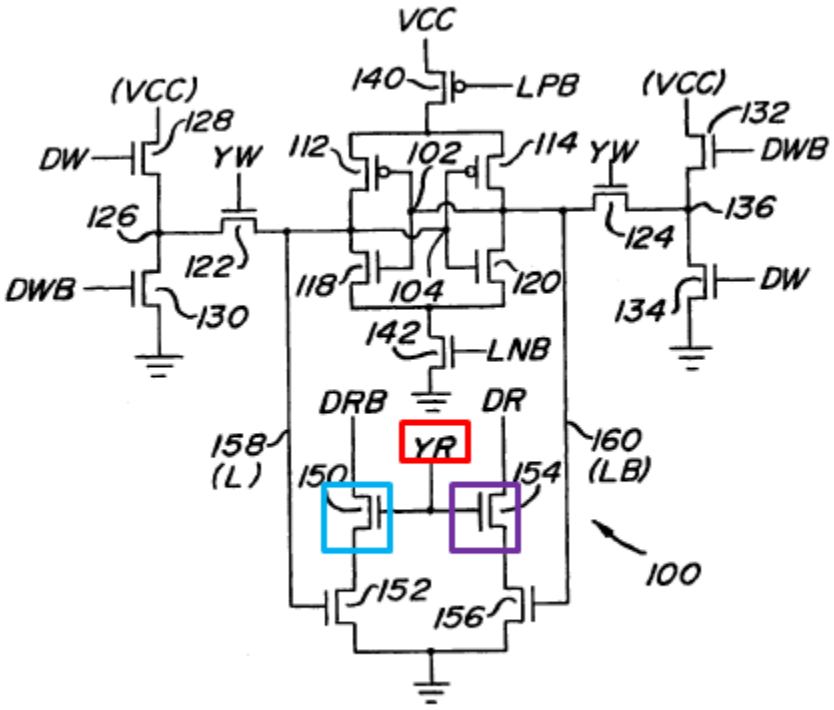


FIG. 5

(Ex.1002, ¶160, citing Ex.1001, FIG. 5 (annotated).)

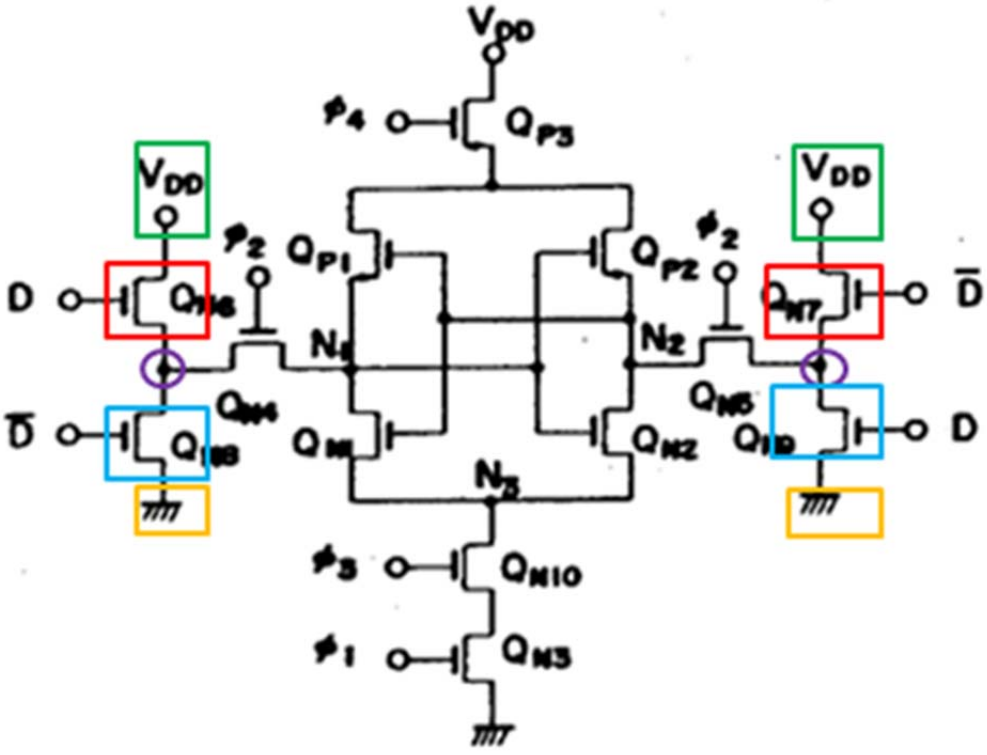
9. Claim 35

a) "The sense amplifier arrangement of claim 30 wherein each of said first and second local data write driver circuits comprises: a pull-up transistor and a pull-down transistor having source-drain paths coupled in series and forming an output node therebetween, said output node being coupled to the corresponding node of the latch circuit, said source-drain paths being coupled between first and second voltages."

As discussed above, in the combined *Inoue-Min-Hamade* system, transistor pairs Q_{N6} and Q_{N8}, and Q_{N7} and Q_{N9} from *Inoue* figure 6 each constitute a "local data write driver circuit." (*Supra* Section IX.A.4(d); Ex.1002, ¶¶44-47, 161.) These "local data write driver circuits" include a transistor Q_{N6} or Q_{N7} ("pull-up

transistor") (shown in red below), and a transistor Q_{N8} or Q_{N9} ("pull-down transistor") (shown in blue below) having source-drain paths coupled in series and forming an output node (shown in purple below) therebetween, wherein the output node is coupled to the node N_1 or N_2 ("the corresponding node") of the flip-flop ("latch circuit"), and the source-drain paths of the pull-up and pull-down transistors are coupled between V_{DD} and ground ("first and second voltages"; shown below in green and orange, respectively). (Ex.1007, 3, FIG. 6; Ex.1002, ¶¶161-162.)

第 6 図



(Ex.1002, ¶161.)

Moreover, when clock ϕ_2 rises, Q_{N4} and Q_{N5} become conducting. (Ex.1007, 3.) As a result, "the current flows from V_{DD} to the node N_1 through Q_{N6} and Q_{N4}, while the current flows out from N_2 to GND through Q_{N5} and Q_{N9}" thereby charging node N_1 to a level "H" (V_{DD}) and discharging node N_2 to "L" (GND). (*Id.*, 3.) Therefore, the output (V_{DD}) of Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} (GND) is provided to nodes N_1 and N_2. (Ex.1007, 3, FIG. 6; Ex.1002, ¶163.) Therefore, the combined *Inoue-Min-Hamade* system discloses "said output node being coupled to the corresponding node of the latch circuit," as claimed. (Ex.1002, ¶163.)

The '574 patent discloses a similar configuration, as shown below.

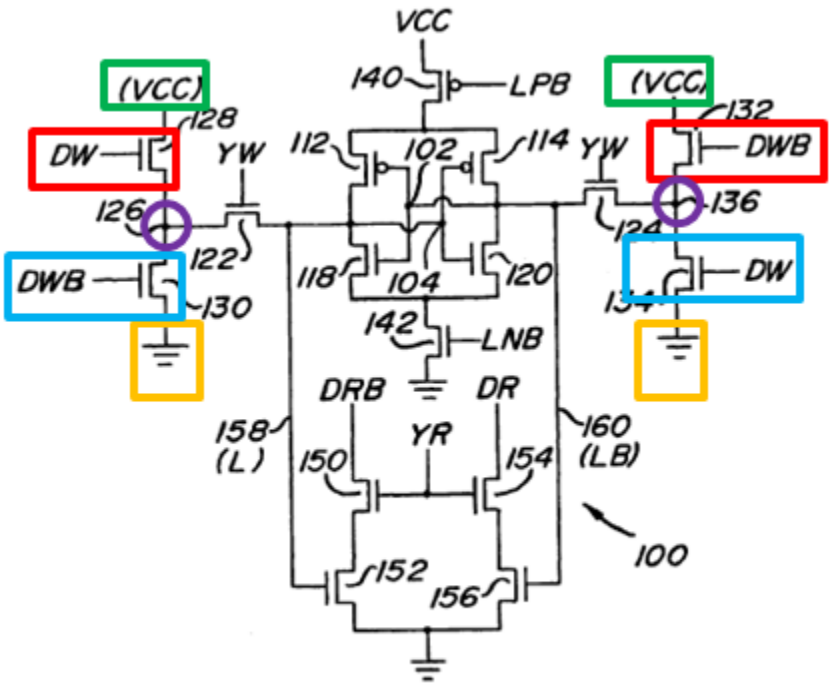


FIG. 5

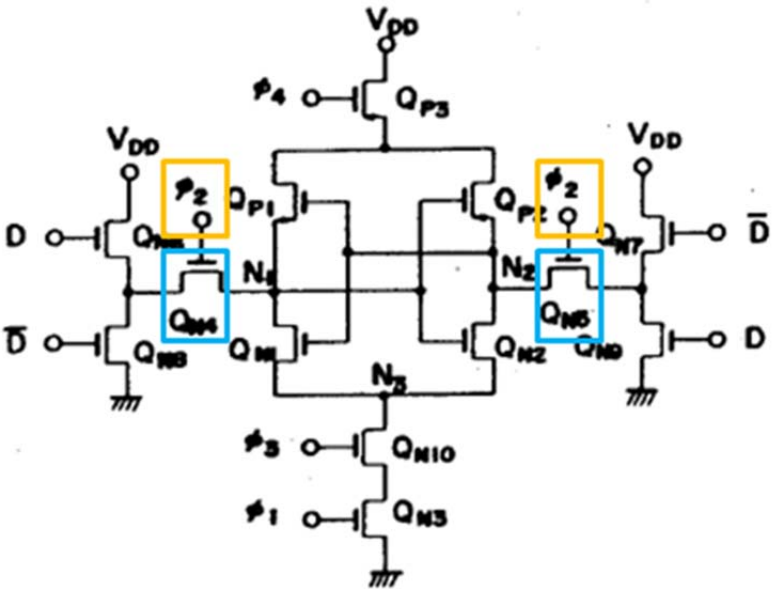
(Ex.1002, ¶164, citing Ex.1001, FIG. 5 (annotated).)

10. Claim 36

a) "The sense amplifier arrangement of claim 35 further comprising: first and second pass transistors responsively coupled to a write control signal;"

As discussed above, in the combined *Inoue-Min-Hamade* system discussed above, the circuit of figure 6 in *Inoue* is replicated for each column. (*Supra* Section IX.A.4(c).) The circuit of figure 6 has transistors Q_{N4} and Q_{N5} ("first and second pass transistors") (blue below) coupled at their gates ("responsively coupled") to write control clock ϕ_2 (Ex.1007, 4) ("a write control signal") (orange below). (*Supra* Sections IX.A.3(a); Ex.1007, 3-4; FIG. 6; Ex.1002, ¶165.)

第 6 図



(Ex.1002, ¶165, citing Ex.1007, FIG. 6 (annotated).)

The '574 patent discloses a similar configuration, as shown below.

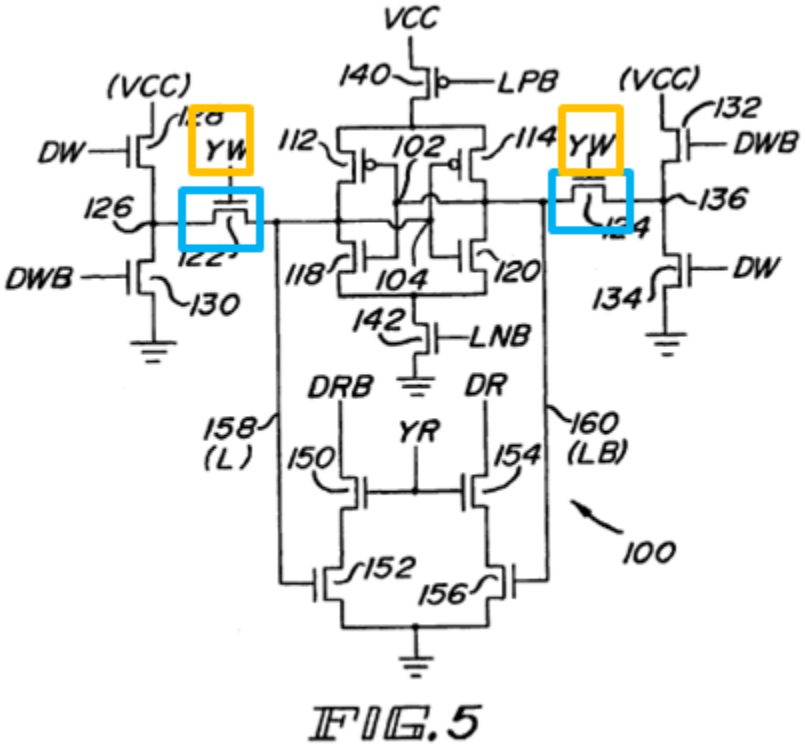


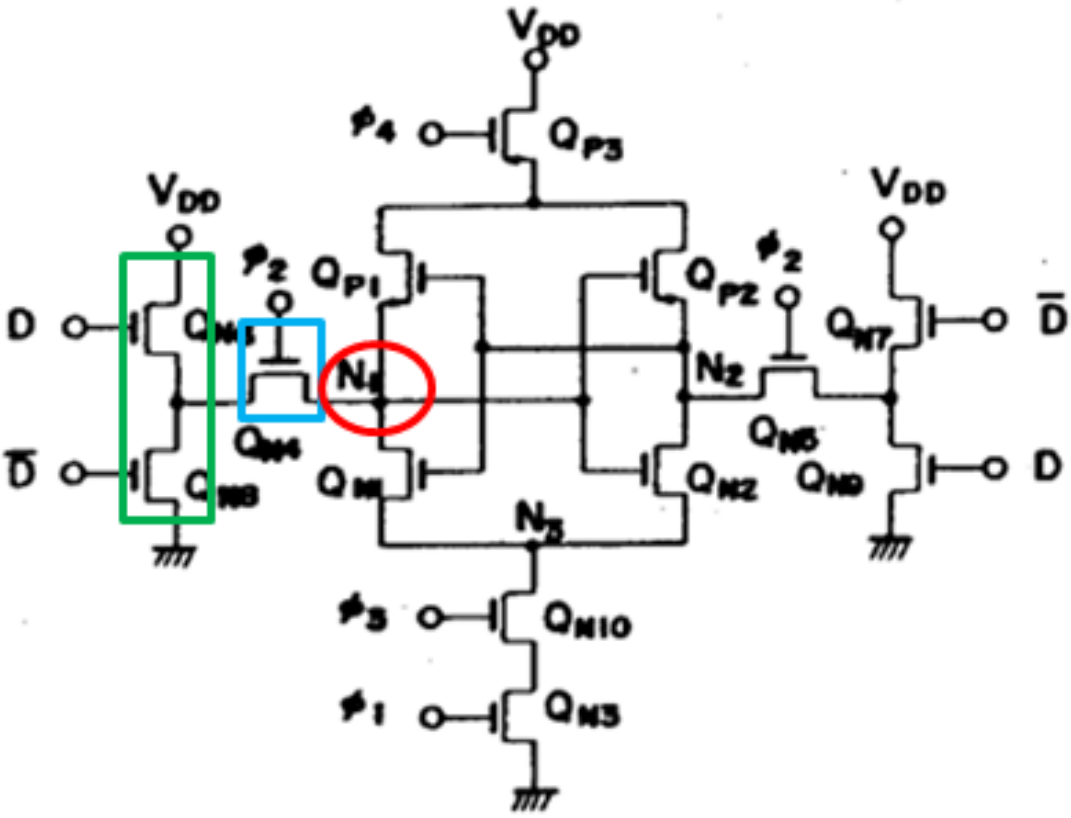
FIG. 5

(Ex.1002, ¶166, citing Ex.1001, FIG. 5 (annotated).)

b) "said first pass transistor selectively coupling said first local data write driver circuit to said first latch node;"

In *Inoue*'s figure 6, transistor Q_{N4} ("said first pass transistor") (blue below) selectively couples Q_{N6} and Q_{N8} ("said first local data write driver circuit") (green below) to node N_1 ("said first latch node") (red below). (*Supra* Section IX.A.3(a); Ex.1007, 3, FIG. 6; Ex.1002, ¶167.)

第 6 図



(Ex.1002, ¶167, citing Ex.1007, FIG. 6 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

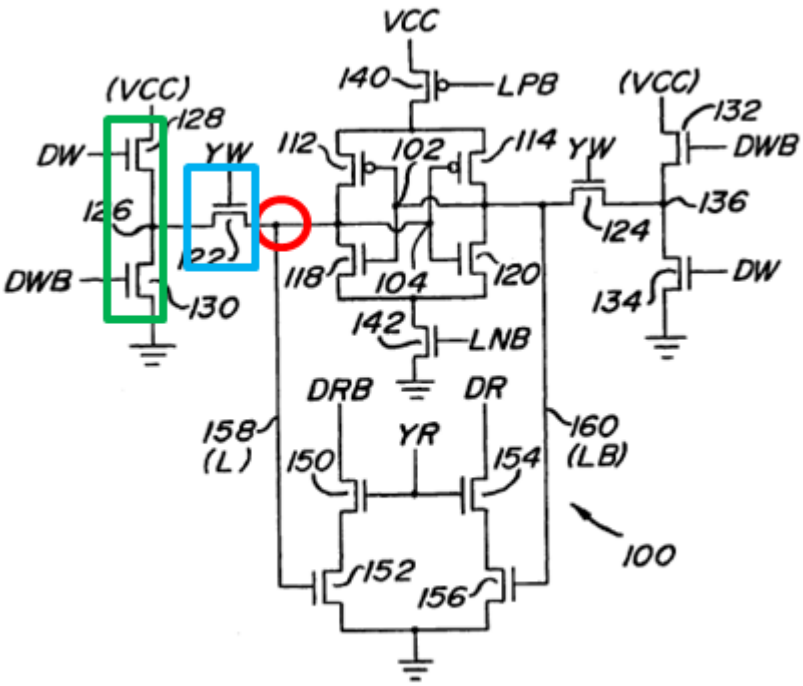


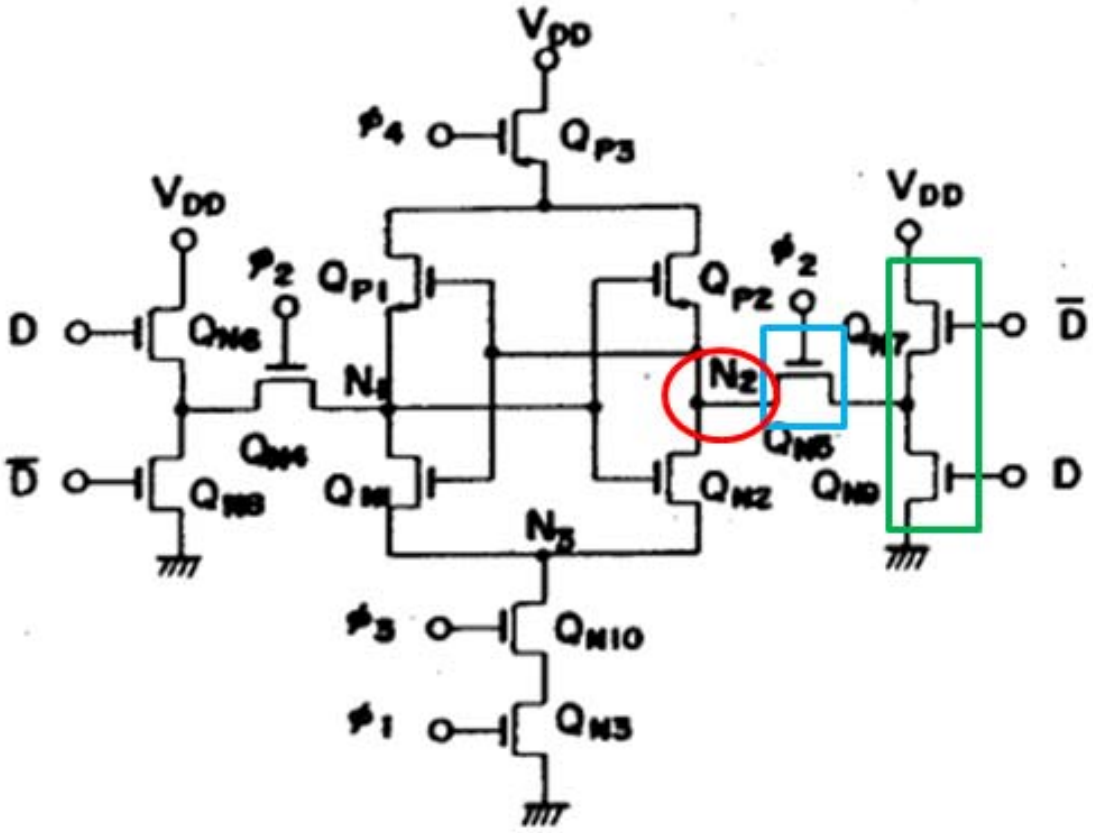
FIG. 5

(Ex.1002, ¶168, citing Ex.1001, FIG. 5 (annotated).)

c) "said second pass transistor selectively coupling said second local data write driver circuit to said second latch node."

In *Inoue*'s figure 6, transistor Q_{N5} ("said second pass transistor") (blue below) selectively couples Q_{N7} and Q_{N9} ("said second local data write driver circuit") (green below) to node N_2 ("said second latch node") (red below). (*Supra* Section IX.A.3(a); Ex.1007, 3, FIG. 6; Ex.1002, ¶169.)

第 6 図



(Ex.1002, ¶169, citing Ex.1007, FIG. 6 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

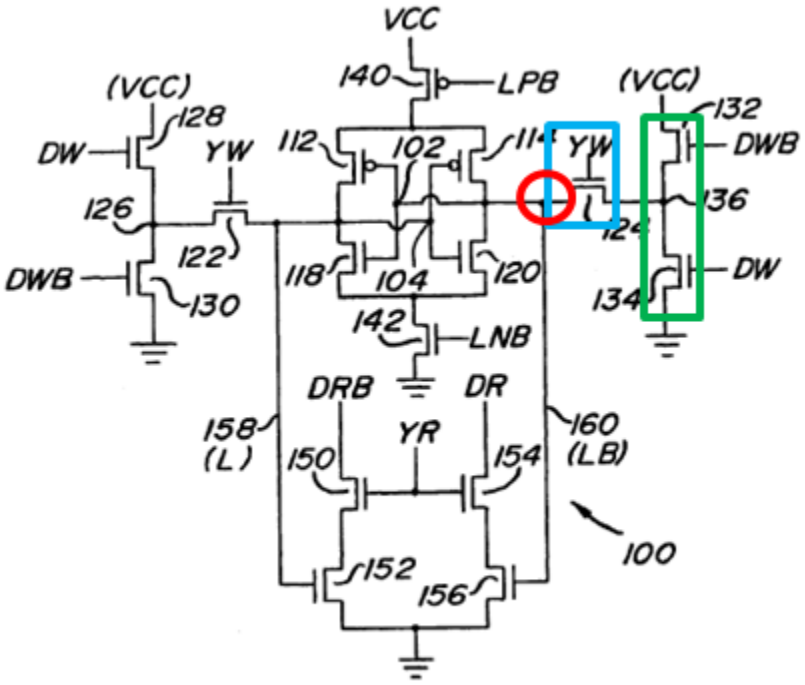


FIG. 5

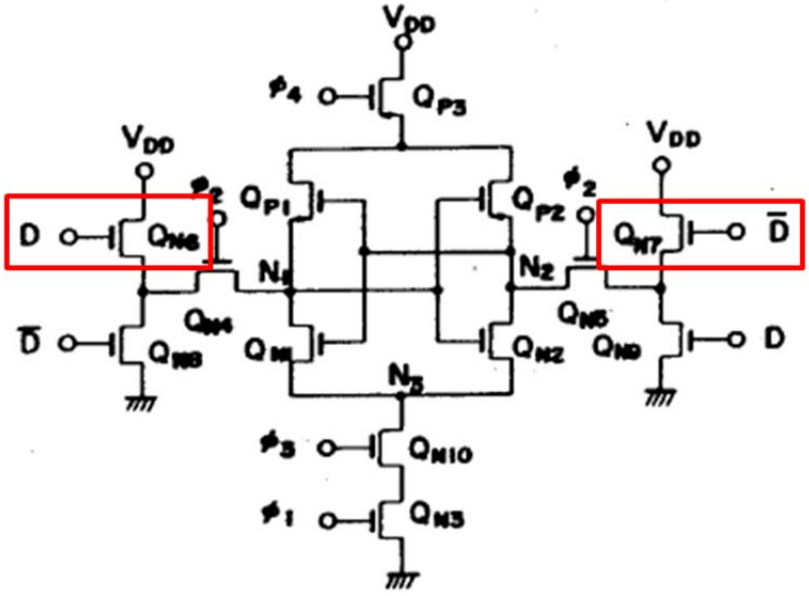
(Ex.1002, ¶170, citing Ex.1001, FIG. 5 (annotated).)

11. Claim 37

a) "The sense amplifier arrangement of claim 36 wherein said pull-up transistors in said write driver circuits further include respective control electrodes coupled to receive respective data write signals, and"

In *Inoue*'s figure 6, the pull-up transistors Q_{N6} and Q_{N7} ("said pull-up transistors in said write driver circuits") include respective gate terminals ("control electrodes") coupled to receive signals at respective write data input terminals D and $\overline{D}$ ("data write signals"). (*Supra* Section IX.A.1(o); Ex.1007, 3, FIG. 6; Ex.1002 ,¶¶171-172.)

第 6 図



(Ex.1002, ¶171, citing Ex.1007, FIG. 6 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

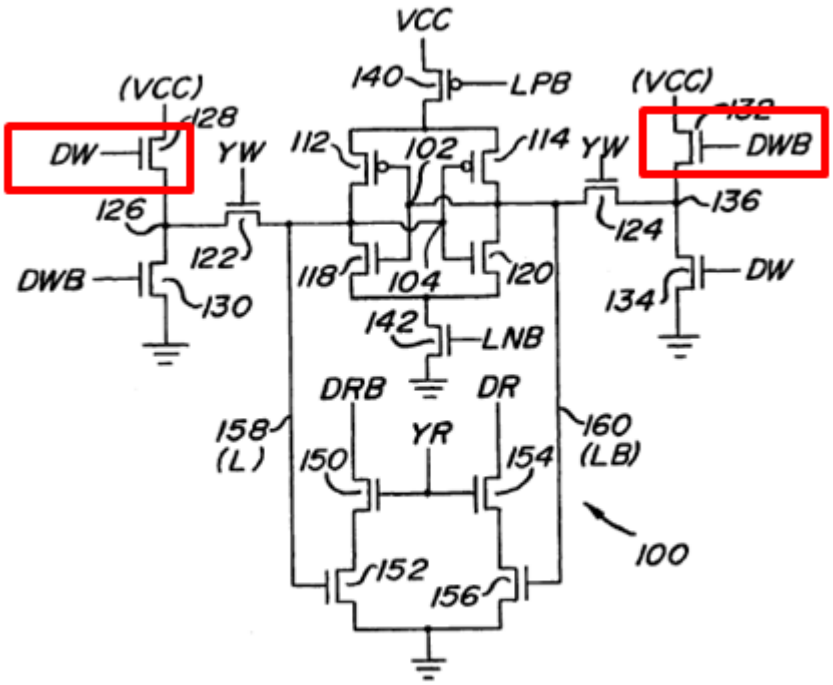


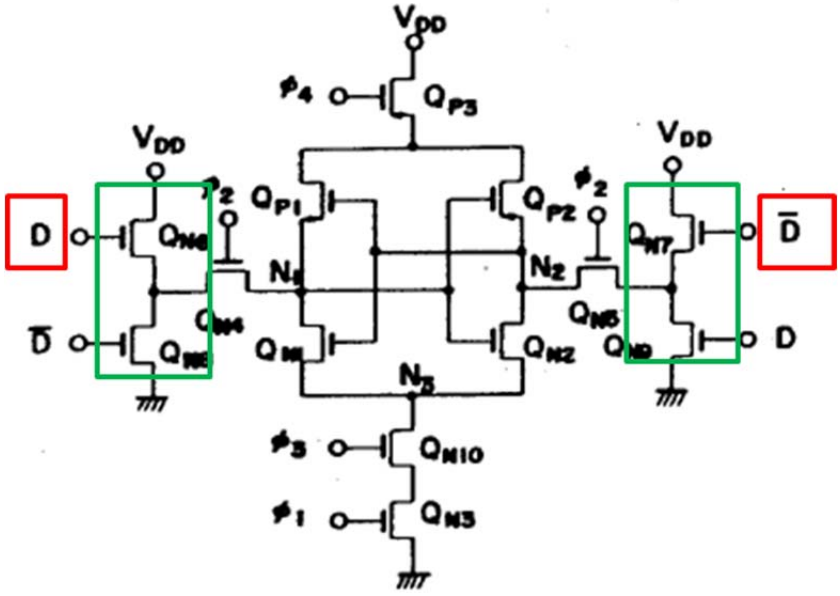
FIG. 5

(Ex.1002, ¶173, citing Ex.1001, FIG. 5 (annotated).)

b) "wherein said source-drain paths are coupled to receive said data write signals."

In *Inoue*'s figure 6, the source-drain paths formed by transistors Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} (green below) are coupled to receive the data write signals D and $\overline{D}$ ("said data write signals") (red below). (Ex.1007, 3, FIG. 6; *supra* Sections IX.A.9,IX.A.11(a); Ex.1002, ¶174.)

第 6 図



(Ex.1002, ¶174, citing Ex.1007, FIG. 6 (annotated).)

The ’574 patent discloses a similar configuration, as shown below.

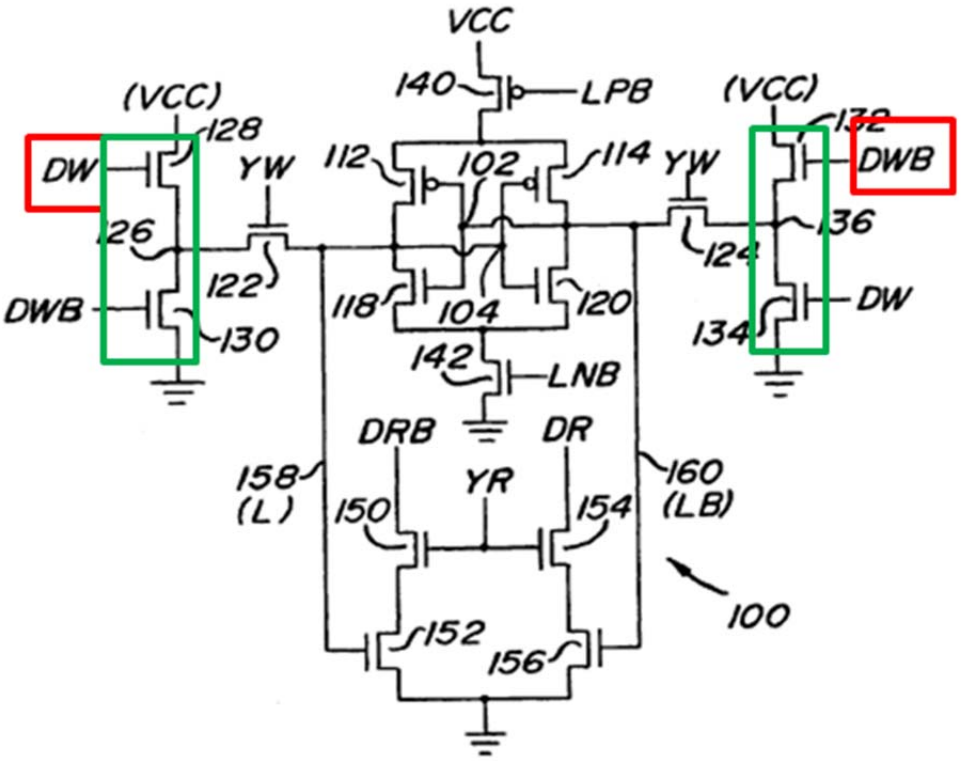


FIG. 5

(Ex.1002, ¶175, citing Ex.1001, FIG. 5 (annotated).)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-3 and 30-37 of the '574 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: May 12, 2017

By: /Naveen Modi/
Naveen Modi (Reg. No. 46224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,208,574 contains, as measured by the word-processing system used to prepare this paper, 13,931 words. This word count does not include the items excluded by 37 C.F.R. § 42.24(a).

Respectfully submitted,

Dated: May 12, 2017

By: /Naveen Modi/
Naveen Modi (Reg. No. 46224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on May 12, 2017, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,208,574 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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