Paper No. __
Filed: May 12, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC
Patent Owner

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U.S. Patent No. 6,069,507

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**PETITION FOR *INTER PARTES* REVIEW**
**OF U.S. PATENT NO. 6,069,507**

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## I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 10, 11, 13, and 15 of U.S. Patent No. 6,069,507 ("the '507 patent") (Ex. 1001), which, according to PTO records, is assigned to ProMOS Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

## II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

**Real Parties-in-Interest**: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

**Related Matters**: Patent Owner has asserted the '507 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al*., No. 1:16-cv-00335-SLR (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 6,172,554 ("the '554 patent"), 7,375,027 ("the '027 patent"), 6,208,574 ("the '574 patent"), 6,559,044 ("the '044 patent"), and 6,562,714 ("the '714 patent") in this action. Petitioner is concurrently filing another IPR petition challenging claims 10, 11, 13, and 15 of the '507 patent as well as additional IPR petitions challenging certain claims of the '554, '027, '574, '044, and '714 patents. Petitioner also previously filed several IPR petitions involving additional patents asserted by Patent Owner in *ProMOS Technologies, Inc. v. Samsung Electronics*

*Co., Ltd. et al.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Specifically, on October 7, 2016, Petitioner filed IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. All of these proceedings were instituted and remain pending except for the 00033 and 00035 proceedings.

**Counsel and Service Information**: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

## III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

## IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the ’507 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

## V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

### A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 10, 11, 13, and 15 ("challenged claims") of the '507 patent, and cancellation of these claims as unpatentable.

### B. Statutory Ground of Challenge

The challenged claims should be canceled as unpatentable in view of the following ground:

**Ground 1**: Claims 10, 11, 13, and 15 are unpatentable under pre-AIA 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,875,219 ("*Kim*") (Ex. 1009).

The '507 patent issued from U.S. Application No. 09/083,790 ("the '790 application") filed May 22, 1998. (Ex. 1001, Cover). The '790 application does not claim priority to any earlier filed applications.

*Kim* issued on February 23, 1999 from U.S. Patent Application No. 778,354 filed January 2, 1997. Thus, *Kim* qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(e) with respect to the '507 patent.

*Kim* was not considered by the Patent Office during prosecution of the '507 patent. (*See generally* Ex. 1001, References Cited.)

## VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '507 patent ("POSITA"), which for purposes of this proceeding is the mid-to-late 1990s (including May 22, 1998, the filing date of the U.S. Application maturing into the '507 patent), would have had at least a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design. (Ex. 1002, ¶¶18-19.)[1] More education can supplement practical experience and vice versa. (*Id.*)

## VII. OVERVIEW OF THE TECHNOLOGY, '507 PATENT, AND PRIOR ART

### A. The '507 Patent

The '507 patent issued from U.S. Application No. 09/083,790 filed on May 22, 1998 and is entitled "Circuit and Method for Reducing Delay Line Length in Delay-Locked Loops." (Ex. 1001, Cover.) The '507 patent relates to "delay-locked loops (DLLs) and more particularly to reducing delay line length in DLLs." (*Id.*, 1:7-9.)

The '507 patent acknowledges that delay locked loops (DLLs) were known as a way to provide "clock deskew functionality," i.e., to address the problem of

[1] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '507 patent. (Ex. 1002, ¶¶1-13; Ex. 1003.)

clock skew. (*Id.*, 1:12-13; Ex. 1002, ¶39; *see also* Ex. 1002, ¶¶25-33, 38.) The '507 patent describes "a typical digital DLL" with respect to figure 1, which is labeled "PRIOR ART."

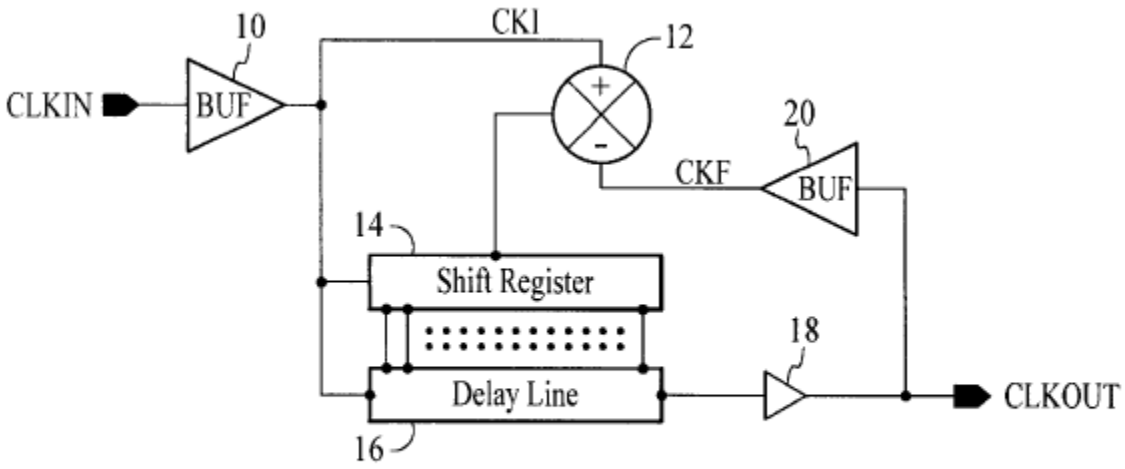



FIG. 1
(PRIOR ART)

(Ex. 1001, FIG. 1; *see also id.*, 1:20-33; Ex. 1002, ¶¶39-40.)

The '507 patent states that "a need exists for more elegant and cost effective solutions to reducing delay line length in DLLs." (Ex. 1001, 1:54-55.) "FIG. 2 illustrates a digital DLL 24 in accordance with the present invention." (*Id.*, 2:49-50.)

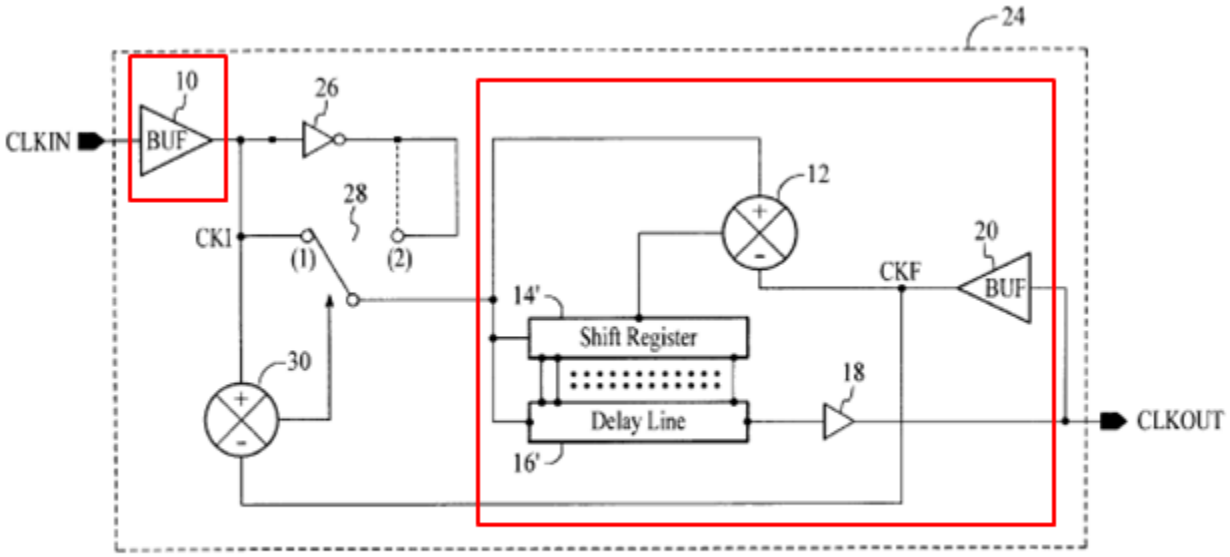



FIG. 2

(Ex. 1002, ¶41, citing Ex. 1001, FIG. 2 (annotated in red to show components found in the prior art DLL of figure 1 of the ’507 patent).)

The ’507 patent states with reference to figure 2 that “[l]ike components to those shown in FIG. 1 have been numbered similarly,” and a comparison of figures 1 and 2 shows that the entire right side of figure 2 and the buffer (BUF) 10 (both annotated above in red) are found in the prior art DLL of figure 1. (Ex. 1001, 2:50-51; Ex. 1002, ¶¶42-43.) As stated by the ’507 patent, these components of figure 2 and their functionality were “well understood by those skilled in the art.” (Ex. 1001, 1:29-33.) The ’507 patent discloses that “the DLL 24 [of figure 2] further includes an inverter 26, a switch 28, and a second phase detector 30” and that “[t]hrough the arrangement of the DLL 24, the length of the delay line 16' and

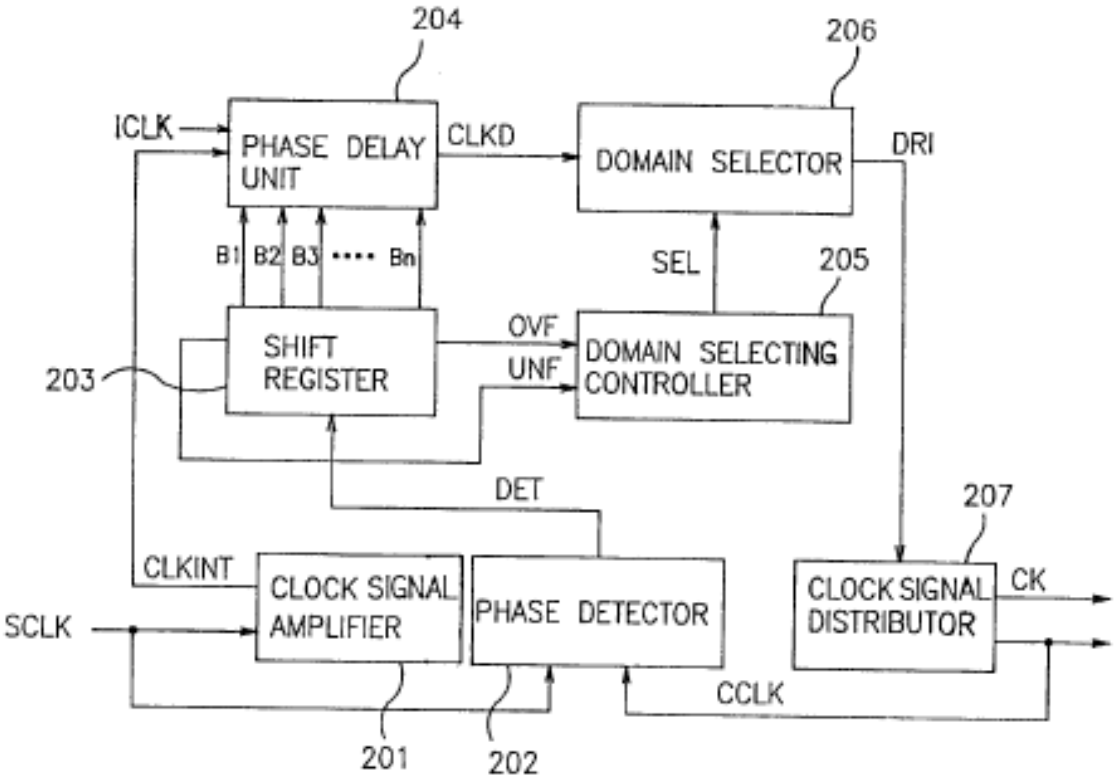
correspondingly the number of cells in the shift register 14' are reduced." (*Id.*, 2:55-60.)

The above features were well known as discussed below at Sections VII.B and IX. (Ex. 1002, ¶¶44, 46-108.)

**B. *Kim***

*Kim* relates to a "digital delay locked loop (DLL)." (Ex. 1009, Abstract.) *Kim* discloses operation of the digital DLL in connection with figure 3. (*Id.*, FIG. 3; Ex. 1002, ¶46.)

FIG. 3



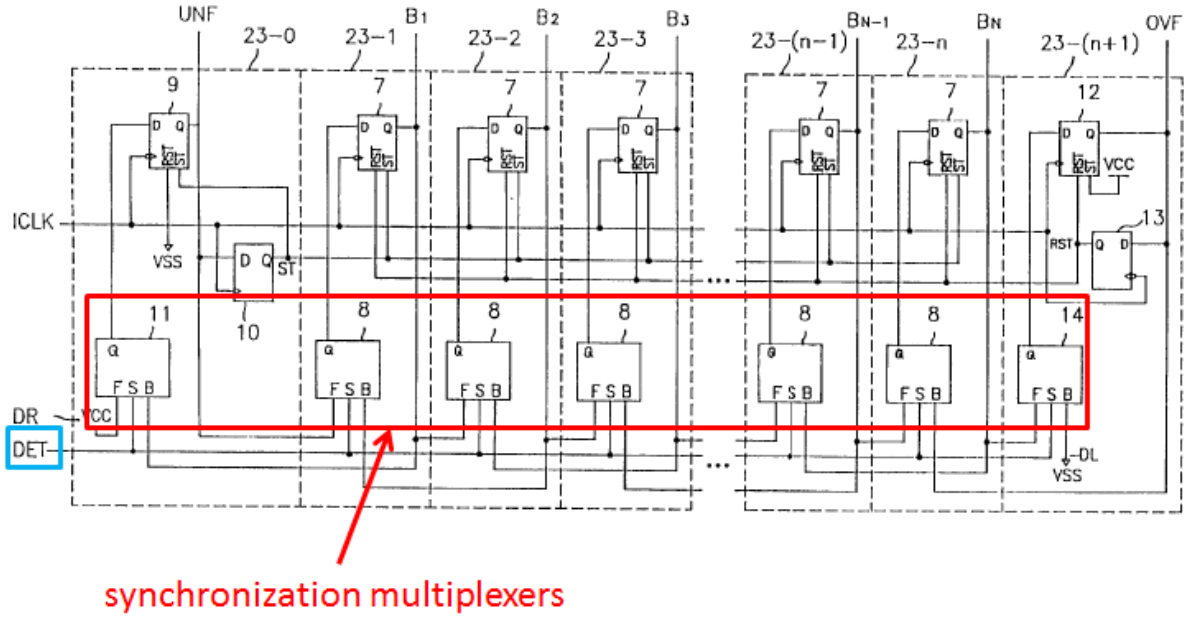

(Ex. 1009, FIG. 3.)

*Kim* discloses a technique that reduces resource requirements for phase delay unit 204 shown above. (*See id.*, 10:4-8 ("[T]he number of the delaying elements of the present invention can be reduced to half, since the phase shift is performed only in the first domain and the phase shift in the second domain is performed inverse to the phase shift in the first domain."); Ex. 1002, ¶47.) In particular, when performing the phase adjustment in the delay locked loop shown above, *Kim* discloses performing a phase shift only in a first domain, which comprises "0°~180°," and performing a phase shift in a second domain, which comprises "180°~360°," inverse to the phase shift in the first domain, where selective inversion of the output of a single phase delay unit is used to produce the signals for both domains and thereby reduce the number of delaying elements required. (Ex. 1009, 7:32-35, 7:19-30, 9:64—10:8.)

*Kim*'s phase detector 202 (shown above in figure 3) compares the chip clock (CCLK) with the system clock (SCLK) and outputs signal DET as either '1' or '0' based on whether CCLK leads or lags SCLK. (*Id.*, 5:14-19 ("the phase detector 202 outputs a comparing signal '1' to shift register 203 when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase, or outputs a '0' to the shift register 203 when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase"); Ex. 1002, ¶48.) The output DET is provided to the select input of each of the synchronization multiplexers (labeled with reference numerals 8, 11,

and 14) within the shift register 203 shown in figure 4 of *Kim*, where the synchronization multiplexers select whether the shift register shifts forward or backward based on the DET signal. (Ex. 1009, 5:20-22, 5:24-26; Ex. 1002, ¶48.)

FIG. 4




(Ex. 1002, ¶48, citing Ex. 1009, FIG. 4 (annotated).)

The shift register 203 provides the bit values B1-Bn to the phase delay unit 204 as depicted in figure 3, where the phase delay unit 204 outputs "a phase-adjusted clock signal (CKLD) by delaying the output of the clock signal amplifier 201 in accordance with the bit values of the shift register 203." (Ex. 1009, 3:29-33; Ex. 1002, ¶49.) As such, the delay through the phase delay unit 204, and hence the digital delay locked loop shown in figure 3, is adjusted based on the bit values provided by the shift register 203.

## VIII. CLAIM CONSTRUCTION

Should the Board institute *inter partes* review, the '507 will expire on May 22, 2018, *i.e.*, during the pendency of the instituted proceeding. Accordingly, the claims of the '507 patent should be construed under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). *See, e.g.*, *Square Inc. v. J. Carl Cooper*, IPR2014-00156, Paper No. 38 at 7 (May 14, 2015) (citing *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)). Under *Phillips*, claim terms are given their ordinary and customary meanings, as would be understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *See, e.g., Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 20 at 2-3 (July 10, 2014).

The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2014-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner submits that for purposes of this proceeding, the terms of the challenged claims should be given their ordinary and customary meaning consistent with *Phillips*.[2] (Ex. 1002, ¶45.)

## IX. DETAILED EXPLANATION OF GROUND

### A. Ground 1: *Kim* Anticipates Claims 10, 11, 13, and 15

#### 1. Claim 10

a) A method for reducing delay line length in a digital delay locked loop (DLL), the method comprising:

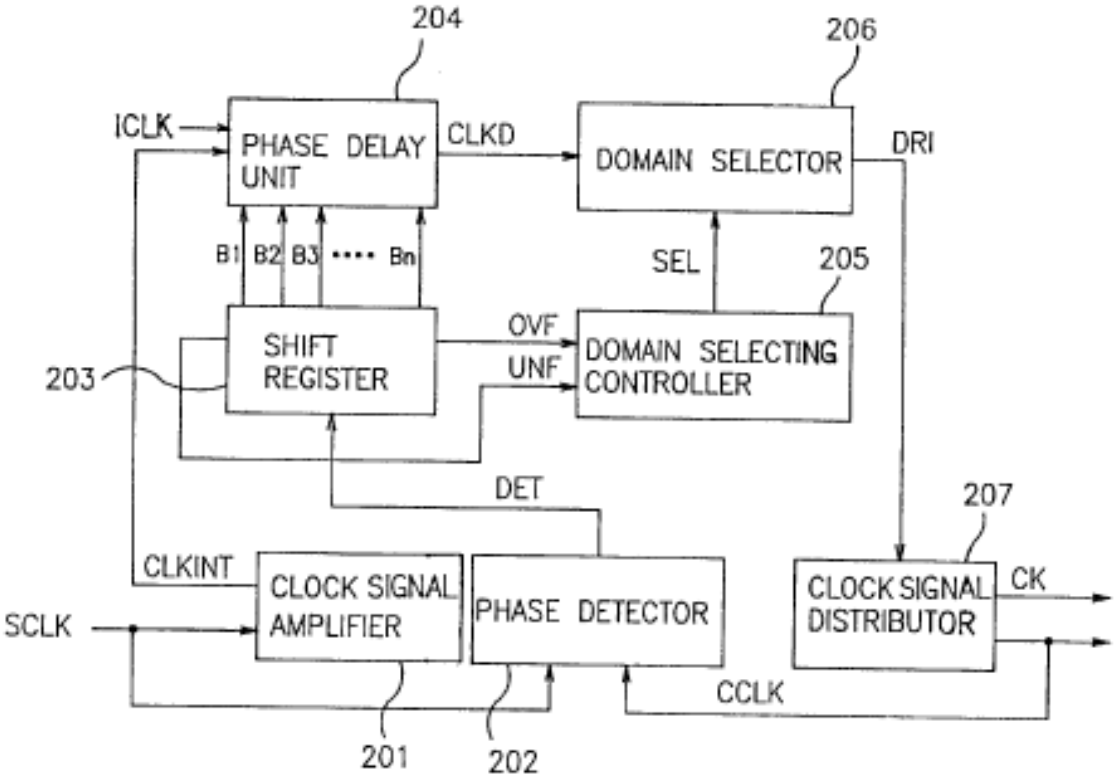
To the extent the preamble is limiting, *Kim* discloses this feature. (Ex. 1002, ¶¶51-56.) For example, *Kim* discloses a "digital delay locked loop (DLL) includes a phase detector for outputting a comparing signal by comparing a system clock signal with a chip clock signal." (Ex. 1009, Abstract, 2:46-63; Ex. 1002, ¶52.)

*Kim*'s digital phase delay locked loop, which includes all of the features listed above, is shown in figure 3 below. (Ex. 1002, ¶53.) *Kim* discloses operation of the digital DLL in connection with the block diagram of figure 3, and thus discloses a "method" as recited in claim 10. (Ex. 1009, FIG. 3.) In particular, *Kim* discloses performing a phase shift only in a first domain, which comprises "0°~180°," and performing a phase shift in a second domain, which comprises

[2] Petitioner does not concede that the challenged claims are not invalid under one or more sections of 35 U.S.C. § 112, which is something that cannot be pursued in this proceeding under the Rules.

"180°~360°," inverse to the phase shift in the first domain, where selective inversion of the output of a single phase delay unit is used to produce the signals for both domains and thereby reduce the number of delaying elements required. (*Id.*, 7:32-35, 7:19-30, 9:64—10:8; Ex. 1002, ¶53.) Accordingly, *Kim* discloses a "method" for reducing delay line length. (Ex. 1002, ¶53; *see also* Ex. 1009, 1:6-11 ("digital phase delay locked loop (DLL) . . . with a minimum number of delay units by applying a domain classifying concept.").)

FIG. 3

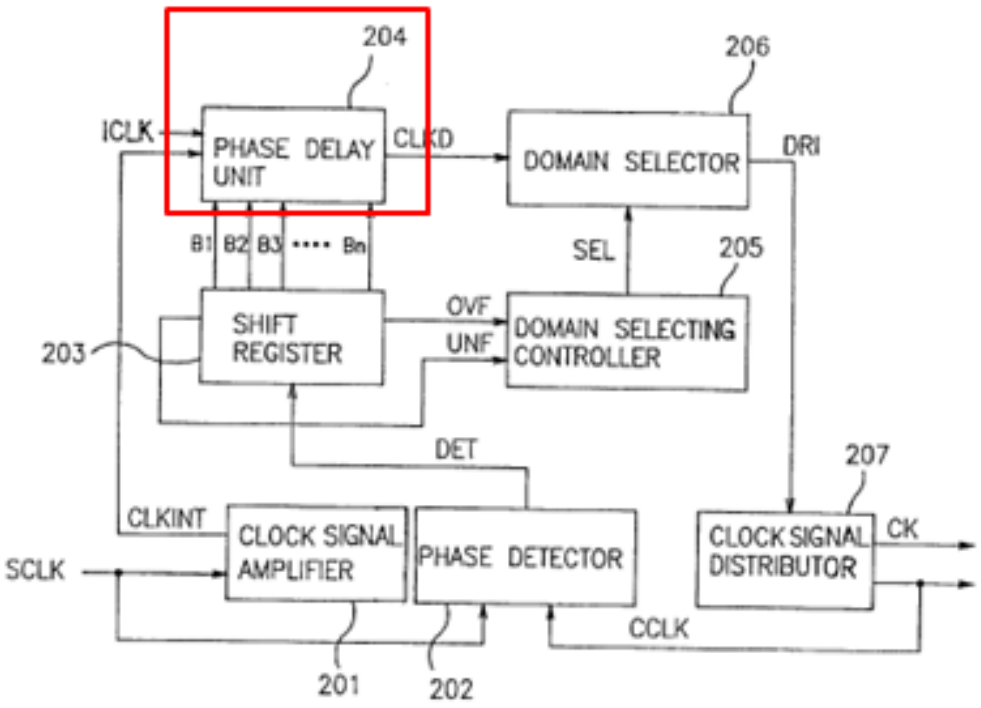



(Ex. 1009, FIG. 3.)

*Kim* discloses a "method for reducing delay line length [in a digital delay locked loop (DLL)]." (Ex. 1002, ¶54.) For instance, *Kim* discloses a method of operating the digital phase delay locked loop of figure 3 that reduces the number of delay elements in the phase delay unit 204 ("method for reducing delay line length"). (*Id.*) In particular, *Kim* discloses that "the present invention has the effect that a phase shift apparatus having a more precise resolution can be embodied, **by reducing the number of the elements comprising the delay units.**" (Ex. 1009, 10:9-12 (emphasis added).) "**[T]he number of the delaying elements of the present invention can be reduced to half**, since the phase shift is performed only in the first domain and the phase shift in the second domain is performed inverse to the phase shift in the first domain." (*Id.*, 10:4-8 (emphasis added).)

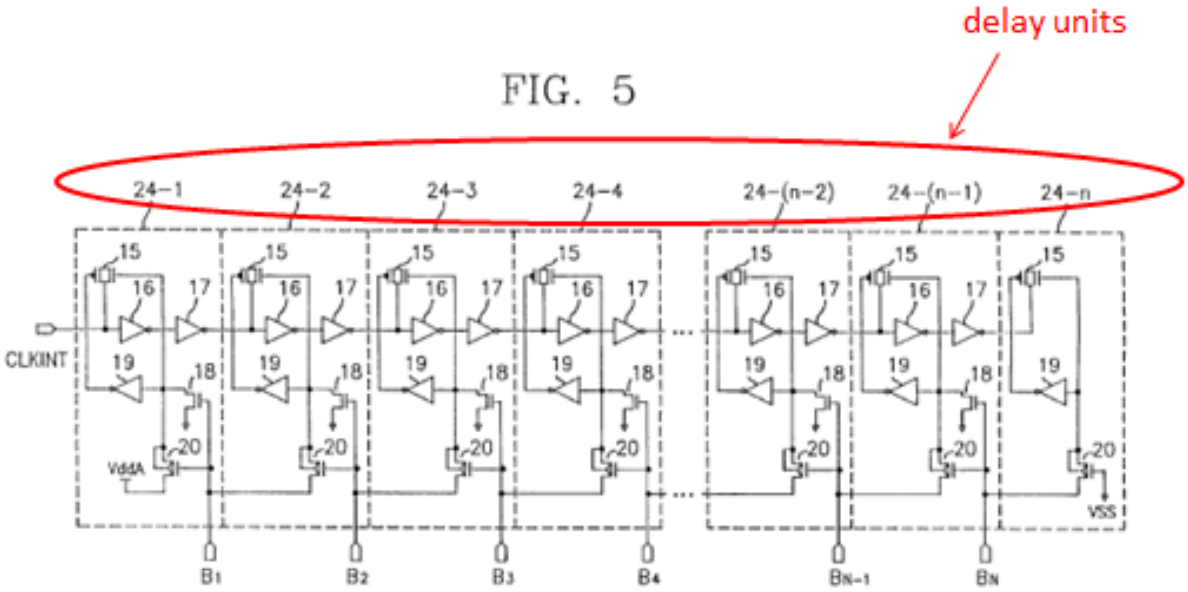
A person of ordinary skill in the art would have understood that *Kim*'s disclosure of "reducing the number of the elements comprising the delay units" constitutes "reducing delay line length" as recited in the preamble of claim 13. (Ex. 1002, ¶55, citing Ex. 1009, 10:11-12.) For example, *Kim*'s phase delay unit of figure 3 (annotated below) is shown in detail in figure 5 (also annotated below). (Ex. 1009, 3:8-9, 4:40-59.)

FIG. 3




(Ex. 1002, ¶55, citing Ex. 1009, FIG. 3 (annotated to show phase delay unit 204).)

FIG. 5



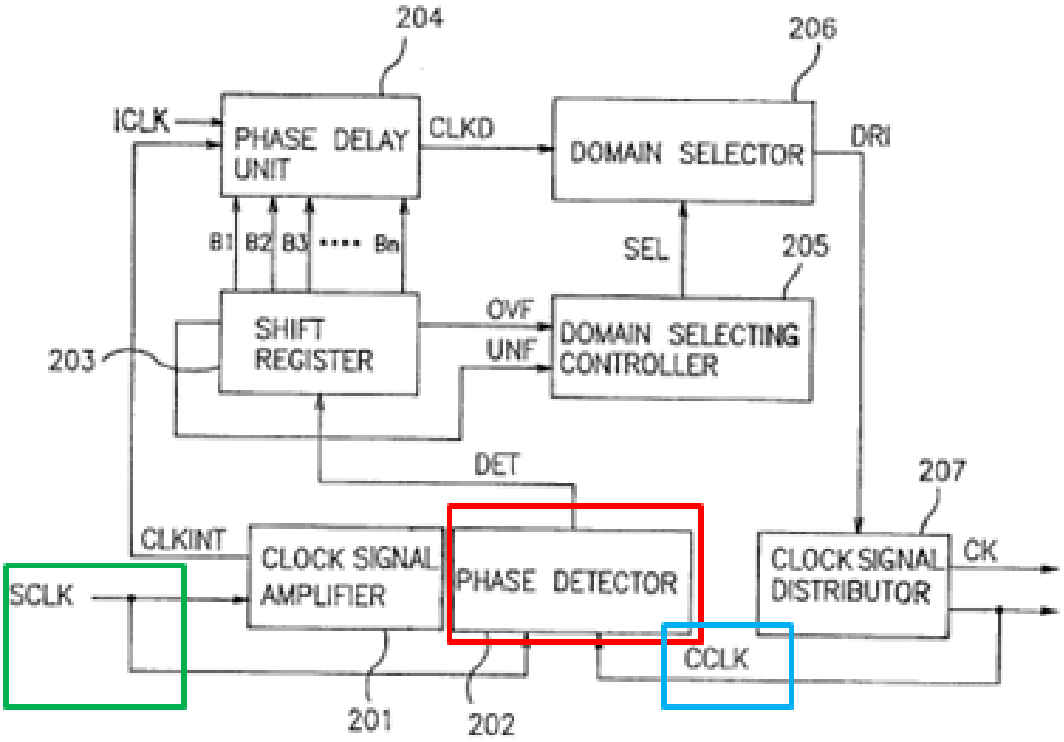
(Ex. 1002, ¶55, citing Ex. 1009, FIG. 5 (annotated to show delay units 24 constituting a delay line).)

*Kim* discloses that the phase delay unit 204 of figure 3 "includes a plurality of delay units 24-1,24-2, . . . ,24-(n-1) , 24-n outputting the phase-adjusted clock signal (CKLD) by sequentially delaying the clock signal (CLKINT) outputted from the clock signal amplifier 201." (Ex. 1009, 4:40-46 (sic).) Because the delay units 24-1,…,24-n sequentially delay a clock signal, they constitute a delay line. (Ex. 1002, ¶56.) Accordingly, because *Kim* discloses "reducing the number of the elements comprising the delay units," that reduction constitutes "reducing delay line length" as recited in the preamble of claim 10. (*Id.*; *see also* Ex. 1009, 10:11-12.)

b) determining a phase difference between an input clock signal and a feedback clock signal;

*Kim* discloses this feature. (Ex. 1002, ¶¶57-60.) For instance, *Kim* discloses determining a phase difference between a system clock signal SCLK ("an input clock signal") and a chip clock signal CCLK ("a feedback clock signal"). (*Id.*) In particular, *Kim* discloses with reference to figure 3 "a phase detector 202 for outputting a comparing signal (DET) by comparing the phases of the system clock signal (SCLK) and a chip clock signal (CCLK)." (Ex. 1009, 3:24-27; *see also id.*, Abstract ("a phase detector for outputting a comparing signal by comparing a system clock signal with a chip clock signal"), FIG. 3.)

FIG. 3




(Ex. 1002, ¶57, citing Ex. 1009, FIG. 3 (annotated to show signals SCLK and CCLK constituting the claimed input clock signal and feedback clock signal in green and blue, respectively, and to show in red the phase detector 202 that determines the phase difference between SCLK and CCLK).)

*Kim* discloses that the system clock signal (SCLK) is a clock signal that is provided as an input to the delay locked loop (DLL) shown in figure 3 and also provided as an input to the phase detector 202. (Ex. 1002, ¶58; Ex. 1009, FIG. 3, 5:13-14 ("system clock signal (SCLK) [is] inputted to the phase detector 202").)

Therefore, the system clock signal (SCLK) is an "input clock signal." (Ex. 1002, ¶58.)

*Kim* discloses that "[t]he chip clock signal (CCLK) [is] fed back from the clock signal distributor 207." (Ex. 1009, 5:12-13, 9:61-63 ("Then the chip clock signal (CCLK) is fed back to the phase detector 202, and the operation is repeatedly performed."); Ex. 1002, ¶59.)

*Kim* discloses that the phase detector 202 outputs either a '1' or a '0' based on whether the chip clock signal (CCLK) leads or lags ("follows") the system clock signal (SCLK). (Ex. 1002, ¶60; Ex. 1009, 5:14-19 ("the phase detector 202 outputs a comparing signal '1' to shift register 203 **when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase**, or outputs a '0' to the shift register 203 **when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase**") (emphasis added).) A person of ordinary skill in the art would have understood detecting whether one clock signal leads or lags another clock signal constitutes "determining a phase difference" between the two clock signals especially given that the determination as to leading or lagging is done by "comparing the phases of the system clock signal (SCLK) and a chip clock signal (CCLK)." (Ex. 1009, 3:24-27; *see also id.*, Abstract ("a phase detector for outputting a comparing signal by comparing a system clock signal with a chip clock signal"), FIG. 3; Ex. 1002, ¶60.) As such, *Kim* discloses "determining a

phase difference between an input clock signal and a feedback clock signal" as recited in claim 10. (Ex. 1002, ¶60.)

> c) maintaining the phase difference between the input clock signal and the feedback clock signal [within] [3] approximately 180°, including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°; and

*Kim* discloses this feature. (Ex. 1002, ¶¶61-79.)

**"maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°"**

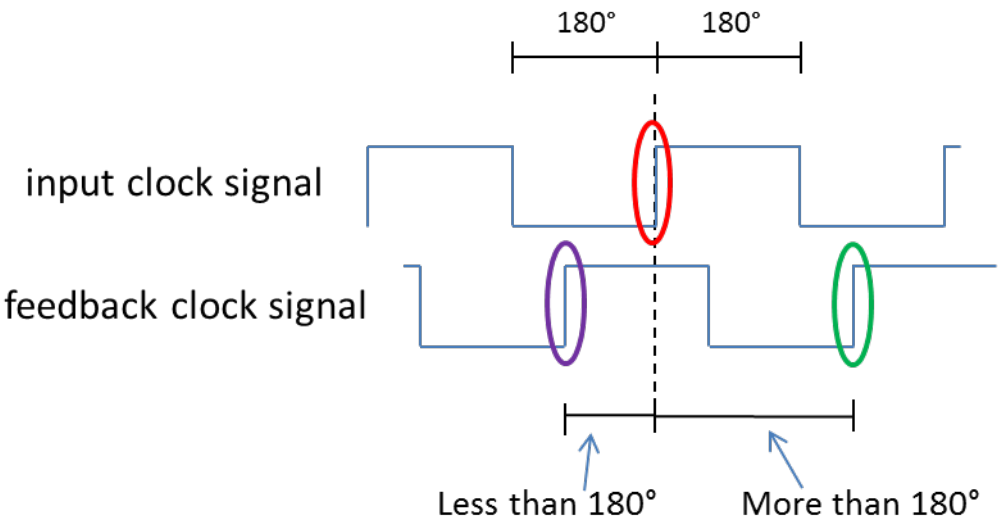
Claim 10 requires that the phase difference between the input clock signal and the feedback clock signal be maintained within approximately 180°. A person

[3] Petitioner assumes for the purposes of this proceeding that limitation 10(c) contains a printing error and that the phrase "**within** approximately 180°" was intended instead of "approximately 180°." During prosecution, Applicant amended claim 11 (which issued as claim 10) and, as amended, claim 11 recited "**within** approximately 180°." (Ex. 1004, 58, 59 (Amendment dated December 13, 1999) (emphasis added).) In the Notice of Allowance, the Examiner also acknowledged claim 11 as reciting "**within** approximately 180°." (*Id.*, 65 (Notice of Allowance dated January 18, 2000) (emphasis added).) Petitioner reserves the right to assert in district court that claim 10 is invalid under 35 U.S.C. § 112.

of ordinary skill in the art would have understood that for two clock signals having the same frequency, and hence the same period, the phase difference between the two signals is always within approximately 180°. (Ex. 1002, ¶62.) For example, if the feedback clock signal is lagging the input clock signal by 210°, that is the same as the feedback clock leading the input clock signal by 150°. (*Id.*) That is because one cycle of a periodic signal encompasses 360° in phase, and 360° – 210° = 150°. (*Id.*) Therefore, the phase difference between the input clock signal (SCLK) and the feedback clock signal (CCLK) in *Kim* is always "within approximately 180°." (*Id.*)

In the demonstrative below, the rising edge of the feedback clock signal (shown in green) lags behind the input clock signal rising edge (shown in red) by more than 180 degrees. (*Id.*, ¶63.) Therefore, the phase difference between the two clocks may appear to be more than 180 degrees. (*Id.*) But the rising edge of the feedback clock signal (shown in purple) is less than 180 degrees ahead of the input clock signal rising edge (shown in red). (*Id.*) As is apparent, the phase difference (plus or minus) between the input clock signal and the feedback clock signal is within approximately 180°, and, regardless of how the feedback clock is shifted to the right or left, a rising edge of the feedback clock signal will always be within approximately 180° of the input clock signal. (*Id.*) As such, the input clock

signal and the feedback clock signal will always have a phase difference within approximately 180°. (*Id.*)




**(**Ex. 1002, ¶63.)

In *Kim* the delay locked loop of figure 3 generates the chip clock signal (CCLK) ("feedback clock signal") by delaying the system clock signal (SCLK) ("input clock signal") and therefore a POSITA would have understood that the chip clock signal (CCLK) and the system clock signal (SCLK) in *Kim* have the same frequency, and hence the same period. (*Id.*, ¶64, citing Ex. 1009, 2:38-45 ("it is an object of the present invention to provide an improved phase delay correction apparatus having an indefinite delay range and to embody a phase shift having a precise resolution"), 9:64-66 ("the present invention can provide an indefinite delay range by adjusting the phase of the driving signal in one domain comprising 0°~180° and in the other domain comprising 180°~360°"), 10:9-12 ("the present

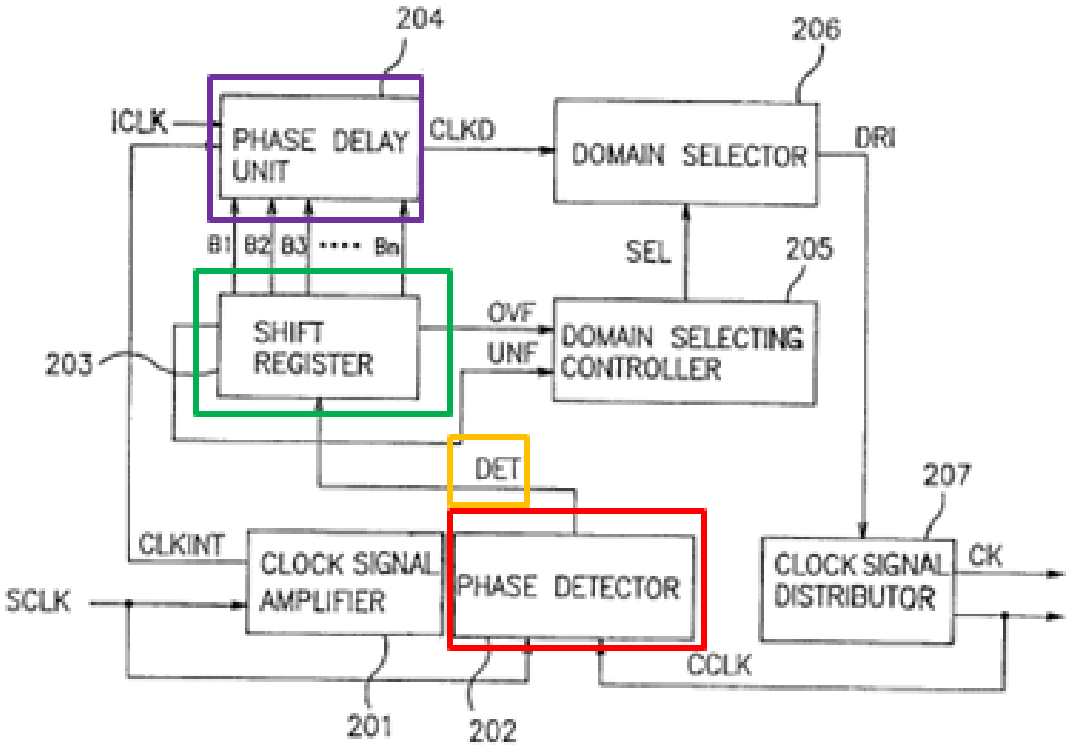
invention has the effect that a phase shift apparatus having a more precise resolution can be embodied, by reducing the number of elements comprising the delay units"), FIGS. 4-6 (showing the path through which SCLK propagates through to produce CCLK).) As discussed above, because CCLK and SCLK have the same frequency, the phase difference between CCLK and SCLK is always within approximately 180°, and therefore *Kim* discloses "maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°" as recited in claim 10. (Ex. 1002, ¶64.)

Moreover, the operation of the delay locked loop in figure 3 of *Kim* demonstrates that *Kim* maintains a phase difference between CCLK and SCLK that is near zero degrees (with some deviation based on the granularity of the delay elements included in *Kim's* delay line). (*Id.*, ¶65.) Regarding the operation of delay locked loops, if it was determined that the output clock lags behind a reference clock, a reduction in the amount of delay in the delay line would reduce the lag and thereby reduce the phase difference between the reference clock and the output clock. (Ex. 1002, ¶65; *see also id.*, ¶¶32-33. In other words, the goal of a delay locked loop is to achieve phase alignment between two clock signals, where one is delayed through the delay line and the other serves as a reference. (*Id.*, ¶65.) Similarly, as discussed immediately below, the delay locked loop in figure 3 of *Kim* maintains the phase difference between the system clock signal

(SCLK) ("input clock signal") and chip clock signal (CCLK) ("feedback clock signal") near zero degrees, which is "within approximately 180°." (*Id.*)

*Kim* discloses with reference to figure 3 "a phase detector 202 for outputting a comparing signal (DET) by comparing the phases of the system clock signal (SCLK) and a chip clock signal (CCLK), a shift register 203 for sequentially shifting data (0 or 1) in two directions in accordance with the comparing signal (DET) from the phase detector 202, [and] a phase delay unit 204 for outputting a phase-adjusted clock signal (CKLD) by delaying the output of the clock signal amplifier 201 in accordance with the bit values of the shift register 203." (Ex. 1009, 3:25-34.)

FIG. 3



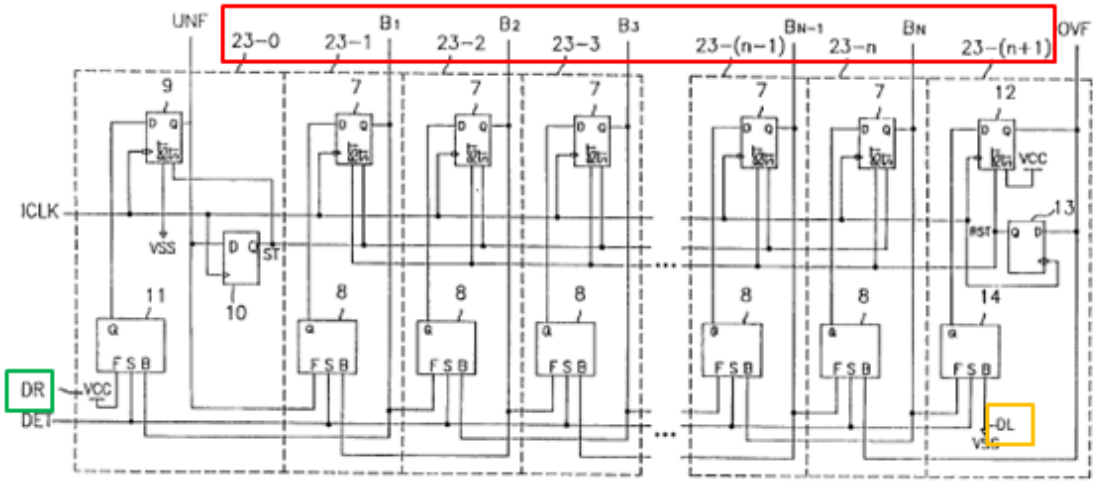

(Ex. 1002, ¶66, citing Ex. 1009, FIG. 3 (annotated to show the phase detector 202 in red, the comparing signal DET in orange, the shift register 203 in green, and the phase delay unit 204 in purple).)

A person of ordinary skill in the art would have understood that the delay locked loop shown in figure 3 of *Kim* functions to lock the system clock signal (SCLK) to the chip clock signal (CCLK) in phase, i.e., so that the two signals are phase-aligned. (Ex. 1002, ¶67.) Such a person would have had this understanding based on *Kim*'s disclosures regarding the phase detector 202, shift register 203, and phase delay unit 204, as explained below. (*Id.*)

*Kim* discloses that "the phase detector 202 outputs a comparing signal '1' to shift register 203 when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase, or outputs a '0' to the shift register 203 when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase." (Ex. 1009, 5:14-19.) "As shown in FIG. 4, the shift register 203 includes data bit units 23-1, . . . ,23-n," and "[w]hen the comparing signal (DET) from the phase detector 202 is '1', the data bit units 23-1, . . . ,23-n shift the data '1' by one bit to the right from the input side (DR) . . . and when the comparing signal (DET) of the same is '0', the data bit units 23-1, . . . ,23-n each shift the data '0' by one bit to the left from the input side (DL)." (Ex. 1009, 3:46-54; *see also* Ex. 1009, 5:21-29 ("When the comparing signal (DET) outputted from the phase detector 202 is '1', the shift register 203 sequentially shifts the data '1' to the right from the input side (DR)," whereas "[w]hen the comparing signal (DET) is '0', the shift register 203 shifts the data '0' to the left from the input side (DL) . . . ."); Ex.1002, ¶68.).

In figure 4 of *Kim*, which is a detailed view of the shift register 203 (Ex. 1009, 3:5-6), the input sides DR and DL correspond to the left and right sides of the figure, respectively. (Ex. 1002, ¶69.)

FIG. 4




(*Id.*, ¶69, citing Ex. 1009, FIG. 4 (annotated to show data bit units 23-i in red, input side DR in green, and input side DL in orange).)

Thus, when the chip clock signal (CCLK) leads the system clock signal (SCLK), a '1' bit is shifted into the shift register 203 from the left, with the existing contents of the data bit units each being shifted by one cell to the right, and when the chip clock signal (CCLK) trails the system clock signal (SCLK), a '0' bit is shifted into the shift register 203 from the right, with the existing contents of the data bit units each being shifted by one cell to the left. (Ex. 1002, ¶70.)

*Kim* discloses that "the phase delay unit 204 is controlled by the bit values (B1,B2, . . . ,Bn) outputted from the shift register 203." (Ex. 1009, 6:50-51.) The number of data bit units containing a '1' in the shift register 203 influences the amount of delay produced by the phase delay unit 204. For example, "when the bit values (B1, . . . ,Bn) outputted from the shift register 203 are all '0', . . . a

minimum clock signal delay occurs," whereas "[w]hen the bit values (B1, . . . ,Bn) outputted from the shift register 203 are all '1', . . . a maximum clock signal delay occurs." (Ex. 1009, 6:55-64.) In other words, shifting a '1' into the shift register 203 increases the delay applied to the clock signal CLKINT, whereas shifting a '0' into the shift register 203 decreases the delay applied to the clock signal CLKINT. (Ex. 1002, ¶71.)

Thus, when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase, DET is set to '1', which causes a '1' bit to be shifted into the shift register 203, which in turn increases the delay applied by the phase delay unit 204; and when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase, DET is set to '0', which causes a '0' bit to be shifted into to shift register 203, which in turn decreases the delay applied by the phase delay unit 204. (*Id*., ¶72.)

*Kim* discloses that the phase delay unit 204 applies delay to clock signal CLKINT, which is an amplified version of system clock signal SCLK. (Ex. 1009, 4:47-49, ("The delay units 24-1,24-2, . . . 24-(n-1) each includes series inverters 16, 17 which sequentially delay the clock signal (CLKINT) from the clock signal amplifier 201"), FIG. 3; *see also id*., 6:50-54; Ex. 1002, ¶73.) *Kim* further discloses that the chip clock signal CCLK is based on the phase-adjusted clock signal CLKD outputted by the phase delay unit 204. (Ex. 1009, 3:30-45, FIG. 3.)

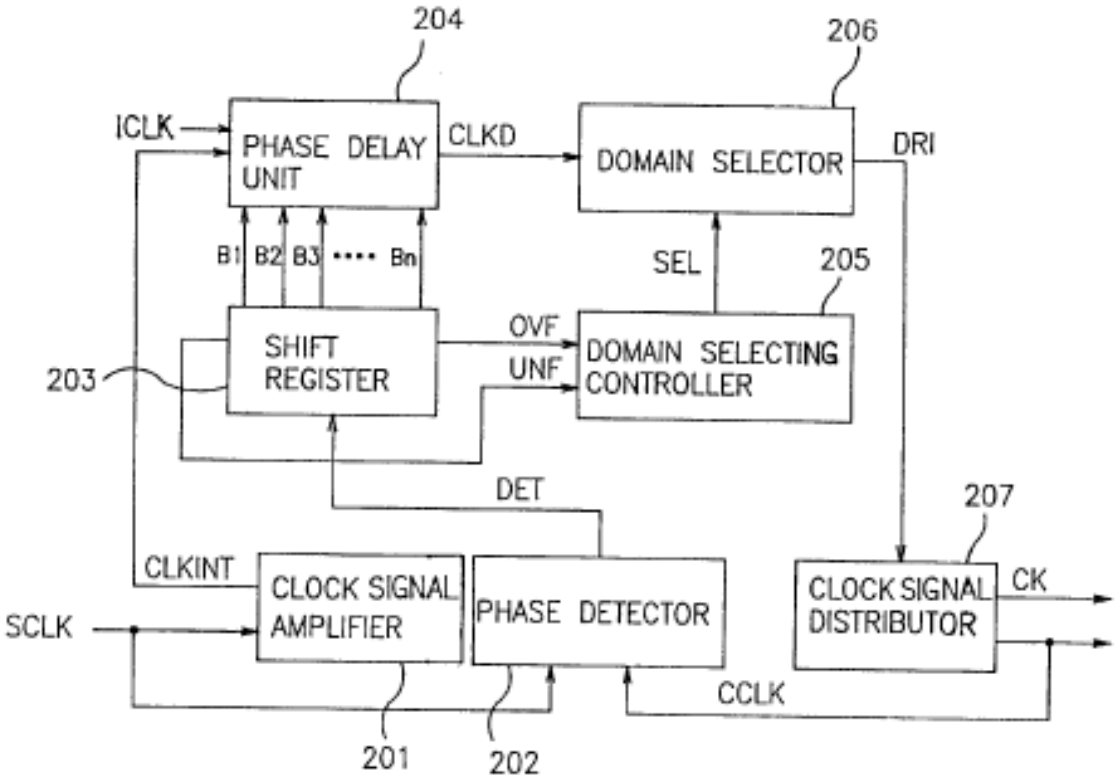
Therefore, a person of ordinary skill in the art would have understood that *Kim*'s delay locked loop described with reference to figure 3 operates to maintain the system clock signal SCLK phase-aligned with the chip clock signal CCLK, i.e., with a goal of maintaining 0° of phase difference. (Ex. 1002, ¶73.) While the degree to which CCLK can be aligned with SCLK is impacted by the granularity of the delay elements included in the phase delay unit 204 of *Kim*, the resulting phase difference between CCLK and SCLK would have been less than 180°. (*Id.*) For example, while the phase delay unit pictured in figure 5 of *Kim* is shown to include more delay units between delay unit 24-4 and delay unit 24-(n-2), even with only those delay units pictured, the six transmission gates 15 (which correspond to taps on the delay line from which the delayed clock signal can be selected) divide the "first domain, which comprises "0°~180°" of delay, into 30° increments. (*Id.*) As such, even without the additional delay units between delay unit 24-4 and delay unit 24-(n-2), once the delay locked loop in figure 3 of *Kim* has achieved a "lock," the resulting chip clock signal (CCLK) and the system clock signal (SCLK) would have a phase difference of less than 30°, which is less than 180°. (*Id.*) A person of ordinary skill in the art would have understood that once the delay locked loop of *Kim* has locked (i.e. achieved the best phase alignment between CCLK and SCLK that it can), it will alternate back and forth between detecting the chip clock signal (CCLK) slightly lagging the system clock signal

(SCLK) at which point it will reduce the delay slightly, and then detecting the chip clock signal (CCLK) slightly leading the system clock signal (SCLK) at which point it will increase the delay slightly. (*Id.*) Once locked, the phase of the chip clock signal (CCLK) will move back and forth over the ideal point of alignment such that the chip clock signal (CCLK) jitters back and forth between lagging and leading the system clock signal (SCLK). (*Id.*)

**"including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°"**

*Kim* further discloses adjusting the system clock signal SCLK ("input clock signal") with a loop comprising phase detector 202 ("phase detector"), shift register 203 ("shift register"), and phase delay unit 204 ("delay line") when the determined phase difference is less than approximately 180°. (Ex. 1002, ¶74; *see also supra*, Section IX.A.1(a) (regarding the phase delay unit 204 constituting a "delay line").)

FIG. 3




(Ex. 1009, FIG. 3; Ex. 1002, ¶74..)

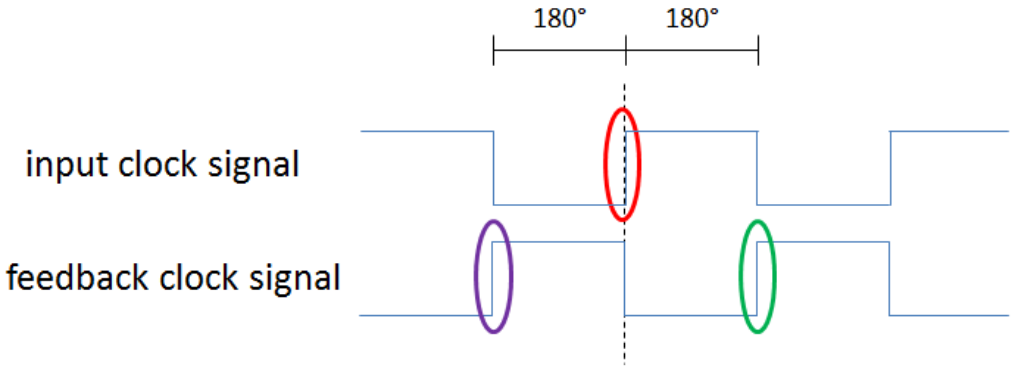
The delay locked loop shown in figure 3 of *Kim* operates to adjust the system clock signal (SCLK) ("input clock signal") when the determined phase difference is less than approximately 180°. As discussed above, the delay locked loop described in *Kim* in conjunction with figure 3 continuously adjusts the system clock signal (SCLK) ("input clock signal") to produce the chip clock signal (CCLK) ("feedback clock signal"). (Ex. 1002, ¶75, citing Ex. 1009, 9:61-63 ("Then the chip clock signal (CCLK) is fed back to the phase detector 202, and the operation is repeatedly performed.").) As such, even when the delay locked loop

in figure 3 of *Kim* achieves near alignment corresponding to a near zero phase difference, it still adjusts the input clock using the loop. Therefore, as explained in more detail below, *Kim* discloses "adjusting . . . when the determined phase difference is less than approximately 180°." (Ex. 1002, ¶75.)

Claim 10 of the '507 patent recites that the adjusting is performed "when the determined phase difference is less than approximately 180°." (Ex. 1001, 4:53-56.) A POSITA would have understood that this condition will always be true in *Kim* because, as discussed above, the phase difference between CCLK and SCLK will always be less than approximately 180°. (Ex. 1002, ¶76.) Hence, each time *Kim* adjusts the delay of SCLK, such adjusting must necessarily occur "when the determined phase difference is less than approximately 180°" because the condition will always be true. (*Id*.) Therefore, *Kim* discloses "adjusting . . . when the determined phase difference is less than approximately 180°" for this additional reason. (*Id*.)

A person of ordinary skill in the art would have understood that the only scenario in which the two clock signals with the same frequency do not have a phase difference that is **less than** 180° is when those signals have a phase difference that is **exactly equal to** 180°. (*Id.*, ¶77.) This ideal-case scenario is illustrated in the demonstrative below in which a first rising edge of the feedback clock signal (shown in purple) leads the rising edge of input clock signal (shown in

red) by exactly 180° and the second rising edge of the feedback clock signal (shown in green) lags the rising edge of input clock signal (shown in red) by exactly 180°. (*Id.*)




(Ex. 1002, ¶77.)

However, claim 10 does not state that the phase adjustment occurs "when the determined phase difference is less than 180°", but instead recites "when the determined phase difference is less than **approximately** 180°" (Ex. 1001, 4:53-56 (emphasis added).)

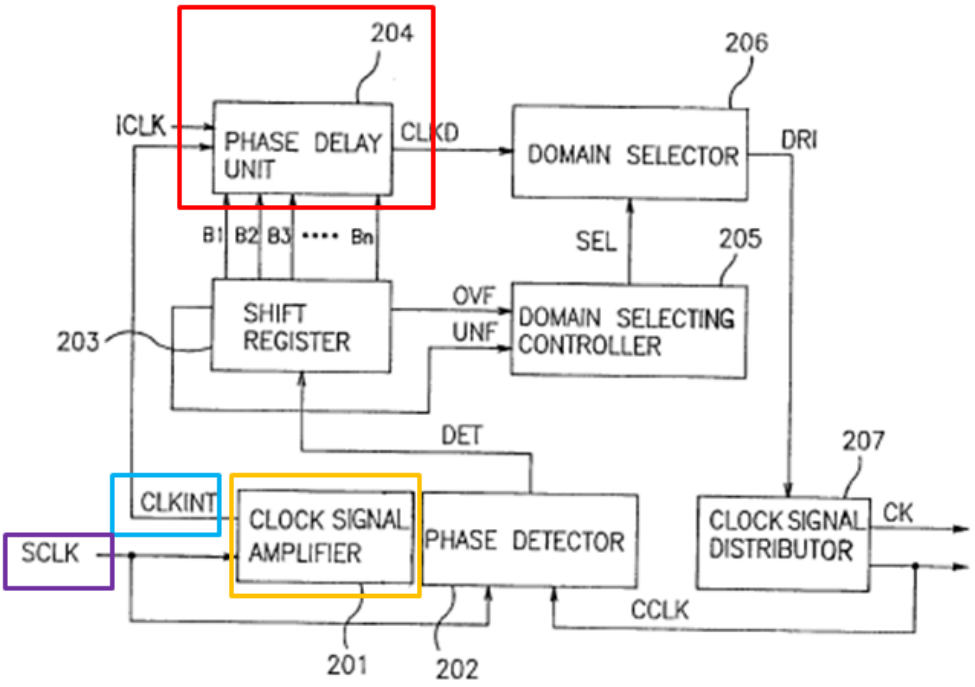
Furthermore, claim 10 uses open-ended, "comprising" language, and states that the adjusting occurs "when the determined phase difference is less than approximately 180°" (Ex. 1001, 4:55-56) and does not state that such adjustment **only** occurs when that condition is met or state that something else occurs when that condition is not met. As such, because *Kim* is constantly adjusting the delay of the system clock signal (SCLK) ("input clock signal") to produce the chip clock

signal (CCLK) ("feedback clock signal") (Ex. 1002, ¶¶78-79; Ex. 1009, 9:61-63), *Kim* discloses that the adjusting occurs "when the determined phase difference is less than **approximately** 180.°" (Ex. 1002, ¶79.)

d) delaying the input clock signal to compensate for the phase difference,

*Kim* discloses this feature, for reasons similar to those discussed above for limitation 10(a). (*See supra*, Section IX.A.1(a); Ex. 1002, ¶¶80-82.) *Kim* discloses that the phase delay unit 204 which is shown at a high level in figure 3 and shown in greater detail in figure 5 "includes a plurality of **delay units** 24-1,24-2, . . . ,24-(n-1) , 24-n outputting the phase-adjusted clock signal (CLKD) by sequentially **delaying** the clock signal (CLKINT) outputted from the clock signal amplifier 201." (Ex. 1009, 4:40-46 (emphasis added)(sic); *see supra,* Section IX.A.1(a); Ex. 1002, ¶80.)

FIG. 3




(Ex. 1002, ¶80, citing Ex. 1009, FIG. 3 (annotated to show the phase delay unit 204 in red, the clock signal amplifier 201 in orange, the system clock (SCLK) in purple and the clock signal CLKINT in blue).)

As disclosed by *Kim*, the phase delay unit 204 delays "the clock signal (CLKINT) outputted from the clock signal amplifier 201." (Ex. 1009, 4:40-49, FIG. 3; *see also id.*, 6:50-53.) *Kim* discloses that "[t]he clock signal amplifier 201 amplifies a system clock signal (SCLK) and outputs it to the phase delay unit 204." (*Id.*, 5:10-11; *see also id.*, 3:23-24 ("a clock signal amplifier 201 for amplifying a system clock signal (SCLK)").) Moreover, *Kim* discloses that "[t]he clock signal amplifier 201 can be omitted if the system clock signal (SCLK) has a relatively

low frequency range and a large swing." (*Id.*, 9:54-56.) As such, the phase delay unit 204 delays the system clock signal (SCLK) ("input clock signal") either directly or as the clock signal CLKINT, which is an amplified version of the system clock signal (SCLK). (Ex. 1002, ¶81.)

*Kim* discloses that "the phase delay unit 204 is controlled in accordance with the bit values (B1,B2, . . . ,Bn) outputted from the shift register" (Ex. 1009, 4:40-42; *see also id.*, 6:50-51), where those bit values are set based on the value of the comparing signal DET, which in turn is based on the determined phase difference. (*See supra*, Section IX.A.1(c); Ex. 1009, FIG. 3; Ex. 1002, ¶82.) Consequently, as discussed above with respect to limitation 10(c), when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase, the delay applied by the phase delay unit 204 is increased, and when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase, the delay applied by the phase delay unit 204 is decreased. (*See supra* Section IX.A.1(c); Ex. 1002, ¶82.) Thus, *Kim* discloses performing delaying the system clock signal (SCLK) ("delaying the input clock signal") where the delay is adjusted based on whether the chip clock signal (CCLK) leads or lags the system clock signal (SCLK) ("to compensate for the phase difference"). (Ex. 1002, ¶82.)

e) wherein a number of delay cells utilized is reduced by approximately one-half.

*Kim* discloses this feature, for reasons similar to those discussed above for limitation 10(a)[4] (Ex. 1002, ¶83; *see also supra* Section IX.A.1(a).) For example, *Kim* discloses that "**the number of the delaying elements of the present invention can be reduced to half**, since the phase shift is performed only in the first domain and the phase shift in the second domain is performed inverse to the phase shift in the first domain." (Ex. 1009, 10:4-8 (emphasis added).)

**2. Claim 11**

a) The method of claim 10 wherein the phase detector comprises a phase difference detector with a first resolution.

*Kim* discloses this feature. (Ex. 1002, ¶¶84-87.)

**"phase difference detector"**

As discussed above with respect to claim limitations 10(a)-(c), *Kim* discloses a phase detector 202 shown in figure 3. (*See supra* Sections IX.A.1(a)-(c); Ex. 1009, FIG. 3; Ex. 1002, ¶85.) *Kim's* phase detector 202 determines whether the chip clock signal (CCLK) leads or lags the system clock signal (SCLK).

> [T]he phase detector 202 outputs a comparing signal "1" to shift register 203 when the chip clock signal (CCLK) leads the

[4] Petitioner reserves the right to assert indefiniteness of claim 10 in district court, e.g., in light of the phrase "reduced by approximately one-half."

> system clock signal (SCLK) in phase, or outputs a "0" to the shift register 203 when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase.

(Ex. 1009, 5:14-19.)

A person having ordinary skill in the art would have understood that a determination as to whether CCLK leads or lags SCLK would indicate a phase difference between the CCLK and SCLK signals. (Ex. 1002, ¶86.) The phase detector 202 of *Kim* is or includes a "phase difference detector." (*Id.*)

**"[phase difference detector] with a first resolution"**

While *Kim* does not expressly disclose that phase detector 202 comprises a phase difference detector "with a first resolution," a person having ordinary skill in the art would have understood that *Kim's* phase detector 202 necessarily has this feature, and that *Kim* inherently discloses this feature. (*Id.*, ¶87.) Such a person would have had that understanding because *Kim* discloses determining a phase difference as discussed above and because a determination of phase difference must be with respect to some resolution ("first resolution"). (*Id.*) Such a person would have understood that resolution refers to the capability to distinguish one phase from another (e.g., the phase of one input of phase detector 202 from the phase of another input of the phase detector), and that if the phase detector 202 did not have a resolution ("first resolution") then it would have been unable to perform

its disclosed function. (*Id.*) In other words, in order for phase detector 202 and the delay locked loop of figure 3 of *Kim* to function properly, phase detector 202 must comprise a phase difference detector that inherently has a "first resolution." (*Id.*)

**3. Claim 13**

a) A method for reducing delay line length in a digital delay locked loop (DLL), the method comprising:

The preamble of claim 13 recites "for reducing delay line length." But the phrase "for reducing delay line length" does not breathe life and meaning into the claim and is not necessary to understand any positive limitations in the body of claim 13 or any claims depending from claim 13. Indeed, the body of claim 13 and the claims depending from claim 13 do not recite anything related to reduction of delay line length. Moreover, "for reducing delay line length" constitutes merely an intended use. Therefore, it is not limiting. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999) (explaining that preamble is limiting if it is "'necessary to give life, meaning, and vitality' to the claim" but that "[i]f, however, the body of the claim fully and intrinsically sets forth the complete invention, including all of its limitations, and the preamble offers no distinct definition of any of the claimed invention's limitations, but rather merely states, for example, the purpose or intended use of the invention, then the preamble . . . cannot be said to constitute or explain a claim limitation"); *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015) (considering whether

preamble terms are "necessary to understand positive limitations in the body of claims," to determine limiting status).

Although a portion of the preamble (specifically, the phrase "a digital delay locked loop (DLL)") serves as antecedent basis for the term "the DLL" in the body of the claim, the remainder of the preamble (i.e., "for reducing delay line length") is still not limiting. *See, e.g., TomTom, Inc. v. Michael Adolph*, 790 F.3d 1315, 1324 (Fed. Cir. 2015) (holding that a portion of the preamble that does not recite essential structure or steps, or give necessary life, meaning, and vitality to the claim does not become limiting simply because of the presence of another limiting phrase in that preamble.)

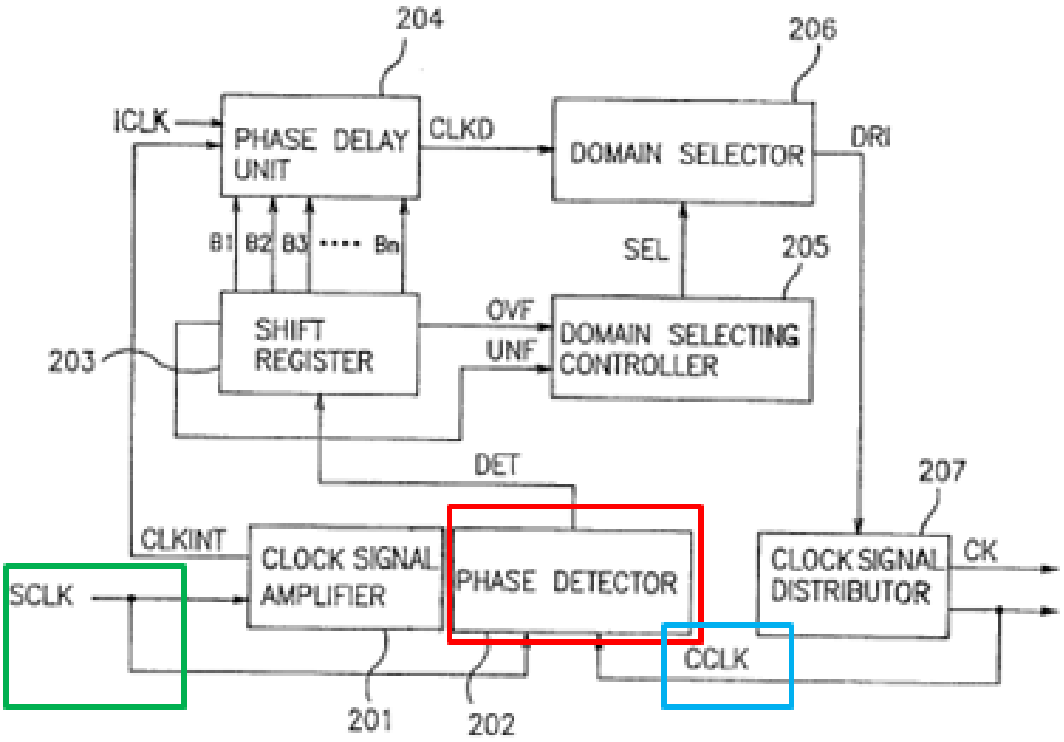
To the extent any portion of the preamble is considered limiting, *Kim* discloses this feature for the same reasons discussed above with respect to claim limitation 10(a). (*See supra* Section IX.A.1(a); Ex. 1002, ¶88.)

> b) determining whether a feedback clock signal in the DLL follows within a 180° phase difference behind an input clock signal; and

*Kim* discloses or suggests this feature. (Ex. 1002, ¶¶89-96.) For instance, *Kim* discloses determining a phase difference between a system clock signal SCLK ("an input clock signal") and a chip clock signal CCLK ("a feedback clock signal"). (*Id.*) In particular, *Kim* discloses with reference to figure 3 "a phase detector 202 for outputting a comparing signal (DET) by comparing the phases of

the system clock signal (SCLK) and a chip clock signal (CCLK)." (Ex. 1009, 3:24-27; *see also id.*, Abstract ("a phase detector for outputting a comparing signal by comparing a system clock signal with a chip clock signal"), FIG. 3.)

FIG. 3




(Ex. 1002, ¶89, citing Ex. 1009, FIG. 3 (annotated to show signals SCLK and CCLK constituting the claimed input clock signal and feedback clock signal in green and blue, respectively, and to show in red the phase detector 202 that determines the phase difference between SCLK and CCLK).)

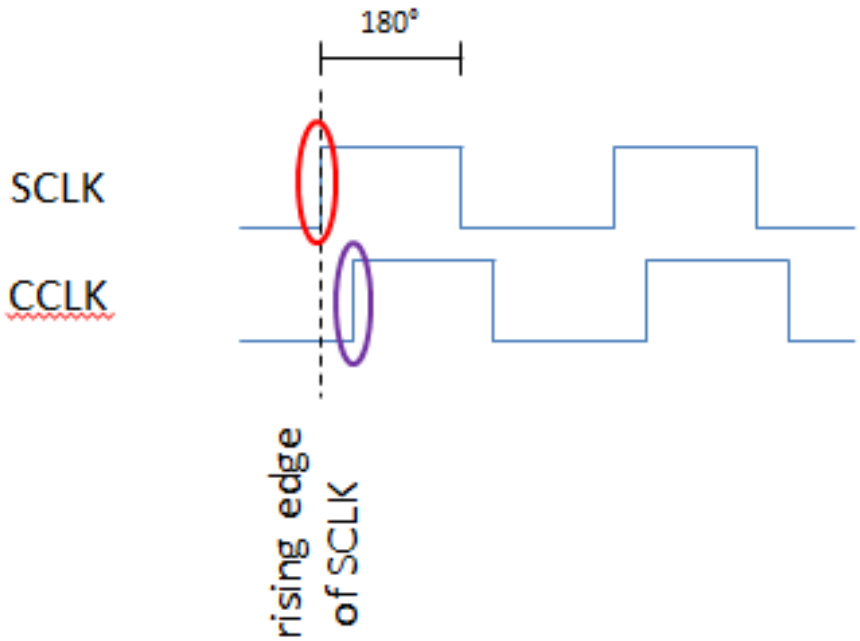
*Kim* discloses that the system clock signal SCLK is a clock signal that is provided as an input to the delay locked loop (DLL) shown in figure 3 and also

provided as an input to the phase detector 202. (Ex. 1002, ¶90; Ex. 1009, FIG. 3, 5:13-14 ("system clock signal (SCLK) [is] inputted to the phase detector 202") Therefore, the system clock signal SCLK is an "input clock signal." (Ex. 1002, ¶90.)

*Kim* discloses that "[t]he chip clock signal (CCLK) [is] fed back from the clock signal distributor 207." (Ex. 1009, 5:12-13.) Therefore, the chip clock signal CCLK is a "feedback clock signal." (Ex. 1002, ¶91.)

*Kim* also discloses determining whether the chip clock signal (CCLK) ("a feedback clock signal") in the digital DLL of figure 3 ("the DLL") follows within a 180° phase difference behind the system clock signal (SCLK) ("an input clock signal"). (*Id.*, ¶92.) Specifically, *Kim* discloses that the phase detector 202 outputs either a '1' or a '0' based on whether the chip clock signal (CCLK) leads or lags ("follows") the system clock signal (SCLK). (Ex. 1009, 5:14-19 ("the phase detector 202 outputs a comparing signal '1' to shift register 203 **when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase**, or outputs a '0' to the shift register 203 **when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase**") (emphasis added).) A person of ordinary skill in the art would have understood that if a clock "lags" another clock in phase, it "follows within a 180° phase difference behind the other clock." (Ex. 1002,

¶92.) The demonstratives below help to illustrate the phase relationship between two clocks where one clock leads or lags another in phase. (*Id.*)

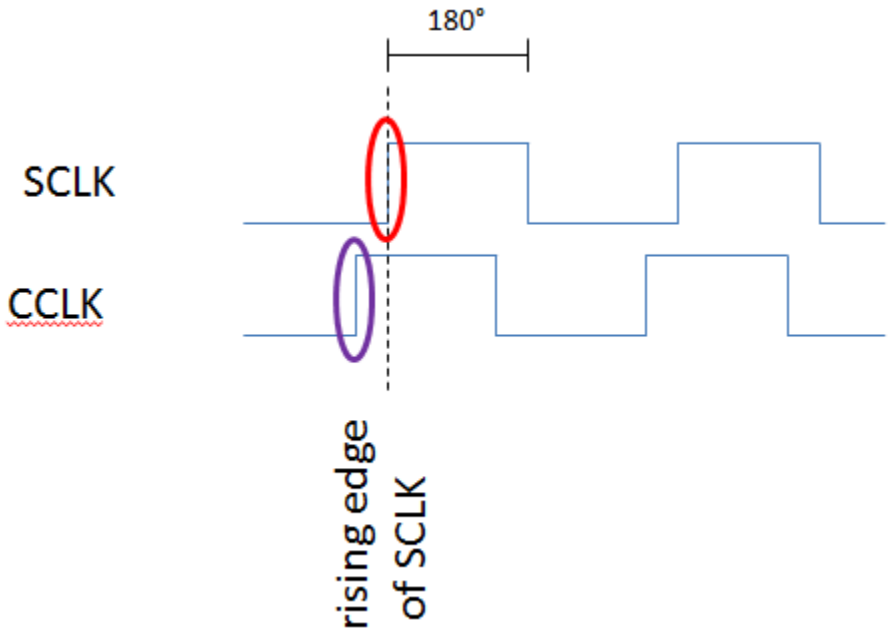



(*Id.*)

In the scenario depicted in the above demonstrative, the rising edge of the chip clock signal (CCLK) ("the feedback clock signal") (annotated in purple) **lags** the rising edge of the system clock signal (SCLK) (corresponding to the dotted line and annotated in red) ("the input clock signal"). (Ex. 1002, ¶93; *see also id.*, ¶¶25-31(discussing phase of a clock signal and leading/lagging clock signals).) In such a scenario, the chip clock signal (CCLK) follows within a 180° phase difference behind the system clock signal (SCLK). (*Id.*, ¶93.) As disclosed by *Kim*, in this

scenario, with CCLK and SCLK as shown above as inputs, the phase comparator 202 outputs a '0' on the DET signal. (Ex. 1009, 5:14-19.)

The following demonstrative illustrates the opposite case in which the chip clock signal (CCLK) **leads** the system clock signal (SCLK).




(Ex. 1002, ¶94.)

In this demonstrative, again, the rising edge of system clock signal SCLK is shown in red and corresponds to the dotted line, while the rising edge of the chip clock signal (CCLK) is shown in purple. (Ex. 1002, ¶95.) In this scenario, the chip clock signal (CCLK) has a rising edge (shown in purple) slightly before the rising edge of the system clock signal SCLK (shown in red). (*Id.*) As such, the chip clock signal (CCLK) **leads** the system clock signal SCLK and therefore does **not** follow within a 180° phase difference behind the system clock signal SCLK,

because as shown in this demonstrative, the rising edge of the chip clock signal (CCLK) (purple) does not occur within the phase interval annotated above as "180°." (*Id.*) Equivalently, in the above scenario the chip clock signal (CCLK) can be considered to follow (lag) the system clock signal SCLK by **more** than 180°. (*Id.*) For example, observe that the second rising edge of the chip clock signal (CCLK), which occurs immediately after the one shown in purple above (i.e., the rising edge in the next cycle), trails the red rising edge of the system clock signal (SCLK) by more than 180°. (*Id.*)

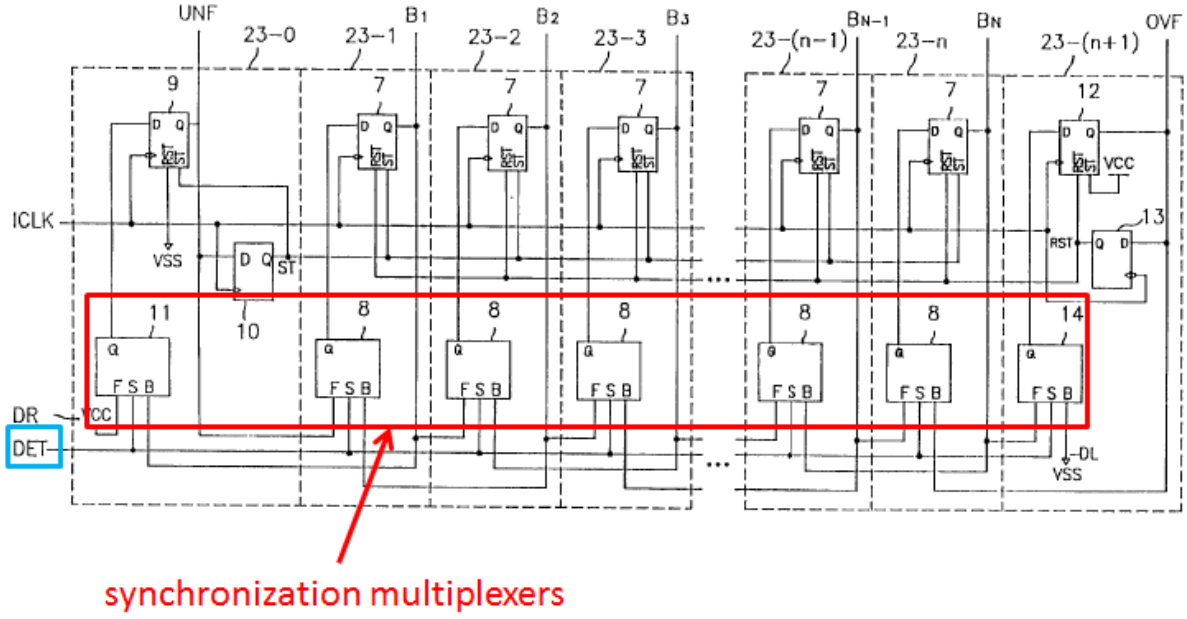
As disclosed by *Kim*, in this scenario, with CCLK and SCLK as shown above as inputs, the phase comparator 202 outputs a '1' on the DET signal. (Ex. 1009, 5:14-19.) Thus, when the chip clock signal (CCLK) leads (**does not** follow within a 180° phase difference behind) the system clock signal (SCLK), the phase detector outputs a '1', whereas when the chip clock signal (CCLK) lags (**does** follow within a 180° phase difference behind) the system clock signal (SCLK), the phase detector outputs a '0'. (Ex. 1002, ¶96.) Therefore, *Kim* discloses determining whether the chip clock signal (CCLK) ("a feedback clock signal") in the DLL follows within a 180° phase difference behind the system clock signal (SCLK) ("an input clock signal"). (*Id.*)

c) selecting a switch position according to the determining step, including selecting a first switch position when the feedback clock signal follows behind the input clock signal with[in] 180°.

*Kim* discloses this feature. (Ex. 1002, ¶¶97-105.)[5] As discussed above with respect to claim limitation 13(b), the figure 3 digital DLL in *Kim* includes the phase detector 202 that performs the claimed "determining." (*Id.*; *see also supra,* Section IX.A.3(b).) As discussed in detail below, the output DET of the phase detector is provided to each of the synchronization multiplexers (11, 8, and 14) within the shift register 203 shown in figure 4 of *Kim*, and each of the synchronization multiplexers constitutes a switch. (Ex. 1002, ¶97; *see also id.*, ¶¶34-37 (discussing multiplexers).)

[5] Petitioner assumes for the purposes of this proceeding that the phrase "within 180°" was intended instead of "with 180°." During prosecution, claim 15 (which issued as claim 13) recited "selecting a switch position according to the determining step, including selecting a first switch position when the feedback clock signal follows behind the input clock signal within 180°." (Ex. 1004, 27-28 (originally filed claim 15), 59 (Amendment dated December 13, 1999.) Similarly, the Examiner used the word "within" when stating the reasons for allowing this claim. (*Id.*, 65 (Notice of Allowance dated January 18, 2000.)

FIG. 4




(Ex. 1002, ¶97, citing Ex. 1009, FIG. 4 (annotated).)

*Kim* discloses that DET is output from the phase comparator as a result of comparing the phases of the system clock signal (SCLK) and a chip clock signal (CCLK). (Ex. 1009, 3:24-27.) The DET signal is provided to the shift register "for sequentially shifting data (0 or 1) in two directions in accordance with the comparing signal (DET) from the phase detector." (*Id.*, 3:27-29.) As further disclosed by *Kim*, the DET signal is "commonly inputted to the selection terminals (S) of the synchronization multiplexers 8,11, and 14." (*Id.*, 4:34-36.) A single DET input is provided over a common signal line to the "S" inputs of the synchronization multiplexers 8, 11 and 14 in figure 4, and therefore DET is

"commonly inputted" to the "S" inputs and thus provided to all of the "S" inputs together. (*Id.*, FIG. 4; Ex. 1002, ¶98.)

*Kim* discloses that each of the synchronization multiplexers has three inputs (F,S,B) and one output (Q) as shown in figure 4. (Ex. 1002, ¶99.)

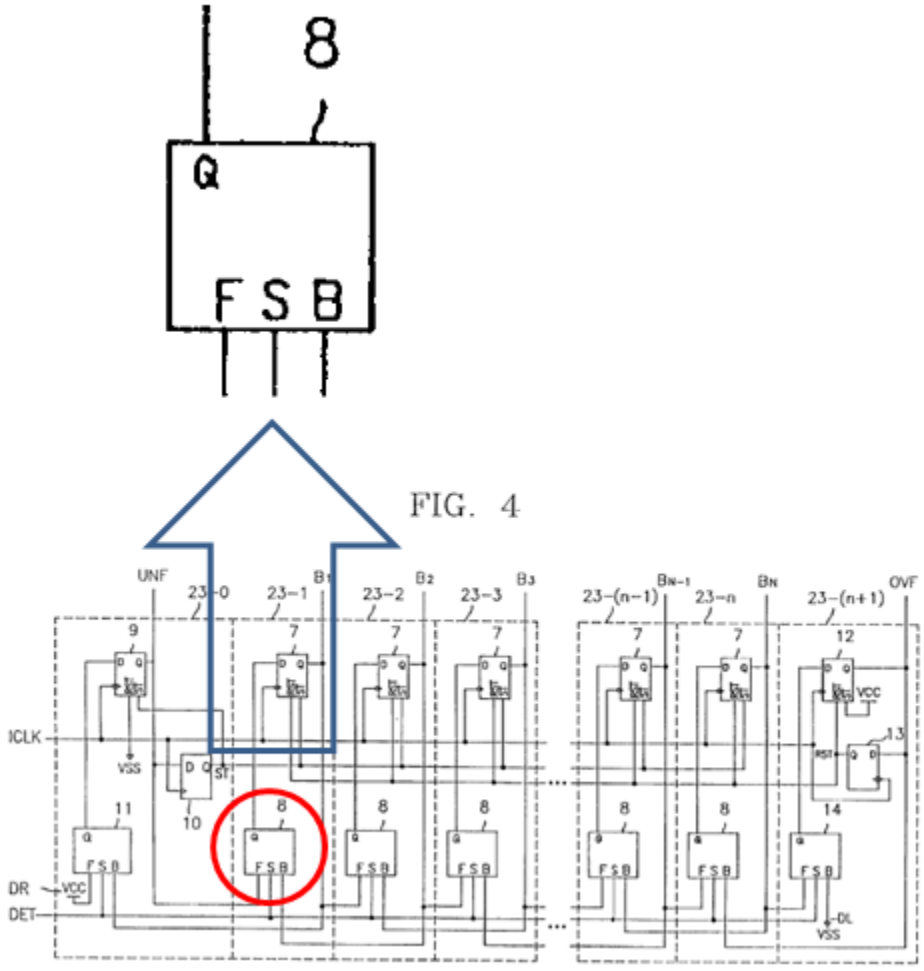



FIG. 4

(*Id.*, citing Ex. 1009, FIG. 4 (annotated to provide magnified view of one of the synchronization multiplexers 8).)

According to *Kim*, (F) is the forward terminal, (B) is the backward terminal, (S) is the selection terminal, and (Q) is the output terminal. (Ex. 1009, 4:2-7 ("a

synchronization multiplexer 8 having its forward terminal (F) connected to the output terminal of the previous data bit unit and its backward terminal (B) connected to the output terminal of the next data bit unit and applying its output signal to the input terminal (D) of the flip flop 7"), 4:34-36, FIG. 4 (showing output (Q) from synchronization multiplexer 8 is applied to the input terminal (D) of the flip flop 7); Ex. 1002, ¶100.)

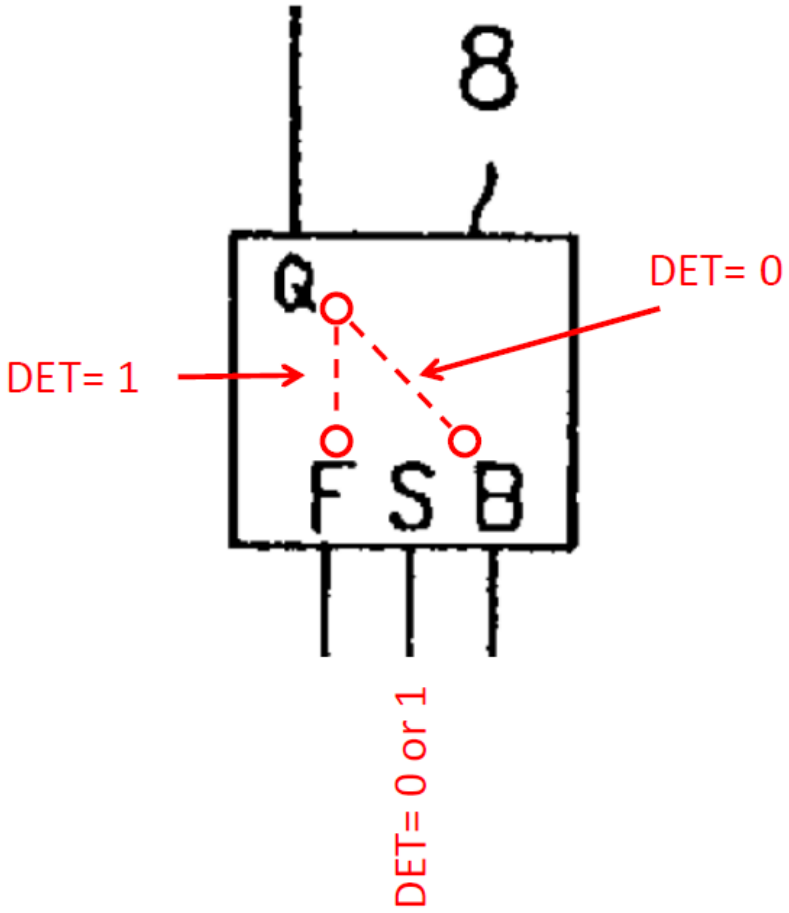
As further disclosed by *Kim*, the synchronization multiplexer selects its output (Q) to be either the signal provided to the forward (F) input or the signal provided to the backward (B) input based on the selection (S) input. (Ex. 1009, 5:51-54 ("The **synchronization multiplexer 8** of the data bit unit 23-1 **outputs the output value '1'** from the underflow bit 23-0 **inputted to its forward terminal (F)** to the flip-flop 7 **in accordance with the comparing signal (DET) '1'")** (emphasis added); 6:21-25 ("the **synchronization multiplexer 8** of the data bit unit 23-n **outputs the output value "0"** from the underflow bit unit 23-(n+1) **inputted to its backward terminal** (2) to the flip-flop 7 **in accordance with the comparing signal (DET) of "0"**) (emphasis added); 5:39-43; Ex. 1002, ¶101.) *Kim*'s use of the DET signal to select forward or backward in the synchronization multiplexers supports the shifting operations within the shift register. (Ex. 1009, 5:20-22 ("When comparing signal (DET) outputted from the phase detector 202 is '1', the shift register 203 sequentially shifts the data '1' to the right from the input

side (DR). . . ."), 5:24-26 ("When the comparing signal (DET) is '0', the shift register 203 shifts the data '0' to the left from the input side (DL). . . ."); Ex. 1002, ¶101.)

In view of the above, a POSITA would have understood that when the output DET of the phase detector 202 is '0', each of the synchronization multiplexers will output on its (Q) output the input on its (B) input to cause the shift register to shift left (backwards). (Ex. 1002, ¶102; *see also id.*, ¶¶34-37 (discussing multiplexers).) Similarly, one of ordinary skill in the art would have understood that when the output DET of the phase detector 202 is '1', each of the synchronization multiplexers will output on its (Q) output the input on its (F) input to cause the shift register to shift right (forwards). (Ex. 1002, ¶102; *see also id.*, ¶¶34-37 (discussing multiplexers).)

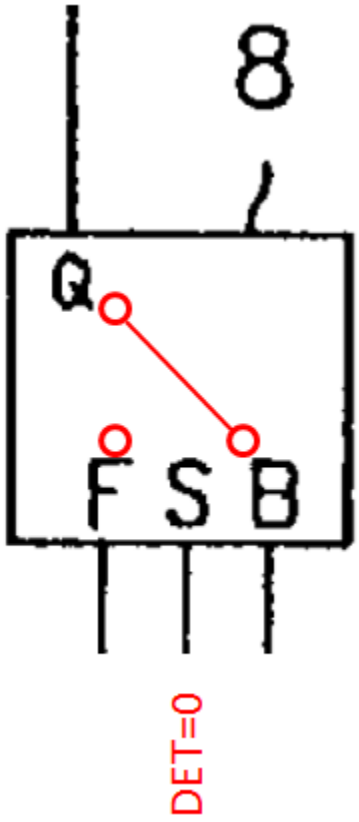
Therefore, *Kim* discloses selecting the (Q) output of each of the synchronization multiplexers 8, 11, and 14 to correspond to its respective (B) input when the DET signal is '0' ("selecting a switch position according to the determining step"), which corresponds to the chip clock signal (CCLK) ("feedback clock signal") following the system clock signal (SCLK) within 180° ("including selecting a first switch position when the feedback clock signal follows behind the input clock signal within 180°"). (*Id.*, ¶103.)

A person of ordinary skill in the art would have understood that the synchronization multiplexers 8, 11, and 14 each choose one of two inputs (F or B) as the output (Q) based on the selection signal (S). (*Id.*, ¶104, citing Ex. 1009, 5:51-54, 6:21-25.) As such, those multiplexers in *Kim* provide the functionality of a single-pole double-throw switch, with two possible states dependent on a control input. (Ex. 1002, ¶104; *see also id.*, ¶¶36-37.) As such, *Kim* discloses selecting a switch position "according to the determining step" (each synchronization multiplexer selects F (forward) or B (backward) based on S (selection)). (Ex. 1002, ¶104.) The demonstrative below helps illustrate this understanding.




(Ex. 1002, ¶104, citing Ex. 1009, FIG. 4 (excerpted and annotated); *see also* Ex. 1002, ¶¶34-37 (discussing multiplexers).)

Thus, *Kim* discloses selecting the switch position shown below, corresponding to connecting the input on B to the output Q ("selecting a first switch position"), when the chip clock signal (CCLK) lags the system clock signal (SCLK) and DET='0' ("when the feedback clock signal follows behind the input clock signal within 180°"). (*See supra* Section IX.A.3(b); Ex. 1002, ¶105; *see also* Ex. 1002, ¶¶34-37 (discussing multiplexers).)




(Ex. 1002, ¶105, citing Ex. 1009, FIG. 4 (excerpted and annotated).)

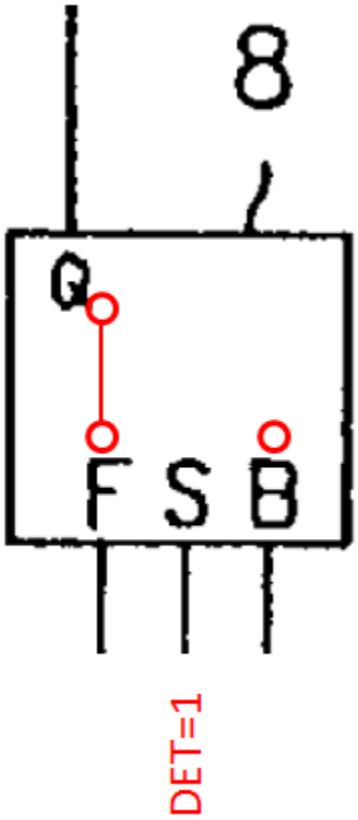
**4. Claim 15**

a) The method of claim 13 wherein selecting further comprises selecting a second switch position when the feedback clock signal does not follow the input clock signal within 180°.

*Kim* discloses this feature. (Ex. 1002, ¶¶106-08.) As discussed above for limitation 13(c), a person of ordinary skill in the art would have understood that a synchronization multiplexer (8, 11, and 14) disclosed by *Kim* provides the functionality of a single-pole double-throw switch, with two possible states dependent on a control input. (*See supra* Section IX.A.3(c); Ex. 1002, ¶106; *see*

*also* Ex. 1002, ¶¶34-37 (discussing multiplexers).) As discussed above, *Kim* discloses selecting a first switch position, where the output (Q) corresponds to the input (B) when the feedback clock signal follows the input clock signal within 180° (which corresponds to the phase detector outputting DET='0' as discussed above for limitation 13(c)). (*See supra* Section IX.A.3(c); Ex. 1002, ¶106; *see also* Ex. 1002, ¶¶34-37 (discussing multiplexers.) *Kim* further discloses selecting a second switch position, where the output (Q) corresponds to the input (F), when the chip clock signal CCLK ("feedback clock signal") does not follow the system clock signal SCLK ("input clock signal") within 180° (which corresponds to the phase detector outputting DET='1' as discussed above for limitation 13(c)). (*See supra* Section IX.A.3(c); Ex. 1002, ¶106; *see also* Ex. 1002, ¶¶34-37.)

The second switch position is shown below corresponding to connecting the input on (F) to the output (Q) ("selecting a second switch position") when the chip clock signal (CCLK) leads the system clock signal (SCLK) and DET='1' (which is equivalent to CCLK trailing SCLK by more than 180°) ("when the feedback clock signal does not follow behind the input clock signal within 180°"). (*See supra* Section IX.A.3(b); Ex. 1002, ¶107; see also Ex. 1002, ¶¶25-31 (discussing clock signals in digital circuits), 34-37 (discussing multiplexers).)




(Ex. 1002, ¶107, citing Ex. 1009, FIG. 4 (excerpted and annotated).)

Thus, *Kim* discloses that when phase detector 202 determines that the chip clock signal (CCLK) leads the system clock signal (SCLK), or equivalently, trails SCLK by more than 180° (i.e., the feedback clock signal does not follow the input clock signal within 180°), the phase detector 202 outputs a '1' on its DET output signal to the "S" input of the synchronization multiplexers 8, 11, and 14. (Ex. 1002, ¶108.) As a result, the synchronization multiplexers output their respective (F) inputs as their (Q) outputs by selecting a second switch position. (*Id.*, ¶108; *see also id.*, ¶¶34-37.)

## X. THE BOARD SHOULD INSTITUTE BOTH PETITIONS FOR THE '507 PATENT

Petitioner is filing another IPR petition challenging claims 10, 12, 13, and 15 of the '507 patent concurrently with the filing of this petition. However, Petitioner's proposed grounds for institution in the two petitions are based on different prior art references. For instance, the primary reference at issue here (*Kim*) is not utilized as prior art for the other petition. The references utilized in the other IPR petition, i.e., *Jefferson* (U.S. Patent No. 5,744,991) and *Donnelly* (U.S. Patent No. 5,945,862) disclose a different configuration for the delay locked loop compared to *Kim*. For instance, while *Kim* discloses a "shift register," *Donnelly* discloses an up/down counter in the delay locked loop. Similarly, Jefferson discloses an exclusive OR gate, which discloses the claimed first and second switch position, while in *Kim* a multiplexer discloses the claimed functionality. Accordingly, Petitioner respectfully requests that the Board adopt all proposed grounds in both petitions.

## XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 10, 11, 13, and 15 of the '507 patent based on the ground specified in this petition.

Respectfully submitted,

Dated: May 12, 2017 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

## CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,069,507 contains, as measured by the word-processing system used to prepare this paper, 9,372 words. This word count excludes the Table of Contents, Table of Authorities, List of Exhibits, Certificate of Compliance, and Certificate of Service.

Respectfully submitted,

Dated: May 12, 2017

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

**CERTIFICATE OF SERVICE**

I hereby certify that on May 12, 2017, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,069,507 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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