Paper No. ___
Filed: May 12, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,069,507

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,069,507

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Page(s)

Cases

Statutes

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 6,069,507
Ex. 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex. 1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex. 1004	Prosecution History of U.S. Patent No. 6,069,507
Ex. 1005	U.S. Patent No. 5,945,862 to Donnelly et al. ("*Donnelly*")
Ex. 1006	U.S. Patent No. 6,292,040 to Iwamoto et al. ("*Iwamoto*")
Ex. 1007	U.S. Patent No. 5,744,991 to Jefferson et al. ("*Jefferson*")
Ex. 1008	Baker, R. J., CMOS Circuit Design, Layout, and Simulation, First Edition, IEEE Press ("*Baker*")

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 10, 11, 13, and 15 of U.S. Patent No. 6,069,507 ("the '507 patent") (Ex. 1001), which, according to PTO records, is assigned to ProMOS Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

Related Matters: Patent Owner has asserted the '507 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al.*, No. 1:16-cv-00335-SLR (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 6,172,554 ("the '554 patent"), 7,375,027 ("the '027 patent"), 6,208,574 ("the '574 patent"), 6,559,044 ("the '044 patent"), and 6,562,714 ("the '714 patent") in this action. Petitioner is concurrently filing another IPR petition challenging claims 10, 11, 13, and 15 of the '507 patent as well as additional IPR petitions challenging certain claims of the '554, '027, '574, '044, and '714 patents. Petitioner also previously filed several IPR petitions involving additional patents asserted by Patent Owner in *ProMOS Technologies, Inc. v. Samsung Electronics*

Co., Ltd. et al., No. 1:15-cv-00898-SLR-SRF (D. Del.). Specifically, on October 7, 2016, Petitioner filed IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. All of these proceedings were instituted and remain pending except for the 00033 and 00035 proceedings.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the ’507 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 10, 11, 13, and 15 ("challenged claims") of the '507 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable in view of the following grounds:

Ground 1: Claims 10 and 11 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,945,862 ("*Donnelly*") (Ex. 1005) and U.S. Patent No. 6,292,040 ("*Iwamoto*") (Ex. 1006); and

Ground 2: Claims 13 and 15 are unpatentable under pre-AIA 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,744,991 ("*Jefferson*") (Ex. 1007).

The '507 patent issued from U.S. Application No. 09/083,790 ("the '790 application") filed May 22, 1998. (Ex. 1001, Cover.) The '790 application does not claim priority to any earlier filed applications.

Donnelly issued on August 31, 1999 from U.S. Patent Application No. 08/904,203 filed July 31, 1997. *Iwamoto* issued on September 18, 2001 from U.S. Patent Application No. 09/047,375 filed March 25, 1998. *Jefferson* issued on April 28, 1998 from U.S. Patent Application No. 543,420 filed October 16, 1995.

Thus, *Donnelly*, *Iwamoto*, and *Jefferson* qualify as prior art at least under pre-AIA 35 U.S.C. § 102(e) with respect to the ’507 patent.

None of the references relied upon in this Petition, except for *Jefferson*, were considered by the Patent Office during prosecution of the ’507 patent. (*See generally* Ex. 1001, References Cited.) *Jefferson* was considered by the Patent Office during prosecution, but Petitioner presents *Jefferson* in a new light never considered by the Office. (*See infra* Section IX.B.) For example, the prosecution history of the ’507 patent does not include any substantive discussion of *Jefferson* relating to patentability of the ’507 patent claims. Although the Examiner stated that *Jefferson* “is considered pertinent to applicant’s disclosure,” *Jefferson* was “not relied upon” for any claim rejections. (Ex. 1004, 47 (Office Action dated September 9, 1999).) Here, Petitioner presents testimony from R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the ’507 patent, who confirms that the relevant teachings of *Jefferson* disclose what is claimed by challenged claims 13 and 15 of the ’507 patent. (*See* Ex. 1002.) As such, consideration of *Jefferson* by the Patent Office during prosecution of the ’507 patent should not preclude the Board from considering and adopting the ground in this petition that involves *Jefferson*.

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '507 patent ("POSITA"), which for purposes of this proceeding is the mid-to-late 1990s (including May 22, 1998, the filing date of the U.S. Application maturing into the '507 patent), would have had at least a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design. (Ex. 1002, ¶¶18-19.)[1] More education can supplement practical experience and vice versa. (*Id*.)

VII. OVERVIEW OF THE TECHNOLOGY, '507 PATENT, AND PRIOR ART

A. The '507 Patent

The '507 patent issued from U.S. Application No. 09/083,790 filed on May 22, 1998 and is entitled "Circuit and Method for Reducing Delay Line Length in Delay-Locked Loops." (Ex. 1001, Cover.) The '507 patent relates to "delay-locked loops (DLLs) and more particularly to reducing delay line length in DLLs." (*Id*., 1:7-9.)

The '507 patent acknowledges that delay locked loops (DLLs) were known as a way to provide "clock deskew functionality," i.e., to address the problem of

[1] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '507 patent. (Ex. 1002, ¶¶1-13; Ex. 1003.)

clock skew. (*Id.*, 1:12-13; Ex. 1002, ¶¶41-43, 25-31, 35-36.) The '507 patent describes "a typical digital DLL" with respect to figure 1, which is labeled "PRIOR ART."

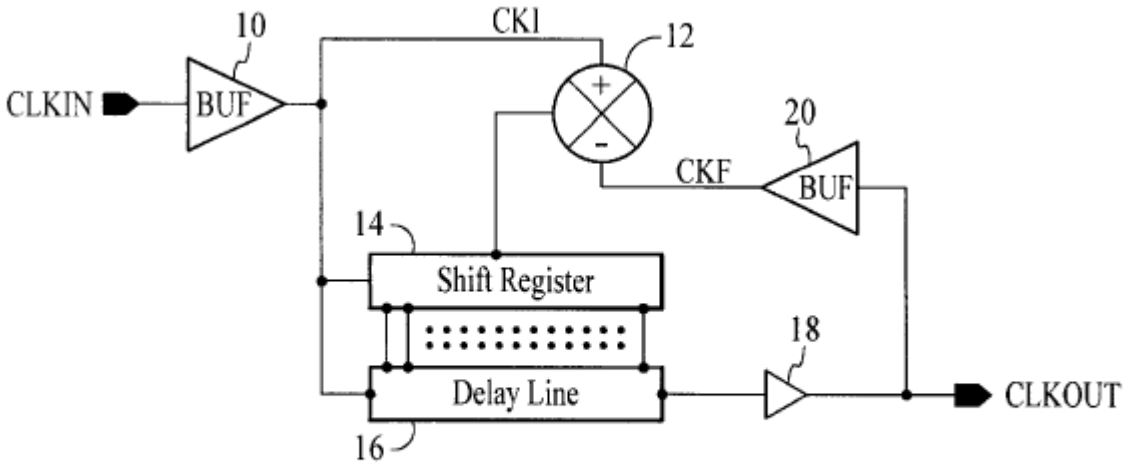


FIG. 1
(PRIOR ART)

(Ex. 1001, FIG. 1; *see also id.*, 1:20-33.)

The '507 patent states that "a need exists for more elegant and cost effective solutions to reducing delay line length in DLLs." (*Id.*, 1:54-55.) "FIG. 2 illustrates a digital DLL 24 in accordance with the present invention." (*Id.*, 2:49-50.)

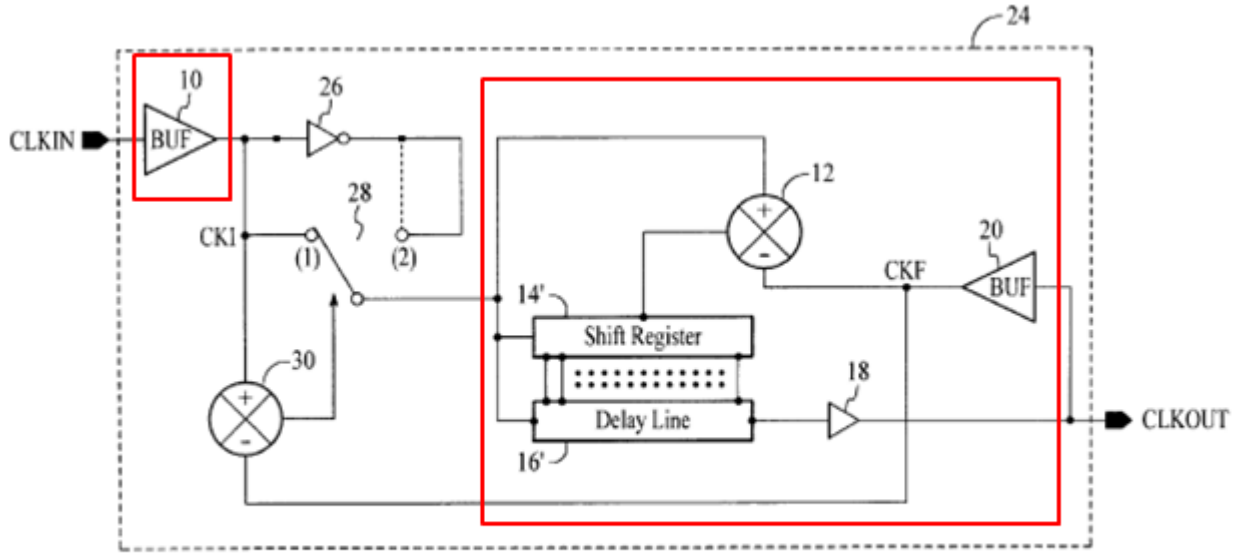


FIG. 2

(Ex. 1002, ¶¶44-46, citing Ex. 1001, FIG. 2 (annotated in red to show components found in the prior art DLL of figure 1).)

The ’507 patent states with reference to figure 2 that “[l]ike components to those shown in FIG. 1 have been numbered similarly,” and a comparison of figures 1 and 2 shows that the entire right side of figure 2 and the buffer (BUF) 10 (both annotated above in red) are found in the prior art DLL of figure 1. As stated by the ’507 patent, these components of figure 2 and their functionality were “well understood by those skilled in the art.” (Ex. 1001, 1:29-33.) The ’507 patent discloses that “the DLL 24 [of figure 2] further includes an inverter 26, a switch 28, and a second phase detector 30” and that “[t]hrough the arrangement of the

DLL 24, the length of the delay line 16' and correspondingly the number of cells in the shift register 14' are reduced." (*Id.*, 2:55-60.)

The above features were well known as discussed below at Sections VII.B-D and IX. (Ex. 1002, ¶47.)

B. *Donnelly*

Donnelly generally relates to "[c]ircuitry for adjusting the delay of a clock signal," including "circuitry [which] is suitable for use in a delay locked loop for controlling the amount of delay adjustment to the clock signal." (Ex. 1005, Title, 1:5-9.) It was known at the time of *Donnelly* to "provid[e] a 360° adjustable delay to an incoming periodic signal [using] a tapped delay line shown in FIG. 1." (*Id.*, 1:11-13; Ex. 1002, ¶49.)

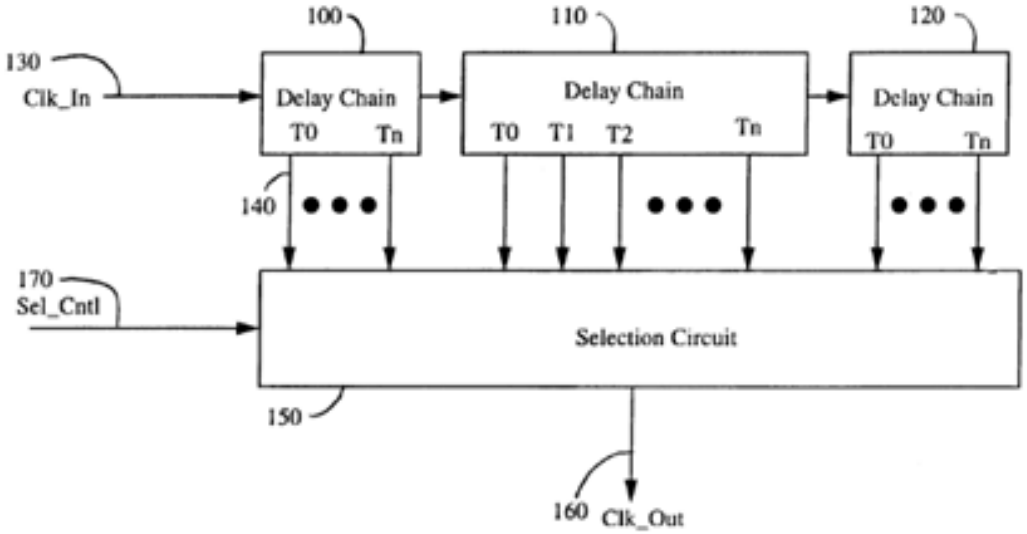


FIG_1

PRIOR ART

(Ex. 1005, FIG. 1; *see also id.*, 1:13-29; Ex. 1002, ¶¶49-50.)

A drawback of the approach of figure 1 is that "if the delay chosen is equal to the input or output tap of chain 110, delay chains 100 and 120, each spanning at least half a period of the incoming signal, must be added to the beginning and the end of chain 110 to cover adjustments less than 0° and greater than 360°[, resulting in] a delay chain which has a large number of delay elements." (Ex. 1005, 1:38-43; *see also id.*, 2:1-4; Ex. 1002, ¶51.)

Donnelly discloses that "[f]or these and other reasons it is desirable to have a technique of producing a 360° adjustable delay to an incoming periodic signal that has a small number of delay elements with better resolution than a simple tapped delay line." (Ex. 1005, 2:12-16.) Accordingly, *Donnelly* discloses with reference to figures 2-5 an improved technique for adjusting the delay of a clock signal. (*Id.*, 2:62-3:6, 3:37-6:9; Ex. 1002, ¶52.) *Donnelly* discloses at figure 5 a delay locked loop, which includes a phase detector 610, up-down counter 620, and block 500 labeled "Delay Chains[,] Selectors, and Blenders." (Ex. 1005, 5:32-34 ("FIG. 5 further shows phase detector 610 and up-down counter 620 connected to form a delay locked loop."), FIG. 5; Ex. 1002, ¶52, 60-61.)

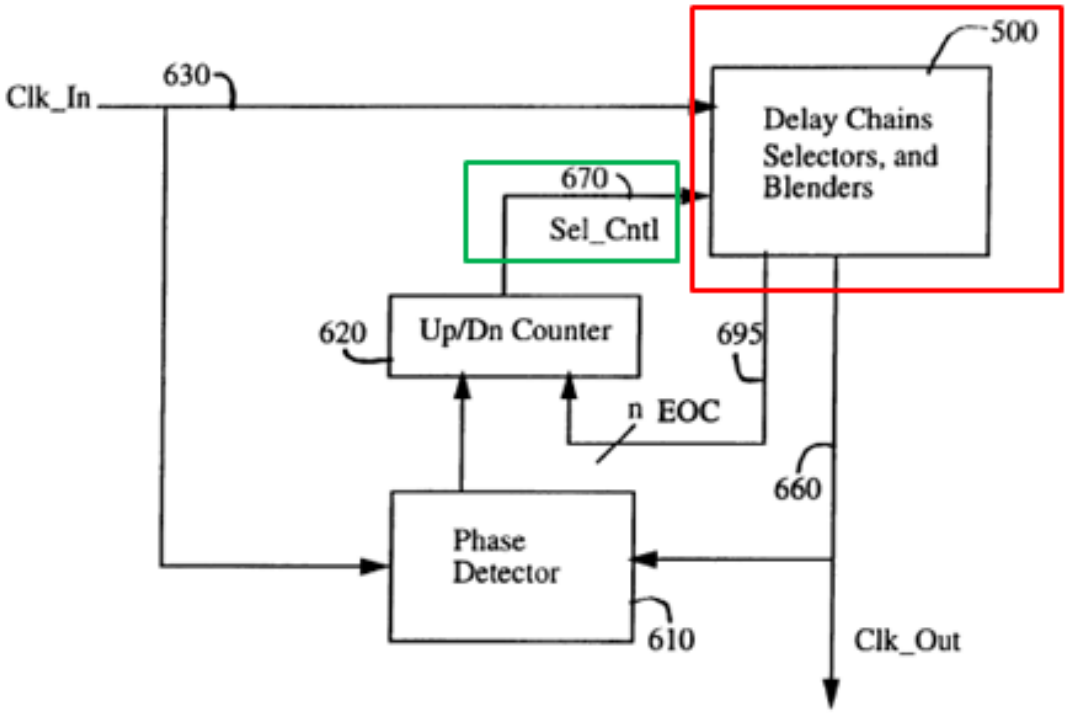


FIG_5

(Ex. 1002, ¶52, citing Ex. 1005, FIG. 5 (annotated to show circuit block 500 in red and its input Sel_Cntl in green).)

Donnelly discloses that any of the circuits shown in figures 2-4 can be used to implement block 500 of figure 5, which is annotated in red above. (Ex. 1005, 3:4-6, 5:30-32; Ex. 1002, ¶53.) In other words, figures 2 through 4 disclose different techniques for providing a delay that is specified by the Sel_Cntl input shown above in green. (Ex. 1005, FIG. 5; Ex. 1002, ¶53)

Figure 2 of *Donnelly* discloses a delay technique "in which a boundary detector is employed to detect the boundaries of the delay chain." (Ex. 1005, 2:62-

64; *see also id.*, 3:37-40; Ex. 1002, ¶54.)

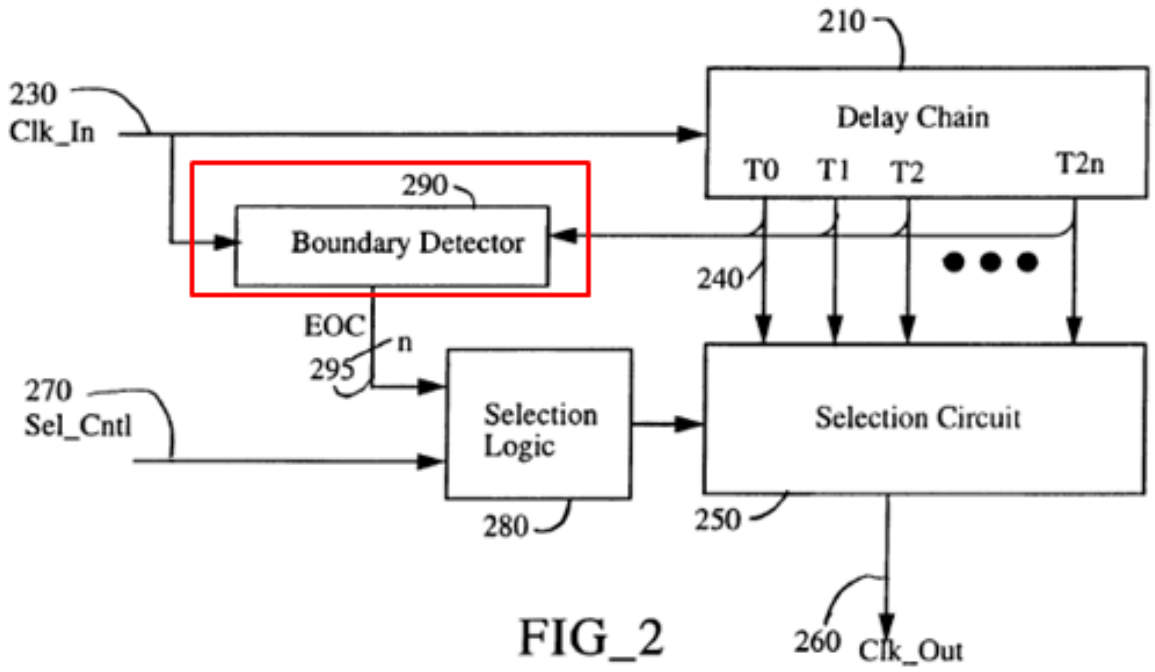


FIG_2

(Ex. 1002, ¶54, citing Ex. 1005, FIG. 2 (annotated to show boundary detector 290).)

Donnelly discloses that because of the boundary detector, "**only 32 delay elements (instead of 64) are required** given the above example discussed in connection with FIG. 1." (Ex. 1005, 3:37-61 (emphasis added); Ex. 1002, ¶55.)

Thus, an advantage that *Donnelly*'s technique of figure 2 provides over the conventional approach of figure 1 is that fewer (in particular, only one-half as many) delay elements are needed, achieving *Donnelly*'s goal of achieving "a small number of delay elements." (Ex. 1005, 2:14-15; Ex. 1002, ¶56.) This is the same benefit (reducing the number of delay elements) that the '507 patent claims as a

feature. (*See supra* Section VII.A, *infra* Section IX.A.1(e); Ex. 1002, ¶56.)

Donnelly describes with reference to figure 3 a further improved delay technique that adds to the circuit of figure 2 a blender circuit 375 (annotated below in red) which uses interpolation to provide improve resolution. (Ex. 1005, 4:1-7, FIG. 3; Ex. 1002, ¶57-58.)

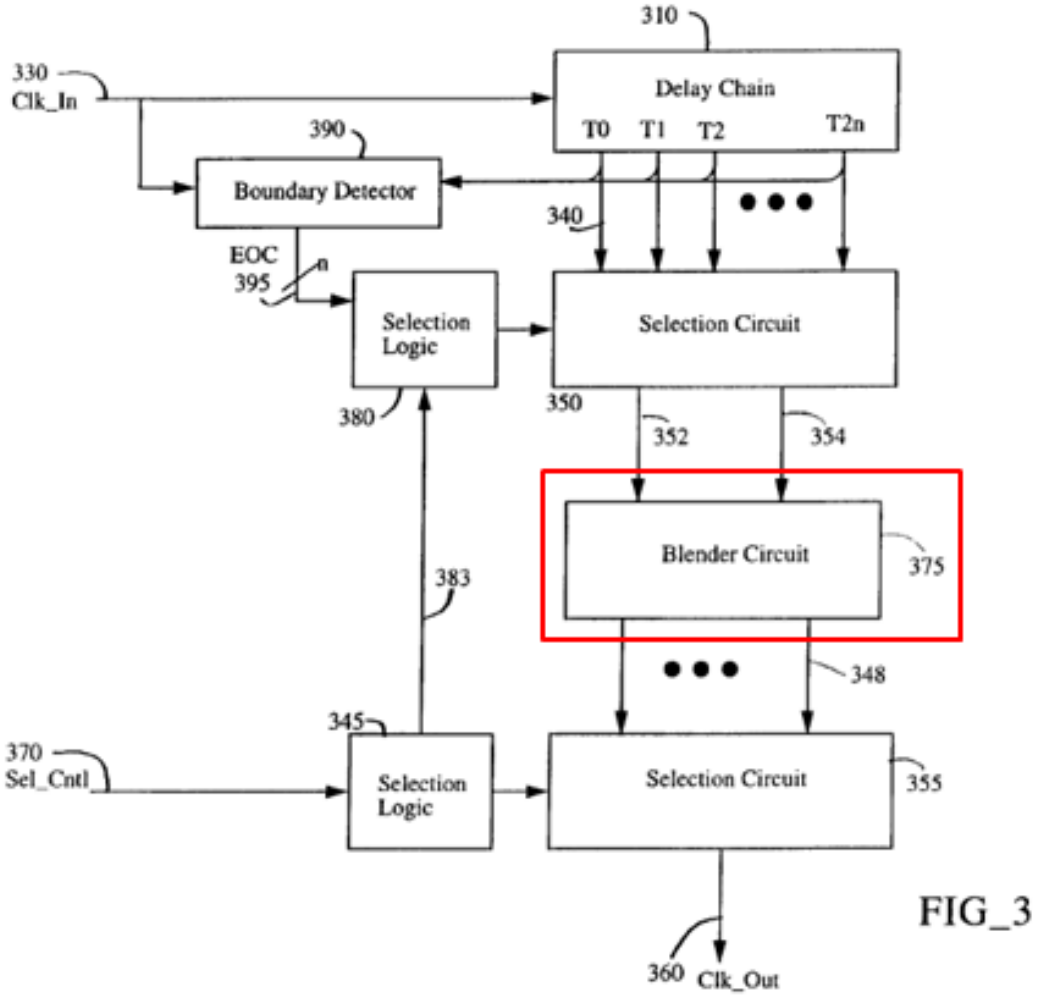


FIG_3

(Ex. 1002, ¶57, citing Ex. 1005, FIG. 3 (annotated to show blender circuit 375).)

Donnelly discloses an additional delay technique with respect to figure 4 that "further improves the resolution of the circuit again by using a pair of delay chains

410 and 510, each chain being constructed from inverting delay elements." (*Id.*, 4:28-30; Ex. 1002, ¶59.)

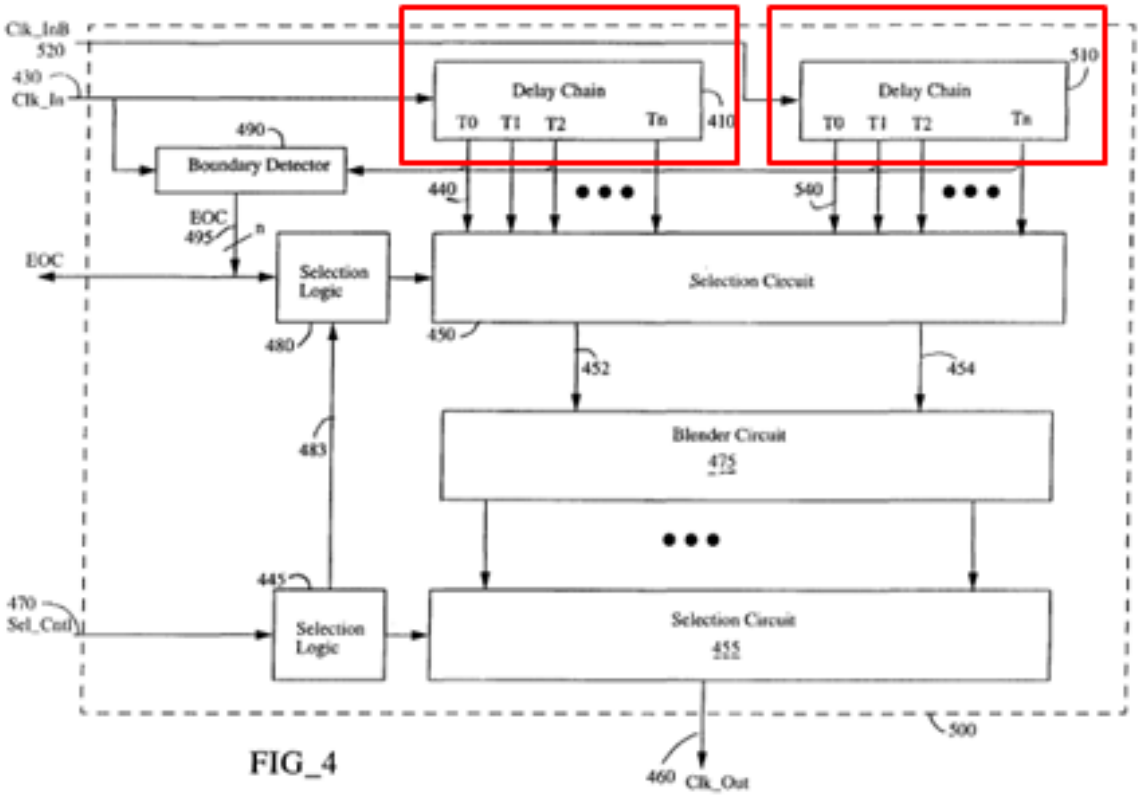


FIG_4

(Ex. 1002, ¶59, citing Ex. 1005, FIG. 4 (annotated).)

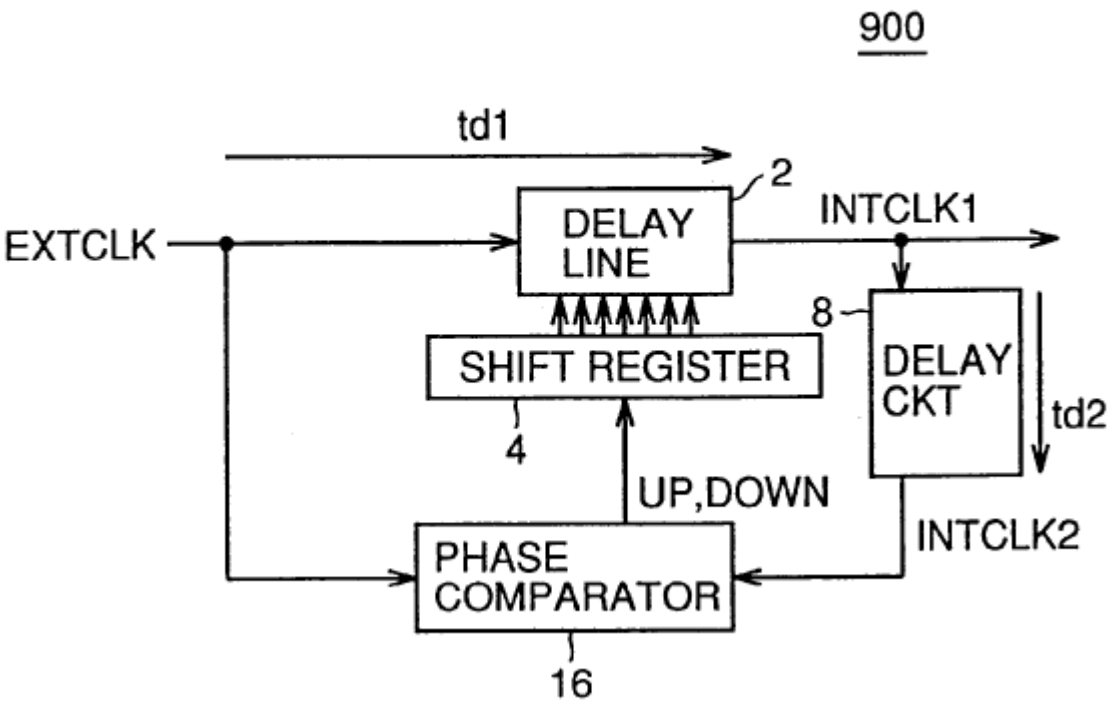
C. *Iwamoto*

Iwamoto, which is in the same field as *Donnelly* (namely, circuits and in particular, providing a clock signal using a delay locked loop), describes various aspects of delay locked loop (DLL) circuits. (Ex. 1002, ¶62.) *Iwamoto* explains that DLL circuits were known at the time of *Iwamoto*. (Ex. 1006, 1:24-29 ("To meet the demand of higher internal clock signals, a delay lock loop (hereinafter

referred to as DLL circuit) has been proposed as an internal clock signal generating circuit which receives an externally applied clock signal (external clock signal) and generates an internal clock signal which is in synchronization with the external clock signal."); Ex. 1002, ¶62.)

Iwamoto discloses a DLL circuit 900 with respect to figure 17. (Ex. 1006, 7:17-18 ("FIG. 17 is a schematic block diagram showing a basic structure of a conventional DLL circuit 900.").)

FIG.17 PRIOR ART



(*Id.*, FIG. 17; *see also id.*, 1:32-47; Ex. 1002, ¶63-64.)

Like *Donnelly*, *Iwamoto* discloses performing a phase comparison and adjusting the amount of delay applied to a clock signal (EXTCLK) accordingly.

(Ex. 1006, FIG. 17; Ex. 1002, ¶65.)

D. *Jefferson*

Jefferson is entitled "System for distributing clocks using a delay lock loop in a programmable logic circuit" and "relates generally to clock distribution in integrated circuits and specifically to a clock distribution scheme using a delay lock loop." (Ex. 1007, Title, 1:6-8; Ex. 1002, ¶66.)

Jefferson discloses that "[t]he present invention applies [to] digital delay lock loops (DDLL) . . . ." (Ex. 1007, 7:53-56.) "An example of an embodiment with DDLL is described" with respect to figure 4, which "shows a digital DLL (DDLL) block diagram using macro and micro phase detectors." (*Id.*, 7:55-58; *see also id.*, 2:45-46.) *Jefferson* discloses that the macro phase detector 202 (annotated in red below) "can be implemented by a circuit similar to that of FIG. 3A." (*Id.*, 8:1-2.)

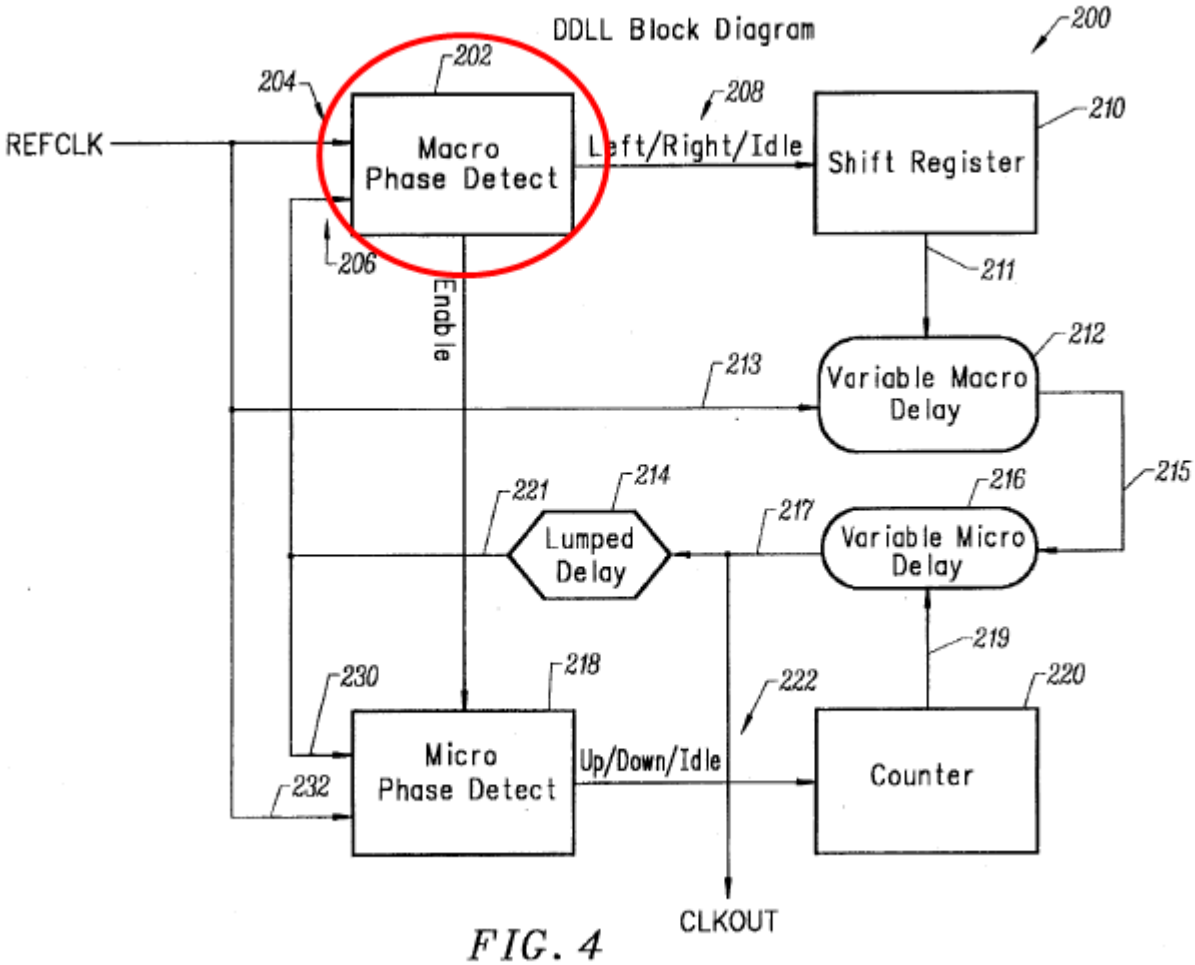


FIG. 4

(Ex. 1002, ¶73, citing Ex. 1007, FIG. 4 (annotated to show macro phase detector 202 in red).)

Jefferson discloses that "FIG. 3A is a diagram of a circuit for achieving the PFD function shown in FIG. 1D's PFD 106." (Ex. 1007, 6:47-48; Ex. 1002, ¶¶67-71.)

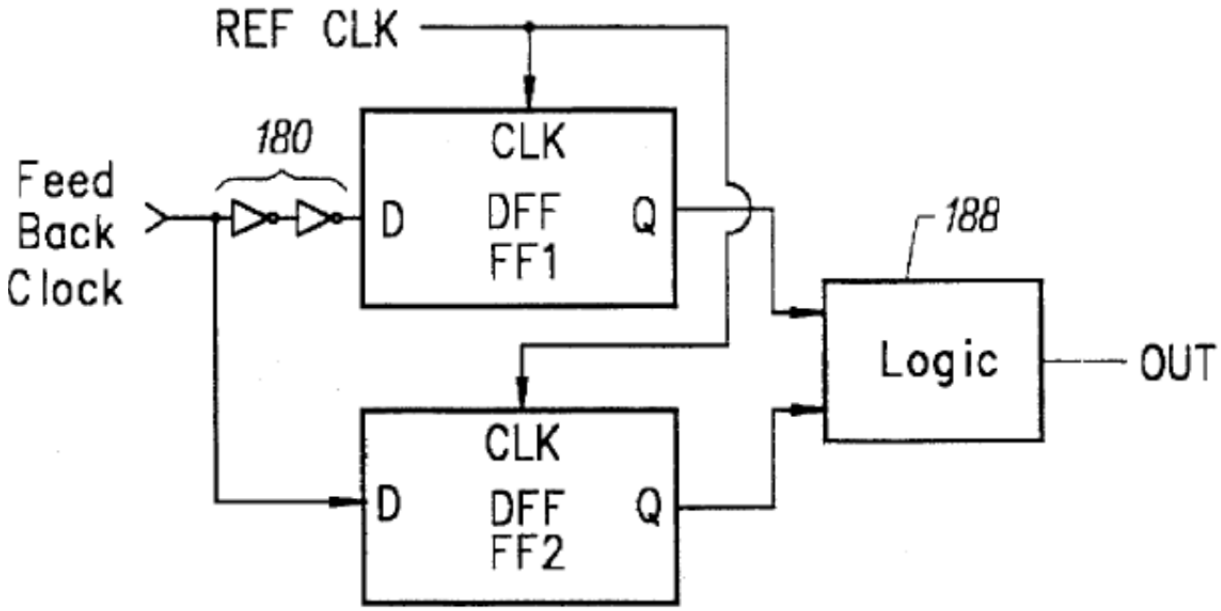


FIG. 3A

(Ex. 1007, FIG. 3A.)

Jefferson discloses that the combinational logic 188 (shown above in orange) can be implemented as a 2-input exclusive OR (XOR) gate. (Ex. 1007, 7:14-18; Ex. 1002, ¶72.)

VIII. CLAIM CONSTRUCTION

Should the Board institute *inter partes* review, the '507 will expire on May 22, 2018, *i.e.*, during the pendency of the instituted proceeding. Accordingly, the claims of the '507 patent should be construed under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). *See, e.g.*, *Square Inc. v. J. Carl Cooper*, IPR2014-00156, Paper No. 38 at 7 (May 14, 2015)

(citing *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)). Under *Phillips*, claim terms are given their ordinary and customary meanings, as would be understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *See, e.g., Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 20 at 2-3 (July 10, 2014).

The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2014-00633, Paper No. 11 at 16 (August 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner submits that for purposes of this proceeding, the terms of the challenged claims should be given their ordinary and customary meaning consistent with *Phillips*.[2] (Ex. 1002, ¶48.)

[2] Petitioner does not concede that the challenged claims are not invalid under one or more sections of 35 U.S.C. § 112, which is something that cannot be pursued in this proceeding under the Rules.

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: *Donnelly* and *Iwamoto* Render Obvious Claims 10 and 11

1. Claim 10

a) A method for reducing delay line length in a digital delay locked loop (DLL), the method comprising:

To the extent the preamble is limiting, *Donnelly* discloses this feature. (Ex. 1002, ¶¶75-87.) For example, the circuitry depicted in figure 5 of *Donnelly* is a digital delay locked loop. (*Id.*, ¶77.) "FIG. 5 . . . shows phase detector 610 and up-down counter 620 connected to form a **delay locked loop**." (Ex. 1005, 5:32-34, emphasis added.)

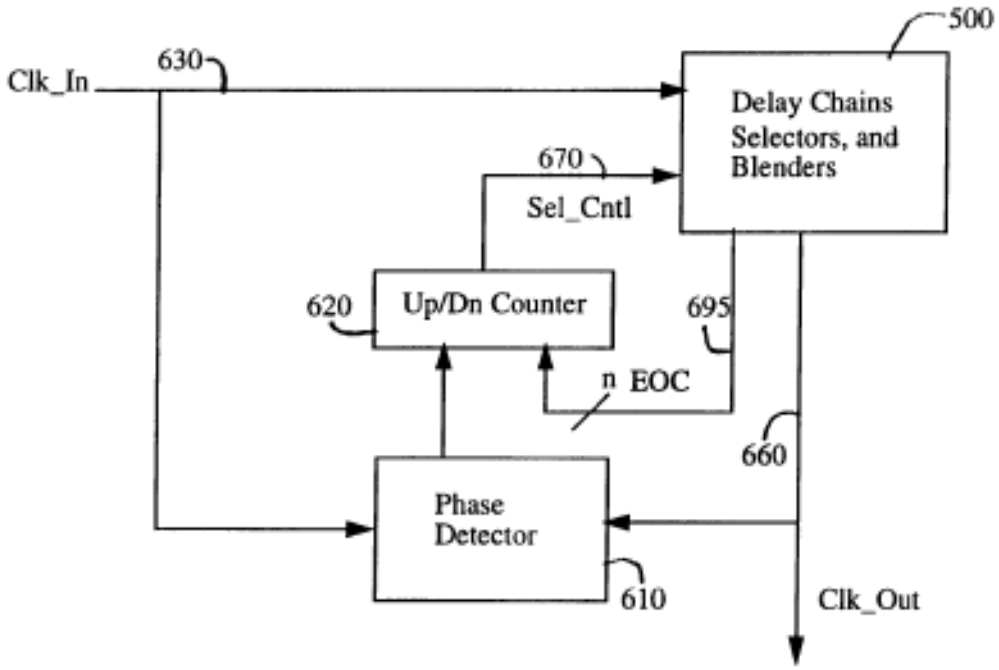


FIG_5

(*Id.*, FIG. 5.)

The delay locked loop in figure 5 of *Donnelly* uses digital devices to implement the variable delay line in the delay locked loop and therefore would have been understood by a person of ordinary skill in the art ("POSITA") to be a "digital" delay locked loop, as recited in claim 10(a). (Ex. 1002, ¶78.) For instance, while the figure 5 delay locked loop includes a phase detector 610 and up/down (up/dn) counter 620, it also includes block 500, which is described in figure 4. (Ex. 1005, 5:30-34; Ex. 1002, ¶78.) The circuitry of figure 4 includes a pair of delay chains 410 and 510, "each chain being constructed from inverting delay elements" where "each delay element . . . [is] a single inverter." (Ex. 1005, 4:28-40.) A POSITA would have known that an inverter is a digital logic gate. (Ex. 1002, ¶78; *see also id.*, ¶¶21-24.)

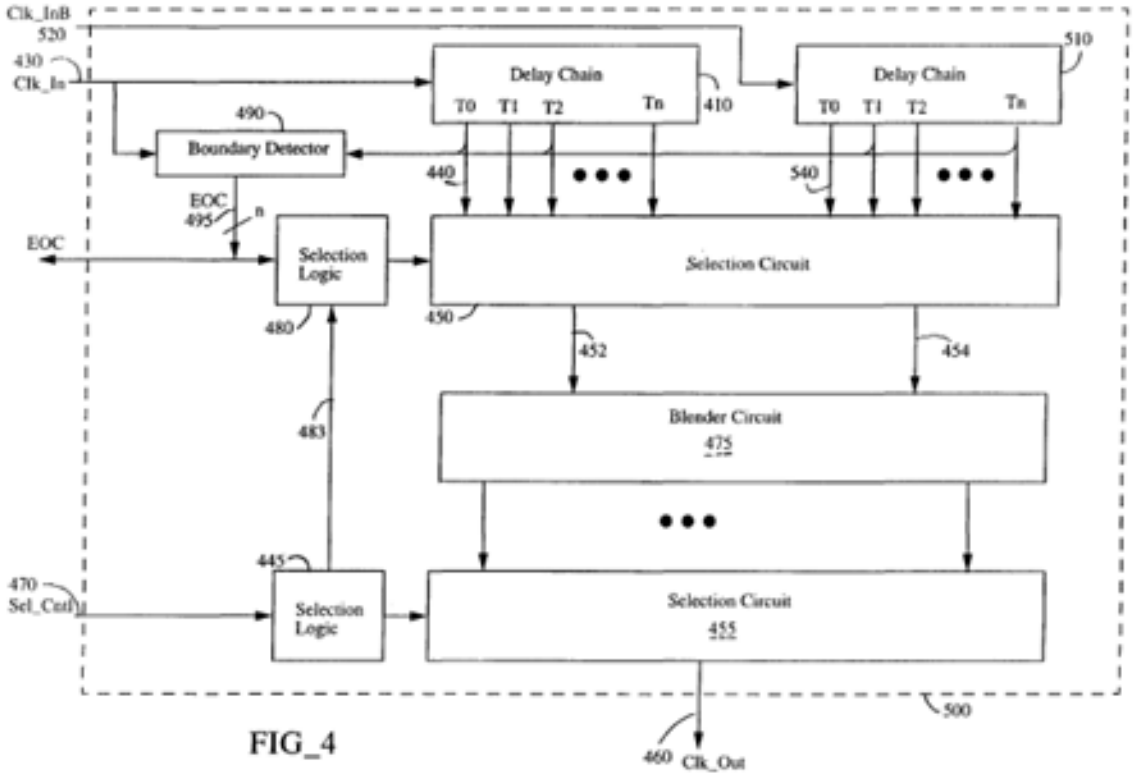


FIG_4

(Ex. 1005, FIG. 4.)

Moreover, digital circuitry is used in the control of the delay locked loops in *Donnelly*, e.g., where a counter is used to select one or more of the taps in the delay chain for use in generating the output clock signal. (Ex. 1002, ¶79.) For instance, *Donnelly* discloses that "[t]he polarity of the phase error [determined by phase detector 610] instructs up/down counter 620 to increase or decrease its count value and the count value is used to derive a suitable Sel-Cntl signal 670." (*Id.*; Ex. 1005, 5:36-38.) The select control signal (Sel-Cntl) 670 is received by

selection logic that determines which tap(s) are selected for the output clock signal. (*See* Ex. 1005, 5:45-48; Ex. 1002, ¶79.)

Donnelly also discloses "a method for reducing delay line length [in a digital DLL]" because the number of delay elements in the delay chain illustrated in figure 4 (which is part of the DLL of figure 5) is half of the number of delay elements in the prior art delay chain discussed with reference to figure 1. (Ex. 1002, ¶80.) Specifically, as explained below, *Donnelly* discloses that the total number of delay elements obtained by adding the delay elements in delay chains 410 and 510 is 32, which is half of the total number of delay elements (64) in the delay chain disclosed with reference to figure 1. (*Id.*)

Donnelly notes that prior art delay locked loops required a large number of delay elements in order to fully cover the adjustments needed between the input clock signal and output clock signal. (Ex. 1005, 1:38-43; Ex. 1002, ¶81.) Specifically, *Donnelly* notes that prior art figure 1 has three delay chains (100, 110, and 120) having "64 inverting delay elements." (Ex. 1005, 1:44-54.) *Donnelly* notes that, among other disadvantages of the prior art circuit of figure 1, the large number of delay elements "take up a good deal of space and consume significant power." (*Id.*, 2:2-4; Ex. 1002, ¶81.) *Donnelly* then states that "[f]or these and other reasons, it is desirable to have a technique of producing a 360° adjustable

delay to an incoming periodic signal that has a small number of delay elements with better resolution than a simple tapped delay line." (Ex. 1005, 2:12-16.)

Donnelly discloses a technique by which the number of delay elements in the delay chain is reduced from 64 (in prior art figure 1) to 32 in the circuit of figure 4. (Ex. 1002, ¶82.) While the reduction in the number of delay elements from 64 to 32 is discussed with respect to figure 2, *Donnelly* explains that figure 4 is merely a variation of the circuit of figure 2 and retains the number of delay elements at 32. (*Id.*) Therefore, *Donnelly*'s disclosure regarding figure 2 is first explained below.

In order to reduce the number of delay elements in the delay chain, *Donnelly* includes the boundary detector 290 shown in figure 2. (*Id.*, ¶83.) The boundary detector is used "to detect the boundaries of the delay chain." (Ex. 1005, 2:63-64; *see also id.*, 3:37-40; Ex. 1002, ¶83.)

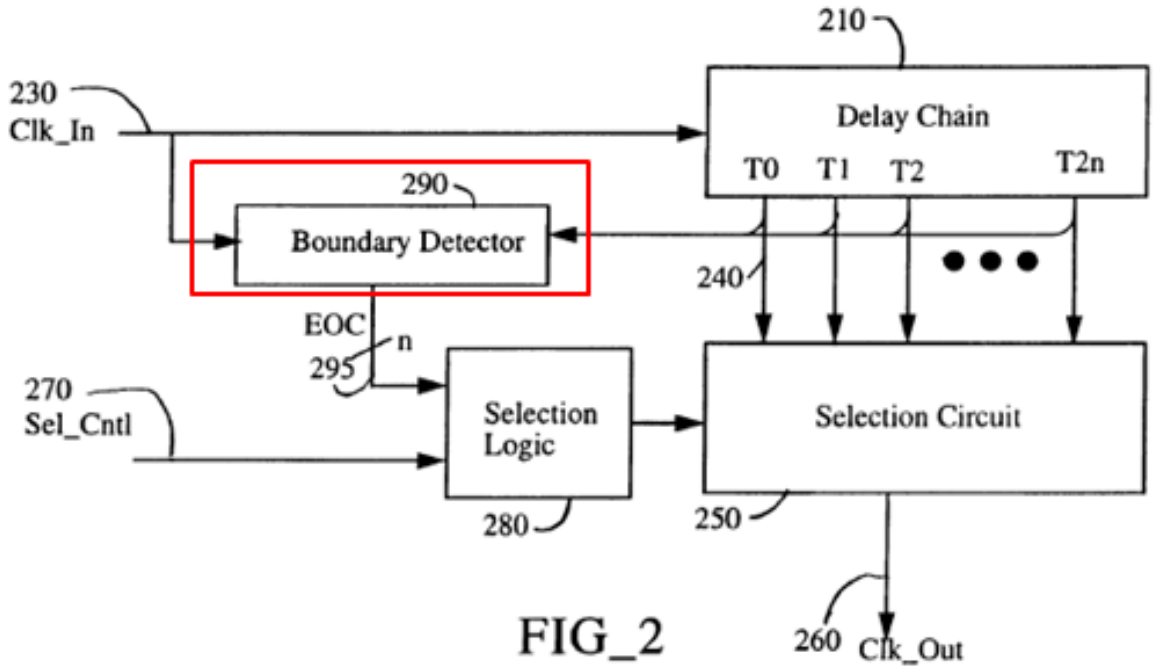


FIG_2

(Ex. 1002, ¶83, citing Ex. 1005, FIG. 2 (annotated to show boundary detector 290).)

Donnelly notes that the inclusion of the boundary detector allows the number of delay elements used in the delay chain to be cut in half. (Ex. 1002, ¶84.) "Assuming that taps 240 have the same polarity and pairs of inverters are used between taps, **only 32 delay elements (instead of 64) are required** given the above example discussed in connection with FIG. 1." (Ex. 1005, 3:58-61 (emphasis added); Ex. 1002, ¶84.) *Donnelly* explains that the boundary detector works with the other components of figure 2 in order to accomplish this reduction

in delay elements, so that "only 32 delay elements (instead of 64) are required." (Ex. 1005, 3:37-61; Ex. 1002, ¶84.)

The reduction in the number delay elements in the delay chain from 64 in the prior art discussed in figure 1 to 32 in the circuit of figure 2 constitutes "reducing delay line length" as recited in claim 10. (Ex. 1002, ¶85.) The delay elements in a delay chain are coupled in series to form a line, and reducing the number of delay elements in such a delay chain reduces the length of the delay chain. (*Id.*) Indeed, *Donnelly*'s goal of achieving "a small number of delay elements" (Ex. 1005, 2:14-15), which is facilitated by the inclusion of a boundary detector, is the same benefit (reducing the number of delay elements) that the '507 patent claims as a feature. (Ex. 1002, ¶85.)

While the discussion directly above is in the context of figure 2, *Donnelly* explains that figure 4 is a variation of figure 2 where the number of delay elements is maintained at 32. (*Id.*, ¶86.) For instance, *Donnelly* explains that "FIG. 3 improves the resolution obtainable from the circuit in FIG. 2 by adding a blender circuit 375 to selection circuit 350." (Ex. 1005, 4:1-3.) "FIG. 4 further improves the resolution of the circuit again by using a pair of delay chains 410 and 510, each chain being constructed from inverting delay elements." (*Id.*, 4:28-30.) The primary difference between the delay chain in figure 4 and that of figures 2 and 3 is that *Donnelly* splits a single delay chain in figures 2 and 3 (figures 2 and 3 have

the same delay chain) into two delay chains 410 and 510 to obtain better resolution. (Ex. 1002, ¶86.) *Donnelly* confirms this because it states that "[t]he number of delay elements over the pair of chains is the same as with a single chain, but each delay is half as long between pairs of the same type of edges, thus allowing increased blender resolution." (Ex. 1005, 4:42-49; Ex. 1002, ¶86.)

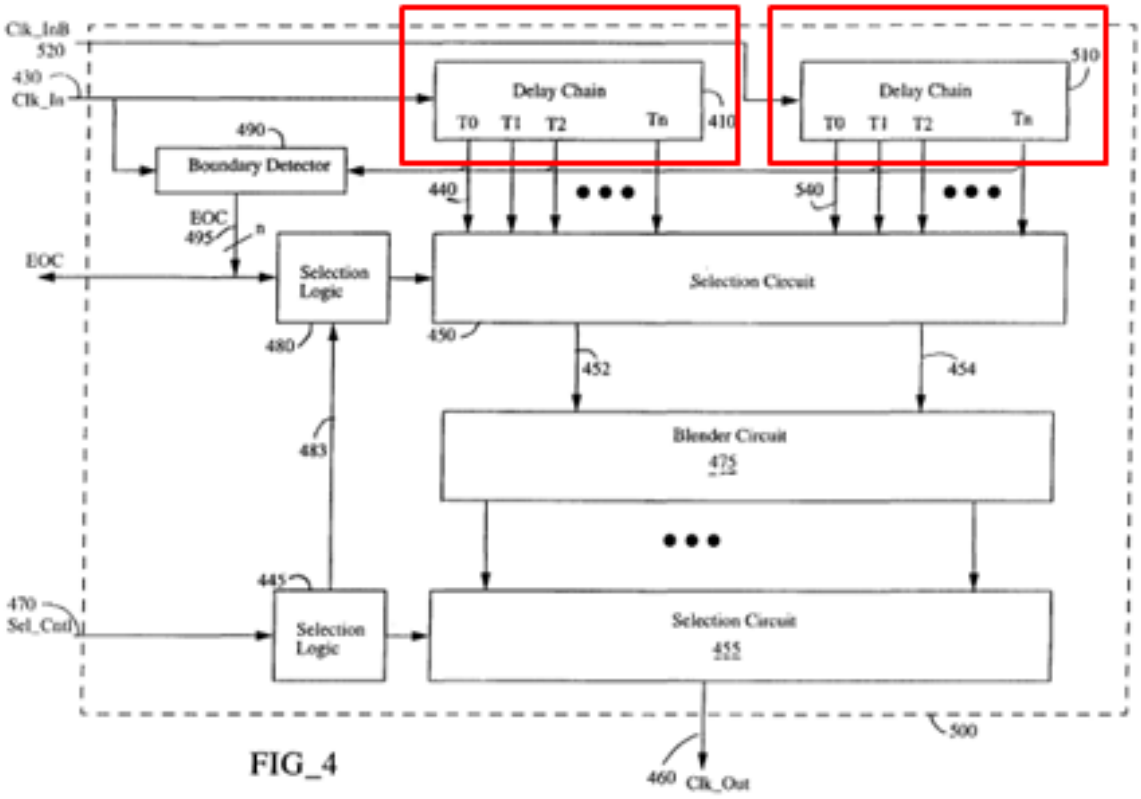


FIG_4

(Ex. 1002, ¶86, citing Ex. 1005, FIG. 4 (annotated).)

In view of the above, *Donnelly* discloses that the number of delay elements in the delay chain of figure 4 (and therefore, in the figure 5 DLL) is reduced to 32 from 64 in the prior art of figure 1. (Ex. 1002, ¶87.)

b) determining a phase difference between an input clock signal and a feedback clock signal;

Donnelly discloses this feature. (Ex. 1002, ¶88.) For instance, *Donnelly* discloses with reference to figure 5 a phase detector 610 that determines a "phase difference between input clock Clk_In 630 and output clock Clk_Out 660." (Ex. 1005, 5:40-43; *see also id.*, 5:32-35 ("FIG. 5 further shows phase detector 610 and up-down counter 620 connected to form a delay locked loop. By **feeding back the Clk_Out 660** and comparing its phase to the phase of **Clk_In 630**, a **phase error is determined**.") (emphasis added).) Thus, input clock Clk_In 630 and output clock Clk_Out 660 read on the claimed "input clock signal" and "feedback clock signal," respectively. (Ex. 1002, ¶88.) Below, the phase detector 610, which determines the phase difference according to limitation 10(b), is annotated in red.

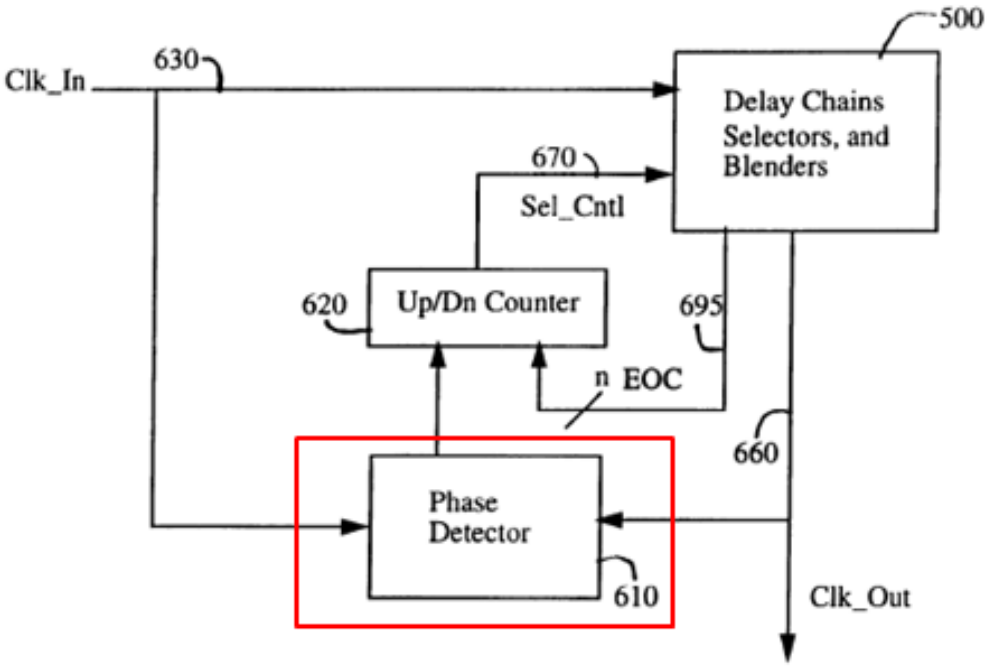


FIG_5

(Ex. 1002, ¶88, citing Ex. 1005, FIG. 5 (phase detector 610 annotated in red); *see also* Ex. 1005, FIG. 6.)

> c) maintaining the phase difference between the input clock signal and the feedback clock signal [within] [3] approximately 180°, including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°; and

Donnelly discloses or suggests this feature. (Ex. 1002, ¶¶89-121.)

"maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°"

As discussed immediately below, *Donnelly* discloses, for example with reference to figure 5, a delay locked loop for maintaining the phase difference between the input clock Clk_In 630 ("input clock signal") and output clock

[3] Petitioner assumes for the purposes of this proceeding that limitation 10(c) contains a printing error and that the phrase "**within** approximately 180°" was intended instead of "approximately 180°." During prosecution, Applicant amended claim 11 (which issued as claim 10) and, as amended, claim 11 recited "**within** approximately 180°." (Ex. 1004, 58, 59 (Amendment dated December 13, 1999) (emphasis added).) In the Notice of Allowance, the Examiner also acknowledged claim 11 as reciting "**within** approximately 180°." (*Id.*, 65 (Notice of Allowance dated January 18, 2000) (emphasis added).) Petitioner reserves the right to assert in district court that claim 10 is invalid under 35 U.S.C. § 112.

Clk_Out 660 ("feedback clock signal") near zero degrees, which is "**within** approximately 180°" (emphasis added). (*Id.*)

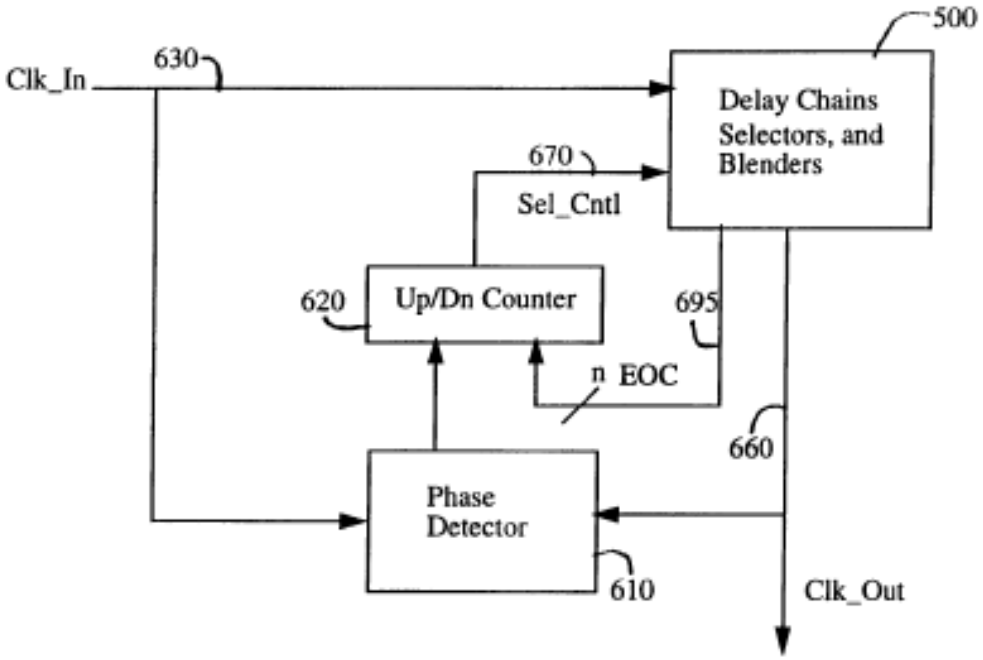


FIG_5

(Ex. 1005, FIG. 5.)

Donnelly describes the circuit in figure 5 as attempting to achieve "phase alignment" between the input clock signal (Clk_In) and the feedback clock signal (Clk_Out), which is shown being fed back to the phase detector 610. (Ex. 1002, ¶91; *see also id.*, ¶90.) Specifically, *Donnelly* states that "[t]he loop in FIG. 5 operates as follows, assuming that the phase difference between input clock Clk_In 630 and output clock Clk_Out 660 is approximately 270° and that the phase

boundary of Clk_In within the delay chain must be crossed **to bring them into phase alignment**." (Ex. 1005, 5:39-43, emphasis added.) *Donnelly* then describes how the circuitry of figure 5 operates in order to bring the output clock Clk_Out and the input clock Clk_In 630 into phase alignment. (*Id.*, 5:43-6:9; Ex. 1002, ¶91; *see also* citations and discussion regarding the operation of the delay locked loop in figure 5 of *Donnelly* at Section VII.B.) A POSITA would have understood "phase alignment" as disclosed by *Donnelly* to correspond to the condition where there is little to no phase difference between the two signals. (Ex. 1002, ¶91.) While perfect phase alignment is achieved when there is zero phase difference between the signals, the limited resolution of the delay elements used in the delay line of the delay locked loop would have impacted the precision with which the signals can be phase aligned. (*Id.*)

Donnelly's explanation of the operation of figure 5 confirms that *Donnelly*'s delay locked loop achieves a high degree of phase alignment. (*Id.*, ¶93.) Assuming that Clk_In and Clk_Out start out misaligned in terms of phase, the phase detector 610 detects such a phase error thereby causing the counter 620 to increment or decrement. (Ex. 1005, 5:34-38; Ex. 1002, ¶93; *see also* Ex. 1002, ¶92.) The count value determines the Sel_Cntl signal 670 (*id.*), which "instructs selection logic 445 in FIG. 4 to switch consecutively through the taps from the

output of the blender circuit **to reduce the phase error**." (Ex. 1005, 5:45-48 (emphasis added); Ex. 1002, ¶93.)

Donnelly discloses that the objective of the DLL, in particular the functionality achieved by the selection logic 445, is to identify a delay tap that is as nearly aligned as possible to the phase of the input clock, i.e., to maintain a zero degree phase difference between input clock Clk_In ("input clock signal") and output clock Clk_Out ("the feedback clock signal"). (Ex. 1005, 5:66—6:1 ("Selection logic 445 then continues to step through the taps from the blender circuit 475 until the blender output tap that is **closest to the phase of the input clock** is found.") (emphasis added); Ex. 1002, ¶94.)

The near zero phase difference between the input clock and the output clock discloses "the phase difference between the input clock signal and the feedback clock signal **within** approximately 180°" because the phase difference is less than 180°. (Ex. 1002, ¶95.) *Donnelly* therefore discloses "maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°" as recited in claim 10. (Ex. 1002, ¶95.)

Donnelly discloses this feature for another reason. (*Id*., ¶96.) Specifically, as discussed above, *Donnelly*'s figure 5 circuit is a delay locked loop that achieves "phase alignment" between Clk_In and Clk_Out. By achieving such "phase alignment," *Donnelly* necessarily discloses that the phase difference between

Clk_In and Clk_Out is "maintain[ed]" approximately within 180° because the phase difference between Clk_In and Clk_out is always within approximately 180° as explained below. (Ex. 1002, ¶96.)

A POSITA would have understood that for two clock signals having the same frequency, and hence the same period, the phase difference between the two clock signals is always within approximately 180°. (Ex. 1002, ¶97.) For example, if the feedback clock signal is lagging the input clock signal by 210°, that is the same as the feedback clock signal leading the input clock signal by 150°. (*Id*.) Therefore, the phase difference between the two clock signals is always less than or equal to 180 degrees, which is "within approximately 180°." (*Id*.)

The output clock (Clk_Out) and the input clock (Clk_In) in *Donnelly* have the same frequency, and hence the same period, as the output clock is simply a delayed version of the input clock. (Ex. 1005, 2:19-21; *see also id.*, 5:39-6:39, FIG. 5; *see infra* Section IX.A.1(d); Ex. 1002, ¶99; *see also* Ex. 1002, ¶98.) Therefore, the phase difference between Clk_In and Clk_out is always within approximately 180° as explained below. (Ex. 1002, ¶99.) Hence, whenever *Donnelly* achieves "phase alignment" between Clk_In and Clk_out, *Donnelly* discloses "maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°" as recited in claim 10. (Ex. 1002, ¶99.)

"including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°"

Donnelly discloses with reference to figure 5 (shown below) that the input clock Clk_In ("input clock signal") is adjusted with a loop comprising phase detector 610 ("a phase detector"), an up/down counter 620, and delay chains 410 and 510 ("delay line") in circuit block 500. (Ex. 1002, ¶100.)

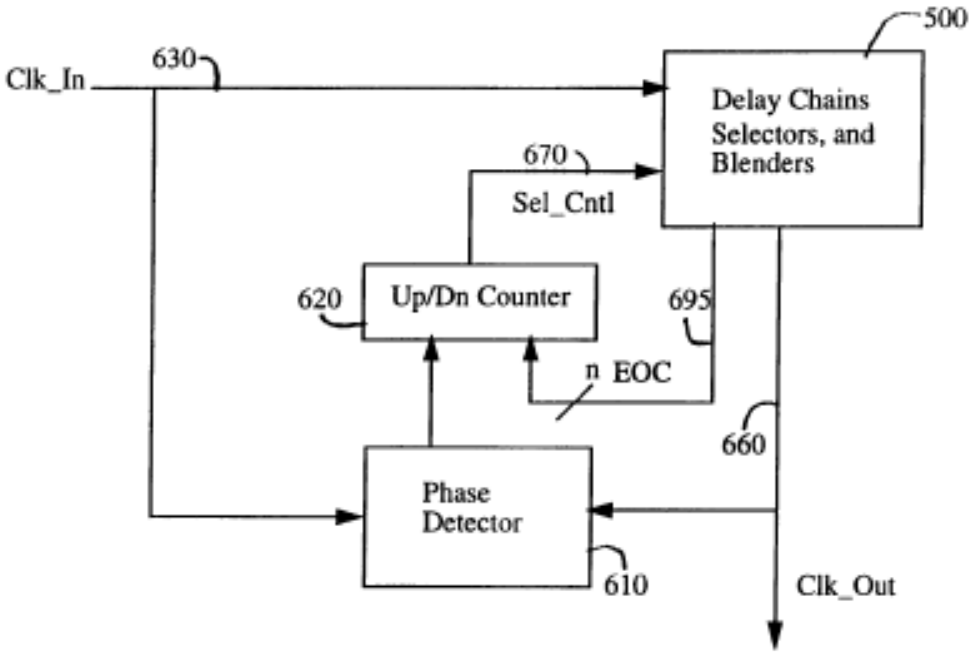


FIG_5

(Ex. 1005, FIG. 5.)

The circuit block 500 "represents in block 500 the circuitry in FIG. 4," which includes "delay chains 410 and 510." (*Id.*, 5:30, 4:28-29.) A POSITA would have understood each of delay chains 410 and 510 to be a "delay line" because they form a chain of delay elements arranged in a line that delay an input signal as it progressed down the line formed by the chain. (*See id.*, 4:28-49; Ex. 1002, ¶101.) As such, a POSITA would have understood *Donnelly*'s circuit block 500 to include a "delay line." (Ex. 1002, ¶101.) The loop formed by the phase detector 610, the up/down counter 620 and the block 500 operates to adjust the input clock signal Clk_In when the determined phase difference is less than approximately 180°. (*Id.*) As discussed above, the delay locked loop described in *Donnelly* in conjunction with figure 5 continues to adjust the input clock signal with the loop "until the blender output tap that is closest to the phase of the input clock is found." (Ex. 1005, 5:67-6:1; Ex. 1002, ¶101.) Indeed, the delay locked loop in figure 5 of *Donnelly* "constantly adjusts the value in the counter by one count causing the phase of the output to jitter around the desired phase relationship between Clk_In and Clk_Out." (Ex. 1005, 6:1-5.) As such, even when the delay locked loop in figure 5 of *Donnelly* achieves near alignment corresponding to a near zero phase difference, it still adjusts the input clock using the loop. (Ex. 1002, ¶101.)

A POSITA would have understood that *Donnelly* discloses performing the claimed "adjusting" when the determined phase difference is various values between 0° and 180°. (Ex. 1002, ¶102.) Indeed, *Donnelly* is constantly adjusting the delay of the input clock (Clk_In) to produce the feedback clock (Clk_Out). (Ex. 1005, 5:67-6:5; Ex. 1002, ¶102.), As such, *Donnelly* discloses that the adjusting occurs "when the determined phase difference is less than approximately 180°" as *Donnelly* discloses the adjusting occurs for all phase differences between Clk_In and Clk_Out. (Ex. 1002, ¶102.)

Furthermore, claim 10 of the '507 patent recites that the adjusting is performed "when the determined phase difference is less than approximately 180°." (Ex. 1001, 4:53-56.) But this condition will always be true in *Donnelly* because, as discussed above, the phase difference between Clk_In and Clk_Out will always be less than approximately 180°. (Ex. 1002, ¶103.) Hence, every time *Donnelly* adjusts the delay of Clk_In, such adjusting must necessarily occur "when the determined phase difference is less than approximately 180°" because the condition will always be true. Therefore, *Donnelly* discloses "adjusting . . . when the determined phase difference is less than approximately 180°" for this additional reason. (*Id*.)

Moreover, claim 10 states that the adjusting occurs "when the determined phase difference is less than approximately 180°" (Ex. 1001, 4:55-56) and does not

require that such adjustment only occurs when that condition is met or require that something else occurs when that condition is not met. As such, because *Donnelly* is constantly adjusting the delay of the input clock (Clk_In) to produce the feedback clock (Clk_Out), (Ex. 1005, 5:67-6:5), *Donnelly* discloses this aspect of claim 10. (Ex. 1002, ¶106; *see also id.*, ¶¶104-05.)

While *Donnelly* does not expressly disclose that a **shift register** is used in the loop, it would have been obvious in view of *Iwamoto* to modify *Donnelly* to implement the loop with a shift register as disclosed in *Iwamoto* to provide the functionality of *Donnelly*'s up/down counter 620 (annotated in red below). (Ex. 1002, ¶107.)

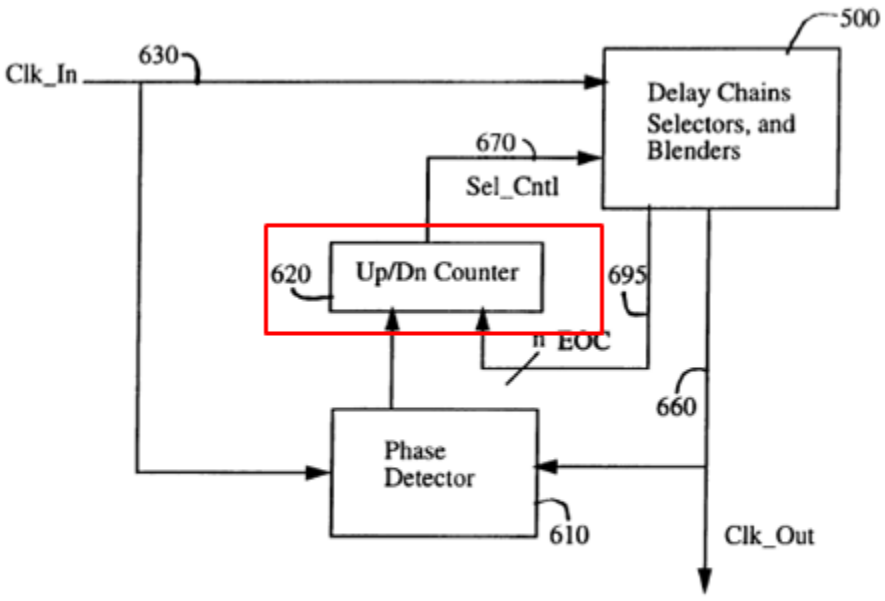


FIG_5

(*Id.*, ¶107, citing Ex. 1005, FIG. 5 (annotated).)

Iwamoto discloses using a shift register in a delay locked loop to choose the output of a delay line, where the tap that will produce the output is varied up and down among various available taps in response to the phase comparison performed by a phase comparator. (Ex. 1006, 1:43-47; Ex. 1002, ¶108.) Similarly, *Donnelly* discloses using an up/down counter in a delay locked loop to choose the output of a delay line, where the tap that will produce the output is varied up and down among the available taps in response to a phase comparison performed by a phase detector. (Ex. 1005, 5:36-38, 6:1-9; Ex. 1002, ¶108.) While *Donnelly* explains the functionality and general operation of the up/down counter, *Donnelly* does not provide any details as to the structure or components of the up/down counter. (Ex. 1002, ¶108.) *Iwamoto* discloses a shift register in a delay locked loop that has the same functionality as the up/down counter of *Donnelly*. (*Id.*) *Iwamoto* further discloses the structure of the well-known shift register, including the circuit elements and interconnection of those elements making up the shift register. (*Id.*)

As discussed in more detail below, a POSITA having the disclosure of *Donnelly* would have looked to *Iwamoto* for the implementation details regarding a circuit having the functionality of the up/down counter as disclosed in *Donnelly* in order to realize a functional implementation of a delay locked loop incorporating the functionality disclosed in *Donnelly*. (*Id.*, ¶109.) As set forth below, the use of

shift registers in delay locked loops to perform the functionality of *Donnelly*'s up/down counter was well known in the art in the mid-late 1990s, and therefore a POSITA would have had a reasonable expectation of success in realizing a functional delay locked loop based on the combination of *Donnelly* and *Iwamoto*. (*Id.*)

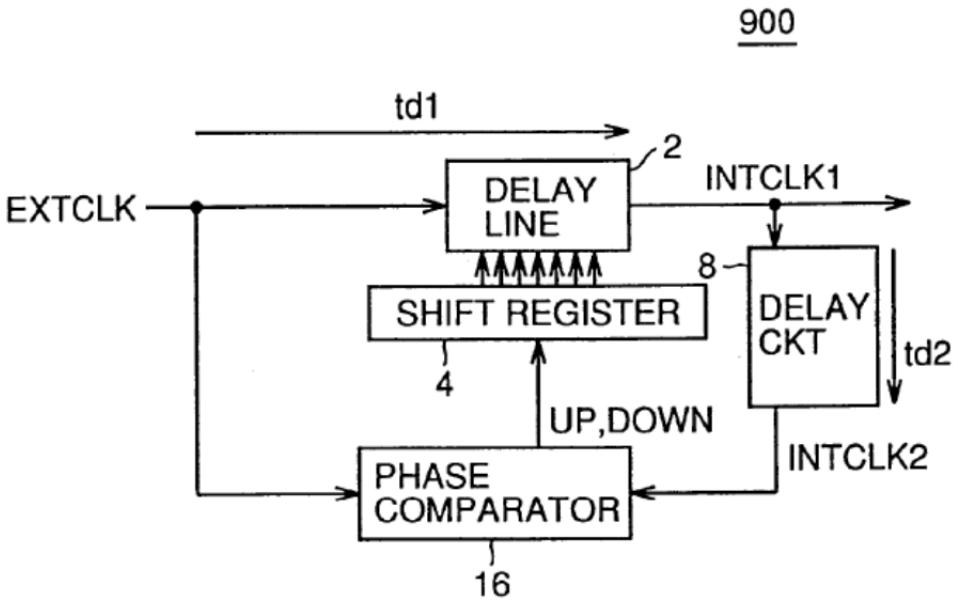
The up/down counter 620 in *Donnelly* stores a count value that is used to "derive a suitable Sel_Cntl signal 670." (Ex. 1005, 5:36-38; Ex. 1002, ¶110.) The Sel_Cntl signal 670 is used to select which of the delayed versions of the input clock signal is output from the block 500 that includes the delay chains. (Ex. 1005, 5:45-48; Ex. 1002, ¶110.) As such, the count value that is in the counter, which corresponds to the state of the counter, is used to determine the tap selection in the delay chain for the delay locked loop. (Ex. 1002, ¶110.)

Donnelly further discloses that the up/down counter 620 is controlled by the phase detector based on the polarity of the phase error detected when the input clock signal is compared with the output clock signal. (Ex. 1005, 5:36-38; Ex. 1002, ¶111) Therefore, the up/down counter changes its state based on information received by the up/down counter from the phase detector indicating that the counter should count up or down. (Ex. 1002, ¶111.) An increase or decrease in the count value alters the delay of the delay locked loop by the increment "equal to the resolution of circuit block 500." (Ex. 1005, 6:1-9; Ex.

1002, ¶¶111-12.) *Iwamoto* discloses a shift register that serves the same function as *Donnelly*'s up/down counter 620. (Ex. 1002, ¶111; *see also id.*, 113.)

Iwamoto discloses a "conventional DLL circuit 900 shown in FIG. 17 [that] includes a delay line 2, a shift register 4, a phase comparator 16 and a delay circuit 8." (Ex. 1006, 1:32-34.)

FIG. 17 PRIOR ART



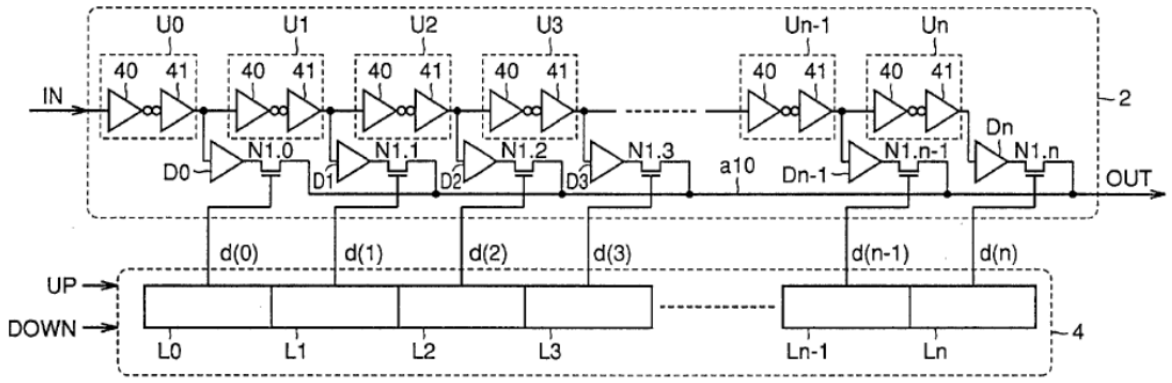
(*Id.*, FIG. 17.)

The "[d]elay line 2 delays an input external clock signal EXTCLK and outputs an internal clock signal INTCLK1." (*Id.*, 1:37-38.) The INTCLK1 signal is then further delayed by delay circuit 8 and "outputs the resulting signal (clock signal INTCLK2)." (*Id.*, 1:38-40; Ex. 1002, ¶114.) Like the delay locked loop of figure 5 of *Donnelly*, *Iwamoto*'s delay locked loop in figure 7 compares an output

clock signal (INTCLK2) with an input clock signal (EXTCLK) using a phase comparator. (Ex. 1006, 1:41-43; Ex. 1002, ¶114.) Based on the phase comparison, the phase comparator 16 outputs either an UP signal or a DOWN signal to the shift register 4. (Ex. 1006, 1:43-47; Ex. 1002, ¶114.) The shift register 4 "changes delay time of delay line 2." (Ex. 1006, 1:43-47.)

Figure 18 of *Iwamoto* shows that, like in *Donnelly*, the delay line in *Iwamoto* includes a number of delay elements (delay units U0-Un) coupled in series to form a delay line 2. (Ex. 1006, 1:51-52, FIG. 18; Ex. 1002, ¶115.)

FIG. 18 PRIOR ART



(Ex. 1006, FIG. 18.)

The shift register 4 is shown below the delay line 2 in figure 18 and "includes a plurality of registers L0, L1, . . ., Ln." (*Id.*, 1:65-67; Ex. 1002, ¶116.) Each of the registers L0-Ln is coupled to the gate of a corresponding NMOS transistor N1.0-N1.n. (Ex. 1006, 2:1-5, FIG. 18; Ex. 1002, ¶116.) The shift

register 4 selects the particular tap from the delay line based on a single HIGH value being stored in one of the registers L0-Ln. (Ex. 1006, 2:6-10; Ex. 1002, ¶116.) The single HIGH value in the shift register that results in one of the control signals d(0), (d1), . . ., d(n) being in the active state shifts up or down in the shift register (i.e. to the right or to the left) in response to the UP and DOWN signals received from the phase comparator 16. (Ex. 1002, ¶116.) For example, *Iwamoto* discloses:

> Selector 17 shown in FIG. 23 may have the same structure as shift register 4 described above. Selector 17 outputs control signals d(0), (d1), . . ., d(n) in response to the DOWN signal or UP signal output from phase comparator 16. Any of control signals d(0), (d1), . . ., d(n) is in an active state. The active state moves in accordance with the DOWN signal or the UP signal.

(Ex. 1006, 4:8-14.)

Therefore, just as the state (count value) of the up/down counter 620 in figure 5 of *Donnelly* selects the tap used to provide the output signal from the delay block 500, the state (location of the HIGH value) of the shift register 4 in figure 17 of *Iwamoto* selects the tap used to provide the output from the delay line 2. (Ex. 1002, ¶117.) Similarly, the phase detector 610 instructs the up/down counter 620 in figure 5 of *Donnelly* to count up or down based on the phase comparison it

performs, while the phase comparator 610 in figure 17 of *Iwamoto* instructs the shift register 4 to shift UP or DOWN based on its phase comparison. (*Id.*) The change of state for both references as a result of the up/down indication from the respective phase comparisons produces the same result in shifting the selected tap up or down by one increment. (*Id.*)

A POSITA having the disclosure of *Donnelly* would have looked to *Iwamoto* for structural details for a circuit that performs the function of the up/down counter in *Donnelly*. (*Id.*, ¶118.) Both *Donnelly* and *Iwamoto* are directed to delay locked loops that incrementally select between different taps to output a clock signal from a delay line based on the state of a circuit that is responsive to up and down instructions received from a phase detector. (*Id.*) As such, a POSITA would have had reason to look to *Iwamoto* for details regarding the structure of such a circuit based on the absence of such details in *Donnelly*. (*Id.*) Such a person would have been motivated to modify *Donnelly*'s delay locked loop in view of the teachings of *Iwamoto* such that *Donnelly's* delay locked loop in figure 5 circuit used a shift register, like that disclosed by *Iwamoto*, to select the appropriate tap from which the output clock (Clk_Out) is provided. (*Id.*)

A POSITA would have understood, based on the teachings of *Iwamoto*, how to include a shift register in the delay locked loop of *Donnelly* to realize the functionality of the up/down counter of *Donnelly*. (*Id.*, ¶119.) A POSITA would

have been motivated to do so in order to achieve an operational delay locked loop having the functionality set forth in *Donnelly*. (*Id.*) *See KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 401 (2007) (hereinafter "*KSR*"). Indeed, a POSITA would have known how to modify *Donnelly* based on *Iwamoto* and would have been able to do so with reasonable success. (Ex. 1002, ¶119.)

A POSITA would have looked to a shift register, like that disclosed in *Iwamoto*, to achieve the function of *Donnelly*'s up/down counter at least in part based on such a skilled person's knowledge that such shift registers were commonly used in delay locked loops, as evidenced by both *Iwamoto* and the '507 patent itself. (*Id.*, ¶120.) As the background section of the '507 patent acknowledges, a POSITA knew how to use shift registers in delay locked loops to shift a delay in the delay line based on a determined phase difference between an input signal and a feedback signal. (*Id.*)

> In operation the phase detector 12 determines if a phase difference exists between the buffered input and feedback clock signals, CK1 and CKF. The phase difference determines an appropriate shift in the buffered input clock signal via adjustment of the shift register 14 to select sufficient delay via the delay line 16, **as is well understood by those skilled in the art**.

(Ex. 1001, 1:27-33 (emphasis added); Ex. 1002, ¶120.)

Indeed, the use of a shift register, like *Iwamoto*'s shift register 4, for *Donnelly*'s up/down counter 620 would have been the mere application of a known technique (*Iwamoto*'s shift register 4) to a known device (*Donnelly*'s up/down counter 620) ready for improvement to yield the predictable result of an operational delay locked loop as disclosed in figure 5 of *Donnelly*. (Ex. 1002, ¶121.) *KSR*, 550 U.S. at 416.

d) delaying the input clock signal to compensate for the phase difference,

Donnelly discloses this feature, for reasons similar to those discussed above for limitation 10(c). (*See supra* Section IX.A.1(c); Ex. 1002, ¶122.)

As seen from figure 5, *Donnelly* discloses that block 500 receives input clock Clk_In. (Ex. 1005, FIG. 5.) Block 500 includes delay chains 410 and 510. (Ex. 1005, 5:30, 4:28-30, FIGS. 4, 5; Ex. 1002, ¶123.) "[**D]elay chain 410 receives and propagates signal Clk_In [] to produce the true outputs 440 spanning at least 180° of Clk_In[]** and the other delay chain 510 receives and simultaneously propagates signal Clk_InB 520, the complement of Clk_In to produce complement outputs 540 spanning at least 180° of Clk_InB 520." (Ex. 1005, 4:30-36 (emphasis added); Ex. 1002, ¶123.) A POSITA would have understood that propagating the input clock signal Clk_In through delay chain 410 and the complement of input clock signal Clk_In through delay chain 510 constitutes "delaying the input clock signal," as recited in limitation 10(d). (Ex.

1002, ¶123.) Indeed, the "outputs 440" and "outputs 540" are delayed versions of the input clock signal Clk_In available as "taps from the delay chains" that become available as the input clock signal passes through delay chains 410 and 510 that are "each . . . constructed from inverting **delay** elements." (Ex. 1005, 4:28-30, 4:38-46, 5:53-55 (emphasis added), FIGS. 4, 5; *see also id.,* 2:21-22; Ex. 1002, ¶123.) This is further confirmed by figure 7 of *Donnelly,* which discloses "[a]n embodiment of a pair of delay chains suitable for use in FIG. 4." (Ex. 1005, 5:26-28; Ex. 1002, ¶123.) Figure 7 discloses that the delay chains have a set of taps (corresponding to outputs 440 and 540) where each tap adds "exactly an inverter delay" to the input clock signal to produce delayed versions of the input clock signal. (Ex. 1005, 8:14-29; Ex. 1002, ¶123.)

Donnelly further discloses that the delayed versions of the input clock signal, i.e., the taps of the delay chains 410 and 510, are used "to compensate for the phase difference," as claimed in limitation 10(d). (Ex. 1002, ¶124.) For instance, *Donnelly* discloses that "[p]hase detector 610 detects **the large phase error** and instructs counter 620 to count up." (Ex. 1005, 5:43-45 (emphasis added); Ex. 1002, ¶124.) "Circuit block 500 then receives the Sel_Cntl 670 information which instructs selection logic 445 in FIG. 4 to switch consecutively through the taps from the output of the blender circuit to **reduce the phase error**." (Ex. 1005, 5:45-48 (emphasis added).) This process of switching through the taps of the

blender circuit "to reduce the phase error" involves utilizing the delayed versions of the input clock signals that are available from the taps of the delay chains 410 and 510:

> Selection logic 445 determines when it gets to the last tap of the blender circuit and a phase error is still present that a different pair of taps from the delay chain is required. It relays a request to alter the selected taps into the blender via signal 483 to selection logic 480. This process continues as selection circuit 480 **switches consecutively through the taps from the delay chains**.

(*Id*., 5:48-55 (emphasis added); Ex. 1002, ¶124.)

Thus, as disclosed in *Donnelly* with reference to figures 4 and 5, the input clock Clk_In is delayed to reduce a phase error ("compensate for the phase difference"). (Ex. 1002, ¶125.)

e) wherein a number of delay cells utilized is reduced by approximately one-half.

Donnelly discloses this feature, for reasons similar to those discussed above for limitation 10(a).[4] (Ex. 1002, ¶126; *supra* Section IX.A.1(a).) For example, *Donnelly* discloses that the number of delay elements is reduced to 32 in figure 4 compared to 64 in the prior art figure 1. (Ex. 1005, 3:58-61 ("Assuming that taps

[4] Petitioner reserves the right to assert indefiniteness of claim 10 in district court, e.g., in light of the phrase "reduced by approximately one-half."

240 have the same polarity and pairs of inverters are used between taps, **only 32 delay elements (instead of 64) are required** given the above example discussed in connection with FIG. 1.") (emphasis added); Ex. 1002, ¶126.)

2. Claim 11

a) The method of claim 10 wherein the phase detector comprises a phase difference detector with a first resolution.

Donnelly in combination with *Iwamoto* discloses or suggests this feature. (Ex. 1002, ¶¶127-30.) As discussed above with respect to claim limitations 10(a)-(c), *Donnelly* discloses a phase detector 610 shown in figure 5. (*See supra* Sections IX.A.1(a)-(c); Ex. 1005, FIG. 5; Ex. 1002, ¶128.) *Donnelly*'s phase detector 610 determines a phase error, where the phase error includes a polarity. (Ex. 1002, ¶128.)

> FIG. 5 further shows phase detector 610 and up/down counter 620 connected to form a delay locked loop. By feeding back the Clk_Out 660 and comparing its phase to the phase of Clk_In 630, a phase error is determined. The polarity of the phase error instructs up/down counter 620 to increase or decrease its count value and the count value is used to derive a suitable Sel_Cntl signal 670.

(Ex. 1005, 5:32-38.)

A POSITA would have understood that a "phase error" would indicate a phase difference between the Clk_Out and Clk_In signals, where the phase error

includes a polarity indicating whether the Clk_Out signal leads or lags the Clk_In signal. (Ex. 1002, ¶129.) As described in *Donnelly*, the polarity of the phase error is used to cause the up/down counter 620 to increase or decrease its count value. (*See* Ex. 1005, 5:32-38; Ex. 1002, ¶129.) The phase detector 610 of *Donnelly* is or includes a "phase difference detector." (Ex. 1002, ¶129.)

While *Donnelly* does not expressly disclose that phase detector 610 comprises a phase difference detector "with a first resolution," a POSITA would have understood that *Donnelly*'s phase detector 610 necessarily has this feature, and that *Donnelly* inherently discloses this feature. (*Id.*, ¶130.) Such a person would have had that understanding because *Donnelly* discloses determining a phase difference as discussed above and because a determination of phase difference must be with respect to some resolution ("first resolution"). (*Id.*) Such a person would have understood that resolution refers to the capability to distinguish one phase from another (e.g., the phase of one input of detector 610 from the phase of another input of the detector), and that if the detector 610 did not have a resolution ("first resolution") then it would have been unable to perform its disclosed function. (*Id.*) In other words, in order for detector 610 and the delay locked loop of figure 5 of *Donnelly* to function at all, detector 610 must comprise a phase difference detector that inherently has a "first resolution." (*Id.*)

B. Ground 2: *Jefferson* Anticipates Claims 13 and 15

1. Claim 13

a) A method for reducing delay line length in a digital delay locked loop (DLL), the method comprising:

The preamble of claim 13 recites "for reducing delay line length." But the phrase "for reducing delay line length" does not breathe life and meaning into the claim and is not necessary to understand any positive limitations in the body of claim 13 or any claims depending from claim 13. Indeed, the body of claim 13 and the claims depending from claim 13 do not recite anything related to reduction of delay line length. Moreover, "for reducing delay line length" constitutes merely an intended use. Therefore, it is not limiting. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (explaining that preamble is limiting if it is "'necessary to give life, meaning, and vitality' to the claim" but that "[i]f, however, the body of the claim fully and intrinsically sets forth the complete invention, including all of its limitations, and the preamble offers no distinct definition of any of the claimed invention's limitations, but rather merely states, for example, the purpose or intended use of the invention, then the preamble . . . cannot be said to constitute or explain a claim limitation"); *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015) (considering whether preamble terms are "necessary to understand positive limitations in the body of claims," to determine limiting status).

Although a portion of the preamble (specifically, the phrase "a digital delay locked loop (DLL)") serves as antecedent basis for the term "the DLL" in the body of the claim, the remainder of the preamble (i.e., "for reducing delay line length") is still not limiting. *See, e.g.*, *TomTom, Inc. v. Michael Adolph*, 790 F.3d 1315, 1324 (Fed. Cir. 2015) (holding that a portion of the preamble that does not recite essential structure or steps, or give necessary life, meaning, and vitality to the claim does not become limiting simply because of the presence of another limiting phrase in that preamble.)

To the extent any portion of the preamble is considered limiting, only "a digital delay locked loop (DLL)" should be considered limiting, and *Jefferson* discloses that portion of the claimed method. (Ex. 1002, ¶¶131-32.) For instance, *Jefferson* discloses with respect to figure 4 "a digital DLL (DDLL) block diagram using macro and micro phase detectors." (Ex. 1007, 7:57-58; *see also id.*, 2:45-46, FIG. 4.) *Jefferson* discloses operation of the digital DLL in connection with the block diagram of figure 4, and thus discloses a "method" as recited in claim 13. (*Id.*, FIG. 4, 2:45-46, 7:57-9:20; Ex. 1002, ¶132.)

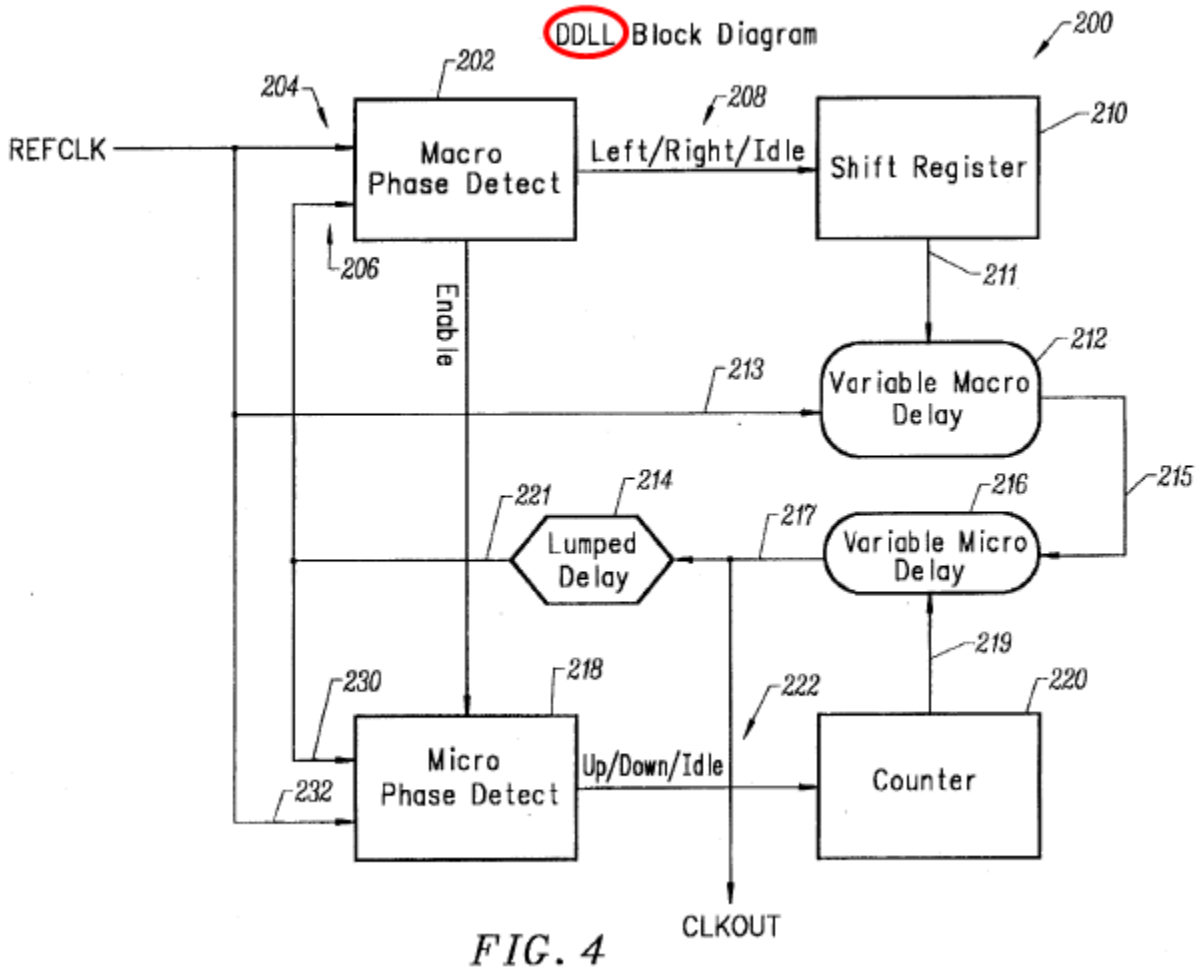


FIG. 4

(Ex. 1002, ¶132, citing Ex. 1007, FIG. 4 (annotated).)

b) determining whether a feedback clock signal in the DLL follows within a 180° phase difference behind an input clock signal; and

Jefferson discloses or suggests this feature. (Ex. 1002, ¶¶133-46.) The digital DLL of figure 4 in *Jefferson* includes "a macro phase detector 202 having a REF CLK input at 204 and a feedback clock input at 206." (Ex. 1007, 7:65-67.) As seen from figure 4 below, the DLL of figure 4 receives REF CLK at input 204. (Ex. 1002, ¶133.) Therefore, REF CLK 204 is an "input clock signal," as recited

in claim limitation 13(b). (*Id.*) The "feedback clock input at 206" is a "feedback clock signal in the DLL," as recited in claim limitation 13(b). (*Id.*)

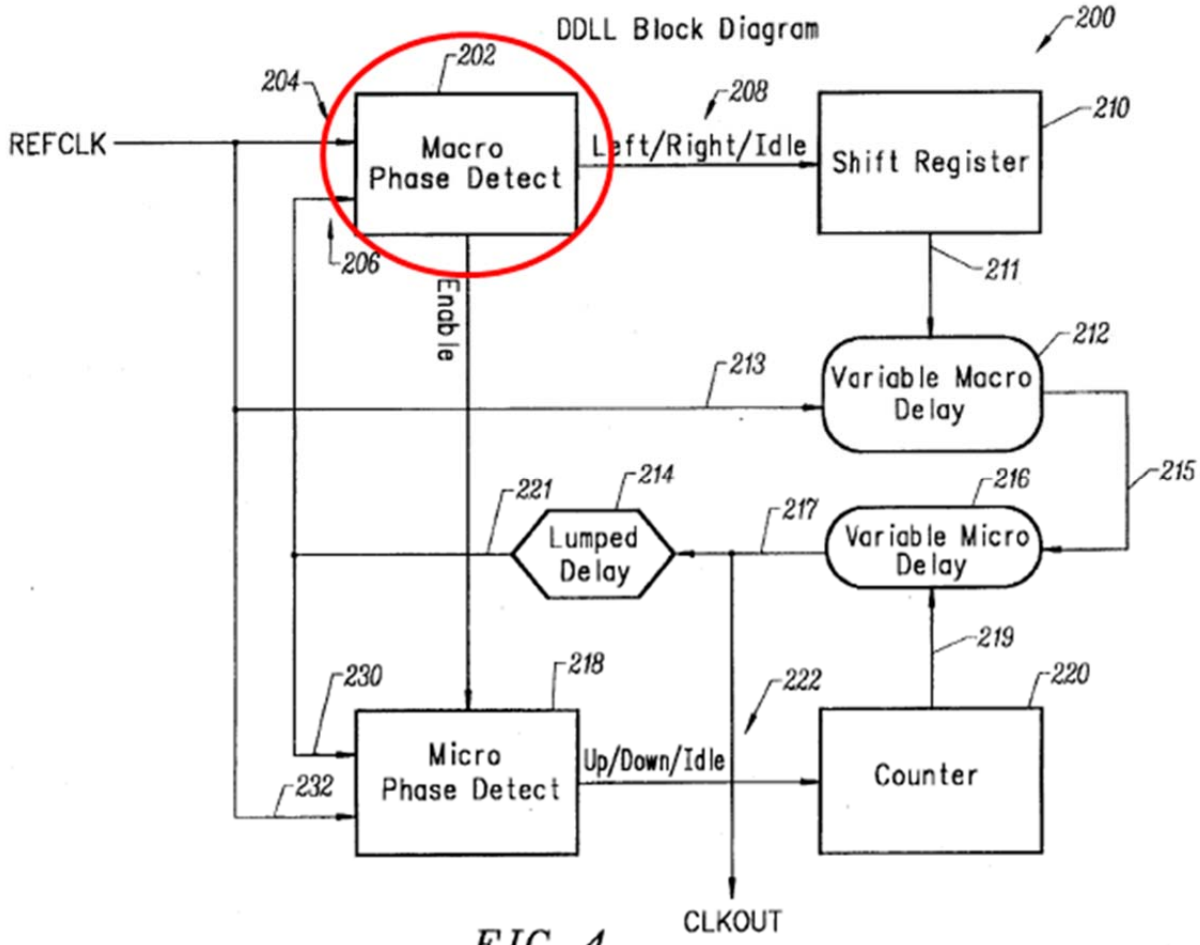


FIG. 4

(*Id.*, ¶133, citing Ex. 1007, FIG. 4 (annotated in red to show macro phase detector 202.)

Jefferson also discloses determining whether the feedback clock signal at 206 ("a feedback clock signal") in the digital DLL 200 of figure 4 ("the DLL") follows within a 180° phase difference behind REF CLK ("an input clock signal").

(Ex. 1002, ¶134.) Specifically, *Jefferson* discloses that the circuit shown in figure 3A performs the function of macro phase detector 202 in the digital DLL of figure 4. (Ex. 1007, 8:1-2; Ex. 1002, ¶134.) As explained below, the claimed "determining" is performed by D flip-flop FF2 shown in figure 3A (annotated below in blue). (Ex. 1002, ¶134.)

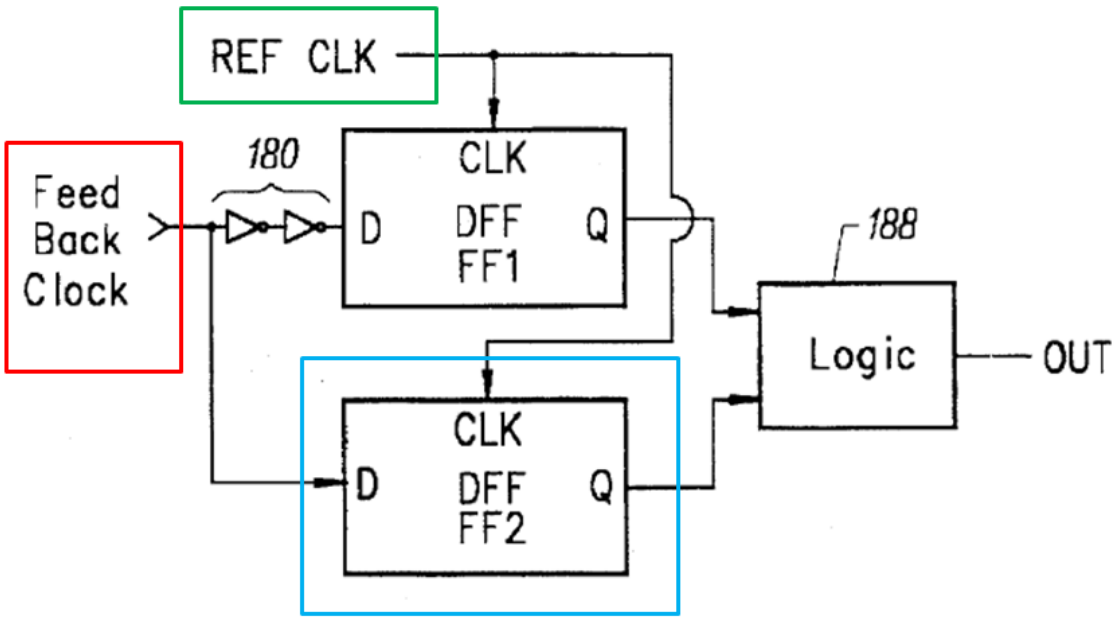


FIG. 3A

(*Id.*, ¶134, citing Ex. 1007, FIG. 3A (annotated in blue to show D flip-flop FF2, in red to show feedback clock ("feedback clock signal"), and in green to show reference clock signal REF CLK ("input clock signal").)

As an initial matter, a person of ordinary skill in the art (POSITA) would have understood that REF CLK signal (green) and Feedback Clock (red) in figure

3A above correspond to REF CLK input at 204 and feedback clock input at 206, respectively, in figure 4. (Ex. 1002, ¶135.) This is because *Jefferson* discloses that "[m]acro phase detector 202 can be implemented by a circuit similar to that of FIG. 3A" (Ex. 1007, 8:1-2) and the description of the circuit of figure 3A and figure 4 use the same notations (i.e., REF CLK and feedback clock). (Ex. 1002, ¶135.)

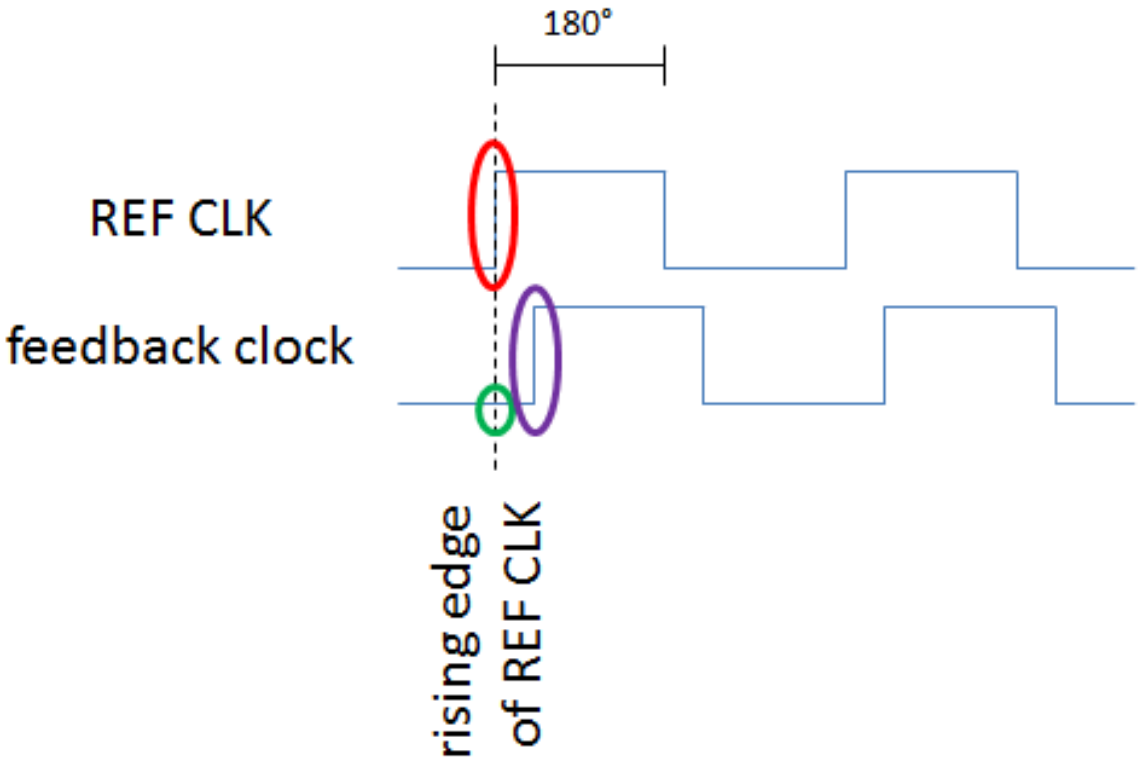
As explained below, the circuit of figure 3A (and therefore, macro phase detect circuit 202) performs the claimed "determining." (*Id.*, ¶136.) *Jefferson* discloses that "[t]he circuit of [figure] 3A is . . . a phase detector . . . ." (Ex. 1007, 6:49-50; *see also id.*, 2:41-42; Ex. 1002, ¶136.) In particular, "FIG. 3A shows two flip-flops, FF1 and FF2," both of which "are of the D-latch type." (Ex. 1007, 6:56-57.) *Jefferson* discloses that the outputs of respective flip-flops FF1 and FF2 are set on the rising edge of the reference clock which is provided to both of those flip-flops. (*Id.*, 7:32-40; Ex. 1002, ¶136.)

Based on this disclosure and the label "DFF" for flip-flops FF1 and FF2 in figure 3A, which indicates they are D flip-flops, a POSITA would have understood that flip-flops FF1 and FF2 are rising edge-triggered D flip-flops. (Ex. 1002, ¶137; *see also id.*, ¶¶32-34.) In other words, the bit ('0' or '1') stored by each of those flip-flops (and thus the output Q of each of those flip-flops, which is the same as the stored bit) is set each time the reference clock signal REF CLK has a rising edge, i.e., rises from '0' to '1'. (*Id.*, ¶137.)

The flip-flop FF2 receives the feedback clock signal at its D input and the reference clock at its CLK input. (Ex. 1007, FIG. 3A; Ex. 1002, ¶138.) As such, when the CLK input goes high, the flip-flop FF2 will sample the state of the feedback clock signal at that point in time. (Ex. 1002, ¶138.) This is because on each rising clock edge of reference clock signal REF CLK, the Q output of flip-flop FF2 is set to the value of the flip-flop's D input, while at other times the Q output maintains its previously stored value. (*Id.*) Because the flip-flop FF2 samples the state of the feedback clock signal (HIGH or LOW) at the rising edge of the reference clock signal, it determines whether the feedback clock signal is transitioning from LOW to HIGH before or after the reference clock with respect to a given period of the reference clock. (*Id.*) By detecting if the feedback clock signal transitions from LOW to HIGH before or after the reference clock, the flip-flop FF2 determines whether the feedback clock signal follows within a 180° phase difference behind the reference clock signal REF CLK. (*Id.*) Specifically, as explained in detail immediately below, **by virtue of FF2 being a positive edge triggered D flip-flop,** the Q output of FF2 will be set to logic LOW ('0') when the feedback clock is determined to follow within a 180° phase difference behind the reference clock signal REF CLK, and it will be set to logic HIGH ('1') otherwise. (*Id.*) Therefore, *Jefferson* discloses determining whether the feedback clock ("a

feedback clock signal") in the DLL follows within a 180° phase difference behind the reference clock signal REF CLK ("an input clock signal"). (*Id.*)

The demonstratives below help to illustrate this aspect of the operation of flip-flop FF2. (*Id.*, ¶139.) Consider a first scenario where the feedback clock signal follows within a 180° phase difference behind the reference clock signal REF CLK. (*Id.*)



(*Id.*)

In the above scenario, the rising edge of the feedback clock signal (annotated in purple) follows within a 180° phase difference behind the rising edge of the

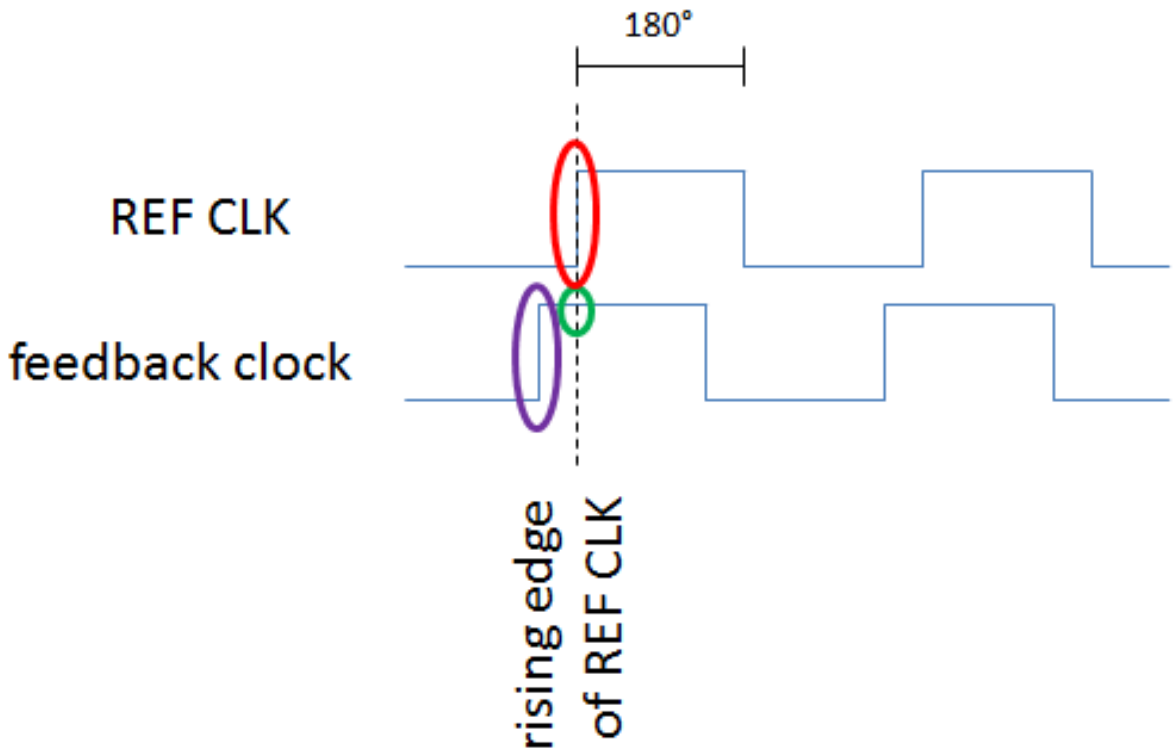
reference clock signal REF CLK (annotated in red). (*Id.*, ¶140.) As shown above in green, in this situation, the feedback clock signal will be LOW ('0') at the point when the reference clock signal transitions HIGH, and, as such, the flip-flop FF2 will sample the LOW value and **output a '0' on its Q output**. (*Id.*)

The reference clock signal REF CLK in *Jefferson* is disclosed as having a 50/50 duty cycle such that it is HIGH ('1') for 50% of the time and LOW ('0') for 50% of the time. (*See* Ex. 1007, FIG. 3B; Ex. 1002, ¶141.) As such, the feedback clock signal also has a 50/50 duty cycle because the feedback clock signal is a delayed version of REF CLK. (Ex. 1007, FIG. 4; Ex. 1002, ¶141.) Therefore, in general, if the purple rising edge of the feedback clock signal occurs anywhere between the red rising edge of REF CLK and the immediately following falling edge of REF CLK, then the feedback clock lags the reference clock by an amount between 0° and180° ("follows within 180° degree phase difference behind the reference clock") (Ex. 1002, ¶141.) As a result, *Jefferson* discloses that in a scenario as shown above where the feedback clock signal is determined to follow within a 180° phase difference behind the reference clock signal REF CLK, the Q output of the flip-flip FF2 is set to '0'. (*Id.*)

Because both clock signals shown above are periodic and have the same period, at every time at which the output Q of flip-flop FF2 is set (i.e., at each rising edge of the reference clock signal REF CLK), the output Q is set to '0'. (*Id.*,

¶142.) At other times (i.e., other than the rising edges of the reference clock signal REF CLK), flip-flop FF2 maintains its already-stored value (i.e., '0' in the above scenario), in accordance with how such a flip-flop would operate. (*Id.*)

On the other hand, the demonstrative below illustrates a scenario where the feedback clock signal does **not** follow within a 180° phase difference behind the reference clock signal REF CLK. (*Id.*, ¶143.) In contrast to the previous scenario, here flip-flop FF2 will sample the HIGH value and **output a '1' on its Q output**. (*Id.*)



(*Id.*)

In this demonstrative, again, the rising edge of reference clock signal REF CLK is shown in red, the rising edge of the feedback clock signal which is provided at the D input of flip-flop FF2 is shown in purple, and the D input of FF2 at the rising edge of REF CLK (i.e., the sampled value) is shown in green. (*Id.*, ¶144.) In this scenario, the feedback clock signal has a rising edge (shown in purple) slightly before the rising edge of the reference clock REF CLK (shown in red). (*Id.*) As such, the feedback clock signal **leads** the reference clock signal and therefore does **not** follow within a 180° phase difference behind the reference clock signal, because as shown in this demonstrative, the rising edge of the feedback clock (purple) does not occur within the phase interval annotated above as "180°." (*Id.*) Equivalently, in the above scenario the feedback clock signal can be considered to follow (lag) the reference clock signal REF CLK by **more** than 180°. (*Id.*) For example, observe that the rising edge of the feedback clock signal that occurs immediately after the one shown in purple above (i.e., the rising edge in the next cycle) trails the red rising edge of REF CLK by more than 180°. (*Id.*)

When the feedback clock does not follow within a 180° phase difference behind the reference clock signal, (i.e., when the scenario depicted above transpires), the flip-flop FF2 samples a HIGH value or logical '1' (annotated in green above) at the rising edge of REF CLK (red above). (*Id.*, ¶145.) The D input of FF2 (i.e., the feedback clock signal) is also '1' at every other rising edge of REF

CLK. (*Id.*) For example, note that at the rising edge of the reference clock signal REF CLK that occurs immediately after the one annotated above in red (i.e., at the rising edge in the next cycle), the value of the feedback clock signal is again HIGH ('1'). (*Id.*) Because both clock signals shown above are periodic and have the same period, at every time at which the output Q of flip-flop FF2 is set (i.e., at each rising edge of the reference clock signal REF CLK), the output Q is set to '1'. (*Id.*) At other times (i.e., other than the rising edges of the reference clock signal REF CLK), flip-flop FF2 maintains its already-stored value (i.e., '1' in the above scenario), in accordance with how such a flip-flop would operate. (*Id.*) Therefore, *Jefferson* discloses **that the Q output of the flip-flop FF2 is set to '1'** when the feedback clock signal is therefore determined **not** to follow within a 180° phase difference behind the reference clock signal REF CLK. (*Id.*)

Thus, *Jefferson*'s flip-flop FF2 provides either logic LOW ('0') or logic HIGH ('1') at its Q output depending on whether or not the feedback clock in the DLL follows within a 180° phase difference behind the reference clock signal REF CLK. (*Id.*, ¶146.) The Q output of FF2 will be set to logic LOW ('0') when the feedback clock is determined to follow within a 180° phase difference behind the reference clock signal REF CLK, and it will be set to logic HIGH ('1') otherwise. (*Id.*) Therefore, *Jefferson* discloses determining whether the feedback clock ("a

feedback clock signal") in the DLL follows within a 180° phase difference behind the reference clock signal REF CLK ("an input clock signal"). (*Id.*)

> c) selecting a switch position according to the determining step, including selecting a first switch position when the feedback clock signal follows behind the input clock signal with[in] 180°.

Jefferson discloses this feature. (Ex. 1002, ¶¶147-154.)[5] As discussed above with respect to claim limitation 13(b), the figure 4 digital DLL in *Jefferson* includes the circuit of figure 3A. (*See supra* Section IX.B.1(b); Ex. 1002, ¶147.) Moreover, the circuit of figure 3A includes flip-flop FF2 that performs the claimed "determining." (*See supra* Section IX.B.1(b); Ex. 1002, ¶147.) As discussed in detail below, the circuit of figure 3A also discloses claim limitation 13(c). (Ex. 1002, ¶147.)

[5] Petitioner assumes for the purposes of this proceeding that the phrase "within 180°" was intended instead of "with 180°." During prosecution, claim 15 (which issued as claim 13) recited "selecting a switch position according to the determining step, including selecting a first switch position when the feedback clock signal follows behind the input clock signal within 180°." (Ex. 1004, 27-28 (originally filed claim 15), 59 (Amendment dated December 13, 1999.) Similarly, the Examiner used the word "within" when stating the reasons for allowing this claim. (*Id.*, 65 (Notice of Allowance dated January 18, 2000.)

Jefferson discloses that the circuit of figure 3A includes "combinational logic at 188 . . . [that] receives the outputs of FF1 and FF2 and generates a combined signal output." (Ex. 1007, FIG. 3A, 7:14-16; Ex. 1002, ¶148.) "For example, combinational logic could be a simple 2-input exclusive OR gate with the inputs to the exclusive OR gate being the outputs of each of FF1 and FF2." (Ex. 1007, 7:16-18.)

It was well known well before the alleged invention of the '507 patent that a two-input exclusive OR (i.e., XOR) gate as described in *Jefferson* (*id.*, 7:14-18) was a logic gate with the truth table depicted below. (Ex. 1002, ¶149.)

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Figure 12.15 Exclusive OR gate.

(Ex. 1008, 246, Figure 12.15 (truth table for XOR logic gate); Ex. 1002, ¶149; *see also* Ex. 1002, ¶¶23-24.)

In the demonstrative below, an XOR gate is depicted (using the symbol for an XOR gate disclosed at figure 12.15 of Ex. 1008) at the position of the combinational logic 188 of *Jefferson*'s figure 3A, based on *Jefferson*'s disclosure of implementing the combinational logic 188 as an XOR gate. (Ex. 1002, ¶150.)

As seen below, the output Q of FF1 is input "A" of the XOR gate and output Q of FF2 is input "B." (*Id.*)

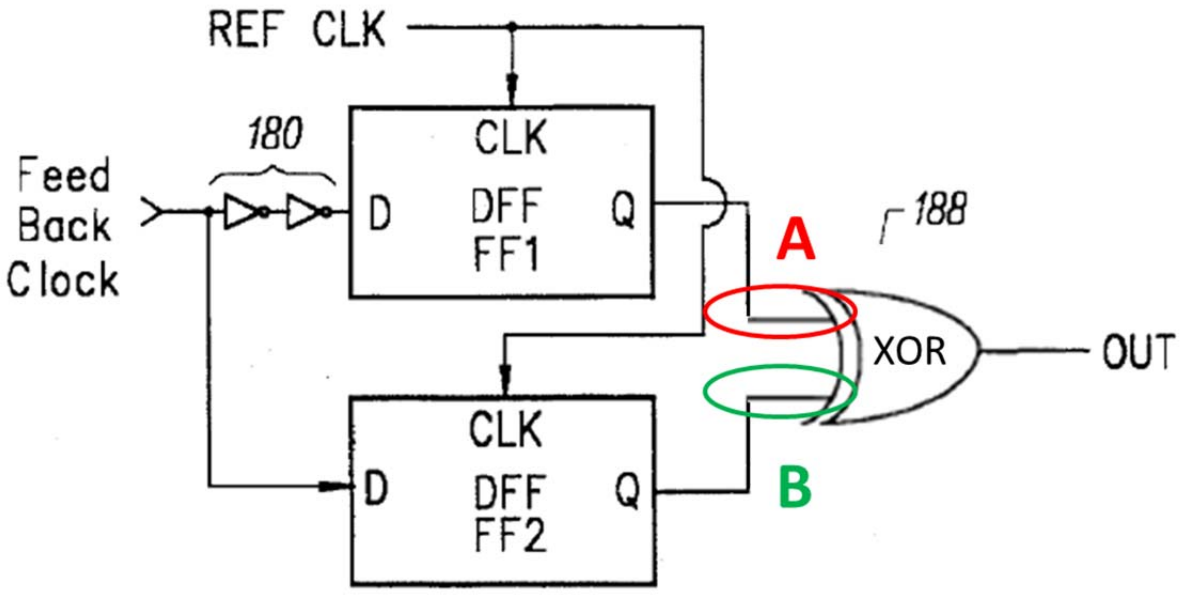


FIG. 3A

(*Id.*)

A POSITA would have understood that when 'B' is LOW ('0'), the output of the XOR will be the signal 'A' whereas if 'B' is HIGH ('1'), the output of the XOR will be the complement of 'A.' (*Id.*, ¶151.) This is confirmed by the following truth tables. (*Id.*)

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

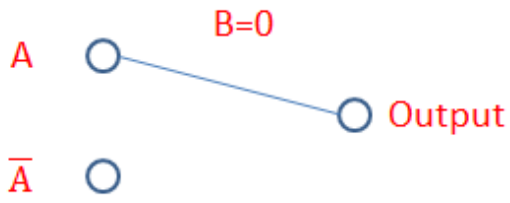
If B=0, then Output = A

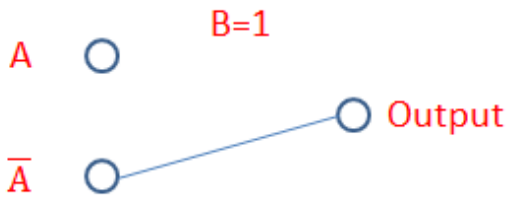
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

If B=1, then Output = $\overline{A}$

(*Id.*; *see also id.*, ¶¶23-24.)

Thus, the state of the B input (i.e., whether that input is LOW or HIGH) selects whether the output of the exclusive OR corresponds to A or the logical complement of A. (*Id.*, ¶152.) The demonstrative below shows that this relationship corresponds to the functionality of a single-pole double-throw (SPDT) switch where the input B of *Jefferson*'s XOR gate 188 controls the switch to select either the true input A or the complement input $\overline{A}$ as the output of the exclusive OR gate. (*Id.*)



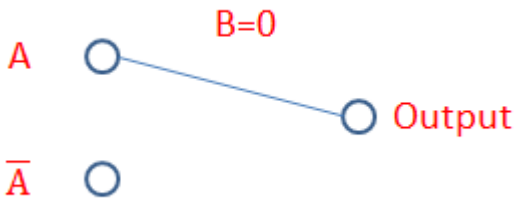


(*Id.*; *see also id.*, ¶¶23-24.)

In view of the above, a POSITA would have understood that when the output of the flip-flop FF2 is LOW ('0'), i.e., B is '0,' which corresponds to the feedback clock ("feedback clock signal") following behind the reference clock signal ("input clock signal") within 180° (*see supra* Section IX.B.1(b)), the exclusive OR gate 188 selects its output as the output of flip-flop FF1 (i.e., 'A' in the annotated figure above). (Ex. 1002, ¶153.) Such a scenario (*see* left of the figure immediately above) constitutes "selecting a first switch position," as recited in limitation 13(c). (*Id.*) Therefore, *Jefferson* discloses selecting the output of the exclusive OR gate 188 to correspond to the output of flip-flop FF1 according to the logic LOW provided by flip-flop FF2 ("selecting a switch position according to the determining step"), where that output of the exclusive OR gate 188 is selected when the output of flip-flop FF2 is LOW, which corresponds to the feedback clock following the reference clock within 180° ("including selecting a first switch position when the feedback clock signal follows behind the input clock signal within 180°"). (*Id.*)

Indeed, a POSITA would have understood that the exclusive OR gate disclosed by *Jefferson* as constituting the logic block 188 in figure 3A provides the functionality of a single-pole double-throw switch, with two possible states dependent on a control input (here, the control input is the logic value of the Q output of flip-flop FF2, i.e., the second input of the XOR gate which implements

the combinational logic 188 shown in figure 3A). (*Id.*, ¶154.) As such, *Jefferson* discloses selecting a switch position "according to the determining step" (the exclusive OR gate selects A or $\overline{A}$. based on B), including selecting the switch position shown below corresponding to connecting A XOR B to A ("selecting a first switch position") when the feedback clock signal follows behind the input clock signal within 180° (which corresponds to B=0 when flip-flop FF2 outputs a LOW logic value as discussed above for limitation 13(b)). (*Id.*; *see supra* Section IX.B.1(b).)



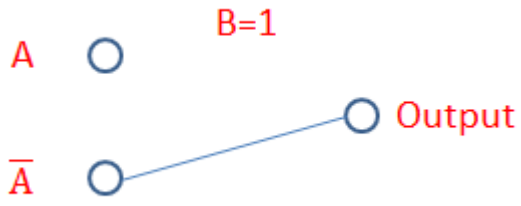
(Ex. 1002, ¶154.)

2. Claim 15

a) The method of claim 13 wherein selecting further comprises selecting a second switch position when the feedback clock signal does not follow the input clock signal within 180°.

Jefferson discloses this feature. (Ex. 1002, ¶¶155-56.) As discussed above for limitation 13(c), a POSITA would have understood that the exclusive OR gate disclosed by *Jefferson* as constituting the logic block 188 in figure 3A provides the functionality of a single-pole double-throw switch, with two possible states

dependent on a control input. (*See supra* Section IX.B.1(c); Ex. 1002, ¶155.) As also discussed above, *Jefferson* discloses selecting a first switch position (where the output is 'A') when the feedback clock signal follows behind the input clock signal within 180° (which corresponds to B=0 when flip-flop FF2 outputs a LOW as discussed above for limitation 13(c)). (*See supra* Section IX.B.1(c) for explanation of 'A' and 'B' inputs of logic gate 188, which are the Q outputs of flip-flops FF1 and FF2, respectively.; Ex. 1002, ¶155.) A POSITA would have understood that *Jefferson* discloses selecting a switch position shown below (corresponding to connecting A XOR B to $\overline{A}$) ("selecting a second switch position") when the output of flip-flop FF2 is a HIGH signal, i.e., B=1. (Ex. 1002, ¶155.) But as discussed above, *Jefferson* discloses that the output of flip-flop FF2 will be a HIGH signal (i.e., B=1) when the feedback clock does not follow the reference clock REF CLK within 180°. (*See supra* Section IX.B.1(b); Ex. 1002, ¶155.)



(*Id.*; *see also id.*, ¶¶21-24.)

Thus, *Jefferson* discloses that when flip-flop FF2 determines that the feedback clock leads the reference clock by an amount between 0° and 180° (i.e., the feedback clock signal does not follow the input clock signal within 180°) the FF2 outputs a HIGH ('1') to the 'B' input of the exclusive OR gate 188. (*Id.*, ¶156.) As a result, the exclusive OR gate 188 outputs the logical complement of the 'A' input of the exclusive OR gate 188 by selecting a second switch position. (*Id.*)

X. THE BOARD SHOULD INSTITUTE BOTH PETITIONS FOR THE '507 PATENT

Petitioner is filing another IPR petition challenging claims 10, 12, 13, and 15 of the '507 patent concurrently with the filing of this petition. However, Petitioner's proposed grounds for institution in the two petitions are based on different prior art references. For instance, the references at issue here (*Donnelly*, *Iwamoto*, and *Jefferson*) disclose configurations for delay locked loops different from *Kim* (U.S. Patent No. 5,875,219), which is the primary reference in the other petition. For instance, while *Kim* discloses a "shift register," *Donnelly* discloses an up/down counter in the delay locked loop. Similarly, *Jefferson* discloses an exclusive OR gate, which discloses the claimed first and second switch position, while in *Kim* a multiplexer discloses the claimed functionality. Accordingly, Petitioner respectfully requests that the Board adopt all proposed grounds in both petitions.

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 10, 11, 13, and 15 of the ’507 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: May 12, 2017

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,069,507 contains, as measured by the word-processing system used to prepare this paper, 11,872 words. This word count excludes the Table of Contents, Table of Authorities, List of Exhibits, Certificate of Compliance, and Certificate of Service.

Respectfully submitted,

Dated: May 12, 2017

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on May 12, 2017, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,069,507 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel listed below:

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