IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SanDisk LLC
Petitioner
v.

Memory Technologies, LLC
Patent Owner

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Patent No. 8,307,180

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PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. § 311, 37 C.F.R. §§ 42.100 *ET SEQ.*

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United States Patent No. 8,307,180

I. INTRODUCTION

Petitioner SanDisk LLC requests *inter partes* review of claims 17-27 and 31-34 of U.S. Patent No. 8,307,180 (the "'180 Patent") entitled "Extended Utilization Area for a Memory Device." *See* Ex. 1001.

II. MANDATORY NOTICES, STANDING, AND FEES

<u>Real Parties in Interest:</u> SanDisk LLC, Western Digital Corporation, Western Digital Technologies, Inc., SanDisk, Limited, SanDisk Storage Malaysia Sdn. Bhd., SanDisk Semiconductor (Shanghai) Co., Ltd., and SanDisk Israel (Tefen) Ltd. The following are direct or indirect parents or subsidiaries of the preceding companies: HGST, Inc., Virident Systems International Holdings Ltd., Western Digital International Ltd., SD International Holdings Ltd., SanDisk Technologies LLC, SanDisk International Holdco B.V., SanDisk IL Ltd., SanDisk Bermuda Limited, SanDisk Manufacturing Unlimited Company, and SanDisk China Limited.

<u>Related Matters:</u> *Memory Technologies, LLC v. SanDisk LLC, et al.,* No. 8:16-cv-2163-JLS-DFM (C.D. Cal.).

The '180 Patent is also subject to an ITC action entitled *In the Matter of Certain Flash Memory Devices and Components Thereof*, Inv. No. 337-TA-1034 ("ITC Matter"). Petitioner is a respondent in this investigation.

<u>Lead Counsel and Request for Authorization:</u> Pursuant to 37 C.F.R.

§§ 42.8(b)(3) and 42.10(a), Petitioner designates the following: Lead Counsel is Eliot D. Williams (Reg. No. 50,822) of Baker Botts L.L.P.; Back-up Counsel are Brian Oaks (Reg. No. 44,981) and Ebby Abraham (Reg. No. 73,399) of Baker Botts L.L.P.

Service Information: Service information is as follows: Baker Botts L.L.P., 1001 Page Mill Road, Building One, Suite 200, Palo Alto, CA 94304; Tel. (650) 739-7500; Fax (650) 739-7609. Petitioner consents to service by electronic mail at eliot.williams@bakerbotts.com, brian.oaks@bakerbotts.com, and ebby.abraham@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

Certification of Grounds for Standing: Petitioner certifies under 37 C.F.R. § 42.104(a) that the U.S. Patent No. 8,370,180 is available for *inter partes* review. Petitioner is not barred or estopped from requesting *inter partes* review of any claim of the '180 Patent on the grounds shown herein.

Fees: Under 37 C.F.R. § 42.103(a), the Office is authorized to charge the fee shown in 37 C.F.R. § 42.15(a) to Deposit Account No. 02-0384, Ref. No. 083480.0106, as well as any additional fees due in connection with this Petition.

III. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Petitioner requests *inter partes* review and cancellation of Claims 17-27 and 31-34 (the "Challenged Claims") of the '180 Patent (Ex. 1001) based on the

United States Patent No. 8,307,180

following grounds.

Ground	'180 Patent Claims	Basis for Rejection
1	17-27, 31-32, and 34	§ 102 based on *CompactFlash*
2	17, 20-27, and 31-34	§ 103 based on *Ziv and Vogt*
3	18 and 19	§ 103 based on *Ziv, Vogt,* and *Toombs*
4	17-19, 21-23, 27, and 31-34	§ 103 based on *Sinclair* and *Toombs*

IV. A PERSON OF ORDINARY SKILL IN THE ART

Relative to the '180 Patent, a person of ordinary skill in the art ("POSITA")

is a person having at least a bachelor's degree in Electrical Engineering, Computer

Engineering, or equivalent training, with at least two to three years of academic or

industry experience in the field of memory system design. Ex. 1002 at ¶65.

V. BACKGROUND OF THE TECHNOLOGY

A. Technical Background

A memory device is used to store electronic data. Ex. 1002 at ¶68. By 2008,

several types of memory devices that use flash or EEPROM memory were in

existence, including MultiMediaCard ("MMC") and CompactFlash ("CF"). *Id*. at

¶71. A memory device can communicate with a host device. Ex. 1009 at 19. For

example, an MMC receives commands from a host device over a "CMD" bus and

communicates data over the "DAT" bus line. Ex. 1002 at ¶74; *see* Ex. 1009 at 142.

Figure 4: MultiMediaCard Architecture
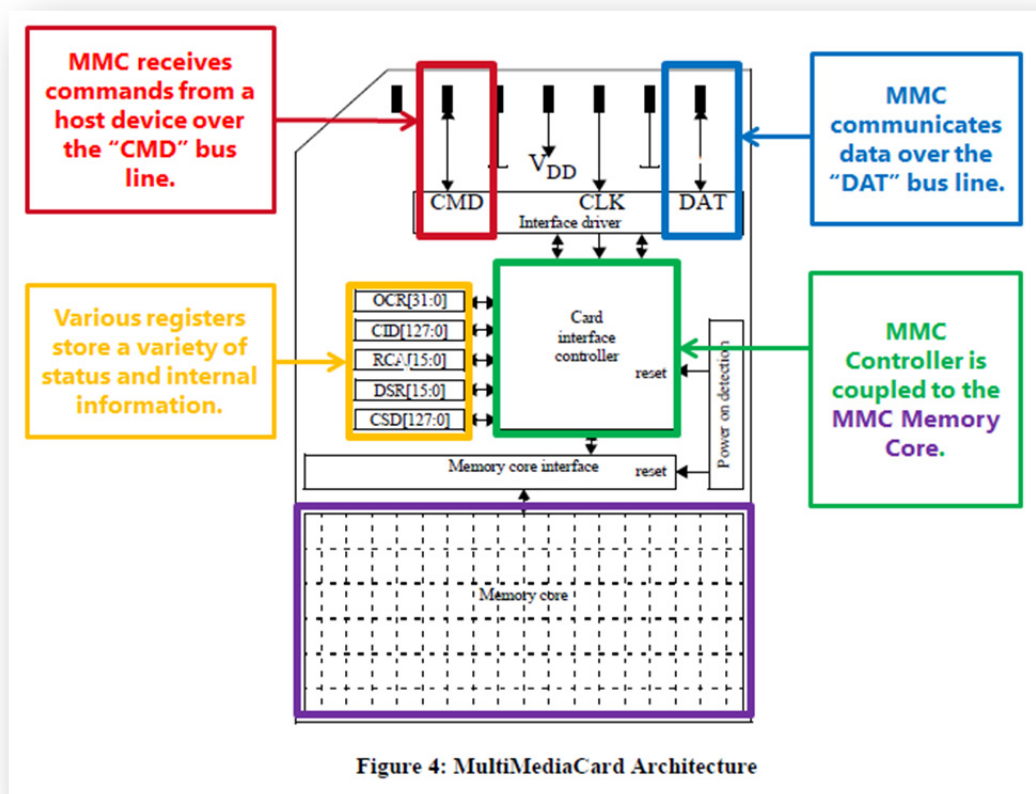
Ex. 1009 at Fig. 4 (annotated).

MMC also includes a group of registers that can store information about the memory card. *Id*. at 19. For example, the MMC device's CSD register provides information on how to access the memory card, including data format, data transfer speed, etc. *Id*. at 68, Table 22.

VI. OVERVIEW OF THE '180 PATENT

The '180 Patent issued on Nov. 6, 2012 from U.S. Patent Application No. 12/039,672 ('672 Application) filed on Feb. 28, 2008.

A.   Summary of the Claimed Subject Matter

The Challenged Claims generally relate to access profiles. An access profile "governs the current access operations to the memory device." Ex. 1001 at 4:57-58. The Challenged Claims, in particular, relate to activating an access profile and configuring a memory device in accordance with an access profile, so that the device is effective for a usage in accordance with the activated profile.

The access profiles are stored in a register of the memory and correspond to memory access operations, such as "a read, a write, an erase, and a modify attribute operation." *Id*. at 1:62-64, 5:1-3, 6:17-21, 7:4-13. The implementation of the access profile can be stored elsewhere. *Id*. at 5:14-17.

The '180 Patent specification describes the invention as applicable "in any stand-alone or embedded system that comprises or accesses a memory device." *Id.* at 5:24-27. When connected to such a system, the memory device can "receive one or more commands . . . for activating a particular access profile." *Id.* at 4:29-32. The portion of the system that issues commands to the memory device is referred to as a "host." *Id.* at 2:59-63.

The '180 Patent specification also describes configurations that may correspond to access profiles. For instance, in a "burst profile mode, [an access profile,] corresponding to fast, contiguous data access," the memory device is configured so that "after receiving all the data" to be written from a host, it may

"indicate 'exit busy' and set the transfer mode to 'transfer state,' thus facilitating faster execution of subsequent accesses by the host." *Id.* at 7:18-21.

Other access profiles may cause the device to configure itself such that a particular profile is "associated with different partitions of the memory device," including either "logical or physical partitions." (7:36-37). Similarly, a profile may result in a device configuration such that access operations are "map[ped] … to certain sections of the physical memory with special characteristics." *Id.* at 7:49-52. Finally, some access profiles may result in a configuration such that the device postpones "management" or "background operations" until after the data transfer. Ex. 1001 at 3:61-64, 4:43-49.

B. The '180 Patent Prosecution History

Before issuance of the '180 Patent, Applicant responded to three office actions and submitted a notice of appeal and a pre-appeal brief. Ex. 1008 at 327, 393, 406, 440. The resulting '180 Patent issued on Nov. 6, 2012.

The first office action rejected the claims as anticipated by Burgan et al. (*Burgan*). *Id*. at 443. *Burgan* teaches smart phones with various profiles, such as a work profile and a family profile, that are accessed in response to caller ID information of a received call. Ex. 1010 at ¶¶5-6.

Applicant's response to the first office action is relevant to the "command" claim element. According to Applicant, "*[a] command in the context of the*

various embodiments of the present application, and in any other context for that matter, ***suggests some type of authoritative direction or instruction to do/not to do something***." *Id*. at 427 (emphasis supplied). In other words, a command must provide a type of instruction. Ex. 1002 at ¶¶131-34. Using this definition, Applicant submitted that a POSITA would not equate the received Caller ID information in *Burgan* with an actual "command," because a Caller ID is a "passive" identifier. Ex. 1008 at 427.

Unconvinced by the Applicant's argument, the Patent Office subsequently issued a final rejection on July 6, 2011, maintaining the rejection. *Id*. at 408. In response, Applicant repeated its arguments in a Reply to the Final Office Action. *Id*. at 399-401. Applicant thereafter filed a notice of appeal and a pre-appeal brief. *Id*. at 382, 393-96. The Pre-Appeal Panel decided to withdraw the rejection and issue a new office action. *Id*. at 357.

The Examiner then rejected the claims over Suwa (*Suwa*) and Bertone et al. (*Bertone*). *Id*. at 329. Applicant made substantial amendments to the claims to distinguish *Suwa* and *Bertone* by further limiting a predefined access profile and the received one or more commands. *Id*. at 259-268. The amendments to Claim 17[1]

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[1] The challenged claims are numbered as they were during prosecution. *Id*. at 581-85.

are shown below:

> 17. (Currently Amended) A memory device, comprising:
>
> one or more registers for storing one or more predefined access profiles associated with said memory device, said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;
>
> ~~receiving means~~ a controller for receiving one or more commands related to said at least one usage of said memory device, said one or more commands for activating said one or more predefined access profiles associated with said memory device, said controller also
>
> ~~; and~~
>
> ~~configuring means~~ for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.

Id. at 261.

Applicant also clarified the claim limitation "configuring access to said memory device." As illustrated in Fig. 5 of *Bertone* (shown below), *Bertone* teaches a device that can contain multiple memories (outlined in red) with different characteristics stored in separate profiles (outlined in blue). Ex. 1011 at 16:28-36. The memory device in *Bertone* optimizes the memory device's speed based on the timing characteristics of the multiple memories. *Id*. at 16:28-36. Applicant argued that, unlike the claim requiring "configuring access to said memory device," the memory device in *Bertone* only configures the memory device according to

"timing characteristics to control the speed performance of the memory module."

Ex. 1008 at 266-67. In other words, because the operating speed does not affect an

access operation (*i.e.,* read, write, modify, or erase operation), Applicant argued

that merely changing an operating speed for the memory device ***does not*** constitute

an access configuration.
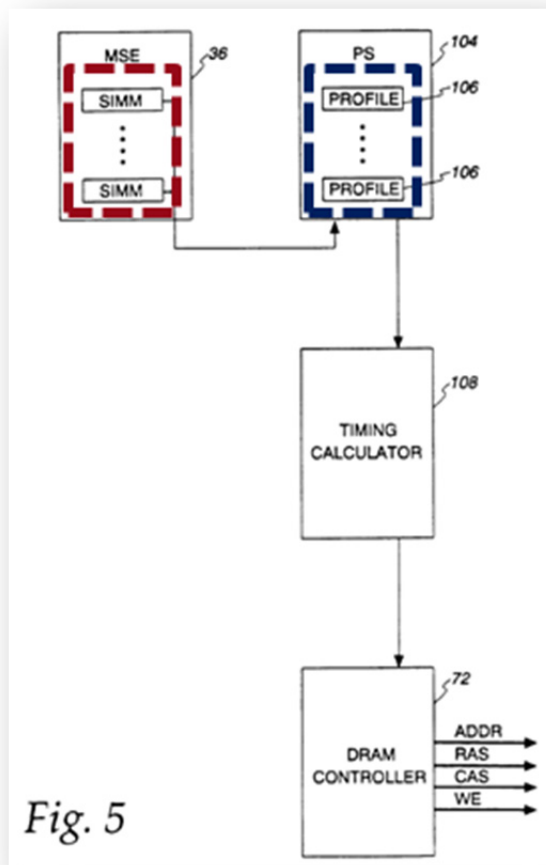
Fig. 5

Ex. 1011 at Fig. 5 (annotated).

Applicant also contended that an access-mode switcher in *Suwa*, which

automatically selects either a random access mode or a sequential mode, fails to

configure access to the memory device in accordance with an access profile. Ex. 1008 at 266. Applicant argued that *Suwa* does not configure an access profile, because the switcher in *Suwa* "automatically completes necessary changes to use the selected mode" upon activation. *Id*. at 266. Applicant argued that the claimed invention requires that the **activation** of an access profile **occurs separately** from the **access configuration** of the memory device. In other words, the configuration of an access to the memory device and the activation of an access profile **are distinct steps**. Ex. 1001 at 4:37-40.

A Notice of Allowance subsequently issued. Ex. 1008 at 244.

VII. CLAIM CONSTRUCTION

A. Legal Overview

Because the '180 Patent will not expire during the pendency of these proceedings, the Board should apply the BRI standard in its review. 37 C.F.R. § 42.100(b). For terms not specifically construed below, Petitioner interprets them for purposes of this review in accordance with their plain and ordinary meaning. Petitioner reserves the right to seek a different claim construction in litigation.

B. "register"

Independent Claim 17 recites the term "register." The context of the Challenged Claims requires one or more registers to store one or more access profiles.

The Board should construe "register" to mean "*a circuit or portion of memory that stores information*." As defined in the 1997 McGraw-Hill Electronics Dictionary, the ordinary meaning of the term "register" is "***a circuit that holds*** information in binary format to be processed or transferred." Ex. 1013 at 3 (emphasis supplied). Similarly, a 2007 technical dictionary confirms this interpretation. *See* Ex. 1027 at 4 (defining the term "register" as "[a] high-speed buffer, or ***region of memory***, that is used ***to store*** digits or characters for a specific purpose.") (emphasis supplied). Moreover, the 1993 IBM Dictionary of Computing defined "register" as "[a] part of internal storage having a specified storage capacity and intended for a specific purpose." Ex. 1020 at 3.

This construction is consistent with how "register" is used in the '180 Patent. *See* Ex. 1001 at 2:32-34 (recognizing the register as an instrument for "storing one or more predefined access profiles."). The claim discloses, "[a] memory device ... comprises ***one or more registers for storing*** one or more predefined access profiles associated with said memory device." *Id*. at Claim 17 (emphasis supplied).

C.   "command"

The Challenged Claims require that a command is used for activating the predefined access profile associated with the memory device. The Board should construe "command" to mean "*an instruction*." This is consistent with how the term is used in the '180 Patent, the prosecution history of the '180 Patent, and with

the ordinary meaning of the term. *See id*. at 3:56-58.

The prosecution history confirms this meaning. *See supra* Section V.B. Applicant repeatedly stated that "***[a] command*** in the context of the various embodiments of the present application ... ***suggests some type of*** authoritative direction or ***instruction*** to do/not to do something." Ex. 1008 at pp. 401, 427 (emphasis supplied).

The specification also consistently discloses the command as an instruction. The '180 Patent describes the various functions of the command as (1) "activating one or more access profiles associated with said memory device;" (Ex. 1001 at 1:56-60) (2) "designating a preferred access profile;" (*id*. at 2:6-10) (3) "configuring the memory device in accordance with an access profile;" (*id*. at 3:37-42) (4) "suspend[ing the] current access profile;" (*id*. at 6:2-7) and (5) "revert[ing] back to the access profile" (*id*. at 6:7-12). These cited functions are consistent with the proposed construction. Ex. 1002 at ¶132.

Accordingly, a POSITA would understand that "command" to mean "an instruction."

VIII. SUMMARY OF THE PRIOR ART

The prior art teaches the purportedly inventive feature of configuring a memory device according to a command-activated access profile that governs the access operations to the memory device.

United States Patent No. 8,307,180

A. CompactFlash

A CompactFlash device is a flash memory mass storage device. Ex. 1002 at ¶136. SanDisk first manufactured a CompactFlash device in 1994. Ex. 1014 at 1:56-59. CompactFlash quickly became the go-to portable mass storage device for electornic devices. Ex. 1002 at ¶137. CompactFlash remains popular and is supported by many devices. *Id*.

In 1995, the CompactFlash Association was formed by a group of international companies with the goal of creating an industry standard for flash-based mass storage. *Id*. at ¶138. The CompactFlash specification establishes the methods, processes, and practices for both the CompactFlash device and a host interacting with the device. *Id*. at ¶139.

On December 23, 2004, the CompactFlash Association released CompactFlash Specification Revision 3.0 (*CompactFlash*). *CompactFlash* was made publicly available to any interested member of the public free of charge from the following CFA website prior to 2008. Ex.1015 (Declaration of Stephen Gross) at ¶¶6-10 (attesting to the public availability of *CompactFlash*). The CompactFlash Association publicly announced on January 6, 2005 that *CompactFlash* "is available to download free from the CFA website at http://www.compactflash.org. Ex. 1017 at 9; Ex. 1016 at ¶6 (authenticating page 9 of Ex. 1017 as an accurate representation of the January 6, 2005 announcement by the CompactFlash

Association); *see also* Ex. 1018 (Jan. 7, 2005 article stating that "[t]he CF Specification Revision 3.0 is available to download free from the CFA web site at http://www.compactflash.org"); Ex. 1019 at ¶3 (describing an exemplary hard drive that utilizes a CompactFlash interface "as described in the CF+ and CompactFlash Specification Revision 3.0, published by the CompactFlash Association, Palo Alto, Calif., Dec. 23, 2004, http://www.compactflash.org.") (published on Apr. 5, 2007).

Moreover, *CompactFlash* was freely and publicly available online from the CompactFlash website as of at least Jan. 13, 2005. Ex. 1015 (Declaration of Stephen Gross) at ¶8 (attesting that a free download of *CompactFlash* was available after completing a registration form); Ex. 1017 at 2-3 (displaying the CompactFlash homepage indicating that *CompactFlash* "is now available to download" on Jan. 13, 2005); *Id.* at 6 (displaying the registration form that once submitted included a link for a free download for *CompactFlash*); Ex. 1016 at ¶6 (authenticating pages 2-3 of Ex. 1017 as an accurate representation of the CompactFlash Association website on Jan. 13, 2005 and page 6 of Ex. 1017 as an accurate representation of the CompactFlash registration form on January 27, 2005). *See Crestron Electronics Inc. v. Intuitive Building Controls Inc.,* Case IPR2015-01460, slip op. at 12-22 (PTAB Jan. 14, 2016) (Paper 14). Accordingly, *CompactFlash* qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and
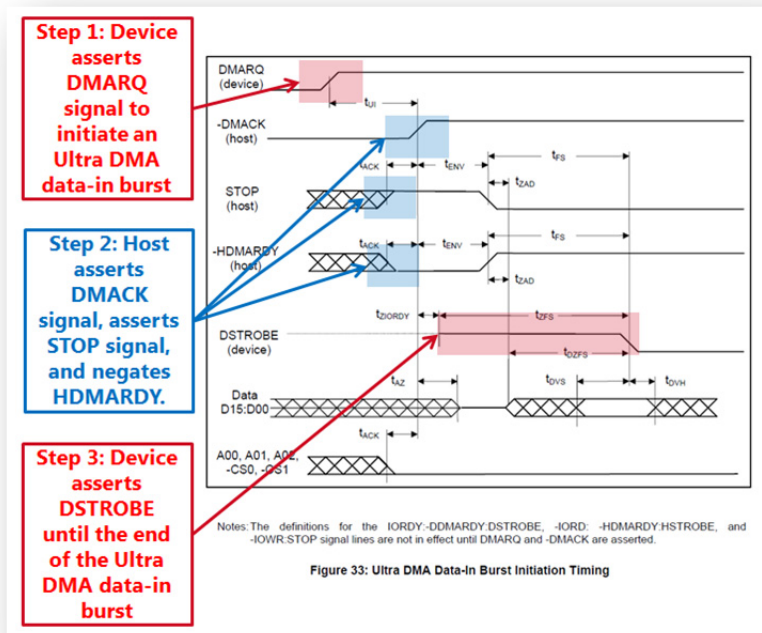
102(b). *CompactFlash* was not previously presented to the PTO in the context of the '180 Patent.

The CompactFlash Association made improvements to direct memory access (DMA) data transfer in Revision 3. A DMA data transfer occurs directly between the hardware subsystem and the memory device, rather than involving the host's CPU as an intermediary. Ex. 1002 at ¶143. In this manner, transfer speeds are boosted and the CPU is freed to work on other tasks while the transfer occurs. *Id*. Starting with Revision 3.0, "UltraDMA" was introduced, which boosted DMA transfer speed four-fold from the prior "MultiWord DMA" transfer. Ex. 1018 ("Ultra DMA 33 and UltraDMA66 [sic] interface modes will increase the CompactFlash interface data transfer rate to 66 MB/sec.").

CompactFlash also introduced several Ultra DMA modes. Ex. 1003 at 137. A CompactFlash controller configures a CompactFlash device to perform the Ultra-DMA transfer according to a protocol based on the mode selected. When a host sets an Ultra DMA mode, the memory device automatically disables any enabled MultiWord DMA mode. *Id*. at 158. In response, the memory device sets the selected Ultra DMA mode in a task file register. *Id*. at 120.

The host may subsequently communicate a READ DMA or WRITE DMA command to transfer data to the device. *Id*. at 52. The CompactFlash device, in response, will begin the Ultra DMA-specific initiation protocol to configure the

memory device for an Ultra DMA transfer. *Id.* at 68-70. As illustrated for a data-in

burst in Fig. 33 and a data-out burst in Fig. 38 (both shown below), the controller

starts the initiation phase of the Ultra DMA burst by asserting a DMARQ signal.

Id. at 75-76, 81-82. After the host responds by asserting and/or negating several

signals, the controller will assert either a DSTROBE signal or DDMARDY signal

until the end of the burst. *Id.* at 75-76, 81-82. Finally, unlike the older MultiWord

DMA modes, the device will calculate a CRC value to ensure the accuracy of the

data transferred in the Ultra DMA modes. *Id.* at 90. If the memory device detects

errors, an Error Register is updated to reflect the error. *Id.* at 90.

Figure 33: Ultra DMA Data-In Burst Initiation Timing

Id. at Fig. 33 (annotated).

Figure 38: Ultra DMA Data-Out Burst Initiation Timing
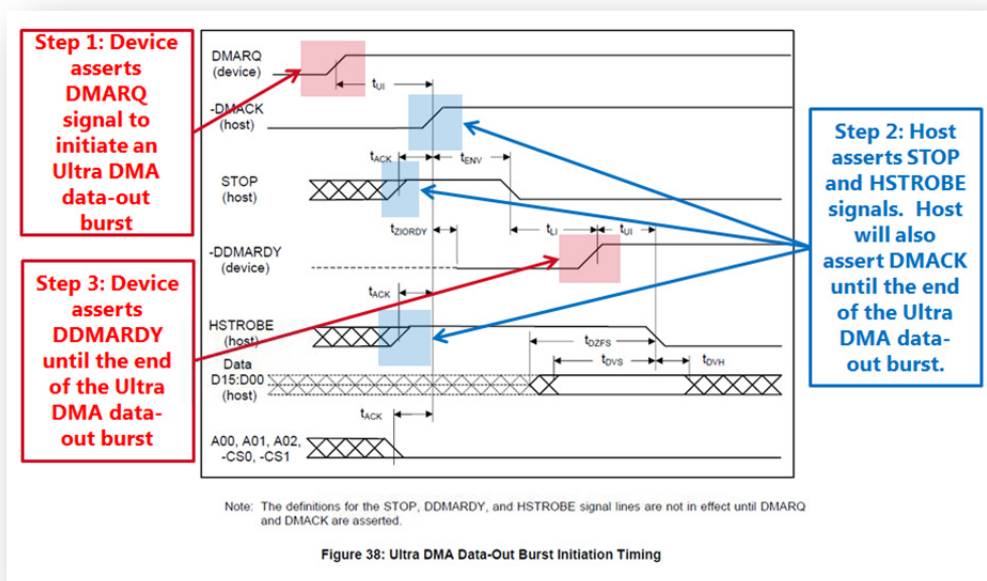
Id. at Fig. 38 (annotated).

B.   United States Patent No. 7,478,248 (*Ziv*)

Ziv was filed Nov. 27, 2002, and published on May 27, 2004. *Ziv* is prior art

under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Ziv* was not previously

presented to the PTO in the context of the '180 Patent.

Ziv discloses a memory controller that allows profile-based access to an

encrypted partition of memory. Ex. 1004 at Abstract. A user first selects a

password that is hashed and stored in a register. *Id*. at 4:15-20. The system also

generates a cryptographic key, which is used with a stored address offset for

accessing the secure area. *Id*. at 5:14-15.
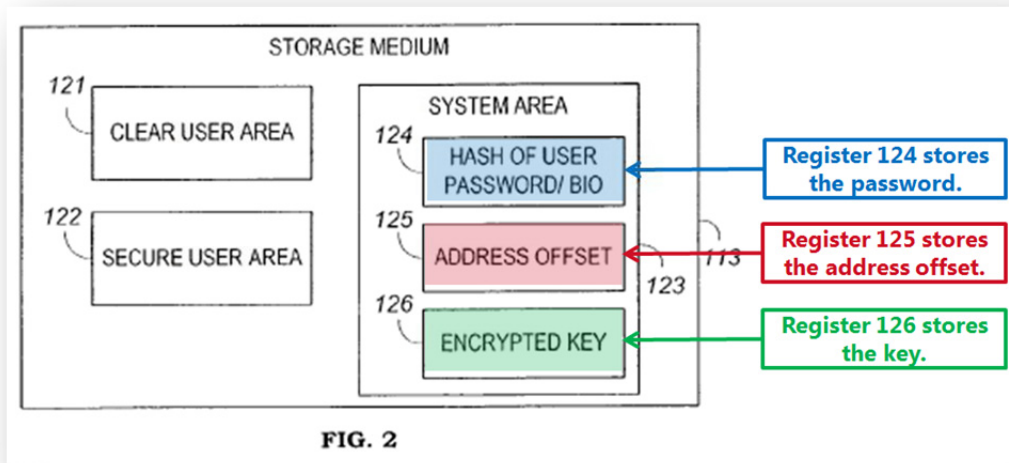
FIG. 2

Id. at Fig. 2 (annotated).

The secure memory area is activated when the host transmits a valid password to the controller. *Id*. at 6:15-22. Then the memory controller remounts the memory by using the stored address offset in the register to point to the secure partition (as illustrated in Fig. 4B). *Id*. at 6:42-49, Fig. 4B (shown below).

Before verification of the entered password, memory controller uses an address offset to point to unprotected memory area.

Unprotected memory area _does not require_ password to access.

After verification of the entered password, memory controller uses a new address offset to point to secure memory area.

Secure user area _requires_ password to access.

FIG. 4A   FIG. 4B

Id. at Figs. 4A-B (annotated).

C.   United States Patent No. 6,681,304 (*Vogt*)

Vogt was filed Jun. 30, 2000 and issued on Jan. 20, 2004. *Vogt* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Vogt* was not previously presented to the PTO in the context of the '180 Patent.

Vogt teaches a "password verify" command to access hidden storage in a memory device. Ex. 1005 at 6:35-37, 8:11-30, 11:53-55.

D.   United States Patent No. 6,279,114 (*Toombs*)

Toombs was filed Nov. 4, 1998, and issued on Aug. 21, 2001. *Toombs* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Toombs* was not previously presented to the PTO in the context of the '180 Patent.
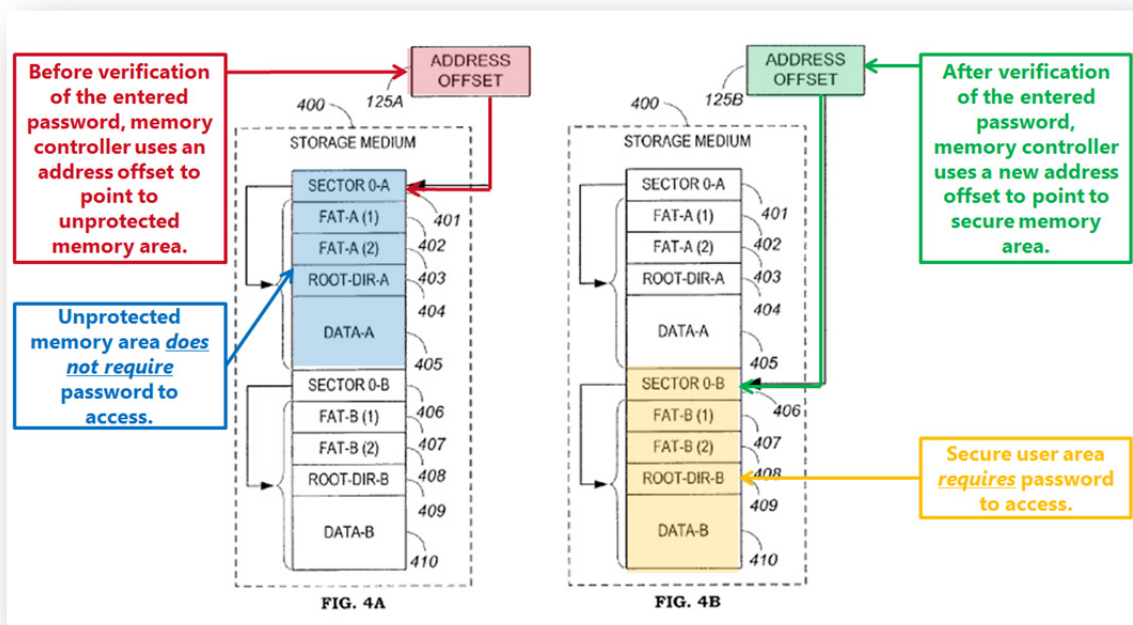
Toombs teaches a MultiMediaCard having parameters stored in various registers as shown in Fig. 14 below. Ex. 1006 at 1:9-14, 6:18-38, 10:22-33, Fig. 14.
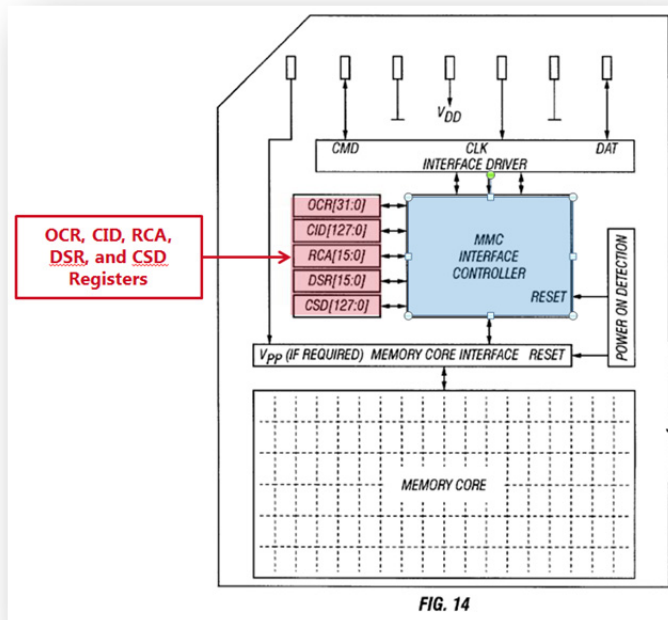
FIG. 14

Id. at Fig. 14 (annotated).

Toombs also teaches two types of data transfer processes. *Id*. at 8:34-34. One type involves sequential data transfer commands, which initiate a sequential, "continuous data stream." *Id*. at 8:35-37; Fig. 5, 7 (shown below); Ex 1002 at ¶191. The sequential data transfer commands reduce command overhead to a minimum, because data is transferred sequentially in a DAT line. Ex. 1006 at 8:39-43.

FIG. 5

FIG. 7
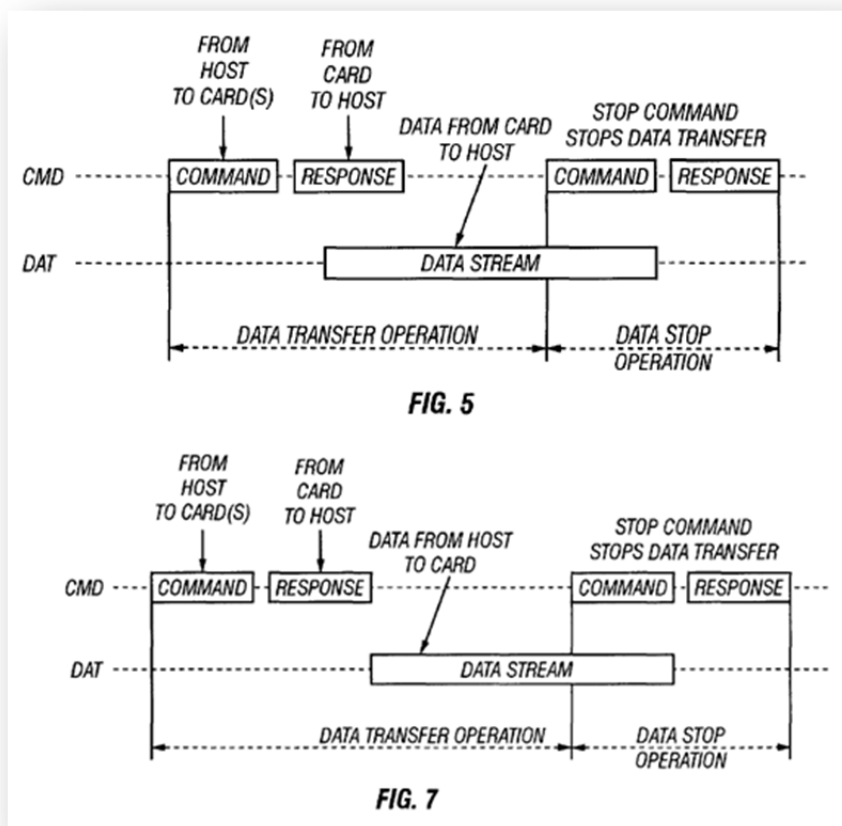
Id. at Figs. 5, 7.

E. United States Patent No. 7,409,489 (*Sinclair*)

Sinclair was filed on Oct. 25, 2005, claims priority to U.S. Provisional App. No. 60/705,388 filed on Aug. 3, 2005, and was published on Feb. 8, 2007. *Sinclair* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Sinclair* was not previously presented to the PTO in the context of the '180 Patent.

Sinclair discloses selectable reclaim operation modes that provide optimizations to the rate that memory reclaim operations (*i.e.,* background/management operations) occur. Ex. 1007 at Abstract. Reclaim

operations convert memory containing obsolete data into writeable memory. *Id.* at 2:9-11. An exemplary reclaim operation mode is the Reclaim Normal mode, which can be activated by the host sending a "Reclaim_normal" command to the memory controller. *Id.* at 23:27-30, 23:47-51. This changes the configuration of the memory device to interject reclaim operations between write commands received from the host. *Id.* at 23:47-51, 2:50-57. The device calculates an optimal interleave ratio of reclaim operations to write commands such that the memory card will run out of writeable memory only when no reclaimable memory remains. *Id.* at 2:50-57.
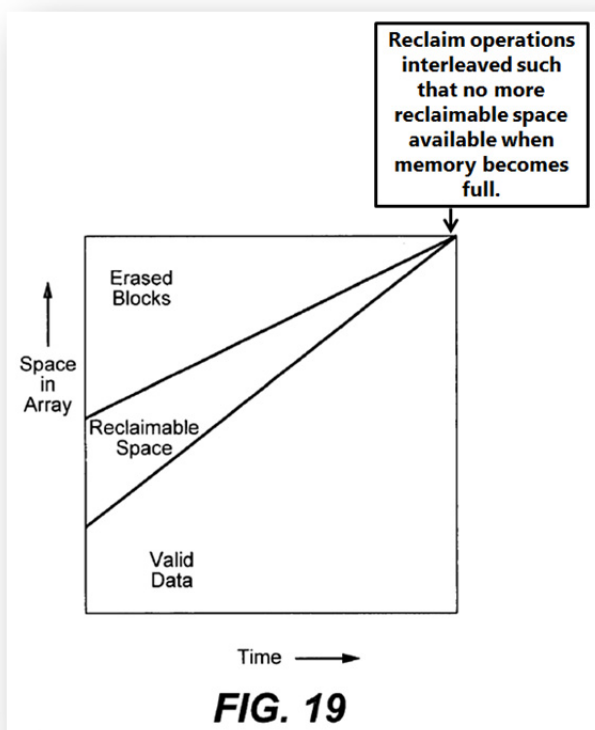
FIG. 19

Id. at Fig. 19 (displaying a time graph illustrating an optimal interleave of reclaim operations to write operations) (annotated).

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The interleave ratio can be recalculated periodically or when triggered by a host command. *Id*. at 18:17-26. As shown in Fig. 20, when host issues a delete command to the memory device at time t10, the system alters the interleave ratio such that the time when no more reclaimable space is available shifts to the newly anticipated time when the memory will be filled to capacity. *Id*. at 18:12-26.
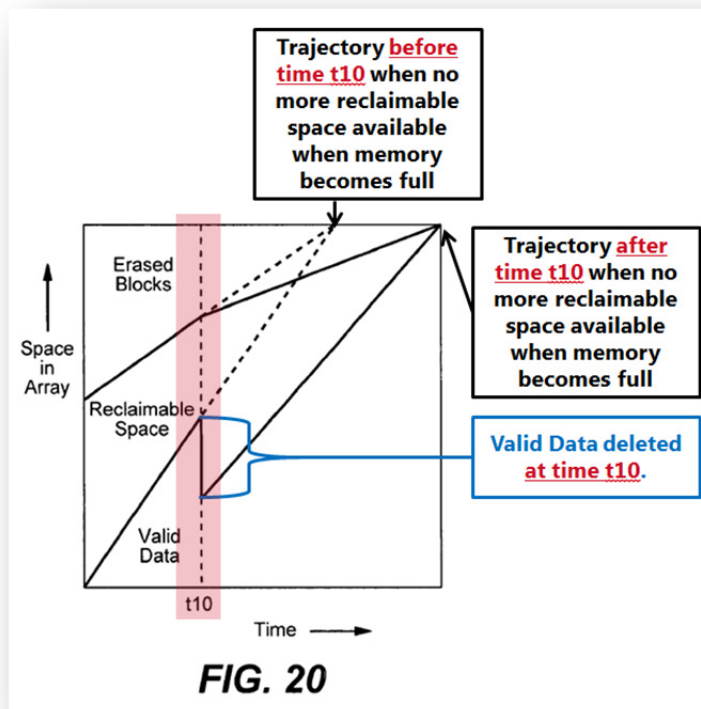
FIG. 20

Id. at Fig. 20 (annotated).

Sinclair also describes other reclaim modes selectable by the host, such that that "the host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity." *Id*. at 23:27-30, 23:36-59.

IX.   GROUNDS FOR CHALLENGE

Inter partes review of Claims 17-27 and 31-34 of the '180 Patent is requested as follows.

A.   GROUND 1: Claims 17-27, 31-32, and 34 are unpatentable under 35 U.S.C. § 102 over *CompactFlash*.

1.   Independent Claim 17

(i)   A memory device, comprising:

The CompactFlash device is a memory device and contains a "controller and flash memory module(s)." Ex. 1003 at 19.

Figure 1: CompactFlash Storage Card Block Diagram
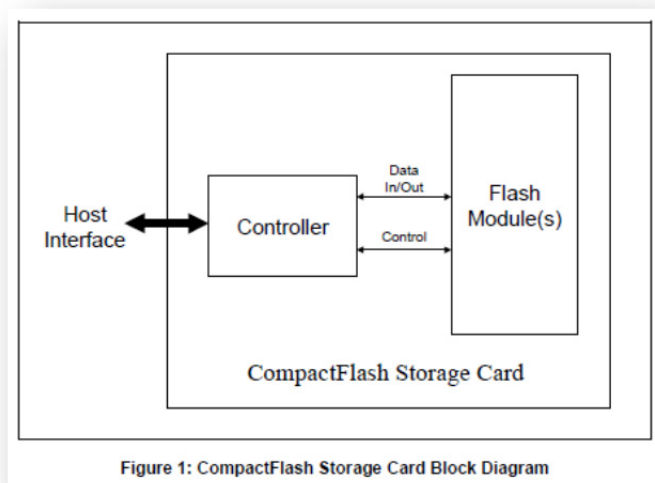
Ex. 1003 at 19.

> **(ii)** **one or more registers for storing one or more predefined access profiles associated with said memory device,**

Predefined Access Profiles

CompactFlash discloses MultiWord and Ultra DMA modes stored in a register on the CompactFlash device. As shown in Table 53, various MultiWord DMA and Ultra DMA modes are supported, each of which constitutes a pre-defined access profile.

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Id. at 158 (equating MultiWord DMA and Ultra DMA "Mode[s]" as "transfer mode number[s]"). For example, the following Ultra DMA Modes are possible:

> #### 6.2.1.6.26 Word 88: Ultra DMA Modes Supported and Selected
>
> ### * * *
>
> Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 Shall be set to 1.
>
> Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 Shall be set to 1.
>
> Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 Shall be set to 1.
>
> Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 Shall be set to 1.
>
> Bit 0: 1 = Ultra DMA mode 0 is supported

Id. at 132-33, 137.

Each DMA mode is an access profile, because the selected mode is used to determine the memory device configuration for the subsequent DMA access operations to the memory device. *See* Ex. 1001 at 3:56-58 ("***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device***.") (emphasis supplied); Ex. 1002 at ¶¶206-11. For instance, if an Ultra DMA mode is activated (unlike MultiWord DMA modes) the device configures itself to perform a CRC check calculation after the data transfer. Ex. 1003 at 90 ("CRC errors are detected and reported only while operating in Ultra mode."). In addition, unlike the MultiWord DMA modes, each Ultra DMA mode utilizes both the rising and falling edge of the clock signal to transfer data and utilizes HDMARDY, DDMARDY, and DSTROBE signals, which are not party of a MultiWord DMA access operation. Ex. 1002 at ¶209; Ex.

1003 at 44, Fig. 32 (illustrating the MultiWord DMA transfer initialization process).

Furthermore, each Ultra DMA mode is different. As an example, after a pause in an Ultra DMA data burst, a memory device will be prepared to receive up to two additional data words for Ultra DMA Modes 0-2 and up to three additional data word for DMA Modes 3-5. *Id*. at 70. Finally, each mode is associated with different maximum transfer rates. *Id*. at Tables 21-22; Ex. 1002 at ¶240.

Each MultiWord and Ultra DMA mode is effective for determining access configuration for the usage. Specifically, the controller configures the CompactFlash device for an access operation according to the host-selected DMA mode. *Cf*. Ex. 1007 at Fig. 32 with Ex. 1007 at Figs. 32, 38 (illustrating the difference in initialization process between a MultiWord DMA transfer and an Ultra DMA transfer). For example, enabling an Ultra DMA mode causes the controller to initiate the Ultra DMA protocol (rather than the MultiWord DMA protocol) when receiving a READ DMA or WRITE DMA command (*i.e.,* at least one usage of the memory device) from the host. Ex. 1003 at 68. Similarly, enabling a MultiWord DMA mode causes the controller to initiate the MultiWord DMA protocol (rather than the Ultra DMA protocol) when receiving a READ DMA or WRITE DMA command (*i.e.,* usage) from the host. Ex. 1003 at 68; Ex. 1002 at ¶207-09.

These DMA modes are access profiles because use of each DMA Mode requires the use of a specific DMA *protocol*, not merely the selection of particular timing characteristics. Ex. 1003 at 68 ("[T]he *Ultra DMA protocol* shall be used instead of the *Multiword DMA protocol.…* This protocol applies to the Ultra DMA data burst only."). *See* Ex. 1008 at 266-67. Moreover, in the example of Ultra DMA, "[s]everal signal lines are redefined to provide different functions during an Ultra DMA burst." *Id*. at 68.

Furthermore, unlike the Patent Owner's argument in the Prosecution History that changing the operating speed does not affect an access operation, the DMA modes ***directly affect*** access operations. Ex. 1008 at 266-67. The selected DMA mode dictates the specific DMA protocol that the memory device utilizes. Moreover, the selection of an Ultra DMA profile rather than a MultiWord DMA profile requires the device to perform a CRC comparison to ensure the accuracy of the data transferred. Ex. 1003 at 90 ("CRC errors are detected and reported ***only while operating in an Ultra mode***.") (emphasis supplied); Ex. 1002 at ¶208.

One or More Registers

The predefined profiles are stored in the card and are available via the "IDENTIFY DEVICE data [which] indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting." Ex. 1003 at 69, 128 ("Table 47 specifies ... data returned by the Identify Device Command"), 132-33.

The IDENTIFY DEVICE data also indicates support of certain MultiWord DMA
modes. *Id*. at 132-33.

Word Address	Default Value	Total Bytes	Data Field Type Information
			Table 47: Identify Device Information
			* * *
63	0X0Xh	2	Multiword DMA transfer. In PCMCIA mode this value shall be 0h
64	00XXh	2	Advanced PIO modes supported
65	XXXXh	2	Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h
66	XXXXh	2	Recommended Multiword DMA transfer cycle time. In PCMCIA mode this value shall be 0h
67	XXXXh	2	Minimum PIO transfer cycle time without flow control
68	XXXXh	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	XXXXh	6	Features/command sets supported
85-87	XXXXh	6	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode Supported and Selected

For instance, Word 88 of the Identify Device Information "identifies the
Ultra DMA transfer modes supported by the device and indicates the mode that is
currently selected." *Id* at 137. This data is stored in a portion of memory (*i.e.,* a
register) in the device, and is made available to the host via a "buffer" (*i.e.,*
register),[2] which the host can access, in response to an IDENTIFY DEVICE

---

[2] All host/card communication "is done using the Task File ***registers***, which
provide all the necessary registers for control and status information related to
the storage medium." Ex. 1003 at 110 (emphasis supplied).

command. Ex. 1002 at ¶204; Ex. 1003 at 128 ("The parameter words in the buffer have the ... meanings defined in Table 47[.]").

Moreover, when the host selects a supported profile, the selected access profile is stored in a register in the CompactFlash device. For example, the host may use the "Set transfer mode subcommand" (designated "Feature 03h") which is part of the "SET FEATURES" command to "select the Ultra DMA mode at which the system operates." Ex 1003 at 69, 156-58. When invoking this subcommand, the selected MultiWord or Ultra DMA mode is identified by storing a value corresponding to the selected access profile "in the Sector Count *register*." Ex. 1003 at 157 (emphasis supplied).

> **(iii)** **said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;**

As discussed above, *CompactFlash* discloses that each MultiWord and Ultra DMA mode (*i.e.*, predefined access profile) is effective for determining how access to the memory device is configured for a usage. *See supra* Section VIII.A.1(i).

The "usage" in *CompactFlash* relates to the host activity in accordance with the selected DMA mode (*e.g.*, a READ DMA or WRITE DMA operation). *Id*. at 68. Specifically, the controller configures the CompactFlash device for a host-initiated access operation according to the host-selected DMA mode. *Cf.* Ex. 1003 at Fig. 32 *with id*. at Figs. 32, 38 (illustrating the difference in initialization process

between a MultiWord DMA transfer and an Ultra DMA transfer). For example, enabling an Ultra DMA mode causes the controller to initiate the Ultra DMA protocol (rather than the MultiWord DMA protocol) when receiving a READ DMA or WRITE DMA command from the host. *Id*. at 68. Similarly, enabling a MultiWord DMA mode causes the controller to initiate the MultiWord DMA protocol (rather than the Ultra DMA protocol) when receiving a READ DMA or WRITE DMA command from the host. *Id*. at 68.

> **(iv) a controller for receiving one or more commands related to said at least one usage of said memory device**

CompactFlash has a CompactFlash controller, which receives a SET FEATURES command from the host. The SET FEATURES command is communicated from the host to the CompactFlash controller to select one of the MultiWord or Ultra DMA modes. *Id*. at 15, 156-57. The SET FEATURES command instructs the controller to set the DMA mode to the selected MultiWord DMA mode or Ultra DMA mode for subsequent DMA access operations (*i.e.*, the usage), such as READ DMA and WRITE DMA. *Id*. at 15, 157-58.

Figure 1: CompactFlash Storage Card Block Diagram
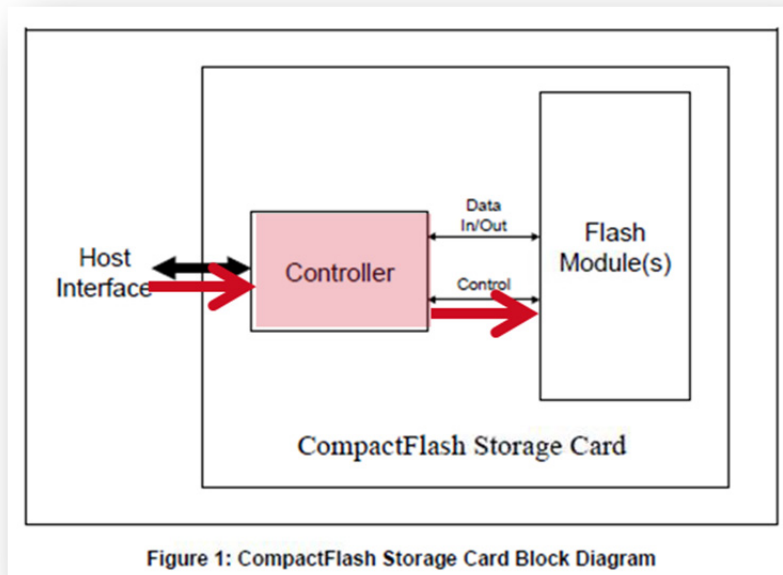
Id. at Fig. 1 (annotated).

> **(v)** **said one or more commands for activating said one or more predefined access profiles associated with said memory device,**

The SET FEATURES command sent from the host activates a selected MultiWord DMA mode or Ultra DMA mode (*i.e.*, a predefined access profile) from among the available modes supported by the device. *Id*. at 157, Table 53 (indicating bits representing a host-selected DMA mode) (shown below).

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Id. at Table 53 (annotated).

For example, for Ultra DMA modes, the Set transfer mode subcommand (using the transfer mode values in Table 53) in the SET FEATURES command allows "a host to select the Ultra DMA mode at which the system operates." *Id*. at 69.

> **(vi) said controller also for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.**

The CompactFlash controller configures the access to the memory device according to the selected DMA mode (*i.e.*, one of the MultiWord or Ultra DMA modes), so that the CompactFlash device is effective to perform a DMA access operation (*i.e.*, usage) using the selected DMA mode.

After a host communicates a READ DMA or WRITE DMA command following the selection of a DMA mode, the controller will begin the DMA-specific initiation protocol to configure access to the memory device for either a

MultiWord DMA transfer or an Ultra DMA transfer in the selected mode. *Id.* at

Figs. 32-33, 38.

For example, in a MultiWord DMA mode, the controller starts the initiation

phase of the MultiWord DMA burst by asserting a DMARQ signal (Step 1 of Fig.

32). The host, in response, asserts a DMACK signal (Step 2 of Fig. 32), and, in

turn, the controller response by asserting the IORD signal (Step 3 of Fig. 32).

Figure 32: True IDE Multiword DMA Mode Read/Write Timing Diagram
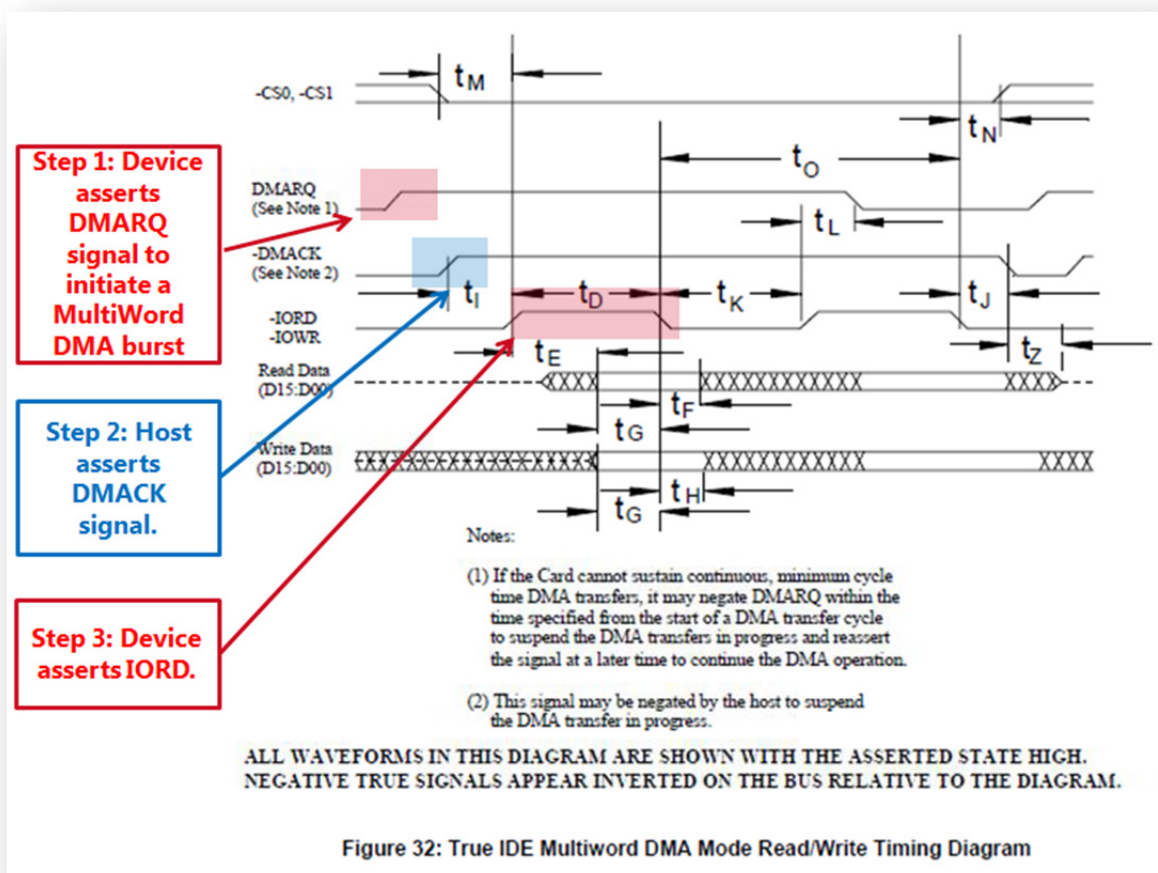
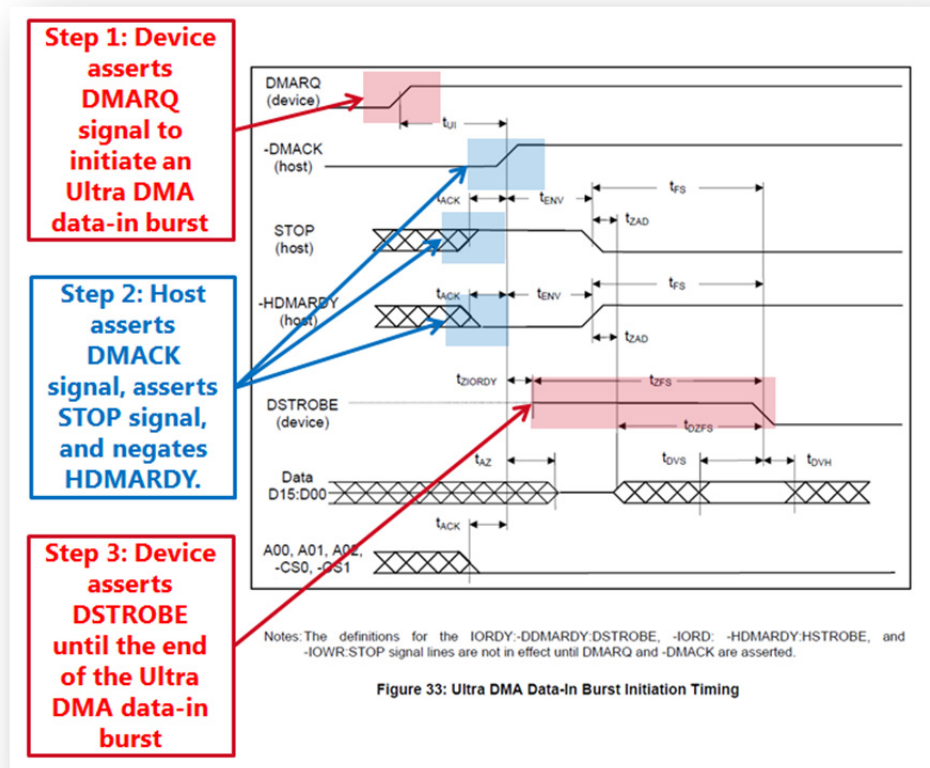*Id.* at Fig. 32 (annotated).

As another example, when an Ultra DMA mode is activated, the controller

starts the initiation phase of the Ultra DMA burst by asserting a DMARQ signal (Step 1 of Fig. 33). Ex. 1003 at 76. The host then asserts a DMACK signal (Step 2 of Fig. 33). *Id.* at Fig. 33. Only at that point do the other signal lines become effective, permitting the transfer. *Id.* ("The definitions for the …DSTROBE… and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted). The device will assert a DSTROBE signal line to start the data-in burst (Step 3 of Fig. 33). *Id.* at Fig. 33.

Id. at Fig. 33 (annotated).

For a data-out burst, the device will wait to negate any signal until generating a STROBE edge (*see* Step 3 of Fig. 38). *Id.* at 70. At this point, the

memory device is now configured for usage (*i.e.*, to perform a data transfer under the selected Ultra DMA mode).

Figure 38: Ultra DMA Data-Out Burst Initiation Timing
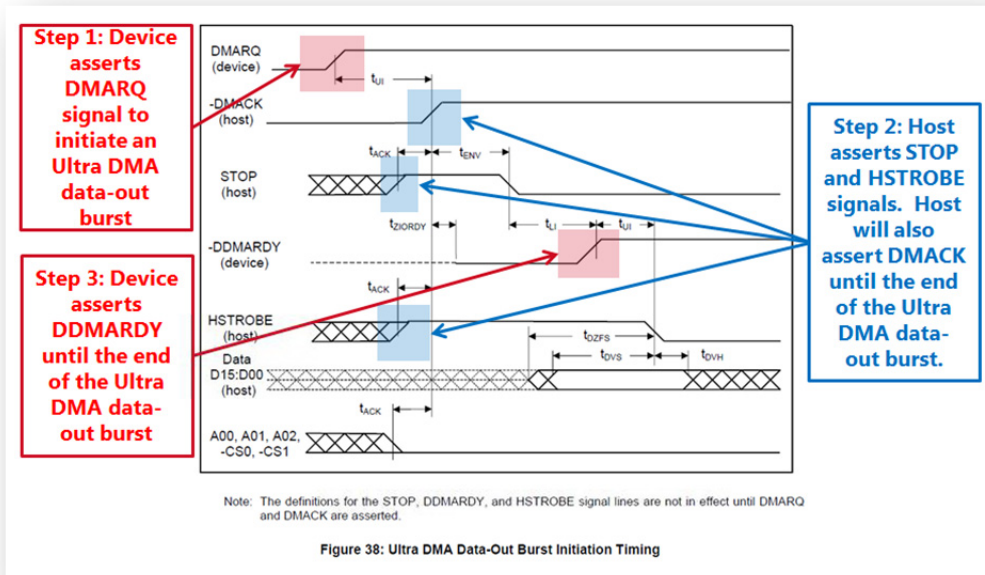
Id. at Fig. 38 (annotated).

2. Dependent Claim 18

(i) **The memory device of claim 17, wherein said one or more access profiles correspond to at least one of a random and a sequential mode of access.**

CompactFlash discloses a READ DMA and WRITE DMA command under one of the MultiWord or Ultra DMA modes (*i.e.*, a predefined access profile) that corresponds to a sequential mode of access. Ex. 1003 at 145 ("[The Read DMA] command uses DMA mode *to read from 1 to 256 sectors as specified in the Sector Count* register.... *The transfer begins at the sector specified in the Sector Number* Register"), 164 ("[The Write DMA] command uses DMA mode *to write*

from 1 to 256 sectors as specified in the Sector Count register.... *The transfer begins at the sector specified in the Sector Number* Register."). The CompactFlash device performs read and write access operations by accessing the starting place of the transfer in the memory (*i.e.,* the Sector Number) and continuing for a number of sequential sectors (*i.e.,* the Sector Count). *Id.* at 145, 164; Ex. 1002 at ¶¶221-30.

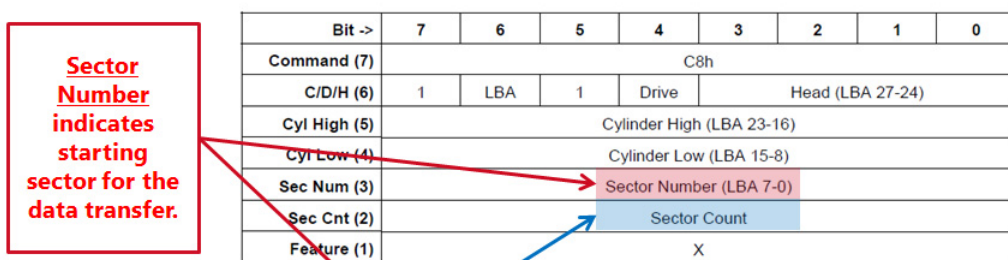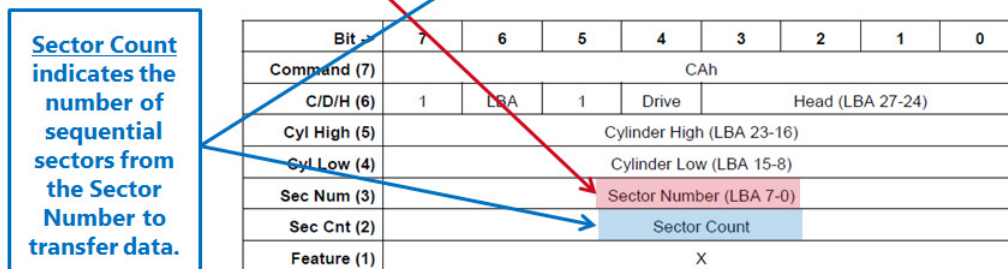
Figure 69: Read DMA

Figure 91: Write DMA

Ex. 1003 at Figs. 69, 91 (annotated).

Accordingly, READ and WRITE DMA operations correspond to a sequential mode of access. *See id.* at 145; Ex. 1002 at ¶229. Both start at a specified Sector Number and continue to access (*i.e.,* read or write) in sequence the number sectors indicated in the Sector Count. Ex. 1003 at 145, 164; Ex. 1002 at ¶¶221-28.

> **3.** **Dependent Claim 19**
>
> > **(i)** **The memory device of claim 18, wherein said access profiles correspond to at least one of a read, a write, an erase, and a modify attribute operation.**

In *CompactFlash*, the various DMA profiles correspond to and support READ DMA (*i.e.*, a read operation) and WRITE DMA (*i.e.*, a write operation). Ex. 1003 at 145, 164.

> **4.** **Dependent Claim 20**
>
> > **(i)** **The memory device of claim 17, wherein said one or more access profiles are adapted to accommodate repeated access requests to an identical address of said memory device.**

In *CompactFlash*, the MultiWord and Ultra DMA modes (*i.e.*, predefined access profiles) accommodate repeated access requests to an identical address of the CompactFlash device. A READ DMA operation under one of the MultiWord or Ultra DMA modes may read data bits in an identical address of the memory device that a previous READ DMA operation already read or a WRITE DMA operation already wrote. Ex. 1002 at ¶235-36. Similarly, a WRITE DMA operation under one of the MultiWord or Ultra DMA modes may write data bits in an identical address to which the WRITE DMA operation already wrote or a READ DMA operation already read. *Id*. at ¶237.

5.   Dependent Claim 21

> **(i)   The memory device of claim 17, wherein said one or more access profiles are adapted to produce an optimized performance associated with said memory device.**

6.   Dependent Claim 22

> **(i)   The memory device of claim 21, wherein said performance is optimized in accordance with at least one of: data throughput, lifetime, and power consumption associated with said memory device.**

For purposes of the Petition, Petitioner applies Patent Owner's proposed construction in the ITC Matter of the claim term "adapted to produce an optimized performance associated with said device" in Claim 21 to mean "designed to produce an improved memory device performance with higher reliability, increased speed, increased lifetime, or reduced energy consumption, than compared to the same memory device not implementing said one or more access profiles." Ex. 1026 at 3.

Each DMA mode is designed to produce an improved memory device performance with increased speed (*i.e.*, higher throughput). Ex. 1002 at ¶¶240; *see, e.g.*, Ex. 1018 ("Ultra DMA … modes will increase the CompactFlash interface data transfer rate[.]"). Each DMA mode is an optimization as it "reduces the processor power required to manage the CompactFlash data transfers." *Id*. Moreover, at the time of *CompactFlash,* the Ultra DMA modes provided the maximum read and write speed available to CompactFlash devices. *Id*.

In addition, in reading and writing data in an Ultra DMA transfer, the host device and the memory controller perform error detection. Ex. 1003 at 90 ("CRC errors are detected and reported only while operating in Ultra mode."). The host device may select a slower Ultra DMA mode if excessive errors are encountered, thereby improving the reliability of the memory device performance. *Id*.

7. Dependent Claim 23

> **(i)** **The memory device of claim 17, wherein said one or more commands comprise a metadata portion for designating a preferred access profile corresponding to said command.**

The "Set transfer mode subcommand" (*i.e.*, metadata portion) in the SET FEATURES command is used by a host to designate a preferred access profile (*i.e.,* selected DMA mode). The "Set transfer mode subcommand" in the SET FEATURES command comprises metadata, because the subcommand provides data about the selected feature (*i.e.,* the selected DMA transfer mode of the modes selectable using the set transfer mode subcommand). Ex. 1003 69; Ex. 1002 at ¶¶244-45.

8. **Dependent Claim 24**

    (i) **The memory device of claim 23, wherein a specific memory location is utilized in accordance with said access profile.**

9. **Dependent Claim 25**

    (i) **The memory device of claim 24, wherein said specific memory location comprises a section of said memory device with special characteristics.**

10. **Dependent Claim 26**

    (i) **The memory device of claim 24, where said specific memory location comprises a separate physical memory chip.**

A specific memory location is utilized in accordance with the access profile. Specifically, a CompactFlash drive may contain multiple memory cards (called "drives"). Ex. 1003 at 117, Fig. 1 (illustrating that a CompactFlash device may contain multiple flash modules); Ex. 1002 at ¶247. The host uses the Drive/Head Register (bit 4) to select a particular "drive (card)" for data access. Ex. 1003 at 117; Ex. 1002 at ¶248. Once selected, the memory device will perform DMA data transfers in accordance with the selected access profile (*i.e.*, selected MultiWord or Ultra DMA mode) to/from the selected card. Ex. 1003 at 117; Ex. 1002 at ¶249. Table 45 explains how the Read/Write DMA command utilizes the Card/Drive/Head Register and the SET FEATURES command utilizes the Drive parameter. Ex. 1003 at Table 45.

Table 45: CF-ATA Command Set

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
				* * *				
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA	C8h	-	Y	Y	Y	Y	Y
				* * *				
1	Set Features	EFh	Y	-	-	-	D	-
				* * *				
2	Write DMA	CAh	-	Y	Y	Y	Y	Y
				* * *				

'Y' indicates that the Drive/Head parameter is used in the command.

'D' indicates that the Drive parameter (not the head parameter) is used.

Id. at Table 45 (annotated).

Each memory drive is a specified memory location that has special characteristics. Ex. 1003 at 107; Ex. 1002 at ¶255. A memory drive, for instance, may support a different set of DMA modes (*i.e.*, special characteristic) than a second memory drive. Ex. 1003 at 107; Ex. 1002 at ¶255.

Moreover, the first memory drive may be a separate physical memory chip from the second memory drive. Ex. 1003 at 107; Ex. 1002 at ¶257. In addition, because the CompactFlash drive is removable, these physical memory chips are separate from the host device. Ex. 1003 at 18; Ex. 1002 at ¶258.

11. Dependent Claim 27

> **(i)   The memory device of claim 17, wherein said one or more access profiles are associated with one or more partitions of said memory device.**

Each Multiword and Ultra DMA mode is associated with at least one partition of the CompactFlash device: common memory. Ex. 1001 at 7:36-37 ("[P]artitions may comprise ... *physical* partitions of the memory device") (emphasis supplied); Ex. 1003 at 110, 113 (specifying that the registers in the memory mapped addressing are in common memory). The common memory is a physical partition that includes storage for the CompactFlash memory. *Id*. at 110; Ex. 1002 at ¶260-61.

During a DMA transfer, data in the common memory is accessed. Ex. 1003 at 110 ("The communication to or from the CompactFlash Storage Card is done using the Task File registers, *which provide all the necessary registers for control and status information related to the storage medium*.") (emphasis supplied), 115 (specifying that in memory mapped addressing the Task File registers are in common memory); Ex. 1002 at ¶261. Accordingly, DMA profiles for *CompactFlash* are associated with the common memory partition.

12. Dependent Claim 31

> (i) **The memory device of claim 17, wherein said memory device is used to effect both mass memory and system memory implementations.**

The CompactFlash device may effect mass memory as the device may be used as mass memory. Ex. 1003 at 15; Ex. 1002 at ¶264. The CompactFlash device may use common memory (*i.e.,* mass memory) to store user data. Ex. 1003 at 110; Ex. 1002 at ¶264.

Second, the CompactFlash device effects system memory implementations because system memory data, like card identification and configuration information, are stored in the attribute memory of the CompactFlash device. Ex. 1003 at 95; Ex. 1002 at ¶265. Moreover, the card may be used to "completely replace[] conventional disk storage" in a host, and be used as "the root storage device" by an operating system. Ex. 1003 at 130.

13. Dependent Claim 32

> (i) **The memory device of claim 17, further comprising a default access profile that is used to configure said memory device upon power up.**

When executing a power-on or hardware reset, *CompactFlash* discloses that the device may revert to a default non-Ultra DMA mode, like a MultiWord DMA mode. Ex. 1003 at 69. As discussed above, each MultiWord DMA mode may be an access profile. *See supra* VIII.A.1(ii); Ex. 1002 at ¶267.

14. Dependent Claim 34

(i) The memory device of claim 17, wherein a currently active access profile resides in a designated memory register.

CompactFlash discloses a designated portion of the memory device (*i.e.,* register) to store the active access profile. Specifically, bits 8-10 of Words 63 and bits 8-12 of Word 88 indicates the DMA mode that is currently selected and active. Ex. 1003 at 137.

B. GROUND 2: Claims 17, 20-27, and 31-34 are unpatentable under 35 U.S.C. § 103(a) over *Ziv* and *Vogt*.

1. Independent Claim 17

(i) A memory device, comprising:

Ziv discloses a memory device, such as a portable storage device that includes a storage memory. Ex. 1004 at 3:48-55, Fig. 2.
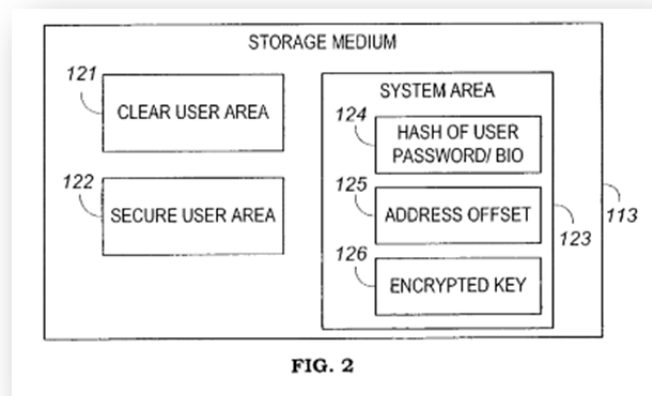
FIG. 2

Id. at Fig. 2.

> **(ii)** **one or more registers for storing one or more predefined access profiles associated with said memory device,**

One or More Registers

Ziv discloses a predefined access profile that contains a password hash, an address offset, and a key, which are predefined. *Id*. at 5:1-25 (describing initial setup); Ex. 1002 at ¶¶280-83. The password hash, address offset, and key are each stored in registers (as illustrated in Fig. 2). Ex. 1004 at 4:16-20, Fig. 2.
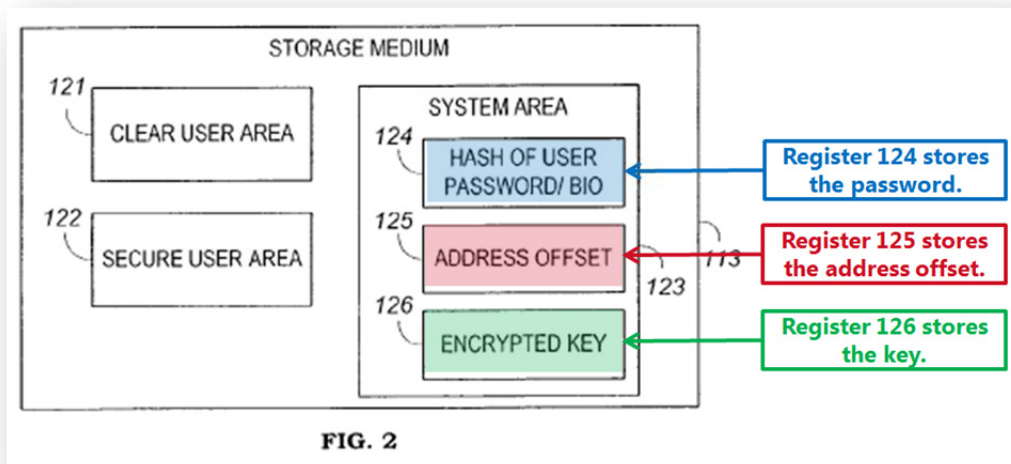
FIG. 2

*Id*. at Fig. 2 (annotated).

Predefined Access Profile

The password hash, address offset, and key in *Ziv* constitutes a predefined access profile that governs the access operations to the memory. *See* Ex. 1001 at 3:56-58 ("***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device***.") (emphasis

supplied). Additionally, each of these components forms an access profile. Ex. 1002 at ¶¶280.

Access to the secure user data is only available when a hash of an entered password matches the password hash stored in the register. Ex. 1004 at 4:11-12 ("[A] secure area 122 that contains secure user data [is] accessible only upon the provision of a password[.]"). In addition, the address offset governs access operations to the memory. After entering the proper password, the memory device uses the stored address offset to properly view the secure memory area. Ex. 1004 at 6:46-48 ("[H]ost 101 will seek 'sector 0' of the remounted device, controller 111 will use offset 125B to point at 'sector 0-B' 406[.]"). Without the address offset, the secure area will not be properly mounted. *Id.*; Ex. 1002 at ¶282.

FIG. 4A   FIG. 4B

United States Patent No. 8,307,180
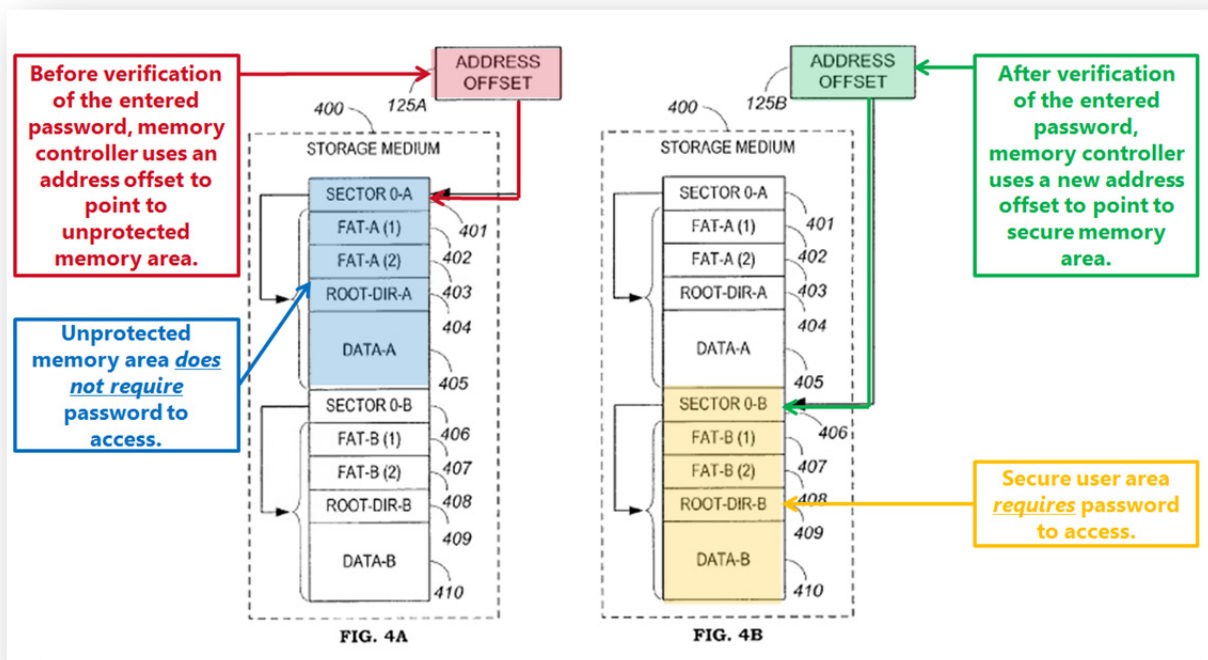
Ex. 1004 at Fig. 4A-4B (illustrating the use of the address offset to access the secure area) (annotated).

Moreover, the key governs the access operations to the memory. The key is the "permanent encryption key for all data stored in the secure memory." *Id*. at 7:7-9. Without the key, a user cannot read or write to the secure area. *Id*. at 7:7-9, 7:36-46 (instructing the controller to decrypt data being read from and encrypt data being read to the secure memory area using the key), Fig. 10 (shown below); Ex. 1002 at ¶283.
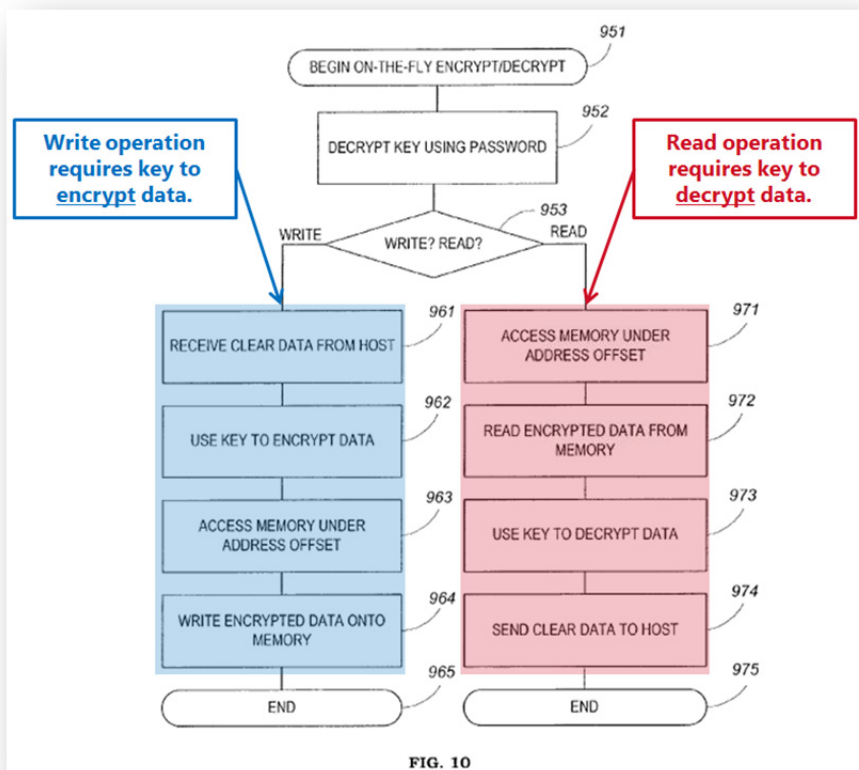

FIG. 10

Ex. 1004 at Fig. 10 (annotated).

          (iii)   **said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;**

The "at least one usage," in the context of *Ziv*, is the host's access to the secure memory area. *See* Ex. 1004 at 1:60-63.

As explained with respect to the previous claim element, the password hash, address, and key in *Ziv* are all effective for determining how access to the memory device is configured, as each is necessary to view, read from, or write to the secure memory area. Ex. 1002 at ¶¶288-90.

          (iv)   **a controller for receiving one or more commands related to said at least one usage of said memory device**

Ziv discloses a controller (microprocessor) in the memory device that receives a command indicating the password entered to gain access the secure area. Ex. 1004 at 6:42-44 ("*[C]ontroller 111* dismounts and remounts portable storage device 110[.]") (emphasis supplied). A skilled artisan would understand the microprocessor to be a controller. Ex. 1002 at ¶292.
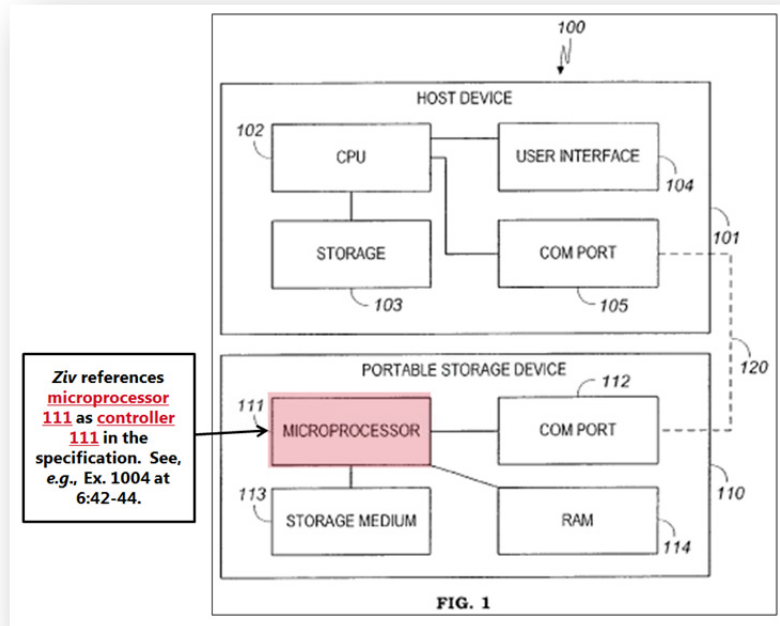
FIG. 1

Ex. 1004 at Fig. 1 (annotated).

The controller receives a command indicating the password entered. *Id*. at 6:19-30 ("If the password has been entered ... via user interface 104, then in step 702 this password is moved to microprocessor 111.... [T]he hashed entered password is then compared to the hashed stored password in register 124."), Fig. 1 (below). In other words, the host system instructs (*i.e.,* sends a command to) the controller (microprocessor) to use the entered password to gain access to the secure memory area (*i.e.,* the usage). Ex. 1002 at ¶293.
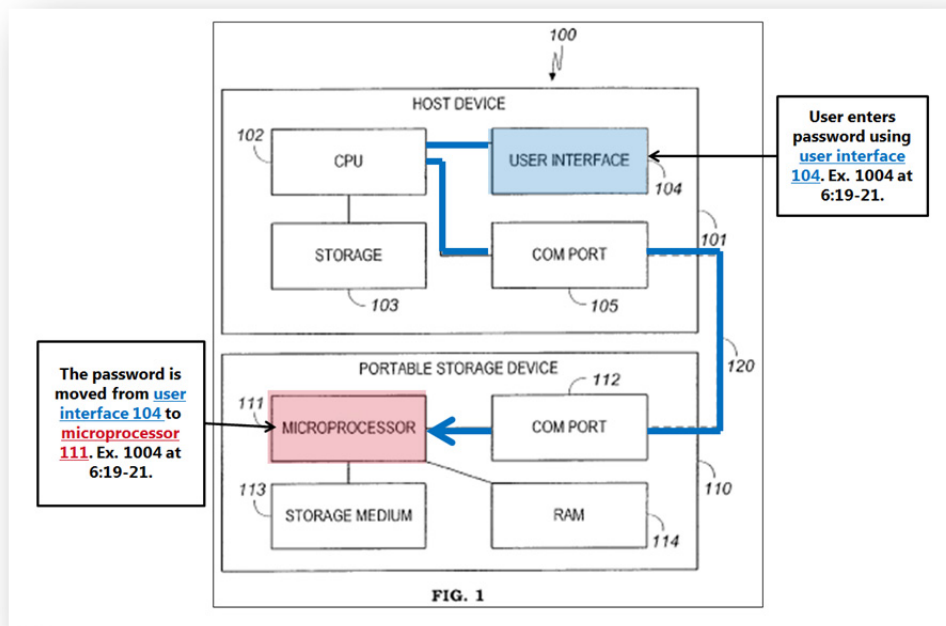
Ex. 1004 at Fig. 1 (annotated).

To the extent that Board disagrees that an instruction to use the entered password to gain access to the secure memory area in *Ziv* teaches the claimed "command," it would have been obvious nevertheless to use the command-based password authentication method in *Vogt* in the memory device of *Ziv*. In particular, *Vogt* discloses a "password verify" command that communicates the entered password to the flash device, like a MMC card. Ex. 1005 at 6:36-38 ("The OS sends a 'password verify' command to the flash. ***The command*** ... ***includes the entered password***.") (emphasis supplied). The "password verify" command instructs the internal processor to "compare[] the entered password with the stored password value." Ex. 1005 at 6:30-32.

It would have been obvious to combine the teachings of *Ziv* and *Vogt* to form a memory controller that receives the "password verify" command in *Vogt* for the following reasons.

Simple Substitution of One Known Element for Another

Ziv's memory device differs from the claimed device at most by the command element. Ex. 1002 at ¶270. Commands, especially commands communicating a password, were well-known in the art to be a fundamental approach to communicating information between devices. *Id*. at ¶¶270, 273; Ex. 1005 at 6:36-38. One of ordinary skill could have substituted one known element (a controller receiving a password) for the other (a controller receiving a command containing the password) and the results would have been predictable (a controller receiving a command containing the password). Ex. 1002 at ¶¶270-73.

Moreover, those predictable results would have included the known advantages of *Ziv*'s memory device, which provides access to a secure memory area, and the known advantages of a command, which include reliably and efficiently communicating a password from the host system to memory device. Ex. 1004 at 6:19-23; Ex. 1005 at 3:23-24; Ex. 1002 at ¶273.

Analogous Art

One of skill in the art would have been motivated to look to the teachings of the prior art due to the similar field, technology, and time frame of *Vogt* and *Ziv*.

Ex. 1002 at ¶274. Both patents concern securing data using non-volatile memory in the early 2000s. Ex. 1004 at 3:48-55; Ex. 1005 at 1:13-15. In addition, both patents describe a solution to a similar problem–improving security of portable flash drives using a secure memory and password. Ex. 1004 at 1:60-63 ("[A] portable storage device for securing data stored in the device in a way that will be both convenient and secure."); Ex. 1005 at 2:5-12 ("Techniques for implementing hidden storage in a non-volatile memory storage," where "[t]he hidden storage area cannot be accessed without a valid password.").

Known Technique to a Known Device to Yield Predictable Results

Base system: *Ziv* discloses a memory device, such as a SecureDigital or CompactFlash device, that receives an entered password from the host system. Ex. 1004 at 6:19-30; Ex. 1002 at ¶276.

Known technique: As shown by *Vogt*, receiving a command containing a password was well known. Ex. 1005 at 6:36-38.

Predictable results and improved system: A POSITA would have recognized that implementing *Vogt*'s structured communication protocol of the "password verify command" in *Ziv*'s memory device would yield the predictable result of a memory device that receives an entered password through a structured command, like the password verify command. Ex. 1002 at ¶277.

As such, using *Vogt*'s password-command implementation of communicating a password was an obvious design choice to implement *Ziv*'s teaching of communicating a password. *Id*. at ¶278.

> **(v)** **said one or more commands for activating said one or more predefined access profiles associated with said memory device,**

As disclosed above, the command is the entering of the password from a host system to the memory controller. *Ziv* further discloses that a password entry from the host triggers several activation procedures associated with the predefined access profile.

The entered password in *Ziv* activates a comparison of a hash of the entered password with the stored password hash. Ex. 1004 at 6:28-30; Ex. 1002 at ¶296.

Additionally, the password in *Ziv* activates the decryption of the stored key. Ex. 1002 at ¶297. When the entered password matches the stored password, the microprocessor decrypts the key of the predefined access profile. Ex. 1004 at 7:32-35.

The communication of a proper password also activates the remounting of the memory according to the address offset. Ex. 1002 at ¶298. After remounting, the stored address offset is used to point to the secure memory area. Ex. 1004 at 6:44-46 ("[W]hen remounting device 110, controller 111 will use an address offset[.]").

Alternatively, the "password verify" command in the *Ziv-Vogt* combination

activates the predefined access profile for substantially similar reasons as discussed

above. Ex. 1005 at 6:30-32; Ex. 1002 at ¶295.

> **(vi)** **said controller also for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.**

The controller in *Ziv* configures access to the secure memory area in

accordance with the password hash, address offset, and key (*i.e.*, predefined access

profile), so that the memory device is effective for the host to view, read from, or

write to the secure memory area (*i.e.*, the usage).

The secure memory area is only accessible when the microprocessor uses the

stored address offset to point to the proper memory sector, which it does after the

user enters the correct password. Ex. 1004 at 6:45-52; Ex. 1002 at ¶300.

The microprocessor must also configure the access operations to perform

on-the-fly encryption/decryption. When accessing the secure memory area, the

microprocessor must apply the encryption key to properly read from and/or write

to the secure memory area. Ex. 1004 at 7:35-46, Fig. 10 (shown below); Ex. 1002

at ¶301.
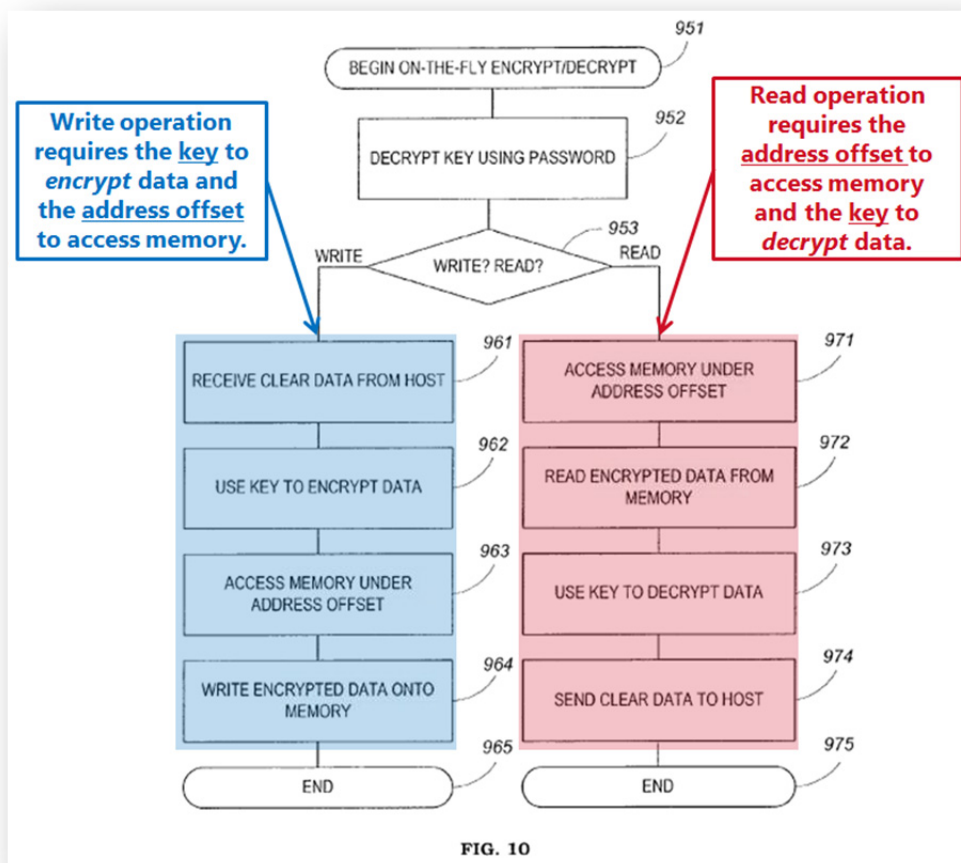
FIG. 10

Ex. 1004 at Fig. 10 (annotated).

2. Dependent Claim 20

(i) **The memory device of claim 17, wherein said one or more access profiles are adapted to accommodate repeated access requests to an identical address of said memory device.**

The stored hashed password, address offset, and key (*i.e.,* the access profile)

can be adapted to accommodate repeated access requests to an identical address of

the memory device of *Ziv*. Once the device verifies the entered password, the

password is adapted to complete a repeated access request without the user

entering a new password. Ex. 1004 at 6:35-38; Ex. 1002 at ¶303. Similarly, the

memory device continuously utilizes the same address offset to point to an

identical address of the memory device for repeated access requests. Ex. 1004 at

6:42-52; Ex. 1002 at ¶304. Finally, the memory device utilizes the same key to

encrypt or decrypt data even when the host repeatedly submits access requests to

an identical memory address. Ex. 1004 at 7:32-47; Ex. 1002 at ¶305.

3. Dependent Claim 21

(i) **The memory device of claim 17, wherein said one or more access profiles are adapted to produce an optimized performance associated with said memory device.**

4. Dependent Claim 22

(i) **The memory device of claim 21, wherein said performance is optimized in accordance with at least one of: data throughput, lifetime, and power consumption associated with said memory device.**

The access profiles in *Ziv* are adapted to produce an optimized performance

when the user enters the password and configures the size of the secure storage

memory area. Ex. 1004 at 5:1-8; Ex. 1002 at ¶307. The provisioning of the

password and secure memory storage size optimizes the performance of the

memory device by the user selecting the appropriate password and memory storage

size deemed fit for the memory device's security and usage. Ex. 1002 at ¶307.

The encryption key and address offset of the access profile also provides an additional optimized performance by allowing the host to properly read from and write to the secure access area of the memory device. *Id*. at ¶308.

Ziv also permits selecting security algorithm optimized to the "desired security level." Ex. 1004 at 1:38-41 ("A file that is considered confidential will be encrypted using a common encryption algorithm such as Data Encryption Standard (DES) or triple-DES using a secret key known only to the user."), 7:9-11 (describing encrypting the key using a "desired security level"); Ex. 1002 at ¶¶309-12. In selecting a security algorithm like DES or triple-DES, the host must balance the speed associated with the security algorithm like DES to the added security that a security algorithm like triple-DES provides. Ex. 1002 at ¶310. For example, a host may implement a DES security algorithm for its speed or a triple-DES security algorithm for its security. Ex. 1022 at 15 ("Triple−DES is a minor variation of DES. Although, three times slower than DES, it can be much more secure if used properly."), Fig. 1-7 (shown below); Ex. 1002 at ¶310.

For triple-DES, the algorithm encrypts the data using a first DES key, decrypts the data using a second DES key, and then encrypts the data with a third DES key. Ex. 1022 at Fig. 1-7.
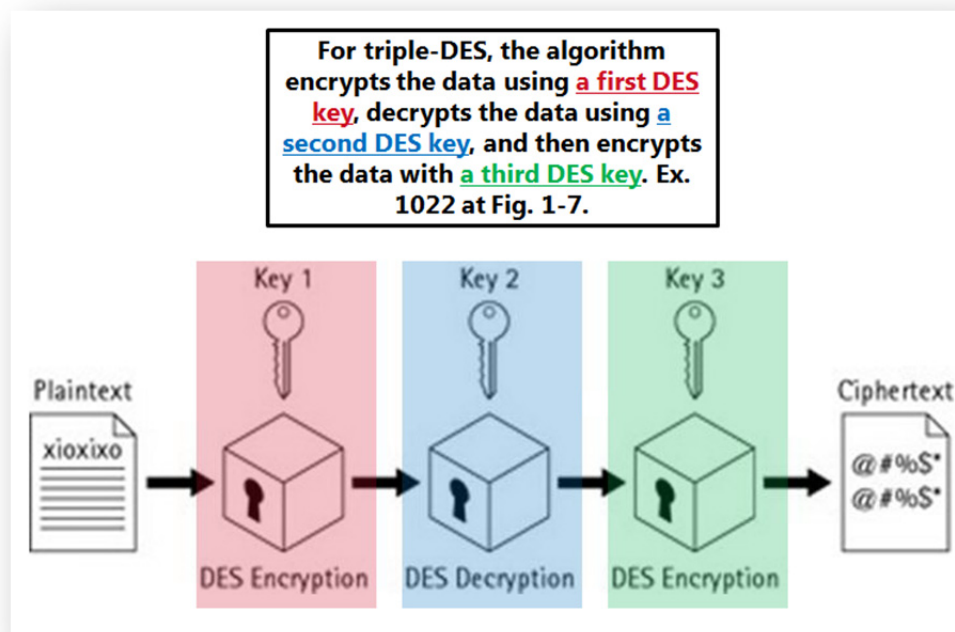
Ex. 1022 at Fig. 1-7 (annotated).

The selection of the security algorithm affects the data throughput by varying the processing time required to encrypt/decrypt data, memory device lifetime by varying the level of security to prevent unauthorized access to data, and power optimization by varying the amount of processor operations required to complete the encryption and decryption. Ex. 1002 at ¶311.

5. Dependent Claim 23

> **(i)** **The memory device of claim 17, wherein said one or more commands comprise a metadata portion for designating a preferred access profile corresponding to said command.**

The "password verify" command in *Vogt* comprises metadata information that identifies the user and the entered password (*i.e.*, predefined access profile).

Ex. 1005 at 6:36-38 ("The OS sends a 'password verify' command to the flash. The command identifies the user (user 1, 2, or 3) and includes the entered password."); Ex. 1002 at ¶315. The entered password designates the preferred access profile corresponding to the command as it defines the user's preference to enter the secure area and designates the user whose password (profile) is to be used. Ex. 1004 at 6:28-30; Ex. 1002 at ¶316.

6. Dependent Claim 24

(i) **The memory device of claim 23, wherein a specific memory location is utilized in accordance with said access profile.**

7. Dependent Claim 25

(i) **The memory device of claim 24, wherein said specific memory location comprises a section of said memory device with special characteristics.**

8. Dependent Claim 26

(i) **The memory device of claim 24, where said specific memory location comprises a separate physical memory chip.**

The secure memory partition is a specific memory location that is utilized with the access profile and is separate from the non-secure area. Ex. 1004 at 4:10-14; *see also id*. at Fig. 2 (shown below). When the entered password activates the access profile, the memory device will access the secure partition of the memory card. *Id*. at 4:11-14.

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Unlike the unsecured memory partition, the secure memory partition contains special characteristics such that "secure user data [is] accessible only upon the provision of a password or biometric signature[.]" *Id.* at 4:11-14, Fig. 2 (shown below).
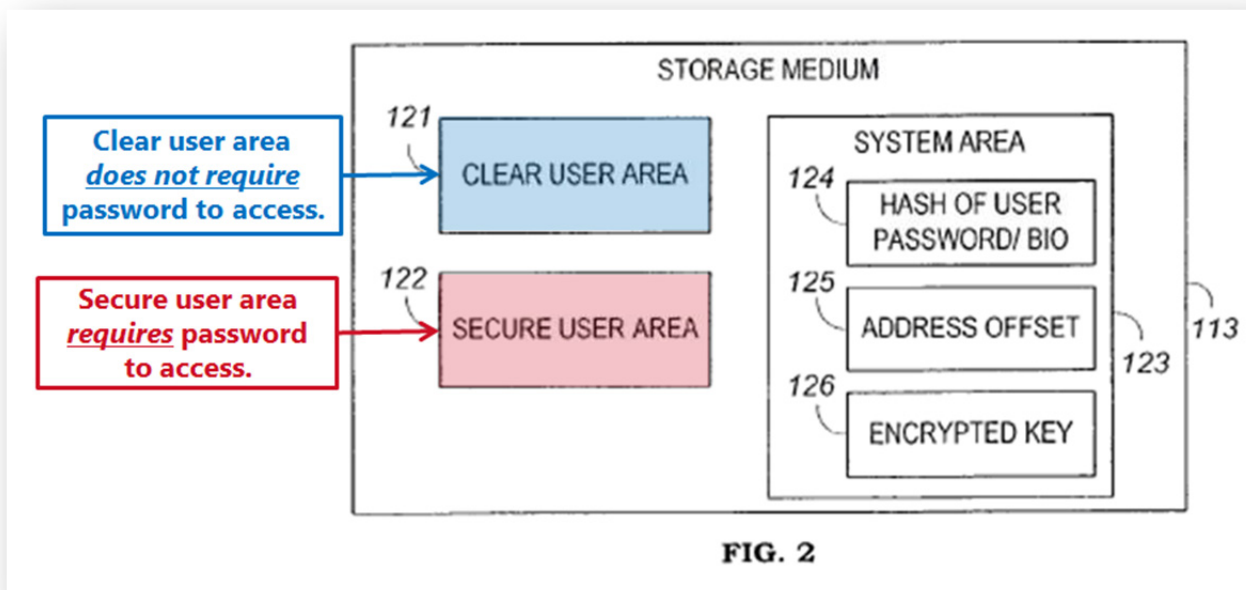
FIG. 2

Ex. 1004 at Fig. 2 (annotated).

Moreover, the secure partition stored in the storage medium is physically separate from the microprocessor and RAM. Ex. 1004 at 4:10-14, Fig. 1 (shown below); Ex. 1002 at ¶¶322-23.
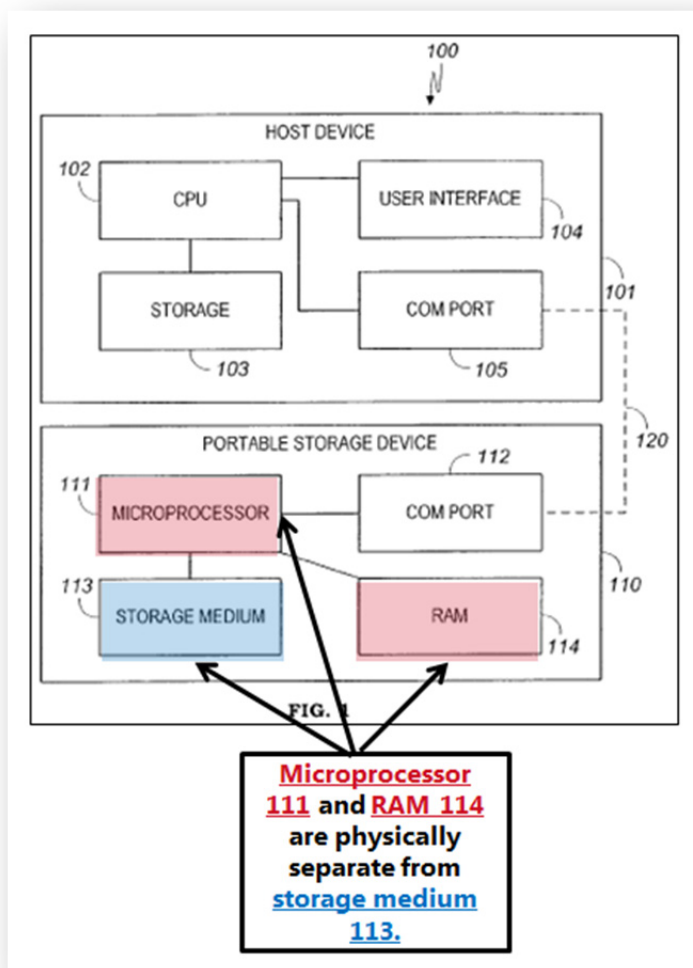
FIG. 1

Ex. 1004 at Fig. 1 (annotated).

Vogt further discloses storing the clear user area and secure user area described by *Ziv* in separate memory dies. Ex. 1002 at ¶324. As seen in Fig. 1 below, *Vogt* discloses a hidden storage that is stored separately from the main memory. Ex. 1005 at 2:14-17 ("Flash device 100 includes a hidden storage area 110, separate from the remainder of the Flash device 100. Main Flash array 105 may be accessed without a password[.]").
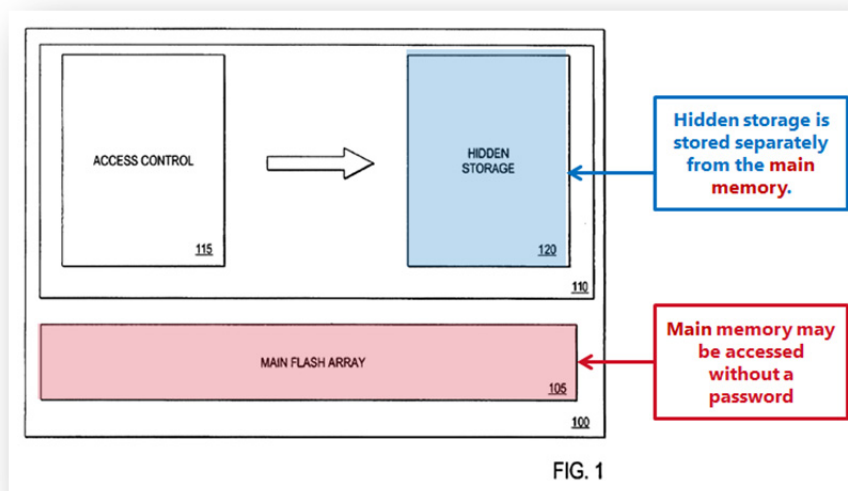
FIG. 1

Ex. 1005 at Fig. 1 (annotated). One of ordinary skill in the art would have been motivated to implement the clear user area and secure user area in *Ziv* on separate dies as disclosed by *Vogt*, because placing the secure user area on a separate die allows for additional security proofing (*e.g.*, tamper-evident seals and self-destruction mechanisms). Ex. 1002 at ¶325.

9. Dependent Claim 27

> **(i)** **The memory device of claim 17, wherein said one or more access profiles are associated with one or more partitions of said memory device.**

Ziv discloses that the password, key, and address offset are associated with the secure memory area of the memory device, which is a partition of the memory device. Ex. 1004 at 4:11-14 ("Storage medium 113 includes a clear user area 121 that contains unsecured data, a secure area 122 ... , and a system area 123."), Fig. 2 (shown below).
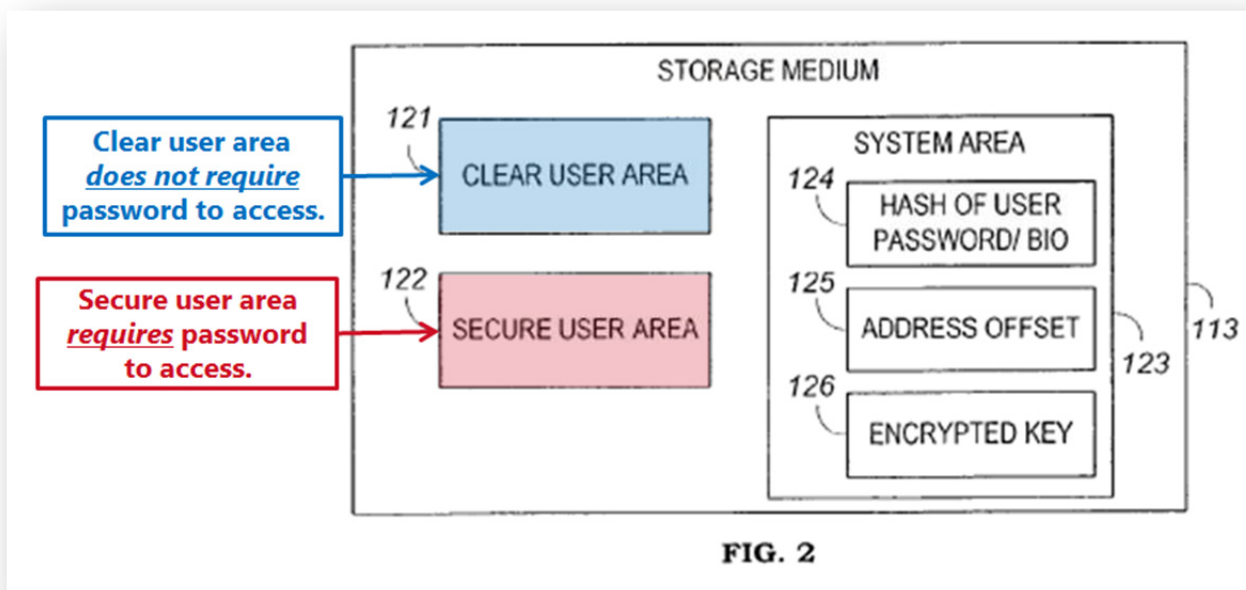
FIG. 2

Id. at Fig. 2 (annotated).

10. Dependent Claim 31

(i) **The memory device of claim 17, wherein said memory device is used to effect both mass memory and system memory implementations.**

The memory device in *Ziv* may effect mass memory as the user areas in the memory device may be used as mass memory. Ex. 1004 at 1:10-12 (describing relevance to "portable storage devices" including "portable flash memory disk"); Ex. 1002 at ¶330. Second, the memory device may effect system memory implementations as the memory device stores system-specific information in a system area of memory. Ex. 1004 at 4:14-16; Ex. 1002 at ¶331.
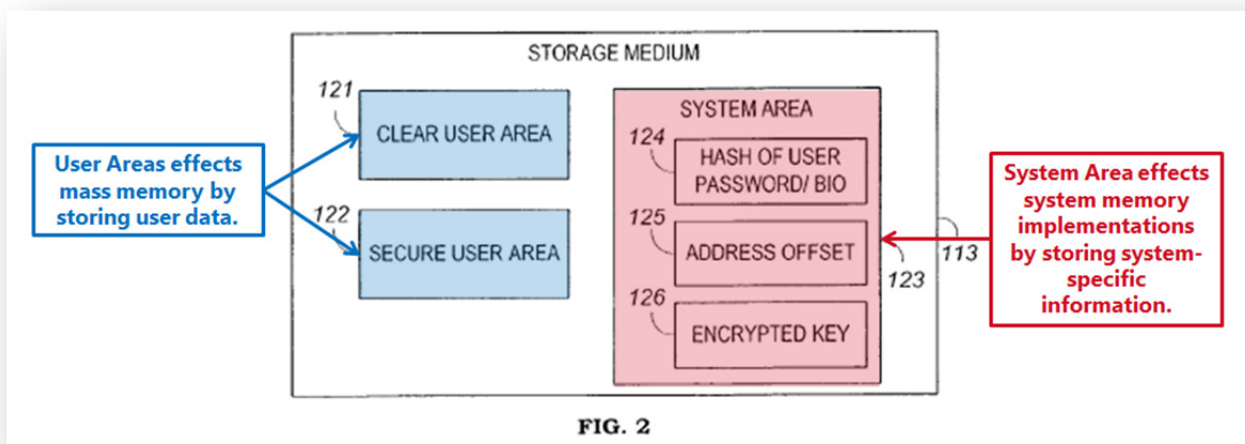
FIG. 2

Ex. 1004 at Fig. 2 (annotated).

11. Dependent Claim 32

> **(i) The memory device of claim 17, further comprising a default access profile that is used to configure said memory device upon power up.**

Ziv comprises a default access profile (*i.e.,* access to the clear user area) that is used to set up the memory device upon power up. Ex. 1004 at 6:2-4 ("By default, microprocessor 111 uses an address offset of zero, thus the host sees clear user area 121[.]"). The access to the clear user area does not require entry of a password. *Id.* at 6:4-7.

12. Dependent Claim 33

> **(i) The memory device of claim 17, wherein one or more of said predefined access profiles are updated with a new version of said access profile.**

Ziv discloses a method to update the password associated with the predefined access profile. Once the new password is entered, the new password

replaces the old password in register 124 and a new encryption key replaces the old

encryption key in register 126. Ex. 1004 at 7:17-27, Fig. 9 (shown below).
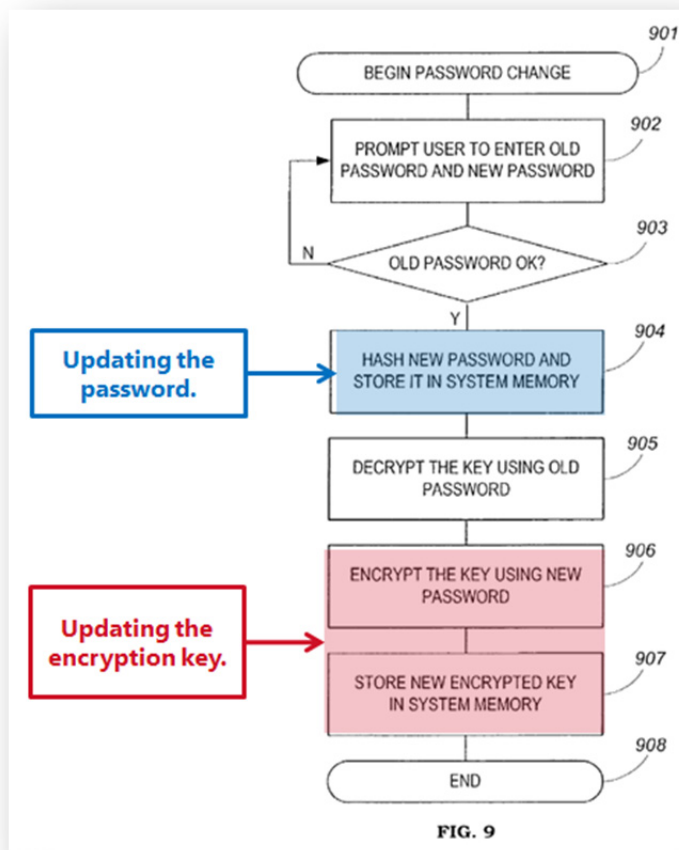
Id. at Fig. 9 (annotated).

13. Dependent Claim 34

(i) The memory device of claim 17, wherein a currently active access profile resides in a designated memory register.

Vogt discloses a designated memory register to store the active access

profile: "a bit in the valid password register 330 is set corresponding to the identity

of the password entered." Ex. 1005 at 4:17-20.

Modifying *Ziv* to also include a memory register to store an active access profile would be desirable and an obvious design choice as it would permit *Ziv* to be improved by *Vogt's* technique to store the currently-active profile. *Id.* at 4:17-20; Ex. 1002 at ¶275. Implementing *Vogt*'s designated active password register in *Ziv*'s memory device would predictably result in *Ziv*'s memory device storing the currently-active access profile in a register. Ex. 1002 at ¶275.

C.   GROUND 3: Claim 18 and 19 are unpatentable under 35 U.S.C. § 103(a) over *Ziv*, *Vogt*, and *Toombs*.

1.   Dependent Claim 18

(i)   The memory device of claim 17, wherein said one or more access profiles correspond to at least one of a random and a sequential mode of access.

Claim 17 in view of *Ziv* and *Vogt* is addressed in Ground 2 above. The read/write commands to the secure area using the hashed password, address offset, and key (*i.e.*, predefined access profile) correspond to a random or sequential mode of access. Random mode of access and sequential mode of access are the only two types of access methods for reading from and/or writing to memory. Ex. 1002 at ¶347.

Toombs teaches these two fundamental types of data transfer: sequential data transfer (sequential mode of access) and block-oriented data transfer (random mode of access). Ex. 1002 at ¶348; Ex. 1006 at 8:34-34 ("[T]wo types of data transfer commands are defined: Sequential commands, and Block-oriented

commands."). The sequential data transfer commands initiate a "continuous data stream[.]" Ex. 1006 at 8:35-37. A single block-oriented transfer initiates a single block transfer. *Id*. at 22:6-10.
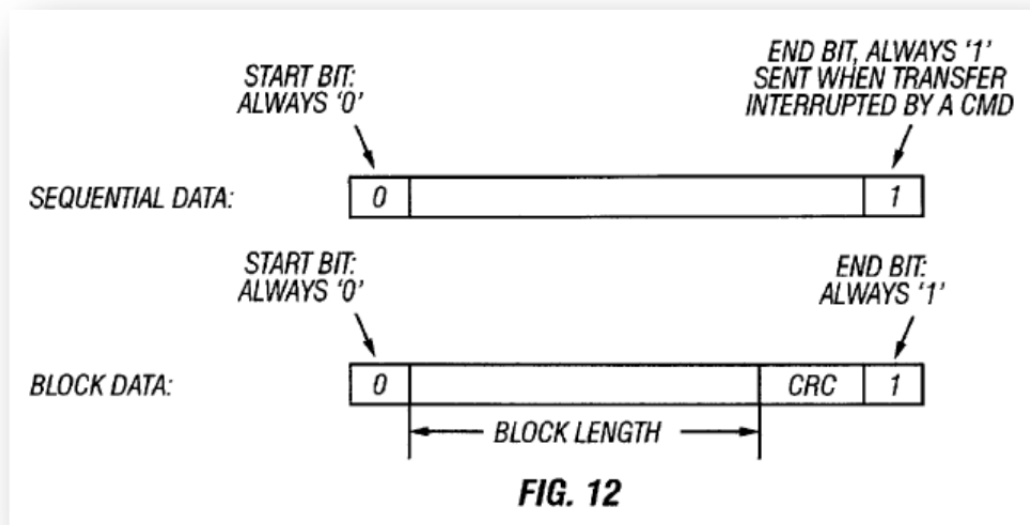
Id. at Fig. 12 (illustrating the difference between sequential data and block data).

A skilled artisan would understand that the read/write commands associated with the access profile in *Ziv* may also include the sequential read/write commands or single read/write commands disclosed by *Toombs*. Ex. 1002 at ¶¶349-51. It would have been obvious to include the sequential read and write command as taught by *Toombs* in the combined *Ziv-Vogt* memory device:

Explicit Teaching to Combine

As described in *Ziv*, the read and write operations perform under well-established standards. Ex. 1004 at 1:23-25 ("[T]he computer controls all read/write

operations under well-established standards."). Sequential and single block read operations and sequential write operations are basic transfer techniques to perform reading and writing operations. Ex. 1006 at 8:34-34. Accordingly, a skilled artisan would have looked for a basic transfer technique, like the sequential or single block read and write operations of *Toombs*, to perform the read/write operations of *Ziv*. Moreover, the sequential operations of *Toombs* were known to be advantageous as they reduce addressing overhead and improve efficiency during sequential access. *See id*. at 8:39-43 ("This [sequential data transfer] mode reduces the command overhead to an absolute minimum[.]"); Ex. 1002 at ¶340. Block-oriented commands were also advantageous as they ensured a successful data transfer. Ex. 1006 at 8:44-45.

A POSITA would have further been motivated to look to the teachings of the prior art due to the similar field, technology, and time frame of *Toombs* to *Ziv* and *Vogt*. Ex. 1002 at ¶341. All three patents center on accessing flash memory. Ex. 1004 at 4:4-9; Ex. 1005 at 2:19-20; Ex. 1006 at 1:30-33; Ex. 1002 at ¶341. Both *Ziv* and *Toombs* were commonly owned by SanDisk. Ex. 1023; Ex. 1024.

Use of Known Technique to Improve Similar Devices in the Same Way

As described in *Ziv*, "well-established standards" control the read and write operation to the secure memory area. Ex. 1004 at 1:23-25. As taught in Toombs

sequential and single-block read/write operations were known standard techniques for reading and writing operations. Ex. 1006 at 8:34-34.

It was within the level of skill in the art to apply the technique of sequential and single-block read and write commands in *Toombs* with the read and write command in the memory device described in *Ziv*. M.P.E.P. 2143(I)(B); Ex. 1002 at ¶¶342-43. Predictably, the *Ziv-Vogt* memory device would efficiently perform sequential read and write operations or single-block read and write operations to read from or write to the secure memory area. *Id*. at ¶¶343-45.

2. Dependent Claim 19

(i) **The memory device of claim 18, wherein said access profiles correspond to at least one of a read, a write, an erase, and a modify attribute operation.**

The address offset and key in *Ziv* corresponds to at least read and write operations. The address offset allows the host to properly read from and write to the secure memory area by pointing the controller to the secure memory area. *See* Ex. 1004 at 6:46-49, Fig. 10 (noting address offset is used in on-the-fly encryption/decryption). In addition, because the key is required to properly read from and write to the secure memory area, the key also corresponds to reading and writing operations. *Id*. at 7:36-46.

D. **GROUND 4: Claims 17-19, 21-23, 27, and 31-34 are unpatentable under 35 U.S.C. § 103(a) over *Sinclair* and *Toombs*.**

1. **Independent Claim 17**

(i) **A memory device, comprising:**

Sinclair discloses "the operation of re-programmable non-volatile memory systems such as semiconductor flash memory[.]" Ex. 1007 at 1:17-19, Fig. 1.
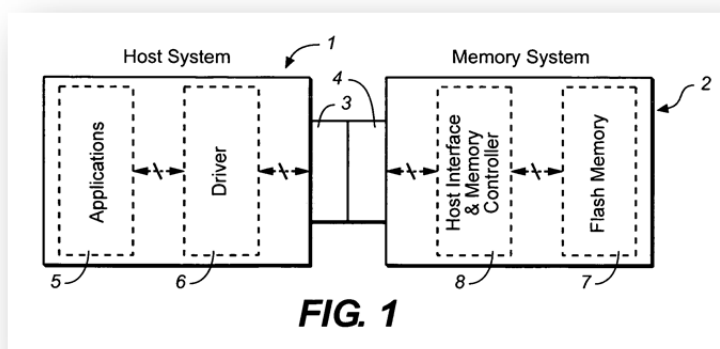
Id. at Fig. 1.

(ii) **one or more registers for storing one or more predefined access profiles associated with said memory device,**

Predefined Access Profiles

Sinclair discloses a Reclaim Normal mode that is a predefined access profile associated with the memory device and is stored in a portion of the memory (*i.e.*, register). Ex. 1007 at 2:50-57, 10:20-22; *see* Ex. 1001 at 3:56-58 ("***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device***.") (emphasis supplied). The Reclaim

Normal mode is the default mode that governs the access operations to the memory device. Ex. 1007 at 23:36-24:8. In this mode, the memory device calculates an optimal interleave ratio of reclaim operations to write commands such that a memory card will not run out of writeable memory until there is no reclaimable memory left. *Id*. at 2:50-57, Fig. 19.

Similarly, the host may also issue a "Reclaim_on" command or a "Reclaim_off" command to select other reclaim modes. *Id*. at 23:36-59. The controller performs continuous reclaim operations in Reclaim On mode and, conversely, prohibits reclaim operations in Reclaim Off mode. *Sinclair*, further, contemplates optional Maximum and Minimum Interleave modes that perform reclaim operations at a maximum or minimum interleave rate. *Id*. at 23:64-24:6. The Reclaim On, Maximum Interleave, Reclaim Normal, Minimum Interleave, and Reclaim Off mode each constitutes a predefined access profile. Ex. 1002 at ¶¶363-65. These various reclaim modes are selectable by the host based on the host's expected activity. Ex. 1007 at 23:25-29.

One or More Registers

Sinclair discloses that exemplary flash memory systems that perform the reclaim operation modes are CompactFlash and MultiMediaCard memories. *Id*. at 1:17-20, 4:28-32. Each of these standardized memory technologies includes a register that stores internal information (*e.g.,* available commands/features). Ex.

1002 at ¶¶370-71. One of ordinary skill in the art would understand that the register in a flash memory system (like CompactFlash or MultiMediaCard) would store the available reclaim modes. *Id*. at ¶¶368-71. Moreover, when the host selects a reclaim mode, that selection would be stored in a portion of the flash memory system (*i.e.,* a register). *Id*. at ¶372.

Sinclair further discloses that a reserved portion of the memory capable of storing operating firmware and data (like supported reclaim modes) (*i.e.,* a register) is used by the memory controller. Ex. 1007 at 10:20-22 ("[A]t least one metablock 167 is usually allocated as a reserved block for storing operating firmware and data used by the memory controller."); Ex. 1002 at ¶372. The available reclaim modes are part of the "operating firmware and data used by the memory controller," because they control the reclaim activity of the memory. Ex. 1007 at 10:20-22; Ex. 1002 at ¶372. *Sinclair* thus discloses a portion of the memory capable of storing information regarding the various supported reclaim modes. Ex. 1007 at 10:20-22; Ex. 1002 at ¶415.

To the extent that a register for storing access profiles is not inherently disclosed in *Sinclair*, it would have been obvious to store the selectable reclaim modes described by *Sinclair* in a memory register as described by *Toombs*. Ex. 1002 at ¶373.

Toombs discloses registers for a MultiMediaCard that stores "a variety of status and internal information" available to a host. Ex. 1006 at 9:46-48. Since a host must select an appropriate reclaim mode, one of ordinary skill would recognize the benefits of using the register in *Toombs* to store the host-selectable reclaim modes in *Sinclair* for the host to select. Ex. 1002 at ¶374. The memory device should inform the host of the supported reclaim modes in order for the host to make an informed selection of an available reclaim mode. *Id*. at ¶375.

Moreover, it would be obvious to use a register to store the host-selected reclaim mode (*i.e.,* profile) as such registers were taught in *Toombs* as a desirable and efficient way of communicating card configuration information to the host. Ex. 1002 at ¶360.

Analogous Art

Toombs and *Sinclair* are in a similar field, technology, and time frame. Ex. 1002 at ¶¶354-55. Both *Toombs* and *Sinclair* expressly teach an exemplary embodiment using MMC. Ex. 1007 at 4:28-31; Ex. 1006 at 2:9-11; Ex. 1002 at ¶354. Moreover, one of ordinary skill in the art would have especially been motivated to consider *Sinclair* and *Toombs* together because these two references are both assigned to SanDisk. Ex. 1024; Ex. 1025; Ex. 1002 at ¶355.

Combining Prior Art Elements According to Known Methods to Yield Predictable Results

Registers storing card-supported operational modes were well-known in the art. Ex. 1006 at 9:46-48. One of ordinary skill could have combined one prior art element (a register for storing card-supported modes) with another prior art element (memory devices supporting certain reclaim modes) according to a known method (combining known functionalities from two different devices into a single device) and the results would have been predictable (storing the supported reclaim modes in a register). M.P.E.P. 2143(I)(B); Ex. 1002 at ¶358. Moreover, those predictable results would have included the known advantages of *Sinclair*'s memory device, which performs reclaim operations at a frequency defined by the host-selected reclaim mode. Ex. 1007 at 23:64-24:6, 2:50-57; Ex. 1002 at ¶358.

Known Technique to a Known Device to Yield Predictable Results

Base system: *Sinclair* discloses a memory device that provides host-selectable reclaim modes. Ex. 1007 at 2:50-57 (disclosing "[a] hierarchy of possible reclaim modes" as selectable modes); Ex. 1002 at ¶367.

Known technique: As shown by *Toombs*, storing card-supported modes of operation in a register was well-known. Ex. 1006 at 9:46-48 ("[E]ach of the cards of the system comprises a group of registers for storing a variety of status and internal information"); Ex. 1002 at ¶359. For example, the Card-Specific Data

register in *Toombs* stores the supported card command classes for a MMC card.
Ex. 1006 at 10:65-67.

Predictable results and improved system: A POSITA would have been
motivated to store the supported reclaim modes on a register to take advantage of
known register-based approach for communicating available options to a host and
receiving selections from the host in order to implement *Sinclair*'s system of
allowing the host to select from available reclaim modes. Ex. 1002 at ¶359. A
register storing available reclaim modes would have been an obvious and desirable
design choice. Ex. 1002 at ¶360.

> **(iii) said predefined access profiles being effective for
> determining how access to said memory device is
> configured for at least one usage;**

The host selects a predefined access profile, like Reclaim Normal mode, to
optimally interrupt host write operations (*i.e.*, determine how access to the memory
device is configured) based on an expected host activity (*i.e.*, usage). *Id.* at 23:28-30.

The selection of Reclaim Normal mode, for example, causes the memory
controller to configure the device to optimally interleave memory access
operations (*e.g.,* write/read) with reclaim operations. *Id.* at Abstract. ("A memory
controller ... schedules the reclaim operations to be evenly distributed between
write operations until the memory is full.").

Reclaim On mode and Reclaim Off mode similarly cause access configuration changes. In Reclaim On mode, the host sits "idle" by not sending additional commands as the memory device performs continuous reclaim operations. *Id*. at 23:38-44. In Reclaim Off mode, the memory device inhibits reclaim operations and only host operations are performed. *Id.* at 23:55-56.

> **(iv)** **a controller for receiving one or more commands related to said at least one usage of said memory device**

The controller receives commands to select the appropriate reclaim mode. Ex. 1007 at 23:28-30 ("[T]he host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity"); Ex. 1002 at ¶¶378-79. The selection is related to at least one usage (*i.e.*, "expected host activity" including "idle"). Ex. 1007 at 23:27-30, 41-44.

> **(v)** **said one or more commands for activating said one or more predefined access profiles associated with said memory device,**

After receiving a reclaim mode command, such as the "Reclaim_normal" command, the controller begins reclaiming memory as specified by the selected profile. Ex. 1007 at 23:27-30. For instance, in Reclaim Normal mode, reclaiming occurs "according to an adaptive schedule." *Id*. at 24:1-3.

> **(vi)   said controller also for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.**

The memory controller calculates an optimal interleave ratio of reclaim operations to write operations in Reclaim Normal mode. Ex. 1007 at 2:56-57. Once calculated, the memory controller configures access to the memory device according to the optimal interleave ratio. *Id*. at 18:46-49. The memory device will then interleave memory access operations, like write and reclaim operations. *Id*. at 18:46-49; Ex. 1002 at ¶381. This ensures write operations to the memory device are effective as long as reclaimable memory remains. Ex. 1007 at 18:17-26.

Similarly, the memory controller configures access to the device in Reclaim On mode and Reclaim Off mode. In Reclaim On mode, the host is "idle" while the memory device performs continuous reclaim operations. *Id*. at 23:38-44. In Reclaim Off mode, reclaim operations are inhibited and only host access operations are performed. *Id.* at 23:55-56.

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2. Dependent Claim 18

(i) **The memory device of claim 17, wherein said one or more access profiles correspond to at least one of a random and a sequential mode of access.**

During the Reclaim Normal mode, reclaim operations are interleaved with write operations. Ex. 1007 at 17:58-60. Moreover, these write operations can either be a sequential or random mode of access.

One method of reclaim operations is data compaction, which rearranges blocks into *a sequential format*. *Id*. at 12:28-30; Ex. 1002 at ¶¶386-87. *Sinclair* teaches the benefit of sequential access: "one advantage of sequentially storing data is that it may not necessary to maintain an index of the locations of different sectors, thus reducing the overhead associated with maintaining such an index." Ex. 1007 at 12:51-54. Accordingly, the reclaim operation associated with the Reclaim Normal mode corresponds to a sequential mode of access as the controller can now access a sequentially-arranged set of data. Ex. 1002. at ¶¶387-88.

3. Dependent Claim 19

(i) **The memory device of claim 18, wherein said access profiles correspond to at least one of a read, a write, an erase, and a modify attribute operation.**

Sinclair teaches that the Reclaim Normal mode corresponds to interleaving reclaim operations *with host data write operations*. Ex. 1007 at 24:1-3 (emphasis supplied).

4.   Dependent Claim 21

>   **(i)   The memory device of claim 17, wherein said one or more access profiles are adapted to produce an optimized performance associated with said memory device.**

5.   Dependent Claim 22

>   **(i)   The memory device of claim 21, wherein said performance is optimized in accordance with at least one of: data throughput, lifetime, and power consumption associated with said memory device.**

Reclaim Normal mode is adapted to produce an optimized performance associated with the memory device. First, the reclaim operation in the Reclaim Normal mode "allows programming of host data to continue at a constant rate until the memory is full." Ex. 1007 at 22:56-61. Without a Reclaim Normal mode, data programming is impeded when no writeable memory remains (*Id*. at 17:23-25), whereas Reclaim Normal ensures higher reliability such that the memory device does not utilize all writeable memory prematurely. *Id*. at 22:56-61. This ensures an optimized performance in accordance with at least data throughput. Ex. 1002 at ¶392. *Sinclair* further teaches changing the interleave ratio to optimize the data programming speed if conditions in the memory change. Ex. 1007 at 18:17-26. In addition, the controller in Reclaim Off mode only performs host operations, thereby "provid[ing] maximum host data write performance." *Id*. at 23:55-58.

Finally, the reclaim modes support "wear leveling" of the device (*id.* at 16:5-11), which a person skilled in the art would understand improves device lifetime through wear leveling technology. Ex. 1002 at ¶394.

6.   Dependent Claim 23

>   **(i)   The memory device of claim 17, wherein said one or more commands comprise a metadata portion for designating a preferred access profile corresponding to said command.**

The "Reclaim_normal" command comprises metadata information that designates a preferred access profile. Ex. 1007 at 23:47-48 ("A 'Reclaim_normal' command allows the memory to operate in a default reclaim mode."); Ex. 1002 at ¶397. The metadata portion, in particular, will identify whether the reclaim operations are performed on an adaptive schedule or selected by the memory controller. Ex. 1007 at 23:48-50 ("[Operating in a default reclaim mode] may mean reclaiming according to an adaptive schedule or may mean giving control of reclaim mode selection to the memory controller that then chooses the reclaim mode based on some predetermined criteria."); Ex. 1002 at ¶¶397-98.

7.   Dependent Claim 27

>   **(i)   The memory device of claim 17, wherein said one or more access profiles are associated with one or more partitions of said memory device.**

The reclaim modes (*i.e.*, predefined access profiles) are associated with at least one or more partitions of the memory device. Ex. 1002 at ¶¶400-01. A

POSITA would understand that *Sinclair*'s memory device must contain at least one or more partitions. Ex. 1002 at ¶400; Ex. 1007 at 1:49-56, 2:5-23, 5:35-54, 9:22-31. Because each reclaim mode (*e.g.*, Reclaim Normal mode) causes the memory device to conduct certain access operations (*i.e.*, reclaim and/or write operations) in a particular manner depending on the mode, each reclaim mode is associated with the memory device. Ex. 1002 at ¶401. *See, e.g.*, Ex. 1007 at 23:36-59. Each reclaim mode, therefore, is also associated with at least the one or more partitions of the memory device (*i.e.*, the partition(s) comprising the memory device). Ex. 1002 at ¶401.

8. Dependent Claim 31

(i)   The memory device of claim 17, wherein said memory device is used to effect both mass memory and system memory implementations.

The memory device in the *Sinclair-Toombs* combination may effect both mass memory and system memory implementations. First, the memory device in *Sinclair-Toombs* combination may effect mass memory as "[t]he memory system controller is programmed to store data files within the blocks and metablocks of a memory array." Ex. 1007 at 10:13-14; Ex. 1002 at ¶403. Second, the memory device may effect system memory implementations as "another metablock 169, or multiple metablocks, may be allocated for storage of host operating software, the host FAT table and the like." Ex. 1006 at 10:22-24; Ex. 1002 at ¶404.

9. Dependent Claim 32

> **(i)** **The memory device of claim 17, further comprising a default access profile that is used to configure said memory device upon power up.**

Sinclair discloses a default access profile, like the Reclaim Normal mode, that configures the memory device upon power up. Ex. 1007 at 23:47-48; Ex. 1002 at ¶406.

10. Dependent Claim 33

> **(i)** **The memory device of claim 17, wherein one or more of said predefined access profiles are updated with a new version of said access profile.**

Sinclair discloses updating an interleave ratio associated with the Reclaim Normal mode based on commands received from the host. For example, the controller computes a new interleave ratio after a host submits a command to erase memory. Ex. 1007 at 18:2-26. This creates a new version of the Reclaim Normal mode, now adapted to the updated memory configuration. *Id*. at 3:3-6 ("[T]he interleave ratio is **updated** as appropriate so that the ratio is adaptive to changing circumstances.") (emphasis supplied).

11. Dependent Claim 34

> **(i)** **The memory device of claim 17, wherein a currently active access profile resides in a designated memory register.**

It would have been obvious to store the currently active access profile described by *Sinclair* in a memory register as described by *Toombs*. Ex. 1002 at

¶410. In order to create a new interleave ratio based on a host triggering event, the memory device must know that currently active access profile is the Reclaim Normal mode. *Id*. Otherwise, the memory device would attempt to change the interleave ratio even if the reclaim operations were prohibited. *Id*. *Toombs* further emphasizes that registers for an MMC card store "a variety of status and internal information." Ex. 1006 at 9:46-48. Accordingly, it would be an obvious design choice for the memory card to store the current profile in a register in the same way that *Toombs* stores other status information relating to the card functionality. Ex. 1002 at ¶411.

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X.   CONCLUSION

SanDisk respectfully requests that *inter partes* review of the '180 Patent be

instituted and that Claims 17-27 and 31-34 be cancelled as unpatentable under 35

U.S.C. § 318(b).

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition, exclusive of the exempted portions as provided in 37 C.F.R. § 42.24(a), contains no more than 13,734 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24(a). The word count was calculated by starting with Microsoft Word's total document word count and subtracting the words for the Table of Contents, the Exhibit List, the Mandatory Notices, the Certificate of Compliance, and the Certificate of Service

May 3, 2017

/s/Eliot D. Williams/
Eliot D. Williams

CERTIFICATE OF SERVICE ON PATENT OWNER UNDER 37 C.F.R. § 42.105

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on the 3rd day of May, 2017, a complete and entire copy of this Petition for *Inter Partes* Review under 35 U.S.C. § 311 and 37 C.F.R. § 42.104, and all supporting exhibits were provided via Federal Express, postage prepaid, to the Patent Owner and its known representatives by serving the correspondence address of record for the '180 Patent holder and the patent holder's counsel:

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The undersigned further certifies that a courtesy copy of the complete and entire Petition was provided by electronic service to counsel retained by Patent Owner in the Related Matters identified herein:

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