

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY
SOLUTIONS INC.,

Petitioners,

v.

NETLIST, INC.

Patent Owner

Patent No. 8,671,243

Issued: March 11, 2014

Filed: May 29, 2013

Inventors: Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, Jayesh Bhakta

Title: Isolation Switching For Backup Memory

Inter Partes Review No. IPR2017-00587

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,671,243
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123**

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Attachment A. Proof of Service of the Petition

Attachment B. List of Evidence and Exhibits Relied Upon in Petition

I. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Certification the '243 Patent May Be Contested by Petitioners

Petitioners certify they are not barred or estopped from requesting *inter partes* review of U.S. Patent No. 8,671,243 (“the '243 Patent”) (Ex. 1001). No Petitioner, nor any party in privity with a Petitioner, has filed a civil action challenging the validity of any claim of the '243 Patent. The '243 Patent has not been the subject of a prior *inter partes* review by any Petitioner or a privy of a Petitioner.

Petitioners also certify this petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of a patent – no complaint alleging infringement of the '243 Patent has been served on any Petitioner. Petitioners therefore certify this patent is available for *inter partes* review.

B. Fee for Inter Partes Review (§ 42.15(a))

The Director is authorized to charge the fee specified by 37 CFR § 42.15(a) to Deposit Account No. 50-1597.

C. Mandatory Notices (37 CFR § 42.8(b))

The real parties of interest of this petition are the Petitioners: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. The '243 Patent has not been involved any legal proceedings.

Petition for *Inter Partes* Review of U.S. Patent No. 8,671,243

Lead Counsel is Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492. Back-up Lead Counsel is Wonjoo Suh (Reg. No. 64,124), Sidley-SKH-IPR@sidley.com, (202) 736-8831.

Service on Petitioner may be made by e-mail (Sidley-SKH-IPR@sidley.com), mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

D. Proof of Service (§§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

II. Identification of Claims Being Challenged (§ 42.104(b))

Petitioners propose several grounds for trial as set forth below, none of which is redundant. Each ground is based primarily on U.S. Patent No. 6,693,840 to Shimada *et al.* (“Shimada”) (Ex. 1005). However, Petitioners also address several arguments that Patent Owner may raise in response by proposing grounds that more closely satisfy the claim limitations to which such arguments would be directed. Such additional grounds are not redundant because they are “rational, narrowly targeted, and not burdensome considering only five claims with very similar limitations are at issue.” IPR2015-01912, Paper 10 at 17-18 (Mar. 22, 2016). Petitioners therefore respectfully request that trial be instituted on all

grounds and arguments advanced herein. Specifically, this Petition seeks a finding that claims 1-30 of the '243 Patent are unpatentable as follows:

- (i) Claims 1-3, 5-15, 17-30 of the '243 Patent are unpatentable as anticipated under 35 U.S.C. § 102 by Shimada (Ex. 1005);
- (ii) Claims 4 and 16 of the '243 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Shimada in view of U.S. Patent No. 7,486,104 to Oh *et al.* ("Oh"; Ex. 1012);
- (iii) Claims 1, 3, 13, 15, and 25 of the '243 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Shimada in view of U.S. Patent Publication No. 2007/0136523 to Bonella *et al.* ("Bonella"; Ex. 1009);
- (iv) Claims 6 and 18 of the '243 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Shimada;
- (v) Claims 9, 21, and 28 of the '243 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Shimada in view of U.S. Patent No. 4,658,204 to Goodwin ("Goodwin"; Ex. 1015);
- (vi) Claims 10, 22, and 29 of the '243 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Shimada in view of U.S. Patent No. 6,721,212 to Sasaki ("Sasaki"; Ex. 1017);
- (vii) Claims 11, 12, 23, 24, and 30 of the '243 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Shimada in view of U.S. Patent Publication No. 2003/0028733 to Tsunoda *et al.* ("Tsunoda"; Ex. 1019).

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ III-V, below.

The evidence relied upon in this petition is listed in **Attachment B**.

III. Relevant Information Concerning the Contested Patent

A. Effective Filing Date of the '243 Patent

The '243 Patent resulted from U.S. Patent Application Serial No. 13/905,048, filed May 29, 2013, but claims priority to several earlier applications, including U.S. Provisional Application No. 60/941,586, filed on June 1, 2007. Ex. 1001 at 1. Because the prior art relied upon in this petition was either filed or published well before the June 1, 2007, for the purposes of the analysis here Petitioners will assume a June 1, 2007 effective date.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the '243 Patent in the 2007 time frame would have been a person with a Bachelor's degree in materials science, electrical engineering, computer engineering, computer science, or in a related field and at least one year of experience with the design or development of semiconductor non-volatile memory circuitry or systems. Ex. 1003 ¶¶ 49-50.

C. The '243 Patent

1. Technical Overview

The '243 Patent discloses a memory system having a "volatile memory subsystem" and a "non-volatile memory subsystem." Ex. 1001 at Abstract; Ex.

1003 ¶ 51. The memory system can switch between two modes of operation through a “circuit.” Ex. 1001 at Abstract, 7:49-50; Ex. 1003 ¶ 51. The ’243 Patent explains that the “circuit” includes switches 170 and 172 (shown in FIG. 4A) that can switch the memory system between the first and second modes. Ex. 1001 at 6:38-49, FIG. 4A; Ex. 1003 ¶ 51.

In the first mode, the “circuit” couples the “volatile memory subsystem” to the host system to allow data to be communicated between the “volatile memory subsystem” and the host system, and at the same time isolates the “volatile memory subsystem” from the “non-volatile memory subsystem,” which is connected to a “controller.” Ex. 1001 at Abstract, 7:49-62; Ex. 1003 ¶ 52.

In the second mode, the “circuit” allows data to be communicated between the “volatile memory subsystem” and the “nonvolatile memory subsystem” by coupling the “non-volatile memory subsystem” (which is connected to a “controller”) to the “volatile memory subsystem,” and at the same time isolates the “volatile memory subsystem” from the host system. Ex. 1001 at Abstract, 7:49-62; Ex. 1003 ¶ 53.

The hybrid memory system in the ’243 Patent functions as a volatile memory system under normal operation (*i.e.*, the first mode), while providing back up functionalities using a non-volatile memory (*i.e.*, the second mode) in case there

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is a power failure, power reduction, request by the host system. Ex. 1001 at 3:24-27, 6:23-34, 7:49-62; Ex. 1003 ¶ 54.

The alleged invention of the '243 Patent is to switch between the two modes of operation so that the volatile memory within the hybrid memory system is not adversely affected by the non-volatile memory (or by the controller) when the volatile memory is interacting with the host system. Ex. 1001 at 3:32-36, 8:17-30; Ex. 1003 ¶ 55. According to the '243 Patent, this configuration protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure. Ex. 1001 at 3:41-45; Ex. 1003 ¶ 55.

2. Prosecution History

The application underlying the '243 Patent was filed on May 29, 2013, as a continuation in a patent family including several prior applications claiming priority back to June 1, 2007. Ex. 1001 at 1; Ex. 1003 ¶ 56.

On August 1, 2013, the United States Patent and Trademark Office (USPTO) rejected claims 1-8, 12-20 and 24-27 as being unpatentable over U.S. Patent No. 6,721,860 to Klein in view of U.S. Patent No. 6,816,982 to Ravid. Ex. 1002 at 92-104 (Non-Final Office Action, Aug. 1, 2013); Ex. 1003 ¶ 57.

The applicants filed a Request for Reconsideration on November 1, 2013. Ex. 1002 at 114-125 (Request for Reconsideration, Nov. 1, 2013); Ex. 1003 ¶¶ 58-59.

The Examiner allowed the claims on December 19, 2013. Ex. 1002 at 143 (Notice of Allowance, Dec. 19, 2013). The '243 Patent issued on March 11, 2014. Ex. 1002 at 181 (Issue Notification, Feb. 19, 2014); Ex. 1003 ¶ 60.

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 CFR § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

1. “host system”

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “host system” includes a “system external to the memory system that communicates with the memory system.” Ex. 1003 ¶ 66.

The '243 Patent does not define the term “host system,” but states that it is in electrical communication with the “memory system.” Ex. 1001 at 4:56-57; Ex.

1003 ¶ 67. The '243 Patent does mention, generally, that examples of “host systems” include “blade servers, 1U servers, personal computers (PCs),” but fails to define which parts of the “servers” or “personal computers” are within the “host system,” as claimed. *See* Ex. 1001 at 4:60-63; Ex. 1003 ¶ 67.

The '243 Patent describes operations of a “host system” that communicates electrically and interacts with a memory system. Ex. 1001 at 4:56-57, 4:65-67, 5:2-5, 6:35-67; Ex. 1003 ¶ 68. As such, the “host system” communication can provide guidance or direction for the memory system operations. *Id.*

Certainly, the “memory system” of the “servers” or “personal computers” cannot be part of the “host system,” as claimed, because the claims recited the “memory system” and “host system” as separate elements. Ex. 1003 ¶ 69.

Accordingly, the broadest reasonable interpretation of “host system” includes a “system external to the memory system that communicates with the memory system.” Ex. 1001 at 4:56-57, 4:65-67, 5:2-5, 6:35-67; Ex. 1003 ¶ 69.

2. **“in a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system”**

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “in a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system” is that the

circuit can be selected to operate in a first mode of operation, in which the circuit does not allow communication between the controller and the volatile memory subsystem while allowing communication between the volatile memory subsystem and the host system. *See, e.g.*, Ex. 1001 at 3:36-41, 7:49-62, 9:40-45; Ex. 1002 at 122-23 (Request for Reconsideration, Nov. 1, 2013 at 9-10); Ex. 1003 ¶ 70.

In particular, to secure allowance of the claims, the applicants argued:

1. In the 1st mode,
 - A. The controller is isolated from the volatile memory subsystem, AND
 - B. The host is coupled to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the host system.”
2. In the 2nd mode,
 - A. The controller is coupled to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, AND
 - B. The host is isolated from the volatile memory subsystem.

Ex. 1002 at 122 (Request for Reconsideration, Nov. 1, 2013); Ex. 1003 ¶ 71.

The applicants then argued that “the AND condition must be addressed, and the occurrence of both features of the first mode, and both features of the second mode, must be shown.” Ex. 1002 at 123 (Request for Reconsideration, Nov. 1, 2013); Ex. 1003 ¶ 72.

This is supported by the specification also. In particular, the '243 Patent describes this “first mode of operation” as a “first state,” which is “when the volatile memory is interacting with the host system.” *See, e.g.*, Ex. 1001 at 3:36-41, 7:49-62, 9:40-45; Ex. 1003 ¶ 73.

In particular, the '243 Patent explains that the switches 170 and 172 (shown in FIG. 4A) can be “selectively switched” to switch the memory system 10 between the first and second modes. Ex. 1001 at 6:38-49, FIG. 4A; Ex. 1003 ¶ 74.

Thus, the '243 Patent discloses two modes – a first in which the volatile memory is operatively coupled to the host system but not to the controller/non-volatile memory pair, and a second in which the volatile memory is operatively coupled to the controller/non-volatile memory pair but not to the host system. Ex. 1003 ¶ 75. Significantly, there is no mode disclosed in the '243 Patent during which the system can either choose to isolate or couple the volatile memory to the controller/non-volatile memory pair. In one mode they are always isolated and in the other they are always not. *Id.* Because that is the only disclosure in the '243 Patent that could even conceivably support this claim language, the broadest reasonable interpretation, consistent with the specification, of “*in a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system*” is that the circuit can be selected to operate in a first

mode of operation, in which the circuit does not allow communication between the controller and the volatile memory subsystem while allowing communication between the volatile memory subsystem and the host system. *See, e.g.*, Ex. 1001 at 3:36-41, 7:49-62, 9:40-45; Ex. 1002 at 122-23 (Request for Reconsideration, Nov. 1, 2013); Ex. 1003 ¶ 75.

3. **“in a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem . . . , and the circuit is operable to selectively isolate the volatile memory subsystem from the host system”**

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “in a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem . . . , and the circuit is operable to selectively isolate the volatile memory subsystem from the host system[.]” is that the circuit can be selected to operate in a second mode of operation, in which the circuit does not allow communication between the volatile memory subsystem and the host system while allowing communication between the volatile memory subsystem and the controller, for the reasons set forth above. *See, e.g.*, Ex. 1001 at 3:36-41, 7:49-62, 9:40-45; Ex. 1002 at 122-23; Ex. 1003 ¶ 76.

4. **“one or more switches”**

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “*one or more switches*” is an element that allows switching between two or more states. *See, e.g.*, Ex 1021 at p. 505 (Microsoft Computer Dictionary, Fifth Edition (2002)) (“switch *n.* 1. A circuit element that has two states: on and off. 2. A control device that allows the user to choose one of two or more possible states.”); Ex. 1003 ¶ 77.

5. “signal level translation”

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “signal level translation” includes “changing voltage levels.” Ex. 1003 ¶ 78.

The ’243 Patent explains that “[t]he logic element 70 can provide signal level translation between the volatile memory elements 32 (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 42 (e.g., 3V TTL for NAND flash memory elements).” Ex. 1001 at 7:39-42; Ex. 1003 ¶ 79.

Accordingly, one skilled in the art would understand that the broadest reasonable construction of a “signal level translation” includes “changing voltage levels.” *Id.*

IV. Overview of the Prior Art

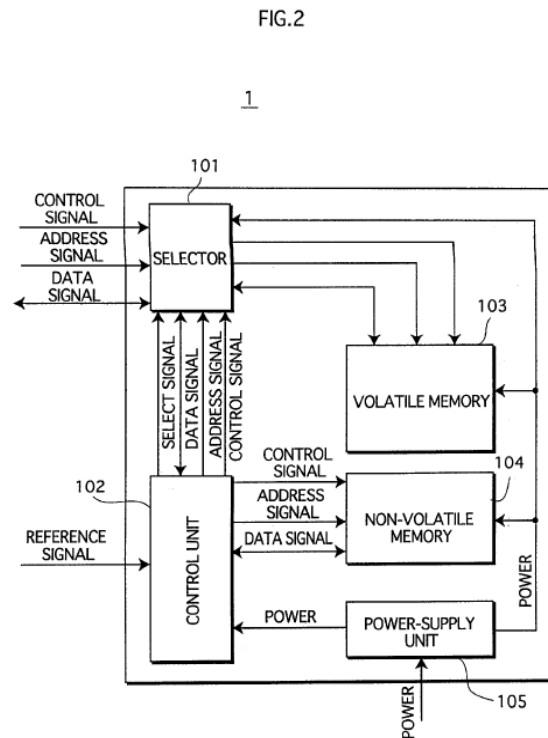
A. U.S. Patent No. 6,693,840 to Shimada (Ex. 1005)

United States Patent No. 6,693,840 to Shimada *et al.* (“Shimada”; Ex. 1005) was filed on October 15, 2002 and issued on February 17, 2004. Ex. 1005 at 1; Ex.

1003 ¶ 80. Shimada is prior art to the '243 Patent under 35 U.S.C. §§ 102 (a), (b) and (e).

Shimada discloses a hybrid memory system having a “volatile memory” and a “non-volatile memory.” Ex. 1005 at Abstract, 3:45-53, FIG. 2; Ex. 1003 ¶ 81.

The memory system can switch between two modes of operation through a “selector.” Ex. 1005 at 4:1-34, FIG. 2 (reproduced below); Ex. 1003 ¶ 81



In particular, Shimada explains that “[t]he selector 101 receives a select signal having been sent from the control unit 102 as in the above, and switches between two modes in which access to the volatile memory is allowed differently. That is, when receiving a select signal (H), the selector 101 allows access from outside the semiconductor memory device 1 to the volatile memory 103; and when

receiving a select signal (L), the selector 101 allows the control unit 102 to access the volatile memory 103.” Ex. 1005 at 4:20-27; Ex. 1003 ¶ 82.

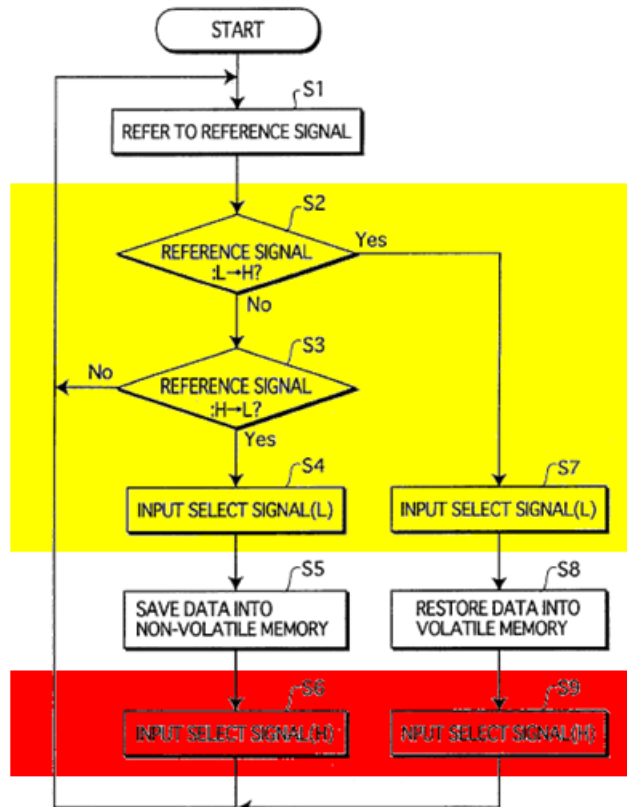
Shimada explains that in the first mode (*i.e.*, when the “selector 101” receives a select signal (H)), the “selector 101” is operable to selectively couple the “volatile memory 103” to the host system to allow data to be communicated between the “volatile memory 103” and the host system. Ex. 1005 at 4:6-9, 4:23-25, 4:28-33; Ex. 1003 ¶ 83. In the first mode (*i.e.*, when the “volatile memory” is coupled to the host system), the “selector 101” shuts out any access of the host system to the remaining portions of the “semiconductor memory device.” *See, e.g.*, Ex. 1005 at 5:30-34, 9:30-39; Ex. 1003 ¶ 83. Shimada explains that the “semiconductor memory device” includes the “control unit 102” and the “non-volatile memory 104.” *See, e.g.*, Ex. 1005 at 3:47-50; Ex. 1003 ¶ 83. Accordingly, in the first mode, the “selector 101” shuts out access of the host system to the “control unit 102” and the “non-volatile memory 104.” Ex. 1005 at 3:47-50, 9:30-39; Ex. 1003 ¶ 83.

Shimada explains that in the second mode (*i.e.*, when the “selector 101” receives a select signal (L)), the “selector 101” is operable to couple the “control unit 102” to the “volatile memory 103” to allow data to be communicated between the “volatile memory 103” and the “non-volatile memory 104” using the “control unit 102.” Ex. 1005 at 4:26-27, 3:55-62, 4:34-41; Ex. 1003 ¶ 84. In the second

mode (*i.e.*, when the “selector 101” receives a select signal (L)), the “selector 101” is operable to selectively isolate the “volatile memory 103” from the host system. *See, e.g.*, Ex. 1005 at 3:64-4:1; Ex. 1003 ¶ 84.

Below is an annotated version of FIG. 3 showing how the “first mode of operation” can be triggered (in red) and how the “second mode of operation” can be triggered (in yellow). Ex. 1005, FIG. 3 (reproduced below with annotations); Ex. 1003 ¶ 85.

FIG.3



As shown in FIG. 3, Shimada shows two ways in which the second mode of operation can be triggered. Ex. 1005 at FIG. 3; Ex. 1003 ¶ 86. First, the second mode of operation can be a mode in which data is copied from the non-volatile memory 104 to the volatile memory 103. Ex. 1003 ¶ 86. This mode is triggered when the “selector 101” receives a select signal (L) after the reference signal has changed from L to H. Ex. 1005 at FIG. 3, 3:64-4:6; Ex. 1003 ¶ 86. Second, the second mode of operation can also be a mode in which data is copied from the volatile memory 103 to the non-volatile memory 104. This mode is triggered when the “selector 101” receives a select signal (L) after the reference signal has changed from H to L. Ex. 1003 ¶ 86.

The hybrid memory system in Shimada functions as a volatile memory system under normal operation (*i.e.*, the first mode), while providing back up functionalities using a non-volatile memory (*i.e.*, the second mode) in case there is a power failure. Ex. 1005 at 5:30-34, 2:28-39; Ex. 1003 ¶ 87.

Similar to the '243 Patent, the invention of Shimada is to switch between the two modes of operation so that the volatile memory within the hybrid memory system is not adversely affected by the non-volatile memory when the volatile memory is interacting with the host system. Ex. 1005 at 9:30-39; Ex. 1003 ¶ 88.

B. U.S. Patent Publication No. 2007/0136523 to Bonella (Ex. 1009)

U.S. Patent Publication No. 2007/0136523 to Bonella *et al.* (“Bonella”) was filed on December 8, 2006 and published on June 14, 2007. Ex. 1009 at 1; Ex. 1003 ¶ 89. Bonella is prior art to the ’243 Patent under 35 U.S.C. § 102 (e).

C. U.S. Patent No. 7,486,104 to Oh (Ex. 1012)

U.S. Patent No. 7,486,104 to Oh *et al.* (“Oh”) was filed on June 2, 2006 and issued on February 3, 2009. Ex. 1012 at 1; Ex. 1003 ¶ 90. Oh is prior art to the ’243 Patent under 35 U.S.C. § 102 (e).

D. U.S. Patent No. 4,658,204 to Goodwin (Ex. 1015)

U.S. Patent No. 4,658,204 to Goodwin (“Goodwin”) was filed on February 7, 1986 and issued on April 14, 1987. Ex. 1015 at 1; Ex. 1003 ¶ 91. Goodwin is prior art to the ’243 Patent under 35 U.S.C. §§ 102 (a), (b) and (e).

E. U.S. Patent No. 6,721,212 to Sasaki (Ex. 1017)

U.S. Patent No. 6,721,212 to Sasaki (“Sasaki”) was filed on January 2, 2003 and issued on April 13, 2004. Ex. 1017 at 1; Ex. 1003 ¶ 92. Sasaki is prior art to the ’243 Patent under 35 U.S.C. §§ 102 (a), (b) and (e).

F. U.S. Patent Publication No. 2003/0028733 to Tsunoda (Ex. 1019)

U.S. Patent Publication No. 2003/0028733 to Tsunoda *et al.* (“Tsunoda”) was filed on June 13, 2002 and published on February 6, 2003. Ex. 1019 at 1; Ex.

1003 ¶ 93. Tsunoda is prior art to the '243 Patent under 35 U.S.C. §§ 102 (a), (b) and (e).

V. Precise Reasons for Relief Requested

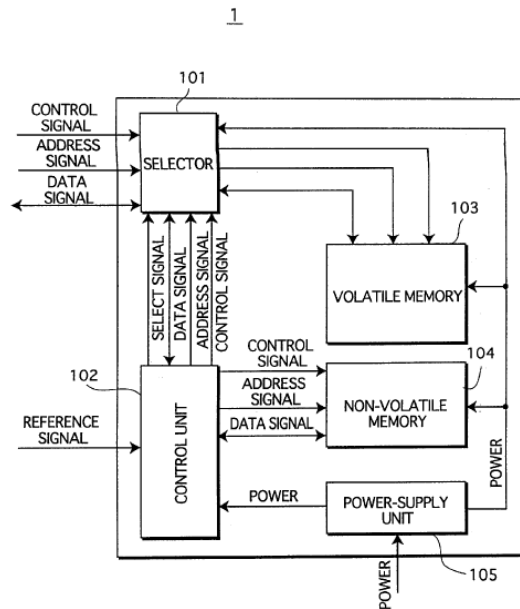
A. Claims 1-3, 5-15, 17-30 are Anticipated By Shimada

1. Claim 1

a) Preamble

Shimada discloses a “semiconductor memory device 1 include[ing] a control unit 102, a volatile memory 103, a non-volatile memory 104, a selector 101, and a power supply unit 105.” Ex. 1005 at 3:47-50, FIG. 2 (reproduced below); Ex. 1003 ¶¶ 94-95. As shown below, the “semiconductor memory device” in FIG. 2 of Shimada is a memory system because it includes a number of memory subsystems (*e.g.*, the “volatile memory 103” and the “non-volatile memory 104”). *Id.*; *see also id.* at 5:43-47, 5:50-53, 6:22-26, 6:30-33, FIGS. 4-5; Ex. 1003 ¶ 96.

FIG.2

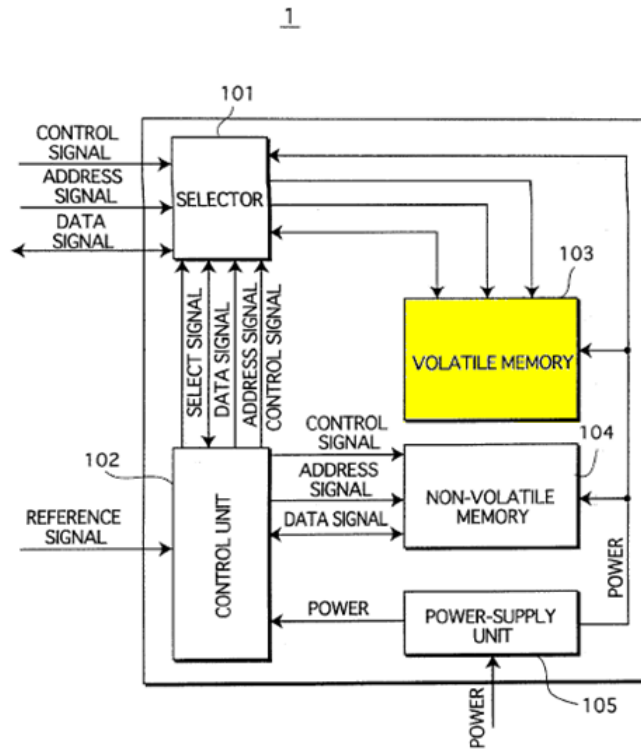


Thus, Shimada discloses “[a] memory system.” Ex. 1001 at 20:30 (emphasis added); Ex. 1003 ¶¶ 94-97.

b) Volatile Memory Sub-System

Shimada discloses a “volatile memory 103” subsystem within the “semiconductor memory device 1.” Ex. 1005 at 3:47-50, FIG. 2 (annotated, below); *see also id.* at 5:43-47, 5:50-53, 6:22-26, 6:30-33, FIGS. 4-5; Ex. 1003 ¶¶ 98-100.

FIG.2

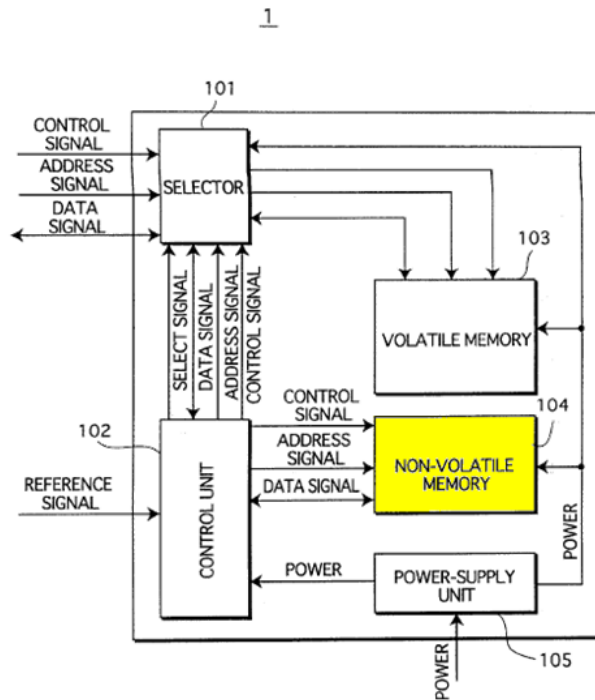


Thus, Shimada discloses “a volatile memory subsystem.” Ex. 1001 at 20:31 (emphasis added); Ex. 1003 ¶¶ 98-101.

c) Non-Volatile Memory Sub-System

Shimada discloses a “non-volatile memory 104” subsystem within the “semiconductor memory device 1.” Ex. 1005 at 3:47-50, FIG. 2 (annotated, below); *see also id.* Ex. 1005 at 5:43-47, 5:50-53, 6:22-26, 6:30-33, FIGS. 4-5; Ex. 1003 ¶¶ 102-104.

FIG.2



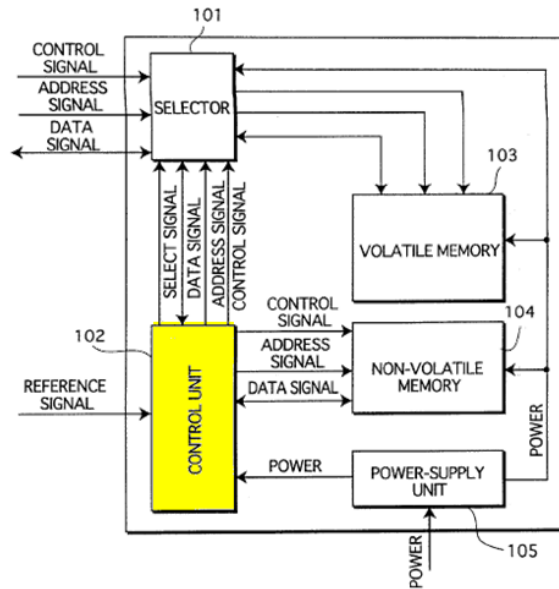
Thus, Shimada discloses “a non-volatile memory subsystem.” Ex. 1001 at 20:32 (emphasis added); Ex. 1003 ¶¶ 102-105.

d) Controller

Shimada discloses a “control unit 102” within the “semiconductor memory device 1.” Ex. 1005 at 3:47-50, FIG. 2; Ex. 1003 ¶¶ 106-107. The “control unit 102 controls operations of the semiconductor memory device 1” Ex. 1005 at 3:54-55; Ex. 1003 ¶ 107, and is coupled to the “non-volatile memory 104” subsystem through address, control, and data signal lines. Ex. 1005 at 3:55-59, 4:39-41, FIG. 2 (annotated below); Ex. 1003 ¶ 107; *see also* Ex. 1005 at 5:43-47, 5:50-53, 6:22-26, 6:30-33, FIGS. 4-5; Ex. 1003 ¶ 108.

FIG.2

1

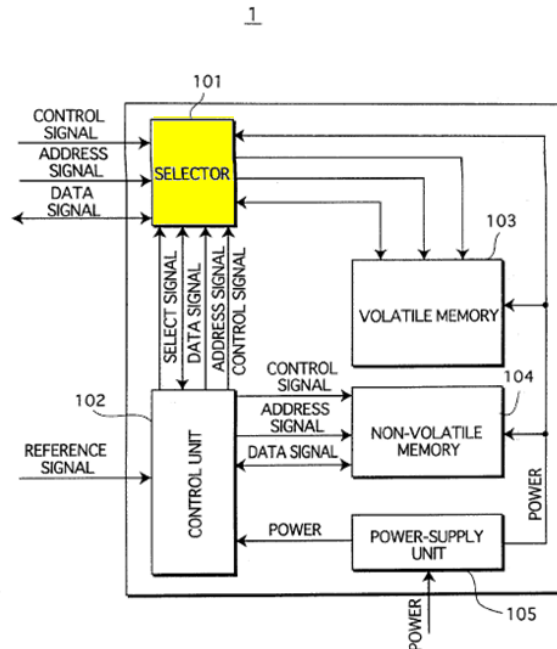


Thus, Shimada discloses “a controller coupled to the non-volatile memory subsystem.” Ex. 1001 at 20:33-34 (emphasis added); Ex. 1003 ¶¶ 106-109.

e) Circuit

Shimada discloses a “selector 101” within the “semiconductor memory device 1.” Ex. 1005 at 3:47-50, FIG. 2 (annotated); Ex. 1003 ¶¶ 110-111.

FIG.2



The “selector 101” is coupled to the “volatile memory 103,” to the “control unit 102,” and to the host system by control, address, and data signal lines. Ex. 1005 at 3:47-50, 4:23-33, FIG. 2; Ex. 1003 ¶ 112. Shimada explains that his invention was intended to address the problems described with respect to the host computer system of Figure 1, Ex. 1005 at 1:40-67, and characterizes the device that seeks to access the memory of his invention (*i.e.*, via the signal lines of selector 101, *id.* at 4:20-34) as “a party that has been allowed an access,” *id.* at 4:29-30 and “an external apparatus,” *id.* at 8:1-8. Ex. 1003 ¶ 113. A skilled artisan would understand from these disclosures that the memory system of Figure 2 is coupled via the control, address and data signals of the selector 101 circuit to a system external to the memory system that communicates with the memory system

(i.e., “a host system”). Ex. 1003 ¶ 113; *see also* Ex. 1005 at 5:43-47, 5:50-53, 6:22-26, 6:30-33, FIGS. 4-5; Ex. 1003 ¶ 114.

Thus, Shimada discloses “*a circuit coupled to the volatile memory subsystem, to the controller, and to a host system.*” Ex. 1001 at 20:35-36 (emphasis added); Ex. 1003 ¶¶ 110-115.

f) First Mode

Shimada discloses a first mode of operation defined by when the selector circuit 101 receives an input select signal (H). Ex. 1005 at 3:64-4:1, 4:20-27; Ex. 1003 ¶¶ 117-118. Shimada explains that in this mode the “selector 101” allows data to be communicated between the “volatile memory 103” and the host system. Ex. 1005 at 4:6-9, 4:23-25, 4:28-33; Ex. 1003 ¶ 119. Shimada therefore discloses “*in a first mode of operation, the circuit is operable . . . to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system.*” Ex. 1001 at 20:37-42 (emphasis added).

Shimada also discloses that in the first mode the “selector 101” does not allow data communication between the host system and the remaining portions of the “semiconductor memory device,” such as “control unit 102” and the “non-volatile memory 104.” *See, e.g.*, Ex. 1005 at 3:47-50, 5:30-34, 9:30-39; Ex. 1003 ¶ 120. A skilled artisan would understand from this disclosure that in the first

mode, the control unit 102 will not be able to communicate with the volatile memory 103 because the selector 101 has coupled the control signal, address signal and data signal lines of the outside system to the volatile memory 103 rather than signal lines of the control unit. Ex. 1003 ¶ 121.

Indeed, one skilled in the art would understand the “selector” of Shimada to be a multiplexor and therefore to operate to prohibit communication with its non-selected ports and therefore isolate those components coupled to such ports. *See* Ex. 1006 at 3:61-63 (U.S. Patent No. 6,810,513 to Vest (“Vest”)); *see also* Ex. 1007 at 6:63-65 (U.S. Patent No. 4,882,709 to Wyland (“Wyland”)); Ex. 1008 at p. 2 (74F257A Selector/Multiplexer Data Sheet by Philips, Mar. 31, 1995 (“Philips”)); Ex. 1003 ¶¶ 122-128. Shimada therefore discloses “*in a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem.*” Ex. 1001 at 20:37-39 (emphasis added).

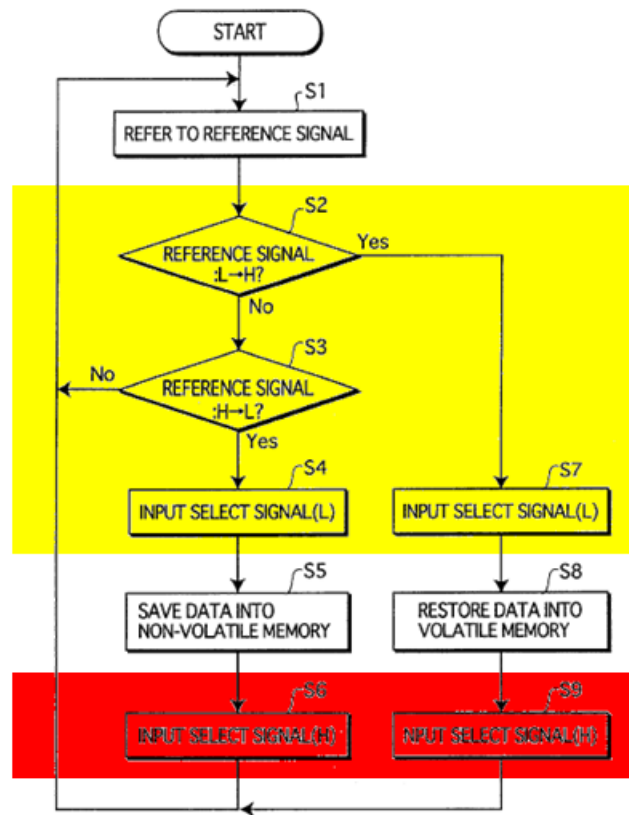
Thus, Shimada discloses “*in a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system.*” Ex. 1001 at 20:37-42 (emphasis added); Ex. 1003 ¶¶ 117-128.

g) Second Mode

Shimada also discloses a second mode of operation, *i.e.*, when the “selector 101” receives an input select signal (L). In the second mode, the “selector 101” allows data to be communicated between the “volatile memory 103” and the “non-volatile memory 104” using the “control unit 102.” Ex. 1005 at 3:55-62, 4:26-27, 4:34-41; Ex. 1003 ¶¶ 136-137. Shimada therefore discloses “*in a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller.*” Ex. 1001 at 20:43-47 (emphasis added).

Shimada further explains that in the “second mode of operation,” (*i.e.*, when the “selector 101” receives a select signal (L)), the “selector 101” does not allow data to be communicated between the “volatile memory 103” and the host system. Ex. 1005 at 3:64-4:1, 4:10-15, FIG. 3. This second mode may be entered into in two different circumstances. *See, e.g.*, Ex. 1005 at 3:64-4:1, FIG. 3 (reproduced and annotated below showing how the “first mode of operation” is triggered in red and how the “second mode of operation” is triggered in yellow); Ex. 1003 ¶ 138.

FIG.3



For example, Shimada explains that, first, the “selector 101” can receive an input select signal (L) after the reference signal has changed from L to H, in which case data is copied from the non-volatile memory 104 to the volatile memory 103. Ex. 1005 at 3:64-4:6, FIG. 3; Ex. 1003 ¶ 139. In this situation, “the control unit 102 . . . shuts out any access to the volatile memory 103 from outside, so that the control unit 102 may access the volatile memory 103.” Ex. 1005 at 3:65-67; Ex. 1003 ¶ 140. Shimada therefore discloses “in a second mode of operation, . . . the

circuit is operable to selectively isolate the volatile memory subsystem from the host system.” Ex. 1001 at 20:43-49 (emphasis added);

Second, and alternatively, the “selector 101” can receive an input select signal (L) after the reference signal has changed from H to L, in which case data is copied from the volatile memory 103 to the non-volatile memory 104. Ex. 1003 ¶ 139. In this situation, “the control unit 102 copies data having been stored in the volatile memory 103 to the non-volatile memory 104 (saving of data) (S5).” Ex. 1005 at 4:14-16, FIG. 3; Ex. 1003 ¶ 141. A skilled artisan would understand that in this situation the host system will not be able to communicate with the volatile memory 103 because the selector 101 has coupled the volatile memory 103 to the control signal, address signal and data signal lines of the control unit 102, rather than to the signal lines of the outside system. Ex. 1003 ¶ 142. Thus, Shimada discloses “*in a second mode of operation, . . . the circuit is operable to selectively isolate the volatile memory subsystem from the host system*” in this alternative manner. *See also* Ex. 1005 at 5:43-47, 5:50-53, 5:65-6:8, 6:22-26, 6:30-33, FIGS. 4-5; Ex. 1003 ¶ 143.

Thus, Shimada discloses the claimed “*second mode*,” Ex. 1003 ¶¶ 136-144, and claim 1 is anticipated.

2. Claim 2

As explained in claim elements (1f) and (1g), the “selector 101” selectively couples the “volatile memory 103” to the host system (*i.e.*, “outside”), and hence selective isolates that “volatile memory 103” from the “control unit 102” when the “selector 101” receives a select signal (H). Ex. 1005 at 4:23-27; *see also id.* 10:2-16 (claim 1); Ex. 1003 ¶¶ 145-146. The “selector 101” also selectively couples the “volatile memory 103” to the “control unit 102,” and hence selectively isolates the “volatile memory 103” from the host system (*i.e.*, “outside”) when the “selector 101” receives a select signal (L). *Id.* Shimada further explains that the select signals (H or L) are from the “control unit 102.” Ex. 1005 at 4:1-3, 4:6-9, 4:10-16, 4:20-23; Ex. 1003 ¶ 147.

Thus, Shimada discloses “*wherein in response to signals from the controller, the circuit is operable to selectively isolate or couple the controller to the volatile memory subsystem, and the circuit is operable to selectively isolate or couple the volatile memory subsystem to the host system.*” Ex. 1001 at 20:50-54 (emphasis added); Ex. 1003 ¶¶ 145-148.

3. Claim 3

Shimada explains that the “selector 101,” which is the “circuit,” as claimed, “switches between two modes.” Ex. 1005 at 4:20-23; Ex. 1003 ¶¶ 149-150.

Accordingly, one skilled in the art would understand that the “selector 101” necessarily includes “one or more switches.” *Id.*

Further, as explained in claim element (1f), one skilled in the art used the terms “selector” and “multiplexer” interchangeably. *See, e.g.*, Ex. 1006 at 3:61-63; *see also* Ex. 1007 at 6:63-65; Ex. 1008 at p. 2; Ex. 1003 ¶ 151. Accordingly, one skilled in the art would have known that the “selector 101” of Shimada is a multiplexer. *Id.*

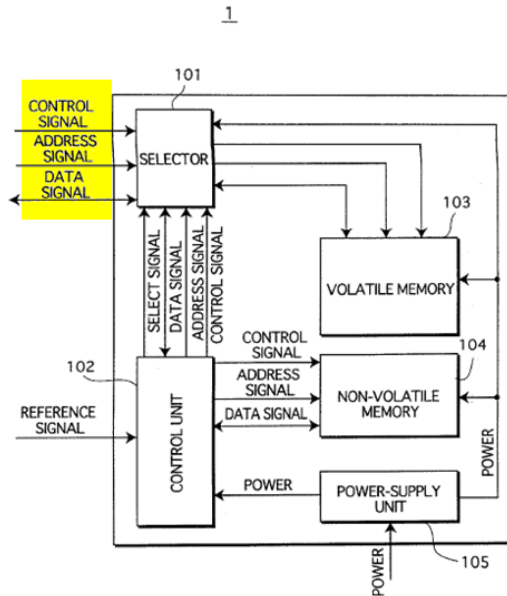
One skilled in the art would have also known that a multiplexer includes “switches.” *See, e.g.*, Ex. 1008 at p. 2; Ex. 1003 ¶ 152. Accordingly, one skilled in the art would have known that the “selector 101” of Shimada is a multiplexer, which is well known to include one or more “switches.” *See* Ex. 1006 at 3:61-63; Ex. 1007 at 6:63-65; Ex. 1008 at p. 2; Ex. 1003 ¶ 152.

Thus, Shimada discloses “*wherein the circuit includes one or more switches.*” Ex. 1001 at 20:55-56 (emphasis added); Ex. 1003 ¶¶ 149-153.

4. Claim 5

Shimada discloses a first set of signal lines (*e.g.*, control signal, address signal, and data signal lines) that couple the “selector 101” to the host. *See* Ex. 1005 at FIG. 2 (annotated below), 4:28-33; Ex. 1003 ¶¶ 155-156.

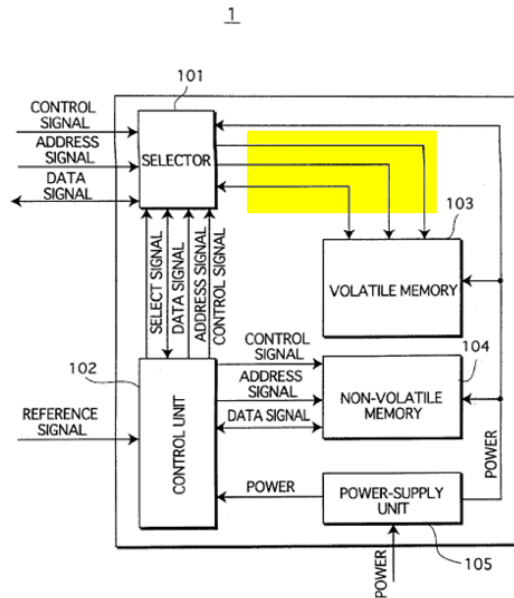
FIG.2



Thus, Shimada discloses “a first set of signal lines to couple the circuit to the host system.” Ex. 1001 at 20:60-61 (emphasis added); Ex. 1003 ¶ 157.

Shimada discloses a second set of signal lines (e.g., control signal, address signal, and data signal lines) that couple the “selector 101” to the “volatile memory 103.” See Ex. 1005 at 4:28-33, FIG. 2 (annotated below); Ex. 1003 ¶¶ 158-159.

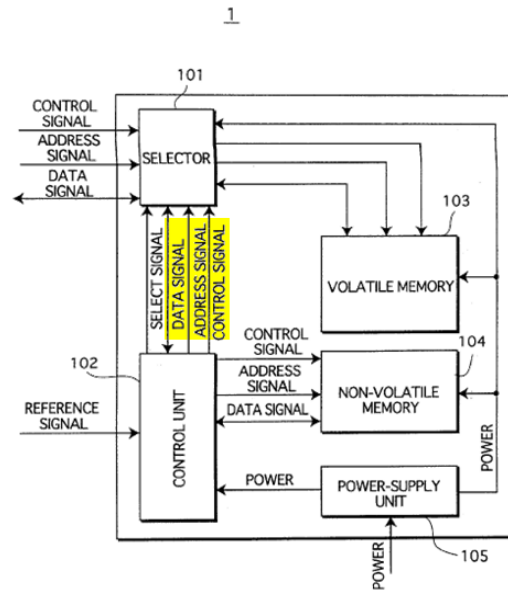
FIG.2



Thus, Shimada discloses “a second set of signal lines to couple the circuit to the volatile memory subsystem.” Ex. 1001 at 20: 62-63 (emphasis added); Ex. 1003 ¶¶ 155-160.

Shimada discloses a third set of signal lines (e.g., control signal, address signal, and data signal lines) that couple the “selector 101” to the “control unit 102.” See Ex. 1005 at 4:39-41, FIG. 2 (annotated below); Ex. 1003 ¶¶ 161-162.

FIG. 2



Thus, Shimada discloses “a third set of signal lines to couple the circuit to the controller.” Ex. 1001 at 20:64-65 (emphasis added); Ex. 1003 ¶¶ 161-163.

As explained above, Shimada discloses that the first, second, and third set of signal lines include data, address and control signal lines. See Ex. 1005 at 4:28-33, 4:39-41, FIG. 2; Ex. 1003 ¶¶ 164-165.

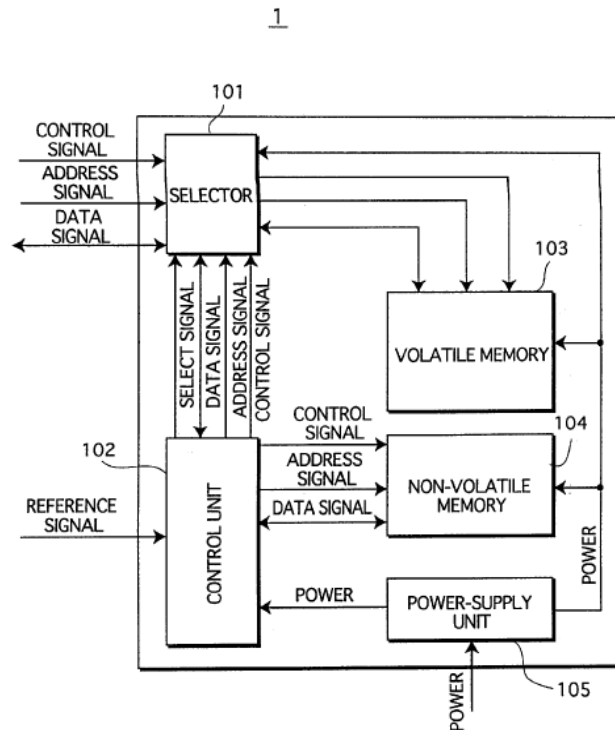
Thus, Shimada discloses “wherein each one of the first, second, and third set of signal lines include data, address and control signal lines.” Ex. 1001 at 20:65-67 (emphasis added); Ex. 1003 ¶¶ 164-166.

5. Claim 6

Shimada explains that the “semiconductor memory device 1,” shown in FIG. 2, is “mountable on a circuit board, in the same manner as existing semiconductor memory devices.” Ex. 1005 at 4:66-5:3; Ex. 1003 ¶¶ 167-168. One skilled in the

art understood that, in order to “mount” a “semiconductor memory device” onto a circuit board, there must necessarily be an interface between the “semiconductor memory device” and other electrical components connected to the circuit board that controls the “semiconductor memory device” (*i.e.*, “host”). *See, e.g.*, Ex. 1021 at 279 (Microsoft Computer Dictionary) (“**Interface** *n.* 1. The point at which a connection is made between two elements so that they can work with each other or exchange information.”) (emphasis added); Ex. 1003 ¶ 168. One skilled in the art also understood that such interface must have been configured to allow electrical communication between the “semiconductor memory device” and the host to serve its intended purpose (*e.g.*, exchange information). In particular, FIG. 2 shows that such electrical communication is through the data, address and control signal lines. *See* Ex. 1005 at FIG. 2 (below); Ex. 1003 ¶ 168.

FIG.2



Thus, Shimada discloses “an interface that is configured to be in electrical communication with the host system and the first set of signal lines.” Ex. 1001 at 21:2-4 (emphasis added); Ex. 1003 ¶¶ 167-169.

FIG. 2 of Shimada shows a plurality of conduits for data, address, and control signals, which forms an “interface” between the host and the “semiconductor memory device 1” (*i.e.*, “memory system,” as claimed). Ex. 1005 at FIG. 2; Ex. 1003 ¶ 171.

Thus, Shimada discloses “wherein the interface provides a plurality of conduits for data, address, and control signals between the memory system and the

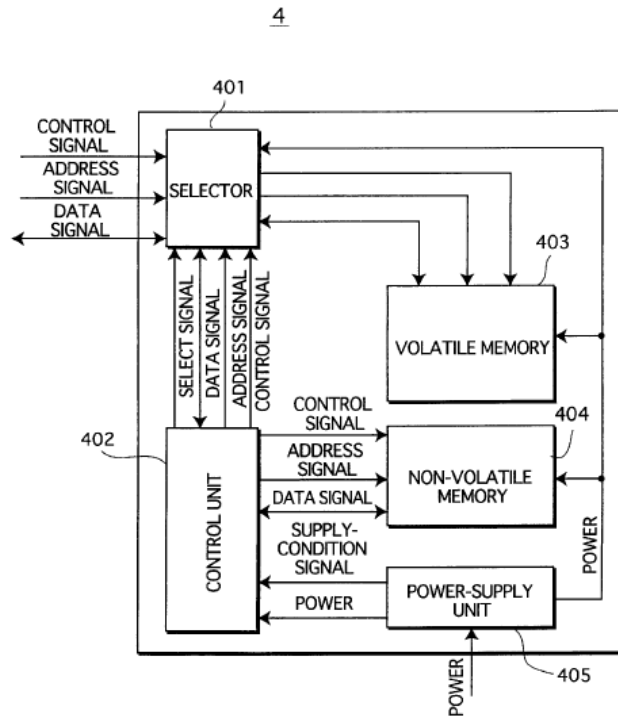
host system using the first set of signal lines.” Ex. 1001 at 21:4-7 (emphasis added); Ex. 1003 ¶¶ 171-172.

6. Claim 7

Shimada explains that the transition of “semiconductor memory device 1” from the first mode to the second mode (*i.e.*, the “selector 101” receiving a select signal (L)) can be in response to various trigger conditions (*e.g.*, “the power supply has begun” or “the power supply has stopped”). Ex. 1005 at 3:64-7:3, 4:10-13; Ex. 1003 ¶¶ 174-175.

Shimada also discloses an alternative embodiment in FIG. 6 (reproduced below), which is substantially similar to the embodiment in FIG. 2, “except for not requiring an input of a reference signal from outside.” Ex. 1005 at 6:66-7:3; Ex. 1003 ¶ 176.

FIG. 6



In this embodiment, the trigger signal (*i.e.*, “supply-condition signal”) comes from the “power-supply unit 405.” Ex. 1005 at 7:10-16. Shimada explains that the “semiconductor memory device 4” transitions from the first mode to the second mode in response to the “supply-condition signal.” Ex. 1005 at 7:17-26; Ex. 1003 ¶ 177.

As such, Shimada explains that the trigger conditions are detected by the “condition-change detect unit” that can detect “power-on to power-off” and “power-off to power-on.” Ex. 1005 at 2:28-39; Ex. 1003 ¶ 178.

Thus, Shimada discloses “*wherein the memory system transitions from the first mode to the second mode in response to a trigger condition.*” Ex. 1001 at 21:8-10 (emphasis added); Ex. 1003 ¶¶ 174-179.

7. Claim 8

As explained in claim 7, Shimada discloses that the transition of “semiconductor memory device 1” from the first mode to the second mode can be in response to various trigger conditions (*e.g.*, “the power supply has begun” or “the power supply has stopped”). Ex. 1005 at 3:64-7:3, 4:10-13; Ex. 1003 ¶¶ 180-181. The “the power supply has stopped” would be a “a power interruption” and also “a power failure.” *Id.*

In the embodiment of FIG. 6, the trigger signal (*i.e.*, “supply-condition signal”) comes from the “power-supply unit 405” and Shimada explains that the “semiconductor memory device 4” transitions from the first mode to the second mode in response to the “supply-condition signal.” Ex. 1005 at 7:10-16; Ex. 1003 ¶ 183.

As such, Shimada explains that the trigger conditions are detected by the “condition-change detect unit” that can detect “power-on to power-off” (*i.e.*, “*power failure,*” “*power interruption,*” “*reboot condition,*” as claimed) and “power-off to power-on.” Ex. 1005 at 2:28-39; Ex. 1003 ¶ 184.

Thus, Shimada discloses “*wherein the trigger condition is any one of a power interruption, a power failure, a power reduction, a system hang-up, a request by the host system, the memory system detects that the host system voltage is below a certain threshold voltage, the memory system detects that the host system voltage is above a certain threshold voltage, the memory system detects that the host system voltage is below a first threshold voltage or above a second threshold voltage, and a reboot condition.*” Ex. 1001 at 21:11-19 (emphasis added); Ex. 1003 ¶¶ 180-185.

8. Claim 9

As explained in claim 8, Shimada discloses that the transition of “semiconductor memory device 1” from the first mode to the second mode can be in response to various trigger conditions (*e.g.*, “the power supply has stopped”), and that the trigger conditions are detected by the “condition-change detect unit” that can detect the transition from the fully “power-on” state to the state of “power-off” (*i.e.*, “power failure,” “power interruption,” “reboot condition,” as claimed). Ex. 1005 at 2:28-39; Ex. 1003 ¶¶ 186-187.

Shimada does not explicitly disclose the details of transitioning from the first mode to the second mode upon detecting that such trigger conditions are “likely to occur.” However, Shimada discloses that “upon detection of a voltage reduction in the main power source, the main power source is replaced.” Ex. 1005 at 1:41-43;

Ex. 1003 ¶ 188. One skilled in the art would have understood that the “condition-change detect unit” detecting a change from “power-on to power-off” must have been implemented in a way that transitions the “semiconductor memory device 1” from the first mode to the second mode before complete “power failure” in order to achieve its intended purpose (*i.e.*, preventing loss of stored data upon power failure). Ex. 1005 at 1:63-67, 9:13-21; Ex. 1003 ¶ 188. Indeed, even in the prior art described by Shimada, the information processing apparatus instructs to save the data from RAM into the external memory device when the battery control apparatus detects merely “a reduction in battery voltage.” Ex. 1005 at 1:34-40; Ex. 1003 ¶ 188. Otherwise, there would be a “loss of the stored data, which would result from a malfunction of the main power source.” Ex. 1005 at 1:45-47; Ex. 1003 ¶ 188. Accordingly, Shimada inherently discloses “*wherein the memory system transitions from the first mode to the second mode upon detecting that a trigger condition is likely to occur.*” Ex. 1003 ¶¶ 186-188.

9. Claim 10

Shimada does not explicitly disclose changing voltage levels of signals communicated between the volatile memory subsystem and the non-volatile memory subsystem. However, one skilled in the art would have understood that the controller unit of Shimada must necessarily have been operable to change the voltage levels of signals communicated between the volatile memory subsystem

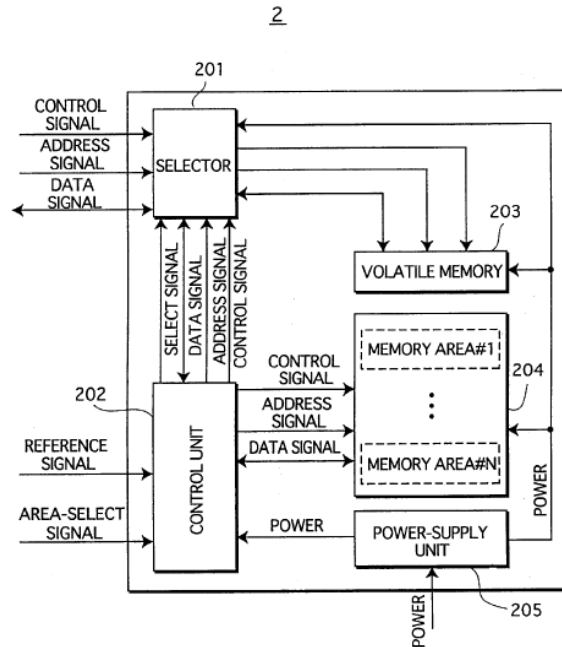
and the non-volatile memory subsystem in order to comply with the different standards associated with those different types of memory and/or to avoid any damage from high voltage. *See, e.g.*, Ex. 1017 at Abstract, 1:14-26, 3:3-6, 3:6-12 (U.S. Patent No. 6,721,212 to Sasaki (“Sasaki”)) ; *see also* Ex. 1018 at 1:17-22 (U.S. Patent No. 5,757,712 to Nagel et al. (“Nagel”)); Ex. 1003 ¶¶ 194-195.

Accordingly, Shimada inherently discloses that “*the controller is operable to perform signal level translation between the volatile memory subsystem and the non-volatile memory subsystem.*” Ex. 1001 at 21:23-26 (emphasis added); *see also* Ex. 1003 ¶¶ 194-195.

10. Claim 11

FIG. 4 of Shimada discloses an embodiment that requires address to address translation between the volatile memory subsystem and the non-volatile memory subsystem. Ex. 1003 ¶ 204. In particular, FIG. 4 discloses an embodiment in which the capacity of the non-volatile memory is N times that of the volatile memory. Ex. 1005 at 5:43-56, FIG. 4; Ex. 1003 ¶ 204.

FIG.4



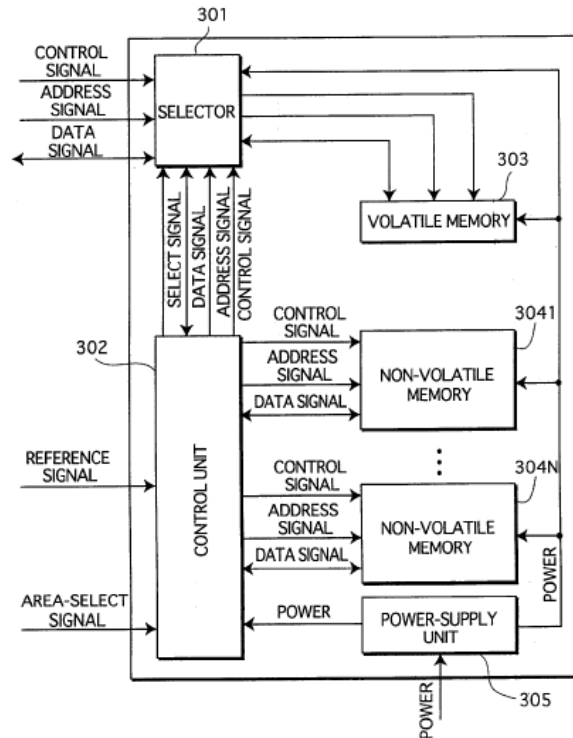
Because the capacity of the non-volatile memory is N times that of the volatile memory, the “control unit 202” must necessarily perform an address to address translation in order to copy data between the non-volatile memory 204 and the volatile memory 203. Shimada explains that such address to address translation is performed using “an area-select signal.” Ex. 1005 at 5:57-64; Ex. 1003 ¶ 205. Shimada explains that “the control unit 202 selects a memory area from the memory areas #1-#N of the non-volatile memory so as to perform data copy between the selected memory area and the volatile memory 203.” Ex. 1005 at 5:60-64; Ex. 1003 ¶ 205.

Alternatively, FIG. 5 (reproduced below) shows an embodiment that is almost the same as the embodiment shown in FIG. 4, except that the non-volatile

memory is increased in number, instead of in capacity. Ex. 1005 at 6:22-26; Ex. 1003 ¶ 206.

FIG.5

3



Because the number of non-volatile memory is N times that of the volatile memory, there is no one-to-one correspondence between the non-volatile memory and the volatile memory. Ex. 1003 ¶ 207. Therefore, the “control unit 302” must necessarily perform an address to address translation in order to copy data between the non-volatile memory (3041 to 304N) and the volatile memory 303. Ex. 1003 ¶ 207. Shimada explains that “[t]he control unit 302 selects one of the non-volatile memories 3041-304N according to the area select signal received from outside the

semiconductor memory device 3, and performs data copy between the selected non-volatile memory and the volatile memory 303.” Ex. 1005 at 6:39-43; Ex. 1003 ¶ 207.

Thus, Shimada discloses “*wherein the controller is operable to perform address to address translation between the volatile memory subsystem and the non-volatile memory subsystem.*” Ex. 1001 at 21:27-30 (emphasis added); Ex. 1003 ¶¶ 201-208.

11. Claim 12

Shimada discloses that the “control unit 102” outputs both the control signal and the address signal. Ex. 1005 at 4:39-41. Ex. 1003 ¶¶ 213-214.

As explained in claim 11, FIG. 4 and FIG. 5 of Shimada disclose embodiments requiring address to address translation before copying data between the non-volatile memory 204 and the volatile memory 203. Ex. 1005 at 5:43-56, 5:57-64, 6:22-26, 6:39-43, FIGs. 4 and 5; Ex. 1003 ¶ 215.

Shimada further explains that “the control unit 202 *selects* a memory area from the memory areas #1-#N of the non-volatile memory so as to perform data copy between the selected memory area and the volatile memory 203.” Ex. 1005 at 5:60-64 (emphasis added); *see also id.* at 6:39-43; Ex. 1003 ¶ 216. Accordingly, one skilled in the art would understand that the “control unit 202” generates the translated address signals for the non-volatile memory. *Id.*

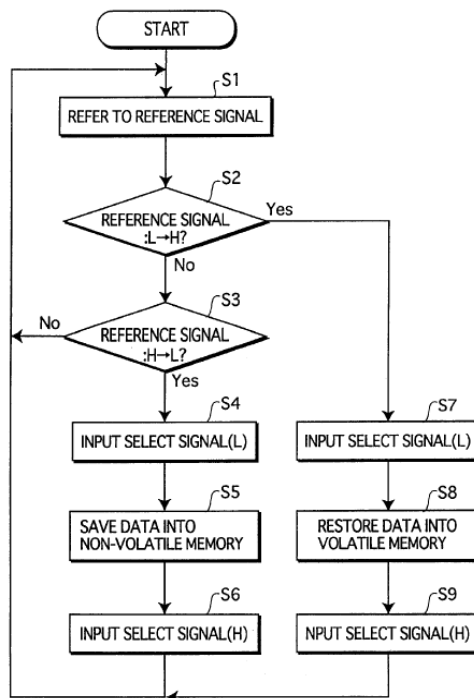
Thus, Shimada discloses “wherein the controller generates at least one of address and control signals for the non-volatile memory subsystem.” Ex. 1001 at 31-33 (emphasis added); Ex. 1003 ¶¶ 213-217.

12. Claim 13

a) Preamble

FIG. 3 of Shimada discloses a method of operating the “semiconductor memory device 1” in FIGs. 2, 4, and 5. Ex. 1005 at 3:21-23, FIG. 3; Ex. 1003 ¶¶ 219-220.

FIG.3



Thus, Shimada discloses “[a] method for operating a memory system.” Ex. 1001 at 21:34-35 (emphasis added); Ex. 1003 ¶¶ 219-221; see also § V.A.1(a).

b) Coupling Step

Claim 13 requires “*coupling a circuit to a host system, a volatile memory subsystem, and a controller, wherein the controller is coupled to a non-volatile memory subsystem.*” Ex. 1001 at 21:36-38 (emphasis added); Ex. 1003 ¶ 222.

Shimada shows this element for the same reasons set forth above. See §§ V.A.1(b)-(e); Ex. 1003 ¶¶ 222-223.

c) First Mode

Claim 13 requires “*in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, using the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system.*” Ex. 1001 at 21:39-44 (emphasis added); Ex. 1003 ¶ 224.

Shimada shows this element for the same reasons set forth above. See §§ V.A.1(e), (f); Ex. 1003 ¶¶ 224-225.

d) Second Mode

Claim 13 requires “*in a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, using the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.*” Ex. 1001 at 21:45-51 (emphasis added); Ex. 1003 ¶ 226.

Shimada shows this element for the same reasons set forth above. See §§ V.A.1(e), (g); Ex. 1003 ¶¶ 226-228.

13. Claim 14

Claim 14 requires “[t]he method of claim 13, further comprising: using the circuit to selectively isolate or couple the controller to the volatile memory subsystem in response to signals from the controller; and using the circuit to selectively isolate or couple the volatile memory subsystem to the host system in response to signals from the controller.” Ex. 1001 at 21:52-58 (emphasis added); Ex. 1003 ¶ 229.

Shimada anticipates claim 14 for the same reasons set forth above for claim 2. See § V.A.2.; Ex. 1003 ¶¶ 229-230.

14. Claim 15

Claim 15 requires “[t]he method of claim 13, wherein the circuit includes one or more switches.” Ex. 1001 at 21:59-60 (emphasis added); Ex. 1003 ¶ 231.

Shimada anticipates claim 15 for the same reasons set forth above for claim 3. See § V.A.3.; Ex. 1003 ¶¶ 231-232.

15. Claim 17

Claim 17 requires “[t]he method of claim 13, further comprising: coupling the circuit to the host system via a first set of signal lines; coupling the circuit to the volatile memory subsystem via a second set of signal lines; and coupling the circuit to the controller via a third set of signal lines, wherein each one of the first,

second, and third set of signal lines includes data, address and control signal lines.” Ex. 1001 at 21: 63-22:4 (emphasis added); Ex. 1003 ¶ 233.

Shimada anticipates claim 17 for the same reasons set forth above for claim 5. *See* § V.A.4.; Ex. 1003 ¶¶ 233-234.

16. Claim 18

Claim 18 requires “[t]he method of claim 17, further comprising: using an interface to couple the first set of signal lines to the host system, wherein the interface is configured to be in electrical communication with the host system, and wherein the interface provides a plurality of conduits for data, address, and control signals between the memory system and the host system.” Ex. 1001 at 22:5-11 (emphasis added); Ex. 1003 ¶ 235.

Shimada anticipates claim 18 for the same reasons set forth above for claim 6. *See* § V.A.5.; Ex. 1003 ¶¶ 235-236.

17. Claim 19

Claim 19 requires “[t]he method of claim 13, further comprising: transitioning the memory system from the first mode to the second mode in response to a trigger condition.” Ex. 1001 at 22:12-14 (emphasis added); Ex. 1003 ¶ 237.

Shimada anticipates claim 19 for the same reasons set forth above for claim 7. *See* § V.A.6.; Ex. 1003 ¶¶ 237-238.

18. Claim 20

Claim 20 requires “[t]he method of claim 19, wherein the trigger condition is any one of a power interruption, a power failure, a power reduction, a system hang-up, a request by the host system, the memory system detects that the host system voltage is below a certain threshold voltage, the memory system detects that the host system voltage is above a certain threshold voltage, the memory system detects that the host system voltage is below a first threshold voltage or above a second threshold voltage, and a reboot condition.” Ex. 1001 at 22:15-23 (emphasis added); Ex. 1003 ¶ 239.

Shimada anticipates claim 20 for the same reasons set forth above for claim 8. See § V.A.7.; Ex. 1003 ¶¶ 239-240.

19. Claim 21

Claim 21 requires “[t]he method of claim 13, further comprising: transitioning the memory system from the first mode to the second mode upon detecting that a trigger condition is likely to occur.” Ex. 1001 at 22:24-27 (emphasis added); Ex. 1003 ¶ 241.

Shimada anticipates claim 21 for the same reasons set forth above for claim 9. See § V.A.8.; Ex. 1003 ¶¶ 241-242.

20. Claim 22

Claim 22 requires “[t]he method of claim 13, further comprising: using the controller to provide signal level translation between the volatile memory

subsystem and the non-volatile memory subsystem.” Ex. 1001 at 22:28-31

(emphasis added); Ex. 1003 ¶ 243.

Shimada anticipates claim 22 for the same reasons set forth above for claim 10. See § V.A.9.; Ex. 1003 ¶¶ 243-244.

21. Claim 23

Claim 23 requires “[t]he method of claim 13, further comprising: using the controller to perform address to address translation between the volatile memory subsystem and the non-volatile memory subsystem.” Ex. 1001 at 22:32-35 (emphasis added); Ex. 1003 ¶ 245.

Shimada anticipates claim 23 for the same reasons set forth above for claim 11. See § V.A.10.; Ex. 1003 ¶¶ 245-246.

22. Claim 24

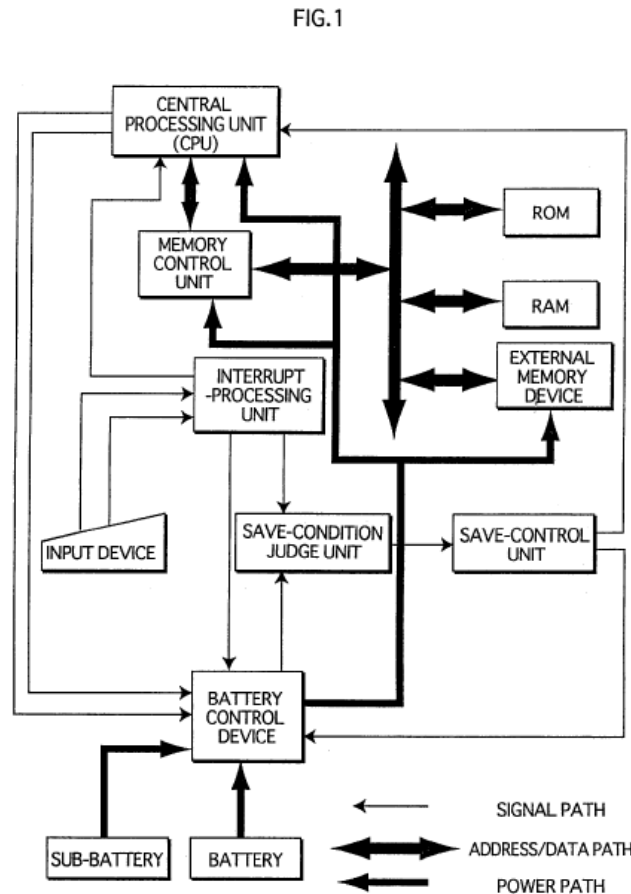
Claim 24 requires “[t]he method of claim 13, further comprising: using the controller to generate at least one of address and control signals for the non-volatile memory subsystem.” Ex. 1001 at 22:36-38 (emphasis added); Ex. 1003 ¶ 247.

Shimada anticipates claim 24 for the same reasons set forth above for claim 12. See § V.A.11.; Ex. 1003 ¶¶ 247-248.

23. Claim 25

a) Preamble

FIG. 1 of Shimada discloses a “nontransitory computer readable storage medium” (e.g., ROM). See Ex. 1005 at FIG. 1. Ex. 1003 ¶¶ 249-250.



To the extent the preamble is limiting the claim, one skilled in the art would have understood that the ROM (as shown in FIG. 1 of Shimada) is a “nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices,” as claimed, that can store a program that performs the methods described in FIG. 3 of Shimada. Ex. 1001 at 2:20-22); *see also*, Ex. 1020 at 1:13-15 (U.S. Patent No. 4,607,332 to Goldberg

(“Goldberg”)) (“A Read-Only Memory (ROM) is often used to store programs for computers, especially in microcomputer systems.”); Ex. 1003 ¶ 251.

Thus, Shimada discloses “[a] *nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices, said programs, when executing on the one or more computing devices, causing a circuit that is coupled to a host system, to a volatile memory subsystem, and to a controller that is coupled to a non-volatile memory subsystem.*” Ex. 1001 at 22:39-45 (emphasis added); Ex. 1003 ¶¶ 249-252; *see also* §§ V.A.1(a)-(e), V.A.13(a), (b).

b) First Mode

Claim 25 requires “*in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, operating the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system.*” Ex. 1001 at 22:46-50 (emphasis added); Ex. 1003 ¶ 254.

Shimada shows this element for the same reasons set forth above. *See* §§ V.A.1(f), V.A.13(c); Ex. 1003 ¶¶ 254-255.

c) Second Mode

Claim 25 requires “*in a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory*

subsystem via the controller, operating the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.” Ex. 1001 at 22:52-58 (emphasis added); Ex. 1003 ¶ 256.

Shimada shows this element for the same reasons set forth above. *See* §§ V.A.1(g), V.A.13(d); Ex. 1003 ¶¶ 256-258.

24. Claim 26

Claim 26 requires “[t]he nontransitory computer readable storage medium of claim 25, wherein the method further comprises: transitioning the memory system from the first mode to the second mode in response to a trigger condition.” Ex. 1001 at 22:59-62 (emphasis added); Ex. 1003 ¶ 259.

Shimada anticipates claim 26 for the same reasons set forth above for claims 7 and 19. *See* §§ V.A.6, V.A.6.17; Ex. 1003 ¶¶ 259-260.

25. Claim 27

Claim 27 requires “[t]he nontransitory computer readable storage medium of claim 26, wherein the trigger condition is any one of a power interruption, a power failure, a power reduction, a system hang-up, a request by the host system, the memory system detects that the host system voltage is below a certain threshold voltage, the memory system detects that the host system voltage is above a certain threshold voltage, the memory system detects that the host system voltage is below

a first threshold voltage or above a second threshold voltage, and a reboot condition.” Ex. 1001 at 22:63-23:5 (emphasis added); Ex. 1003 ¶ 261.

Shimada anticipates claim 27 for the same reasons set forth above for claims 8 and 20. *See* §§ V.A.7, V.A.18; Ex. 1003 ¶¶ 261-262.

26. Claim 28

Claim 28 requires “[t]he nontransitory computer readable storage medium of claim 25, wherein the method further comprises: transitioning the memory system from the first mode to the second mode upon detecting that a trigger condition is likely to occur.” Ex. 1001 at 23:6-10 (emphasis added); Ex. 1003 ¶ 263.

Shimada anticipates claim 28 for the same reasons set forth above for claims 9 and 21. *See* §§ V.A.8, V.A.19; Ex. 1003 ¶¶ 263-264.

27. Claim 29

Claim 29 requires “[t]he nontransitory computer readable storage medium of claim 25, wherein the method further comprises: using the controller to provide signal level translation between the volatile memory subsystem and the non-volatile memory subsystem.” Ex. 1001 at 23:11-15 (emphasis added); Ex. 1003 ¶ 265.

Shimada anticipates claim 29 for the same reasons set forth above for claims 10 and 22. *See* §§ V.A.9, V.A.20; Ex. 1003 ¶¶ 265-266.

28. Claim 30

Claim 30 requires “[t]he nontransitory computer readable storage medium of claim 25, wherein the method further comprises: using the controller to perform address to address translation between the volatile memory subsystem and the non-volatile memory subsystem.” Ex. 1001 at 23:16-20 (emphasis added); Ex. 1003 ¶ 267.

Shimada anticipates claim 30 for the same reasons set forth above for claims 11 and 23. *See* §§ V.A.10, V.A.21; Ex. 1003 ¶¶ 267-268.

B. Claims 4 and 16 are Obvious over Shimada in view of Oh

Claims 4 and 16 require “wherein the circuit includes an on-die termination.” Ex. 1003 ¶¶ 269, 277.

To the extent one might argue Shimada does not explicitly disclose this claim element, it would have been obvious to implement the circuit of Shimada using an on-die termination structure. Implementing circuit elements within memory devices using an on-die termination structure was well-known as of the priority date of the ’243 Patent. *See, e.g.*, Ex. 1012 (Oh) at 1:13-20; Ex. 1003 ¶ 270.

In particular, Oh explains that on-die termination is a technology where the termination resistor for impedance matching in transmission lines is located inside an integrated circuit of the memory device instead of on mother boards or printed

circuit boards. Ex. 1012 at 1:13-20; Ex. 1003 ¶ 271. Oh further explains that the on-die termination structure includes “switch elements.” Ex. 1012 at 1:38-49; Ex. 1003 ¶ 271.

Oh further teaches that On Die Termination can be on the “memory device” or outside the memory device (*e.g.*, on the “memory controller”). Ex. 1012 at 1:16-20; Ex. 1003 ¶ 272.

Shimada and Oh are analogous art to the '243 Patent because they are all in the same field of endeavor, *i.e.*, memory systems, (Ex. 1001 at 1:34-56; Ex. 1005 at 1:15-18; Ex. 1012 at 1:11-28), are at least reasonably pertinent to the particular problem addressed by the '243 Patent, *e.g.*, transitioning between various power states. Ex. 1001 at 1:34-2:38, 3:24-27, 6:23-34, 7:49-62; Ex. 1005 at 1:63-3:5, 2:28-39, 4:20-27; Ex. 1012 at 10:5-11; Ex. 1003 ¶ 273.

One skilled in the art would have been motivated to combine Shimada and Oh, because of the desire to increase the bandwidth of the memory systems by matching the impedances within the integrated circuit. *See* Ex. 1012 at 1:13-20; *see also* Ex. 1013 at 1:16-18 (U.S. Patent No. 7,208,973 to Kwon (“Kwon”)); Ex. 1003 ¶ 274.

One skilled in the art would have been also motivated to combine Shimada and Oh, because implementing an on-die termination outside the volatile memory device was routinely done at the time the '243 Patent was filed, and therefore

would have been expected to provide predictable, and therefore reliable, performance. *See, e.g.*, Ex. 1011 at ¶¶ [0140], [0091] (U.S. Patent Publication No. 2008/0010435 to Smith et al. (“Smith”)); Ex. 1003 ¶ 275. Moreover, a skilled artisan would have been further motivated to employ such a combination because an off-chip on-die terminations were required by standards at the time the ’243 Patent was filed, and a skilled artisan would have been motivated to comply with such standards. *See, e.g.*, Ex. 1014 at 27-40 (JESD205); Ex. 1003 ¶ 275. For example, U.S. Pat. No. 5,630,096 to Zuravleff (Ex. 1022) teaches that it is desirable to design memory systems compatible with JEDEC standards for DRAMS to support many design applications. Ex. 1022, 1:65-2:3; Ex. 1003 ¶ 275.

Thus, Shimada in view of Oh renders obvious claims 4 and 16. Ex. 1003 ¶¶ 269-278.

C. Claims 1, 3, 13, 15, and 25 are Obvious over Shimada in view of Bonella

1. Claims 1 and 13

To the extent one might argue that the “selector 101” of Shimada is not operable to “*selectively isolate the controller from the volatile memory subsystem*” in this first mode of operation as required by claims 1 and 13, it would have been obvious to include that functionality in Shimada in view of Bonella (Ex. 1009). Ex. 1003 ¶ 129.

In particular, Bonella discloses a hybrid memory system including a volatile memory and a non-volatile memory. Ex. 1009 at Abstract, ¶ [0027], FIG. 1; Ex. 1003 ¶ 130.

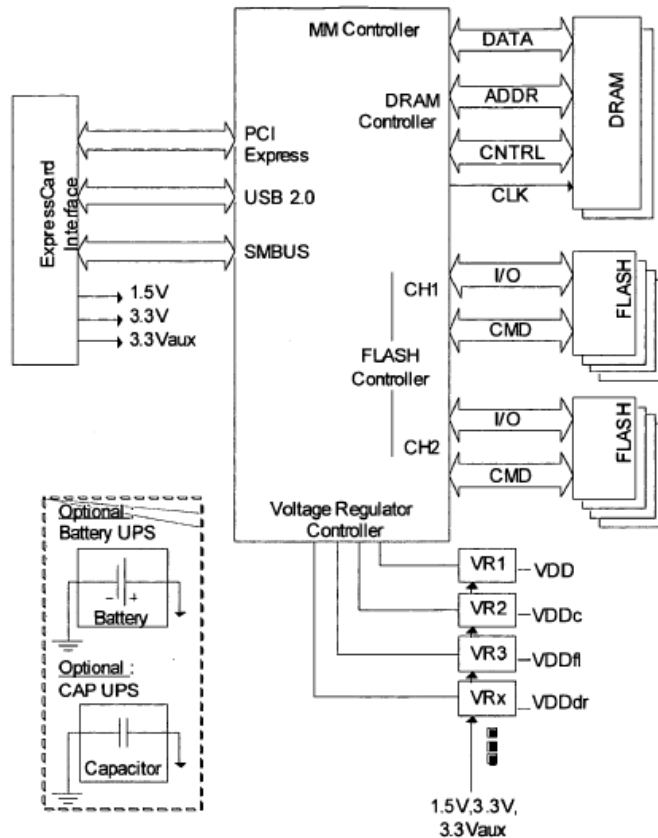


FIG. 1 Memory Module Block Diagram

Bonella explains that the data in the DRAM is written to the Flash memory upon detecting a power loss. Ex. 1009 at ¶ [0101]; Ex. 1003 ¶ 131. Bonella further explains that a router (within the “Memory Module Controller”) determines which data may be communicated between the two memories and/or the host. Ex. 1009 at FIG. 2, ¶ [0041]; Ex. 1003 ¶ 132.

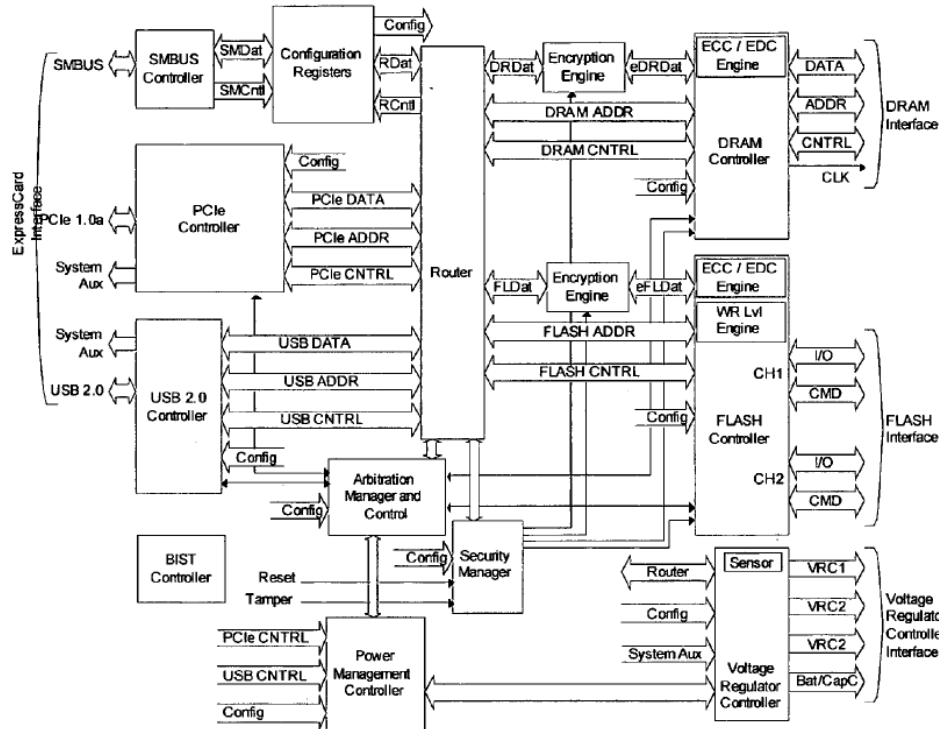


FIG. 2 Memory Module Controller Block Diagram

Bonella further discloses that the router “is made up of path multiplexers.”

Ex. 1009 at ¶ [0043]; Ex. 1003 ¶ 133. Use of path multiplexors would have selectively isolated unselected ports. Ex. 1003 ¶¶ 122-126; Ex. 1008 at pp. 2-3; Ex. 1006 at 3:61-63; Ex. 1007 at 6:63-65. Accordingly, one skilled in the art would have found it obvious to implement the “selector 101” of Shimada to be “operable to selectively isolate the controller from the volatile memory subsystem,” in the first mode of operation, by using one or more path multiplexers as shown in Bonella. Ex. 1003 ¶ 134.

Shimada and Bonella are both analogous art to the '243 Patent because each is from the field of memory systems. See, e.g., Ex. 1001 at 1:34-56; Ex. 1005 at

1:15-18; Ex. 1009 at ¶ [0002]; Ex. 1003 ¶ 135. Further, Shimada and Bonella are also reasonably pertinent to the particular problem addressed by the '243 Patent (*e.g.*, copying data between non-volatile memory and volatile memory within a hybrid memory system). *See, e.g.*, Ex. 1001 at 3:24-25, 7:49-62; Ex. 1005 at 4:34-41; Ex. 1009 at Abstract, ¶¶ [0027], [0101]; Ex. 1003 ¶ 135.

One skilled in the art would have been motivated to combine Shimada and Bonella for various reasons. First, it was commonly known that writing to a non-volatile memory is much slower than writing to a volatile memory, Ex. 1009 at [0027], and one skilled in the art would have been motivated to use the “multiplexer” of Bonella in the scheme of Shimada to isolate the load of the non-volatile memory and achieve “the same access speed as that of the conventional volatile memory” when the volatile memory is being accessed by the host. Ex. 1005 at 5:30-34, 9:30-39. Second, one skilled in the art would have been motivated to use the “multiplexer” of Bonella in the scheme of Shimada to “greatly reduce the erase/write cycles to be performed for the non-volatile memory portion,” as it is commonly known that non-volatile memory can be written to for only a limited number of times. Ex. 1005 at 9:30-35; Ex. 1003 ¶ 135. Thus, it would have been obvious to include the “selectively isolating” functionality of Bonella in the system of Shimada.

Further, to the extent one might argue that Shimada does not disclose “*a circuit coupled to the volatile memory subsystem, to the controller, and to a host system*” (as required by claim 1) or “*coupling a circuit to a host system, a volatile memory subsystem, and a controller*” (as required by claim 13), it would have been obvious to enable electric communication with the host by coupling the memory device of Figure 2 to a host computer system. Ex. 1003 ¶ 116. Shimada states that his invention is intended to address the problems he describes with the host computer system of Figure 1, Ex. 1005 at 1:40-67, thereby expressly suggesting that his memory device should be coupled to such a system, Ex. 1003 ¶ 116. Moreover, a skilled artisan would understand that the types of semiconductor memory disclosed in Shimada (*e.g.*, DRAM and flash) are conventionally used in host computer systems, *see id.* at 1:20-45, and so would be motivated to couple the memory device (*e.g.*, FIG. 2) of Shimada in such a system via the signal lines of the selector 101 in order to employ the invention of Shimada in a conventional computer system and thereby gain the advantage in such a system of secure data retention without the need for a large-scale backup power source in a power loss situation, and “enhanced erase/write cycle endurance.” Shimada at 1:64-67; Ex. 1003 ¶ 116.

Accordingly, claims 1 and 13 would have been obvious over Shimada in view of Bonella. Ex. 1003 ¶¶ 116, 129-135, 228.

2. Claims 3 and 15

To the extent one might argue that Shimada does not disclose that the “*circuit includes one or more switches*” as required by claims 3 and 15, it would have been obvious to include it in the system of Shimada. Ex. 1003 ¶ 154. Shimada discloses that selector 101 performs a switching operation, Ex. 1005 at 4:20-23, and switches are a well-known and conventional circuit element as of the priority date of the ’243 Patent. *See, e.g.*, Ex. 1010 at ¶¶ [0001], [0016] (U.S. Patent Publication No. 2002/0053944 to Brass *et al.* (“Brass”)); Ex. 1003 ¶ 154. It would have been merely common sense for a skilled artisan to implement the basic switching functionality of “selector 101” with conventional switching circuitry. Ex. 1003 ¶ 154. To do so would have been the use of a prior art structure for its prior art purpose to achieve a predictable result, and a skilled artisan would have been motivated to use one or more switches because of their well-understood functionality and structure. One skilled in the art would also have been motivated to use conventional devices whose operation is well known and readily available. *Id.* Moreover, as demonstrated in § V.C.1, one skilled in the art would have found it obvious to use Bonella’s “multiplexer” in the scheme of Shimada. Ex. 1003 ¶ 154, which a skilled artisan would have known included a number of switches. *See* § V.C.1; Ex. 1006 at 3:61-63; Ex. 1007 at 6:63-65; Ex. 1008 at 2; 1003 at ¶

154. Accordingly, Shimada in view of Bonella renders obvious claims 3 and 15.

Id.

3. Claim 25

Patent Owner may also argue that certain elements of claim 25 are not disclosed in Shimada, but that claim would still be unpatentable as obvious even if one were to credit such arguments.

For example, to the extent one might argue that Shimada does not disclose a “*nontransitory computer readable storage medium*,” it would have been obvious to include it in the system of Shimada. Shimada discloses a “nontransitory computer readable storage medium” (*e.g.*, ROM), Ex. 1005 at FIG. 1, and using ROMs to store programs for computer systems was well known as of the priority date of the ’243 Patent. *See, e.g.*, Ex. 1020 at 1:13-15; Ex. 1003 ¶ 253. It would have been merely common sense for a skilled artisan to store the program performing the functionality described in Shimada into a “nontransitory computer readable storage medium.” Ex. 1003 ¶ 253. For example, one skilled in the art would have been motivated to use ROM to store programs because it is not only non-volatile, but more secure in a power outage or surge situations compared to Flash memory. Ex. 1003 ¶ 253. To do so would have been the use of a prior art structure for its prior art purpose to achieve a predictable result, and a skilled artisan would have been motivated to store programs on nontransitory computer readable storage mediums

such as ROMs because of their well-understood functionality and structure. Ex. 1003 ¶ 253.

To the extent one might argue that the “selector 101” of Shimada is not a circuit to “*selectively isolate the controller from the volatile memory subsystem,*” modifying the “selector 101” of Shimada to “*selectively isolate the controller from the volatile memory subsystem*” would have been obvious over Shimada in view of Bonella for the same reasons set forth above for claim 1. See § V.C.1; Ex. 1003 ¶¶ 129-135, 255.

To the extent one might argue that Shimada does not disclose “*a circuit that is coupled to a host system,*” coupling the “selector 101” of Shimada to a host system would have been obvious over Shimada for the same reasons set forth above for claim 1. See § V.C.1; Ex. 1003 ¶ 116.

Accordingly, claim 25 would have been obvious over Shimada in view of Bonella. See § V.C.1; Ex. 1003 ¶¶ 116, 129-135, 253, 255, 258.

D. Claims 6 and 18 are Obvious over Shimada

Claims 6 and 18 require similar limitations directed to “an interface,” which Shimada renders obvious even if one were to conclude that it does not disclose such limitations. For example, to the extent one might argue that Shimada does not disclose “*an interface that is configured to be in electrical communication with the host system and the first set of signal lines,*” as required by claim 6, it would

have been obvious to include it in the system of Shimada in order to connect the memory device with the outside world. Ex. 1003 ¶ 170. As demonstrated above, Shimada discloses that his invention is intended to solve the problems he explains with respect to Figure 1. Ex. 1005 at 1:30-40; Ex. 1003 ¶ 170. Shimada also discloses a number of signal lines coming from the “outside,” and “an external apparatus.” Ex. 1005 at FIG. 2, 4:6-9, 4:23-27, 5:30-34, 7:67-8:3; Ex. 1003 ¶ 170. A skilled artisan would understand that for Shimada’s invention to work and/or be useful the signal lines connecting to the volatile memory would necessarily have to be coupled to the host computer system via some type of interface, and would be motivated to employ such an interface to use the invention of Shimada. Ex. 1003 ¶ 170

Similarly, to the extent one might argue that Shimada does not disclose “*wherein the interface provides a plurality of conduits for data, address, and control signals between the memory system and the host system using the first set of signal lines,*” it would have been obvious to include it in the system of Shimada. Ex. 1003 ¶ 173. As demonstrated above, it would have been obvious to form an interface between the host and the semiconductor memory device in Shimada, because without such interfaces, there would be no electrical communication, and hence no exchange of information, between the “semiconductor memory device” and the host. *See, e.g.*, Ex. 1021 at 279; Ex. 1003 ¶ 173. Moreover, since Shimada

discloses data, address, and control signals for coupling to the volatile memory, Ex. 1005 at FIG. 2, it would have further been obvious to employ an interface that included conduits that used signal lines for each of those different types of signals, so as to simplify the design of the system and keep the different type of signals separate. Further, one skilled in the art would have known that conduits for the signals can be optimized for signal noise reduction, speed, and reliability. Ex. 1003 ¶ 173.

Accordingly, claim 6 would have been obvious in view of Shimada. Ex. 1003 ¶ 170. Claim 18, which requires “*using an interface to couple the first set of signal lines to the host system, wherein the interface is configured to be in electrical communication with the host system, and wherein the interface provides a plurality of conduits for data, address, and control signals between the memory system and the host system,*” would have been obvious for the same reasons. *Id.*

E. Claims 9, 21, and 28 are Obvious over Shimada in view of Goodwin

To the extent one might argue that “*transitions/[ing] from the first mode to the second mode upon detecting that a trigger condition is likely to occur*” as required by claims 9, 21 and 28 is not disclosed by Shimada, it would have been obvious to include it in the system of Shimada. Ex. 1003 ¶ 189. It was known to skilled artisans to switch to a mode of operation and use backup power upon detecting that a “power failure” is likely to occur, as opposed to switching when it

is too late. *See, e.g.*, Ex. 1015 at 1:37-54 (Goodwin); Ex. 1003 ¶ 189. Thus, use of that technique in the system of Shimada would have been merely the use of known prior art technique for its known purpose to achieve a predictable result. Ex. 1003 ¶ 189

Shimada and Goodwin are analogous art to the '243 Patent because they are at least reasonably pertinent to the particular problem addressed by the '243 Patent (*i.e.*, dealing with potential power disruptions in electronic circuits). Ex. 1001 at 1:34-2:38; Ex. 1005 at 1:63-3:5; Ex. 1015 at Abstract, 1:63-2:39; Ex. 1003 ¶ 190.

As explained in Goodwin, anticipating the occurrence of a potential power failure can provide additional time for the device to react to the power failure, thereby avoiding any disruptions. Ex. 1015 at 1:46-54; Ex. 1003 ¶ 191. Goodwin further explains that a well known way of anticipating the power failure is by detecting “when the load voltage decreases below a set reference threshold.” Ex. 1015 at 3:38-40; Ex. 1003 ¶ 191. One skilled in the art would therefore have been motivated to combine Shimada with the power backup technologies disclosed in Goodwin to further ensure that the volatile memories in Shimada do not lose data by entering the backup mode when a power loss condition could reasonably be expected. Ex. 1005 at 1:28-29; Ex. 1003 ¶ 191. As explained in Shimada, “[s]ince DRAM and SRAM are volatile memories, they need to receive power *all the time*, in order to retain the data having been stored therein.” Ex. 1005 at 1:26-28

(emphasis added). Accordingly, one skilled in the art would have been motivated to combine the teachings of Shimada with the power failure detection circuitry that can “anticipate” the occurrence of a power failure, so that the transition from the first mode to the second mode can occur before the trigger condition (*e.g.*, “power failure”) occurs. *See, e.g.*, Ex. 1015 at 1:46-54; Ex. 1003 ¶¶ 191-192.

Thus, Shimada in view of Goodwin renders obvious these claims. Ex. 1003 ¶¶ 189-193.

F. Claims 10, 22, and 29 are Obvious over Shimada in view of Sasaki

To the extent one might argue that those claim elements relating to a controller that performs “*signal level translation between the volatile memory subsystem and the non-volatile memory subsystem,*” as required by claims 10, 22 and 29, are not disclosed by Shimada, it would have been obvious over Shimada in view of Sasaki (Ex. 1017). Ex. 1003 ¶ 196. As explained in Sasaki, one skilled in the art would have known that volatile memory and non-volatile memory have different input swing levels that are acceptable. *See, e.g.*, Ex. 1017 at 3:3-6; Ex. 1003 ¶ 196.

Shimada and Sasaki are analogous art to the '243 Patent because they are all in the same field of endeavor, *i.e.*, hybrid memory systems including volatile and non-volatile memory subsystems. *See, e.g.*, Ex. 1001 at 3:20-31, FIG. 1; Ex. 1005 at 2:1-13, 3:45-5:38, FIG. 2; Ex. 1017 at 3:3-6, 7:6-32, FIGS. 1, 14; Ex. 1003

¶ 196. Further, Shimada and Sasaki are reasonably pertinent to the particular problem addressed by the '243 Patent (*e.g.*, sharing signal lines between non-volatile memory and volatile memory). *See, e.g.*, Ex. 1001 at 3:24-25, 7:49-62; Ex. 1005 at 4:34-41; Ex. 1017 at Abstract, FIGs. 1, 14; Ex. 1003 ¶ 196.

Sasaki further explains that one must translate the voltage levels between non-volatile memory and volatile memory systems in order to prevent any high voltage (used in non-volatile memory systems) from being applied to volatile memory systems, and a skilled artisan would therefore have been motivated to employ that technique in the system of Shimada. Ex. 1017 at 3:6-12; Ex. 1003 ¶ 196.

One skilled in the art would also have been motivated to combine Shimada and Sasaki to comply with the applicable JEDEC standards and therefore employ readily-available standard-compliant memories in the system of Shimada. Ex. 1003 ¶ 197. In particular, Shimada teaches transfer of data between non-volatile memory and volatile memory. *See, e.g.*, Ex. 1005 at 3:55-62, 4:34-41; Ex. 1003 ¶ 197. As explained in Sasaki, the logic interface for volatile memory (*e.g.*, RAM) is in accordance with the SSTL standard (which requires higher voltage) while the logic interface for non-volatile memory is in accordance with TTL (which require lower voltage). Ex. 1017 at Abstract, 1:14-26; Ex. 1003 ¶ 197.

Further, one skilled in the art would have been motivated to combine the teachings of Shimada with the voltage translation techniques in Sasaki because they would have known that volatile memory systems would not function or be damaged if a high voltage was applied. *See, e.g.*, Ex. 1018 at 1:17-22; Ex. 1003 ¶ 198.

Accordingly, one skilled in the art would have found it obvious to perform a signal level translation (by changing the voltage level) when copying data from a non-volatile memory to a volatile memory (or vice versa). Ex. 1003 ¶ 199.

Thus, Shimada in view of Sasaki renders obvious claims 10, 22, and 29. Ex. 1003 ¶¶ 196-200.

G. Claims 11, 12, 23, 24, and 30 Patent are Obvious over Shimada in view of Tsunoda

1. Claims 11, 23, and 30

To the extent one might argue that a controller that can “*perform address to address translation between the volatile memory subsystem and the non-volatile memory subsystem,*” as required by claims 11, 23, and 30, is not disclosed by Shimada, it would have been obvious over Shimada in view of Tsunoda. Ex. 1003 ¶¶ 209-212.

For example, Tsunoda explains that the “control unit” translates the address between the volatile memory (“SDRAM”) and non-volatile memory (“flash memory”) using an “address correspondence setting function.” Ex. 1019 at

¶ [0062]; Ex. 1003 ¶ 210. Tsunoda further explains that such translation is done by using a “mapping table.” Ex. 1019 at ¶ [0107]; Ex. 1003 ¶ 210.

Shimada and Tsunoda are analogous art to the '243 Patent because they are all in the same field of endeavor, *i.e.*, hybrid memory systems including volatile and non-volatile memory subsystems. *See, e.g.*, Ex. 1001 at 3:20-31, FIG. 1; Ex. 1005 at 2:1-13, 3:45-5:38, FIG. 2; Ex. 1019 at ¶ [0001], FIG. 1; Ex. 1003 ¶ 211. Further, Shimada and Tsunoda are reasonably pertinent to the particular problem addressed by the '243 Patent (*e.g.*, copying data between non-volatile memory and volatile memory). *See, e.g.*, Ex. 1001 at 3:24-25, 7:49-62; Ex. 1005 at 4:34-41; Ex. 1019 at ¶¶ [0002], [0042]; Ex. 1003 ¶ 211.

Moreover, one skilled in the art would have been motivated to combine Shimada and Tsunoda, and use the “address translation” techniques of Tsunoda in the hybrid memory system of Shimada because, in certain embodiments of Shimada, the capacity of the non-volatile memory is N times that of the volatile memory, Ex. 1005 at 5:43-56, FIG. 4, or the number of non-volatile memory is greater than that of the volatile memory, Ex. 1005 at 6:22-26, Ex. 1003 ¶ 212. In particular, one skilled in the art would have been motivated to use the “address translation” techniques of Tsunoda in these embodiments of Shimada where there is no one-to-one correspondence between the address(es) of the non-volatile memory and the volatile memory, because without such “address translation,” not

all of the non-volatile memory space could be utilized (*i.e.*, because the capacity of the non-volatile memory is greater than that of the volatile memory). *Id.*

Accordingly, claims 11, 23 and 30 would have been obvious over Shimada in view of Tsunoda. Ex. 1003 ¶¶ 209-212.

2. Claims 12 and 24

To the extent one might argue that a controller that “*generates at least one of address and control signals for the non-volatile memory subsystem,*” as required by claims 12 and 24, is not disclosed by Shimada, it would have been obvious over Shimada in view of Tsunoda. Ex. 1003 ¶ 218. As explained in claim 11, Tsunoda discloses a “control unit” that translates the address between the volatile memory (“SDRAM”) and non-volatile memory (“flash memory”) using an “address correspondence setting function,” Ex. 1019 at ¶ [0062], using a “mapping table.” *Id.* at ¶ [0107], and generates control signals in order to execute data transfer. Ex. 1003 ¶ 218. One skilled in the art would understand that the “control unit” of Tsunoda generates the translated address signals for the non-volatile memory subsystems in Tsunoda. Ex. 1003 ¶ 218. Accordingly, the “control unit” of Tsunoda “generates at least one of address and control signals,” as required by claim 12. One skilled in the art would have been motivated to combine Shimada and Tsunoda for reasons set forth in claim 11. *Id.*

Accordingly, claims 12 and 24 would have been obvious over Shimada in view of Tsunoda. *Id.*

VI. CONCLUSION

For the foregoing reasons, the challenged claims are unpatentable.

Dated: January 6, 2017

Respectfully Submitted,

/Joseph Micallef/
Joseph A. Micallef
Registration No. 39,772
Sidley Austin LLP
1501 K Street NW
Washington, DC 20005

CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,400 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

Dated: January 6, 2017

Respectfully Submitted,

/Joseph Micallef/
Joseph A. Micallef
Registration No. 39,772
Sidley Austin LLP
1501 K Street NW
Washington, DC 20005

Petition for *Inter Partes* Review of U.S. Patent No. 8,671,243

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 8,671,243**

Attachment A:

Proof of Service of the Petition

Petition for *Inter Partes* Review of U.S. Patent No. 8,671,243

CERTIFICATE OF SERVICE

I hereby certify that on this 6th day of January, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

Khaled Shami
P.O. Box 60610
Palo Alto CA 94306

Dated: January 6, 2017

Respectfully Submitted,

/Joseph Micallef/
Joseph A. Micallef
Registration No. 39,772
Sidley Austin LLP
1501 K Street NW
Washington, DC 20005

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Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Petition for *Inter Partes* Review of U.S. Patent No. 8,671,243

Exhibit #	Reference Name
1001	U.S. Patent No. 8,671,243
1002	File History of U.S. Patent No. 8,671,243
1003	Declaration of Ron Maltiel
1004	Curriculum Vitae of Ron Maltiel
1005	U.S. Patent No. 6,693,840 to Shimada <i>et al.</i>
1006	U.S. Patent No. 6,810,513 to Vest
1007	U.S. Patent No 4,882,709 to Wyland
1008	74F257A Selector/Multiplexer Data Sheet by Philips (March 31, 1995)
1009	U.S. Patent Publication No. 2007/0136523 to Bonella <i>et al.</i>
1010	U.S. Patent Publication No. 2002/0053944 to Brass <i>et al.</i>
1011	U.S. Patent Publication No. 2008/0010435 to Smith <i>et al.</i>
1012	U.S. Patent No. 7,486,104 to Oh <i>et al.</i>
1013	U.S. Patent No. 7,208,973 to Kwon
1014	JEDEC Standard, DDR2 SDRAM Fully Buffered DIMM Design Specification, JESD205 (March 2007)
1015	U.S. Patent No. 4,658,204 to Goodwin
1016	U.S. Patent No. 7,107,480 to Moshayedi <i>et al.</i>
1017	U.S. Patent No. 6,721,212 to Sasaki
1018	U.S. Patent No. 5,757,712 to Nagel
1019	U.S. Patent Publication No. 2003/0028733 to Tsunoda <i>et al.</i>
1020	U.S. Patent No. 4,607,332 to Goldberg
1021	Microsoft Computer Dictionary, Fifth Edition (2002)
1022	U.S. Patent No. 5,630,096 to Zuravleff <i>et al.</i>