Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.,

Petitioners,

v.

NETLIST, INC.

Patent Owner

Patent No. 8,516,185

Issued: August 20, 2013

Filed: April 15, 2010

Inventors: Hyun Lee and Jayesh R. Bhakta

Title: System and Method Utilizing Distributed Byte-Wise Buffers on a Memory Module.

Inter Partes Review No. IPR2014-00577

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,516,185 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123

TABLE OF CONTENTS

PETITIONER'S MANDATORY NOTICES

A. Real Party-in-Interest (37 CFR § 42.8(b)(1))

The real parties of interest of this petition are SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

B. Related Matters (37 CFR § 42.8(b)(2))

U.S. Patent No. 8,516,185 ("the '185 Patent") is or was involved in the following legal proceedings:

- IPR2014-01369 ("the '1369 IPR") filed by Smart Modular Technologies challenging the validity of claims 1-19 of the '185 Patent (the '1369 IPR was not instituted) (EX1011);
- IPR2014-01029 ("the '1029 IPR") filed by SanDisk challenging the validity of claims 1-19 of the '185 Patent (the '1029 IPR was not instituted) (EX1012);
- *Netlist, Inc. v. SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.*, Case No. 8:16-cv-01605 (C.D. Cal. filed Aug. 31, 2016)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016)

C. Lead and Back-up Lead Counsel (37 CFR § 42.8(b)(3))

Lead Counsel is: Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492.

Back-up Counsel are:

- Theodore W. Chandler (Reg. No. 50,319), Sidley-SKH-IPR@sidley.com, (213) 896-5830
- Wonjoo Suh (Reg. No. 64,124), Sidley-SKH-IPR@sidley.com, (202) 736-8831
- Ferenc Pazmandi (Reg. No. 66,216), Sidley-SKH-IPR@sidley.com, (415) 772-7410.

D. Service Information (37 CFR § 42.8(b)(4))

Service on Petitioner may be made by e-mail (Sidley-SKH-IPR@sidley.com), mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

I. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Certification the '185 Patent May Be Contested by Petitioner

Petitioner certifies it is not barred or estopped from requesting *inter partes* review of U.S. Patent No. 8,516,185 ("the '185 Patent") (EX1001). Neither Petitioner, nor any party in privity with Petitioner, has filed a civil action challenging the validity of any claim of the '185 Patent. Neither Petitioner, nor any party in privity with Petitioner, has filed a prior *inter partes* review ("IPR") challenging the validity of any claim of the '185 Patent.

Petitioner also certifies this petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of a patent. Petitioner therefore certifies this patent is available for *inter partes* review.

B. Fee for Inter Partes Review (§ 42.15(a))

The Director is authorized to charge the fee specified by 37 CFR § 42.15(a) to Deposit Account No. 50-1597.

C. Proof of Service (§§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

II. Identification of Claims Being Challenged (§ 42.104(b))

Petitioners propose several grounds for trial as set forth below, none of which is redundant. Each ground is based primarily on U.S. Patent No. 7,024,518 to Halbert et al. ("Halbert") (EX1005). However, Petitioners also address several

arguments that Patent Owner may raise in response by proposing grounds that more closely satisfy the claim limitations to which such arguments would be directed. Such additional grounds are not redundant because they are "rational, narrowly targeted, and not burdensome considering only five claims with very similar limitations are at issue." IPR2015-01912, Paper 10 at 17-18 (3/22/2016). Petitioners therefore respectfully request that trial be instituted on all grounds and arguments advanced herein. Specifically, this Petition seeks a finding that claims 1-3, 7, 8, and 10-12 of the '185 Patent are unpatentable as follows:

(i) U.S. Patent No. 7,024,518 to Halbert et al. ("Halbert") (EX1005) anticipates claims 1-3, 7, 8, and 10-12 of the '185 Patent under 35 U.S.C. § 102;

(ii) Halbert renders obvious claims 1-3, 7, 8, and 10-12 of the '185 Patent under 35 U.S.C. § 103;

(iii) Halbert in view of U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. ("Amidi") (EX1019) renders obvious claims 1-3, 7, 8, and 10-12 of the '185 Patent under 35 U.S.C. § 103;

(iv) Halbert in view of U.S. Patent No. 6,070,217 to Connolly et al. ("Connolly") (EX1016) renders obvious claim 3 of the '185 Patent under 35 U.S.C. § 103; and

(v) Halbert in view of JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) ("JESD79") (EX1007) renders obvious Claim 10 of the '185 Patent under 35 U.S.C. § 103.

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ III-V, below. The evidence relied upon in this petition is listed in **Attachment B**.

III. Relevant Information Concerning the Contested Patent

A. Effective Filing Date of the '185 Patent

The application that resulted in the '185 Patent is U.S. Patent Application Serial No. 12/761,179, filed April 15, 2010. EX1001 at 1. The '185 Patent is a continuation-in-part of application No. 12/504,131 filed on July 16, 2009 (published January 20, 2011 as U.S. Patent Aplication Publication No. 2011/0016269). *Id*.; *see also*, Ex. 1021 ("the '131 priority application"). As the '185 Patent includes substantial new matter added to the '131 priority application, it is unclear whether and which claims are properly supported by the priority application. But even if the '131 priority application were found to support the challenged '185 claims, the prior art relied upon in this petition was either filed or published well before the July 16, 2009, date of the prior application. *See* §§ IV.A-C. Thus, whether the '185 Patent is entitled to the earlier priority date is irrelevant to the issues raised by this petition. Therefore, in order to simplify the issues in the

present procedure, Petitioner assumes for purposes of this proceeding that the claims of the '185 Patent have an effective filing date of July 16, 2009.[1]

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the '185 Patent in 2009 would have been someone with an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and at least five years working the field. Such a person would have been knowledgeable about the design and operation of computer memories, most particular DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and more low level circuits such as tri-state buffers, flip flops and registers. EX1003 ¶45.

C. The '185 Patent

1. Technical Overview

[1] Petitioner reserves the right to challenge the priority date of any of the '185 patent claims if it becomes a material issue for any reason.

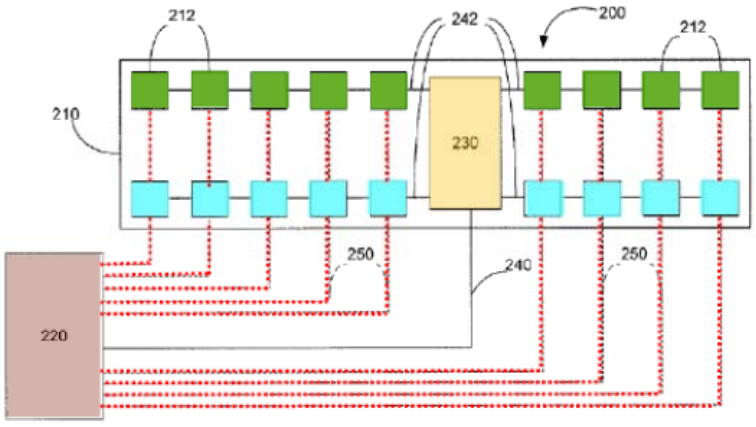
The ’185 Patent is directed to computer memory subsystems including memory boards that have memory devices, such as dynamic random-access memory (DRAM) devices or synchronous dynamic random-access memory (SDRAM) devices, mounted on a printed circuit board (PCB). EX1001, 1:14-23. These memory boards are configured to be attached to memory slots of the computer system. *Id.* at 23-27. EX1003 ¶46.

“Memory boards typically include one or more memory modules,” such as one or more dual in-line memory modules (DIMMs). EX1001, 1:14-32. The memory devices of each module can be organized into rows or “ranks.” *Id*. Exemplary two and four rank modules are illustrated in FIGS. 1A, 1B, 2A and 2B of the ’185 Patent. *Id.*, 1:55-65, 4:31-5:4, 14-59-60. “During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals.” *Id*., 1:47-51. Such memory modules were well known at the time and specific designs were standardized by a consortium called Joint Electron Device Engineering Council (JEDEC). *Id.*; EX1003 ¶47.

An exemplary JEDEC memory module 210 is illustrated in FIG. 2A of the ’185 Patent. EX1001, FIG. 2A (reproduced below with annotations). The memory module 210 includes memory devices 212 organized in two ranks (green and blue

rows). *Id.* The memory module 210 communicates with a system memory controller 220 (brown) of the computer system through control lines 240 (continuous black) and data lines 250 (dashed red). EX1001, 5:27-47. The memory module 210 has a register 230 (orange) which receives the control lines 240 and which, in turn, is connected to the memory devices 212 of the two ranks (green, blue) through module control lines 242. *Id.* In this prior art system, the data lines 250 (dashed red) directly connect the system controller 220 (brown) to the memory devices 212 of the two ranks (green, blue). *Id.*; EX1003 ¶48.

Figure 2A: (Prior Art)



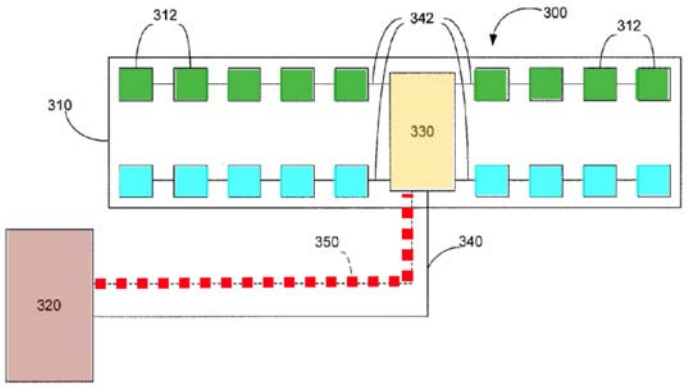
The '185 Patent explains that, in such systems, increasing memory space can raise problems. EX1001, 3:66-4:27. For example, "by directly adding memory chips, a heavier load is presented to the outputs of the system controller and the outputs of the memory devices, resulting in a slower system." *Id.*, 4:12-14. Also, "the increase in the number of the memory devices translates to an increase in the

distributed RC load on the data paths, but not on the control paths (*e.g.*, address paths), thereby introducing uneven signal propagation delay between the data signal paths and control signal paths." *Id.*, 4:22-24. In the example of FIG. 2A, "during a write operation, the system memory controller 220 sees all the memory devices 212 as its load via the data lines 250, and during a read operation, each memory device 212 sees multiple other memory devices 212, as well as the system memory controller 220, as its load via the data lines 250." *Id.,* 5:41-46. According to the '185 Patent, such systems "suffer from large loads which result in slower clock speeds." *Id.* at 6:45-45; EX1003 ¶49.

The '185 Patent admits that this "large load" problem was addressed in the prior art by "a memory buffer which handles both the control signals and the data signals." EX1001, 6:46-47. Prior systems with such a control-and-data buffer are illustrated in FIG. 2C and 2D of the '185 Patent. *Id.* at 6:48-7:22. In the example of FIG. 2C (reproduced below with annotations), a memory module 310 has a memory buffer 330 (orange) which receives both the control lines 340 (continuous black) and the data lines 350 (dashed red) from the system controller 320 (brown), and connects to the memory devices 312 in two ranks (green and blue) through

control lines 342 and data lines (not shown) on the module. EX1003 ¶50.

Figure 2C: (Prior Art)

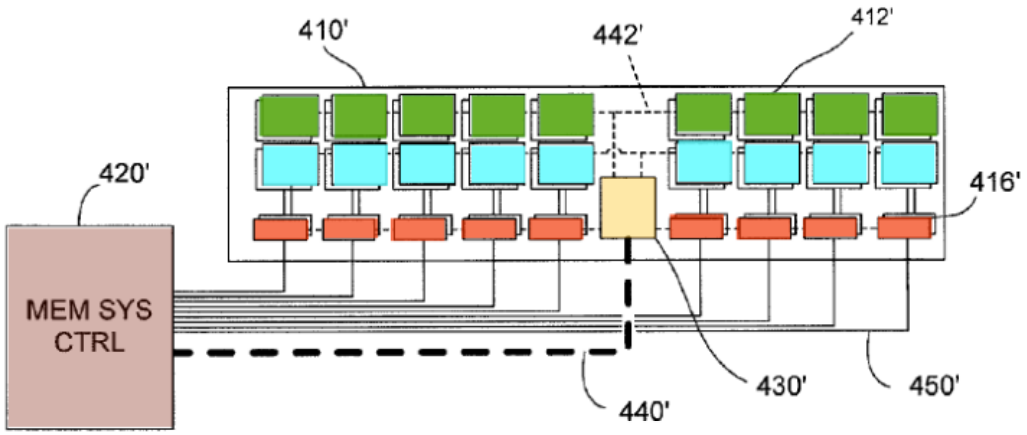


According to the '185 Patent, a load reducing memory module with such a single control-and-data buffer (as shown in FIG. 2C above) has "significant drawbacks" because it "includes an extremely large number of data lines (not shown for clarity)." EX1001, 6:64-7:2. To address these alleged drawbacks, the '185 Patent's "memory module . . . includes a plurality of circuits, for example byte-wise buffers, which are configured to selectively isolate the plurality of memory devices from the system memory controller. The circuits are operable . . . to drive write data from the system memory controller to the plurality of memory devices and to merge read data from the plurality of memory devices to the system memory controller. The circuits are distributed at corresponding positions separate from one another." *Id.,* Abstract; EX1003 ¶51.

An exemplary embodiment of a memory module with such distributed buffers is shown in FIG. 3C of the '185 Patent (reproduced below with

annotations). *See also* EX1001, 7:23-60. Here, the control lines 440′ (dashed) and data lines 450′ (solid) are coupling the system memory controller 420′ (brown) to the memory modules 410′. *Id.,* 7:34-40. The memory module 410’ includes multiple ranks of memory devices 412’ (green and blue), a control circuit 430’ (orange), and multiple data transmission circuits 416’ (red) that are “distributed at corresponding positions relative to the at least one printed circuit board . . . 410′.” *Id*., 8:7-8. The control circuit 430’ is coupled to the control lines 440’ from the system memory controller 420’ and provides control signals to the memory devices 412’ in the module. *Id.*, 10:10-30. The transmission circuits 416’ are coupled to the system memory controller 420’ by the data lines 450’ and receive module control signals from the controller 430’. *Id*., 8:8-12; EX1003 ¶52.

Figure 3C:



Each of the data transmission circuits 416’ (red) is also coupled to at least two memory devices (green and blue) and “is configurable to respond to the

module control signals by selectively allowing or inhibiting data transmission" between the system controller 420' (brown) and a selected one of the two memory devices 412 (green and blue). EX1001, 8:12-31; EX1003 ¶53.

"[T]hese data transmission circuits . . . 416′ [(red)] can be referred to as 'load-reducing circuits' or 'load-reducing switching circuits' . . . to reduce the load seen by the system memory controller . . . 420′ when operatively coupled to the memory module." EX1001, 10:41-47. "To reduce the memory device loads seen by the system memory controller 420 [(brown)] (e.g., during a write operation), the data transmission circuit 416 [(red)] . . . is advantageously configured to be recognized by the system memory controller 420 as a single memory load. This advantageous result is desirably achieved . . . by using the data transmission circuits 416[(red)] to electrically couple only the enabled memory devices 412 to the memory controller 420 (e.g., the one, . . . to which data is to be written) and to electrically isolate the other memory devices 412 from the memory controller 420 (e.g., the one . . . to which data is not to be written)." *Id*., 14:30-42; EX1003 ¶54.

The '185 Patent's "FIG. 5 schematically illustrates an example data transmission circuit 416." EX1001 , 14:63-64, FIG. 5 (reproduced below with

annotation); EX1003 ¶55.

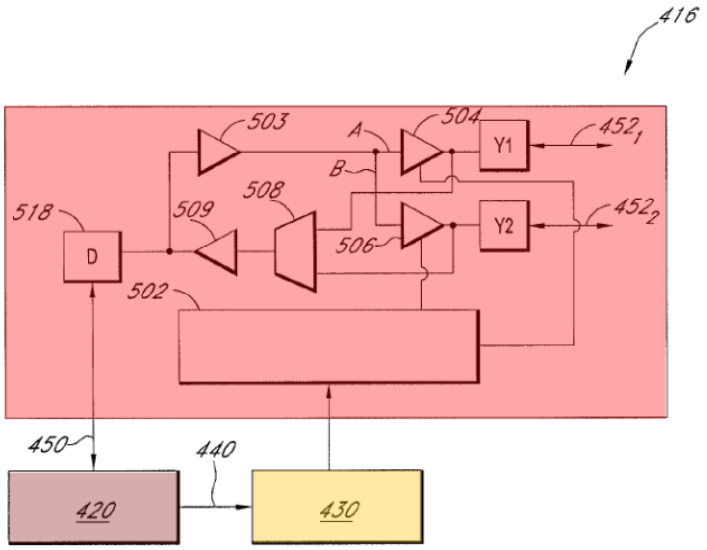


FIG. 5

"In the operational embodiment shown in FIG. 5, in a write operation, data entering a data transmission circuit 416 [(red)] via a data line 518 is driven onto two data paths, labeled path A and path B, preferably after passing through a write buffer 503." *Id.*, 15:13-17. "For a write operation, during the CAS latency, the control circuit 430 . . . provides enable control signals to the control logic circuitry 502 of each data transmission circuit 416, whereby the control logic circuitry 502 selects either path A or path B to direct the data. Accordingly, when the control logic circuitry 502 receives . . . an 'enable A' signal, a first tristate buffer 504 in path A is enabled and actively drives the data value on its output, while a second tristate buffer 506 in path B is disabled with its output in a high impedance condition." *Id.*, 15:47-50; EX1003 ¶56.

"For a read operation, the data transmission circuit 416 operates as a multiplexing circuit. In . . . FIG. 5, for example, data signals read from the memory devices 412 of a rank are received at the first or second terminals Y1, Y2 of the data transmission circuit 416. The data signals are fed to a multiplexer 508, which selects one to route to its output. The control logic circuitry 502 generates a select signal to select the appropriate data signal, and the selected data signal is transmitted to the system memory controller 420 along a single data line 518, preferably after passing through a read buffer 509. The read buffer 509 may be a tristate buffer that is enabled by the control logic circuitry 502 during read operations." EX1001, 15:60-16:5. The '185 Patent also explains that other variations of multiplexers and tristate buffers may also be used. *Id.*, 16:5-11; EX1003 ¶57.

The '185 Patent's "data transmission circuits 416 present a load on the data lines 518 from the write buffer 503 and the read buffer 509 . . . . that is substantially the same as the load that one of the memory devices 412 would present. Similarly, the data transmission circuits 416 present a load on the first and second terminals Y1, Y2 from the multiplexer 508 and the first tristate buffer 504 (on the first terminal Y1) and the second tristate buffer 506 (on the second terminal Y2)[] . . . that is substantially the same as the load that the memory controller 420 would present." EX1001, 16:12-30; EX1003 ¶58.

2. Prosecution History

The application underlying the '185 Patent was filed on April 15, 2010, as a continuation-in-part of the '131 priority application. EX1002, p. 1 (Filing Receipt, 4/29/2010).

Before examination, the original claims were cancelled and a new set of claims were filed. EX1002, pp. 6-9 (Prelim. Amendment, 2/6/2012). The new set of claims were rejected as being anticipated by US Patent No. 8,130,560 to Rajan et al. which discloses buffer chips between the memory devices and the data bus. EX1002, p. 56 (Office Action, 3/23/2012). In response, the applicants amended the claims to require that each of the data transmission circuits be configured to selectively allow data transmission between the system memory controller and a selected memory device and to selectively isolate another memory device. EX1002, pp.70-73 (Amendment, 6/21/2012). Applicant argued that Rajan's buffers, even if they isolate, they do not "selectively" allow data transmission between the system memory controller and a selected memory device, and do not "selectively" isolate another memory device from the system memory controller. *Id.*, pp. 74-75. Applicant also argued that "Rajan does not disclose that the buffer chips are responsive to any module control signals produced by the Rajan register." *Id.*, p. 75.

The Examiner rejected the amended claims over Rajan in view of US Patent Application Publication No. 2006/0262586 by Solomon et al. (EX1006). *See, e.g.*, EX1002, pp. 86-89 (Office Action, 9/13/2012). Solomon discloses a memory module with a circuit that "selectively isolates one or more loads of the memory devices from the computer system." EX1006, Abstract, and FIG. 1.

The applicants further amended the claims to recite that the selective data transmission with one memory device and the selective isolation of another memory device happens "in response to the module control signals," (EX1002,pp. 104-05 (Amendment, 3/13/2013)), and argued that the cited art did not disclose that element. In light of these amendments and arguments, the Examiner allowed the claims. EX1002, pp. 124-26 (Notice of Allowance, 7/11/2013).

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 CFR § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

1. *"selectively isolate"*

The broadest reasonable interpretation of the term "*selectively isolate*" is "selectively electrically separating one component from another."

The Board has previously interpreted the phrase "selectively isolate" in the '185 Patent to mean "electrically separate one component from another." IPR2014-01369, Paper 12 at 7-8 (3/9/2015). This interpretation, however, does not seem to require a "selective" separation of components. Because each word of a patent claim is assumed to have meaning, the isolation required by this claim must be "selective" in some manner. Although one skilled in the art might be able to read the Board's interpretation in IPR2014-01369 as including some "selectivity," in order to avoid any ambiguity, that characteristic of the claimed isolation should be explicit. Moreover, ensuring the interpretation maintains the selectivity expressly set forth in the claims is also consistent with the '185 Patent applicants' argument during prosecution that Rajan's buffer chips provide load isolation but do not selectively isolate as required by the claims. *See supra* §III.C.2. Petitioners' proposed interpretation therefore makes that limitation of the claims explicit.

Petitioner's proposed interpretation is also consistent with the disclosure of the '185 Patent, which describes circuitry that "electrically couple" a memory device to a memory controller and at the same time other memory devices are "electrically isolated" from the memory controller. *See, e.g.*, EX1001, 14:36-40 (".

. . using the data transmission circuits 416 to electrically couple only the enabled memory devices 412 to the memory controller . . . and to electrically isolate the other memory devices 412 from the memory controller ”). That disclosure would be read by a skilled artisan to mean that in the context of the ’185 Patent isolating two components from each other is the opposite of coupling them (which would be electrical separation), and also that the ’185 Patent concerned with selective isolation, not just any isolation at all. EX1003 ¶73.

Thus, a person of ordinary skill in the art would conclude that the broadest reasonable construction of the term “*selectively isolate*” is selectively electrically separating one component from another component. In the context of the claim language at issue here, one component is a memory device which is selectively electrically separated from another component, the system controller. EX1001, 18:53-55 (“*selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller*”) EX1003 ¶¶71-79.

IV. Overview of the Prior Art

A. U.S. Patent No. 7,024,518 to Halbert et al. (EX1005)

The application for U.S. Patent No. 7,024,518 to Halbert et al. (“Halbert”) was filed on March 13, 2002, published on August 15, 2002, and issued as a patent

on April 4, 2005. EX1005 at 1. Halbert is prior art to the '815 Patent pursuant to at least 35 U.S.C. §§ 102 (a), (b) and (e).

Halbert discloses "a new memory module architecture" for a typical memory system configuration at the time, such as that shown in FIG. 1 (reproduced below). EX1005, Abstract, 1:31-39; EX1003 ¶81.

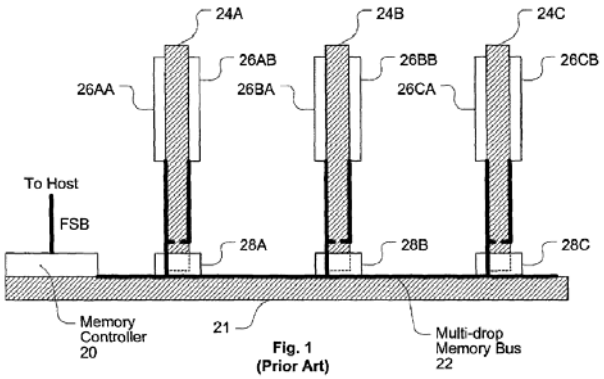
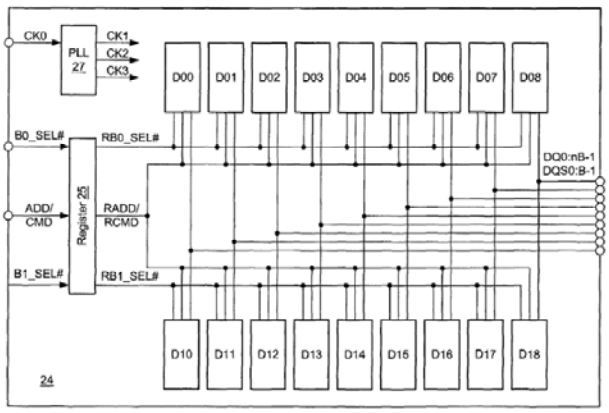


Fig. 1
(Prior Art)

Halbert's FIG. 1 illustrates an exemplary system with three memory modules 24A, 24B, and 24C, such as Dual In-Line Memory Modules (DIMMs), inserted into corresponding sockets 28A, 28B and 28C and connected to a Memory Bus 22 which connects the memory modules to a system Memory Controller 20. EX1005, 1:61-2:14. The memory bus 22 carries clock and control signals, address signals, command signals, and data signals. *Id*., 1:40-60. EX1003 ¶82.

Halbert also illustrates an exemplary prior art module, "a registered DIMM 24 containing eighteen memory devices arranged in two banks, one containing devices D00-D08 and the other containing devices D10-D18." EX1005, 2:25-28, and FIG. 2 (reproduced below).

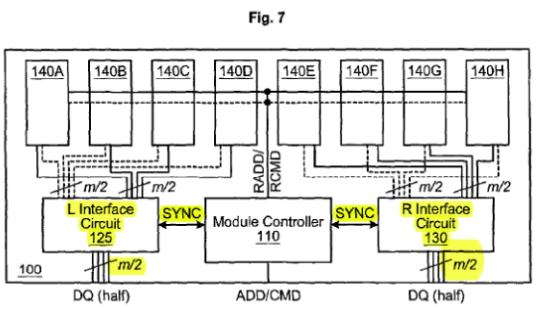
Fig. 2
(Prior Art)

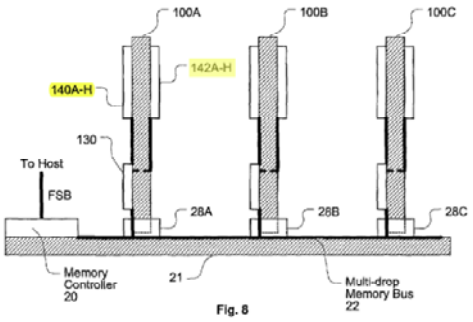


The DIMM 24 has a register 25 that latches on the address and command signals ADD/CMD and re-drives those signals onto the module's address/command bus to the memory devices D00-D18. The register 25 also receives bank select signals B0_SEL# and B1_SEL# and provides registered versions of those to chip select pins of corresponding banks of memory devices. The data lines from each bank are connected to a common set of DQ lines carrying data and DQS lines carrying data strobes. Each device has a data width of 'n' (4, 8, or 16) bits that add up to the total of n*B data lines, where 'B' is the number of memory devices per bank (here, nine). This prior art module has data lines directly connecting the memory chips to the system data bus 22. *Id.*; EX1003 ¶83.

Halbert's new module architecture improves on the prior art modules and can be implemented to be "transparent to the memory system and to the memory devices . . . [which] allows for an embodiment that is compatible with an existing memory controller/bus and with existing memory devices." EX1005, 3:49-57. An

exemplary implementation of Halbert's inventive module is shown in FIGS. 7 and 8 (reproduced below with annotations). EX1003 ¶84.





In the implementation of FIGS. 7 and 8, the module 100 has a module controller 110 which, like the register 25 in the prior art module, receives the address and command signals from the system controller and provides registered versions of those signals to two ranks of memory devices 140A-H and 142A-H. EX1005, 7:31-61. The module 100, as illustrated by modules 100A-C in Fig. 8, can be attached to the prior art system's memory bus sockets 28A-C. The module 100, unlike the prior art module, includes Left and Right Interface Circuits 125 and 130 that interface between the system memory data bus 22, at one side, and corresponding memory devices in ranks 140 and 142, on the other side. The interface circuits 125 and 130 are controlled by the Module Controller 110 through control signals (here, labeled 'SYNC'). EX1003 ¶85.

Each of the interface circuits 125 and 130 can be implemented as a circuit which is almost identical to the data interface circuit 120 of Halbert's FIG. 4 (reproduced below with annotations) except that the number of data signal lines is

split in half, i.e., interface circuit 120 has 'm' DQ lines connecting to the data bus, and each of the Left and Right Interface Circuits 125 and 130 has only half of those data signal lines, 'm/2'. EX1005, 7:37-40; EX1003 ¶86.

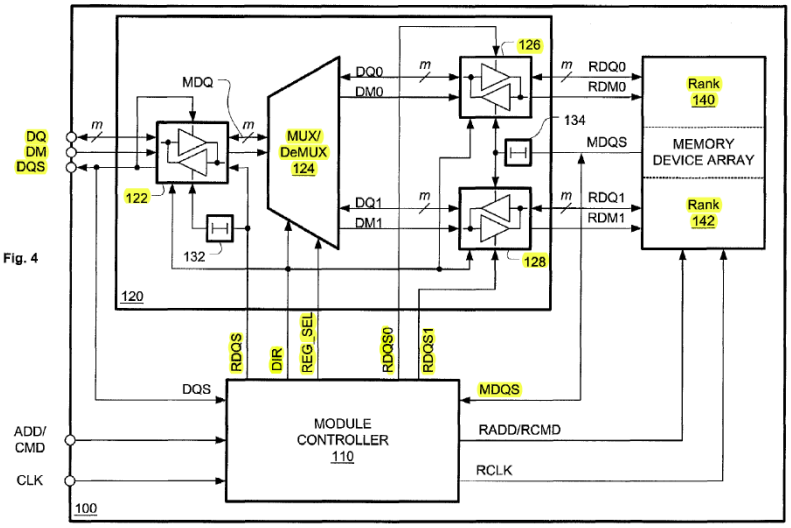


Fig. 4

On the memory data bus side, the interface circuit 120 has a bi-directional buffer 122 that receives and drives data signals DQ on the system memory data bus. EX1005, 4:60-5:5. The bidirectional buffer 122 can also drive data strobe signals onto the memory data bus. *Id*. On the memory rank side, the interface circuit 120 has two bi-directional registers 126 and 128 to connect to the memory ranks 140 and 142, respectively. *Id*., 5:6-14. Signals are switched by a multiplexer/demultiplexer 124 between the buffer 122 and the registers 126 and 128. EX1003 ¶87.

The interface circuit 120 is controlled by the module controller 110 using signals such as DIR, REG_SEL, RDQS0 and RDQS1. EX1005, 5:23-65. "For

instance, direction signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." *Id*., 5:25-28. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ0 [from Rank 140] or DQ1 [from 142] will be supplied to buffer 122[] . . . [which] drives that data onto the memory data bus." *Id*., 5:40-50. "In the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle . . . . When RDQS0 transitions, register 126 latches data from DQ0 (and DM0) [and w]hen RDQS1 transitions, register 128 latches data from DQ1 (and DM1)." *Id*., 5:51-58; EX1003 ¶88.

Halbert also discloses alternative implementations. For example, in the TO mode, DQ can be supplied to both registers 126 and 128, instead of using the DeMUX 124 to select which of those registers receives that data. EX1005, 5:53-54. Further, "[a]lthough bi-directional registers/buffers and a combination multiplexer/demultiplexer are illustrated, those skilled in the art recognize that an embodiment of the invention can also be constructed using two data paths with unidirectional components." *Id*., 9:30-35. Also, "although the illustrated embodiments use one or two interface circuits and a separate module controller, all of these devices could be integrated in a single device, or in some other number of packages with some other division of the tasks to be performed by the module." *Id*., 10:2-6. EX1003 ¶89.

Halbert's modules "can improve on the dual-bank registered DIMM in several respects. For instance, . . . a DIMM . . . can, with the same type of devices, number of devices, and data signal pins as the dual-bank registered DIMM, provide twice the data rate of the registered DIMM. This configuration can also allow the memory devices to operate at voltage levels independent of the voltage levels of the memory system that the module is attached to. The exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus. Further, the memory devices of the embodiments avoid arrangements of competing memory banks that load each other, as is the case with a dual-bank DIMM." EX1005, 3:59-4:5; EX1003 ¶90.

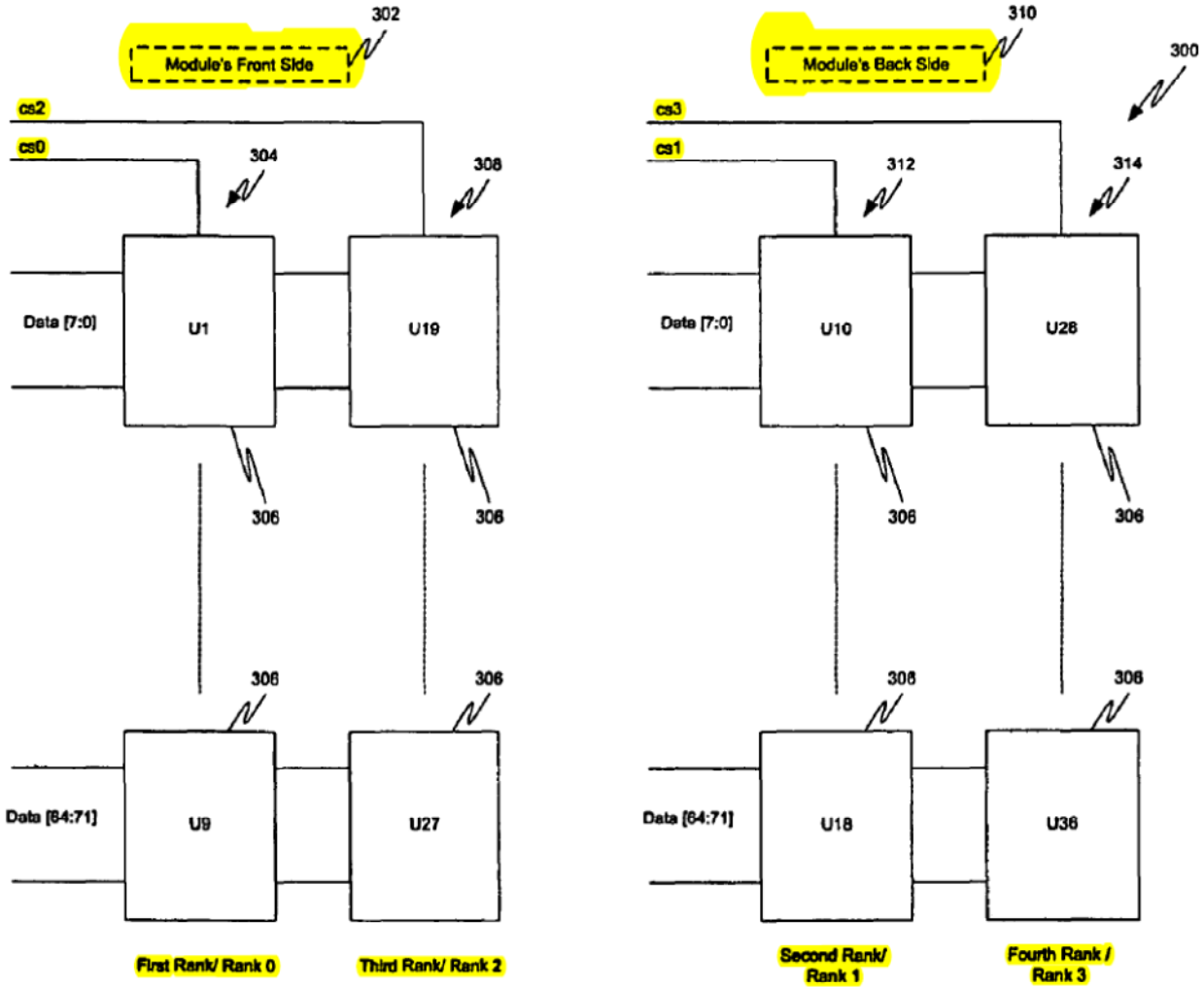
B. U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. (EX1019)

U.S. Patent Appliation Publication No. 2006/0117152 to Amidi et al. ("Amidi"; EX1019) was filed on January 5, 2004 and published on June 1, 2006. Therefore, Amidi is prior art to the '185 Patent under §§ 102 (a), (b) and (e).

Amidi explains that prior-art memory modules had one or two ranks of memory devices and were configured to be attached to sockets on the computer's main board. EX1019, ¶¶[0002-0007]. "Common system implementations . . . have typically two memory chip selects routed per socket." *Id.*, ¶[0003]. "The system chip select signals control individual memory modules ranks." *Id.*

Amidi teaches that "[b]ecause memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices. However, in order to achieve a [higher] density . . . the memory module needs four ranks." EX1019, ¶[0008]. "A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed." *Id.*, ¶[0011].

Amidi is directed to such a four rank memory module. EX1019, ¶[0001]. Each rank of Amidi's memory module has a corresponding chip select signal as shown in Amidi's FIG. 3 (reproduced below with annotations, showing four ranks of memory devices, each receiving a respective chip select signal cs0, cs2, cs1, and cs3).



Transparent Four Rank DDR Module Block Diagram
FIG. 3

Amidi's memory module also includes a "[Complex Programmable Logic Device] CPLD 410 [which] emulates a two rank memory module on the four rank memory module 400. CPLD 410 allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module . . . . The CPLD 410 determines which rank from the four ranks to activate based upon the address and command signals from a memory controller coupled to the memory module 410." EX1019, ¶[0041], FIG. 4. In particular, Amidi's CPLD

"ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank memory modules." *Id.*, ¶52.

In particular, Amidi's CPLD determines which rank is active based on the first and second chip select signals CS0 and CS1, and the highest address number, as depicted in the table of FIG. 5 (below). *Id.*, FIG. 5, ¶[0043].

Add(n)	CS1	CS0	Active Bank
0	1	0	0
0	0	1	1
1	1	0	2
1	0	1	3

C. Microcomputer Interfacing by H. Stone (EX1013)

Microcomputer Interfacing ("Stone") is a book authored by Dr. Harold Stone and published in 1982. EX1013 at Cover-3. Stone is prior art to the '185 Patent under §§ 102(a) and (b). Stone describes, among other things, various techniques and issues related to interfacing different components of a computer system. Chapter 4 of Stone is specifically directed to such issues as they relate to accessing computer memories, including the use of bidirectional buffers. EX1013, p.133, FIG. 4.7.

D. U.S. Patent No. 6,070,217 to Connolly et al. (EX1016)

U.S. Patent No. 6,070,217 to Connolly et al. ("Connolly") issued on May 30, 2000 from an application filed May 12, 1998. Therefore, Connolly is prior art to the '185 Patent under §§ 102(a), (b) and (e).

Connolly describes a direct inline memory module residing on a printed circuit board. EX1016, Abstract, FIGS . 6A-6C. The DIMM module includes interface circuits such as FETs mounted at spaced locations across the board, as shown below in FIG. 6A:

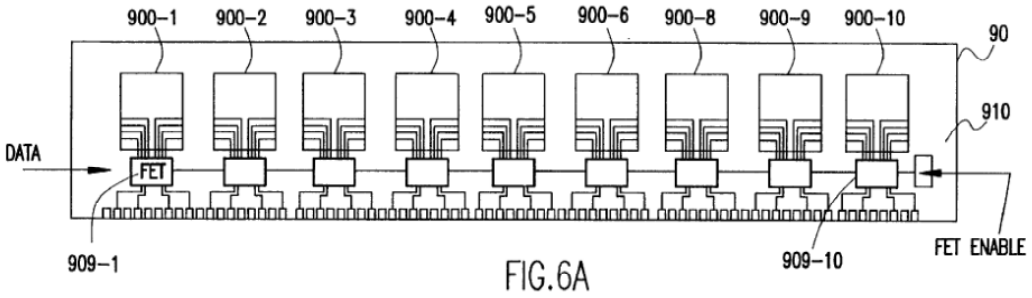


FIG.6A

Id., 5:5-13, FIG. 6A.

E. JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79, June 2000. (EX1007)

JEDEC Standard JESD79 ("JESD79") is an Electronic Industries Alliance (EIA) publication of an industry standard for DDR SDRAMs dated June 2000. EX1007 at Cover. JESD79 was published in June 2000, EX1010, ¶3, making it prior art to the '185 Patent pursuant to 35 U.S.C. §§ 102 (a) and (b).

JESD79 defines the minimum set of requirements for JEDEC-compliant Double Data Rate (DDR) Synchronous DRAMs (SDRAMs) having four banks of

DRAM memory, including requirements for the CAS Latency. EX1007 at i, 1; EX1003 ¶102. JESD79 explains that the DDR SDRAMs must be initialized by setting a mode register using a mode register set command to control the CAS latency of the memory. EX1007, 8, 14, FIG. 1; EX1003 ¶103.

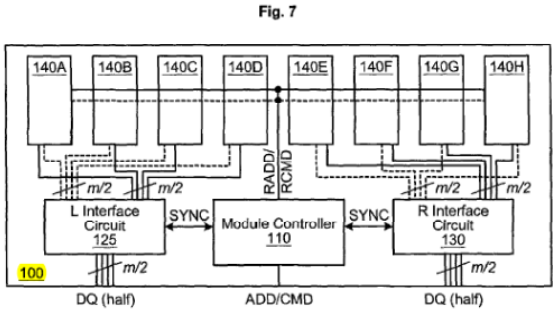
V. Precise Reasons for Relief Requested

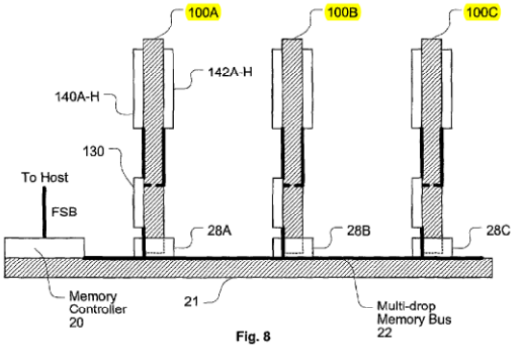
A. Halbert Anticipates Claims 1-3, 7, 8, 10-12

1. Claim 1 is Anticipated

a) Preamble

The preamble of claim 1 requires *"[a] memory module.*" EX1001, 18:36 (emphasis added). Halbert discloses several exemplary implementations of memory modules, such as Dual In-line Memory Modules (DIMM), that are configured to be coupled to a memory controller. *See, e.g.*, EX1005, FIGS. 1, 2, 4, 7, 8, 10-13, 1:31-42, 2:3-14; EX1003 ¶¶105-107. Halbert's FIG. 7, for example, "shows the general component arrangement for a memory module 100 in a DIMM form factor. Two ranks of memory devices are arranged along the top of the DIMM card: memory devices 140A–140H are arranged on the facing side of the module, with memory devices 142A–142H arranged directly behind these (see the side view of module 100A in FIG. 8)." EX1005, 7:31-37; *see also id*. at FIGS. 7-8 (reproduced below with annotations highlighting memory module 100, 100A, 100B, 100C).





EX1003 ¶108. Thus, Halbert discloses a "*memory module*."

b) Memory Devices

Claim 1 requires that the memory module includes "*a plurality of memory devices.*" EX1001, 18:37 (emphasis added). Halbert's FIG. 7 includes two ranks of memory devices. EX1005, 7:31-37, FIGS. 7, 8; EX1003 ¶111. Thus, Halbert discloses a "*plurality of memory devices.*"

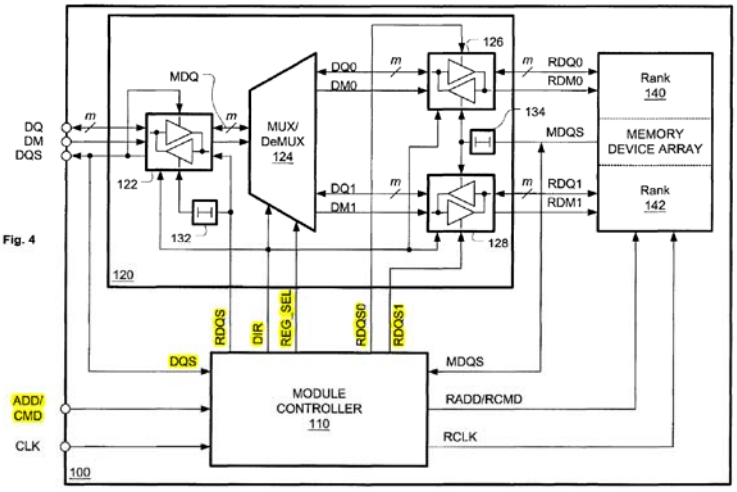
c) Controller

Claim 1 requires that the memory module include "*a controller configured to receive control information from a system memory controller and to produce module control signals.*" EX1001, 18:38-40 (emphasis added).

Halbert discloses a Module Controller 110 ("*a controller*"), in both FIGS. 4 and 7. *See, e.g.*, EX1005, 3:11-13. Halbert explains that the controller 110 is "*configured to receive control information*," such as control signals on the ADD/CMD input control signal lines, from a "primary memory controller" ("*a system memory controller*"), (*see* EX1005, 5:28-30, 6:1-4, 6:66-7:2, 8:33-35, Figs.

8 (Memory Controller 20), 11 (Memory Controller 200),) and to produce a number of control signals, collectively designated "SYNC." *See, e.g.*, EX1005, FIG. 7; EX1003 ¶114.

Halbert explains that the "SYNC" signals include the control signals RDQS, DIR, REG_SEL, RDQS0, and RDQS1 shown in FIG. 4, annotated below:



EX1005, 7:51-53, FIG. 7. Such signals are "*module control signals*" because they are used to control the memory module. EX1003 ¶114. Indeed, Halbert describes how those signals are used to control the operation of Halbert's system in both a "TO" mode (a write to the memory devices) and an "AWAY" mode (a read from the memory devices). EX1005, 4:40-48, 5:23-65; EX1003 ¶83, 115. Halbert also discloses that the "*control information from a system memory controller*" can include memory commands related to read operations (*see, e.g.,* ACTIVE and

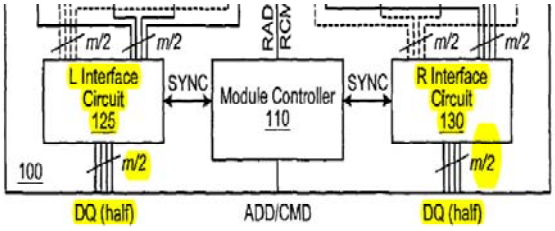
READ commands in FIG. 5) and write operations (*see, e.g.*, ACTIVE and WRITE commands in FIG. 6). *See* EX1005, 5:66-7:30; EX1003 ¶116.

Thus, Halbert discloses this element.

d) Plurality of Circuits

Claim 1 also requires that that the memory module includes "*a plurality of circuits configured to receive the module control signals, each circuit of the plurality of circuits having a first bit width and operatively coupled to at least two corresponding memory devices of the plurality of memory devices, the at least two corresponding memory devices each having a second bit width smaller than the first bit width.*" EX1001, 18:41-47.

Halbert discloses that, in the embodiment of FIG. 7, "[i]nterface circuit 120 of FIG. 4 is split into two identical interface circuits (left circuit 125 and right circuit 130) in FIG. 7, each handling half of the data lines." EX1005, 7:37-40. In particular, the "[d]ata interface circuit 120 [of FIG. 4] provides for m-bit-wide data transfers between the module and the system memory data bus," *id.*, 4:49-51, and each of the left and right circuits 125 and 130 provides for m/2 bit transfers as shown in FIG. 7. *Compare* bit width of DQ lines in EX1006, FIG. 7 *with* FIG. 4 (partially reproduced below with annotations showing the corresponding DQ lines and their bit widths).



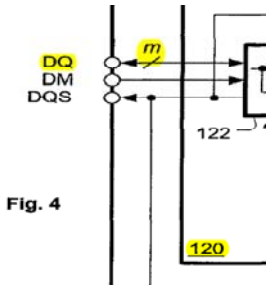


Fig. 4

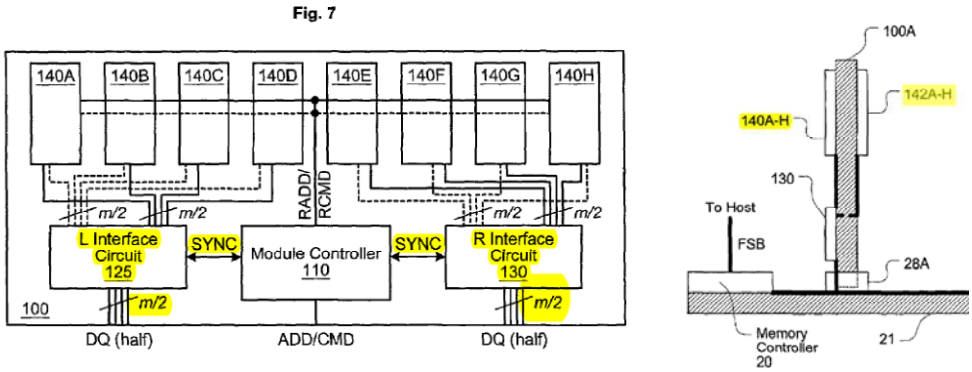
EX1003 ¶119.

A skilled artisan would understand this disclosure to mean that each of the L Interface Circuit 125 and R Interface Circuit 130 ("*a plurality of circuits*") have the same structure and functionality as interface circuit 120 of FIG. 4, but are each coupled to only half the relevant data signal lines as depicted in FIG. 7. *See, e.g.*, EX1005, 7:51-53 (explaining that the interface circuits 125 and 130 receive the same signals from controller 110 in FIG. 7 as the interface circuit 120 in FIG. 4); *see also id.* ("The signals labeled 'SYNC' include the signals DQS, RDQS, DIR, REG_SEL, RDQS0, and RDQS1 shown in FIG. 4."); EX1003 ¶120.

Halbert further discloses that L Interface Circuit 125 and R Interface Circuit 130 each receive the module control signals included in the "SYNC" signal in FIG. 7. EX1005, 7:51-53. Halbert therefore discloses "*a plurality of circuits to receive the module control signals.*" EX1003 ¶123.

Halbert also discloses that each of the L and R Interface Circuits 125 and 130 has a bit width of m/2 ("*a first bit width*") and is operatively coupled to first and second memory ranks 140 and 142, each rank consisting of multiple memory

devices. *See, e.g.*, EX1005, FIG. 7 (reproduced below with annotations highlighting the L and R Interface Circuits 125 and 130 and their bit width, and module control signals SYNC); *see also id.* FIG. 8 (reproduced below in part with annotations highlighting the first 140A-H and second 142A-H memory ranks).



EX1003 ¶124.

For example, Halbert explains that "FIG. 7 shows the general component arrangement for a memory module 100 in a DIMM form factor. Two ranks of memory devices are arranged along the top of the DIMM card: memory devices 140A–140H are arranged on the facing side of the module, with memory devices 142A–142H arranged directly behind these (see the side view of module 100A in FIG. 8). Interface circuit 120 of FIG. 4 is split into two identical interface circuits (left circuit 125 and right circuit 130) in FIG. 7, each handling half of the data lines. This arrangement allows for more uniform lead lengths between an interface circuit and each of the memory devices, and reduces the pin count on each interface circuit package. In FIG. 7, the data signal lines for one memory rank are

arranged on the front side of the card (solid lines leading to the memory devices), and the data signal lines for the other memory rank are arranged on the back side of the card (dashed lines leading to the memory devices)." EX1005, 7:31-47; EX1003 ¶125.

Thus, Halbert discloses that each interface circuit 125 and 130 is operatively coupled to four memory devices of a first rank (*e.g.*, L interface circuit 125 is operatively coupled to memory devices 140A-D while R interface circuit 130 is operatively coupled to memory devices 140E-H, indicated by solid lines on Figure 7) and also to four memory devices of a second rank (*e.g.*, L interface circuit 125 is operatively coupled to memory devices 142A-D while R interface circuit 130 operatively coupled to memory devices 142E-H, indicated by dashed lines on Figure 7). Halbert therefore discloses "*each circuit of the plurality of circuits having a first bit width and operatively coupled to at least two corresponding memory devices of the plurality of memory devices.*" EX1003 ¶126.

Halbert also discloses that the bit width of each memory device is less than the bit width m/2 of the Interface circuits. In particular, Halbert discloses that the "data lines DQ of the memory device banks each connect to the memory bus of the host system. A total of nB DQ lines carry data signals, where B is the number of devices in one bank (e.g., eight or nine), and n is the data width of each device (e.g., four, eight, or sixteen bits)." EX1005, 2:37-42. Since FIG. 7 shows that

each interface circuit receives data from four memory devices (B=4) in each bank, thus the bit width 'n' of each memory device is (m/2)/B = m/8, which is less than m/2, the bit width of the interface circuit. Halbert therefore discloses "*the at least two corresponding memory devices each having a second bit width smaller than the first bit width.*" EX1003 ¶127.

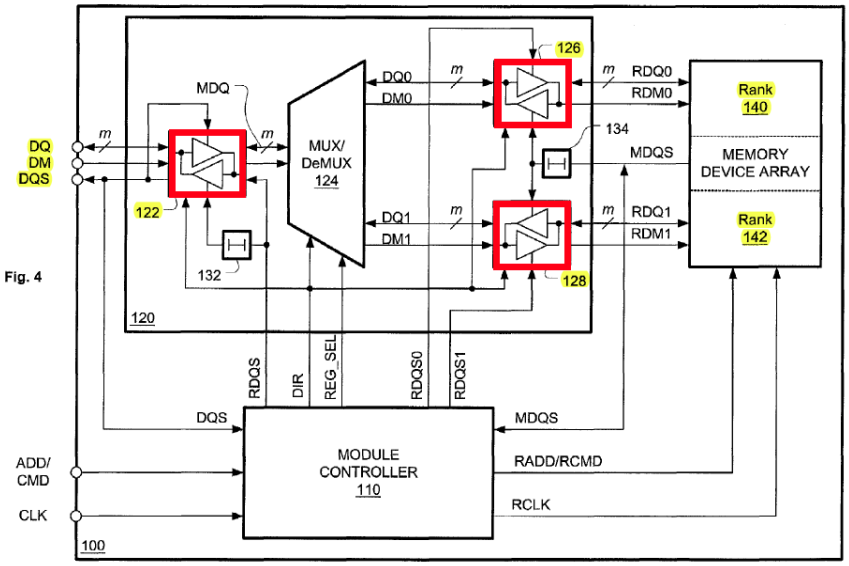
Thus, Halbert discloses this claim element.

e) Write and Read Buffers

Claim 1 further requires "*each circuit of the plurality of circuits comprising at least one write buffer and at least one read buffer.*" EX1001, 18:47-49.

Halbert discloses that each interface circuit 125 and 130 includes a bi-directional buffer 122, and bi-directional registers 126 and 128. EX1005, 4:60-5:14, 7:37-47, FIGS. 4, 7; EX1003 ¶¶120-121. A skilled artisan would understand Halbert to disclose that each of the bi-directional buffer 122 and registers 126 and 128 includes a buffer to drive write data into the memory ("*write buffer*") and another buffer to drive read data from the memory ("*read buffer*"). *See* EX1005, FIG. 4 (reproduced below with annotations around the buffer 122 and registers 126

and 128).



EX1003 ¶130.

In particular, the symbols used by Halbert to represent the buffer 122 and registers 126 and 128 would be understood by a skilled artisan to represent bidirectional tri-state buffers, each comprising a tri-state buffer for write operations (triangle pointing towards the memory device array) and another tri-state buffer for read operations (triangle pointing away from the memory device array). *See, e.g.*, EX1014, 5:61-6:4, FIG. 3; EX1015, 5:55-7:6, FIGS. 4-6; EX1003 ¶131; *see also* EX1013, 74, 133, FIGS. 2.28, 4.7 (reproduced below with annotations):

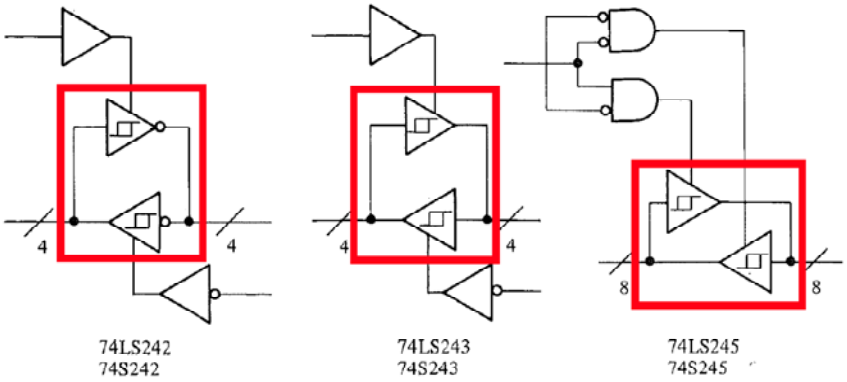


FIGURE 2.28 Drivers and receivers (continued on next page).

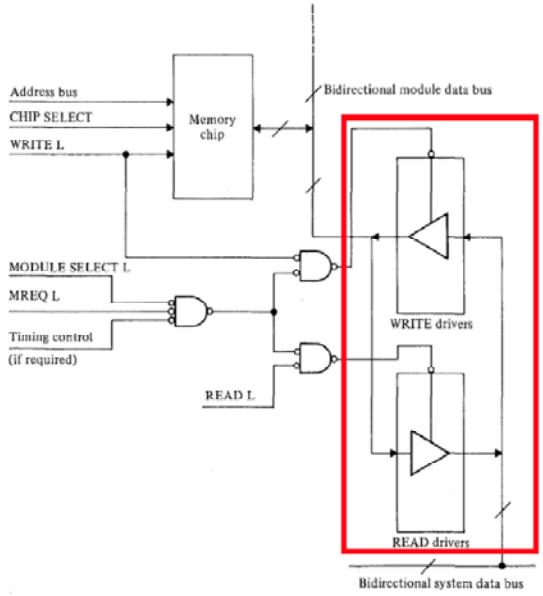


FIGURE 4.7 Tri-state driver control for interfacing memory chips to bidirectional data lines.

EX1003 ¶132. Such buffers were well known in the prior art and well understood. EX1009; U.S. Patent No. 7,191,302 (EX1014) at FIG. 3 (showing bi-directional buffer 7 including IN and OUT buffers 7a and 7b) and U.S. Patent No. 6,704,910 (EX1015) at FIG. 4 (showing bidirectional buffer 24 having separate buffers for the in and out directions). EX1003 ¶¶133-134.

Thus, Halbert discloses that "*each circuit of the plurality of circuits compris[es] at least one write buffer and at least one read buffer.*"

In addition, Halbert discloses that "[a]lthough bi-directional registers/buffers and a combination multiplexer/demultiplexer are illustrated, those skilled in the art recognize that an embodiment of the invention can also be constructed using two data paths with unidirectional components." EX1005, 9:30-35. A skilled artisan would have understood that an embodiment "using two data paths with unidirectional components" would include "*at least one write buffer*" (to write data into the memory devices) and "*at least one read buffer*" (to read data from the memory devices). *See, e.g.,* EX1009, 2; EX1013, 74, 129; EX1003 ¶¶132-133, 136-137.

Thus, Halbert discloses this element.

f) Selectively Allow Data Transmission

Claim 1 further requires "*[each circuit of the plurality of circuits] configured to selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices in response to the module control signals.*" EX1001, 18:49-53.

Halbert's interface circuits 125 and 130 selectively allow data transmission between the memory devices in respective ranks 140 and 142 and the system

memory controller via memory bus lines, such as DQ. EX1005, 5:6-65, 7:37-40, FIGS.4, 7. Specifically, Halbert discloses a data path through a buffer 122, MUX 124 and registers 126 and 128, all controlled by "*module control signals*," such as RDQS, DIR, REG_SEL, RDQS0 and RDQS1. EX1005, 4:60-5: 65, FIG. 4, 7, 8; EX1003 ¶148-149.

Halbert further discloses that in the TO mode (*i.e.*, a write to memory), "*In one memory bus clock cycle, m bits are directed to register 126 by strobing RDQS0. In the following bus clock cycle, m bits are directed to register 128 by strobing RDQS1.* Both register contents are then written to memory device array 140/142 during a single device write cycle." EX1005, 5:51-65 (emphasis added); EX1003 ¶150. Thus, in the TO mode of Halbert, and in response to the "*module control signals*," those memory devices associated with register 126 (i.e. Rank 140) receive data transmission from the system memory controller in the first clock cycle, but not in the second clock cycle. Similarly, in the TO mode and responsive to the "*module control signals*," those memory devices associated with register 128 (i.e., Rank 142) receive data transmissions from the system memory controller in the second clock cycle, but not in the first clock cycle. This circuitry and signaling therefore selectively allows information to pass between the system memory controller and one set of memory devices, or between the controller and the other set of memory devices, in a given clock cycle. EX1003 ¶151.

Halbert also discloses the operation of his interface circuits in what he calls "the AWAY mode" (i.e., a read from memory). EX1005, FIG. 5 and 6:1-19. Halbert discloses that in the AWAY mode the communication of data from the memory devices is selective in that data from those memory devices associated with register 126 are communicated through the interface circuit and over the memory bus during one clock cycle and data from those memory devices associated with register 128 are communicated through the interface circuit and over the memory bus during the next clock cycle. EX1005, 5:45-47 ("For instance, REG_SEL can first select, e.g., DQ0 during a first bus clock cycle, and then DQ1 during the following bus clock cycle."); EX1003 ¶152.

Halbert therefore discloses this element.

g) Selectively Isolate Another Memory Device

Claim 1 further requires "*[each circuit of the plurality of circuits] configured . . . to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller in response to the module control signals.*" EX1001, 18:49-56.

As discussed above, the broadest reasonable construction of the term "*selectively isolate at least one other memory device . . . from the system memory controller*" is selectively electrically separating another memory device from the system controller.

As demonstrated immediately above, Halbert discloses that for a "TO mode" memory operation, for example, the memory devices in Rank 142 will not receive data communications and therefore are isolated from the primary memory controller (the claimed "system memory controller") during the first cycle of the operation while the associated memory device in Rank 140 receives data from the primary memory controller. Similarly, the memory devices in Rank 140 will not receive data communications and therefore are isolated from the primary memory controller during the second cycle while the associated memory device in Rank 142 receives data. A similar selective isolation happens in Halbert's "AWAY mode" as well. EX1005, 5:40-65; EX1003 ¶150-152, 156.

Thus, Halbert discloses circuitry and control signaling that selectively permits the communication of data between the system memory controller and one set of memory devices, or between the controller and the other set of memory devices, in a given clock cycle. The set of memory devices not permitted to receive data during a particular clock cycle is electrically separated from the system memory controller during that clock cycle because it is not permitted to exchange data with the controller during that time period. The isolation is selective because it isolates different memory devices in different clock cycles – in the first clock cycle one set of memory devices is isolated; in the second clock cycle the other set of memory devices is isolated. Moreover, as demonstrated

above, this selective isolation is implemented "*in response to the module control signals.*" *See, e.g.*, EX1005, 5:23-65; *see also* EX1003 ¶¶ 148-151, 157.

Halbert therefore discloses this element.

h) Drive Write Data

Claim 1 further requires "*wherein each circuit of the plurality of circuits is operable, in response to the module control signals, to actively drive write data from the system memory controller to the at least one selected memory device of the at least two corresponding memory devices through the at least one write buffer.*" EX1001, 18:56-61.

As demonstrated above, Halbert discloses that the interface circuits 125 and 130 each include at least one write buffer as illustrated in FIG. 4 for each of buffer 122 and registers 126 and 128. *Supra* §V.A.1.e). Furthermore, Halbert discloses an alternative embodiment that uses a unidirectional read buffer and a unidirectional write buffer in place of each bidirectional buffer 122, 126 and 128 (*supra* and EX1005, 9:20-35). A skilled artisan would have understood that the write buffer in 122 is used to actively drive write data from the system memory controller through the write buffers of 126 and 128 to their associated memory devices. EX1005 5:23-65; EX1003 ¶181. Also as demonstrated above, in the "TO mode" interface circuits 125 and 130 actively drive write data from the system

memory controller to a selected memory device in response to the module control signals. *See, e.g.*, EX1005, 5:30-65, FIG. 4; EX1003 ¶182.

Halbert therefore discloses this element.

i) Drive Read Data

Claim 1 further requires "*[wherein each circuit of the plurality of circuits is operable, in response to the module control signals] to receive and drive read data from the at least one selected memory device of the at least two corresponding memory devices to the system memory controller through the at least one read buffer.*" EX1001, 18:62-65.

As demonstrated above, Halbert discloses that the interface circuits 125 and 130 each include at least one read buffer as illustrated in FIG. 4 for each of buffer 122 and registers 126 and 128. *Supra* §V.A.1.e). Furthermore, Halbert discloses an alternative embodiment that uses a unidirectional read buffer and a unidirectional write buffer in place of each bidirectional buffer 122, 126 and 128 (*see above* and EX1005, 9:20-35). A skilled artisan would understand the read buffer in 126 and 128 is used to receive and drive read data from their associated memory devices to the system controller through the read buffer of 122. As demonstrated above, in the "AWAY mode" interface circuits 125 and 130 read data from memory devices and send them to the system memory controller through the read buffer in response to module control signals. *See, e.g.*, EX1005, 5:30-65;

FIG. 4. Fig. 5 shows the timing of an exemplary "AWAY" operation (the claimed "read" operation) in which data to be read, 'a1' and 'a2', are received from memory ranks 140 and 142 on buses RDQ0 and RDQ1 at clocks T7n and T8, and delivered through the read buffer portions of registers126 and 128 to the memory bus MDQ at clocks T8 and T8n. The memory bus MDQ is coupled to the memory controller through the read buffer of driver 122. EX1003 ¶186.

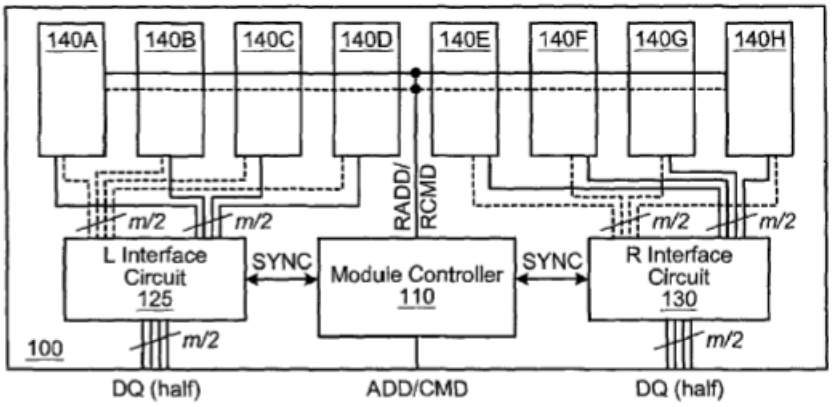
Halbert therefore discloses this element.

j) Distribution of the Circuits

Claim 1 further requires "*wherein the circuits of the plurality of circuits are distributed at corresponding positions separate from one another.*" EX1001, 18:65-67.

Halbert discloses, in the embodiment of FIG. 7, that the interface circuits 125 and 130 are distributed at positions separate from one another, *e.g.*, on opposite (left and right) sides of memory controller 110. *See, e.g.,* EX1005, FIG. 7 (reproduced below); EX1003 ¶190.

Fig. 7



Halbert therefore discloses this element.

2. Claim 2 is Anticipated

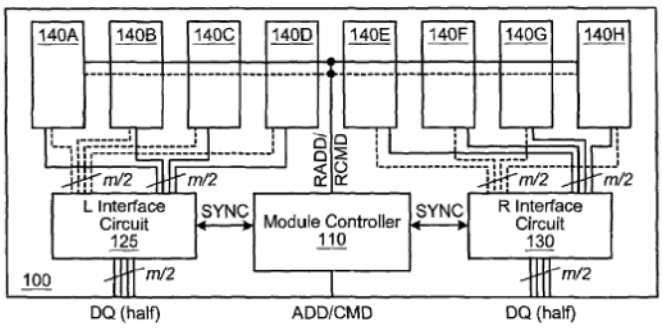
Claim 2 requires "*[t]he memory module of claim 1, wherein the plurality of circuits is contained in a plurality of packages at locations spaced from one another.*" EX1001, 19:1-3.

Halbert discloses that "FIGS. 7 and 8 show, respectively, a side view for a general DIMM module *layout for the memory module* of FIG. 4, and a side edge view of multiple DIMM modules of this type connected to a multi-drop memory bus." EX1005, 3:11-14 (emphasis added). Halbert further discloses that in the embodiment of Figure 7 "[i]nterface circuit 120 of FIG. 4 is split into two identical interface circuits (left circuit 125 and right circuit 130) in FIG. 7, each handling half of the data lines. This *arrangement allows for more uniform lead lengths between an interface circuit and each of the memory devices*, and reduces the pin count on each ***interface circuit package***. … Module controller 110 is centered

below the memory modules, equalizing signal *distance to interface circuits 125 and 130*." EX1005 7:37-49 (emphases added). A skilled artisan would therefore understand those figures to depict the physical layout of the module in which each of the interface circuits 125 and 130 has a corresponding package ("interface circuit package") at the specific location as depicted in those figures. EX1003 ¶193.

Figures 7 and 8, moreover, depict interface circuits 125 and 130 as contained in separate packages at locations spaced from one another. *See, e.g.*, FIGS. 7-8 (reproduced below).

Fig. 7



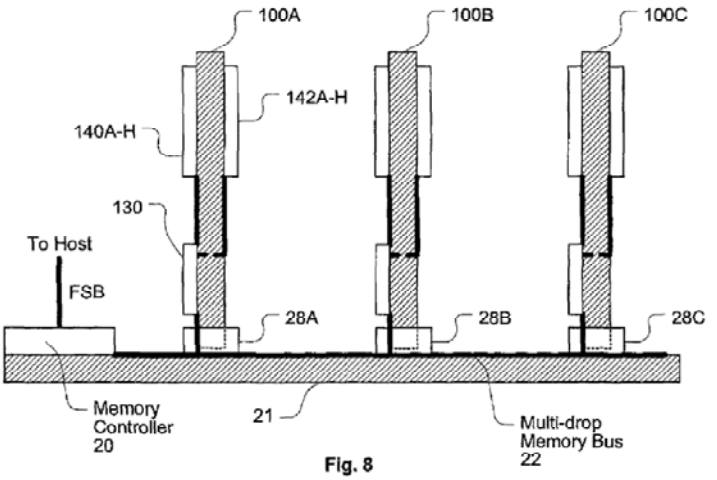


Fig. 8

EX1003 ¶194.

Halbert therefore discloses this element.

3. Claim 3 is Anticipated

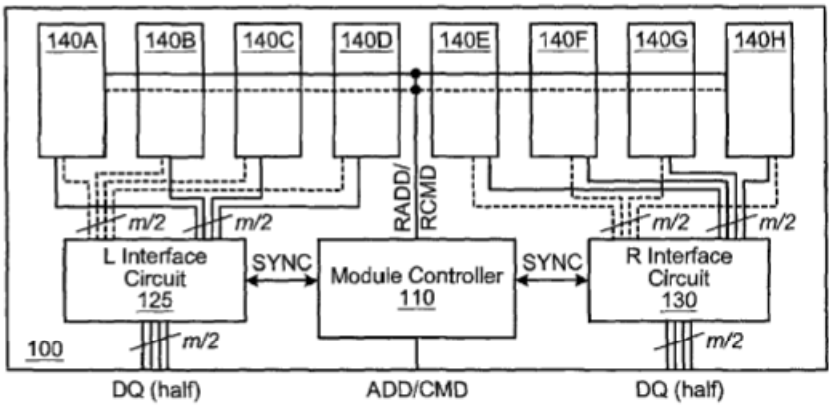
Claim 3 requires "*[t]he memory module of claim 2, wherein the plurality of memory devices, the controller, and the plurality of circuits are mechanically coupled to a printed circuit board having an edge, wherein the packages are positioned along the edge and between the edge and the plurality of memory devices.*" EX1001, 19:4-8.

Halbert discloses that the memory devices 140A-H and 142A-H, the controller 110, and the interface circuits 125 and 130 are mechanically coupled to a DIMM card circuit board, which a skilled artisan would understand to be "*a printed circuit board having an edge.*" *See, e.g.*, EX1005, 1:31-2:45, FIGS. 1, 2, 7. For example, Halbert expressly discloses that the "DIMM is a rectangular low-profile circuit board that has electrical contact points arranged on both sides along

one long edge." *Id*., 2:9-11. Skilled artisans also understood that a DIMM circuit board was a printed circuit board. EX1006, [0160]; EX1016, 3:4-10, FIG. 6A; EX1003 ¶197.

Halbert further discloses that the packages in which the interface circuits 125 and 130 are contained are positioned along the board's edge between the edge and the memory devices 140A-H. *See, e.g.*, EX1005, 3:11-14, 7:31-32, FIG. 7 (reproduced below).

Fig. 7



EX1003 ¶198.

Figure 8 (reproduced below with annotations), in particular, demonstrates that the positions of the module controller 110 and interface circuits 125 and 130 is between the edge of the card connecting to the memory bus (toward the bottom of the figure) and the memory devices 140 and 142 (toward the top of the figure) (EX1005):

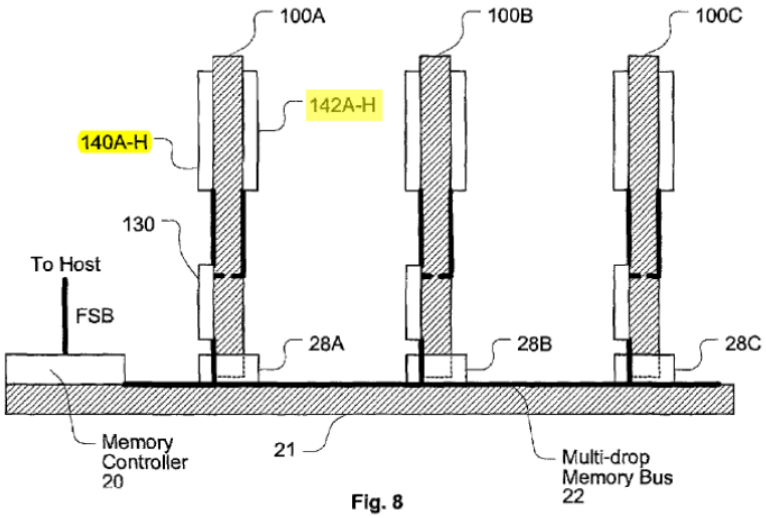


Fig. 8

EX1003 ¶¶199-200; *see also* EX1005, 7:31-53.

Thus, Halbert discloses that this claim element.

4. Claim 7 is Anticipated

Claim 7 requires "*[t]he memory module of claim 1, wherein the memory module is a dual in-line memory module.*" EX1001, 19:39-40.

Halbert discloses that the memory devices 140A-H and 142A-H, the controller 110, and the interface circuits 125 and 130 are implemented as a dual in-line memory module. *See* EX1005, 1:31-2:45, FIGS. 1, 2, 7, 8; EX1003 ¶207.

5. Claim 8 is Anticipated

Claim 8 requires "*[t]he memory module of claim 1, wherein the plurality of memory devices comprise one or more synchronous dynamic random access memory devices.*" EX1001, 19:41-43.

Halbert discloses that the "types, sizes, or numbers of memory devices selected for use with the present invention are not critical. Some possible device

types include dynamic random access memory (DRAM) devices, synchronous DRAM (SDRAM) devices including double-data-rate (DDR) SDRAM devices, quad-data-rate (QDR) SDRAM devices, Rambus™ DRAM devices (with an appropriate controller), static RAM and flash memory devices. It may be possible to combine memory modules in a memory system according to the invention where two modules incorporate different types of memory devices." EX1005 9:55-65; EX1003 ¶209.

Halbert therefore discloses this element.

6. Claim 10 is Anticipated

Claim 10 requires "*[t]he memory module of claim 1, wherein the controller is configured to control the plurality of circuits using a Column Access Strobe (CAS) latency parameter*." EX1001, 19:53-55.

Halbert discloses that a prior art memory module, such as a registered DIMM 24, places data onto bus lines DQ "[a]fter a ***known*** CAS (column address strobe) latency." EX1005, 2:55-56 (emphasis added); *see also id.*, FIG. 3 (showing a CAS latency of 4 between receiving an address for a read operation and placing the corresponding data onto the bus lines); EX1003 ¶212. Halbert also discloses that its "primary memory controller" interfaces with the interface circuits of FIGS. 4 and 7 for read and write operations, and "initiates READ operations *just like it would for a registered DIMM (see the description accompanying FIG. 3)*."

EX1005, 6:2-4 (emphasis added). Thus, Halbert's interface circuits necessarily provide data to the system memory bus consistent with how the prior art DIMM of Figure 3 would do so, including by implementing the CAS latency of that DIMM, such as by placing data onto bus lines DQ "[a]fter a known CAS (column address strobe) latency." *Id.*, 2:55-56; EX1003 ¶213.

Halbert therefore discloses this element.

7. Claim 11 is Anticipated

Claim 11 requires "*[t]he memory module of claim 1, wherein the module control signals include first indication of a direction of data flow and second indication of whether a first group of the plurality of memory devices or a second group of the plurality of memory devices are being accessed.*" EX1001, 19:55-59.

Halbert discloses that the module control signals include a DIR signal which provides an "*indication of a direction of data flow*." EX1005, 5:23-39, FIG. 4; EX1003 ¶231. Halbert also discloses that the module control signals include REG_SEL, RDQS0 and RDQS1 signals which provide an "*indication of whether a first group of the plurality of memory devices or a second group of the plurality of memory devices are being accessed.*" In particular, the REG_SEL, RDQS0 and RDQS1 signals indicate whether the first or second ranks 140 or 142 are being accessed. EX1005, 5:40-65; EX1003 ¶¶232, 234-235.

Halbert therefore discloses this element.

8. Claim 12 is Anticipated

Claim 12 requires "*[t]he memory module of claim 1, further comprising module control signal lines extending across a substantial portion of the memory module, wherein the controller transmits the module control signals over the module control signal lines, and wherein the plurality of circuits are distributed along the module control signal lines and receive the module control signals via the module control signal lines*." EX1001, 19:60-20:2.

Halbert discloses that the SYNC signal lines ("*module control signal lines*") extend from the controller 110 to the interface circuits 125 and 130. EX1005, 7:31-53, FIG. 7; EX1003 ¶¶242-243. In the context of FIG. 7, a skilled artisan would conclude that the SYNC signal lines extend across a "*substantial portion*" of the memory module because they extend into both halves of the module and therefore towards interface circuits associated with memory devices located across the entire longest axis of the module. EX1003 ¶244.

Halbert further discloses that the module controller 110 transmits the SYNC signals over the SYNC lines to the interface circuits ("*wherein the controller transmits the module control signals over the module control signal lines, and wherein the plurality of circuits . . . receive the module control signals via the module control signal lines*"). EX1005, 7:40-53; EX1003 ¶245. Moreover, in the embodiment of FIG. 7 the interface circuits 125 and 130 are located along the same

horizontal axis as the SYNC lines, albeit in two different directions, "*distributed along the module control signal lines.*" EX1005, FIG. 7; EX1003 ¶245. Thus, Halbert discloses this claim.

B. Halbert Renders Claims 1-3, 7, 8, 10-12 Obvious

1. Claim 1

a) Plurality of Circuits

To the extent one might argue that Halbert does not disclose that interface circuits 125 and 130 have the same structure and functionality as Halbert's interface circuit 120, it would have been obvious to include the structure and functionality of circuit 120 in the circuits 125 and 130. It would have been common sense to do so since circuit 120 is readily available from and closely related to the disclosed circuits 125 and 130 of Halbert. Moreover, such inclusion would be merely the use of known prior art structures in their known ways to achieve predictable results. EX1003 ¶121.

A skilled artisan would have been motivated to use the same structure and functionality because she would assume that the related circuits of Halbert would likely work well together and because Halbert expressly notes that many variations of his disclosed circuits are possible. EX1005, 9:20-35; 2:39-46; EX1003 ¶122. Using the structure and functionality of circuit 120 in the circuits 25 and 130 would therefore have been obvious.

b) Write and Read Buffers

To the extent one might argue that Halbert does not disclose the claimed read and write buffers of claim 1, or the claimed "driving" functionality, it would have been obvious to include those elements in the system of Halbert.

Halbert expressly suggests such an implementation by the symbols representing the buffer 122 and registers 124 and 126, and its express disclosure of alternate embodiments that use unidirectional components. One skilled in the art would have been further motivated to use separate read and write buffers because they were well known at the time for driving bi-directional buses, such as memory data buses, and were recognized to provide predictable results. EX1003 ¶¶ 139-141.

Further, since in the system of Halbert data must travel in both direction (i.e., a read and a write) across the same busses, there was only a limited number of possible ways to provide such buffering, such as a bidirectional buffer or two unidirectional buffers. Thus, it would have been obvious to try a pair of unidirectional read and write buffers in place of Halbert's bidirectional buffers as expressly disclosed, e.g., by Exs. 1009 and 1013. *See, e.g.*, EX1013,133, FIG. 4.7; EX1003 ¶142. Moreover, the very purpose of using such buffers in the system of Halbert would be to receive and actively drive data in one direction or the other. EX1003 ¶¶184, 188.

Thus, Halbert renders obvious that "*each circuit of the plurality of circuits compris[es] at least one write buffer and at least one read buffer*" and also those claim elements requiring such buffers to "*actively drive write data*" or "*receive and drive read data.*" EX1003 ¶¶139-143, 184, 188.

2. Claim 10

To the extent one might argue Halbert does not disclose the requirements of claim 10, it would have been obvious to include that functionality in the system of Halbert. Halbert discloses a "primary memory controller" that interfaces with the memory modules of FIGS. 4 and 7 for read and write operations, and "initiates READ operations *just like it would for a registered DIMM (see the description accompanying FIG. 3)*," EX1005, 6:2-4 (emphasis added), and that such operation includes providing data to the DQ lines based on a CAS latency. A skilled artisan would therefore have been motivated to configure the module controller 110 "*to control the plurality of circuits using a Column Access Strobe (CAS) latency parameter*" in order to achieve proper operation of the system of Halbert. EX1003 ¶215.

Further, Halbert discloses embodiments that are "compatible with an existing memory controller/bus and with existing memory devices." EX1005, 3:55-57; *see also id*., 3:48-52; EX1003 ¶216. Skilled artisans at the time would have understood that this compatibility requirement meant that Halbert's modules

must be able to replace the prior art memory modules and would work in such a system. *Compare* EX1005 FIG. 1 *with* FIG. 8; EX1003 ¶217. Skilled artisans would also have understood that existing controller/bus configurations and memory devices used CAS latency parameters to set when the requested data would be available on the memory bus. *See, e.g.*, EX1007, 1; EX1003 ¶218; Thus, skilled artisans would have been motivated to use the known CAS latency parameter of the prior art system in order to be "transparent to the memory system" as taught by Halbert. EX1005, 3:49.

Accordingly, it would have been obvious to skilled artisans to configure the module controller 110 to synchronize the interface circuits of Halbert using the Column Access Strobe (CAS) latency parameter of the prior art as it was well known at the time. EX1005, 4:45-47; EX1003 ¶219.

3. Claim 11

To the extent one might argue that Halbert does not disclose the requirements of claim 11 because that claim requires accessing the first and second groups of memory devices at different times, it would have been obvious to include such functionality in the system of Halbert by using additional selection signals to activate one or the other memory ranks of Halbert alternately. For example, in its description of the prior art Halbert describes the use of chip selection signals with respect to FIG. 2. EX1005, 2:35-38. The use of such chip

selection signals with the ranks and existing control signals of Halbert's Figure 4 would allow activating the ranks alternately and thus accessing the ranks at different times. EX1003 ¶237.

It would have been obvious to employ such functionality in Halbert for several reasons because to do so would have been the use of known techniques (separate control signals per rank) for their known purpose (to access only a subset of available memory devices at one time) to achieve predictable results.

Further, a skilled artisan would have been motivated to include such prior art selection signals so that additional memory devices, or denser memory devices, could be added to the module and appropriately accessed using the existing address and data signal lines. *See, e.g.,* EX1019, ¶¶[0003]-[0011].

Furthermore, Halbert suggests such a use by disclosing that "[m]any other variations on the illustrated embodiments are possible. For instance, . . . [t]he illustrated examples also show two ranks of memory, but other numbers of ranks are also possible." EX1005 at 9:20-26. Skilled artisans at the time would have understood that, in case the number of ranks is increased, chip/bank select signals would need to be used to activate some but not all of the ranks. *See, e.g.*, EX1019, FIGS. 5, 6A-6B; EX1003 ¶238.

4. Claim 12

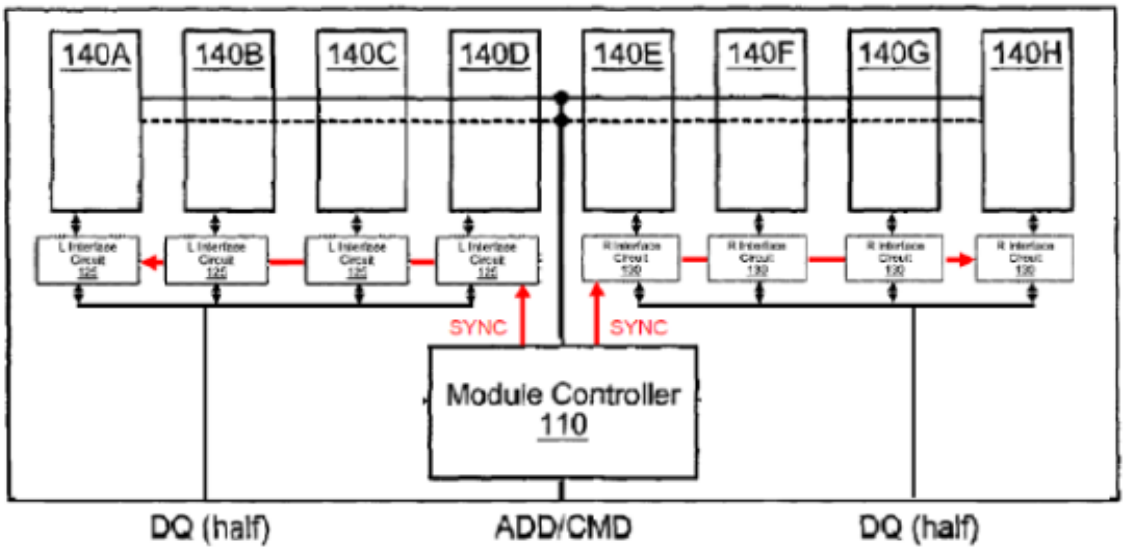
To the extent one might argue that Halbert does not disclose module control signal lines "*extending across a substantial portion of the memory module*" or "*the plurality of circuits [] distributed along the module control signal lines,*" it would have been obvious to include that configuration in the system of Halbert.

For example, Halbert discloses that the number of interface circuits in his system is not limited to one or two, but could instead be a larger number of such circuits. EX1005, 10:1-6; EX1003 ¶248.

Skilled artisans would have understood that other arrangements including more interface circuits, such as four or eight for example, could be advantageously used to implement larger bit widths for the data bus, and those circuits would necessarily be arranged along the edge of the board. EX1005, 7:31-53; EX1016, FIG. 6A; EX1003 ¶249.

Such an arrangement would extend the interface circuits, and therefore necessarily the SYNC signal lines which must be connected to such circuits, across all or nearly all of the horizontal width of the module ("*extending across a substantial portion of the memory module*"). Similarly, since the interface circuits in such an arrangement would have extended across the PCB between the lower edge and the memory devices, they would be "*distributed along the module control signal lines.*" Skilled artisans at the time would have understood such an

arrangement to look like Halbert's FIG. 7 (reproduced below with annotations with the SYNC lines (in red) extending to each interface circuit).



EX1003 ¶249.

Such an arrangement would have been obvious for several reasons. The arrangement of control circuitry and associated signal lines across all or nearly all of a PCB between memory devices and the lower side connection to the system memory bus was known in the prior art. EX1016, 5:14-24, FIG. 6A-B; EX1020, FIG. 5; EX1008, FIG. 6. The use of that configuration in Halbert would therefore have been the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement, *i.e.*, the distribution of interface circuitry across the substrate. EX1003 ¶250.

Moreover, a skilled artisan would have been motivated to adopt such an arrangement in the system of Halbert in order to place the interface circuits close to their associated memory devices and in between those memory devices and the lower edge connection to the system memory bus. Such an arrangement would create the shortest connection between the memory device and memory bus, thereby limiting flight time of the data signals and signal degradation due to reflections on the transmission line between the memory devices and the system memory bus. EX1013 at 66. Further, in such an arrangement, the most practical arrangement of the SYNC signal lines would be to run them horizontally along the line of interface circuits, since that would be the shortest and most direct path. EX1003 ¶251. Thus, this claim element would have been obvious over Halbert.

C. Halbert in View of Stone Render Claims 1-3, 7, 8, 10-12 Obvious

To the extent one might argue that Halbert alone does not sufficiently disclose or render obvious "*each circuit of the plurality of circuits comprising at least one write buffer and at least one read buffer*" and the claimed functionality of those buffers, it would have been obvious to include that limitation in the system of Halbert in view of the known designs of bi-directional buffers, such as those in Stone (EX1013). EX1003 ¶144.

Halbert and Stone are analogous art to the '185 Patent because they are all in the field of interfaces between components in a computer system. Indeed, Halbert,

the portions of Stone cited above and the '185 Patent are specifically in the field of memory interfaces for computer systems. EX1001, Abstract; EX1005, Abstract; EX1013, 126. The use of Stone's bidirectional buffers, each of which includes a write buffer and a read buffer, would have been merely the use of a known structure for its known purpose to achieve the predictable result of bidirectional transfer of data. EX1003 ¶145.

One of skill would have been motivated to look at known designs, such as those in Stone, in order to implement Halbert's interface circuit in a reliable way, since such known circuits provided predictable behavior. It was known, moreover, that to read and write data to and from a memory device a buffer of some type was needed and advantageous in order to drive a memory bus with several taps because the driver would have to deliver the required higher current and would have to deal with the transmission line characteristics of the bus. EX1013, 74; EX1003 ¶146. Moreover, Halbert's statement (EX1005, 9:30-35) indicating that unidirectional buffers may be used is an express suggestion to make that substitution. Finally, it would have been obvious to try separate read and write buffers, since there were only a few number of practical options for communicating data in both directions in the system of Halbert. EX1003 ¶¶142, 146. Claim 1 would therefore have been obvious over Halbert. *Id.*, ¶¶139-143, 146, 184, 188.

D. Halbert in View of Amidi Render Claims 1-3, 7, 8, 10-12 Obvious

1. Claim 1

To the extent one might argue that Halbert does not disclose "*each circuit of the plurality of circuits . . . configured to selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices in response to the module control signals, and to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller in response to the module control signals*," Halbert would render that limitation obvious in light of Amidi, EX1019.

Halbert and Amidi are analogous art to the '185 Patent because each is directed to the field of memory module design, *see* EX1001, 1:14-19; EX1005, 1:16-19; EX1019, ¶¶[0001-0012], and also because they are reasonably pertinent to the particular problem the inventor of the '185 Patent was trying to solve (efficient support of multi-rank memory modules, *see* EX1001, 1:35-2:51; EX1005, 1:40-2:60; EX1019, ¶¶[0001-0012]; EX1003 ¶160.

Amidi discloses a transparent four rank memory module, each rank having a corresponding chip select signal, and an emulator permitting the module to communicate with a memory socket having only two chip select signals. EX1019, ¶[0036], FIGS. 3, 6A; EX1003 ¶161. Amidi teaches using a CPLD 40 or other

controller circuitry configured to receive memory commands and addresses from a system memory controller, to determine which of four memory ranks to select for the memory operation based on first and second chip select signals and the highest address bits. *See* EX1019, ¶¶ [0008-0012], [0041], [0043], [0050-0057], FIGS. 3, 5, 6A-6B; EX1003 ¶¶162-163.

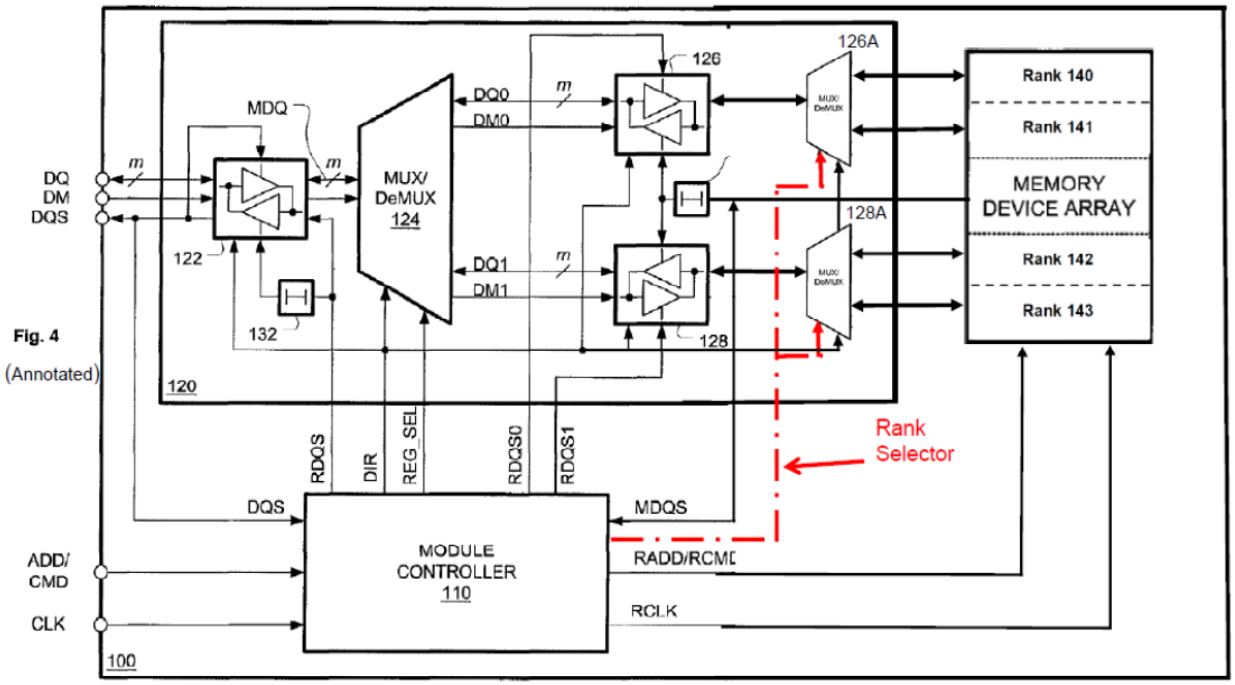
Amidi therefore discloses circuitry that selectively allows data transmission between a memory rank and a memory controller, and selectively isolates other ranks of memory from the memory controller, in response to CPLD control signals, as claimed. EX1003 ¶¶163-164[2]

It would have been obvious to employ the chip-select emulation functionality (*i.e.*, decoding address bits to generate module control signals in

[2] Indeed, the Board has previously found, in a proceeding analyzing a related patent also owned by Patent Owner, that Amidi's chip-select functionality "falls within the scope of the term 'selectively electrically isolating' as we have construed that term." IPR2014-01011, Paper 34 at 42 (12/14/2015). In that proceeding, the Board interpreted the phrase "selectively electrically isolating" to mean "making a selection between at least two components and not transferring power or signal information from on selected component to the other selected component." *Id*. at 13.

order to select among memory ranks) of Amidi in Halbert's memory module, and specifically in *Halbert*'s interface circuits. In such a combination of Halbert and Amidi, a high order address bit would be used by module controller 110 to produce a rank selector signal provided to multiplexors in the interface circuitry. EX1003 ¶165. A skilled artisan would be motivated to place this functionality in the interface circuitry of Halbert because a mismatch in timing between memory devices and data bus is one of Halbert's primary concerns, Ex. 1005, 3:42-52, so it would make sense for a skilled artisan to modify the interface circuits of Halbert, the timing of which Halbert's module controller is already designed to control and which are critical to Halbert's goals. EX1003 ¶¶166-169.

The modified interface circuitry of Halbert in an exemplary implementation of such a combination would look like the annotated version of Halbert's Figure 4 (reproduced below with annotations), with the new rank selector signals (shown in red) output by the module controller 110 and input to new multiplexors 126A and 128A in order to select among an increased number of memory ranks (i.e., four, rather than two in Halbert):



EX1003 ¶¶166-167.

In such a combination, Halbert's module controller 110 would include functionality similar to Amidi's CPLD 40, and would use a high order address bit to create the rank select signal, *see* EX1019, ¶¶ [0049], [0052], FIGS. 5, 8, which signal would then be provided to new multiplexors 126A and 128A. Based on the rank seector signal the multiplexors would select from among the outputs of the ranks of an expanded memory array that included additional ranks, Rank 141 and Rank 143. EX1003 ¶170.

For example, as Dr. Stone explains, during a read memory operation in which module controller 110 decodes the high order address bit such that the rank seector signal is output as logic 0, the outputs of Ranks 140 and 142 would be

selected (by multiplexors 126A and 128A, respectively) and provided to bidirectional buffers 126 and 128, respectively. The outputs of Ranks 141 and 143, however, would not be selected and could not be accessed during that memory operation; those ranks would be electrically separated, i.e., isolated, from the rest of the system, including from the system memory controller during that memory operation. EX1003 ¶171. A similar operation in which the rank seector signal is decided to be inactive would select the alternative Ranks Ranks 141 and 143, while isolating Ranks 140 and 142. EX1003 ¶172. In either case, the operation of the rest of the circuitry would occur as described in Halbert for his "AWAY" mode. EX1003 ¶173. The operation of this modified version of Halbert for a write to memory would be similar, with the mutliplexors 126A and 128A configured to connect the outputs of buffers 126 and 128, respectively, to the selected set of memory ranks, and the remainder of the interface circuitry operating as described in Halbert. EX1003 ¶173.

To employ this chip select functionality of Amidi in the system of Halbert would have been only the arrangement old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement, i.e., the predictable result of operating each rank at desired times, and well within the level of ordinary skill to achieve. EX1003 ¶¶175-176.

Moreover, a person of ordinary skill in the art would have been motivated to use the chip select functionality of Amidi in the system of Halbert to permit the use of lower density, and therefore cheaper and more readily available, memory in the system of Halbert, while using the existing address and data signal lines of Halbert. EX1019, ¶[0008]; *see also id.*, ¶¶ [0002-0012]; EX1003 ¶177.

A skilled artisan would also have been motivated to include such prior art chip selection signals in Halbert in order to follow the traditional design of memory ranks including the use of traditional memory devices and the traditional address signals, as Halbert explains. EX1005, 3:55-57; EX1003 ¶178.

Furthermore, Halbert suggests such a use by disclosing that "[m]any other variations on the illustrated embodiments are possible. For instance, . . . [t]he illustrated examples also show two ranks of memory, but other numbers of ranks are also possible." EX1005, 9:20-26. Skilled artisans at the time would have understood that, in case the number of ranks is increased, chip/bank select signals would need to be used to activate some but not all of the ranks. *See, e.g.*, EX1019 at FIGS. 5, 6A-6B (showing logic circuitry to generate chip select signals for additional ranks); EX1003 ¶179.

Claim 1 is therefore obvious over Halbert in view of Amidi.

2. Claim 11

To the extent one might argue that Halbert alone does not disclose or render obvious the requirement of claim 11 of a "*second indication of whether a first group of the plurality of memory devices or a second group of the plurality of memory devices are being accessed*," it would have been obvious over Halbert in view of Amidi, EX1019. As demonstrated above, it would have been obvious to include the chip-select functionality of Amidi in the system of Halbert and in that combination Halbert's module controller would output chip-select signals to activate different ranks of memory at different times and for different memory accesses. *See* EX1003 ¶¶159-179. Such chip-select signals constitute a "*second indication of whether a first group of the plurality of memory devices or a second group of the plurality of memory devices are being accessed*" because they indicate which ranks are being accessed. Thus, the combination of Halbert and Amidi renders this claim obvious. EX1003 ¶240.

E. Halbert in View of Connolly Render Claim 3 Obvious

To the extent one might argue that Halbert does not disclose mechanically coupling memory and control circuits to a printed circuit board having an edge "*wherein the packages are positioned along the edge and between the edge and the plurality of memory device*" as required by claim 3, it would have been obvious to include it in the system of Halbert in view of Connolly. Connolly discloses such

an arrangement of circuit packages on a PCB, EX1016, 3:4-10 and FIG. 6A, so the combination of Halbert and Connolly would satisfy this claim element and would therefore have been the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement. EX1003 ¶202.

Moreover, Halbert, Connolly and the '185 Patent are analogous art because they are each in the field of memory module design, (EX1001, 1:14-19; EX1005, 1:16-19; EX1016 1:19-22), or at least reasonably pertinent to the problem of optimizing or making more efficient computer memory modules, which is the problem addressed by the '185 Patent. EX1001, 1:40-2:17; EX1005, 3:32-4:35; EX1016, 1:24-52; EX1003 ¶203.

A skilled artisan would have been motivated to employ the arrangement of Connolly in the system of Halbert to use conventional, readily available materials (such as a PCB) and in order to reduce the transmission line length (and therefore flight time and signal degradation due to reflections on the transmission line) between the memory devices and the system memory bus. *See, e.g.*, EX1013, 66; EX1016, 1:56-2:19; EX1003 ¶204.

This claim would therefore have been obvious over Halbert in view of Connolly.

F. Halbert in View of JESD79 Render Claim 10 Obvious

To the extent one might argue that Halbert does not disclose or render obvious the use of the CAS latency parameter as recited in claim 10, that use would have been obvious over Halbert in view of the JESD79 standard, EX1007. Halbert and JESD79 are analogous art to the '185 Patent because each is in the field of computer memory systems. EX1001, 1:14-19; EX1005, 1:16-19; EX1007, i; EX1003 ¶220.

The skilled artisan would have been motivated to look to the JEDEC standard JESD79 when implementing the system of Halbert because Halbert expressly teaches to use DDR SDRAM devices, EX1005, 9:56-61, and because JESD79 "define[s] the minimum set of requirements for JEDEC-compliant 64M x4/x8/x16 DDR SDRAMs." EX1007, i. JESD79 specifies permitted values for CAS Latency of compliant memories and how to program such values into a memory device using a mode register set command. *Id*. at 1, 8, 9, 14. Thus, in order to determine available latencies for DDR SDRAM devices at the time and therefore employ the interface circuitry of Halbert with industry-standard JEDEC memory devices, the skilled artisan would have turned to JESD79 which was a well-known and widely adopted standard for DDR SDARM memory chips to obtain the required latencies. EX1007, Cover; EX1010. Skilled artisans at the time would also have been motivated to use such CAS latency parameters in order

to provide interoperability between different devices as provided by the relevant standards, such as JESD79. For example, U.S. Pat. No. 5,630,096 to Zuravleff (EX1024) expressly teaches that it is desirable to design memory systems compatible with JEDEC standards for DRAMS to support many design applications. EX1024, 1:65-2:3; EX1003 ¶221.

The JESD79 standard teaches that "DDR SDRAMs must be powered up and initialized in a predefined manner." EX1007, p. 8. This initialization includes "a MODE REGISTER SET command [which] should be issued for the Mode Register, to reset the DLL, and to program the operating parameters." *Id*. These parameters include a CAS latency (A4-A6). *Id*., pp. 8-9, FIG. 1. Skilled artisans at the time would have understood this disclosure to require the system memory controller to initialize the SDRAM devices and set their CAS latency parameter. EX1003 ¶222.

Because Halbert discloses embodiments compatible with such prior systems where the system controller sets the CAS latency of the memory devices in the memory module, skilled artisans would have understood that, to be "transparent" to the system controller as Halbert desires, EX1005 3:48-56, the controller 110 should use the same CAS latency parameter to determine when the requested data should be available. Indeed, in the implementation of FIG. 5, the controller 110 generates control signals, such as RDQS and REG_SEL signals, with a timing so

that the requested data appears on the DQ bus at the same CAS latency as in the prior art. EX1005, 5:66-6:65, FIG. 5; EX1003 ¶223.

Furthermore, Halbert discloses that the module controller 110 can "snoop" command signals as they pass through and can use the "snooped" signals to generate control signals, such as the signal DIR, for the interface circuits 125 and 130. EX1005, 5:25-30. Skilled artisans at the time would have understood that the module controller 110 could also have determined the CAS latency parameter the same way, by snooping the mode register set commands that are disclosed, for example, in the JEDS79 standard. EX1007, pp. 8, 13; EX1003 ¶¶224-227.

Thus, a skilled artisan would have been motivated to implement the interface circuits of Halbert such that they would be controlled by the module controller "*using a Column Access Strobe (CAS) latency parameter*" so that his system could be compliant with the well-accepted and widely available JEDEC standard JESD79. EX1003 ¶228. Thus, Halbert in combination with the JEDEC standard JEDS79 renders obvious that "*the controller is configured to control the plurality of circuits using a Column Access Strobe (CAS) latency parameter.*"

VI. CONCLUSION

Because the information presented in this petition shows that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the petition, the Petitioner respectfully requests that a

Trial be instituted and that claims 1-3, 7, 8, and 10-12 of the ’185 Patent be canceled as unpatentable.

Dated: January 5, 2017

Respectfully Submitted,

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,821 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 8,516,185

Attachment A:

Proof of Service of the Petition

CERTIFICATE OF SERVICE

I hereby certify that on this 5th day of January, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by Federal Express on the following counsel of record for patent owner:

Jamie J. Zheng
P.O. Box 60573
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Dated: January 5, 2017

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 8,516,185

Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Exhibit #	Reference Name
1001	U.S. Patent No. 8,516,185
1002	File History of U.S. Patent No. 8,516,185
1003	Declaration of Harold S. Stone
1004	Curriculum Vitae of Harold S. Stone
1005	U.S. Patent No. 7,024,518 to Halbert et al.
1006	USP Application Pub. No. 2006/0262586 by Solomon et al.
1007	JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79, June 2000
1008	U.S. Patent No. 8,130,560 to Rajan et al.
1009	TI74LS245
1010	Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC)
1011	IPR2014-01369 ("the '1369 IPR") filed by SMART Modular Technologies, Inc.
1012	IPR2014-01029 ("the '1029 IPR") filed by SanDisk Corporation
1013	Microcomputer Interfacing by Harold S. Stone, © 1982 by Addison-Wesley Publishing Company
1014	U.S. Patent No. 7,191,302 to Usami
1015	U.S. Patent No. 6,704,910 to Hong
1016	U.S. Patent No. 6,070,217 to Connolly et al.
1017	U.S. Patent No. 7,289,386 to Bhakta et al.
1018	U.S. Patent No. 7,532,537 to Solomon et al.
1019	U.S. Patent Application Publication No. 2006/0117152 to Amidi et al.

Exhibit #	Reference Name
1020	U.S. Patent Application Publication No. 2007/0070669
1021	U.S. Patent Application Publication No. 2011/0016269 (Application No. 12/504, 131, "the '131 priority application")
1022	U.S. Patent No. 6,721, 860 to Klein
1023	U.S. Patent No. 6,011,710 to Wiggers
1024	U.S. Patent No. 5,630,096 to Zuravleff
1025	U.S. Patent Application Publication No. 2011/0016250