UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner

Patent No. 8,359,501
Issued: January 22, 2013
Filed: July 14, 2011
Inventors: Hyun Lee, Jayesh Bhakta, Soonju Choi
Title: MEMORY BOARD WITH SELF-TESTING CAPABILITY

Inter Partes Review No. IPR2017-00562

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,359,501 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123

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I. INTRODUCTION

This Petition seeks cancellation of claim 16 of U.S. Patent No. 8,359,501 ("the '501 Patent") based, primarily, on U.S. Patent Application Publication No. 2005/0257109 to Averbuj ("Averbuj"). The Board has previously found numerous claims of the 501 Patent and its parent unpatentable based on Averbuj. *See* IPR2014-00971, Paper 37, IPR2014-00970, Paper 32. This Petition is based primarily on the analysis accepted by the Board in those prior proceedings. Indeed, there is nothing in the claims challenged here that could distinguish them from Averbuj under the Board's previous analysis, so those claims are also unpatentable.

However, the Petition also adds to that analysis and strengthens it. For example, Petitioners address arguments that Patent Owner may raise by proposing additional grounds that more closely satisfy the claim limitations to which such arguments would be directed. Such additional grounds are not redundant because they are "rational, narrowly targeted, and not burdensome considering only [two] claims with very similar limitations are at issue." IPR2015-01912, Paper 10 at 17-18. Petitioners therefore respectfully request that trial be instituted on all grounds and arguments advanced herein.

II. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR *INTER PARTES* REVIEW

A. Mandatory Notices

1. Real Parties In Interest

The real parties of interest of this petition are the Petitioners: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

2. Related Matters

U.S. Patent No. 8,359,501 ("the '501 Patent") relates to the following legal proceedings: *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 4:13-cv-05889-YGR (N.D. Cal.); *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 2:13-cv-02613-TLN (E.D. Cal.); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No. IPR2014-00970 (PTAB); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No. IPR2014-00971 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01372 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01373 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01374 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01375 (PTAB); *Netlist, Inc. v. SanDisk LLC et al.*, Case Nos. 16-2274, -2338, -2339 (Fed. Cir.); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 16-2666 (Fed. Cir.); *Netlist, Inc. v. SK hynix Inc. et al.*, Case No. 8:16-cv-01605-JLS (C.D. Cal.); and *In re Certain Memory Modules & Components Thereof*, Inv. No. 337-TA-1023 (ITC).

In addition, petitions for *inter partes* review of U.S. Patent Nos. 8,001,434 (IPR2017-00561) and 8,689,064 (IPR2017-00560), which are related to the '501 Patent, are being filed concurrently with this petition.

3. Lead & Back-up Counsel

Lead Counsel is Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492. Backup Lead Counsel are: Steve Baik (Reg. No. 42,281), Sidley-SKH-IPR@sidley.com, 650-565-7016, Wonjoo Suh (Reg. No. 64,124), Sidley-SKH-IPR@sidley.com, (202) 736-8831, and Ryuk Park (*pro hac vice* to be requested), Sidley-SKH-IPR@sidley.com, 650-565-7074.

4. Service Information

Service on Petitioners may be made by e-mail (Sidley-SKH-IPR@sidley.com), or by mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

B. Fee for *Inter Partes* Review (37 C.F.R. § 42.15(a))

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 50-1597.

C. Certification of Word Count (37 C.F.R. § 42.24(a)(1))

Petitioners certify that this petition for *inter partes* review contains 7,695 words, excluding the parts of that are exempted by 37 C.F.R. § 42.24(a)(1), per the count of the word-processing system used to prepare this petition.

D. Certification of Standing (37 C.F.R. § 42.104(a))

Petitioners certify they are not barred or estopped from requesting *inter partes* review of the ’501 Patent (Ex. 1001). This petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of the ’501 Patent. Neither Petitioners nor any party in privity with Petitioners has filed a civil action challenging the validity of any claim of the ’501 Patent. The ’501 Patent has not been the subject of a prior *inter partes* review by Petitioner or a privy of Petitioners. Petitioners therefore certify this patent is available for *inter partes* review.

E. Proof of Service (37 C.F.R. §§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Claims 1 and 4 of the '501 Patent are unpatentable as follows:

1. Claims 1 and 4 of the '501 Patent are unpatentable as anticipated under 35 U.S.C. § 102 by U.S. Patent Publication No. 2005/0257109 by Averbuj ("Averbuj"; Ex. 1005);
2. Claims 1 and 4 of the '501 Patent are unpatentable as obvious under 35 U.S.C. § 103over Averbuj; and
3. Claim 4 of the '501 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Averbuj in view of U.S. Patent Publication No. 2007/0070669 by Tsern ("Tsern"; Ex. 1006).

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ IV-VI, below. The evidence relied upon in this petition is listed in **Attachment B**.

IV. RELEVANT INFORMATION CONCERNING THE '501 PATENT

A. Effective Filing Date of the '501 Patent

The application that resulted in the '501 Patent is U.S. Patent Application Serial No. 13/183,253, filed July 14, 2011. Ex. 1001 at 1. The '501 Patent is a continuation of U.S. Patent No. 8,001,434, which claims priority to Provisional Application Nos. 61/044,801, 61/044,825, and 61/044,839, filed on April 14, 2008. *Id.* Patent Owner contended, in a related proceeding, that the conception date of

the ’501 Patent is June 21, 2007. While Petitioners disagree with Patent Owner’s assertion of an earlier conception date, Petitioners will assume, solely for the purpose of this proceeding, that the claims of the ’501 Patent have an effective filing date of June 21, 2007.

B. Person of Ordinary Skill in the Art

A person of ordinary skill (“POSITA”) in the art in the field of the ’501 Patent would have been someone with “a Bachelor’s degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST.” IPR2014-00971, Paper 34 at 10-11 (Dec. 14, 2015); IPR2014-00970, Paper 32 at 10-11 (Dec. 14, 2015); Ex. 1003 at ¶ 51.

C. Overview of the ’501 Patent

The ’501 Patent discloses a self-testing memory module for testing a plurality of memory devices using a control module that generates test address and control signals, and a data module comprising a plurality of data handlers that generate test data signals. Ex. 1001 at 1 (Abstract). An illustrative example is shown in Fig. 2, as reproduced below. Ex. 1003 at ¶ 52.

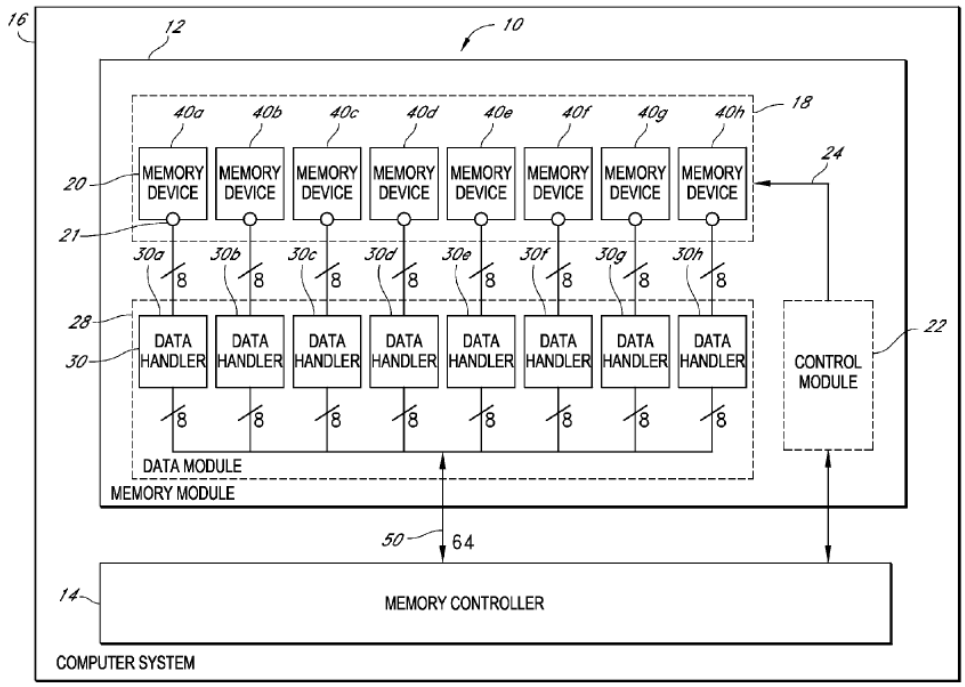


FIG. 2

Ex. 1001 at Fig. 2.

As shown in Fig. 2, the memory module (12) includes a control module (22) and a data module (28) that are connected to an array of memory devices (20). The control module (22) generates the address and control signals for testing the memory devices. Ex. 1001 at 5:12-14, Figs. 2-3; Ex. 1003 at ¶ 53. The data module (28) generates test patterns to write to the memory devices (20) and checks the data patterns read or received back from the memory devices (20) for agreement with corresponding data patterns that are expected to be read back from the memory devices. Ex. 1001 at 5:27-33; Ex. 1003 at ¶ 53.

The data module (28) includes a plurality of data handlers (30) that are each located in proximity to a corresponding memory device (20), as illustrated in Fig.

2. Ex. 1001 at 9:17-26, Figs. 2-3; Ex. 1003 at ¶ 54. Each data handler (30) is operable independently from each of the other data handlers (30) in that each data handler (30) is configured to write to and/or read from the corresponding plurality of data ports of one or more of the memory devices (20) without being in communication with any of the other data handlers (30) or other data ports of the memory devices (20). Ex. 1001 at 8:5-35; Ex. 1003 at ¶ 54.

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 C.F.R. § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

The Board has previously interpreted certain claim terms of the ’501 Patent in prior IPR proceedings. For the purposes of this proceeding only, Petitioner adopts the Board’s interpretations and therefore applies those same interpretations, as set forth below:

1. *"operated independently"* (claim 1)

The Board has previously concluded that the broadest reasonable interpretation of "*operated independently*" is "[o]perated, operating, without influence or control by another." *See* IPR2014-00971, Paper 37 at 13-18, 30 (Apr. 27, 2016). This is consistent with the '501 Patent's disclosure. *See*, *e.g.*, Ex. 1001 at 1 (Abstract), 5:16-23, 8:5-15, 8:22-35.

2. *"configured to"* (claim 1)

The Board has previously concluded that the broadest reasonable interpretation of "*configured to*" is "designed to, adapted to, or arranged to [e.g., perform a function or be capable of performing a function]." *See* IPR2014-00971, Paper 37 at 18-22, 31. This is consistent with the '501 Patent's disclosure and a POSITA's understanding and usage of the term. *See*, *e.g.*, Ex. 1001 at 7:25-31; Ex. 1007 at 292 (dictionary definition of "configure"). Further, Patent Owner's expert, Dr. Sechen, previously offered testimony supporting the Board's construction. *See* IPR2014-00971, Paper 37 at 21 ("Dr. Sechen testified that 'configured to' as used in the context of the phrase 'a printed circuit board configured to be operatively coupled . . . might mean designed [to].'").

3. *"generate"* (claim 1)

The broadest reasonable construction of "*generate*" is "produce." *See* IPR2014-00971, Paper 37 at 31. This is consistent with the '501 Patent's disclosure. *See*, *e.g.*, Ex. 1001 at 5:48-55, 6:11-17, 9:29-31, 10:31-37.

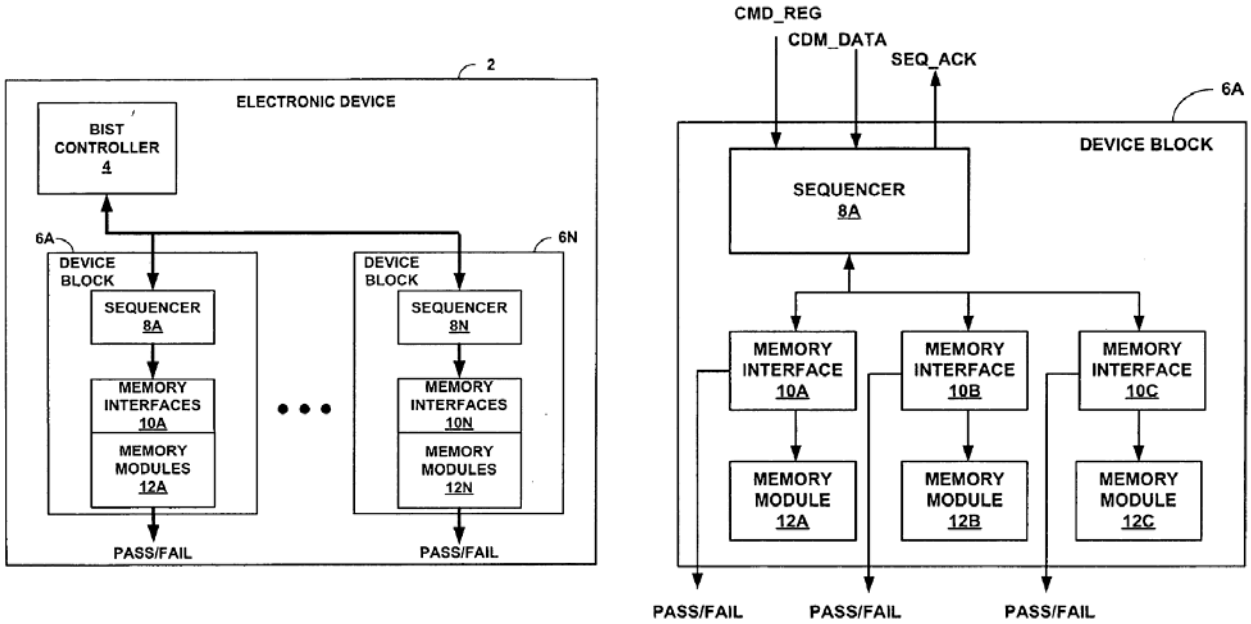
V. OVERVIEW OF THE PRIOR ART

A. U.S. Patent Application No. 2005/0257109 to Averbuj (Ex. 1005)

U.S. Patent Application No. 2005/0257109 to Averbuj ("Averbuj"; Ex. 1005) was filed on July 29, 2003 and published on November 17, 2005. Ex. 1005 at 1. Averbuj is thus prior art to the '501 Patent under 35 U.S.C. §§ 102 (a), (b), and (e).

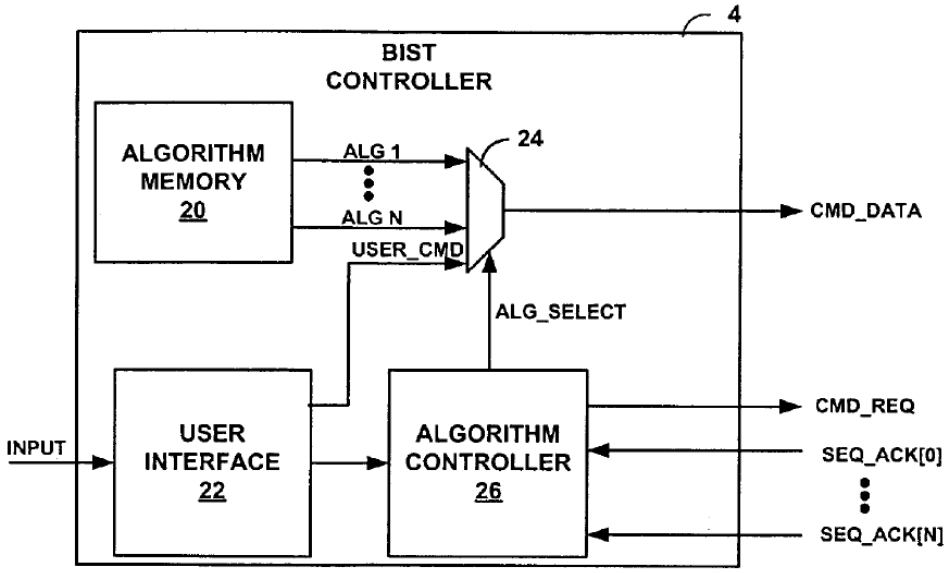
Averbuj is titled "Built-In Self Test (BIST) Architecture Having Distributed Interpretation and Generalized Command Protocol" and generally directed to a built-in self test ("BIST") architecture for memory modules in electronic devices. More particularly, Averbuj discloses an improved BIST architecture for reducing redundant circuitry. Ex. 1005 at ¶¶ [0007-0008], Fig. 1; Ex. 1003 at ¶ 64.

Averbuj explains that BIST units at the time were commonly incorporated into each memory chip and memory module of an electronic device. Ex. 1005 at ¶¶ [0003-0005]; Ex. 1003 at ¶ 65. Having a fully-integrated BIST unit in each memory chip or module created redundant circuitry since some of the functions performed by the BIST units, such as providing test algorithms, were common to many or all of the memory chips and modules. Ex. 1005 at ¶ [0008]; Ex. 1003 at ¶ 65.



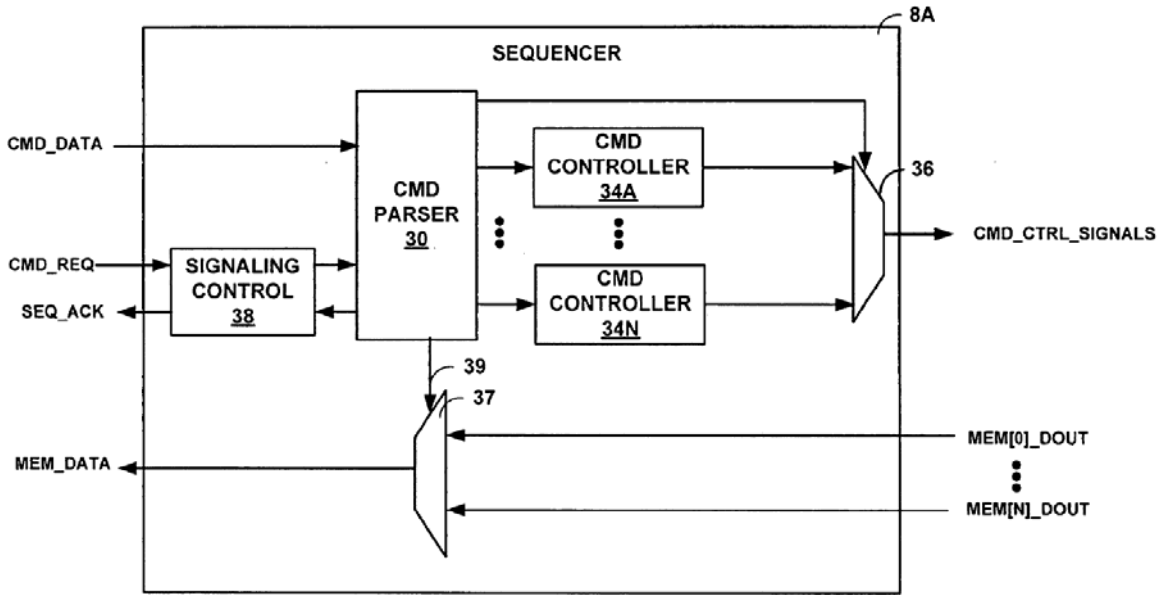
Ex. 1005 at Figs. 1 (left) & 4 (right).

Averbuj's proposed solution was a distributed BIST architecture with a hierarchy that reduces such redundancies. Ex. 1005 at ¶ 8; Ex. 1003 at ¶ 66. As shown in Fig. 1 of Averbuj, at the top of the hierarchy is a single, centralized BIST controller which provides high-level algorithms or test patterns to all of the memory modules of an electronic device. Ex. 1005 at Fig. 1, ¶ [0008]; Ex. 1003 at ¶ 67. The BIST controller reduces redundant circuits because the "common test patterns need not be redundantly stored within memory modules." Ex. 1005 at ¶ [0008]; Ex. 1003 at ¶ 67.



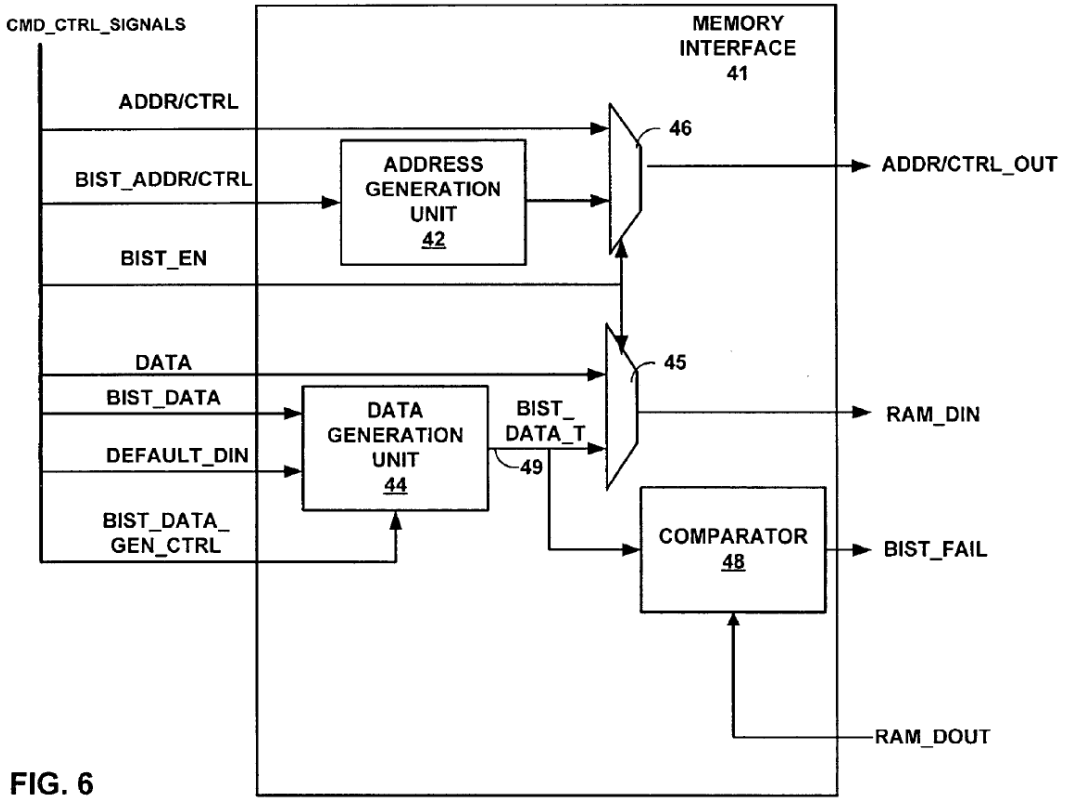
Ex. 1005 at Fig. 2.

At the next level of hierarchy are the sequencers (8). The sequencers (8) are "distributed within device blocks that include one or more memory modules." Ex. 1005 at ¶ [0009]. Each sequencer (8) of a device block (6) receives one or more high-level commands from the BIST controller (4) and generates test address, control, and data signals for the plurality of memory modules (12). Ex. 1005 at ¶¶ [0009], [0043-0044], Figs. 4-6; Ex. 1003 at ¶ 68.



Ex. 1005 at Fig. 5.

At the bottom of the hierarchy are the memory interfaces (10, 41). The memory interface "handles specific interface requirements for each of the memory modules" by "receiv[ing] memory operations from a controlling sequencer, and translat[ing] the memory operations, including associated address and data signals, **as needed** based on the physical characteristics of the respective memory module." Ex. 1005 at ¶ [0011] (emphasis added); *see also id.* at Fig. 6; Ex. 1003 at ¶ 69.



Ex. 1005 at Fig. 6.

Specifically, the memory interface (41) receives the test address and control signals from its controlling sequencer (8). The memory interface (41) either provides the same test address and control signals to the memory module (12) as is, or creates its own test address and control signals for the memory module (12) by transforming the test address and control signals from the sequencer (8). Ex. 1005 at Fig. 6, ¶¶ [0011], [0048], [0051-0052],; Ex. 1003 at ¶ 70. The memory interface (41) also receives the test data signals from its controlling sequencer (8), and either provides the same test signals to the memory module (12) as is, or generates its own test data signals for the memory module (12) by modifying the data signals from the sequencer (8). Ex. 1005 at Fig. 6, ¶¶ [0011], [0049-0050]; Ex. 1003 at

¶ 70. Finally, the memory interface (41) uses the comparator (48) to check the data patterns read or received back from the memory module (12) to verify whether the data that is read back from the memory module (12) corresponds to the data pattern. Ex. 1005 at Fig. 6, ¶ [0053]; Ex. 1003 at ¶ 70.

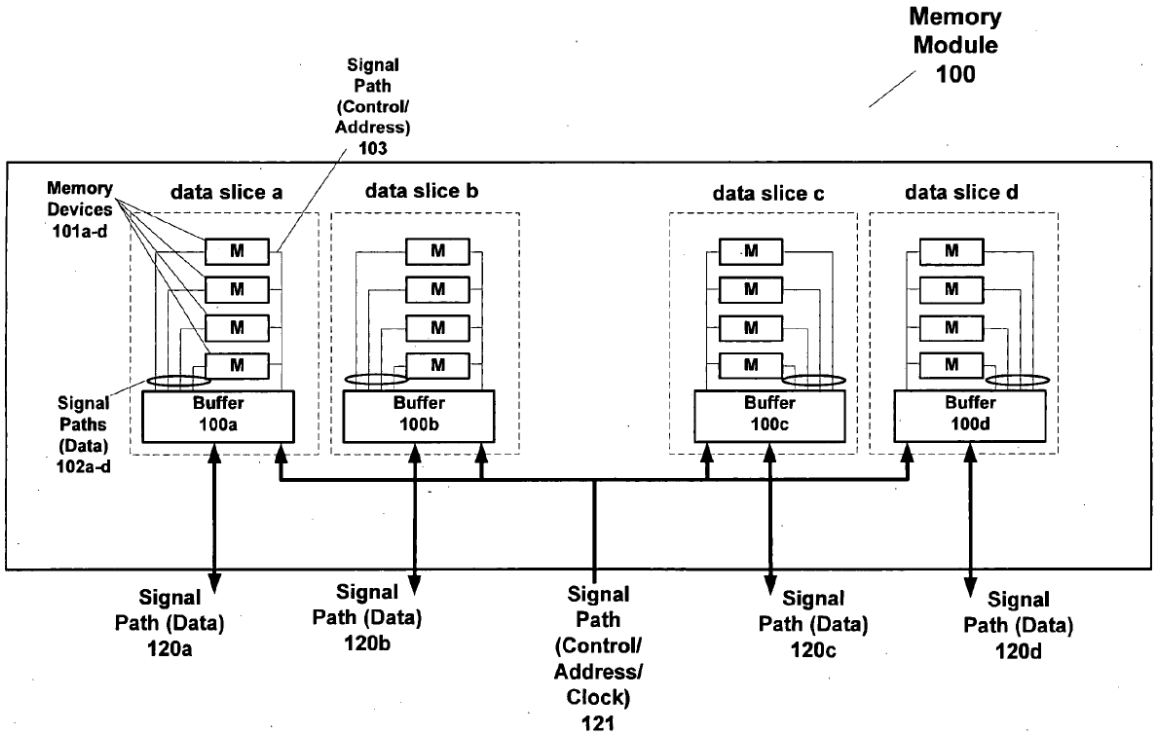
As shown in Figs. 1 and 4 of Averbuj, each memory interface (10, 41) is positioned directly above, and in alignment with, a corresponding memory module (12). Ex. 1005 at Figs. 1, 4; Ex. 1003 at ¶ 72. Further, no signal is described as flowing from one memory interface (*e.g.*, 10A) to another (*e.g.*, 10B). Ex. 1005 at Fig. 4; Ex. 1003 at ¶ 72. Instead, each memory interface (10, 41) is configured to write to and/or read from the corresponding address and data ports of a corresponding memory module (12) without being in communication with any of the other memory interfaces (10, 41) or other data ports of the other memory modules (12). Ex. 1005 at Fig. 4; Ex. 1003 at ¶ 72.

B. U.S. Patent Application No. 2007/0070669 to Tsern (Ex. 1006)

U.S. Patent Publication No. 2007/0070669 to Tsern ("Tsern"; Ex. 1006) was filed on September 26, 2005 and published on March 29, 2007. Ex. 1006 at 1. Tsern is thus prior art to the '501 Patent under 35 U.S.C. §§ 102(a), (b), and (e).

Tsern is titled "Memory Module Including a Plurality of Integrated Circuit Memory Devices and a Plurality of Buffer Devices in a Matrix Topology." Fig. 1

of Tsern illustrates an embodiment of a memory module with memory devices (101a–d) and corresponding buffer devices (100a–d). Ex. 1003 at ¶ 74.



Ex. 1006 at Fig. 1.

Tsern discloses that, in one embodiment, each buffer device (100a) includes a redundancy and repair unit (1883) which tests and repairs the corresponding memory device(s). Ex. 1006 at Fig. 18, ¶ [0077]; Ex. 1003 at ¶ 75. Each such buffer device (100a) includes data, address, and control interfaces (1820a and 1820b) that can be programmed or configured to support memory modules with different number, size, width, and type of memory devices. Ex. 1006 at Fig. 18, ¶ [0099]; Ex. 1003 at ¶ 75.

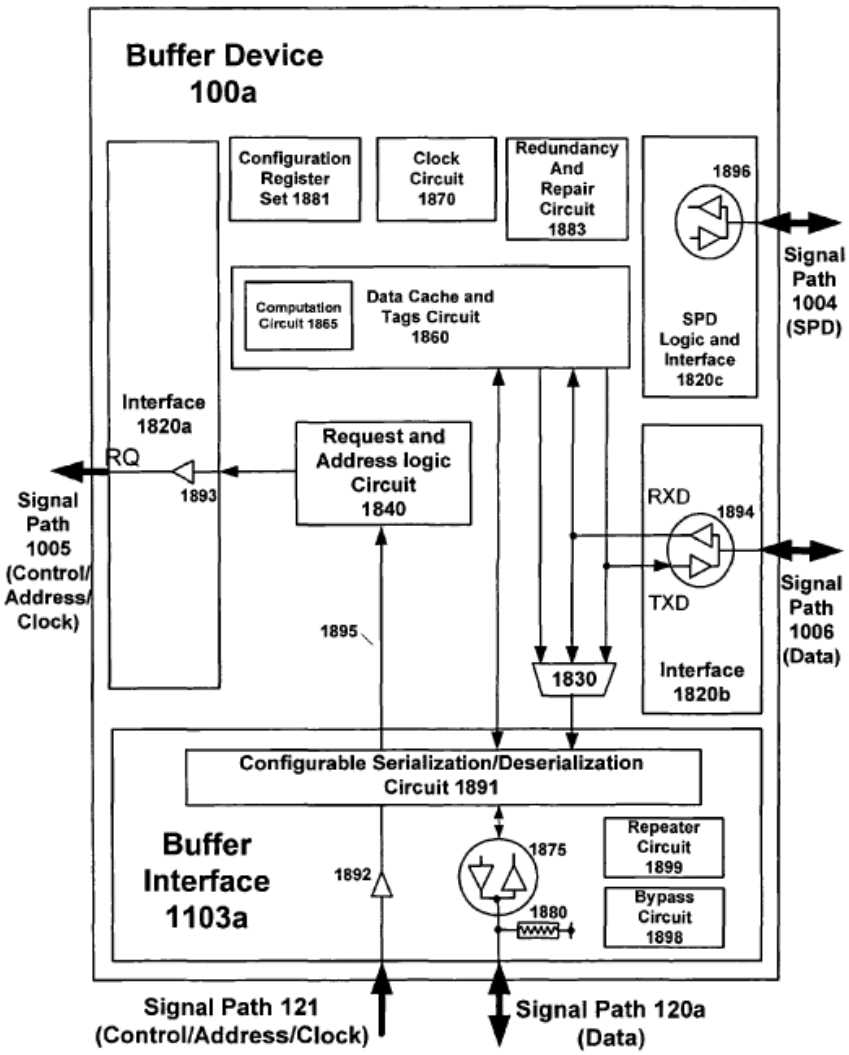


Fig. 18

Ex. 1006 at Fig. 18.

In one embodiment, the redundancy and repair circuit (1883) periodically tests one or more of memory devices (101a-d) by writing test patterns to a range of addresses and then reading back the values from the same addresses. Ex. 1006 at ¶ [0097], Fig. 18; Ex. 1003 at ¶ 76. If the value read from an address does not match the value written to that address, the redundancy and repair circuit (1883) blocks access to that address and maps the address to an alternate storage location by

translating incoming address signals accordingly. Ex. 1006 at ¶ [0097], Fig. 18; Ex. 1003 at ¶ 76.

Fig. 1 of Tsern shows that each buffer device (100a-d) communicates address, control, and data signals with its corresponding memory device(s) (101a-d) without being in communication with any of the other buffer devices (100a-d) or other data ports of the other memory devices. Ex. 1006 at Fig. 1; Ex. 1003 at ¶ 77.

Fig. 1 of Tsern also shows that each buffer device (100a-d) is positioned close to its corresponding memory device(s). In fact, each buffer device in Fig. 1 of Tsern is shown as being positioned closer to the data port(s) of its corresponding memory devices than to the data ports of the other memory devices. Ex. 1006 at Fig. 1; Ex. 1003 at ¶ 78.

Finally, Fig. 9 of Tsern shows an implementation of a memory module in which each of the four buffer devices (100a-d) is implemented as a physically separate integrated circuit package and mounted on different portions of the printed circuit board that houses the memory module. Ex. 1006 at Figs. 9A-C; Ex. 1003 at ¶ 79.

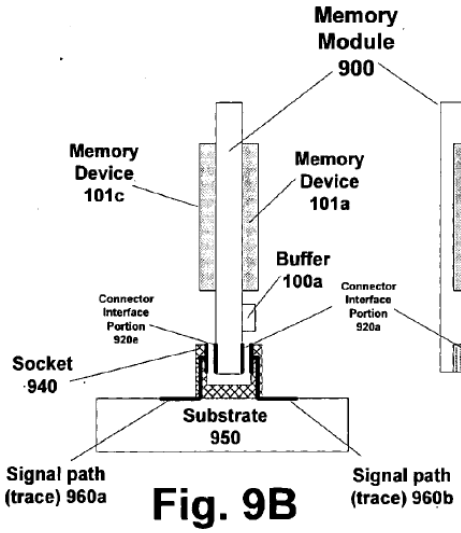


Fig. 9B

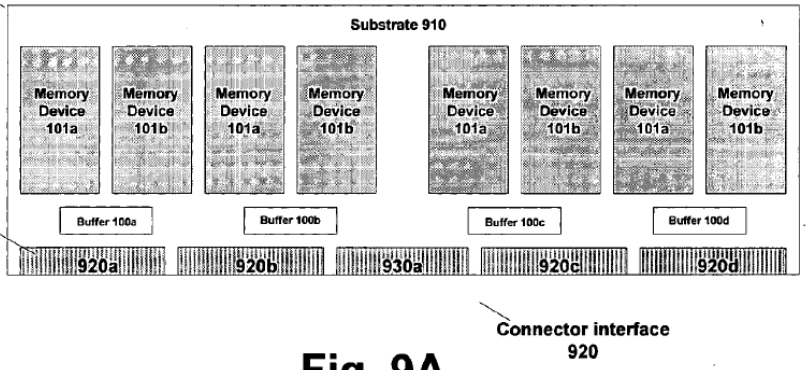


Fig. 9A

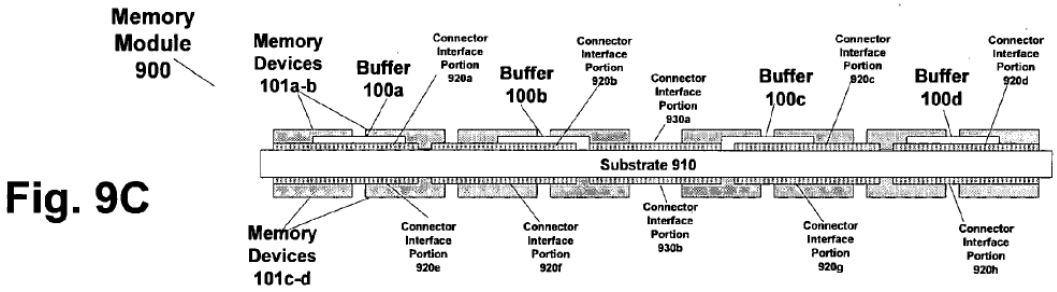


Fig. 9C

Ex. 1006 at Figs. 9A-C.

VI. PRECISE REASONS FOR RELIEF REQUESTED

A. Averbuj Anticipates Claims 1 and 4

1. Averbuj Anticipates Claim 1

a. Preamble

The preamble of claim 1 recites "*a memory system configured to be operatively coupled to a memory controller of a computer system*." Ex. 1001 at 16:38-39 (emphasis added).

Petitioner observes that the preamble of claim 1 is not limiting, as nothing in the body of the claim refers to an operative coupling to a memory controller of a computer system.

Nevertheless, Averbuj discloses this preamble, as demonstrated immediately below.

i. *"a computer system"*

Averbuj discloses that his electronic device (2) can be an embedded computer system, a computer, or a server. Ex. 1005 at ¶ [0032], Fig. 1; Ex. 1003 at ¶ 84. The electronic device (2) therefore constitutes a "*computer system*." Ex. 1003 at ¶ 84.

ii. "a memory system"

Averbuj discloses that electronic device (2) includes a plurality of device blocks (6), each of which includes a sequencer (8), a set of memory interfaces (10) interfacing with a set of corresponding memory modules (12). Ex. 1005 at Figs. 1. 4; Ex. 1003 at ¶ 83. Therefore, Averbuj discloses "*a memory system*."

iii. *"configured to be operatively coupled to a memory controller"*

Averbuj also discloses a BIST controller (4) that operates as a centralized "*memory controller*" during test mode by sending test commands (CMD_DATA and CMD_REQ) to the device blocks ("*memory system*") of the electronic device, ("*a computer system"*) and monitoring the status of the memory testing operation

(*e.g.*, SEQ_ACK). Ex. 1005 at ¶¶ [0008], [0029], [0033-0037], Figs. 1-2, 9A-E; Ex. 1003 at ¶ 85. Averbuj therefore discloses "*a memory system configured to be operatively coupled to a memory controller of a computer system*," as claimed. Ex. 1003 at ¶ 86.

Alternatively, in one embodiment, a "programmable processor" also provides address, control, and data signals to the device blocks (6) ("*memory system*"), which are applied to the memory modules (12) during normal mode. Ex. 1005 at ¶ [0048]; Fig. 6; Ex. 1003 at ¶ 87. The "programmable processor" disclosed in Averbuj is, or includes, "*a memory controller of a computer system*" as claimed because a device that provides the address, control, and data signals to, and thereby controls the data flow of, the memory modules of an electronic device such as an "embedded computing system, computer, [or] server" (Ex. 1005 at ¶ [0032]) is "*a memory controller of a computer system*." Ex. 1008 at 497; Ex. 1009 at Figs. 1-2 (at 5); Ex. 1003 at ¶¶ 88-90.

Finally, the preamble does not actually require that "*a memory system*" be "*operatively coupled to a memory controller*." All that is required is that "*a memory system*" be "designed to, adapted to, or arranged to [be] or be capable of [being]" "*operatively coupled to a memory controller*." IPR2014-00971, Paper 37 at 31. That Averbuj's electronic device is capable of receiving address, control, and data signals from an external device demonstrates that it is capable of being

operatively coupled to a device that manages the data flow of a memory by issuing address, control, and data signals. Ex. 1008 at 497; Ex. 1009 at Fig. 1-2; Ex. 1003 at ¶ 91.

Therefore, Averbuj discloses the preamble of claim 1. Ex. 1003 at ¶ 92.

b. "memory chips"

Claim 1 requires "*a plurality of memory chips*." Ex. 1001 at 16:41 (emphasis added).

Averbuj discloses an electronic device (2) that includes a plurality of memory modules (12) which may be any type of memory. Ex. 1005 at Figs. 1, 4, ¶ [0032]; Ex. 1003 at ¶ 94. Each memory module (12) disclosed in Averbuj is a "*memory chip*" because Averbuj equates "memory chips" with the various types of memory (*e.g.*, DRAM, Flash memory) that are disclosed as comprising the memory modules (12) of his electronic device. Ex. 1005 at ¶ [0003]; *compare* Ex. 1005 at ¶ [0006] (DRAM chip) *with* ¶ [0032] (DRAM module); Ex. 1003 at ¶¶ 95-96. This is consistent with Averbuj's disclosure that his electronic devices are constructed from many integrated circuit chips. Ex. 1005 at ¶ [0005]; Ex. 1003 at ¶ 97.

Therefore, Averbuj discloses this claim element. Ex. 1003 at ¶ 98.

c. "data handlers"

Claim 1 also requires "*a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips*." Ex. 1001 at 16:42-46 (emphasis added).

i. *"a plurality of data handlers"*

Each of the plurality of memory interfaces (10, 41) of a device block (6) includes a data generation unit (44), an associated comparator (48), and an associated multiplexor (45). Ex. 1005 at Fig. 6. Each data generation unit (44), multiplexor (45), and comparator (48) (collectively "data generation circuitry"), as a whole, is a "*data handler*" because it handles data written to and read out from its associated memory modules. Ex. 1005 at ¶¶ [0049-0050]; Ex. 1003 at ¶ 100.

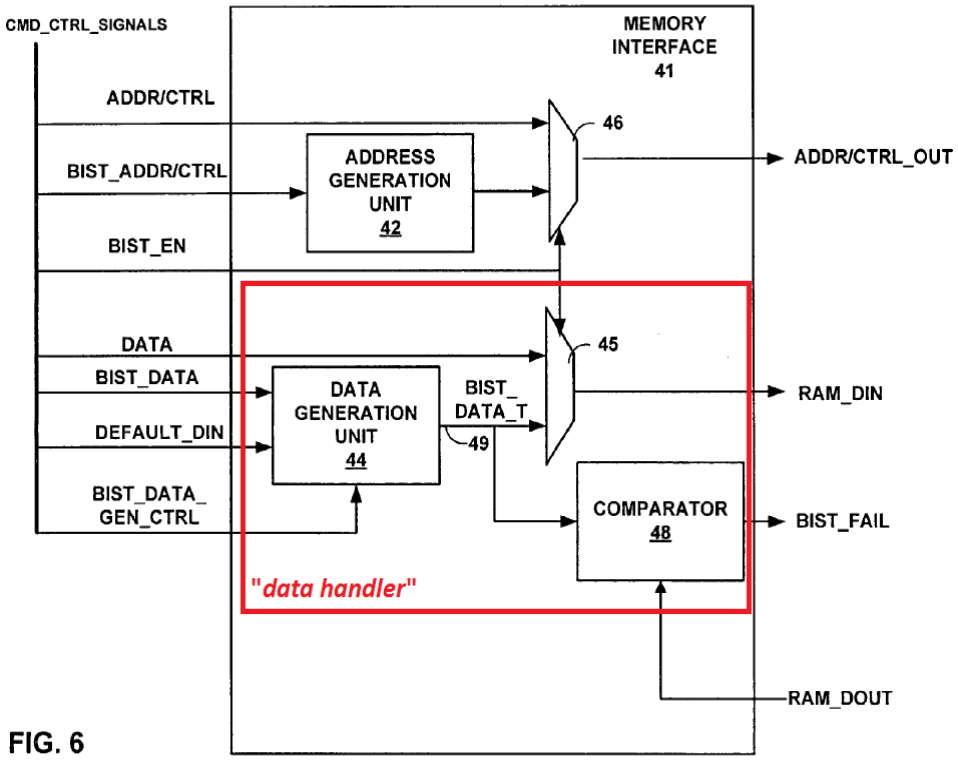


FIG. 6

Ex. 1005 at Fig. 6 (annotated and highlighted).

ii. *"configured to be operated independently from one other"*

Each data generation circuitry (44, 45 and 48) is "designed to, adapted to, or arranged to . . . [be] operated without influence or control by another" data generation circuitry because each does not communicate with any other. *See*, *e.g.*, IPR2014-00971, Paper 37 at 30-31; Ex. 1005 at ¶ [0039], Fig. 4; Ex. 1003 at ¶ 101. Because no signal is described as flowing from one memory interface (*e.g.*, 10A) to another (*e.g.*, 10B), the data generation circuitry of the various memory interfaces operate without influence on each other. Ex. 1005 at Fig. 4; Ex. 1003 at ¶ 101. Averbuj therefore discloses that the data generation circuitry (44, 45, and 48) of each memory interface (10, 41) is "*a data handler configured to be operated*

independently from each of the other data handlers of the plurality of data handlers." Ex. 1003 at ¶ 101.

Moreover, Petitioners observe that the "*operable independently* ..." claim language has been construed by the Board in the context of a related patent to mean "operable without influence or control by another." *See* IPR2014-00970, Paper 32 at 33. That phrase is therefore a negative limitation that is satisfied by silence in the prior art. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009); Clio USA, Inc. v. Proctor and Gamble Co., IPR2013-00448, Paper 15 at 3-4. Averbuj satisfies this claim element for this reason as well.

iii. *"configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips"*

Each data generation unit (44) and its associated circuitry (45 and 48) ("*data handler*") is "designed to" ("*configured to*") transform the generic test data signals (BIST_DATA) received from the sequencer (8) to produce modified test data signals (BIST_DATA_T) ("*generate data*"), which is applied to the memory input (RAM_DIN) for writing to the memory module ("*for writing to a corresponding one or more memory chips of the plurality of memory chips*"). Ex. 1005 at Fig. 7, ¶¶ [0049-0050], [0057]; Ex. 1003 at ¶¶ 102-103. And as explained above, Averbuj discloses that each memory module is a "*memory chip*." Ex. 1003 at ¶ 104.

Averbuj therefore discloses that the data generation circuitry (44, 45, and 48) of each memory interface (10, 41) is "*configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips*." Ex. 1003 at ¶ 104.

d. "a control circuit"

Claim 1 also requires "*a control circuit configured to generate address and control signals*." Ex. 1001 at 16:41-48 (emphasis added).

i. The "*sequencer*" constitutes "*a control circuit*"

The Board previously found that the sequencer (8) of Averbuj constitutes "*a control circuit*" as claimed because it "'*generate[s] address and control signals' for testing the memory [devices]*" and also because it is "configured to apply to the memory modules the same address and control signals received from, and produced by, the sequencers for testing . . . without modification or transformation [], directly to a memory module irrespective of its physical configuration." IPR2014-00971, Paper 37 at 41 (internal citation omitted); Ex. 1003 at ¶ 106.

Each sequencer (8) is, or at least a portion of, "*a circuit*" because each is an electronic component that receives and send electronic signals to other components. Ex. 1012 at 99; Ex. 1003 at ¶ 107. Moreover, each sequencer constitutes "*a control*" circuit because it is a circuit that is dedicated to controlling the self-test functionality of the system. Ex. 1003 at ¶ 107.

As shown in Fig. 5, each sequencer (8) receives test high-level commands (CMD_DATA) from the BIST controller and parses the high-level commands to produce its output signal (CMD_CTRL_SIGNALS). Ex. 1005 at Fig. 5, ¶¶ [0040-0041]; IPR2014-00971, Paper 37 at 41; Ex. 1003 at ¶ 108. As shown in Fig. 6, the output signal (CMD_CTRL_SIGNALS) includes test address and control signals (BIST_ADDR/CTRL), which are selected and applied to the memory module (12) during self-test mode. Ex. 1005 at Fig. 6, ¶¶ [0043-0044]; Ex. 1003 at ¶¶ 109-110. As the Board previously found, in one configuration, the test address/control signals (BIST_ADDR/CTRL) are provided to the memory modules (12) "without modification or transformation . . . , directly to a memory module, irrespective of its physical configuration." IPR2014-00971, Paper 37 at 41 (citing Ex. 1005 at ¶ [0056]). Thus, the sequencer produces (*i.e.*, brings into existence) address and control signals that are actually applied to the memory modules during self-testing. Ex. 1003 at ¶ 111. Therefore, the sequencer is "*a control circuit configured to generate address and control signals*." IPR2014-00970, Paper 37 at 41 (emphasis added); Ex. 1003 at ¶ 112.

ii. The "*address generation units*" constitute "*a control circuit*"

Alternatively, the address generation unit (42) of the memory interface (41) disclosed in Averbuj also constitutes "*a control circuit*" as claimed because it too can produce (*i.e.*, "*generate*") address and control signals as needed, as the Board

also recognized, and the Patent Owner conceded, in IPR2014-00971. IPR2014-00971, Paper 37 at 40-41. Ex. 1003 at ¶ 113.

In another configuration, the address generation unit of a memory interface generates test address and control signals by transforming or modifying the test address and control signals (BIST_ADDR/CTRL) received from the sequencer (8). Ex. 1005 at ¶ [0051] (". . . address generation unit 42 transforms the address provided by sequencer . . ."), ¶ [0052] (". . . [e]ach memory interface . . . transforms the received address **as needed** …") (emphasis added), Figs. 6, 10; Ex. 1003 at ¶¶ 115-117. Hence, the address generation unit (42) of the memory interface (41) also constitutes "*a control circuit configured to generate address and control signals*." IPR2014-00971, Paper 37 at 40-41; Ex. 1003 at ¶ 118.

iii. The "*sequencer*" and the "*address generation units,*" combined, constitute "*a control circuit*"

As a further alternative, the sequencer (8) and the address generation units (42) of each device block, combined, constitute "*a control circuit*" as claimed. Ex. 1003 at ¶ 119. As set forth above, each generates address and control signals in different circumstances or configurations. IPR2014-00971, Paper 32 at 41-42; *see* § VI.A.1.d.i-ii, above. Further, the sequencer (8) and the address generation units (42) of each device block are operatively coupled to each other so as to provide that functionality. *E.g.*, Ex. 1005 at Figs. 1, 4; Ex. 1003 at ¶ 119. And the sequencer and the address generation units of each device block are "a

combination of electrical components interconnected to perform a particular task" of generating address and control signals for their corresponding memory modules, and are therefore a "*circuit*." Ex. 1012 at 99; Ex. 1003 at ¶ 119. Therefore, the sequencer and the address generation units, as a whole, are also "*a control circuit configured to generate address and control signals*." Ex. 1003 at ¶ 120.

e. "wherein the memory system is configured to test the one or more memory chips"

Claim 1 requires that "*the memory system is configured to test the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the one or more data handlers*." Ex. 1001 at 16:48-51 (emphasis added).

During self-test mode, after the test data is written to a memory module (12), the memory interface (41) may read data from the same addresses of the memory module (12). Ex. 1005 at ¶ [0053], Fig. 6; Ex. 1003 at ¶ 122. The comparator (48) in the memory interface (41) compares the read-out data to the write data to determine if they are identical. Ex. 1005 at ¶ [0053], Figs. 6, 10; Ex. 1003 at ¶ 122. This comparison constitutes a "*test*" of the memory modules as it tests for errors in the memory module. Ex. 1005 at Fig. 10; ¶ [0053]; Ex. 1003 at ¶ 123.

Averbuj therefore discloses this claim element. Ex. 1003 at ¶ 124.

2. Averbuj Anticipates Claim 4

Claim 4 requires that "*the memory system [of claim 1] comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers*." Ex. 1001 at 16:61-65 (emphasis added).

Averbuj discloses that BIST units are "commonly incorporated into memory chips and other integrated circuits." Ex. 1005 at ¶ [0003]. Because the memory interfaces are part of a BIST unit, Averbuj also discloses the memory interface (10, 41) is commonly incorporated into (memory or other) chips, or "*integrated circuits*." Ex. 1012 at 98, 277; Ex. 1003 at ¶ 126. Averbuj further discloses that the device block (6) and the components contained therein, such as the sequencer (8) and the memory modules (12), are "distributed" and "located throughout an electronic device," *i.e.*, physically separated. *See e.g.*, Ex. 1005 at ¶¶ [0013], [0015]; Ex. 1003 at ¶ 127. Since memory interfaces (10, 41) are also components of each device block (6), at a minimum, the different sets of memory interfaces (10, 41) belonging to different device blocks (6) must also be physically separated. Ex. 1003 at ¶ 127. Averbuj also discloses that the various integrated circuits or chips of an electronic device are "mounted on a circuit board," indicating that the integrated circuits and chips comprising the electronic device are **packaged** integrated circuits or chips. Ex. 1005 at ¶ [0005]; Ex. 1016 at 1:15-27; Ex. 1003 at

¶ 128. Therefore, Averbuj discloses that the memory interfaces (each containing a "*data handler*") of different device blocks (which comprise a "*memory system*") must be distributed across "*at least two physically separate integrated circuit packages*." Ex. 1003 at ¶ 129.

Therefore, Averbuj discloses this claim element. Ex. 1003 at ¶ 130.

B. Averbuj Renders Claims 1 and 4 Obvious

Patent Owner may also argue that claims 1 and 4 are not anticipated by Averbuj, for various reasons. Even if one were to accept such arguments, claims 1 and 4 as a whole would have been obvious over Averbuj.

1. Averbuj Renders Claim 1 Obvious

a. "memory controller"

To the extent one might argue that Averbuj does not disclose "*a memory system configured to be operatively coupled to a memory controller of a computer system*" and that preamble is found to be limiting, it would have been obvious to include it in the system of Averbuj.

Averbuj discloses that his electronic device can be a "computer [or] server" that incorporates a variety of memory modules, such as DRAM and Flash memory. Ex. 1005 at ¶ [0032]; Ex. 1003 at ¶ 132. Averbuj discloses that the device blocks ("*memory system*") in his electronic system receives address/control signals (ADDR/CTRL) and data signals (DATA) from a programmable processor and

applies those signals under normal operating conditions. Ex. 1005 at ¶ [0048], Figs. 5, 6; Ex. 1003 at ¶ 132.

At the time, memory controllers were commonly used in computers and servers in order to manage access to the memory systems. *See e.g.*, Ex. 1008 at 316-17 (showing a "Memory Controller" on Fig. 7.2); Ex. 1011 at Figs. 1 & 2 (showing "Memory Hub Controller" and "Memory Controller"); Ex. 1023 at Fig. 1 (showing a "Memory Controller"); Ex. 1024 at Fig. 1 (showing a "Common Memory Controller"); Ex. 1003 at ¶ 133. Thus, to use a memory controller to manage memory accesses in the system of Averbuj by providing the device blocks with address, control, and data signals would have been the use of known techniques and structures in their known ways to achieve the predictable result of accessing memory. Ex. 1003 at ¶ 133.

A skilled artisan would have been motivated to use a memory controller with the device of Averbuj for a number of reasons. A memory controller could relieve the main processor of the burden of complying with the complex interface protocols and requirements of the memory system and thus improve the overall performance of a computer or server. *See e.g.*, Ex. 1008 at 497-98; Ex. 1003 at ¶ 134. A memory controller could also efficiently arbitrate and schedule simultaneous requests by multiple components to access the memory system and therefore avoid resource scheduling conflicts and improve throughput, especially

in a multi-processor environment. Ex. 1008 at 328, Figure 13.1 ; Ex. 1003 at ¶ 135. For these reasons, a skilled artisan would have been motivated to include a memory controller in a computer or server, such as the computer or server contemplated in Averbuj. Ex. 1003 at ¶ 136.

Thus, it would have been obvious to design, arrange, or adapt ("*configure*") the memory modules and the device blocks of Averbuj such that they would be or be capable of being "*operatively coupled to a memory controller of a computer system.*" Ex. 1003 at ¶ 137.

b. "memory chip"

To the extent one might argue that Averbuj does not disclose "*a plurality of memory chips,*" it would have been obvious to implement the plurality of memory modules of Averbuj as memory chips.

Averbuj discloses that electronic devices were constructed from many integrated circuits and chips, including memory chips. Ex. 1005 at ¶¶ [0005-0006]; Ex. 1003 at ¶ 139. Further, an object of Averbuj is to improve the conventional BIST units that were "incorporated into memory chips" in electronic devices. *See* Ex. 1005 at ¶ [0003]; Ex. 1003 at ¶ 139. As such, it would have been obvious to a skilled artisan that the memory modules (12) of Averbuj would be "*memory chips*." Ex. 1003 at ¶ 139.

The term "*memory chip*" refers to memory implemented using integrated circuits. *See* Ex. 1012 at 98, 277 (defining "chip" and "integrated circuit" as synonyms). Memory in computer systems around the priority date of the '501 Patent, *e.g.*, DRAMs, was available almost exclusively in the form of integrated circuits; and due to low cost and widespread use and availability, a skilled artisan would have invariably used integrated circuit memory in designing a computer or a server. Ex. 1008 at 457-58; Ex. 1003 at ¶ 140.

Therefore, it would have been obvious that the memory modules of Averbuj's electronic devices are "*a plurality of memory chips*." Ex. 1003 at ¶ 141.

2. Averbuj Renders Claim 4 Obvious

To the extent one might argue that Averbuj does not sufficiently disclose "*the memory system [of claim 1] comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers,*" it would have been obvious to include it in Averbuj.

It was known in the art to include circuit components of a memory system, including those components responsible for handling the transfer of data to and from a memory device, in physically separate integrated circuit packages, and to do so would have been well within the average skill in the art. *See, e.g.*, Ex. 1006 at Fig. 9A; ¶¶ [0052-0053] (explaining that the depicted separate "buffer devices"

are in one embodiment "housed in separate packages"); ¶ [0029] (noting that as used therein "an integrated circuit buffer device is also referred to as a buffer or buffer device."); Ex. 1003 at ¶ 143. To employ that technique in the system of Averbuj would therefore have been the use of a known technique for its known purpose and would have achieved only predictable results, such as the protection of integrated circuits by the packaging. Ex. 1003 at ¶ 143.

Moreover, a skilled artisan would have been motivated to use physically separate integrated circuit packages for the data handlers of Averbuj in at least two different ways. Ex. 1003 at ¶ 144.

A skilled artisan applying the teachings of Averbuj to improve a preexisting, conventional BIST unit and memory chip would have been motivated to retain the memory interface (or the equivalent circuitry) within each memory chip of a memory module. Ex. 1003 at ¶ 145. Memory modules at the time, such as DRAM modules, comprised of a plurality of packaged memory chips mounted on different portions of a printed circuit board. *See e.g.*, Ex. 1013 at Fig. 1; Ex. 1014 at 1; Ex. 1003 at ¶ 146. Averbuj explains, and prior references confirm, that it was common to place BIST units in each memory chip. Ex. 1005 at ¶ [0003]; Ex. 1010 at Fig. 2; Ex. 1003 at ¶¶ 147-148. The common BIST functions were thus redundantly duplicated in each conventional memory chip of a memory module. Ex. 1003 at ¶ 149. Averbuj discloses and teaches that such redundant BIST circuitry can be

reduced or eliminated if the circuitry that provides common functions, *e.g.*, BIST controller, are taken out of each memory chip and centralized or merged into a single component. Ex. 1005 at ¶ [0008]; Ex. 1003 at ¶ 149.

Averbuj, however, does not disclose or teach taking out of each memory chip portions of the BIST units that are not redundant. In particular, Averbuj acknowledges that each memory interface is particularized to meet the specific needs of each memory chip it services, and is therefore not redundant. Ex. 1005 at ¶¶ 11, 49-50; Ex. 1003 at ¶ 150.

A skilled artisan that seeks to reduce the redundant BIST circuitry of conventional memory chips and BIST units would have been motivated to modify the conventional design in such a way as to minimize the modifications to the conventional design. Ex. 1003 at ¶ 151. Specifically, a skilled artisan would have understood that the BIST controller and sequencer portions of conventional BIST units would need to be removed from each memory chip and combined in order to reduce redundant circuitry. Ex. 1003 at ¶ 151. However, a skilled artisan would also have understood and recognized that the memory interface portions need not be excised and implemented as a separate chip since doing so would not reduce much, if any, circuitry. Ex. 1003 at ¶ 151. Hence, a skilled artisan would have been motivated to avoid unnecessary design changes by keeping the original design with respect to the memory interface portion—*i.e.*, retain the memory

interfaces (each of which includes a "*data handler*") within each memory chip that was separately packaged and mounted on a printed circuit board of a memory module ("*physically separate integrated circuit packages*."). Ex. 1003 at ¶ 152.

Alternatively, a skilled artisan, particularly a skilled artisan looking to implement Averbuj's BIST circuitry in a memory module that does not have a BIST circuitry, would have been motivated to incorporate each component of Averbuj's BIST circuitry—*i.e.*, BIST controller, sequencers, and memory interfaces—into separate integrated circuit chips/packages. Ex. 1003 at ¶ 153. This design approach had already been proposed and/or practiced by others (*see e.g.*, Ex. 1006 at Figs. 9A-C), and thus a skilled artisan would have been motivated to try this approach. Ex. 1003 at ¶ 154. This alternative approach is equally consistent with the teachings of Averbuj in that it still combines redundant BIST circuitry together. Ex. 1003 at ¶ 155. Keeping each memory interface (and each other component of Averbuj's BIST circuitry) in separate chips/packages provides a number of benefits, that would motivate a skilled artisan, including: (1) reduction of the busing area of the chips/packages (Ex. 1017 at 3:45-53; Ex. 1003 at ¶ 156); (2) reduction of load on the chips/packages (Ex. 1018 at 1:5-23, Fig. 3; Ex. 1019 at 1:32-2:3, Fig. 5; Ex. 1013 at ¶ 157); (3) reduction of signal line capacitance affecting data transmission rates (Ex. 1020 at 2:27-3:6; Ex. 1003 at ¶ 158); (4) reduction of signal crosstalk affecting signal integrity (Ex. 1010 at 23-25, 207; Ex.

1003 at ¶ 158); and (5) simplification of PCB routing (Ex. 1021 at 6; Ex. 1003 at ¶ 158). In addition, keeping the memory interfaces and other components of Averbuj's BIST circuitry in separate integrated circuit packages allows for efficient maintenance and repair since only the packages that require repair or upgrade need be replaced. Ex. 1003 at ¶ 159. For these reasons, a skilled artisan would have been motivated to keep the memory interfaces (each of which includes a "*data handler*") in separately packaged integrated circuits or chips ("*physically separate integrated circuit packages*."). Ex. 1003 at ¶ 160.

Accordingly, claim 4 would have been obvious to a skilled artisan over Averbuj. Ex. 1003 at ¶ 161.

C. Averbuj in View of Tsern Renders Claim 4 Obvious

Patent Owner may also argue that claim 4 is neither anticipated nor rendered obvious by Averbuj, for various reasons. Even if one were to accept such arguments, claim 4 as a whole would have been obvious over Averbuj in view of Tsern.

Tsern discloses a memory module including a number of memory devices, such as DRAM or SRAM devices (Ex. 1006 at ¶ [0035]), and a number of buffer devices. *See, e.g.*, Ex. 1006 at ¶¶ [0033-0042], [0052-0059], Figs. 1 & 9. Tsern discloses that these buffer devices are each associated with and interface with one or more memory devices. Ex. 1006 at ¶ [0033]; Ex. 1003 at ¶ 163.

Tsern further discloses that these buffer devices at least in some embodiments do not exchange signals and therefore operate independently of each other. *See, e.g.*, Ex. 1006 at ¶¶ [0033-0042], [0052-0059]; Figs. 1 & 9. Tsern further discloses this these buffer devices are coupled to data ports of the associated memory devices for purposes of writing data, including test data, into those memory devices. *See, e.g.*, Ex. 1006 at ¶¶ [0077-0101]; Fig. 18. The Tsern buffer devices are therefore "*data handlers*" as claimed, or at least very similar to such circuits. Ex. 1003 at ¶ 164.

Tsern further discloses that his buffer devices may be separate integrated circuit devices that can be housed in separate packages. Ex. 1006 at ¶ [0031] ("Likewise in an embodiment, an integrated circuit buffer device is distinguished from a buffer die in that a buffer die is a monolithic integrated circuit formed from semiconductor materials and performs at least one or more buffer functions described herein, *whereas an integrated circuit buffer device is a buffer die having at least some form of packaging or interface that allows communication with the buffer die*.") (emphasis added.); *see also id*. at ¶ [0053] ("In an embodiment, each memory device and buffer device are housed in separate packages."); ¶ [0043] ("packages used to house buffer devices **100*a*** and **100*d***"); Ex. 1003 at ¶ 165.

Tsern therefore discloses a "*memory system . . . compris[ing] at least two physically separate integrated circuit packages, wherein each of the at least two*

physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers".

It would have been obvious to include the "separate integrated circuit packages" configuration of Tsern, including the distribution of self-test circuitry, in the system of Averbuj for several reasons. First, to do so would have been merely the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement. Tsern demonstrates that, before the priority date of the '501 Patent, it was within the average skill of the art to include a plurality of data handler circuits in physically separate integrated circuit packages, on a printed circuit board and that such circuits would operate as expected. Ex. 1003 at ¶ 167.

A skilled artisan would have been further motivated to implement the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj, particularly for the memory interfaces of Averbuj, in order to reduce the busing area a centralized approach would require. *See*, *e.g.*, Ex. 1017 at 3:45-53; Ex. 1003 at ¶ 168.

A skilled artisan also would also have been motivated to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj so that the self-test circuitry could be conveniently placed in the same packaging as buffer circuitry used to access and isolate different portions of the

memory array. By the priority date of the '501 Patent it was known that separate buffers, in separate packages, for different portions of the memory array could advantageously reduce the load experienced by the memory controllers and improve the memory timing. Ex. 1018 at 1:5-23, Fig. 3; Ex. 1019 at 1:32-2:3, Fig. 5. A skilled artisan would therefore have been motivated to place the sequencers and the memory interfaces of Averbuj within such buffer components in order to reduce the load on the memory controller and also improve memory timing. Ex. 1003 at ¶ 169.

A skilled artisan also would have been motivated to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj so that failing sequencers and memory interface components could be easily replaced, by simply replacing a standard package on the printed circuit board, without the necessity to replace other self-test circuitry in other packages that was operating normally. Ex. 1003 at ¶ 170.

A skilled artisan also would have been motivated to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj in order to place each data handler at positions on the PCB close and perhaps closest to its associated memory. Doing so would (i) simplify the wiring plan on the circuit board (Ex. 1021 at 6); (ii) reduce EMI interference and improve signal integrity (Ex. 1010 at 23-24, 207); and (iii) limit the capacitive load on those lines

and permit faster and more efficient data transmission (Ex. 1020 at 2:27-3:6). *See* above at § V.C.1; Ex. 1003 at ¶ 171.

Claim 4 is therefore obvious over Averbuj in view of Tsern. Ex. 1003 at ¶ 172.

VII. CONCLUSION

Because the information presented in this petition shows that there is a reasonable likelihood that the Petitioners would prevail with respect to at least one of the claims challenged in the petition, the Petitioners respectfully request that a Trial be instituted and that claims 1 and 4 of the '501 Patent canceled as unpatentable.

Dated: January 3, 2017

Respectfully Submitted,

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 8,359,501

Attachment A:
Proof of Service of the Petition

CERTIFICATE OF SERVICE

I hereby certify that on January 3, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

Jamie J. Zheng
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Dated: January 3, 2017

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 8,359,501

Attachment B:
List of Evidence and Exhibits Relied Upon in Petition

Exhibit #	Reference Name
1001	U.S. Patent No. 8,359,501
1002	File History of U.S. Patent No. 8,359,501
1003	Declaration of Dr. Pinaki Mazumder
1004	Curriculum Vitae of Dr. Pinaki Mazumder
1005	U.S. Patent Publication No. 2005/0257109 to Averbuj ("Averbuj")
1006	U.S. Patent Publication No. 2007/0070669 to Tsern ("Tsern")
1007	Excerpts from the American Heritage College Dictionary, 3d Ed.
1008	Jacob *et al.*, "Memory Systems," 1d Ed.
1009	Catsoulis, "Designing Embedded Hardware," 2d Ed.
1010	Montrose, "EMC and the Printed Circuit Board"
1011	U.S. Patent No. 7,210,059 to Jeddeloh
1012	Excerpts from the Microsoft Computer Dictionary, 5th Ed.
1013	Micron MT8JTF12864A DDR3 SDRAM UDIMM Specifications
1014	JEDEC PC2-5300 RDIMM Assembly V310 (Sept. 2, 2005), available at https://www.jedec.org/sites/default/files/docs/design/DDR2/PC2-5300_RDIMM_V310_RC_P0_20050221.zip
1015	JEDEC PC2-5300 RDIMM PCB Layout (Sept. 2, 2005), available at https://www.jedec.org/sites/default/files/docs/design/DDR2/PC2-5300_RDIMM_V310_RC_P0_20050221.zip
1016	U.S. Patent No. 6,271,060 to Zandman
1017	U.S. Patent No. 6,011,748 to Lepejian
1018	U.S. Patent No. 6,639,820 to Khandekar
1019	U.S. Patent No. 6,317,352 to Halbert

Exhibit #	Reference Name
1020	U.S. Patent No. 6,011,710 to Wiggers
1021	Micron, Technical Note 4720: (Point-to-Point) Package Sizes and Layout Basics, Rev. A, 2006
1022	U.S. Patent No. 6,108,798 to Heidel
1023	U.S. Patent No. 3,588,831 to Figueroa
1024	U.S. Patent No. 3,618,041 to Horikoshi