**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner

Patent No. 8,001,434
Issued: August 16, 2011
Filed: April 13, 2009
Inventors: Hyun Lee, Jayesh Bhakta, Soonju Choi
Title: MEMORY BOARD WITH SELF-TESTING CAPABILITY

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*Inter Partes* Review No. IPR2017-00561

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# PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,001,434 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123

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**Attachment A. Proof of Service of the Petition**
**Attachment B. List of Evidence and Exhibits Relied Upon in Petition**

## I. INTRODUCTION

This Petition seeks cancellation of claims 1-7 of U.S. Patent No. 8,001,434 ("the '434 Patent") based, primarily, on U.S. Patent Application Publication No. 2005/0257109 to Averbuj ("Averbuj"). The Board has previously found numerous claims of the 434 Patent, and its child, unpatentable based on Averbuj. *See* IPR2014-00971, Paper 37 and IPR2014-00970, Paper 32. This Petition is based primarily on the analysis accepted by the Board in those prior proceedings. Indeed, there is nothing in the challenged claims here that could distinguish them from Averbuj under the Board's previous analysis, so those claims are also unpatentable.

However, the Petition also adds to that analysis and strengthens it. For example, Petitioners address arguments that Patent Owner may raise by proposing additional grounds that more closely satisfy the claim limitations to which such arguments would be directed. Such additional grounds are not redundant because they are "rational, narrowly targeted, and not burdensome considering only [two] claims with very similar limitations are at issue." IPR2015-01912, Paper 10 at 17-18. Petitioners therefore respectfully request that trial be instituted on all grounds and arguments advanced herein.

# II. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR *INTER PARTES* REVIEW

## A. Mandatory Notices

### 1. Real Parties In Interest

The real parties of interest of this petition are the Petitioners: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

### 2. Related Matters

U.S. Patent No. 8,001,434 ("the '434 Patent") relates to the following legal proceedings: *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 4:13-cv-05889-YGR (N.D. Cal.); *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 2:13-cv-02613-TLN (E.D. Cal.); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No. IPR2014-00970 (PTAB); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No. IPR2014-00971 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01372 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01373 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01374 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01375 (PTAB); *Netlist, Inc. v. SanDisk LLC et al.*, Case Nos. 16-2274, -2338, -2339 (Fed. Cir.); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 16-2666 (Fed. Cir.); *Netlist, Inc. v. SK hynix Inc. et al.*, Case No. 8:16-cv-01605-JLS (C.D. Cal.); and *In re Certain memory modules & Components Thereof*, Inv. No. 337-TA-1023 (ITC).

In addition, petitions for *inter partes* review of U.S. Patent Nos. 8,359,501 and 8,689,064, which are related to the '434 Patent, are being filed concurrently with this petition.

### 3. Lead & Backup Counsel

Lead Counsel is Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492. Backup Lead Counsel are: Steve Baik (Reg. No. 42,281), Sidley-SKH-IPR@sidley.com, 650-565-7016, Wonjoo Suh (Reg. No. 64,124), Sidley-SKH-IPR@sidley.com, (202) 736-8831, and Ryuk Park (*pro hac vice* to be requested), Sidley-SKH-IPR@sidley.com, 650-565-7074.

### 4. Service Information

Service on Petitioners may be made by e-mail (Sidley-SKH-IPR@sidley.com), or by mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

## B. Fee for *Inter Partes* Review (37 C.F.R. § 42.15(a))

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 50-1597.

## C. Certification of Word Count (37 C.F.R. § 42.24(a)(1))

Petitioners certify that this petition for *inter partes* review contains 13,631 words, excluding the parts of that are exempted by 37 C.F.R. § 42.24(a)(1), per the count of the word-processing system used to prepare this petition.

### D. Certification of Standing (37 C.F.R. § 42.104(a))

Petitioners certify they are not barred or estopped from requesting *inter partes* review of the ’434 Patent (Ex. 1001). This petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of the ’434 Patent. Neither Petitioners nor any party in privity with Petitioners has filed a civil action challenging the validity of any claim of the ’434 Patent. The ’434 Patent has not been the subject of a prior *inter partes* review by Petitioner or a privy of Petitioners. Petitioners therefore certify this patent is available for *inter partes* review.

### E. Proof of Service (37 C.F.R. §§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

## III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Claims 1-7 of the '434 Patent are unpatentable as follows:

1. Claims 1-7 of the '434 Patent are unpatentable as anticipated under 35 U.S.C. § 102 by U.S. Patent Publication No. 2005/0257109 by Averbuj ("Averbuj");
2. Claims 1-7 of the '434 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Averbuj; and
3. Claims 1-7 of the '434 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Averbuj in view of U.S. Patent Publication No. 2007/0070669 by Tsern ("Tsern").

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ IV-VI, below. The evidence relied upon in this petition is listed in **Attachment B**.

## IV. RELEVANT INFORMATION CONCERNING THE '434 PATENT

### A. Effective Filing Date of the '434 Patent

The application that resulted in the '434 Patent is U.S. Patent Application Serial No. 12/422,925, filed April 13, 2009. Ex. 1001 at Face. The '434 Patent claims priority to Provisional Application Nos. 61/044,801, 61/044,825, and 61/044,839, filed on April 14, 2008. *Id.* Patent Owner contended, in a related proceeding, that the conception date of the '434 Patent is June 21, 2007. While Petitioners disagree with Patent Owner's assertion of an earlier conception date,

Petitioners will assume, solely for the purpose of this proceeding, that the claims of the ’434 Patent have an effective filing date of June 21, 2007.

### B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the ’434 Patent would have been someone with “a Bachelor’s degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST.” IPR2014-00970, Paper 32 (Final Written Decision) at 10-11; IPR2014-00971, Paper 37 (Final Written Decision) at 10-11; Ex. 1003 ¶ 51.

### C. Overview of the ’434 Patent

The ’434 Patent discloses a self-testing memory module for testing a plurality of memory devices using a control module that generates test address and control signals, and a data module comprising a plurality of data handlers that generate test data signals. Ex. 1001 at Abstract. An illustrative example is shown in FIG. 2, as reproduced below. Ex. 1003 ¶ 52.

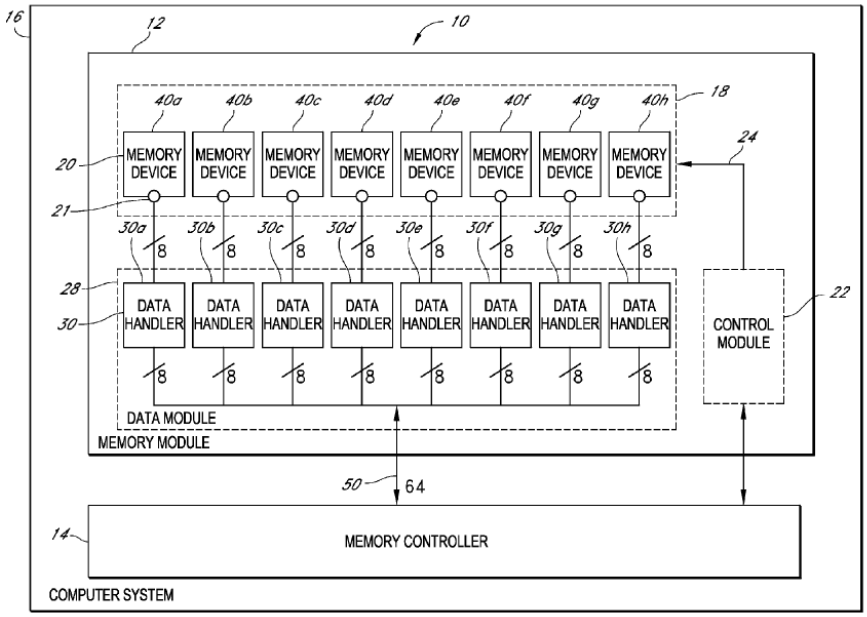



FIG. 2

**Ex. 1001 at FIG. 2.**

As shown in FIG. 2, the memory module (12) includes a control module (22) and a data module (28) that are connected to an array of memory devices (20). The control module (22) generates the address and control signals for testing the memory devices. Ex. 1001 at 5:7-9, FIGS. 2-3; Ex. 1003 ¶ 53. The data module (28) generates test patterns to write to the memory devices (20) and checks the data patterns read or received back from the memory devices (20) for agreement with corresponding data patterns that are expected to be read back from the memory devices. Ex. 1001 at 5:22-28, FIGS. 2-3; Ex. 1003 ¶ 53.

The data module (28) includes a plurality of data handlers (30) that are each located in proximity to a corresponding memory device (20), as illustrated in FIG. 2. Ex. 1001 at 9:13-22, FIGS. 2-3; Ex. 1003 ¶ 54. Each data handler (30) is

operable independently from each of the other data handlers (30) in that each data handler (30) is configured to write to and/or read from the corresponding plurality of data ports of one or more of the memory devices (20) without being in communication with any of the other data handlers (30) or other data ports of the memory devices (20). Ex. 1001 at 8:1-32; Ex. 1003 ¶ 54.

### D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 C.F.R. § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See Notice of Practice Guide*, 77 Fed. Reg. 48,756, 48,764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

The Board has previously interpreted certain claim terms of the '434 Patent in prior IPR proceedings. For the purposes of this proceeding only, Petitioner adopts the Board's interpretations and therefore applies those same interpretations, as set forth below:

#### 1. ***"self-testing memory module"*** **(claims 1-7)**

The Board has previously concluded that the broadest reasonable interpretation of "*self-testing memory module*" includes "a memory module that

can be tested, at a minimum with only internal, or both internal and external test equipment." *See* IPR2014-00970, Paper 32 at 33. This is consistent with the '434 Patent's disclosure. *See, e.g.*, Ex. 1001 at 3:52-54, 13:65-67.

**2. *"operable independently"* (claim 1)**

The Board has previously concluded that the broadest reasonable interpretation of "*operable independently*" is "operable without influence or control by another." *See* IPR2014-00970, Paper 32 at 33. This is consistent with the '434 Patent's disclosure. *See, e.g.*, Ex. 1001 at Abstract, 5:11-18, 8:1-11, 8:19-32.

**3. *"configured to"* (claims 1, 7)**

The Board has previously concluded that the broadest reasonable interpretation of "*configured to*" is "designed to, adapted to, or arranged to [e.g., perform a function or be capable of performing a function]." *See* IPR2014-00970, Paper 32 at 20-24, 33. This is consistent with the '434 Patent's disclosure and skilled artisans' understanding and usage of the term. *See, e.g.*, Ex. 1001 at 7:21-27; Ex. 1007 at 292 (dictionary definition of "configure"). Further, Patent Owner's expert, Dr. Sechen, previously offered testimony supporting the Board's construction. *See* IPR2014-00970, Paper 32 at 24 ("Dr. Sechen testified that 'configured to' in the context of the phrase 'configured to be operatively coupled … might mean designed [to].'").

**4. *"generate"* (claim 1)**

The Board has previously concluded that the broadest reasonable interpretation of "*generate*" is "produce." *See* IPR2014-00970, Paper 32 at 24-33. This is consistent with the '434 Patent's disclosure. *See, e.g.*, Ex. 1001 at 5:43-50, 6:6-12, 9:25-27, 10:27-33.

**5. *"proximate to"* (claim 5)**

The Board has not previously interpreted the phrase "*proximate to*". However, the broadest reasonable construction of that phrase is "close."

The patent specification and the claims supports this interpretation. The '434 Patent explains that:

> In certain embodiments, each of the plurality of data handlers **30** is positioned on the PCB **12** proximate to the corresponding plurality of data ports. For example, each data handler **30** of certain embodiments is positioned closer to the corresponding plurality of data ports **21** than the data handler **30** is to the other data ports **21** of the plurality of memory devices **18**. For example, the data handler **30a** is positioned closer to the corresponding plurality of data ports **21** of the memory device **40a** than to the other data ports **21** of the other memory devices **40b-40h**.

Ex. 1001 at 9:13-22.

While this passage discloses placing one data handler "closer" to its associated data handler than another data handler, the patent merely cites that as an "example" of positioning the data handlers "proximate" to their associated memory device data ports.

The passage quoted above further discusses the data handlers of FIG 2, which are fairly described as being close to their associated memory devices:

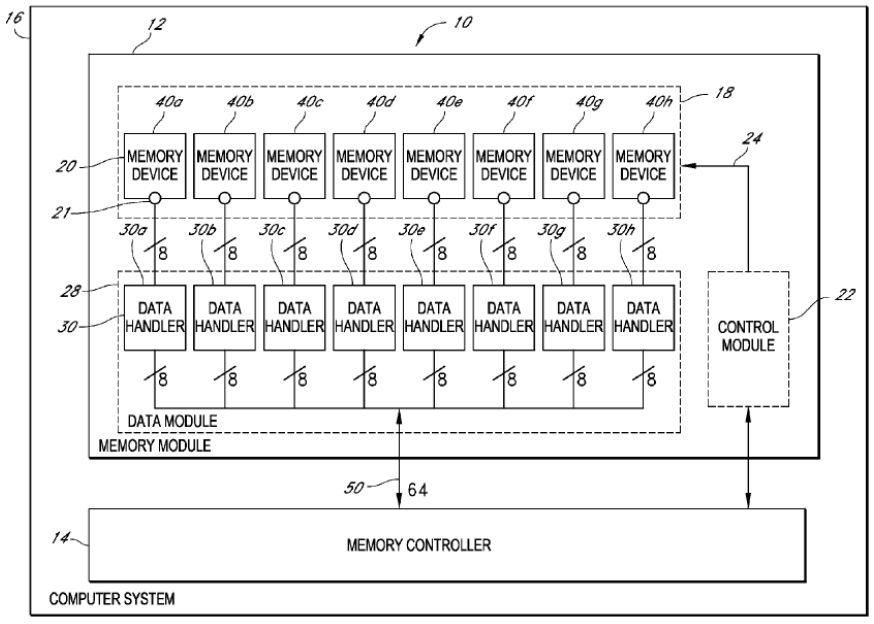



FIG. 2

**Ex. 1001 at FIG. 2.**

Moreover, claim 6, which depends from claim 5, further requires that the data handlers be "*positioned **closer** to the corresponding plurality of data ports than to the other data ports of the plurality of memory devices*." Ex. 1001 at 16:66-17:2 (claim 6) (emphasis added). A dependent claim (such as claim 6) must further limit the claim from which it depends (such as claim 5). 35 U.S.C. §

112(d). A person of ordinary skill in the art reading the claims would understand that the term "*proximate to*" (which is recited in claim 5) is broader than the term "*closer*" (which is recited in claim 6). This further supports an interpretation of "proximate to" to mean "close."

Evidence extrinsic to the patent documents also supports the interpretation of "*proximate to*" as close. The ordinary definition of the word "proximate" is "very near" or "close." Ex. 1007 at 1102.

In light of the intrinsic record and the extrinsic evidence, the broadest reasonable interpretation of "***proximate to** the corresponding plurality of data ports*" is "**close to** the corresponding plurality of data ports." Ex. 1003 ¶¶ 64-70.

## V. OVERVIEW OF THE PRIOR ART

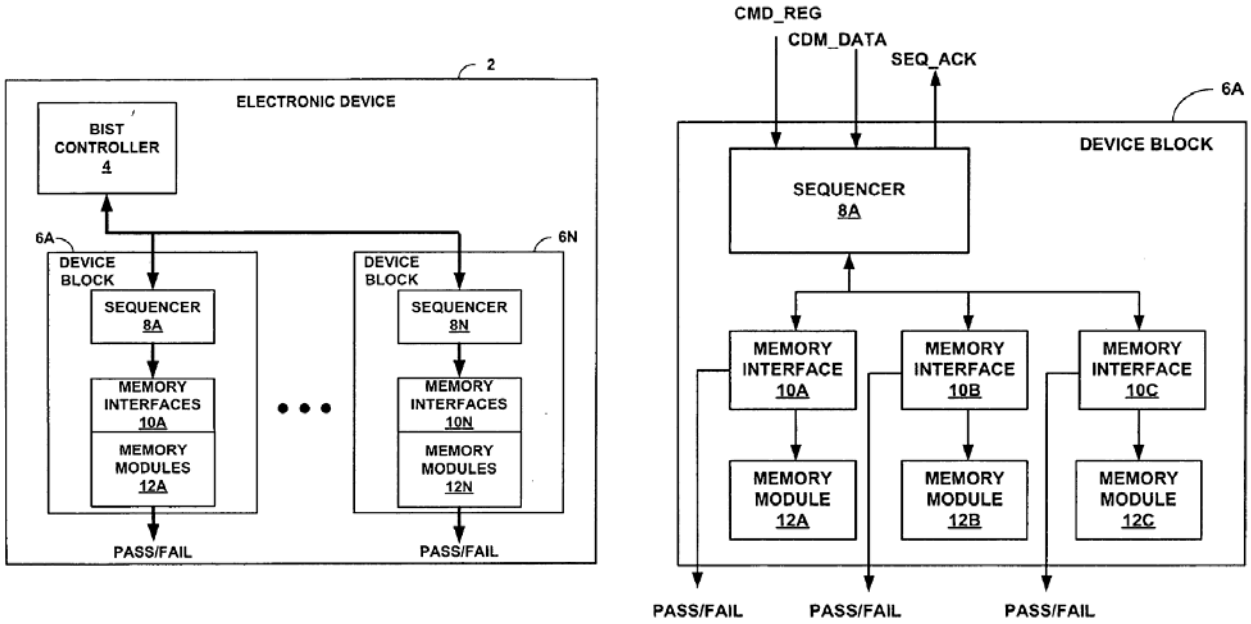
### A. U.S. Patent Publ. No. 2005/0257109 to Averbuj (Ex. 1005)

United States Patent Publication No. 2005/0257109 to Averbuj ("Averbuj"; Ex. 1005) was filed on July 29, 2003 and published on November 17, 2005. Ex. 1005 at Face. Averbuj is thus prior art to the '434 Patent pursuant to 35 U.S.C. §§ 102 (a), (b), and (e).

Averbuj is titled "Built-In Self Test (BIST) Architecture Having Distributed Interpretation and Generalized Command Protocol" and generally directed to a built-in self test ("BIST") architecture for memory modules in electronic devices.

More particularly, Averbuj discloses an improved BIST architecture for reducing redundant circuitry. Ex. 1005 at ¶¶ [0007-0008], FIG. 1; Ex. 1003 ¶ 72.

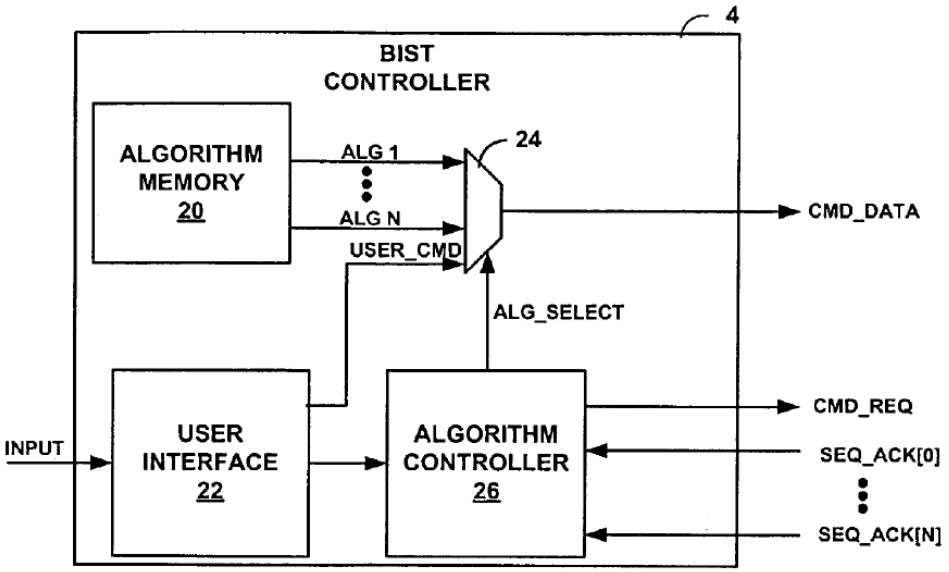
Averbuj explains that BIST units at the time were commonly incorporated into each memory chip and memory module of an electronic device. Ex. 1005 at ¶¶ [0003-0005]; Ex. 1003 ¶ 73. Having a fully-integrated BIST unit in each memory chip or module created redundant circuitry since some of the functions performed by the BIST units, such as providing test algorithms, were common to many or all of the memory chips and modules. Ex. 1005 at ¶ [0008]; Ex. 1003 ¶ 73.




**Ex. 1005 at FIGS. 1 (left) & 4 (right).**

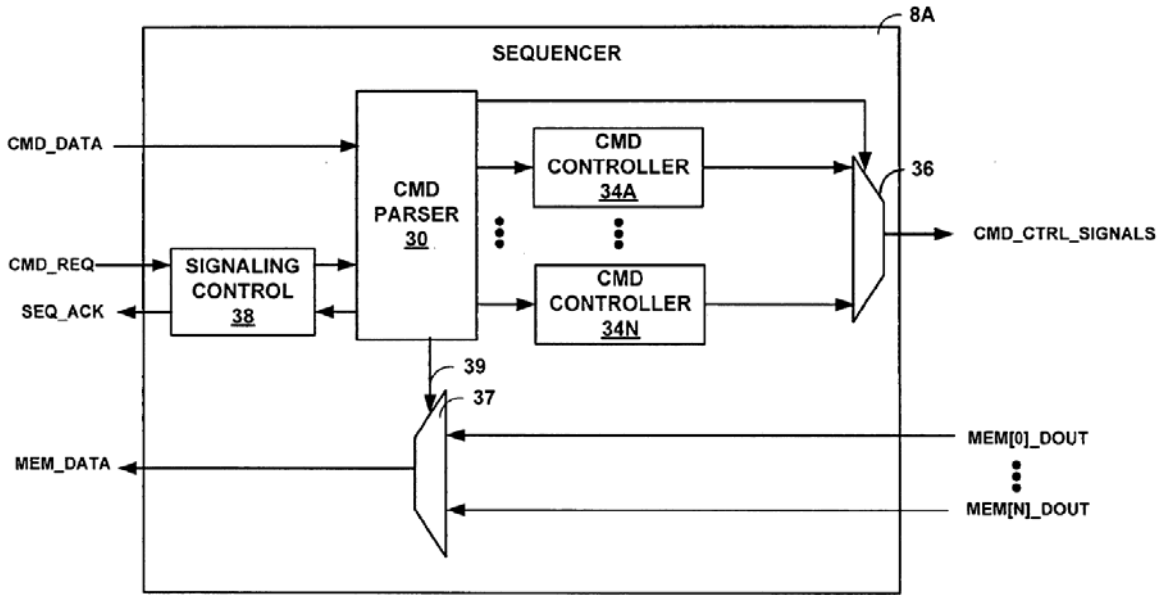
Averbuj's proposed solution was a distributed BIST architecture with a hierarchy that reduces the redundancies. Ex. 1005 at ¶ [0008]; Ex. 1003 ¶ 74. As shown in FIG. 1 of Averbuj, at the top of the hierarchy is a single, centralized

BIST controller which provides high-level algorithms or test patterns to all of the memory modules of an electronic device. Ex. 1005 at FIG. 1, ¶ [0008]; Ex. 1003 ¶ 75. The BIST controller reduces redundancy because the "common test patterns need not be redundantly stored within memory modules." Ex. 1005 at ¶ [0008]; Ex. 1003 ¶ 75.



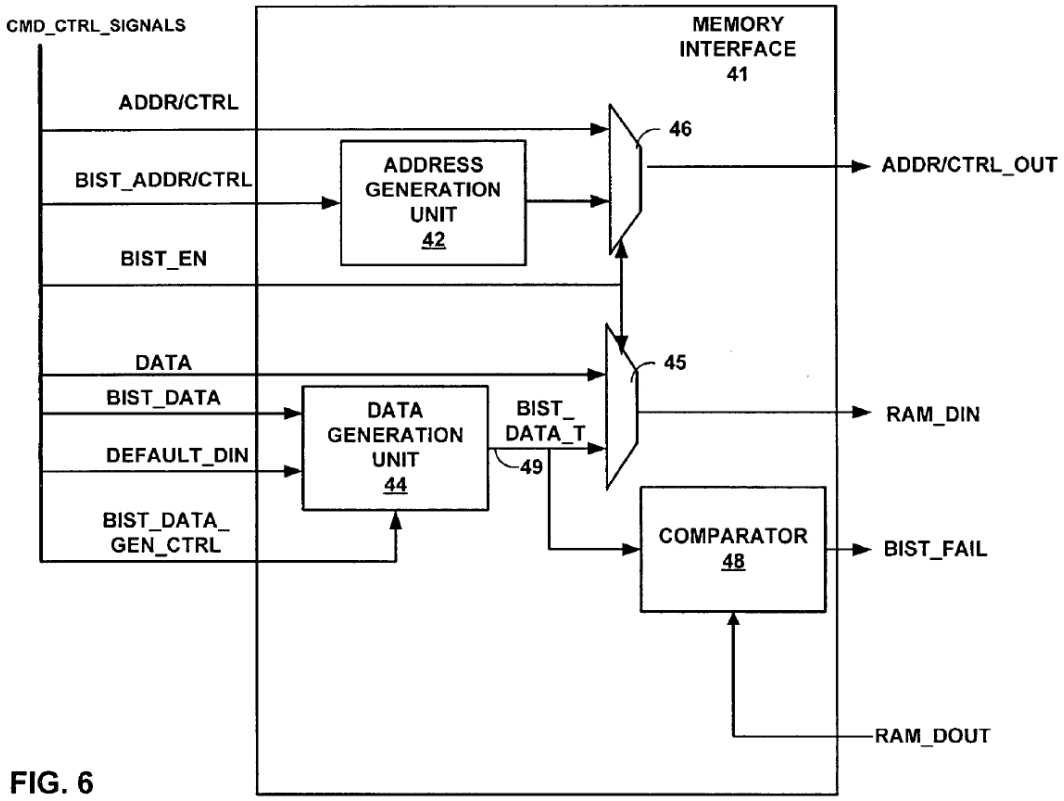

**Ex. 1005 at FIG. 2.**

At the next level of hierarchy are the sequencers (8). The sequencers (8) are "distributed within device blocks that include one or more memory modules." Ex. 1005 at ¶ [0009]. Each sequencer (8) of a device block (6) receives one or more high-level commands from the BIST controller (4) and generates test address, control, and data signals for the plurality of memory modules (12). Ex. 1005 at ¶¶ [0009], [0043-0044], FIGS. 4-6; Ex. 1003 ¶ 76.




**Ex. 1005 at FIG. 5.**

At the bottom of the hierarchy are the memory interfaces (10, 41). The memory interface "handles specific interface requirements for each of the memory modules" by "receiv[ing] memory operations from a controlling sequencer, and translat[ing] the memory operations, including associated address and data signals, **as needed** based on the physical characteristics of the respective memory module." Ex. 1005 at ¶ [0011] (emphasis added); *see also id.* at FIG. 6; Ex. 1003 ¶ 77.




**Ex. 1005 at FIG. 6.**

Specifically, the memory interface (41) receives the test address and control signals from its controlling sequencer (8). The memory interface (41) either provides the same test signals to the memory module (12) as is, or creates its own test address and control signals for the memory module (12) by transforming the data signals from the sequencer (8). Ex. 1005 at FIG. 6, ¶¶ [0011], [0048], [0051], [0052]; Ex. 1003 ¶ 78. The memory interface (41) also receives the test data signals from its controlling sequencer (8) and either provides the same test signals to the memory module (12) as is, or creates its own test data signals for the memory module (12) by modifying the data signals from the sequencer (8). Ex.

1005 at FIG. 6, ¶¶ [0011], [0049], [0050]; Ex. 1003 ¶ 78. Finally, the memory interface (41) uses the comparator (48) to check the data patterns read or received back from the memory module (12) to verify whether the data that is read back from the memory module (12) corresponds to the data pattern. Ex. 1005 at FIG. 6, ¶ [0053]; Ex. 1003 ¶ 79.

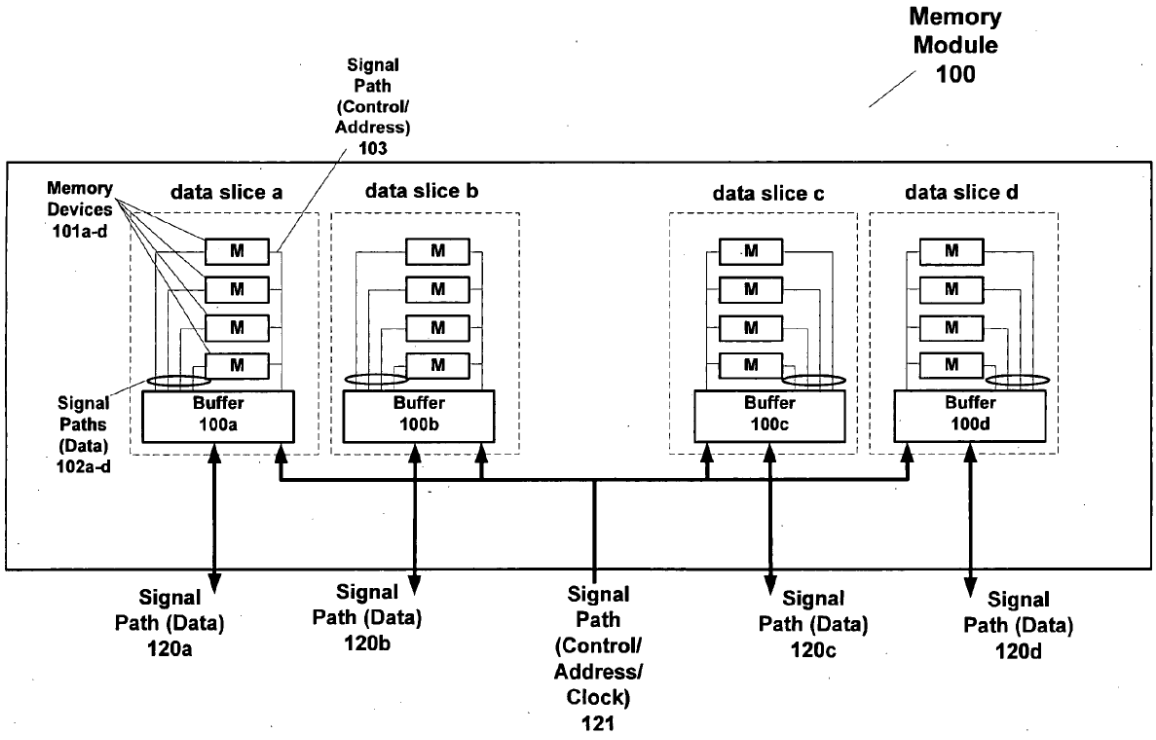
As shown in FIGS. 1 and 4 of Averbuj, each memory interface (10, 41) is positioned directly above, and in alignment with, a corresponding memory module (12). Ex. 1005 at FIGS. 1, 4; Ex. 1003 ¶ 80. Further, no signal is described as flowing from one memory interface (*e.g.*, 10A) to another (*e.g.*, 10B). Ex. 1005 at FIG. 4l; Ex. 1003 ¶ 80. Instead, each memory interface (10, 41) is configured to write to and/or read from the corresponding address and data ports of a corresponding memory module (12) without being in communication with any of the other memory interfaces (10, 41) or other data ports of the other memory modules (12). Ex. 1005 at FIG. 4; Ex. 1003 ¶ 80.

**B. U.S. Patent Publ. No. 2007/0070669 to Tsern (Ex. 1006)**

U.S. Patent Publication No. 2007/0070669 to Tsern ("Tsern") was filed on September 26, 2005 and published on March 29, 2007. Ex. 1006 at Face. Tsern is thus prior art to the '434 Patent at least pursuant to 35 U.S.C. §§ 102(a) and (e).

Tsern is titled "memory module Including a Plurality of Integrated Circuit Memory Devices and a Plurality of Buffer Devices in a Matrix Topology." FIG. 1

of Tsern illustrates an embodiment of a memory module with memory devices (101a–d) and corresponding buffer devices (100a–d). Ex. 1006 at FIG. 1; Ex. 1003 ¶ 82.




**Ex. 1006 at FIG. 1.**

Tsern discloses that, in one embodiment, each buffer device (100a) includes a redundancy and repair unit (1883) which tests and repairs the corresponding memory device(s). Ex. 1006 at FIG. 18, ¶ [0077]; Ex. 1003 ¶ 83. Each such buffer device (100a) includes data, address, and control interfaces (1820a and 1820b) that can be programmed or configured to support memory modules with different number, size, width, and type of memory devices. Ex. 1006 at FIG. 18, ¶ [0099]; Ex. 1003 ¶ 83.

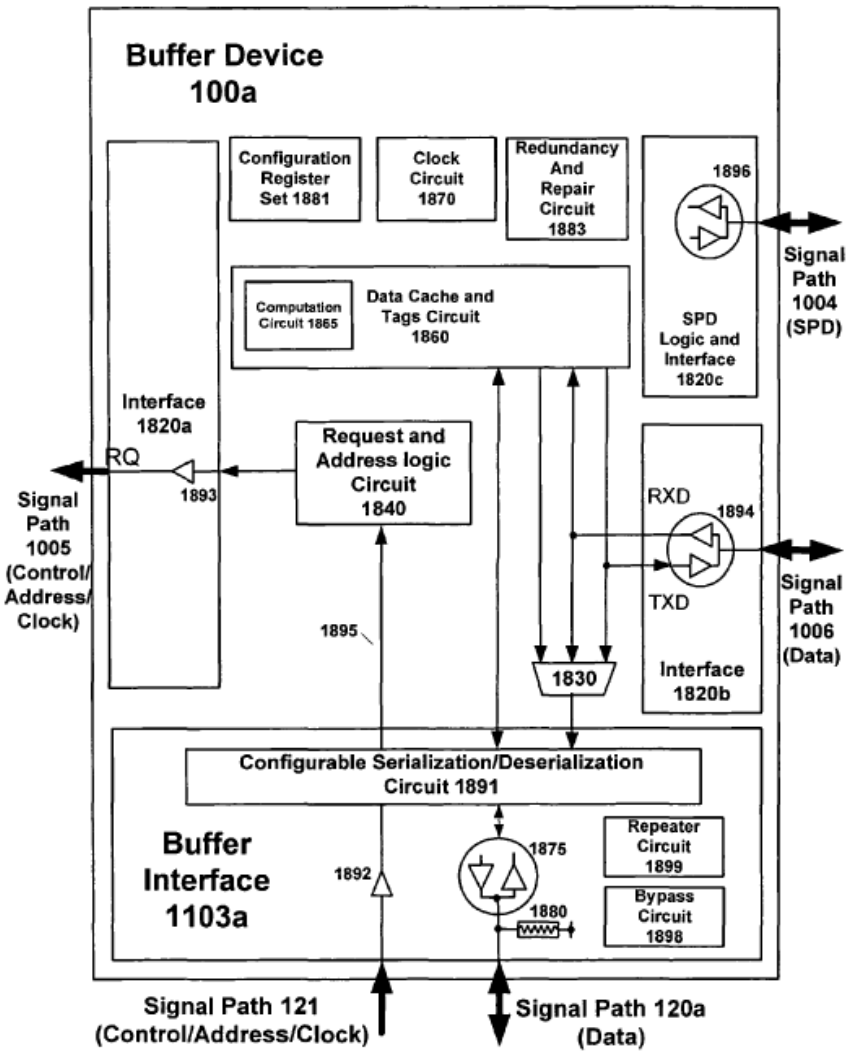



**Fig. 18**

**Ex. 1006 at FIG. 18.**

In one embodiment, the redundancy and repair circuit (1883) periodically tests one or more of memory devices (101a-d) by writing test patterns to a range of addresses and then reading back the values from the same addresses. Ex. 1006 at ¶ [0097], FIG. 18; Ex. 1003 ¶ 84. If the value read from an address does not match the value written to that address, the redundancy and repair circuit (1883) blocks access to that address and maps the address to an alternate storage location by

translating incoming address signals accordingly. Ex. 1006 at ¶ [0097]; Ex. 1003 ¶ 84.

FIG. 1 of Tsern shows that each buffer device (100a-d) communicates address, control, and data signals with its corresponding memory device(s) (101a-d) without being in communication with any of the other buffer devices (100a-d) or other data ports of the other memory devices. Ex. 1006 at FIG. 1; Ex. 1003 ¶ 85.

FIG. 1 of Tsern also shows that each buffer device (100a-d) is positioned close to its corresponding memory device(s). In fact, each buffer device in FIG. 1 of Tsern is shown as being positioned closer to the data port(s) of its corresponding memory devices than to the data ports of the other memory devices. Ex. 1006 at FIG. 1; Ex. 1003 ¶ 86.

Finally, FIG. 9 of Tsern shows an implementation of a memory module in which each of the four buffer devices (100a-d) is implemented as a physically separate integrated circuit package and mounted on different portions of the printed circuit board that houses the memory module. Ex. 1006 at FIGS. 9A-C; Ex. 1003 ¶ 87.

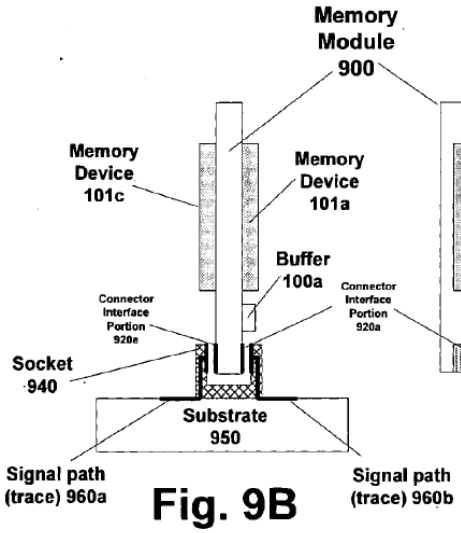



Fig. 9B

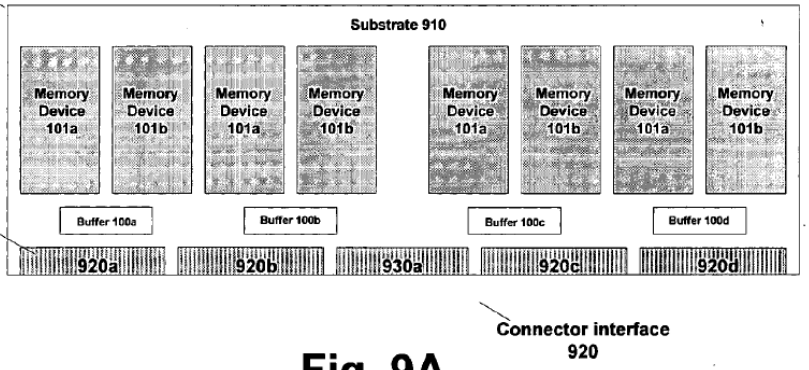



Fig. 9A

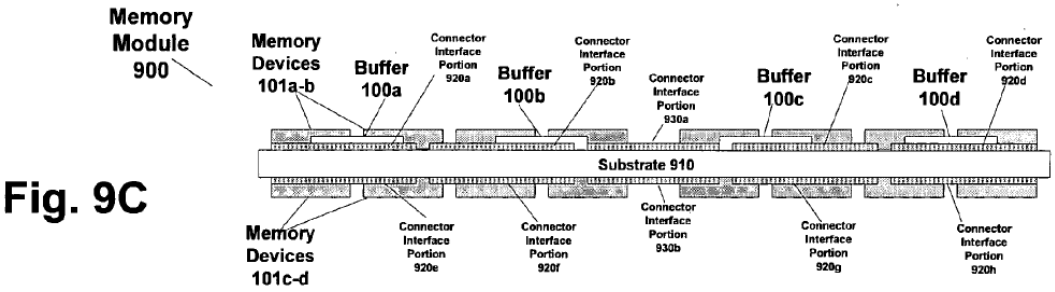



Fig. 9C

**Ex. 1006 at FIG. 9.**

## VI. PRECISE REASONS FOR RELIEF REQUESTED

### A. Averbuj Anticipates Claims 1-7

#### 1. Averbuj Anticipates Claim 1

##### *a.* Preamble

The preamble of claim 1 requires "*a self-testing memory module*."

Averbuj discloses a built-in self-test ("BIST") architecture for testing memory modules. FIG. 1 of Averbuj illustrates an electronic device (2) that includes a BIST controller (4) and a plurality of device blocks (6A-6N). Ex. 1005 at FIG. 1. Each device block (6A-6N) includes a sequencer (8A-8N), one or more

memory interfaces (10A-10N), and one or more respective memory modules (12A-12N). Ex. 1005 at ¶ [0028], FIG. 1. The memory modules (12) may be any type of memory, such as Flash memory or DRAM. Ex. 1005 at ¶ [0032]. Ex. 1003 ¶ 89.

Averbuj further discloses that the BIST controller (4) can initiate, and the device blocks (6) implement and execute, a self-test of the memory modules (12) upon receiving an "external input, such as a control signal from an external testing apparatus" or "automatically [] upon power-up of electronic device." Ex. 1005 at ¶ [0034]; *see also id.* at ¶¶ [0047-0054], FIGS. 1-6; Ex. 1003 ¶ 90.

Because Averbuj's electronic device (2) as well as each of the device blocks (6) include one or more "memory modules that can be tested with only internal, or both internal and external test equipment," the electronic device (2) and device blocks (6) are individually and collectively "*a self-testing memory module*." Ex. 1003 ¶ 91.

***b. "a printed circuit board "***

Claim 1 requires "*[1] a printed circuit board [2] configured to be operatively coupled to a memory controller of a computer system*."

**i. *"a printed circuit board"***

Averbuj discloses that electronic devices that are the subject of his invention may be constructed from many integrated circuit chips and components mounted

on a circuit board. Ex. 1005 at ¶ [0005]; Ex. 1003 ¶ 94; *see also* IPR2014-00970, Paper 12 (Inst. Decision) at 15.

Averbuj also discloses that the electronic device (2) depicted in FIG. 1 is "an example electronic device." Ex. 1005 at ¶ [0018]; *see id*. at ¶¶ [0028-0032]. From this disclosure a skilled artisan would understand Averbuj to disclose that one or more components of his electronic device (2) may be mounted upon "*a printed circuit board*" because printed circuit boards were the most efficient, reliable, and widespread substrate or circuit boards for such devices. *See*, *e.g.*, Ex. 1009 at 140-141; *see also id.* at 136-140; Ex. 1003 ¶¶ 95-96.

**ii. *"configured to be operatively coupled to a memory controller of a computer system"***

Averbuj further discloses that electronic device (2) can be an embedded computer system, a computer, or a server. Ex. 1005 at ¶ [0032], FIG. 1; Ex. 1003 ¶ 97. The electronic device (2) therefore constitutes a "*computer system*." Ex. 1003 ¶ 97.

Averbuj also discloses a BIST controller (4) that operates as a centralized "*memory controller*" during test mode by sending test commands (CMD_DATA and CMD_REQ) to the device blocks ("*memory module*") of the electronic device, ("*a computer system*") and monitoring the status of the memory testing operation (*e.g.*, SEQ_ACK). Ex. 1005 at ¶¶ [0008], [0029], [0033-0037], FIGS. 1-2, 9A-E; Ex. 1003 ¶ 97. Averbuj therefore discloses "*a printed circuit board configured to*

*be operatively coupled to a memory controller of a computer system*," as claimed. Ex. 1003 ¶ 99.

Alternatively, in one embodiment, a "programmable processor" also provides address, control, and data signals to the device blocks (6) ("*memory system*"), which are applied to the memory modules (12) during normal mode. Ex. 1005 at ¶ [0048]; FIG. 6; Ex. 1003 ¶ 100. The "programmable processor" disclosed in Averbuj is, or includes, "*a memory controller of a computer system*" as claimed because a device that provides the address, control, and data signals to, and thereby controls the data flow of, the memory modules of an electronic device such as an "embedded computer system, computer, [or] server" (Ex. 1005 at ¶ [0032]) is "*a memory controller of a computer system*." Ex. 1008 at 497; Ex. 1009 at FIGS. 1-2, at 5; Ex. 1003 ¶¶ 100-103.

Finally, the preamble does not actually require that "*a memory system*" be "*operatively coupled to a memory controller*." All that is required is that "*a memory system*" be "designed to, adapted to, or arranged to [be] or be capable of [being]" "*operatively coupled to a memory controller*." IPR2014-00971, Paper 37 at 31. That Averbuj's electronic device is capable of receiving address, control, and data signals from an external device demonstrates that it is capable of being operatively coupled to a device that manages the data flow of a memory by issuing

address, control, and data signals. Ex. 1008 at 497; Ex. 1009 at FIG. 1-2; Ex. 1003 ¶ 104.

Therefore, Averbuj discloses the preamble of claim 1.

***c. "memory devices"***

Claim 1 requires "*[1] a plurality of memory devices on the printed circuit board, [2] each memory device of the plurality of memory devices comprising data, address, and control ports*."

**i. *"a plurality of memory devices on the printed circuit board"***

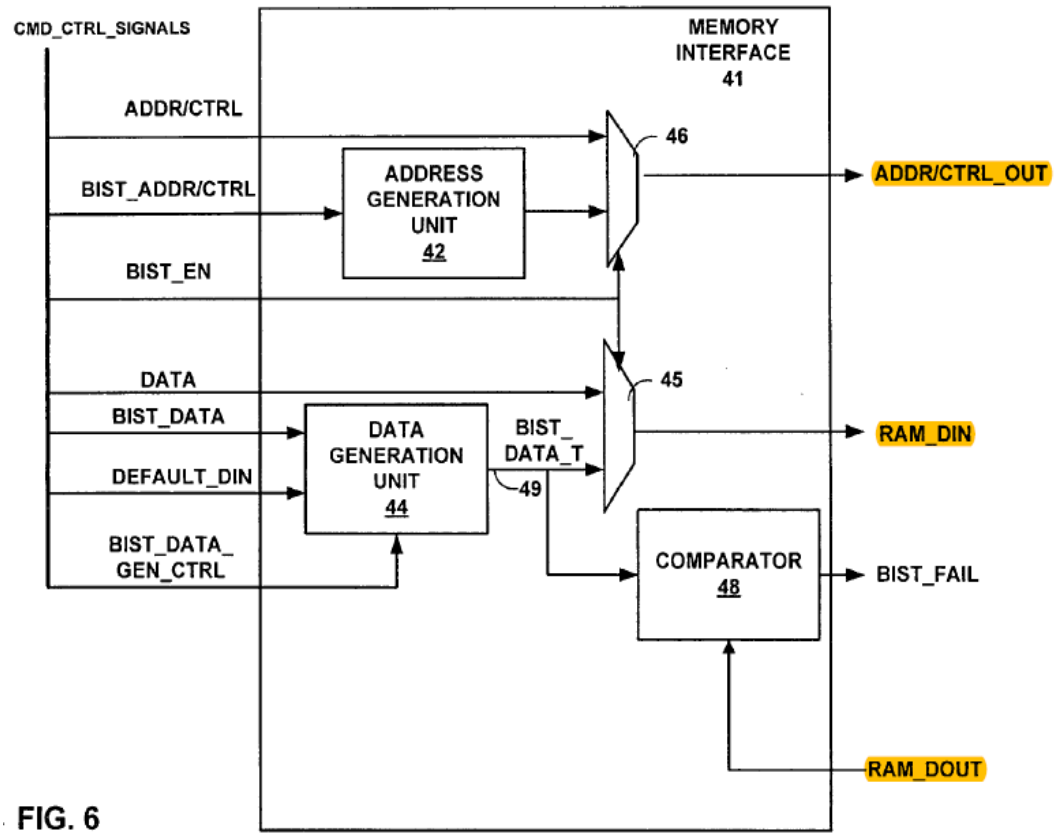
Averbuj discloses that the electronic device (2) incorporates a number of memory modules (12), which may be any type of memory, Ex. 1005 at ¶ [0032], and are hence "*a plurality of memory devices*." Specifically, FIG. 1 depicts an embodiment of the electronic device (2) incorporating "N" memory modules (12A-N). Ex. 1005 at FIG. 1. Similarly, FIG. 4 of Averbuj discloses a device block that includes three memory modules, each associated with a particular sequencer. Ex. 1005 at FIG. 4. Averbuj thus discloses this claim element. Ex. 1003 ¶ 106.

Each memory module (12) disclosed in Averbuj is a memory chip because Averbuj equates "memory chips" with the various types of memory (*e.g.*, DRAM, Flash memory) that are disclosed as comprising the memory modules (12) of his electronic device (2). Ex. 1005 at ¶ [0003]; *compare* Ex. 1005 at ¶ [0006] (DRAM chip) *with* ¶ [0032] (DRAM module); Ex. 1003 ¶¶ 107-108. Averbuj further

discloses that his electronic devices are constructed from many integrated circuit chips, such as memory chips, that are "mounted on a circuit board." Ex. 1005 at ¶ [0005]; Ex. 1003 ¶ 109. And as explained above, a skilled artisan would understand the "circuit board" of Averbuj to be a "*printed circuit board*." *See* § VI.A.1.b.i, above. Therefore, Averbuj discloses that the memory modules (12) ("*a plurality of memory devices*") are "*mounted on a printed circuit board*." Ex. 1003 ¶ 110.

**ii. *"each memory device of the plurality of memory devices comprising data, address, and control ports"***

Averbuj discloses that each memory interface (10) functions as an "interfaces 'wrapper'" around the "address, data, and control signals[] for each respective memory module 12." Ex. 1005 at ¶ [0031]; Ex. 1003 ¶ 111. More particularly, the memory interface exchanges address, data, and control signals with its corresponding memory module (12) through its ADDR/CTRL_OUT, RAM_DIN, and RAM_DOUT ports. Ex. 1005 at FIG. 6, ¶¶ [0049], [0053]; Ex. 1003 ¶¶ 112-113. Therefore, Averbuj discloses that each memory module (12) ("*each memory device of the plurality of memory devices*") comprises "*data, address, and control ports*." Ex. 1003 ¶¶ 114-115.




**Ex. 1005 at FIG. 6 (highlighted).**

***d. "a circuit comprising: a control module …"***

Claim 1 requires "*a circuit comprising: a control module configured to generate address and control signals for testing the memory devices*."

**i. The "sequencer" constitutes "*a control module*"**

As found by the Board in IPR2014-00970, the sequencers (8) disclosed in Averbuj constitute "*a control module*" as claimed because they "*generate address and control signals for testing the memory devices*" and also because "Averbuj's memory interfaces are further configured to apply to the memory modules the same address and control signals received from, and produced by, the sequencers

for testing [] e.g., when the sequencer sends signals that can be applied, without modification or transformation, directly to a memory module irrespective of its physical configuration." IPR2014-00970, Paper 32 at 42 (citations omitted); Ex. 1003 ¶ 118.

Each sequencer 8 (and 8A) of Averbuj is, and all of them collectively are, at least a portion of "*a circuit*" because each is an electronic component that receives and sends electronic signals to other components. Ex. 1012 at 99; Ex. 1003 ¶ 119. Moreover, such sequencers each include, or collectively constitute, "*a control module*" because they are "self-contained component[s]" dedicated to controlling the self-test functionality of the system. Ex. 1007 at 877; Ex. 1012 at 346; Ex. 1003 ¶ 119.

Each sequencer (8), and all of them collectively, "*generate address and control signals for testing the memory devices*" as previously found by the Board. For example, sequencer (8A) parses the test commands (CMD_DATA) it receives from the BIST controller (4) and produces the appropriate command control signals (CMD_CTRL_SIGNALS) for the memory interfaces (10). Ex. 1005 at FIG. 5, ¶¶ [0040-0041]; IPR2014-00970, Paper 32 at 40; Ex. 1003 ¶ 120. And as shown in FIG. 6 of Averbuj, the command control signals (CMD_CTRL_SIGNALS) include address and control signals used for testing (BIST_ADDR/CTRL). Ex. 1005 at FIG. 6, ¶ [0043] ("The command control

signals may include signals to provide a memory address and data to the receiving memory interfaces 10 ...”); *see also id*. at ¶ 44; Ex. 1003 ¶ 121.

When the electronic device (2) is in self-test mode, the test address/control signals (BIST_ADDR/CTRL) are selected and applied on the address and control ports (ADDR/CTRL_OUT) of the corresponding memory module (12). Ex. 1005 at ¶ [0048]; Ex. 1003 ¶ 122. Further, in one configuration, the test address/control signals (BIST_ADDR/CTRL) are provided to the memory modules (12) “without modification or transformation, directly to a memory module, irrespective of its physical configuration.” IPR2014-00970, Paper 32 at 42 (citing Ex. 1005 at ¶ [0056]); Ex. 1003 ¶ 123. Thus, in that configuration Averbuj discloses that the address and control signals that are actually applied to the memory devices for purposes of the self-test are produced/originated (i.e., brought into existence) by the sequencer. Therefore, each sequencer (8), and all of them collectively, is “*a control module configured to generate address and control signals for testing the memory devices*.” IPR2014-00970, Paper 32 at 4; Ex. 1003 ¶ 124.

#### ii. The “address generation unit” also constitutes a “*control module*”

Alternatively, the address generation unit (42) of the memory interface (41) disclosed in Averbuj also constitutes “*a circuit comprising: a control module*” as claimed because it is an electrical component that exchanges electronic signals with other components and because it too can produce (“*generate*”) address and

control signals as needed, as the Board also recognized, and the Patent Owner conceded, in IPR2014-00970. IPR2014-00970, Paper 32 at 41-42 (citation omitted); Ex. 1003 ¶ 125.

The address generation units (42), individually and collectively, are part of "*a circuit*" because each is an electronic component that receives and sends electronic signals to other components. Ex. 1012 at 99; Ex. 1003 ¶ 126. Moreover, such address generation units (42) collectively constitute "*a control module*" because they are a "self-contained component that can provide the function" of controlling the self-test functionality of the memory modules (12) of an electronic device (2). Ex. 1012 at 346 (definition of "module"); Ex. 1007 at 877 (same); Ex. 1003 ¶ 126.

The memory interface (41) of Averbuj receives the command control signals (CMD_CTRL_SIGNALS) from its controlling sequencer (8), which include the test address and control signals (BIST_ADDR/CTRL). Ex. 1006 at FIG. 6; Ex. 1003 ¶ 127. In one configuration, the memory interface (41) further "transforms" the test address/control signals (BIST_ADDR/CTRL) received from the sequencer (8) according to the requirements specified by the sequencer (8). Ex. 1005 at ¶¶ [0051-0052], FIG. 10; Ex. 1003 ¶¶ 128-129. In other words, in this configuration the address generation unit generates/originates test address/control signals by transforming or modifying the signals received from the sequencer. Ex. 1003 ¶

130. Therefore, each address generation unit, and all of them collectively, is also "*a control module configured to generate address and control signals for testing the memory devices*." IPR2014-00970, Paper 32 at 40-41; Ex. 1003 ¶¶ 125-131.

**iii. The "sequencer" and the "address generation unit," combined, constitute "*a control module*"**

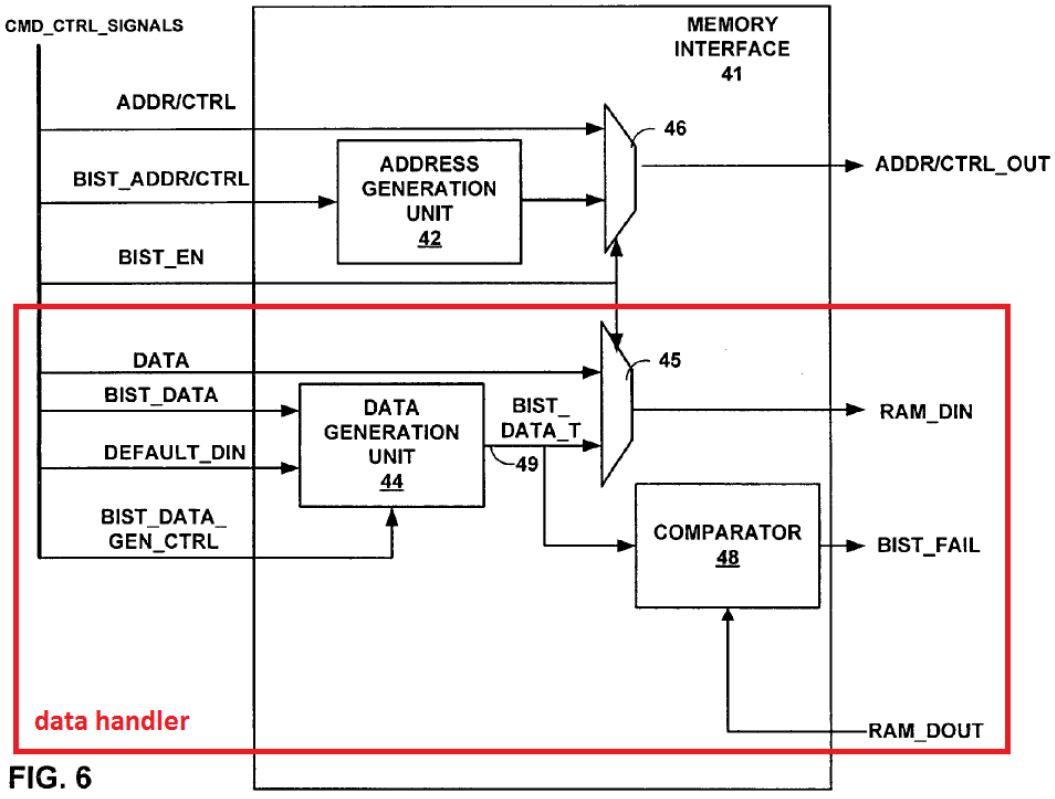
As a further alternative, the sequencers and address generation units , combined, constitute "*a control module*" as claimed. As set forth above, each generates/originates address and control signals in different circumstances or configurations. IPR2014-00970, Paper 32 at 40-42; *see* §§ VI.A.1.d.i-ii. Further, the circuits are operatively coupled to each other so as to provide that functionality, as explained above. *See* §§ VI.A.1.d.i-ii. Therefore, they are also "*a control module configured to generate address and control signals for testing the memory devices*." Ex. 1003 ¶¶ 132-133.

***e. "a circuit comprising: … a data module"***

Claim 1 requires "*[1] a circuit comprising: … a data module comprising a plurality of data handlers, [2] each data handlers operable independently from each of the other data handlers of the plurality of data handlers and [3] operatively coupled to a corresponding plurality of the data ports of one or more of the memory devices and [4] configured to generate data for writing to the corresponding plurality of data ports …*"

### i. *"a circuit comprising: a data module comprising a plurality of data handlers"*

Each memory interface (10) of Averbuj includes a data generation unit (44), an associated comparator (48) and an associated multiplexor (45) (hereinafter "data generation circuitry"). Ex. 1005 at FIG. 6. Each data generation circuitry is part of the "*circuit*" that also includes the sequencers and address generation units discussed above because each exchanges electronic signals with its associated sequencers and address generation units. Ex. 1011 at 8; Ex. 1003 ¶ 135135. Each data generation circuitry is also a "*data handler*" because it is circuitry that handles data written to the associated memory devices. Ex. 1005 at ¶¶ [0049-0050]137.




**Ex. 1005 at FIG. 6 (annotated and emphasis added).**

Petitioner observes that the data generation circuitry from each memory interface (10) of Averbuj constitutes a "*data module*" in the same manner the data handlers of the '434 Patent constituted a "*data module*"—*i.e.*, while independently operable, collectively they are "a self-contained component that performs the function of" transferring data to and from the memory devices of the system. *Compare* Ex. 1001 at FIG. 1 *with* Ex. 1005 at FIG. 4; Ex. 1012 at 6; Ex. 1003 ¶ 136. Thus, the data generation circuitry from each memory interface of Averbuj similarly collectively constitutes "*a data module*." Ex. 1003 ¶ 138.

**ii. "*each data handler operable independently from each of the other data handlers*"**

Each data generation unit and its associated circuitry is "*operable without influence or control by another*" data generation unit and its associated circuitry because each does not communicate with any other. *See, e.g.*, Ex. 1005 at ¶ [0039]. Each memory interface receives command control signals only from the sequencer (8) and interacts only with its corresponding memory module (12). Ex. 1005 at FIG. 4; Ex. 1003 ¶ 139. No signal is described as flowing from one memory interface (*e.g.*, 10A) to another (*e.g.*, 10B). Ex. 1005 at FIG. 4; Ex. 1003 ¶ 139. Because, the data generation circuitry of the various memory interfaces operate without influencing each other, each is "*operable independently from one other*." Ex. 1003 ¶ 140.

Moreover, Petitioner observes that the "*operable independently ...*" claim language has been construed by the Board to mean "operable without influence or control by another." *See* IPR2014-00970, Paper 32 at 33. That phrase is therefore a negative limitation that is satisfied by silence in the prior art. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009); *Clio USA, Inc. v. Proctor and Gamble Co.*, IPR2013-00448, Paper 15 at 3-4. Averbuj satisfies this claim element for this reason as well.

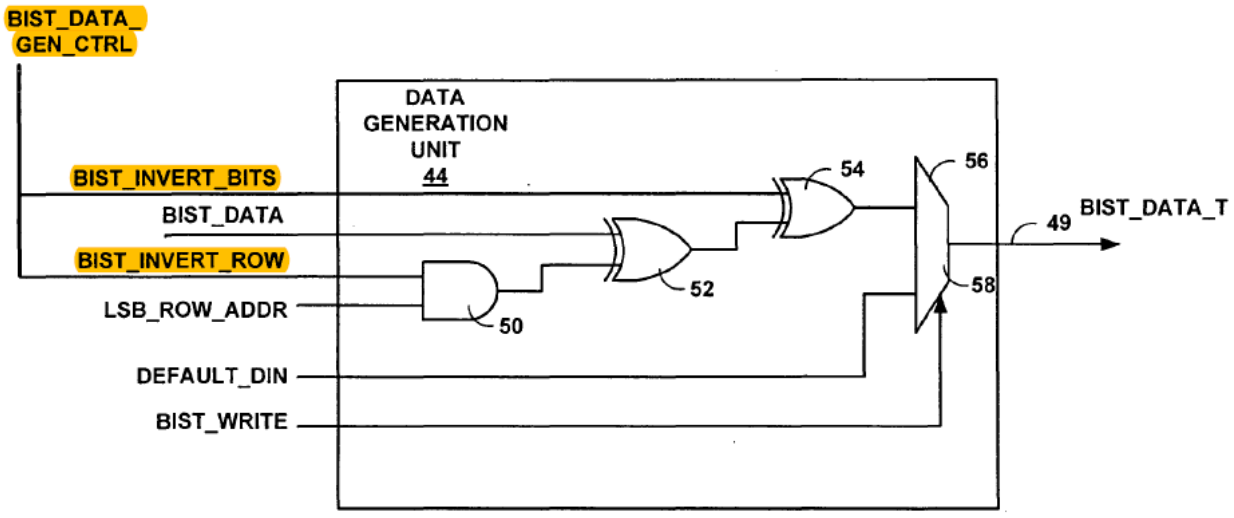
Averbuj therefore discloses that the data generation unit (44) and its associated circuitry of each memory interface (10, 41) is "*a data handler operable independently from each of the other data handlers of the plurality of data handlers*." Ex. 1003 ¶ 140.

**iii. *"each data handler … operatively coupled to a corresponding plurality of the data ports of one or more of the memory devices"***

Averbuj further discloses that each data generation circuitry (44, 45, 48) exchanges data signals with its corresponding memory interfaces through the RAM_DIN and RAM_DOUT ports. Ex. 1005 at ¶¶ [0049, 0053], FIG. 6; Ex. 1003 ¶ 141. Averbuj therefore discloses that each data generation circuitry (44, 45, and 48) ("*data handler*") is "*operatively coupled to a corresponding plurality of the data ports of one or more of the memory devices*." Ex. 1003 ¶ 142.

### iv. *"each data handler … configured to generate data for writing to the corresponding plurality of data ports"*

In one configuration, each data generation circuitry (44, 45, 48) "transforms" the test data signal (BIST_DATA) received from the sequencer (8) into the BIST_DATA_T signal and applies the transformed signal on the RAM_DIN port. Ex. 1005 at ¶¶ [0049-0050]; Ex. 1003 ¶ 143. In one embodiment, the data generation unit (44) transforms the test data signals (BIST_DATA) from the sequencer (8) by inverting specified bits when the BIST_INVERT_BITS signal or the BIST_INVERT_ROW signal is asserted. Ex. 1005 at FIG. 7, ¶ [0057]; Ex. 1003 ¶ 144. Averbuj therefore discloses that each data generation circuitry (44, 45, and 48) ("*data handler*") is "*configured to generate data for writing to the corresponding plurality of data ports*." Ex. 1003 ¶ 145.




**Ex. 1005 at Fig. 7 (highlighted).**

### *f. "wherein the circuit is configured to test the memory devices …"*

Claim 1 requires that "*the circuit is configured to test the memory devices using the address and control signals generated by the control module and the data generated by the plurality of data handlers*."

Averbuj discloses that each data generation circuitry (44, 45, 48) ("*data handler*") may be arranged to test the associated memory modules (12) by writing test data generated by the data generation unit (44) into the memory memory module (12) at addresses generated either by the sequencer (8) or the address generation unit (42). Ex. 1003 ¶ 148. After such data is written to a memory module (12), the memory interface (41) may be arranged to read the data from the same addresses of the memory module (12). Ex. 1005 at ¶ [0053], FIG. 6. The comparator (48) from the memory interface (41) may be arranged to compare the data that is read out to the data that was previously written to determine if they are identical. *Id.*; Ex. 1003 ¶ 148. This comparison constitutes a "*test*" because it determines whether a memory error exists. Ex. 1005 at ¶ [0053], FIG. 6; Ex. 1003 ¶ 149. Averbuj therefore discloses that "*the circuit is configured to test the memory devices using the address and control signals generated by the control module and the data generated by the plurality of data handlers*." Ex. 1003 ¶ 150.

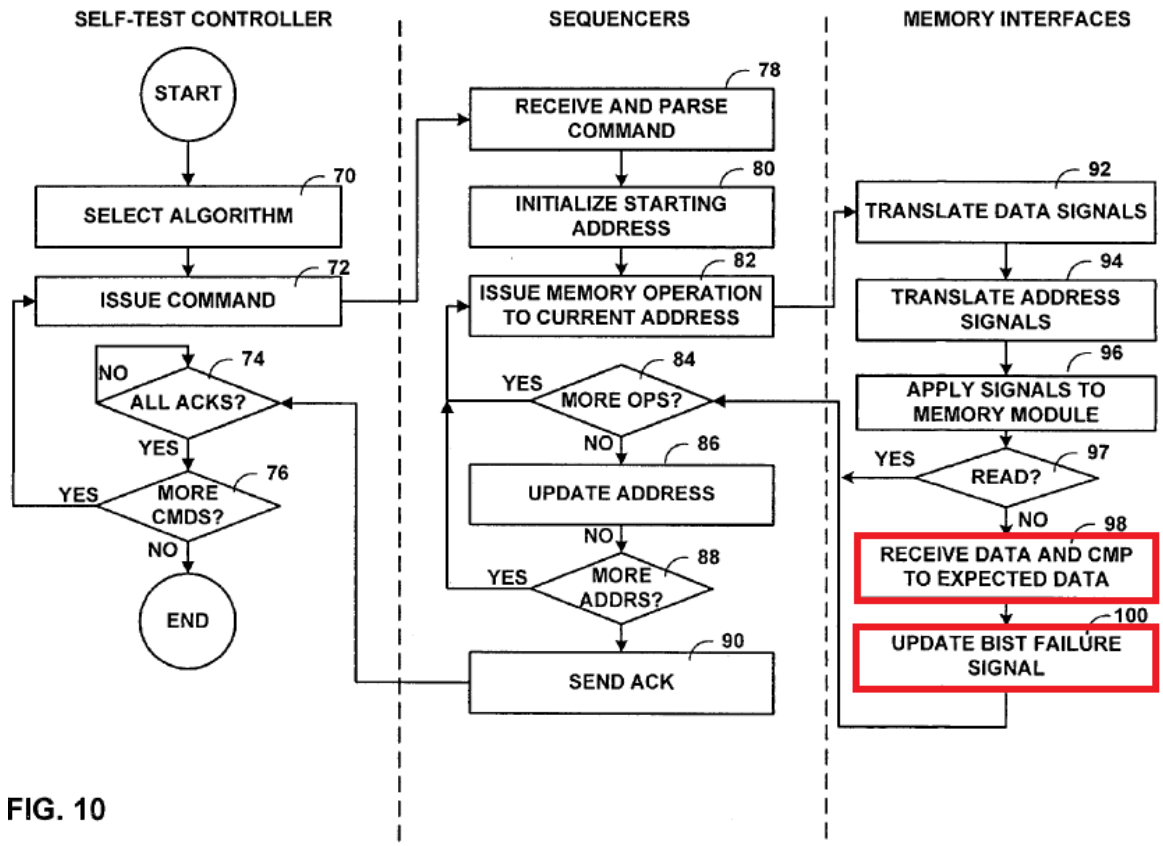



FIG. 10

**Ex. 1005 at FIG. 10.**

### 2. Averbuj Anticipates Claim 2

Claim 2 requires "*[t]he self-testing memory module of claim 1, wherein the plurality of data handlers comprise at least two physically separate components mounted on the printed circuit board*."

Averbuj describes the various components of his BIST circuitry as being "distributed" and "located throughout an electronic device." *See*, *e.g.*, Ex. 1005 at ¶¶ [0012, 0013, 0015]; Ex. 1003 ¶ 153. Moreover, each memory interface (10, 41) and its data generation circuitry (44, 45, and 48) ("*data handler*") is designed in accordance with particular interface requirements of its associated memory module

(12). Ex. 1005 at ¶ [0011]; Ex. 1003 ¶ 153. From these disclosures, a skilled artisan would understand that the various memory interfaces (10, 41) and their data generation circuitry (*i.e.*, each data generation unit 44 and its associated multiplexor 45 and comparator 48) are "*physically separate components.*" Ex. 1003 ¶ 153.

Averbuj further discloses that electronic devices, such as his electronic device (2), are constructed from many integrated circuit chips and other components mounted on a circuit board. Ex. 1005 at ¶ [0005] ("[The electronic devices] are constructed from many integrated circuit chips and many supporting components mounted on a circuit board."); Ex. 1003 ¶ 154. Averbuj discloses that BIST units are commonly incorporated into chips or integrated circuits, which are synonyms. Ex. 1005 at ¶ [0003]; Ex. 1012 at 3, 5. Because the memory interface (12) is part of a BIST unit, it comprises a chip or an integrated circuit of an electronic device "mounted on a circuit board." Ex. 1005 at ¶ [0005]; Ex. 1003 ¶ 154. As demonstrated above, Averbuj also discloses that his electronic device includes a printed circuit board. *See* § VI.A.1.b.i. Accordingly, Averbuj discloses that "*the plurality of data handlers comprise at least two physically separate components mounted on the printed circuit board.*" Ex. 1003 ¶ 154.

### 3. Averbuj Anticipates Claim 3

Claim 3 requires that "*[t]he self-testing memory module of claim 2, wherein the plurality of data handlers comprise at least two physically separate integrated circuit packages*."

Averbuj discloses that the memory interfaces, each of which includes a data generation circuitry ("*data handler*"), are distributed among a plurality of memory chips mounted on a circuit board. *See* § VI.A.2, above. An integrated circuit chip, such as a memory chip, must be packaged in order to be mounted on a circuit board. Ex. 1016 at 1:15-27; Ex. 1003 ¶ 158. Thus, each of the plurality of chips, including the chip that incorporates a memory interface and its data generation circuitry ("*data handler*"), is a **packaged** memory chip, and therefore a "*physically separate integrated circuit package*." Ex. 1003 ¶ 159 Accordingly, Averbuj discloses claim 3. Ex. 1003 ¶ 160.

**4. Averbuj Anticipates Claim 4**

Claim 4 requires that "*[t]he self-testing memory module of claim 3, wherein the physically separate integrated circuit packages are mounted on different portions of the printed circuit board*."

As explained above, Averbuj discloses that each memory interface (10, 41), which includes a data generation circuitry (44, 45, and 48) ("*data handler*"), is incorporated into a separately packaged chip, *i.e.*, "*physically separate integrated circuit package*," and "*mounted on a printed circuit board*." *See* § VI.A.2-3,

above. Averbuj further discloses that various components of his BIST circuitry, including the sequencer (8) and the memory modules (12), are "distributed" and "located throughout an electronic device." Ex. 1005 at ¶¶ [0012, 0013, 0015]. As each memory interface (10, 41), which includes a data generation circuitry (44, 45, 48), is designed to receive signals from its controlling sequencer (8) and also function as an interface "wrapper" for each memory module (12), a skilled artisan would understand that each memory interface (10) is also "distributed" and "located throughout an electronic device." Ex. 1003 ¶ 163. Averbuj therefore discloses that the memory interfaces are positioned, or mounted, on different portions of the circuit board. Ex. 1005 at ¶¶ [0012, 0013, 0015]; Ex. 1003 ¶ 163. Averbuj therefore discloses this claim element. Ex. 1003 ¶ 163.

### 5. Averbuj Anticipates Claim 5

Claim 5 requires that "*[t]he self-testing memory module of claim 2, wherein the plurality of data handlers is positioned on the printed circuit board proximate to the corresponding plurality of data ports*."

The '434 Patent describes the position of the "*data handlers*" in FIG. 2, which is directly below the corresponding "*memory devices*," as being "proximate to the corresponding plurality of data ports [of the corresponding memory device]." Ex. 1001 at 9:13-15; Ex. 1003 ¶ 165.

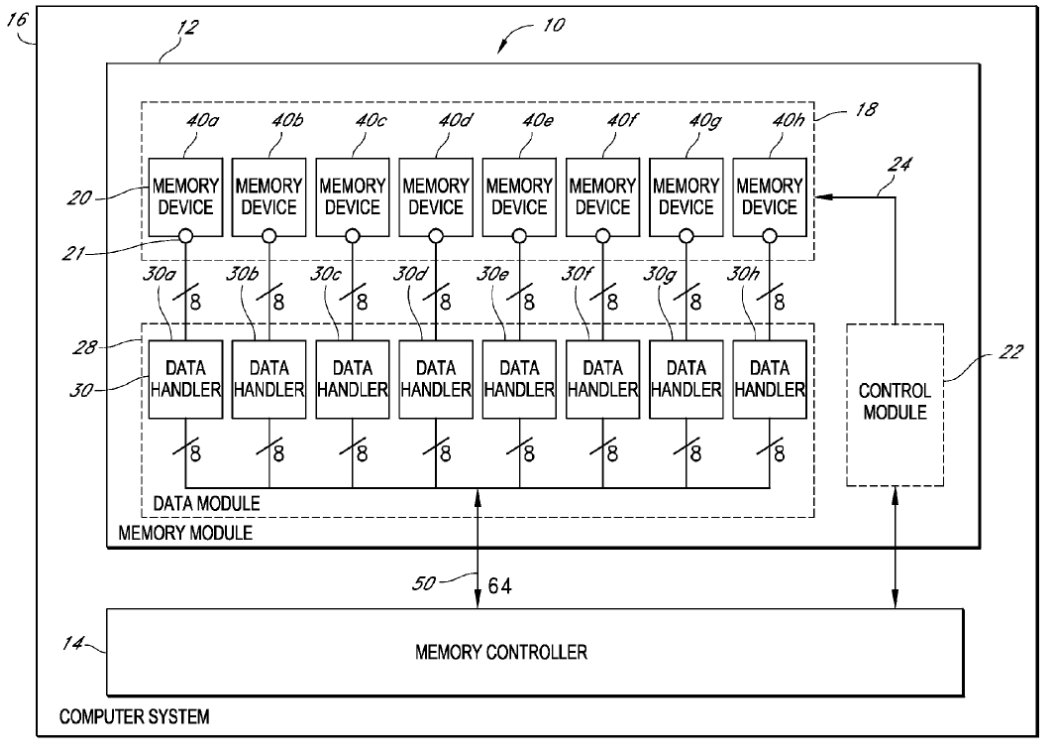



FIG. 2

**Ex. 1001 at FIG. 2.**

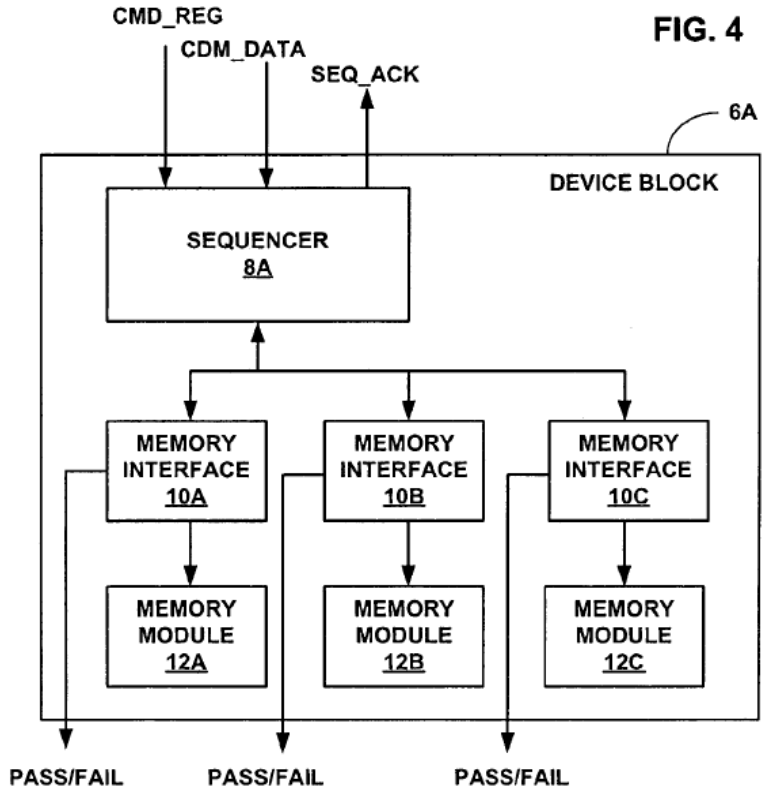



FIG. 4

**Ex. 1005 at FIG. 4.**

Averbuj discloses similar positioning of the memory interfaces (10, 41), which include the data generation circuitry ("*data handlers*"). *See* Ex. 1005 at FIGS. 1, 4; Ex. 1003 ¶¶ 166-167. Averbuj therefore discloses that the memory interfaces (10, 41) and their data generation circuitry (44, 45, 48) ("*data handlers*") are "*positioned … proximate to the corresponding plurality of data ports*" in the same manner as the '434 Patent. Ex. 1003 ¶ 168.

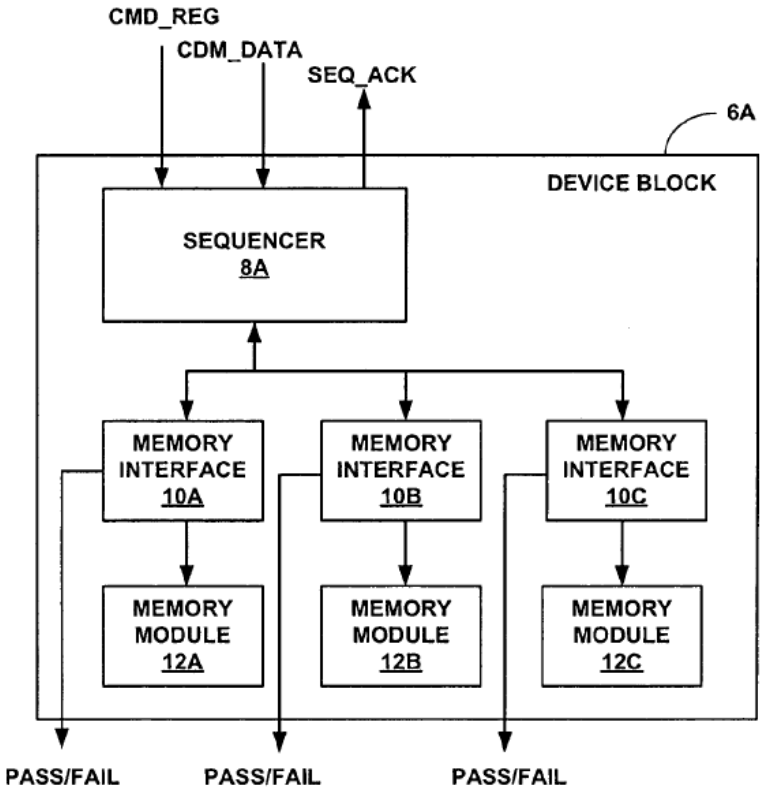



FIG. 4

**Ex. 1005 at FIG. 4.**

### 6. Averbuj Anticipates Claim 6

Claim 6 requires that "*"[t]he self-testing memory module of claim 5, wherein each of the plurality of data handlers is positioned closer to the corresponding plurality of data ports than to the other data ports of the plurality of memory devices*."

As demonstrated above, Averbuj discloses "*wherein each of the plurality of data handlers is positioned on the printed circuit board proximate to the corresponding plurality of data ports.*" *See* § VI.A.5, above. Averbuj similarly discloses this claim. For example, each memory interface (10A-C) (which includes a data generation circuitry, *i.e.*, "*data handler*") in FIG. 4 is "positioned closer to" its associated memory module (12A-C) and its data ports, than to the other memory modules or data ports. Ex. 1005 at FIG. 4; Ex. 1003 ¶ 171. Averbuj therefore discloses claim 6. Ex. 1003 ¶ 172.

### 7. Averbuj Anticipates Claim 7

Claim 7 requires that "*[t]he self-testing memory module of claim 6, wherein each of the data handlers is further configured to read from the corresponding plurality of data ports and further comprises a verification element for checking for failures in the operation of the memory devices by verifying that data read from the corresponding plurality of data ports corresponds to the data generated by the data handler for writing to the corresponding plurality of data ports*."

**i. *"each of the data handlers is further configured to read from the corresponding plurality of data ports"***

Averbuj discloses that, after data is written to a memory module (12) by asserting the test address/control and data signals on the ADDR/CTRL_OUT and RAM_DIN ports, respectively, the data generation circuitry is arranged so that the data from the same address of the memory module (12) is read out through the RAM_DOUT port. Ex. 1005 at ¶ [0053]; FIG. 6; Ex. 1003 ¶ 174. The data generation unit (44) of the memory interface (41) is therefore "*further configured to read from the corresponding plurality of data ports*" as claimed. Ex. 1003 ¶ 175.

**ii. *"each of the data handlers … further comprises a verification element for checking for failures in the operation of the memory devices by verifying that data read from the corresponding plurality of data ports corresponds to the data generated by the data handler for writing to the corresponding plurality of data ports"***

During test mode, each comparator (48) ("*a verification element for checking for failures in the operation of the memory devices*") compares the data that is read out from the memory module (12) ("*verifying that data read from the corresponding plurality of data ports*") with the test data that was generated by the data generation unit (44) and written to the memory module (12) to see if they are equal ("*corresponds to the data generated by the data handler for writing to the*

*corresponding plurality of data ports*"). Ex. 1005 at ¶ [0053], FIG. 6, 10; Ex. 1003 ¶ 176. If the data read from the memory module (12) is different from the data previously written to the memory module (12), it asserts the BIST_FAIL signal to indicate a failure ("*checking for failures in the operations of the memory devices*"). Ex. 1005 at ¶ [0053], FIGS. 6 & 10; ; Ex. 1003 ¶ 176. Averbuj therefore discloses this claim element. Ex. 1003 at ¶177.

### B. Averbuj Renders Claims 1-7 Obvious

Patent Owner may also argue that claims 1-7 are not anticipated by Averbuj, for various reasons. Even if one were to accept such arguments, claims 1-7 as a whole would have been obvious over Averbuj.

#### 1. Averbuj Renders Claim 1 Obvious

##### *a. "memory controller of a computer system"*

To the extent one might argue that Averbuj does not disclose "*memory controller of a computer system*," it would have been obvious to include that element in the system of Averbuj.

Averbuj discloses that the device blocks ("*memory modules*") receives address/control signals (ADDR/CTRL) and data signals (DATA) from a programmable processor and applies those signals under normal operating conditions. Ex. 1005 at ¶ [0048], FIGS. 5, 6; Ex. 1003 ¶ 179. Averbuj discloses that his electronic device (2) can be a "computer [or] server" that incorporates a

variety of memory modules, such as DRAM and Flash memory. Ex. 1005 at ¶ [0032]; Ex. 1003 ¶ 179.

At the time, memory controllers were commonly used in computers and servers in order to manage access to the memory systems. *See, e.g.*, Ex. 1008 at 316-317 (showing a "Memory Controller" on Fig. 7.2); Ex. 1011 at FIGS. 1 & 2 (showing "Memory Hub Controller" and "Memory Controller"); Ex. 1023 at FIG. 1 (showing a "Memory Controller"); Ex. 1024 at FIG. 1 (showing a "Common Memory Controller"); Ex. 1003 ¶ 180. Thus, to use a memory controller to manage memory accesses in the system of Averbuj by providing the device blocks (6) with address, control, and data signals would have been the use of known techniques and structures in their known ways to achieve the predictable result of accessing memory. Ex. 1003 ¶ 180.

A skilled artisan would have been motivated to use a memory controller with the electronic device (2) of Averbuj for a number of reasons. A memory controller could relieve the main processor of the burden of complying with the complex interface protocols and requirements of the memory system and thus improve the overall performance of a computer or server. *See, e.g.*, Ex. 1008 at 497-498; Ex. 1003 ¶ 181. A memory controller could also efficiently arbitrate and schedule simultaneous requests by multiple components to access the memory system and therefore avoid resource scheduling conflicts and improve throughput,

especially in a multi-processor environment. Ex. 1008 at 328, FIG. 13.1; Ex. 1003 ¶ 182. For these reasons, a skilled artisan would have been motivated to include a memory controller in a computer or server, such as the computer or server contemplated in Averbuj. Ex. 1003 ¶ 183.

Thus, it would have been obvious to design, arrange, or adapt ("*configure*") the memory modules (12) and the device blocks (6) of Averbuj ("*memory module*") such that they would be or be capable of being "*operatively coupled to a memory controller of a computer system.*" Ex. 1003 ¶ 184.

***b. "a plurality of memory devices on a printed circuit board"***

To the extent one might argue that Averbuj does not disclose "*a plurality of memory devices on the printed circuit board*," it would have been obvious to use such a substrate to mount the components of the electronic device (2) of Averbuj.

Because printed circuit boards were by far the most common substrate for memory modules in the prior art (Ex. 1009 at 140-41; *see*, *e.g.*, Ex. 1013 at 1; Ex. 1014 at 1; Ex. 1015 at 1), to use them with the "*memory module*" of Averbuj would have been the use of a known structure for its known purpose to achieve a predictable result, *i.e.*, mount circuit components. Ex. 1003 ¶ 186. Furthermore, printed circuit boards were often considered to be the only viable substrate for many high-speed or commercial circuits, as alternatives lacked the characteristics required for such use, such as good electrical properties (*e.g.*, low impedance),

reliability, and ease of mounting and routing. Ex. 1009 at 136-41; Ex. 1003 ¶¶ 187-188. Due to its low cost, superior performance, reliability, and widespread use, a skilled artisan would have been motivated to use a printed circuit board as the substrate for mounting various components of a memory module. *Id.*; *see also* Ex. 1009 at 44-49; Ex. 1003 ¶ 189. Accordingly, "*memory devices mounted on a printed circuit board*" would have been obvious to a person of ordinary skill in the art. Ex. 1003 ¶ 190.

### 2. Averbuj Renders Claim 2 Obvious

To the extent one might argue that Averbuj does not sufficiently disclose "*wherein the plurality of data handlers comprise at least two physically separate components mounted on the printed circuit board*" of claim 2, it would have been obvious for a skilled artisan to keep the plurality of data generation units (and associated circuits) distributed among "*at least two physically separate components mounted on the printed circuit board*."

It was known in the art to include circuit components of a memory system, including those components responsible for handling the transfer of data to and from a memory device, in physically separate integrated circuit packages, and to do so would have been well within the average skill in the art. *See*, *e.g.*, Ex. 1006 at FIG. 9A; ¶¶ [0052-0053] (explaining that the depicted separate "buffer devices" are in one embodiment "housed in separate packages"); ¶ [0029] (noting that as

used therein "an integrated circuit buffer device is also referred to as a buffer or buffer device."); Ex. 1003 ¶ 192. To employ that technique in the system of Averbuj would therefore have been the use of a known technique for its known purpose and would have achieved only predictable results, such as the protection of integrated circuits by the packaging. Ex. 1003 ¶ 192.

Moreover, a skilled artisan would have been motivated to use physically separate integrated circuit packages for the data handlers of Averbuj in at least two different ways. Ex. 1003 ¶ 193. A skilled artisan applying the teachings of Averbuj to improve a conventional BIST unit and memory chip would have been motivated to retain the memory interface (or the equivalent circuitry) within each memory chip of a memory module. Ex. 1003 ¶ 194. Memory modules at the time, such as DRAM modules, typically comprised of a plurality of packaged memory chips mounted on different portions of a printed circuit board. *See*, *e.g.*, Ex. 1013 at FIG. 1; Ex. 1014 at 1; Ex. 1003 ¶ 195. Averbuj explains, and prior references confirm, that it was common practice at the time to place BIST units in each memory chip. Ex. 1005 at ¶ [0003]; Ex. 1010 at FIG. 2; Ex. 1003 ¶¶ 196-197.

One downside of such conventional design is that overlapping BIST functions and circuitry were redundantly duplicated in each conventional memory chip of a memory module. Ex. 1003 ¶ 198. Averbuj discloses and teaches that such redundant BIST circuitry can be reduced or eliminated if the circuitry that

provides overlapping functions, *e.g.*, BIST controller, are taken out of each memory chip and centralized or merged into a single component. Ex. 1005 at ¶ [0008]; Ex. 1003 ¶ 198. Averbuj, however, does not disclose or teach taking out of each memory chip portions of the BIST units that are not redundant. In particular, Averbuj acknowledges that each memory interface is particularized to meet the specific needs of each memory chip it services, and is therefore not redundant. Ex. 1005 at ¶¶ 11, 49-50; Ex. 1003 ¶ 199.

A skilled artisan that seeks to reduce the redundant BIST circuitry of conventional memory chips and BIST units would have been motivated to modify the conventional design in such a way as to avoid unnecessary modifications to the conventional design. Ex. 1003 ¶ 200. Specifically, a skilled artisan would have understood that the BIST controller and sequencer portions of conventional BIST units would need to be carved out from each memory chip and combined to reduce redundant circuitry. Ex. 1003 ¶ 200. However, a skilled artisan would also have understood and recognized that the memory interface portions need not be carved out and/or combined since doing so would not reduce much, if any, circuitry. Ex. 1003 ¶ 200. Because a skilled artisan would have been motivated to make modifications in an efficient manner, he or she would have been motivated to keep the original design with respect to the memory interface portion. In other words, a skilled artisan would have been motivated to keep the memory interfaces (10, 41)

(each of which includes a "*data handler*") within each memory chip that was separately packaged and mounted on a printed circuit board of a memory module ("*physically separate integrated circuit packages*."). Ex. 1003 ¶ 201.

Alternatively, a skilled artisan, particularly a skilled artisan looking to add new BIST circuitry for a memory module according to the teachings of Averbuj, would have been motivated to incorporate each component of Averbuj's BIST architecture—*i.e.*, BIST controller, sequencers, and memory interfaces—into separate integrated circuit chips/packages. Ex. 1003 ¶ 202. This design approach had already been proposed and/or practiced by others (*see, e.g.*, Ex. 1006 at FIGS. 9A-C), and thus a skilled artisan would have known and have been motivated to try this approach. Ex. 1003 ¶ 203. This alternative approach is equally consistent with the teachings of Averbuj in that it still combines redundant BIST circuitry together. Ex. 1003 ¶ 204.

Furthermore, either design choice, which keeps each memory interface (and each other component of Averbuj's BIST circuitry) in separate chips/packages—provides a number of benefits, that would have motivated a skilled artisan, including: (1) reduction of the busing area of the chips/packages (Ex. 1017 at 3:45-53; Ex. 1003 ¶ 205); (2) reduction of load on the chips/packages (Ex. 1018 at 1:5-23, FIG. 3; Ex. 1019 at 1:32-2:3, FIG. 5; Ex. 1013 at ¶ 206); (3) ease of wiring / routing (Ex. 1021 at 6; Ex. 1003 ¶¶ 224); (4) reduction of signal line capacitance

affecting data transmission rates (Ex. 1020 at 2:27-3:6; Ex. 1003 ¶¶ 225); and (5) reduction of signal crosstalk affecting signal integrity (Ex. 1010 at 23-25, 207; Ex. 1003 ¶¶ 226). Ex. 1003 ¶ 208. In addition, keeping the memory interfaces and other components of Averbuj's BIST circuitry in separate integrated circuit packages allows for efficient maintenance and repair since only the packages that require repair or upgrade need be replaced. Ex. 1003 ¶ 207. For these reasons, a skilled artisan would have been motivated to keep the memory interfaces (10, 41) and their respective data generation circuitry (44, 45, 48) ("*data handlers*") in separate chips ("*physically separate components*") to be mounted on the printed circuit board of a memory module ("*mounted on the printed circuit board*.") Ex. 1003 ¶ 209.

Accordingly, claim 2 is obvious over Averbuj. Ex. 1003 ¶ 210.

### 3. Averbuj Renders Claim 3 Obvious

To the extent one might argue that Averbuj does not sufficiently disclose "*wherein the plurality of data handlers comprise at least two physically separate integrated circuit packages*," it would have been obvious to include it in the electronic device (2) of Averbuj.

It was known in the prior art to include separate circuit components of a memory system, including those components responsible for handling the transfer of data to and from a memory device, in physically separate integrated circuit

packages, and to do so would have been well within the average skill in the art. *See, e.g.*, Ex. 1006 at FIG. 9A; ¶¶ 29 (noting that as used therein "an integrated circuit buffer device is also referred to as a buffer or buffer device."), 52-53 (explaining that the depicted separate "buffer devices" are in one embodiment "housed in separate packages"). To employ that technique in the system of Averbuj would have been the use of a known technique for its known purpose and would have achieved only predictable results, such as the protection of integrated circuits by the packaging. Ex. 1003 ¶ 212.

Moreover, a skilled artisan would have been motivated to incorporate each memory interface (10, 41) and its data generation circuitry (44, 45, 48) ("*data handlers*") in a physically separate integrated circuit package in order to reduce the busing area of the chips/packages (Ex. 1017 at 3:45-53; Ex. 1003 ¶ 205) and the load on the chips/packages (Ex. 1018 at 1:5-23, FIG. 3; Ex. 1019 at 1:32-2:3, FIG. 5; Ex. 1013 at ¶ 206), and to place the memory interfaces (10, 41) close to their corresponding memory modules (10, 41). Ex. 1003 ¶ 213; *see also* Ex. 1003 ¶¶ 224-226.

Accordingly, claim 3 is obvious over Averbuj. Ex. 1003 ¶ 214.

#### 4. Averbuj Renders Claim 4 Obvious

To the extent one might argue that Averbuj does not sufficiently disclose "*wherein the physically separate integrated circuit packages are mounted on*

*different portions of the printed circuit board*," it would have been obvious to incorporate in the device of Averbuj.

It was known to spread out separate integrated circuit packages, such as data buffer devices, across different portions of a circuit board. *See*, *e.g.*, Ex. 1006 at FIG. 9A (showing different packages mounted across different portions of the board); ¶¶ [0052-0053] (explaining that the depicted separate "buffer devices" are in one embodiment "housed in separate packages"); ¶ [0029] (noting that as used therein "an integrated circuit buffer device is also referred to as a buffer or buffer device."). To use such a technique in Averbuj would therefore have been only the use of a known technique for its known purpose and would have achieved only predictable result of spreading circuit components across the printed circuit board. Ex. 1003 ¶ 216.

A skilled artisan would have been motivated to position "*the physically separate integrated circuit packages…[at]… different portions of the printed circuit board.*" First, there are only a limited number of places such components could be placed on a standard printed circuit board, so it would have been obvious to try to place each "*data handler*" at different portions of the printed circuit board. Ex. 1003 ¶ 217. Second, a skilled artisan would have been motivated to place each memory interface (10) and its data generation circuitry (44, 45, and 48) ("*data handler*") at different portions of the board in order to place the data generation

circuitry ("*data handler*") near its associated memory module (12) ("*memory device*"). Such placement would shorten the signal lines between the data generation circuitry ("*data handlers*") and their associated memory modules (12) ("*memory devices*"), which would (i) simplify wiring / routing (Ex. 1021 at 6; Ex. 1003 ¶ 224); (ii) reduce the signal line capacitance affecting data transmission rates (Ex. 1020 at 2:27-3:6; Ex. 1003 ¶ 225); and (iii) reduce signal crosstalk affecting signal integrity (Ex. 1010 at 23-25, 207; Ex. 1003 ¶ 226). Ex. 1003 ¶ 218.

Accordingly, claim 4 is obvious over Averbuj. Ex. 1003 ¶ 219.

**5. Averbuj Renders Claim 5 Obvious**

To the extent one might argue that Averbuj does not sufficiently disclose "*wherein the plurality of data handlers is positioned on the printed circuit board proximate to the corresponding plurality of data ports*," it would have been obvious to incorporate in the device of Averbuj.

It was, for example, known to include circuitry for reading and writing data from/to memory devices at locations that were closer to the data ports of associated memory devices than to those of other memory devices in the system. *See, e.g.*, Ex. 1006 at FIG. 9A. Use of that technique in Averbuj would therefore have been only the use of a known technique for a known purpose to achieve the predictable result of more compactly and efficiently place related circuits near each other. Ex. 1003 ¶ 221.

Further, FIGS. 1 and 4 of Averbuj depict each memory interface (10) as being near or adjacent to its corresponding memory module (12), which suggests that each data generation unit (41, 45, 48) ("*data handler*") should be near its corresponding memory module (12) ("*memory device*"). Ex. 1003 ¶ 222.

Moreover, there are only a limited number of places such components could be placed on a standard printed circuit board, so it would have been obvious to try to place each "data handler" near its corresponding memory module. Ex. 1003 ¶ 223.

Furthermore, a skilled artisan would have been motivated to place the data generation circuitry (44, 45, 48) of each memory interface (10, 41) near the data ports of their respective memory modules (12) for a number of reasons. First doing so simplifies the wiring or routing of signals. Ex. 1021 at 6; Ex. 1003 ¶ 224. Second, doing so reduces the trace length, which in turn reduces the capacitance of the trace that contribute to signal propagation delays (Ex. 1020 at 2:27-3:6; Ex 1003 at ¶ 225) and also the high-frequency inductance of the trace that creates signal crosstalk and EMI (1010 at 23-25, 207; Ex. 1003 ¶ 226).

Accordingly, claim 5 is obvious over Averbuj.

### 6. Averbuj Renders Claim 6 Obvious

To the extent one might argue that Averbuj does not sufficiently disclose "*wherein each of the plurality of data handlers is positioned closer to the*

*corresponding plurality of data ports than to the other data ports of the plurality of memory devices*," it would have been obvious to incorporate in the device of Averbuj.

It was, for example, known to include circuitry for reading and writing data from/to memory devices at locations that were closer to the data ports of associated memory devices than to other un-associated memory devices in the system. Ex. 1006 at FIG. 9. To do so would therefore have been the use of a known technique for its known purpose to achieve the predictable result of a more compact device. Ex. 1003 ¶ 230.

Moreover, a skilled artisan would have been motivated to do so for the same reasons set forth above with respect to claim 5. *See* § VI.B.5. Indeed, the same motivations for placing data handling circuitry close to related memory devices would have motivated a skilled artisan to place those circuitry **closer** to the data ports of those devices, in order to simplify the wiring paths, and recue EMI and signal line impedance even further. Ex. 1003 ¶¶ 231-232.

Accordingly, claim 6 is obvious over Averbuj. Ex. 1003 ¶ 233.

### C. Claims 1-7 Are Obvious over Averbuj in View of Tsern

Patent Owner may also argue that claims 1-7 are not obvious over Averbuj, for various reasons. Even if one were to accept such arguments, the claims as a whole would have been obvious over Averbuj in view of Tsern.

**1. Claim 1 Is Obvious over Averbuj in View of Tsern**

To the extent one might argue that Averbuj does not disclose "*a printed circuit board*" as required by claim 1, it would have been obvious to include it in the system of Averbuj per the teachings of Tsern.

Both Averbuj and Tsern are in the same field of endeavor as the '434 Patent, *i.e.*, self-testing memory modules (*see* Ex. 1001 at 1:23-25; Ex. 1005 at ¶ [0002]; Ex. 1006 at ¶¶ [0001 & 0097]), and/or at least reasonably pertinent to the problem sought to be solved by the inventors of the '434 Patent, *i.e.*, efficient self-testing of memory modules (*see* Ex. 1001 at 1:26-2:16; Ex. 1005 at ¶¶ [0003-0017]; Ex. 1006 at ¶ [0002]). Tsern, for example, is concerned with the need to remove faulty memory cells through self-testing in the context of the need for memory module systems to keep up with increasing data bandwidth and system memory requirements. Ex. 1006 at ¶¶ [0002 & 0097]. Ex. 1003 ¶ 235.

Tsern discloses a memory module including a number of memory devices, such as DRAM or SRAM devices (Ex. 1006 at ¶ [0035]), and a number of buffer devices, in several embodiments. *See, e.g.*, Ex. 1006 at ¶¶ [0033-0042, 0052-0059]; FIGS. 1 & 9. Tsern further discloses that his memory module may consist of a number of buffer circuits and associated memory devices mounted on a printed circuit board ("PCB"). Ex. 1006 at ¶ [0052], FIG. 9A. Tsern also discloses that his buffer circuits implement the reading and writing of data from and to the

memory devices, and also may include self-test functionality. Ex. 1006 at ¶ [0097]. The use of the printed board of Tsern in the system of Averbuj, in order to mount the memory devices and data generation circuitry for example, would therefore have been merely the use of a known structure for its known purpose to achieve the predictable result of mounting such electronic components in a sturdy and efficient substrate. Ex. 1003 ¶ 236.

It would have been obvious to employ the PCB of Tsern in the system of Averbuj for several reasons. First, it was known that PCBs were relatively inexpensive and sturdy substrates for memory modules and related circuitry. Ex. 1009 at 48-49. Second, PCB memory modules were widely used, standard technology, which a skilled artisan would have preferred over less well known or exotic material for a memory module substrate. *See*, *e.g.*, Ex. 1014 at 1-2 (JEDEC PC2-5300 RDIMM PCB Assembly); Ex. 1015 at 1-10 (JEDEC PC2-5300 RDIMM PCB Layout). Third, Averbuj notes that the device of his system may be, among other things, a computer or server (Ex. 1005 at ¶ [0032]), which commonly included PCB memory modules such as those of Tsern. Fourth, Tsern discloses that his PCB can advantageously include self-test circuitry on the same PCB as the memory devices, which a skilled artisan would have understood was an efficient placement for the self-test data generation circuits of Averbuj, since Averbuj explains that such circuits implement memory operations in accordance with the

specific characteristics of their associated memory devices, so placement close to the associated memory devices would have advantageously limited signal line impedance and simplified wiring paths. Ex. 1010 at 4-6, 56 (reducing EMI and signal crosstalk); Ex. 1020 at 2:27-3:6 (reducing capacitance); Ex. 1021 at 6 (simplifying PCB layout); Ex. 1003 ¶ 237.

Thus, it would have been obvious to use the printed circuit board of Tsern in the system of Averbuj. Ex. 1003 ¶ 238.

### 2. Claim 2 Is Obvious over Averbuj in View of Tsern

To the extent one might argue that Averbuj does not disclose or render obvious this claim element, it also would have been obvious to include "*the plurality of data handlers comprise at least two physically separate components mounted on the printed circuit board*" in the system of Averbuj in view of Tsern.

Tsern discloses a memory module including a number of memory devices, such as DRAM or SRAM devices (Ex. 1006 at ¶ [0035]), and a number of buffer devices. *See, e.g.*, Ex. 1006 at ¶¶ [0033-0042, 0052-0059]; FIGS. 1 & 9. Tsern discloses that these buffer devices are each associated with and interface with one or more memory devices. Ex. 1006 at ¶ [0033]. Ex. 1003 ¶ 240. Tsern further discloses embodiments of buffer devices that do not exchange signals or influence one another and therefore operate independently of each other. *See, e.g.*, Ex. 1006 at ¶¶ [0033-0042, 0052-0059]; FIGS. 1 & 9. Tsern also discloses that these buffer

devices are coupled to data ports of the associated memory devices for purposes of writing data, including test data, into those memory devices. *See, e.g.*, Ex. 1006 at ¶¶ [0077-0101]; FIG. 18. For example, Tsern discloses "redundancy and repair circuit 1883 periodically, during a calibration operation and/or during initialization, tests one or more of memory devices 101 a-d by writing a predetermined plurality of values to a storage location in a selected memory device (for example, using transceiver 1894 and a look-up table storing the predetermined values) using a selected data path and then reading back the stored predetermined plurality of values from the selected memory device using the selected data path." Ex. 1006 at ¶ [0097]. Ex. 1003 ¶ 241.

Tsern also discloses that his buffer and memory devices may be mounted on a printed circuit board substrate. Ex. 1006 at ¶ [0052]. Tsern further discloses that his memory devices and buffer devices may be separate devices that can be housed in separate packages, *id.* at ¶¶ [0031, 0036, 0053]. Ex. 1003 ¶ 242.

Tsern therefore discloses a plurality of circuits for handling data that "*comprise at least two physically separate components mounted on the printed circuit board.*"

It would have been obvious to include the "separate components" configuration of Tsern, including the distribution of self-test circuitry, in the system of Averbuj for several reasons. First, to do so would have been merely the

arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement. Tsern demonstrates that, before the priority date of the '434 Patent, it was within the average skill of the art to include a plurality of data handler circuits in physically separate components, such as separate circuit packages, on a printed circuit board and that such circuits would operate as expected. Ex. 1003 ¶ 244.

A skilled artisan would have been further motivated to include the "separate components" configuration of Tsern in the system of Averbuj, particularly for the Memory Interfaces of Averbuj, in order to reduce the busing area a centralized approach would require. *See*, *e.g.*, Ex. 1017 at 3:45-53 ("It has been proposed to reduce the busing area by using a separate pattern generator for each array to be tested and routing only a simple coded instruction from the controller to the pattern generator to instruct the pattern generator which of a set of canned tests stored in the pattern generator to execute. This approach ***saves on routing area*** at the expense of the area necessary to create individual pattern generators to test a plurality of memories.") (emphasis added). Ex. 1003 ¶ 245.

A skilled artisan also would also have been motivated to include the "separate components" configuration of Tsern in the system of Averbuj so that the self-test circuitry could be conveniently placed in the same packaging as buffer

circuitry used to access and isolate different portions of the memory array. By the priority date of the '434 Patent it was known that separate buffers, in separate packages, for different portions of the memory array could advantageously reduce the load experienced by the memory controllers and improve the memory timing. Ex. 1018 at 1:5-23, FIG. 3; Ex. 1019 at 1:32-2:3, FIG. 5. A skilled artisan would therefore have been motivated to place the Sequencers and the Memory Interfaces of Averbuj within such buffer components in order to reduce the load on the memory controller and also improve memory timing. Ex. 1003 ¶ 246.

Claim 2 is therefore obvious over Averbuj in view of Tsern. Ex. 1003 ¶ 247.

### 3. Claim 3 Is Obvious over Averbuj in View of Tsern

To the extent one might argue that Averbuj does not anticipate or render obvious this claim element, it would have been obvious to include it in the system of Averbuj per the teachings of Tsern.

As demonstrated above with respect to claim 2, Tsern discloses that the buffer circuitry used to access his memory devices, including the circuitry for handling data, may comprise multiple "*physically separate integrated circuit packages.*" *E.g.*, Ex. 1006 at ¶ [0031] ("Likewise in an embodiment, an integrated circuit buffer device is distinguished from a buffer die in that a buffer die is a monolithic integrated circuit formed from semiconductor materials and performs at least one or more buffer functions described herein, *whereas an integrated circuit*

*buffer device is a buffer die having at least some form of packaging or interface that allows communication with the buffer die*." (emphasis added.)); *see also id*. at ¶¶ [0036, 0053] ("In an embodiment, each memory device and buffer device are housed in separate packages.").

It would have been obvious to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj for reasons similar to those set forth above. For example, to do so would have been merely the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement for the same reasons demonstrated above, *i.e.*, Tsern demonstrates that such a configuration was accomplished in the prior art without any unexpected results. Ex. 1003 ¶ 250.

A skilled artisan also would have been motivated to include the "separate packages" configuration of Tsern in the system of Averbuj so that BIST components could be easily replaced or upgraded by simply replacing a standard package on the printed circuit board, without the necessity to replace other BIST circuitry in other packages. Ex. 1003 ¶ 251.

Moreover, as demonstrated above, a skilled artisan would have been motivated to distribute the "*data handlers*" near the buffer circuitry used to access memory devices in order to reduce the routing area needed for bussing. Ex. 1017

at 3:45-53; Ex. 1003 ¶ 252. Physically distributing the "*data handlers*" in that manner would have further motivated, and likely required, a skilled artisan to place the "*data handlers*" in separate packages in order to protect them, as one package holding all data handlers distributed across the printed circuit board would have been infeasible. Ex. 1003 ¶ 252.

Also as demonstrate above, a skilled artisan would also have been motivated to use physically separate integrated circuit packages for the data generation circuitry (44, 45, 48) ("*data handlers*") of Averbuj in order to place each data handler at positions on the PCB close and perhaps closest to its associated memory devices, thereby simplifying the wiring plan on the circuit board (Ex. 1021 at 6; Ex. 1003 ¶ 224), reducing capacitance/propagation delay of the data lines (Ex. 1020 at 2:27-3:6; Ex. 1003 ¶ 225), and reducing the inductance/crosstalk of the data lines (Ex. 1010 at 23-25, 207; Ex. 1003 ¶ 226). Ex. 1003 ¶ 253.

Accordingly, claim 3 is obvious over Averbuj in view of Tsern. Ex. 1003 ¶ 254.

#### 4. Claim 4 Is Obvious over Averbuj in View of Tsern

To the extent one might argue Averbuj does not anticipate or render obvious this claim element, it would have been obvious to include it in the system of Averbuj per the teachings of Tsern.

Tsern discloses his data handler circuitry "*mounted on different portions of the printed circuit board.*" *See, e.g.*, Ex. 1006 at FIG. 9A (Buffers 100a-d); ¶¶ [0031, 0036, 0052, 0053]; Ex. 1003 ¶ 255.

It would have been obvious to adopt such a configuration for the "*data handlers*" of Averbuj because to do so would have been merely the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement, i.e. placing such circuitry closer to the memory devices with which it would interface. Ex. 1003 ¶ 257.

Moreover, as demonstrated above, it was known that distributing data handling circuitry in separate components or packaging placed closer to memory devices associated with that circuitry advantageously provided the ability to isolate the load associated with the memory device and control signal timing more effectively (Ex. 1018 at 1:5-23, FIG. 3; Ex. 1019 at 1:32-2:3, FIG. 5.), and reduced routing area for signal busses (Ex. 1017 at 3:45-53). Ex. 1003 ¶ 258. A skilled artisan would therefore have been motivated to place the data handlers of Averbuj in physically separate integrated circuit packages mounted on different portions of the printed circuit board for each of those reasons, particularly since Averbuj discloses the use of shared circuitry for applying BIST signals and normal operation memory access signals, as explained above. Ex. 1003 ¶ 258.

Further, as demonstrated above, there are only a limited number of places such components could be placed on a standard printed circuit board, so it would have been obvious to try to place each "data handler" at different portions of the board. And a skilled artisan would also have been motivated to place each "data handler" at different portions of the board in order to (i) simplify the wiring paths (so that all connections were not running to/from the same portion of the board) (*see, e.g.*, Ex. 1021 at 6); (ii) permit faster data transmission by reducing the capacitance of the signal lines (*see, e.g.*, Ex. 1020 at 2:27-3:6); and (3) improve signal integrity by reducing impedance on signal lines (*see, e.g.*, Ex. 1010 at 4-6, 56); (iii). Ex. 1003 ¶ 259.

Accordingly, claim 4 is obvious over Averbuj in view of Tsern. Ex. 1003 ¶ 260.

### 5. Claim 5 Is Obvious over Averbuj in View of Tsern

To the extent one might argue that Averbuj does not anticipate or render obvious this claim element, it would have been obvious to include it in the system of Averbuj per the teachings of Tsern. Ex. 1003 ¶ 261.

Tsern discloses placing each of a plurality of data handling circuitry on a printed circuit board near its corresponding plurality of data ports of its associated memory devices. *See* Ex. 1006 at FIGS. 1, 9A (Buffers 100a-d). Thus, Tsern

discloses data handling circuitry that "*is positioned on the printed circuit board proximate to the corresponding plurality of data ports.*" Ex. 1003 ¶ 262.

It would have been obvious to employ such placement with the data handlers of Averbuj because to do so would have been the arrangement of old elements (data handler placed near associated memory devices) with each performing the same function it had been known to perform (the expected ability to access the memory devices via the data handlers) and yielding no more than one would expect from such an arrangement (efficient access to the memory device). Ex. 1003 ¶ 263.

Moreover, a skilled artisan would have been motivated to place the "*data handlers*" of Averbuj nearby and near the data ports of its associated "*memory device*" in order to (i) simplify the wiring (Ex. 1021 at 6; Ex. 1003 ¶ 224), reduce capacitance affecting signal transmission speed (Ex. 1020 at 2:27-3:6; Ex. 1003 ¶ 225), and reduce signal crosstalk affecting signal integrity (Ex. 1010 at 23-25, 207; Ex. 1003 ¶ 226). Ex. 1003 ¶ 264.

Accordingly, claim 5 is obvious over Averbuj in view of Tsern. Ex. 1003 ¶ 265.

### 6. Claim 6 Is Obvious over Averbuj in View of Tsern

To the extent one might argue that Averbuj does not anticipate or render obvious this claim element, it would have been obvious to include it in the system of Averbuj per the teachings of Tsern.

Tsern also discloses placing each of a plurality of data handling circuitry on a printed circuit board closer to the data ports of its associated memory device than other data handling circuitry. *E.g.*, Ex. 1006 at FIGS. 1, 9A. For example, buffer 100a of FIG. 1 of Tsern is closer to the ports of its associated memory devices ("data slice a") than buffers 100b-d are to those data ports. Ex. 1003 ¶ 266.

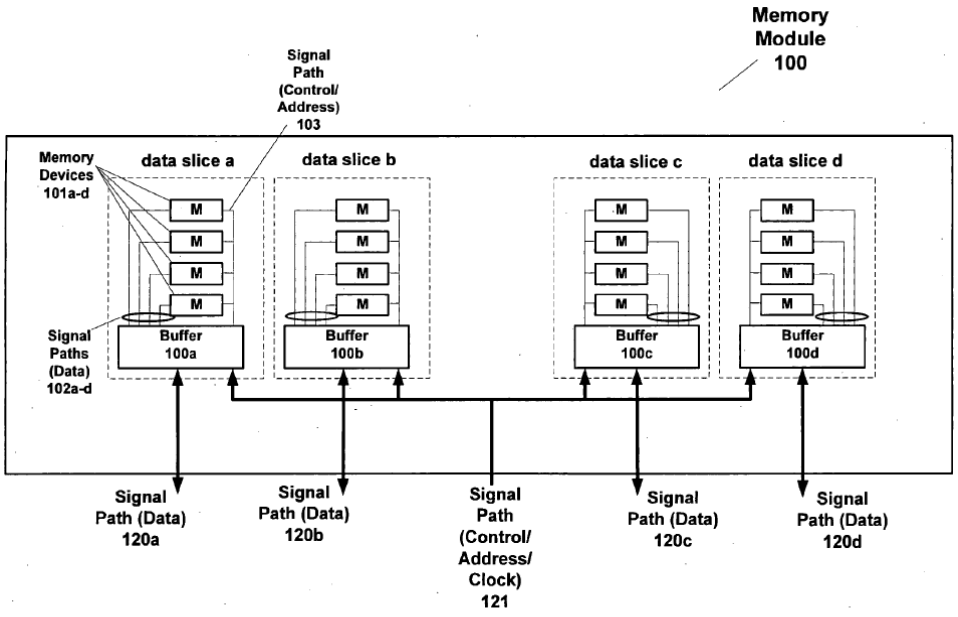



**Fig. 1**
**Ex. 1006 at FIG. 1.**

Thus, Tsern discloses data handling circuitry that "*is positioned closer to the corresponding plurality of data ports than to the other data ports of the plurality of memory devices*." Ex. 1003 ¶ 268.

It would have been obvious to employ such circuit placement with the data handlers of Averbuj because to do so would have been the arrangement of old elements (data handler placed closer to associated memory devices) with each performing the same function it had been known to perform (the expected ability to access the memory devices via the data handlers) and yielding no more than one would expect from such an arrangement (efficient access to the memory device). Ex. 1003 ¶ 269.

Moreover, a skilled artisan would have been motivated to place the "*data handlers*" of Averbuj nearby and closer to the data ports of its associated "*memory device*" in order to (i) simplify the wiring (Ex. 1021 at 6; Ex. 1003 ¶ 224), reduce capacitance affecting signal transmission speed (Ex. 1020 at 2:27-3:6; Ex. 1003 ¶ 225), and reduce signal crosstalk affecting signal integrity (Ex. 1010 at 23-25, 207; Ex. 1003 ¶ 226). Ex. 1003 ¶ 271.

Accordingly, claim 6 is obvious over Averbuj in view of Tsern. Ex. 1003 ¶ 272.

### 7. Claim 7 Is Obvious over Averbuj in View of Tsern

To the extent one might argue Averbuj does not sufficiently disclose this claim element, it would have been obvious to include it in the system of Averbuj in view of Tsern.

Tsern discloses, for example, the inclusion of self-test circuitry in the Redundancy and Repair Circuit 1883 of his buffer device. Ex. 1006 at FIG. 18; ¶ 97. Tsern explains that such circuitry writes data into associated memory cells, reads that data out and then makes a comparison of the written to the read data in order to identify defective memory locations. *See id.* Tsern therefore discloses self-test circuitry that is "*configured to read from the corresponding plurality of data ports and further comprises a verification element for checking for failures in the operation of the memory devices by verifying that data read from the corresponding plurality of data ports corresponds to the data generated by the* [self-test circuitry] *for writing to the corresponding plurality of data ports*." It would have been obvious to include this functionality in the system of Averbuj. Ex. 1003 ¶ 274.

First, to do would have been merely the use of a known technique for its known purpose to achieve a predictable result, *i.e.*, the identification of working and defective memory cells. Ex. 1003 ¶ 275. Moreover, a skilled artisan would have been motivated to include this functionality in Averbuj, since Averbuj is directed to the testing of memory cells and he already discloses writing test data into those cells and the circuitry for comparing such data to data read from those cells. Thus, a skilled artisan would have been motivated to accomplish the goal of

Averbuj – the testing of memory cells using Averbuj's components. Ex. 1003 ¶ 275.

Accordingly, claim 7 is obvious over Averbuj in view of Tsern. Ex. 1003 ¶ 276.

## VII. CONCLUSION

Because the information presented in this petition shows that there is a reasonable likelihood that the Petitioners would prevail with respect to at least one of the claims challenged in the petition, the Petitioners respectfully request that a Trial be instituted and that claims 1-7 of the '434 Patent be canceled as unpatentable.

Dated: January 5, 2017 Respectfully Submitted,

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**PETITION FOR INTER PARTES REVIEW**

**OF U.S. PATENT NO. 8,001,434**

**Attachment A:**
**Proof of Service of the Petition**

**CERTIFICATE OF SERVICE**

I hereby certify that on January 5, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by Federal Express on the following counsel of record for patent owner:

Jamie Zheng
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**PETITION FOR INTER PARTES REVIEW**

**OF U.S. PATENT NO. 8,001,434**

**Attachment B:**
**List of Evidence and Exhibits Relied Upon in Petition**

| Exhibit # | Reference Name |
|---|---|
| 1001 | U.S. Patent No. 8,001,434 |
| 1002 | File History of U.S. Patent No. 8,001,434 |
| 1003 | Declaration of Dr. Pinaki Mazumder |
| 1004 | Curriculum Vitae of Dr. Pinaki Mazumder |
| 1005 | U.S. Patent Publication No. 2005/0257109 to Averbuj ("Averbuj") |
| 1006 | U.S. Patent Publication No. 2007/0070669 to Tsern ("Tsern") |
| 1007 | Excerpts from the American Heritage College Dictionary, 3d Ed. |
| 1008 | Jacob *et al.*, "Memory Systems," 1d Ed. |
| 1009 | Catsoulis, "Designing Embedded Hardware," 2d Ed. |
| 1010 | Montrose, "EMC and the Printed Circuit Board" |
| 1011 | U.S. Patent No. 7,210,059 to Jeddeloh |
| 1012 | Excerpts from the Microsoft Computer Dictionary, 5th Ed. |
| 1013 | Micron MT8JTF12864A DDR3 SDRAM UDIMM Specifications |
| 1014 | JEDEC PC2-5300 RDIMM Assembly V310 (Sept. 2, 2005), available at https://www.jedec.org/sites/default/files/docs/design/DDR2/PC2-5300_RDIMM_V310_RC_P0_20050221.zip |
| 1015 | JEDEC PC2-5300 RDIMM PCB Layout (Sept. 2, 2005), available at https://www.jedec.org/sites/default/files/docs/design/DDR2/PC2-5300_RDIMM_V310_RC_P0_20050221.zip |
| 1016 | U.S. Patent No. 6,271,060 to Zandman |
| 1017 | U.S. Patent No. 6,011,748 to Lepejian |
| 1018 | U.S. Patent No. 6,639,820 to Khandekar |
| 1019 | U.S. Patent No. 6,317,352 to Halbert |

| Exhibit # | Reference Name |
|---|---|
| 1020 | U.S. Patent No. 6,011,710 to Wiggers |
| 1021 | Micron, Technical Note 4720: (Point-to-Point) Package Sizes and Layout Basics, Rev. A, 2006 |
| 1022 | U.S. Patent No. 6,108,798 to Heidel |
| 1023 | U.S. Patent No. 3,588,831 to Figueroa |
| 1024 | U.S. Patent No. 3,618,041 to Horikoshi |