UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner

Patent No. 8,689,064
Issued: April 1, 2014
Filed: January 19, 2013
Inventors: Hyun Lee, Jayesh Bhakta, Soonju Choi
Title: APPARATUS AND METHOD FOR SELF-TEST IN A MULTI-RANK MEMORY MODULE

Inter Partes Review No. 2017-00560

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,689,064 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123

I. INTRODUCTION

This Petition seeks cancellation of claim 16 of U.S. Patent No. 8,689,064 ("the '064 Patent") based, primarily, on U.S. Patent Application Publication No. 2005/0257109 to Averbuj ("Averbuj"). The Board has previously found numerous claims of the 064 Patent's parent and grandparent unpatentable based on Averbuj, *see* IPR2014-00971, Paper 37, IPR2014-00970, Paper 32, claims which are very similar to the challenged claim here. This Petition is based primarily on the analysis accepted by the Board in those prior proceedings. Indeed, there is nothing in claim 16 of the 064 Patent that could distinguish it from Averbuj under the Board's previous analysis, so that claim is also anticipated.

However, the Petition also adds to that analysis and strengthens it. For example, Petitioners address arguments that Patent Owner may raise by proposing one additional ground that more closely satisfies the claim limitations to which such arguments would be directed. Such additional grounds are not redundant because they are "rational, narrowly targeted, and not burdensome considering only [two] claims with very similar limitations are at issue." IPR2015-01912, Paper 10 at 17-18. Petitioners therefore respectfully request that trial be instituted on all grounds and arguments advanced herein.

II. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR *INTER PARTES* REVIEW

A. Mandatory Notices

1. *Real Parties In Interest*

The real parties of interest of this petition are the Petitioners: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

2. *Related Matters*

U.S. Patent No. 8,689,064 ("the '064 Patent") relates to the following legal proceedings: *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 4:13-cv-05889-YGR (N.D. Cal.); *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 2:13-cv-02613-TLN (E.D. Cal.); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No. IPR2014-00970 (PTAB); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No. IPR2014-00971 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01372 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01373 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01374 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01375 (PTAB); *Netlist, Inc. v. SanDisk LLC et al.*, Case Nos. 16-2274, -2338, -2339 (Fed. Cir.); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 16-2666 (Fed. Cir.); *Netlist, Inc. v. SK hynix Inc. et al.*, Case No. 8:16-cv-01605-JLS (C.D. Cal.); and *In re Certain Memory Modules & Components Thereof*, Inv. No. 337-TA-1023 (ITC).

In addition, petitions for *inter partes* review of U.S. Patent Nos. 8,001,434 (IPR2017-00561) and 8,359,501 (IPR2017-00562), which are related to the '064 Patent, are being filed concurrently with this petition.

3. *Lead & Backup Counsel*

Lead Counsel is: Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492. Backup Lead Counsel are: Steven S. Baik (Reg. No. 42,281), Sidley-SKH-IPR@sidley.com, (650) 565-7016; Wonjoo Suh (Reg. No. 64,124), Sidley-SKH-IPR@sidley.com, (202) 736-8831; Ryuk Park (*pro hac vice*), Sidley-SKH-IPR@sidley.com, (650) 565-7074.

4. *Service Information*

Service on Petitioners may be made by e-mail (Sidley-SKH-IPR@sidley.com), or by mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

B. Fee for *Inter Partes* Review (37 C.F.R. § 42.15(a))

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 50-1597.

C. Certification of Word Count (37 C.F.R. § 42.24(a)(1))

Petitioners certify that this petition for *inter partes* review contains 3,608 words, excluding the parts of that are exempted by 37 C.F.R. § 42.24(a)(1), per the count of the word-processing system used to prepare this petition.

D. Certification of Standing (37 C.F.R. § 42.104(a))

Petitioners certify they are not barred or estopped from requesting *inter partes* review of the ’064 Patent (Ex. 1001). This petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of the ’064 Patent. Neither Petitioners nor any party in privity with Petitioners has filed a civil action challenging the validity of any claim of the ’064 Patent. The ’064 Patent has not been the subject of a prior *inter partes* review by Petitioner or a privy of Petitioners. Petitioners therefore certify this patent is available for *inter partes* review.

E. Proof of Service (37 C.F.R. §§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Claims 16 of the '064 Patent are unpatentable as follows:

1. Claim 16 of the '064 Patent is unpatentable as anticipated under 35 U.S.C. § 102 by U.S. Patent Publication No. 2005/0257109 by Averbuj ("Averbuj"); and
2. Claim 16 of the '064 Patent is unpatentable as obvious under 35 U.S.C. § 103 over Averbuj.

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ **IV-VI**, below. The evidence relied upon in this petition is listed in **Attachment B**.

IV. RELEVANT INFORMATION CONCERNING THE '064 Patent

A. Effective Filing Date of the '064 Patent

The application that resulted in the '064 Patent is U.S. Patent Application Serial No. 13/745,790, filed January 19, 2013. Ex. 1001 at 1. The '064 Patent is a continuation of U.S. Patent Nos. 8359,501 and 8,001,434, and claims priority to Provisional Application Nos. 61/044,801, 61/044,805, and 61/044,839, filed on April 14, 2008. *Id.* Patent Owner contended, in a related proceeding, that the conception date of the '064 Patent is June 21, 2007. While Petitioners disagree with Patent Owner's assertion of an earlier conception date, Petitioners assumes for purposes of this proceeding only that the challenged claims of the '064 Patent have an effective filing date of June 21, 2007.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the '064 Patent would have been someone with "a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST." IPR2014-00970, Paper 32 (Final Written Decision) at 10-11; IPR2014-00971, Paper 37 (Final Written Decision) at 9-11; Ex. 1003 at ¶ 51.

C. Overview of the '064 Patent

The '064 Patent discloses a self-testing memory module for testing a plurality of memory devices using a control module that generates or provides address and control signals, and a data module comprising a plurality of data handlers that generate or provide data signals. Ex. 1001 at Abstract, 2:30-34, 9:27-29, Fig. 3; Ex. 1003 at ¶ 52.

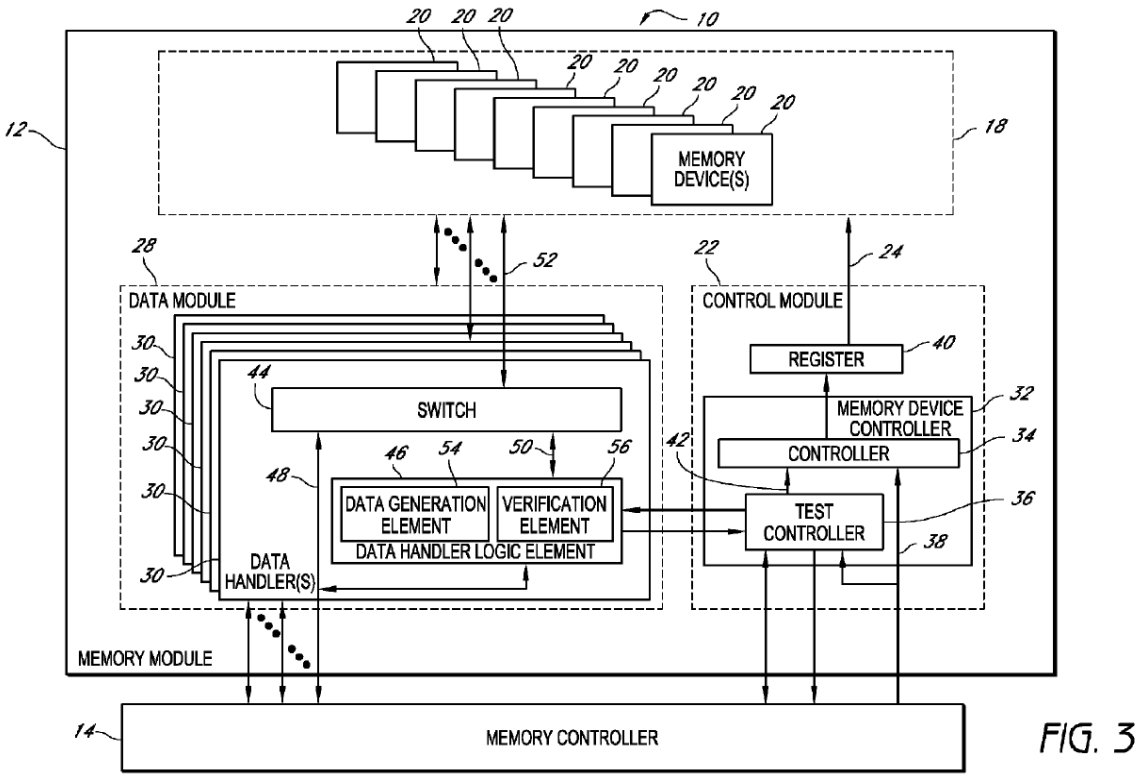


FIG. 3

Ex. 1001 at Fig. 3.

The control module (22) receives address and control signals (38) from the system memory controller (14), also generates the test address and control signals (42). Ex. 1001 at 9:44-49, 54-57, Fig. 3; Ex. 1003 at ¶ 53. The data module (28) includes one or more of data handlers (30), each of which receives data signals (48) from the system memory control (14), and also generates test data signals (50) based on signals it receives from the control module (22). Ex. 1001 at 10:4-7, 10:10-15, 10:34-41, Fig. 3; Ex. 1003 at ¶ 54. When the memory module (10) is operating in test mode, each data handler (30) writes the test data to one or more memory devices (20), reads data from the same memory device(s) (20), and

verifies that data read from the memory devices corresponds to the test data written to the memory device(s) (20). Ex. 1001 at 11:9-19, Fig. 3; Ex. 1003 at ¶ 55.

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 C.F.R. § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48764 at II.B.6 (August 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

The Board has previously interpreted certain claim terms of U.S. Patent Nos. 8,001,434 ("the '434 Patent") and 8,359,501 ("the '501 Patent"), both of which are parents of the '064 Patent. For the purposes of this proceeding only, Petitioner adopts the Board's interpretations and therefore applies those same interpretations, as set forth below:

1. *"configured to" (claim 16)*

The Board previously construed the term "*configured to*" recited in the '434 Patent and the '501 Patent as "designed to, adapted to, or arranged to [e.g., perform a function or be capable of performing a function]." IPR2014-00970, Paper 32 at 20-24, 33; IPR2014-00971, Paper 37 at 18-22, 31. This construction is consistent

with the ’064 Patent’s disclosure and skilled artisans’ understanding and usage of the term. *See e.g.*, Ex. 1001 at 7:25-31; Ex. 1007 at 292 (dictionary definition of “configure”). Further, the Patent Owner’s expert, Dr. Sechen, previously offered testimony supporting the Board’s construction. *See* IPR2014-00970, Paper 32 at 24 (“Dr. Sechen testified that ‘configured to’ in the context of the phrase ‘configured to be operatively coupled … might mean designed [to].’”).

2. *“generate” (claim 16)*

The Board previously construed the term “generate” recited in the ’434 Patent and the ’501 Patent as “produce.” IPR2014-00970, Paper 32 at 24-33; IPR2014-00971, Paper 38 at 22-31. This construction is consistent with the ’064 Patent’s disclosure. *See e.g.*, Ex. 1001 at 5:48-55, 6:11-17, 9:29-31, 10:31-41.

V. OVERVIEW OF THE PRIOR ART

A. U.S. Patent Publ. 2005/0257109 to Averbuj (Ex. 1005)

U.S. Patent Publication No. 2005/0257109 by Averbuj *et al.* (“Averbuj”) was published on November 17, 2005. Therefore, Averbuj is prior art to the ’064 Patent under 35 U.S.C. §§ 102(a), (b), and (e).

Averbuj is titled “Built-In Self Test (BIST) Architecture Having Distributed Interpretation and Generalized Command Protocol.” Ex. 1005 at 1. Averbuj is generally directed to a hierarchical built-in self-test (“BIST”) architecture for testing memory modules of an electronic device. Ex. 1005 at Abstract, ¶ [0007], Fig. 1; Ex. 1003 at ¶ 63.

The electronic device (2) of Averbuj includes a BIST controller (4) and a plurality of device blocks (12). Each device block (12) includes a sequencer, one or more memory interfaces (10), and one or more corresponding memory modules (12). Ex. 1001 at Figs. 1, 4.

FIG. 1

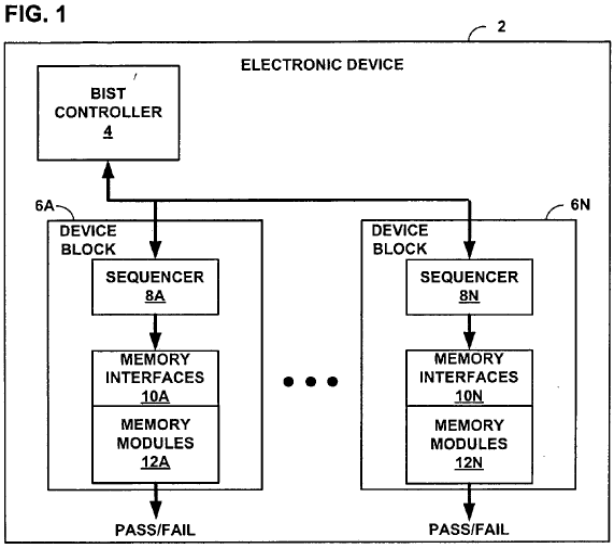
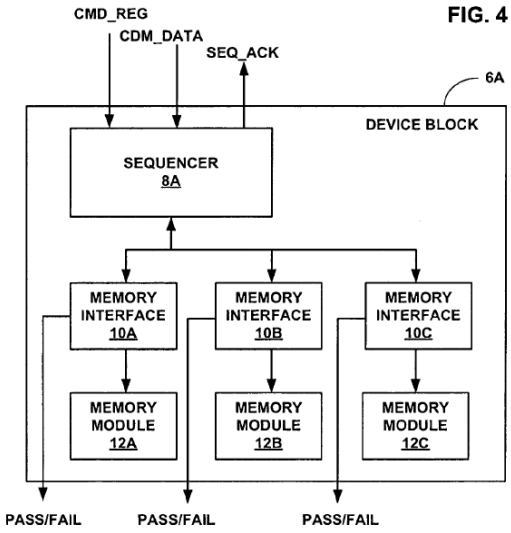
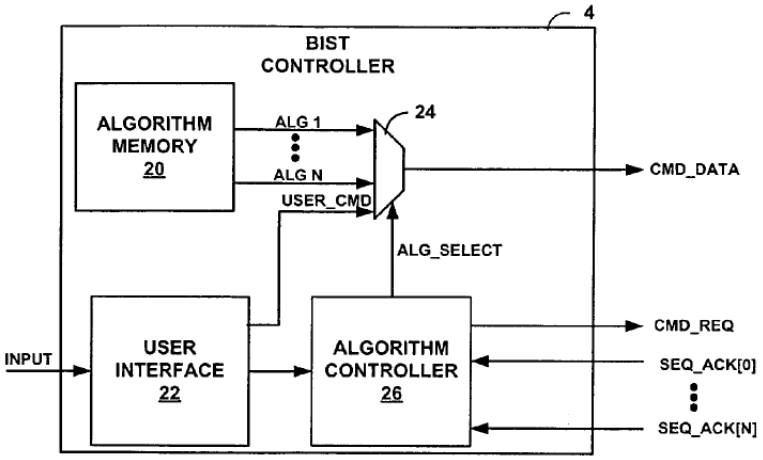


FIG. 4



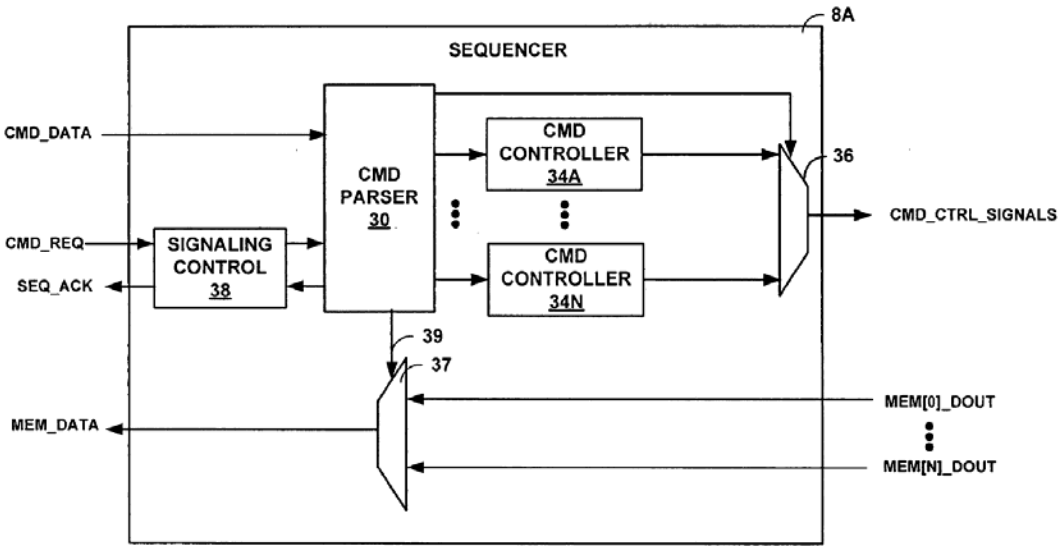
Ex. 1005 at Figs. 1 & 4.

The BIST controller (4) provides centralized, high-level control over the testing of the memory modules (12) by issuing test commands to the sequencers (8) of the device blocks (6). Ex. 1005 at ¶¶ [0008], [0029], [0033-0036], Fig. 2 (see below); Ex. 1003 at ¶ 64.



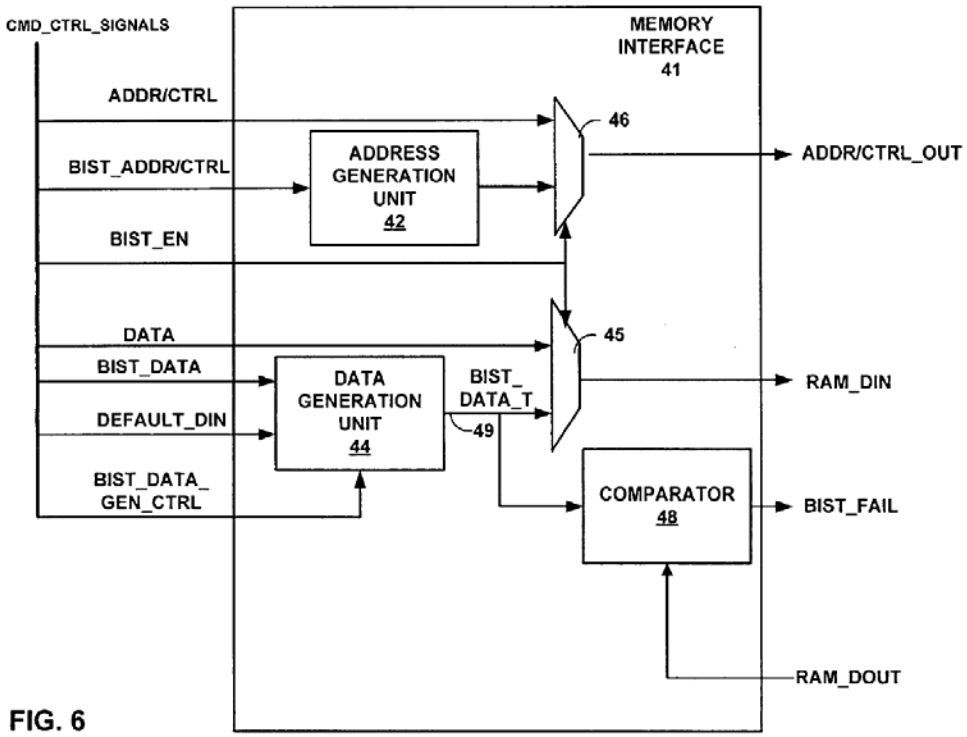
Ex. 1005 at Fig. 2.

Each sequencer (8) receives address and control signals from a programmable processor (for normal mode) and test commands from the BIST controller (for self-test mode), and also generates test address and control signals for controlling the operations of the one or more memory modules (12) and other BIST circuitry within the corresponding device block (6). Ex. 1005 at ¶¶ [0009], [0030], [0040-0044], Fig. 5 (see below); Ex. 1003 at ¶ 65.



Ex. 1005 at Fig. 5.

Each memory interface (10, 41) receives data signals, *e.g*, from a programmable processor. Ex. 1005 at ¶ [0048], Fig. 6; Ex. 1003 at ¶ 66. The data generation unit (44) of each memory interface (10, 41) also generates test data signals for testing a corresponding memory module (12) according to the control signals received from a controlling sequencer (8). Ex. 1005 at ¶¶ [0049-0050], [0055-0057], Figs. 6-7; Ex. 1003 at ¶ 66. The multiplexer (45) of each memory interface (10, 41) selects either the data signals from the programmable processor or the test data signals generated by the data generation unit (44) according to the control signals received from the controlling sequencer (8). Ex. 1005 at ¶¶ [0048-0049], Fig. 6 (see below); Ex. 1003 at ¶ 66.



Ex. 1005 at Fig. 6.

During self-test mode, the data generation unit (44), multiplexer (45), and comparator (48) write the test data to the memory module (12), read out data from the same memory module (12), and check whether the data read out of the memory module (12) equals the data written to the memory module (12). Ex. 1005 at ¶¶ [0049], [0053], Figs. 6, 10; Ex. 1003 at ¶ 67.

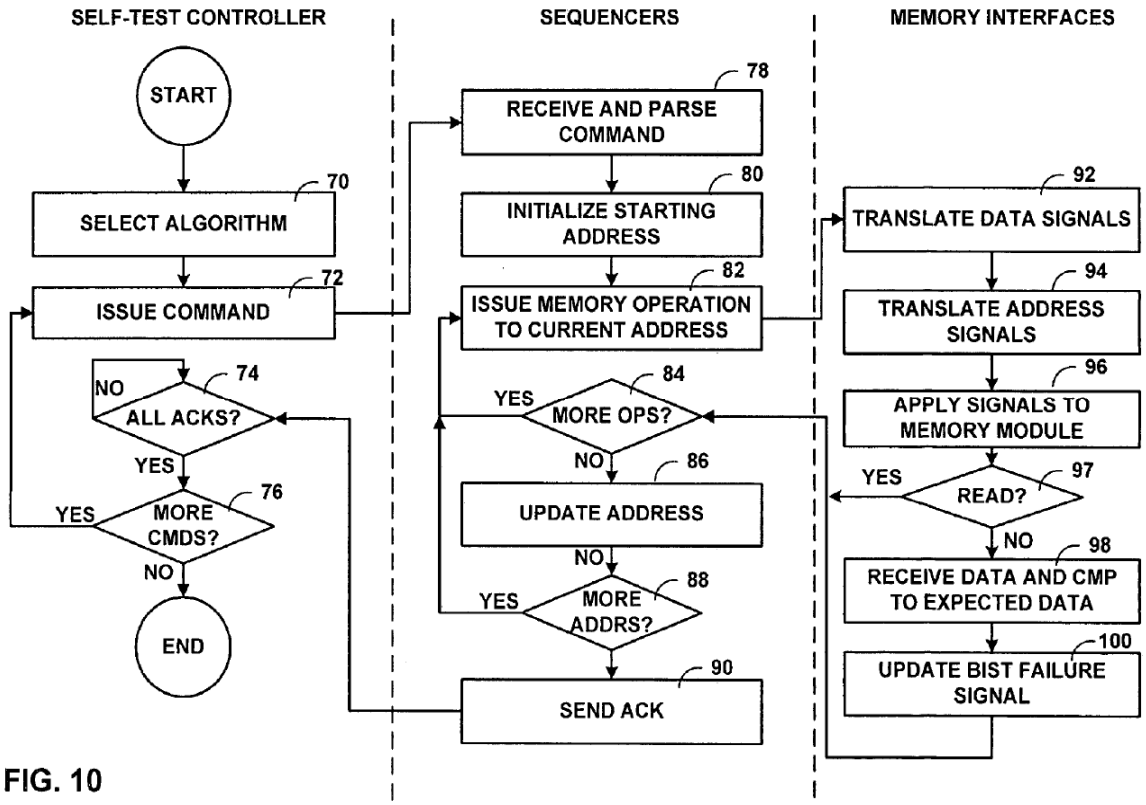


FIG. 10

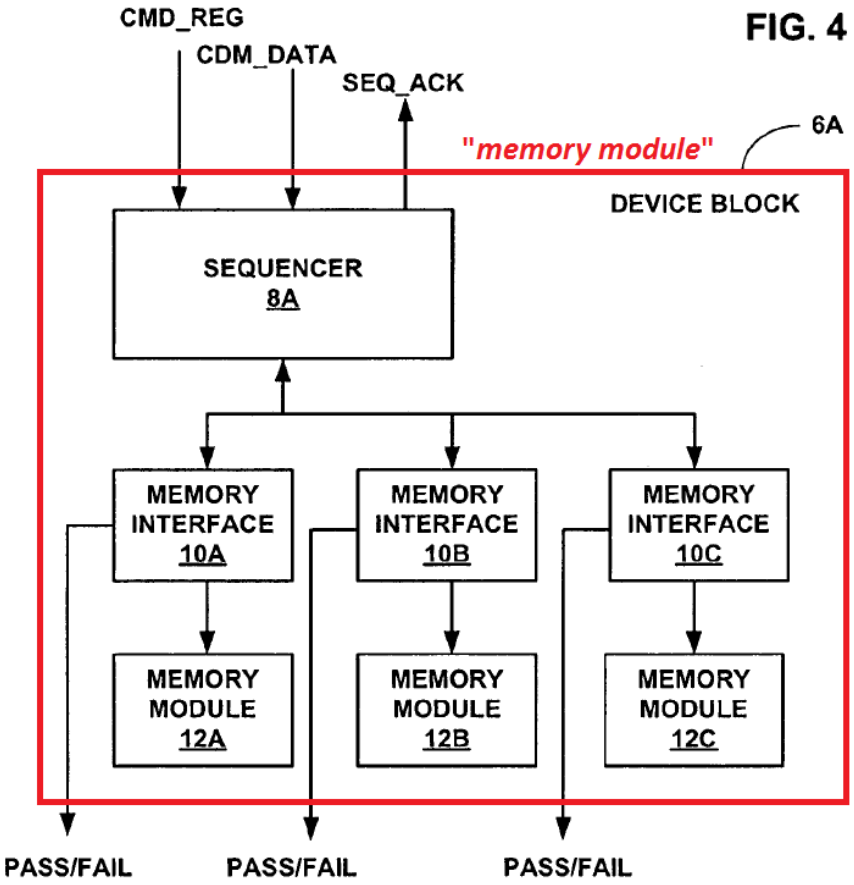
Ex. 1005 at Fig. 10.

VI. PRECISE REASONS FOR RELIEF REQUESTED

B. Claim 16 Is Anticipated By Averbuj

1. Preamble

The preamble of claim 16 requires "*[a] memory module for operating with a system memory controller*."



Ex. 1005 at Fig. 4 (annotated and highlighted).

Fig. 1 of Averbuj illustrates an electronic device (2) that includes a BIST controller (4) and a plurality of device blocks (6A-N). Ex. 1005 at ¶ [0028], Fig. 1; Ex. 1003 at ¶ 69. Each device block (6A), as further depicted in Fig. 4 of Averbuj, includes one or more memory modules (12), such as Flash memory or DRAM. Ex. 1005 at ¶¶ [0032], [0039], Fig. 4; Ex. 1003 at ¶ 69. Each device block (6A-N) of Averbuj is therefore "*a memory module*" as claimed. *Id.*

The BIST controller (4) operates as a centralized memory controller during test mode by sending test commands (CMD_DATA and CMD_REQ) to the device blocks ("*memory modules*") of the system and monitoring the status of the memory

testing operation (*e.g.*, SEQ_ACK). Ex. 1005 at ¶¶ [0008], [0029], [0033-0037]; Figs. 1, 2; Ex. 1003 at ¶ 70. Therefore, the BIST controller is "*a system memory controller*" as claimed. *Id.*

Alternatively, in one embodiment, a "programmable processor" also provides address, control, and data signals to the device blocks (6) ("*memory modules*"), which are applied to the memory modules (12) during normal mode. Ex. 1005 at ¶ [0048]; Fig. 6; Ex. 1003 at ¶ 71. The "programmable processor" disclosed in Averbuj is, or includes, "[*a system] memory controller*" as claimed because it provides the address, control, and data signals to, and thereby controls the data flow of, the memory modules of an electronic device such as an "embedded computing system, computer, [or] server" Ex. 1005 at ¶ [0032]; Ex. 1008 at 497; Ex. 1009 at Fig. 1-2 ; Ex. 1003 at ¶¶ 72-74.

Accordingly, Averbuj discloses the preamble of claim 16.

2. *"a module controller"*

Claim 16 requires "*[1] a module controller [2] to process input control signals from the system memory controller and [3] to generate output control signals.*"

Each sequencer (8) "control[s] the application of the test algorithms to a plurality of memory modules" of a corresponding device block ("*memory*

module"). Ex. 1005 at ¶¶ [0009], [0010]; *see also id*. at ¶ [0030], Fig. 4; Ex. 1003 at ¶ 76. Each sequencer is therefore "*a module controller*" as claimed. *Id.*

Each sequencer (8) receives test command signals (CMD_REQ and CMD_DATA) from the BIST controller ("*system memory controller*") and "processes the received command" to identify the specified test operation. Ex. 1005 at ¶ [0041]; *see also id.* at ¶¶ [0037-0038], Fig. 2; Ex. 1003 at ¶ 77. The test command signals from the BIST controller are "*control signals*" because the test command signals encode instructions to be carried out by the sequencer (8) and thus control the operation of the sequencer. Ex. 1005 at ¶¶ [0037-0038], [0041], [0061], Fig. 9; Ex. 1003 at ¶ 78. The sequencer therefore "*process[es] input control signals from the system memory controller*." *Id.* at ¶ 79.

Alternatively, the sequencer (8) receives address, control, and data signals from, for example, a programmable processor and processes them for inclusion in its output signal. Ex. 1005 at ¶ [0048], Fig. 6; Ex. 1003 at ¶ 80. In this regard, the sequencer also "*process[es] input control signals from the system memory controller*." *Id.*

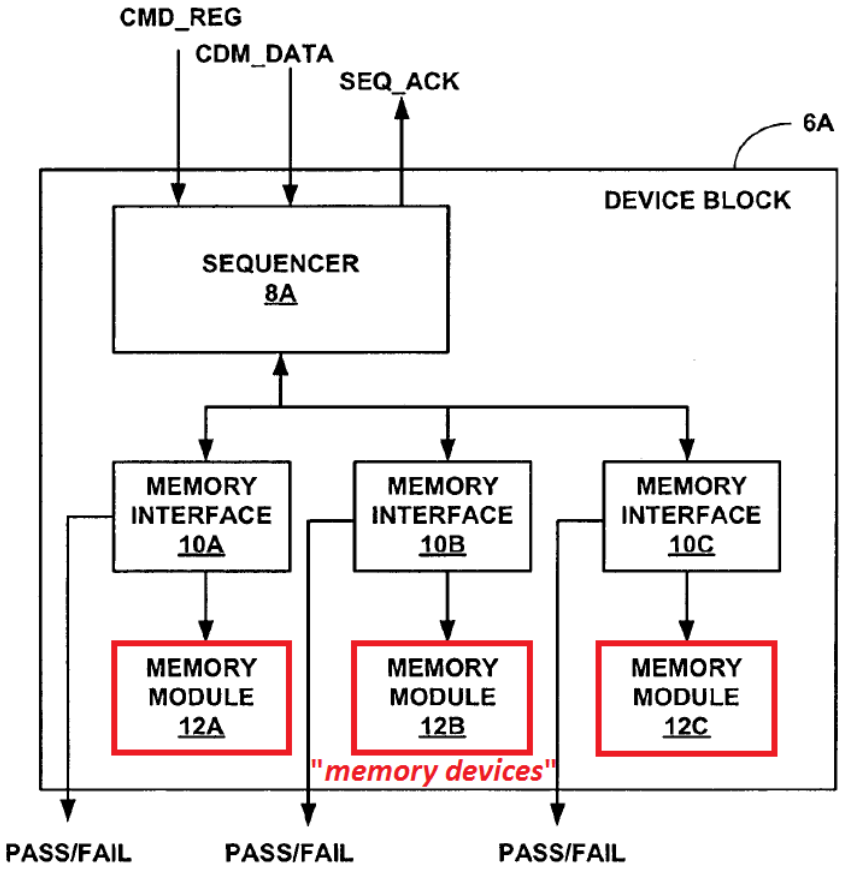
As a result of such processing, the sequencer produces ("*generate[s]*") the CMD_CTRL_SIGNALS, which includes control signals for the memory modules (*e.g.*, BIST_CTRL) and the BIST circuitry (*e.g.*, BIST_EN, BIST_DATA_GEN_CTRL) ("*output control signals*"). Ex. 1005 at Figs. 5-7; Ex.

1003 at ¶ 81. The sequencer therefore "*generate[s] output control signals*" as claimed. *Id.; see also* IPR2014-00971, Paper 37 at 41 ("Averbuj describes 'operating a control circuit [(i.e., a sequencer)] to generate address and control signals' …") (parenthesis in original).

Accordingly, Averbuj discloses this claim element. Ex. 1003 at ¶ 83.

3. *"a plurality of memory devices"*

Claim 16 requires "*[1] a plurality of memory devices [2] configured to perform memory operations in response to signals from the module controller*."



Ex. 1005 at Fig. 4 (annotated and highlighted).

Averbuj discloses that the memory modules (12) of a device block (6) "may be any type of memory, such as random access memory (RAM), read-only memory (ROM), Flash memory, dynamic random access memory (DRAM), SDRAM, RDRAM, DDR-RAM," each of which is a different memory device. Ex. 1005 at Fig. 4, ¶ [0032]; Ex. 1003 at ¶ 85. The memory modules (12) of a device block (6) are therefore "*a plurality of memory devices*" as claimed. *Id.*

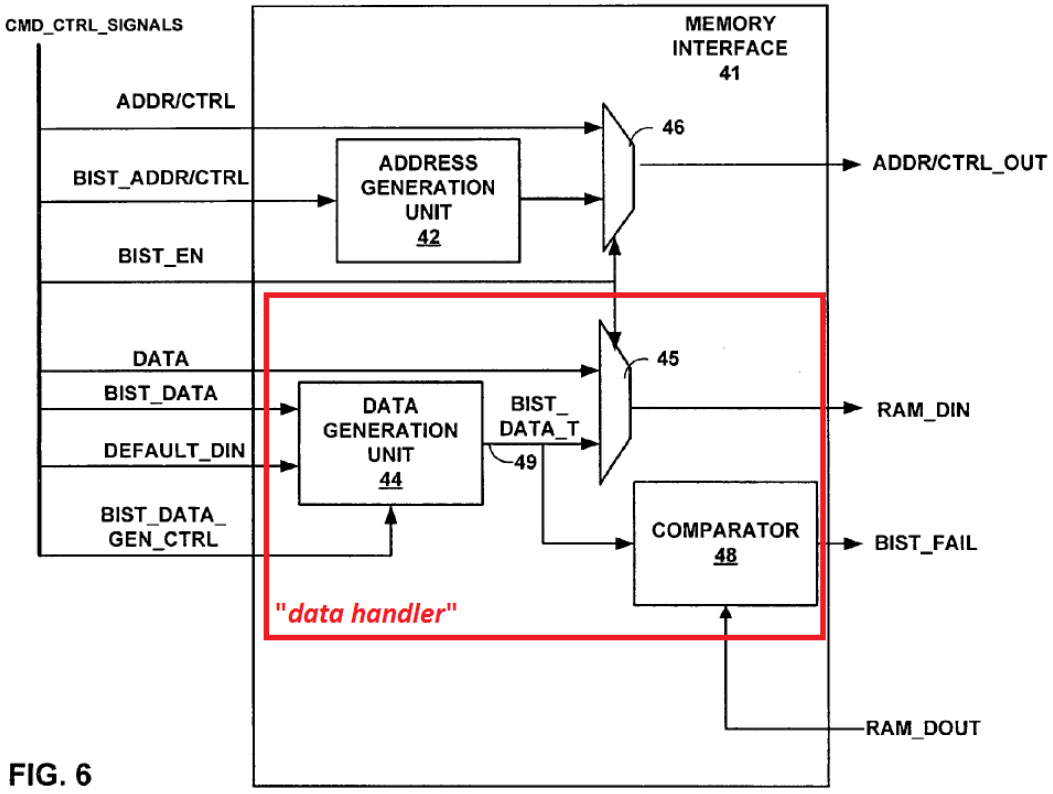
Each memory modules (12) ("*memory devices*") operate according to the address, control, and data signals asserted on the ADDR/CTRL_OUT and RAM_DIN ports of the corresponding memory interface (41). Ex. 1005 at ¶ [0048], Fig. 6; Ex. 1003 at ¶ 86. The output address, control, and data signals (ADDR/CTRL_OUT and RAM_DIN) are selected "*in response to*" the BIST_EN signal received from the sequencer (8). Ex. 1005 at ¶ [0048], Figs. 5-6; Ex. 1003 at ¶ 86. Further, the test data signal (BIST_DATA_T) is generated (by the data generation unit of the memory interface) "*in response to*" the BIST_DATA_GEN_CTRL signal from the sequencer (8). Ex. 1005 at ¶ [0049], [0055-0057], Figs. 6-7; Ex. 1003 at ¶ 86. The memory modules (12) ("*memory devices*") are therefore "*configured to perform memory operations in response to signals from the module controller*" as claimed. *Id.*

Accordingly, Averbuj discloses this claim element. *Id.* at ¶ 87.

4. *"a plurality of data handlers"*

Claim 16 requires "*[1] a plurality of data handlers, [2] each respective data handler being configured to generate test data and [3] to provide the test data to a respective set of at least one memory device of the plurality of memory devices [4] in response to signals from the module controller*."

The device block (6) depicted in Fig. 4 of Averbuj includes a plurality of memory interfaces (10), each of which interfaces with a corresponding memory module (12). Ex. 1005 at ¶ [0031], Fig. 4; Ex. 1003 at 89.



Ex. 1005 at Fig. 6 (annotated and highlighted).

In one embodiment, as shown in Fig. 6 of Averbuj, each memory interface (10, 41) includes a data generation unit (44), an associated multiplexer (45), and an

associated comparator (48). Ex. 1005 at Fig. 6; Ex. 1003 at ¶ 89. The data generation unit (44) and the associated multiplexer (45) and comparator (48) of each memory interface constitute a "*data handler*" because they writes data to and read data from the corresponding memory module (12). Ex. 1005 at Fig. 4, 6; Ex. 1003 at ¶ 89. Accordingly, the plurality of data generation units (44), associated multiplexers (45) and comparators (48) in the plurality of memory interfaces (10, 41) disclosed in Averbuj constitute "*a plurality of data handlers*."

The data generation unit (44) ("*data handler*") is designed to produce ("*configured to generate*") the BIST_DATA_T signal ("*test data*") for its corresponding memory module (12) by transforming the BIST_DATA signal from the sequencer (8). Ex. 1005 at ¶¶ [0049], [0050], [0057], Fig. 7; Ex. 1003 at ¶ 90. The data generation unit (44) ("*data handler*") transforms the BIST_DATA signal from the sequencer (8) into a BIST_DATA_T signal "*in response to*" the BIST_INVERT_BITS and BIST_INVERT_ROWS signals from the sequencer (8) ("*signals from the module controller*"). Ex. 1005 at ¶¶ [0055-0057], Figs. 6-7; Ex. 1003 at ¶ 91. Averbuj therefore discloses "*a plurality of data handlers, each respective data handler being configured to generate test data … in response to signals from the module controller*" as claimed.

The associated multiplexer (45) is designed to ("*configured to*") select the generated BIST_DATA_T signal ("*test data*") and provide it to the memory

module (12) ("*memory device*") through the RAM_DIN port during self-test mode. Ex. 1005 at ¶ [0049], Fig. 6; Ex. 1003 at ¶ 92. The associated multiplexer (45) selects the BIST_DATA_T signal ("*test data*") "*in response to*" the BIST_EN signal from the sequencer (8) ("*signals from the module controller*"). Ex. 1005 at ¶ [0047], Fig. 6; Ex. 1003 at ¶ 93. Averbuj therefore discloses "*a plurality of data handlers, each respective data handler being configured to … provide the test data to a respective set of at least one memory device of the plurality of memory devices in response to signals from the module controller*" as claimed. Ex. 1003 at ¶ 93.

Accordingly, Averbuj discloses this claim element. *Id.*

5. *"wherein the memory module is configured to obtain test results"*

Claim 16 requires that "*the memory module is [1] configured to obtain test results [2] by reading from the respective set of at least one memory device in response to signals from the module controller and [3] by comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device*."

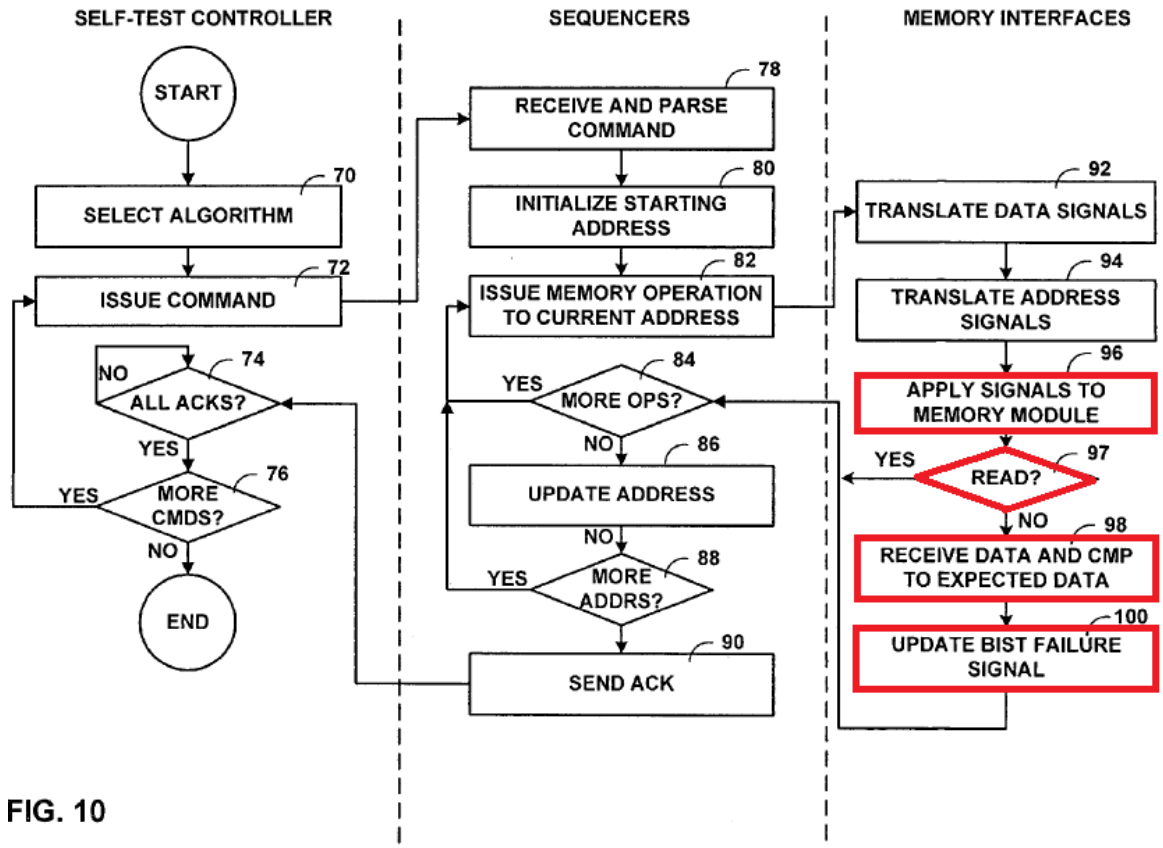


FIG. 10

Ex. 1005 at Fig. 10 (highlighted).

As explained above, during self-test mode, the BIST_DATA_T signal ("*test data*") is generated by the data generation unit ("*data handler*") and written to the memory module (12) ("*the respective set of at least one memory device*") through the RAM_DIN port. *See* § V.A.4, above; Ex. 1003 at ¶ 96.

After the BIST_DATA_T signal ("*test data*") is written to a memory module (12), the memory interface (41) reads the data from the same addresses of the corresponding memory module (12) ("*respective set of at least one memory device*") through the RAM_DOUT port, as instructed by the sequencer via the ADDR/CTRL port ("*in response to signals from the module controller*"). Ex.

1005 at ¶ [0053], Fig. 6; Ex. 1003 at ¶ 97. Averbuj therefore discloses "*reading from the respective set of at least one memory device in response to signals from the module controller*" as claimed.

The comparator (48) compares the data that is read out from the memory module (12) to the data that was previously written to the same address of the memory module (12) to determine if they are identical. Ex. 1005 at ¶ [0053], Fig. 6, 10; Ex. 1003 at ¶ 98. Averbuj therefore discloses "*comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device*" as claimed.

When the comparison fails, the comparator (48) asserts the BIST_FAIL signal ("*test result*") to indicate a memory error. Ex. 1005 at ¶ [0053], Fig. 10. Ex. 1005 at ¶ [0053]; Ex. 1003 at ¶ 99. Averbuj therefore discloses that the device block ("*memory module*") is "*configured to obtain test results*" as claimed.

Accordingly, Averbuj discloses this claim element.

B. Claim 16 Is Obvious Over Averbuj

1. *"a module controller to process input control signals from the system memory controller"*

To the extent one might argue that Averbuj does not anticipate claim 16 of the '064 Patent because it does not disclose "*a module controller to process input control signals from the system memory controller*," it would have been obvious to include that element in the system of Averbuj. Ex. 1003 at ¶ 101.

Averbuj discloses that his electronic device can be a "computer [or] server" that incorporates a variety of memory modules, such as DRAM and Flash memory. Ex. 1005 at ¶ [0032]; Ex. 1003 at ¶ 102. Averbuj discloses that the device blocks ("*memory module*") in his electronic system receives address/control signals (ADDR/CTRL) and data signals (DATA) from a programmable processor and applies those signals under normal operating conditions. Ex. 1005 at ¶ [0048], Figs. 5, 6; Ex. 1003 at ¶ 102.

At the time, memory controllers were commonly used in computers and servers in order to manage access to the memory systems. *See e.g.*, Ex. 1008 at 315-316, Fig. 7.2 (showing a "Memory Controller"); Ex. 1011 at Figs. 1- 2 (showing a "Memory Hub Controller" and "Memory Controller"); Ex. 1023 at Fig. 1 (showing a "memory controller"); Ex. 1024 at Fig. 1 (showing a "common memory controller"); Ex. 1003 at ¶ 103. Thus, to use a system memory controller to manage memory accesses in the system of Averbuj by providing the device blocks with address, control, and data signals would have been the use of known techniques and structures in their known ways to achieve the predictable result of accessing memory. Ex. 1003 at ¶ 103.

A skilled artisan would have been motivated to use a memory controller with the device of Averbuj for a number of reasons. A memory controller could relieve the main processor of the burden of complying with the complex interface

protocols and requirements of the memory system and thus improve the overall performance of a computer or server. *See e.g.*, Ex. 1008 at 497-498; Ex. 1003 at ¶ 104. A memory controller could also efficiently arbitrate and schedule simultaneous requests by multiple components to access the memory system and therefore avoid resource scheduling conflicts and improve throughput, especially in a multi-processor environment. Ex. 1008 at 498, Fig. 13.1 ; Ex. 1003 at ¶ 105. For these reasons, a skilled artisan would have been motivated to include a memory controller in a computer or server, such as the computer or server contemplated in Averbuj. Ex. 1003 at ¶ 106.

Accordingly, the use of a memory controller to manage access to the device blocks and memory modules in Averbuj's electronic device would have been obvious to a skilled artisan. Ex. 1003 at ¶ 107.

VII. CONCLUSION

Because the information presented in this petition shows that there is a reasonable likelihood that the Petitioners would prevail with respect to at least one of the claims challenged in the petition, the Petitioners respectfully request that a Trial be instituted and that claim 16 of the ’064 Patent canceled as unpatentable.

Dated: January 3, 2017

Respectfully Submitted,

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 8,689,064

Attachment A:
Proof of Service of the Petition

CERTIFICATE OF SERVICE

I hereby certify that on January 3, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

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Attachment B:
List of Evidence and Exhibits Relied Upon in Petition

Exhibit #	Reference Name
1001	U.S. Patent No. 8,689,064
1002	File History of U.S. Patent No. 8,689,064
1003	Declaration of Dr. Pinaki Mazumder
1004	Curriculum Vitae of Dr. Pinaki Mazumder
1005	U.S. Patent Publication No. 2005/0257109 to Averbuj ("Averbuj")
1006	[Reserved]
1007	Excerpts from the American Heritage College Dictionary, 3d Ed.
1008	Jacob *et al.*, "Memory Systems: Cache, DRAM, Disk," 1d Ed.
1009	Catsoulis, "Designing Embedded Hardware," 2d Ed.
1010	[Reserved]
1011	U.S. Patent No. 7,210,059 to Jeddeloh
1012	[Reserved]
1013	[Reserved]
1014	[Reserved]
1015	[Reserved]
1016	[Reserved]
1017	[Reserved]
1018	[Reserved]
1019	[Reserved]
1020	[Reserved]
1021	[Reserved]

Exhibit #	Reference Name
1022	[Reserved]
1023	U.S. Patent No. 3,588,831 to Figueroa
1024	U.S. Patent No. 3,618,041 to Horikoshi