IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Gerald J. Banks
U.S. Patent No.:	5,764,571
Issue Date:	June 9, 1998
Serial No.:	08/410,200
Filing Date:	Feb. 27, 1995
Title:	Electrically Alterable Non-Volatile Memory With N-Bits Per Cell

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REQUEST FOR EX PARTE REEXAMINATION
UNDER 35 U.S.C. § 302 AND 37 C.F.R. § 1.510

Reexamination under 35 U.S.C. § 302 and 37 C.F.R. § 1.510 is requested for claims 1, 9, 12, 30, 42, and 45 of U.S. Patent No. 5,764,571 (the ’571 patent), which issued on June 9, 1998 to assignee BTG USA Inc.

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I. INTRODUCTION

The ’571 patent is generally directed to an “electrically alterable, non-volatile multi-bit memory cell.” The specification and prosecution history indicate that the alleged patentability of the claims challenged in this request lies in combining two well-known types of multi-level cell (“MLC”) memory devices: read-only, non-volatile memory such as multi-bit ROM, and electrically programmable, volatile memory such as multi-bit DRAM) to create a non-volatile, electrically-alterable MLC device. *See* Ex. A at 2:31-46.

The prior art and evidence described in this request demonstrate that the challenged claims are unpatentable for three simple and independent reasons. First, a prior art Japanese patent application to Kitamura that was not considered during original prosecution had already made the purported combination that formed the basis for alleged patentability. Kitamura describes an electrically programmable, non-volatile, multi-level cell memory device and a programming technique as claimed in the ’571 patent. MLC attempted to distinguish Kitamura in an *Inter Partes Review* (“IPR”) proceeding by arguing that a D/A converter disclosed as part of the memory apparatus in Kitamura performs only a voltage “converting” function, rather than a voltage “selecting” function as claimed in the ’571 patent. However, as demonstrated by three previously unconsidered prior art references submitted with this request, conventional D/A converters that were known long before the ’571 patent was filed performed the very same “selecting” function described and claimed in the ’571 patent. Kitamura has never been considered by the PTO in combination with any of these three prior art references. Kitamura combined separately with each such reference therefore raises three independent substantial new questions of patentability.

Second, evidence newly discovered by the Requester in a co-pending litigation—including the inventor’s notebook and prior sworn deposition testimony—flatly contradicts assertions made by the patent owner to preserve the alleged validity of the ’571 patent in IPR. This evidence was never disclosed by the patent owner (an LLC of which the inventor is a current member) to the USPTO despite the fact that it debunks the patent owner’s previous statements to the USPTO. The inventor’s notebook and prior testimony show that the PTAB’s decision denying institution of IPR in view of Kitamura was a direct result of false and misleading statements of the patent owner. This new evidence further supports that Kitamura in

view of the previously unconsidered secondary references present substantial new questions of patentability.

Third, the challenged claims are invalid for obviousness-type double patenting as a result of a related patent prosecuted after the ’571 patent issued. Specifically, the challenged claims of the ’571 patent are obvious variants of the claims of US Patent No. 7,911,851 (“the ’851 patent”) (Ex. H). Because the ’851 patent expired before the ’571 patent and the patentee did not disclaim the term of the ’571 patent that extended beyond expiration of the ’851 patent, the ’571 patent is invalid. The ’851 patent was filed after issuance of the ’571 patent and was never considered, and could not have been considered, by the USPTO during prosecution of the ’571 patent. Nor was it raised or considered in any IPR proceeding because obviousness-type double patenting is not a permissible ground for challenging claims in IPR. Accordingly, obviousness-type double patenting in view of the ’851 patent is a substantial new question of patentability that justifies reexamination.

A. New Prior Art References Teach the Features that were the Basis for Allowance of the ’571 Patent

During the prosecution of the application from which the ’571 patent issued, the Applicant attempted to distinguish over Examiner-cited prior art by arguing that the Examiner-cited prior art was (i) not electrically alterable, non-volatile memory, (ii) did not disclose the selection of a reference voltage, and (iii) did not disclose comparing the selected reference voltage with the cell voltage and generating a control signal indicating that the cell is correctly programmed. *See* Ex. B at 164-166. The Applicant further indicated that these alleged deficiencies in the prior art were reasons for allowance. *See* Ex. B at 166.

However, as described in more detail in Sections VII to IX, several prior art references clearly disclose the allegedly novel and non-obvious features. Each reason for allowance noted by the Applicant is rendered obvious based on noted combinations of the Kitamura, VLSI Design, Connolly, and Oshita references.

For example, Japanese Patent Application Kokai No. S62-34398 (A) (“Kitamura”) (Ex. D) describes the same type of electrically alterable, non-volatile memory as the ’571 patent. Ex. D at ¶¶ [02], [06], [14]. The Kitamura application’s title is “Non-volatile memory,” and the

device described therein uses MLC memory cells allowing a "plurality of bits of digital data to be written to the memory cell transistor of a single element." Ex. D at ¶ [14].

Kitamura's process of writing data also compares a reference voltage to a memory cell voltage to indicate if a memory cell is correctly programmed. Kitamura describes obtaining a reference voltage using "a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal." *Id.* at ¶ [06]. The resulting analog signal serves as a reference voltage representing the information in "input digital signals B_0 and B_1 to be written" in the memory cell. *Id.* at ¶ [09]. Kitamura determines whether the memory cell has been correctly programmed with a "circuit that compares a read level from a memory cell to the level of the analog signal." *Id.* at ¶¶ [06], [09]. Specifically, a "comparator 9" compares the analog signal from the D/A conversion circuit 10 with the "output voltage (V_O) of the read point 8" for the memory cell. *Id.* The comparator 9 then triggers the programming process to stop once the correct memory state is reached:

> . . . when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3. Meanwhile, the two-bit input digital signals B0 and B1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the [programming] operation is continued with write/read signals while lower than these analog signals, but **when the comparator 9 determines that V_O [read from the memory cell] is higher than the analog signals** from the D/A conversion circuit 10 [, which represent the information to be stored], **the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation**. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals . . . .

Id. at ¶ [09] (emphasis added). Thus, the output of Kitamura's comparator 9 when "V_0 is higher than the analog signals from the D/A conversion circuit 10" serves as a control signal that "ends the write operation" when the correct state of the memory is reached, e.g., when the memory cell reaches the state that "corresponds to the input digital signals" to be written. *Id.* at ¶ [09].

In addition, the VLSI Design, Connolly, and Oshita references each separately disclose selection of a reference signal from a predetermined set of reference voltages. VLSI Design, Connolly, and Oshita each disclose digital-to-analog conversion techniques that involve selecting a voltage from a predetermined set of voltages. Ex. C at ¶¶ 86-91, 109-111, 126-131. Because Kitamura's design includes a "D/A conversion circuit 10," it, would have been obvious to use well-known digital-to-analog conversion techniques, such as those taught by VLSI Design,

Connolly, and Oshita, to implement Kitamura's "D/A conversion circuit 10." *Id.* at ¶¶ 80-83, 90, 117-120, 130-131.

Regarding selecting a reference signal, VLSI Design describes voltage-scaling digital-to-analog converters that use "series resistors connected between Vref and ground to **selectively obtain voltages between these limits**." Ex. E at 626 (emphasis added). Taps between the series resistors have predetermined voltage levels, and "[e]ach tap is connected to a switching tree whose switches are controlled by the bits of the digital word" to be converted by the circuit. *Id.* at 627. Thus, the circuit selects one of the analog voltages at the taps to output based on the digital input to the circuit. *Id.* at 627-629; Ex. C at ¶¶ 83, 86-90.

Connolly also describes selecting a reference voltage from a predetermined set of reference voltages. Connolly describes circuits in which each digital-to-analog converter "includes a resistor ladder and switching tree that permits coupling the output to any single tap on the ladder." Ex. F at Abstract. The act of "coupling the output to any single tap" based on digital input shows that the switching tree selects a voltage (e.g., the voltage at the selected "single tap") from among the set of reference voltages available at the different taps of the resistor ladder. *Id.*; Ex. C at ¶¶ 108-112.

Oshita also describes selecting a reference voltage from a predetermined set of reference voltages. Oshita states that a "digital-to-analog converter of the resistor string type comprises a string of resistors for dividing a reference voltage into a series of divided voltages, and **a switch matrix circuit for selectively generating the divided voltages as an analog signal** when activated in response to a digital signal." Ex. G at Abstract (emphasis added). The "switch matrix circuit" includes a "selection means" or "selector" that responds to a digital signal by "selecting one of the respective [] divided voltages" at the input of the selector "to generate the selected one divided voltage as the analog signal" for output by the circuit. *Id.*; *see also id.* at 3:1-5, claim 1. Oshita uses a multiplexer 7 as the selector, and multiplexers are well-known to perform the function of selecting an output from among various inputs. *Id.* at 5:19-54, Fig. 1; Ex. C at ¶ 127. The multiplexer 7 receives four signals from different sections of the resistor string (e.g., arrays A, B, C, and D), and the multiplexer 7 selects one voltage to output on an external line 9:

> the multiplexer 7 cooperates with the decoder 8 responsive to signals appearing on the input lines B_0, B_1 to permit electrical connection between the external line 9 and the output line 5 of line decoder 4 for one of the square arrays A, B, C and

> D. **This means that the multiplexer 7 cooperates with decoder 8 to select one of the square arrays A to D on a basis of the signals appearing on the input lines B_0, B_1.**

Ex. G at 5:46-54 (emphasis added).

Therefore, combinations of Kitamura, VLSI Design, Connolly, and Oshita, which were not considered by the Examiner during original prosecution, raise substantial new questions of patentability with respect to the claims of the '571 patent, because the combinations of these references render obvious all of the claim features which appear to have been responsible for allowance.

B. New Prior Art References Teach the Features Cited as the Basis for Not Instituting *Inter Partes* Review of the '571 Patent

The '571 patent was subject to two petitions for *inter partes* review (IPR) that were substantively identical. The PTAB declined to institute trial on the basis that the references in the asserted IPR grounds allegedly did not teach or suggest a "reference voltage selecting means" to select from "reference voltages." Ex. J (Denying Institution of *Inter Partes* Review) at 9-10.'

The PTAB's denial of institution of IPR was based on a finding that is contradicted by evidence that was not submitted by the patent owner and was not considered by the PTAB, but has now been discovered by the requester and is described and submitted in Appendix A, which is subject to a protective order. Appendix A is being submitted concurrently with this request and under seal pursuant to MPEP § 724.02. This new evidence soundly refutes arguments made by the Patent Owner in the IPR and reasons that the PTAB gave for not instituting IPR in view of the Kitamura reference.

Moreover, the VLSI Design, Connolly, and Oshita references—which were not part of the asserted IPR grounds—describe the exact features that were allegedly not taught in the IPR grounds. As noted above, VLSI Design and Connolly each separately disclose resistor networks to generate reference voltages, and switching trees to select from among the voltages. Ex. E (VLSI Design) at 626-629; Ex. F (Connolly) at Abstract. Further, Oshita describes a "selection means" including a multiplexer 7, which has the purpose of selecting from among the "divided voltages" from a resistor string. Ex. G (Oshita) at Abstract, 3:1-5, 5:19-54.

Thus, VLSI Design, Connolly, and Oshita, in combination with Kitamura as discussed below, raise substantial new questions of patentability with respect to the claims of the '571

patent, because VLSI Design, Connolly, and Oshita each teaches the "reference voltage selecting means" feature that was the basis for not instituting IPR of the '571 patent.

C. New Reference U.S. Patent No. 7,911,851 Shows that the Claims of the '571 Patent Are Invalid for Obviousness-type Double Patenting

The original prosecution of the '571 patent did not consider U.S. Patent No. 7,911,851 ("the '851 patent"), which renders the claims of the '571 patent invalid for obviousness-type double patenting. The '851 patent has the same inventor as the '571 patent, claims the same or patentably indistinct technology as the '571 patent, and expired before the '571 patent. Because the term of the '571 patent unlawfully extends beyond the full statutory term of the '851 patent for the same or patentably indistinct technology, the '571 patent is invalid for obviousness-type double patenting.

The '571 patent improperly prevents the public from using the technology claimed in the earlier-expiring '851 patent—technology that should have been freely available to the public after the '851 patent expired. This is precisely the scenario that the doctrine of obviousness-type double patenting is intended to prevent:

> The doctrine of double patenting seeks to prevent the unjustified extension of patent exclusivity beyond the term of a patent. The public policy behind this doctrine is that:
>
> > **The public should . . . be able to act on the assumption that upon the expiration of the patent it will be free to use not only the invention claimed in the patent but also modifications or variants** which would have been obvious to those of ordinary skill in the art at the time the invention was made, taking into account the skill in the art and prior art other than the invention claimed in the issued patent.
>
> *In re Zickendraht,* 319 F.2d 225, 232, 138 USPQ 22, 27 (CCPA 1963) (Rich, J., concurring). Double patenting results when the right to exclude granted by a first patent is unjustly extended by the grant of a later issued patent or patents. *In re Van Ornum,* 686 F.2d 937, 214 USPQ 761 (CCPA 1982). **Note that in *Gilead Sciences, Inc. v. Natco Pharma Ltd.,* 753 F.3d 1208, 110 USPQ2d 1551 (Fed. Cir. 2014), the court found an earlier-expiring patent, which was issued after the later-expiring patent, may be used to invalidate the later-expiring patent.**

MPEP § 804 (emphasis added).

As discussed in detail below, the claims of the '851 patent teach or render obvious each of the features of claims 1, 9, 12, 30, 42, and 45 of the '571 patent. Therefore, the expiration of

the ’851 patent before the ’571 patent, and the patent owner’s failure to disclaim the improper term of the ’571 patent, renders these claims of the ’571 patent invalid under obviousness-type double patenting, as an unlawful extension of patent rights.

D. New Evidence in Appendix A Supports Re-Examination

Appendix A has been filed under seal pursuant to MPEP § 724.02. The documents in this appendix provide additional reasons that support re-examination. The documents contain information subject to protective order that was not previously considered by the USPTO.

The references discussed in this request combine as reflected in the following table to render claims of the ’571 patent obvious and invalid for obviousness-type double patenting. Each basis for rejection includes at least one reference that was not considered by the Examiner and was not included any previously-asserted IPR grounds.

Claims	Basis for Rejection
1, 9, 12, 30, 42, and 45	Obviousness in view of Kitamura in view of VLSI Design
1, 9, 12, 30, 42, and 45	Obviousness in view of Kitamura in view of Connolly
1, 9, 12, 30, 42, and 45	Obviousness in view of Kitamura in view of Oshita
1, 9, 12, 30, 42, and 45	Obviousness-type double patenting in view of claims 3, 7, and 14 of the ’851 patent

II. CLAIMS FOR WHICH REEXAMINATION IS REQUESTED

Reexamination is requested for each of claims 1, 9, 12, 30, 42, and 45 of the ’571 patent.

As explained in greater detail below, prior art that was not considered by the USPTO during prosecution of the ’571 patent renders obvious all features of claims 1, 9, 12, 30, 42, and 45 of the ’571 patent.

Claims 1, 9, 12, 30, 42, and 45 are also invalid for non-statutory obviousness-type double patenting in view of U.S. Patent No. 7,911,851 (Ex. H), which was not considered by the USPTO during prosecution of the ’571 patent.

Consequently, reexamination is hereby requested for claims 1, 9, 12, 30, 42, and 45 of the ’571 patent in view of the patents and publications discussed below. A copy of the ’571 patent is attached as Ex. A of this document.

III. IDENTIFICATION OF PATENTS AND PRINTED PUBLICATIONS PRESENTED TO SHOW SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

1. Certified Translation of Japanese Patent Application Kokai No. S62-34398 (A) (“Kitamura”) (Ex. D); the Japanese-language version of Kitamura is attached as Ex. I;

2. Excerpts from “VLSI Design Techniques for Analog and Digital Circuits,” by Geiger, Allen, and Strader, McGraw-Hill, 1989 (“VLSI Design”) (Ex. E)

3. U.S. Patent No. 4,198,622 to Connolly (“Connolly”) (Ex. F)

4. U.S. Patent No. 5,014,054 to Oshita (“Oshita”) (Ex. G)

5. U.S. Patent No. 7,911,851 to Banks (“the ’851 patent”) (Ex. H)

The references at Exhibits D-H were not named on the face of the ’571 patent and were not documented as being considered by the Examiner during ex parte prosecution of the ’571 patent.

Prior IPR proceedings considered an invalidity ground of obviousness in view of Kitamura alone. Ex. J (IPR Institution Decision) at 7-10. VLSI Design was included as an exhibit in the IPR petition, and was discussed in a declaration by Dr. R. Jacob Baker in support of the IPR petition. However, the PTAB specifically noted that VLSI Design and other textbooks cited in the declaration were not part of the asserted invalidity grounds:

> Dr. Baker goes on to further interpret Kitamura . . . , citing additional references [including VLSI Design], **but those additional references do not form part of the obviousness ground, and are not cited in the Petition**.”

Ex. K (IPR Rehearing Decision) at 6. Moreover, Appendix A provides important evidence that contradicts the patent owner's arguments to the PTAB in IPR regarding the teachings of Kitamura and certain elements of the challenged patent claims, and contradicts the PTAB's findings about Kitamura in response to those arguments. This evidence was not submitted by the patent owner and therefore has not yet been considered by the USPTO. Thus, the combination of Kitamura and VLSI design represents a substantial new question of patentability that was not considered in the IPR proceedings.

IV. CO-PENDING PROSECUTION AND LITIGATION

Requester is aware of the following civil actions involving the '571 patent: *MLC Intellectual Property, LLC v. Micron Technology, Inc*., No. 3:14-cv-03657 (N.D. Cal. August 12, 2014); *BTG International Inc. v. Apple Inc. et al*, No. 2:09-cv-00223 (E.D. Tex. July 20, 2009); *BTG International Inc. v. Samsung Electronics Co. LTD et al*, No. 2:08-cv-00482 (E.D. Tex. December 29, 2008); and *MLC Flash Memory Devices and Products Containing Same*, Inv. No. 337-TA-683, (January 19, 2011) (Completed).

As noted above, the '571 patent was the subject of two petitions for IPR, IPR2015-00504, filed December 24, 2014, and IPR2015-00517, filed on December 30, 2014. The PTAB did not institute trial for either of the IPR petitions.

Requester is not aware of any previous disclaimers or reexamination certificates for the '571 patent. Requester is not aware of any pending prosecution concerning the '571 patent.

V. THE ORIGINAL PROSECUTION HISTORY

U.S. Patent No. 5,764,571 was filed on February 27, 1995, as U.S. Patent Appl. Ser. No. 08/410,200 ("the '200 application"), and issued on June 9, 1998. *See* Ex. A. The '571 patent claims to be a divisional of U.S. Patent No. 5,394,362 filed on June 4, 1993, which, in turn, claims to be continuation of U.S. Patent No. 5,218,569 filed on February 8, 1991. *See id*.

The USPTO issued an office action on December 17, 1996, rejecting or objecting to all of the original twenty-three claims of the '200 application over Suzuki (U.S. Patent No. 4,809,224) as being "drawn to a basic multi-level memory with comparator as shown by Suzuki et al." *See* Ex. B (Prosecution History) at 107-08.

In response, the Applicant amended certain claims to add limitations directed to selecting a reference voltage for use in comparing to a signal representing the current state of the memory cell. *See* Ex. B at pages 144-167. The Applicant then argued that it "is apparent that Suzuki neither teaches nor suggests a multi-level memory device having the aforementioned features of Claim 1. Note, for example, that Suzuki discloses a conventional ROM which is not electrically alterable . . . . Further, Suzuki lacks any suggestion whatsoever of the reference voltage selecting means and comparator means, both as now defined." Ex. B at 165.

The USPTO subsequently allowed all pending claims in a Notice of Allowance, which did not include any reasons for allowance or an examiner's amendment. *See* Ex. B at 169. Thus, the above-described amendments to the independent claims appear to have led directly to and been the basis for the Examiner's allowance. As described above, and as shown in more detail in the claim charts below, the Kitamura, VLSI Design, Connolly, and Oshita references render obvious the claim elements that the patent owner relied upon to distinguish the claims in the '571 patent over the prior art.

VI. PRIOR IPR PETITIONS

A petition for *inter partes* review (IPR) of the '571 patent was filed on December 24, 2014. A second petition for IPR, which was essentially a copy of the first petition, was filed on December 30, 2017. These petitions asserted invalidity on two separate grounds: (1) obviousness over Kitamura alone, and (2) obviousness over U.S. Patent No. 5,172,338 ("Mehrotra") alone.

In a Patent Owner Preliminary Response (POPR), the patent owner argued that the prior art failed to describe "reference voltage selection means." Ex. L at 4-15. The patent owner further argued that the petition did not demonstrate that Kitamura's "digital-to-analog conversion circuit makes a selection of any type, let alone a selection of a plurality of reference voltages." *Id.* at 6. The patent owner also alleged that there was "no evidence or reason to believe that the conversion of digital input signals to an analog signal involves a 'selection' of 'one of a plurality of reference voltages.'" *Id.* at 7.

In a Decision dated July 20, 2015, the PTAB declined to institute IPR of the '571 patent. Ex. J at 10-11. The PTAB stated that "[w]e are not persuaded that Kitamura teaches or suggests the selection of one of a plurality of reference voltages in accordance with the input information,

per the challenged claims." Ex. J at 10. In a Decision denying a request for rehearing, the PTAB further noted that additional references relied upon to further interpret Kitamura "do not form part of the obviousness ground, and are not cited in the Petition." Ex. K at 4-5. In denying rehearing, the PTAB offered the following clarification:

> The cited comment in the Decision ("[i]n addition, the Petitions fail to provide any rationale for why Kitamura's disclosure of D/A conversion renders the selection of a reference voltage or signal obvious," Dec. 10; Reh'g Req. 15) was made to note that Petitioner was relying on the same or equivalent structures in both, and was not relying on the obviousness of one over the other. *One example of this would have been if Petitioner had cited a structure in Kitamura, acknowledged that it was not the same, but argued that the equivalent structure disclosed in the '571 Patent would have been obvious in view of the structure in Kitamura; i.e., pointing out that one would have been an obvious variation of the other. Petitioner had not done this, as we merely noted.*

Ex. K at 8 (emphasis added). In other words, the PTAB declined to find that the D/A conversion circuit of Kitamura "must" perform a selection or must contain the same selection circuit as claimed in the '571 patent, but declined to address whether the D/A conversion circuit of Kitamura rendered obvious the selection function and circuit of the '571 patent, finding that this issue was not properly raised by the petition.

As shown in this request, the newly-presented prior art addresses the limitations alleged to be lacking in references previously presented, including the alleged deficiency of the petitions for IPR. While acknowledging that Kitamura does not specifically describe the details of the internal operation of Kitamura's D/A conversion circuit 10, this request demonstrates that Kitamura's teaching to use a D/A conversion circuit, in combination with references that describe in greater detail conventional digital-to-analog conversion techniques and circuits that include selecting one of a plurality of reference voltages, renders obvious the claims of the '571 patent. VLSI Design, Connolly, and Oshita each describe the feature of a "reference voltage selection means." In particular, each of these references describes digital-to-analog conversion techniques that unambiguously involve selecting one of a plurality of reference voltages, the very feature that was found to be lacking in the references used in the grounds of the prior IPR petitions. *See* Ex. E at 626-628 (DAC circuit "to selectively obtain voltages" from taps representing different voltages); Ex. F at Abstract (DAC including "a resistor ladder and switching tree that permits coupling the output to any single tap on the ladder"); Ex. G at claim 1

(DAC including "selection means responsive to the digital signal for selecting one of the respective divided voltages . . . as the analog [output] signal"); Ex. C at ¶¶ 86-91, 109-111, 126-131.

And as set forth in Appendix A, inventor Gerald Banks' prior testimony and engineering notebook further support institution of this ex parte reexamination request and show that the references present a substantial new question of patentability. Mr. Banks' testimony and notebook were not submitted to the PTAB by the patent owner during IPR and only recently became available to Requester through discovery in co-pending litigation. This evidence therefore has not previously been considered by the Patent Office.

Finally, as an additional difference from the Petitions for IPR, this request raises the issue of obviousness-type double patenting over the '851 patent as a substantial new question of patentability. Obviousness-type double patenting was not raised in the petitions for IPR, nor could the issue have been raised there because, in IPR, claims may be challenged "only on a ground that could be raised *under section 102 or 103*. . . ." 35 U.S.C. § 311 (emphasis added). Thus, the issue of obviousness-type double-patenting in view of the '851 patent, which was not considered by the examiner during prosecution of the '571 patent, is a substantial new question of patentability that justifies reexamination.

VII. THE REFERENCES RELIED UPON HEREIN PROVIDE NEW, NON-CUMULATIVE TECHNICAL TEACHINGS

VLSI Design (Ex. E), Connolly (Ex. F), and Oshita (Ex. G) provide new technical teachings and present substantial new questions of patentability. Specifically, each reference teaches features that the patent owner relied on to distinguish prior art and which the PTAB relied on to decline institution of prior-filed petitions for IPR.

A. VLSI Design Provides New, Non-Cumulative Technical Teachings

VLSI Design qualifies as prior art under 35 U.S.C. § 102(b) because it was published and publicly available on or before December 8, 1989, which is more than one year before the earliest possible effective filing date of the '571 patent (i.e., February 8, 1991). VLSI Design describes techniques and circuits for digital-to-analog conversion, including voltage-scaling D/A

converter circuits. Ex. E at 615, 626-629. The voltage-scaling circuits use "series resistors connected between Vref and ground to selectively obtain voltages between these limits." *Id.* at 626. Taps between resistors are "connected to a switching tree whose switches are controlled by the bits of the digital word," and the switching tree selects one of the taps to provide an output voltage. *Id.* at 627.

VLSI Design was not before the Examiner during prosecution of the '571 patent. VLSI Design was included as an exhibit in the prior IPR petitions, but was not part of the asserted invalidity grounds in the IPR petitions. VLSI Design presents new, non-cumulative teachings that were not previously considered by the Patent Office and therefore presents a substantial new question of patentability with respect to the claims of the '571 patent. Specifically, VLSI Design clearly describes features of the independent claims that led to allowance of the application and the decision not to institute IPR. For example, VLSI Design teaches the feature of a "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with . . . input information" as recited in claim 1 the '571 patent as well as similar "selecting" features of claims 9, 12, 30, 42, and 45, which the patent owner relied upon to distinguish the prior art in original prosecution and during the IPR proceedings. *See* Ex. C at ¶¶ 86-91; Ex. L at 4-10.

B. Connolly Provides New, Non-Cumulative Technical Teachings

United States Patent No. 4,198,622 to Connolly qualifies as prior art under 35 U.S.C. § 102(b) because it issued on April 15, 1980, which is more than one year before the earliest possible effective filing date of the '571 patent (i.e., February 8, 1991). The Connolly reference describes digital-to-analog conversion circuits and techniques in which a "converter includes a resistor ladder and switching tree that permits coupling the output to any single tap on the ladder." Ex. F at Abstract. A different, predetermined voltage is present at each tap on the resistor ladder. Ex. 2:49-57, 3:57-4:23; Ex. C at ¶¶ 109-111. By "coupling the output to any single tap," the switching tree performs a selection of a voltage—that is, the switching tree selects a voltage to output from among the predetermined set of voltages present at the taps of the resistance ladder. *Id.*

Connolly was not before the Examiner during prosecution of the '571 patent and was not considered by the PTAB in the prior IPR proceedings. Connolly thus presents new, non-

cumulative teachings that were not previously considered by the Patent Office and therefore presents a substantial new question of patentability with respect to claims of the ’571 patent. Specifically, Connolly clearly describes features of the independent claims that led to allowance of the application and the decision not to institute IPR. For example, Connolly teaches the feature of a “reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with . . . input information” as recited in claim 1 the ’571 patent as well as similar “selecting” features of claims 9, 12, 30, 42, and 45, which the patent owner relied upon to distinguish the prior art in original prosecution and IPR proceedings. *See* Ex. C at ¶¶ 126-131; Ex. L at 4-10.

C. Oshita Provides New, Non-Cumulative Technical Teachings

United States Patent No. 5,014,054 to Oshita qualifies as prior art under 35 U.S.C. § 102(e) because it was filed on July 22, 1988, which is before the earliest possible effective filing date of the ’571 patent (i.e., February 8, 1991). The Oshita reference describes a “digital-to-analog converter of the resistor string type” that includes “a string of resistors for dividing a reference voltage into a series of divided voltages, and a switch matrix circuit for selectively generating the divided voltages as an analog signal when activated in response to a digital signal.” Ex. G at Abstract (emphasis added). The “switch matrix circuit” includes a “selection means” that responds to a digital signal by “selecting one of the respective [] divided voltages” at the input of the selector “to generate the selected one divided voltage as the analog signal” for output by the circuit. *Id.* at 3:1-5, claim 1.

Oshita was not before the Examiner during prosecution of the ’571 patent and was not considered by the PTAB in the prior IPR proceedings. Oshita thus presents new, non-cumulative teachings that were not previously considered and therefore presents a substantial new question of patentability with respect to claims of the ’571 patent. Specifically, Oshita clearly describes features of the independent claims that led to allowance of the application and the decision not to institute IPR. For example, Oshita teaches the feature of a “reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with . . . input information” as recited in claim 1 the ’571 patent as well as similar “selecting” features of claims 9, 12, 30, 42, and 45, which the patent owner relied upon to distinguish the prior art in original prosecution and IPR proceedings. *See* Ex. C at ¶¶ 126-131; Ex. L at 4-10.

VIII. ADDITIONAL PRIOR ART AND NEWLY SUBMITTED EVIDENCE

Requester submits that substantial new questions of patentability are raised by the combination of (i) Kitamura (which was discussed in prior IPR proceedings but not original prosecution of the '571 patent) with (ii) the new references in Exhibits E-G (which were not before the examiner during prosecution and were not part of the invalidity grounds of the prior IPR proceedings). Requester further notes that inventor testimony and the inventor's notebook, which contradict the patent owner's arguments to the PTAB regarding Kitamura and elements of the challenged claims, was not disclosed by the patent owner and has never been considered by the USPTO. Kitamura, in combination with the new references and in view of this newly submitted evidence, presents a substantial new question of patentability. In addition, according to MPEP 2242(II)(A), "reliance on old art does not necessarily preclude the existence of a substantial new question of patentability."

Kitamura qualifies as prior art under 35 U.S.C. § 102(b) because it published on February 14, 1987, which is more than one year before the earliest priority date of the '571 patent (February 8, 1991). Kitamura describes a storage device with non-volatile memory cells allowing a "plurality of bits of digital data to be written to the memory cell transistor of a single element." Ex. D at ¶ [14]. Kitamura determines whether a memory cell has been correctly programmed with a "circuit that compares a read level from a memory cell to the level of the analog signal" representing the desired memory state. *Id.* at ¶¶ [06], [09]. Specifically, a "comparator 9" compares the analog signal from a D/A conversion circuit 10 with the "output voltage (V_O) of the read point 8" for the memory cell, and the comparator 9. *Id.*

Kitamura was not before the Examiner during prosecution of the '571 patent. The prior IPR proceedings asserted invalidity of the '571 patent on the basis of obviousness over Kitamura alone.

Kitamura clearly describes various features of the independent claims that led to the allowance of the application. For example, Kitamura teaches features of 1, 9, 12, 30, 42, and 45 including an electrically alterable, non-volatile memory having more than two memory states, as well as comparing a selected reference voltage with a memory cell voltage and generating a control signal indicating that the cell is correctly programmed, which the patent owner relied upon to distinguish the prior art during original prosecution. *See* Ex. B at 164-166.

Although the prior IPR petitions asserted a ground based on obviousness over Kitamura alone, they did not include grounds based on combinations of Kitamura with any other reference. *See* Ex. J (IPR Institution Decision) at 7-10. When combined with other references that were not before the examiner and were not before the PTAB, the teachings of Kitamura in combination with these references present a substantial new question of patentability with respect to claims 1, 9, 12, 30, 42, and 45 of the '571 patent.

Additionally, Kitamura provides a substantial new question of patentability when understood in light of the new evidence in Appendix A. While Appendix A does not recite new prior art references, the new evidence contained within nevertheless compels a different and more expansive interpretation of the '571 patent and the similarity with the Kitamura reference. In particular, Appendix A directly contradicts statements by the Patent Owner and reasons that the PTAB gave for denying institution of IPR in view of Kitamura. The new evidence in Appendix A shows that the PTAB's interpretations of the '571 patent and the Kitamura reference were incorrect and incomplete, and the Challenged Claim are invalid over Kitamura and other references as discussed below.

IX. SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY NOT RAISED DURING PROSECUTION OF THE '571 PATENT

Four substantial new questions of patentability (SNQs) are described in detail below: three based on obviousness under 35 U.S.C. § 103 and one based on obviousness-type double patenting. Each SNQ demonstrates that each of claims 1, 9, 12, 30, 42, and 45 is invalid and should not have been allowed by the USPTO.

With respect to SNQ's 1-3, a person of ordinary skill in the art (POSITA) would have had numerous reasons to combine Kitamura with VLSI Design, Connolly, or Oshita. As discussed further below, Kitamura's memory system uses a D/A conversion circuit 10. *See* Ex. D at ¶¶ [07]-[09]. However, since digital-to-analog converters were well-known, ubiquitous, devices, Kitamura does not fully describe the internal structure and operation of this element. *See id.* at ¶¶ [09]-[11]; Ex. C at ¶ 82. As a result, a POSITA implementing Kitamura's design would have been motivated to implement the D/A conversion circuit 10 using well-known techniques for digital-to-analog conversion as taught in other documents. Ex. C at ¶ 82. VLSI Design, Connolly, and Oshita each independently disclose digital-to-analog conversion

techniques that a POSITA would have found obvious to use to implement Kitamura's D/A conversion circuit 10. *Id.* at ¶¶ 83-85, 117-122, 130-132. The reason for the combination is simple: Kitamura's circuit requires a DAC (e.g., D/A conversion circuit 10) and VLSI Design, Connolly, and Oshita each teach a DAC that can perform the D/A conversion function needed in Kitamura's circuit. *Id.*

First, combining any of VLSI Design, Connolly, and Oshita with Kitamura would have been obvious as a combination of prior art elements according to known methods to yield predictable results. *See* MPEP 2143(I)(A); *KSR Intl. Co. v. Teleflex Inc*, 550 U.S. 398, 417 ("when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious") (quotation omitted); *id.* at 416 ("The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results."). As discussed below and shown in the claim charts, Kitamura discloses all elements of the Challenged Claims except the "reference voltage selecting means" or "selecting device," but VLSI Design, Connolly, and Oshita each supply this final element in the form of a DAC. Ex. C at ¶¶ 68-86, 106-107, 124-125. A POSITA would have used the DAC techniques of VLSI Design, Connolly, or Oshita in Kitamura's D/A conversion circuit 10, with the D/A conversion circuit 10 performing the same function that VLSI Design, Connolly, and Oshita disclose. Ex. C at ¶¶ 90-91, 117-122, 130-132. The DAC from VLSI Design, Connolly, or Oshita would have produced the same predictable results that a DAC is known to produce: output of an analog voltage selected from a predetermined set of voltages in accordance with the digital input to the DAC. *Id.* at ¶¶ 76, 83, 118-119, 130.

Second, combining any of VLSI Design, Connolly, and Oshita with Kitamura would have been obvious as a simple substitution of one known element for another to obtain predictable results. *See* MPEP 2143(I)(B); *KSR*, 550 U.S. at 417 (discussing obviousness of "the simple substitution of one known element for another" and the importance of asking "whether the improvement is more than the predictable use of prior art elements according to their established functions"). VLSI Design, Connolly, and Oshita each describe a DAC that is equivalent to the "reference voltage selecting means" or "selecting device" of the Challenged Claims—each DAC selects one of a predetermined plurality of analog signals to output. Ex. C at ¶¶ 86-91, 109-111, 126-131. When substituted for Kitamura's D/A conversion circuity, the

DAC of any of VLSI Design, Connolly, and Oshita would perform in exactly the same manner, producing the same predictable result of outputting the selected voltage corresponding to the digital input to the DAC. *Id.* at ¶¶ 76, 83, 118-119, 130. The operation of Kitamura's overall circuit would not be changed due to the substitution, since this is the same function as Kitamura's D/A conversion circuit 10 performs. *Id.* at ¶¶ 86-91, 109-111, 126-131.

Third, combining any of VLSI Design, Connolly, and Oshita with Kitamura would have been obvious as a use of a known technique to improve a similar device in the same way. *See* MPEP 2143(I)(C); *KSR*, 550 U.S. at 417 ("if a technique has been used to improve one device, and a POSITA in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill."). A POSITA would have recognized that VLSI Design, Connolly, and Oshita each teach DAC techniques that can improve Kitamura's D/A conversion circuit 10 in the same way those techniques improve other DACs. For example, a POSITA would have recognized that the techniques of VLSI Design, Connolly, and Oshita improve Kitamura's D/A conversion circuit 10 through simple circuit techniques that are easy to manufacture; use simple, well-known circuit elements; and provide versatility to meet many different circuit configurations. Ex. C at ¶¶ 84, 118-119, 130.

Fourth, combining any of VLSI Design, Connolly, and Oshita with Kitamura would have been obvious as an application of a known technique to a known device ready for improvement to yield predictable results. *See* MPEP 2143(I)(D); *KSR*, 550 U.S. at 417 (discussing obviousness of "application of a known technique to a piece of prior art ready for the improvement"). In particular, Kitamura's device presents a circuit that is ready for application of the DAC techniques of VLSI Design, Connolly, and Oshita. Ex. C at ¶¶ 68-86, 106-107, 124-125. A POSITA would have recognized that these DAC techniques would have improved Kitamura by providing a reliable and effective design that would perform the functions that the D/A conversion circuit 10 is designed to perform. Ex. C at ¶¶ 76, 83, 118-119, 130.

Fifth, design incentives and market forces would also have prompted a POSITA to combine any of VLSI Design, Connolly, and Oshita with Kitamura, since their techniques represent a variation that is predictable to one of ordinary skill in the art. *See* MPEP 2143(I)(F); *KSR*, 550 U.S. at 417 ("When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a

POSITA can implement a predictable variation, § 103 likely bars its patentability.") A POSITA implementing Kitamura's circuit would have had an incentive to minimize cost and manufacturing complexity. As a result, a POSITA would have been motivated to use the DAC techniques of VLSI Design, Connolly, and Oshita to implement the D/A conversion circuit 10 of Kitamura, because these DAC techniques use very simple parts and a small number of parts. Ex. C at ¶¶ 84, 117-119, 130. This would have been desirable to facilitate manufacturing and minimize IC chip area, and thus minimize cost, while still providing the D/A conversion needed in Kitamura's circuit. *Id.*

The circuits taught by VLSI Design, Connolly, and Oshita are each consistent with the structure and function that Kitamura describes for the D/A conversion circuit 10. Kitamura mentions that the D/A conversion circuit 10 has "a voltage dividing element and a reference voltage supply." Ex. D at ¶ [11]. VLSI Design, Connolly, and Oshita each have a corresponding resistor string that serves as a "voltage dividing element" connected to a "reference voltage supply," demonstrating that each of these DAC designs generates voltages in the same way Kitamura contemplates. *See* Ex. E at 627 ("resistor string"); Ex. F at Abstract ("resistor ladder"); Ex. G at Abstract ("string of resistors for dividing a reference voltage").

In addition to the reasons for combination discussed above, a POSITA would have been motivated to combine the references as discussed in SNQs 1-3 because of the specific teachings and advantages disclosed in VLSI Design, Connolly, and Oshita. *See* MPEP 2143(I)(G). These additional reasons are discussed in more detail in the respective sections below.

The new evidence in Appendix A is relevant to each of SNQs 1-3 and further demonstrates that each combination of references presents a substantial new issue of patentability not previously before the USPTO.

A. Overview of the '571 Patent Claims, Key Claim Constructions

Claims 1, 9, 12, and 30 of the '571 patent vary slightly, but all essentially claim a device with four main components and functions: (1) an electrically alterable, non-volatile memory, (2) reference voltage selecting, (3) memory cell programming, and (4) comparing. Method claims 42 and 45 mirror these claim requirements, albeit using modified language. Claim 1 is exemplary:

1. A multi-level memory device comprising:

> an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;
>
> memory cell programming means for programming said multi-level memory cell in accordance with said input information;
>
> reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and
>
> comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.

When compared to claims 9, 12, and 30, it is clear that claim 1 contains similar requirements, but claim 1 is written in means-plus-function form while claims 9, 12, and 30 are not. Claim 9 is exemplary:

> 9. Multi-level memory apparatus, comprising:
>
> an electrically alterable non-volatile memory cell having more than two predetermined memory states;
>
> a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;
>
> a programming signal source which applies a programming signal to said memory cell; and
>
> a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.

Means-plus-function claiming is controlled by 35 U.S.C. § 112 ¶ 6, which provides that "[a]n element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the

specification and equivalents thereof." 35 U.S.C. § 112 ¶ 6. "If a claim limitation recites a term and associated functional language, the examiner should determine whether the claim limitation invokes 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph." MPEP 2181(I). "The claim limitation is presumed to invoke 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph when it explicitly uses the term 'means' or 'step' and includes functional language." *Id.* When using the means-plus-function format, "[t]he applicant must describe in the patent specification some structure which performs the specified function." *Valmont Industries, Inc. v. Reinke Manufacturing Co., Inc*., 983 F.2d 1039, 1042 (Fed. Cir. 1993). "The first step in construing such a limitation is a determination of the function of the means-plus-function limitation. The next step is to determine the corresponding structure described in the specification and equivalents thereof." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001) (internal citations omitted). As is described in more detail below, the '571 patent's use of mean-plus-function language in claim 1 invokes specific corresponding structure that is obvious in view of the references relied upon herein.

Moreover, three groups of terms within these four main required components and functions require additional attention.

1. The "reference voltage selecting" terms. The "reference voltage selecting" term takes on three forms across claims 1, 9, 12, 30, 42, and 45: (1) "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information" in claim 1; (2) "a selecting device which selects one of a plurality of [predetermined] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" in claims 9, 12, and 30[1]; and (3) "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" in claims 42 and 45. While each of these three "reference voltage selecting" terms require the substantially similar analysis, each will be addressed in turn to address their slight differences.

[1] This phrase appears in identical form in claim 9, 12, and 30, except claim 9 further specifies that the reference signals are "predetermined."

2. The "reference voltages/signals" terms. The "reference voltages/signals" terms, as can be seen in exemplary claims 1 and 9 above, occur throughout the claims across various components. A "reference signal" is broader than and includes a "reference voltage." *See* Ex. C at ¶ 53. The prior art reference Kitamura discloses the narrower element of "reference voltage," and so also discloses the broader "reference signal." *See id*. at ¶ 91. Similarly, for obviousness-type double patenting, the '851 patent discloses reference parameters that "are voltages," which meets the requirement for the "reference voltage" and the "reference signal." Ex. H at claim 3; Ex. C at ¶¶ 149-154. Thus, the invalidity analysis for "reference voltage" and "reference signal" is the same because the reference voltages in the references meet both limitations.

3. The remaining means-plus-function claim elements from claim 1. As can be seen above, these are the "memory cell programming means" and "comparator means" terms. Because of their means-plus-function claiming, they require identification of both appropriate structure and appropriate function.

1. <u>"Reference Voltage Selecting" Terms</u>

(a) "Reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information"

Claim 1 recites a "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states." As is prescribed by MPEP 2181(I), using the word "means" in this claim (*i.e.*, "selecting means") and including functional language (*i.e*., "selecting one of a plurality of reference voltages in accordance with said input information") invokes means-plus-function treatment. As the '571 patent discloses, the corresponding structure for the "reference voltage selecting means" includes at least the "verify reference select circuit 222." *See* Ex. C at ¶¶ 45-46.

For example, the '571 patent describes that the "voltage threshold of memory cell 102 is then determined by using the comparator 202 to compare the bit line voltage at terminal 168 with ***the selected verify reference voltage from the verify reference voltage select circuit 222***." Ex. A ('571) at 8:66-9:3 (emphasis added). "The verify reference voltage select circuit 222 analog ***output voltage X*** is determined by decoding the output of the n-bit input latch/buffer 224 (n=2 in

the illustrative form)." *Id*. at 9:11-14 (emphasis added). The "verify reference select circuit 222" also generates an analog voltage reference signal that is used by an analog comparator. *See id*. at 8:26-29 ("For the write mode of operation, a verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of an analog comparator 202."). Figure 8 echoes this by also showing the verify reference select circuit 222 providing the reference signal "X" to the comparator 202. *See id.* at Figure 8. Thus, the '571 patent discloses that the corresponding structure for the "reference voltage selecting means" includes at least the "verify reference select circuit 222."[2] *See* Ex. C at ¶ 46. The corresponding function is "selecting one of a plurality of reference voltages in accordance with the input information."[3] *See id*. at ¶ 46. Further information concerning the meaning of this term and its corresponding structure is included in the inventor notebook and testimony provided in Appendix A.

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[2] This claim construction mirrors Judge Illston's claim construction order in the parties' co-pending litigation. *See MLC Intellectual Prop., LLC v. Micron Tech., Inc*., No. 3:14-cv-03657, 2016 WL 6563343, at *5 (N.D. Cal. Nov. 4, 2016) ("[T]he specification clearly links the verify reference select circuit to the function recited in the claim. . . . The Court does not limit the structure to the specific structures disclosed in Figure 8, and thus the ***verify reference select circuit*** may include, but is not limited to, the structure designated as '222' in Figure 8.") (emphasis added). While Judge Illston's identification of the corresponding structure is perhaps slightly broader than "verify reference select circuit 222" because it is not limited to the specific structure designated as "222" in the '571 patent, the distinction is immaterial for purposes of this ex parte reexamination. Thus, the prior art discloses the corresponding structure under either construction.

[3] This matches the function adopted by Judge Illston in the co-pending litigation. *See MLC*, 2016 WL 6563343, at *5 ("For the foregoing reasons, the Court adopts the plain language function of 'selecting one of a plurality of reference voltages in accordance with the input information' with the corresponding structure of a verify reference select circuit.").

(b) "A selecting device which selects one of a plurality of [predetermined] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed"

This "selecting device" claim limitation from device claims 9, 12, and 30 is substantially similar to the "reference voltage selecting means" described directly above from claim 1. *See* Ex. C at ¶ 47. While this claim term is not explicitly written in means-plus-function form, it claims a generic device ("selecting device") with associated function ("which selects . . ."), thus requiring it to be construed in means-plus-function format. *See, e.g., Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1350 (Fed. Cir. 2015) (quoting *Mass. Inst. of Tech. & Elecs. For Imaging, Inc. v. Abacus Software*, 462 F.3d 1344, 1354 (Fed. Cir. 2006) ("Generic terms such as . . . 'device,'" are "nonce words that reflect nothing more than verbal constructs . . . used in a claim in a manner that is tantamount to using the word 'means' because they 'typically do not connote sufficiently definite structure' and therefore may invoke § 112, para. 6."). Based on the same disclosures from the '571 patent identified for the "reference voltage selecting means" above, the corresponding structure for the "selecting device" includes at least the "verify reference select circuit 222," and the function is "selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed."[4] *See* Ex. C at ¶ 47.

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[4] This claim construction mirrors Judge Illston's construction in the co-pending litigation. *See MLC*, 2016 WL 6563343, at *9 ("[T]his Court will construe this term as a means-plus-function term subject to § 112, ¶ 6. . . . The Court . . . construes the claim as having the structure of the ***verify reference select circuit***, pictured as example only in Fig. 8 as item 222, with the function of "***selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed***.") (emphases added). In

However, should the Office disagree that this "selecting device" term warrants means-plus-function treatment, a POSITA would have interpreted this "selecting device" component to be broad enough to include and be met by a device or process, that takes input information and selects, for a given memory cell's program/verify cycle, a reference signal from multiple reference signals such that the selected reference signal uniquely corresponds to the input information to be programmed in the memory cell. *See* Ex. C at ¶ 48. Further information concerning the meaning of this term and its corresponding structure is included in the inventor notebook and testimony provided in Appendix A.

(c) "Selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed"

This "selecting one of . . ." step from method claims 42 and 45 is substantially similar to the "reference voltage selecting means" described above from claim 1 but without requiring the means-plus-function treatment. Based on the same disclosures from the '571 patent identified for the "reference voltage selecting means" above, the proper construction for this term is

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construing the claimed function, Judge Illston replaced the phrase "in accordance with information indicating" with the phrase "that corresponds to." *See id.* This is a non-substantive variation in the plain claim language that merely clarifies the term, as Judge Illston recognized when she said, "[t]he Court ***adopts the same function*** . . . for [the 'selecting device . . .' term] as it did for [the 'reference voltage selecting means . . .' term]," and then proceeded to modify the language of the function slightly from her construction of the function for the "reference voltage selecting means" term. *Id.* Because the difference between the express claim language and the construction adopted by Judge Illston does not affect the invalidity analysis, either one could be used.

"selecting one of a plurality of reference signals that corresponds to a memory state to which the memory cell is to be programmed."[5] As discussed above for the "selecting device" term, replacing the phrase "in accordance with information indicating" with the phrase "that corresponds to" helps to clarify this term but does not alter its scope or meaning. *See* Ex. C at ¶ 49. Further information concerning the meaning of this element and the nature of devices that perform the claimed function is included in the inventor notebook and testimony provided in Appendix A.

2. <u>"Reference Voltages/Signals" Terms</u>

The three "reference voltage selecting" terms above interchangeably use "reference voltages" and "reference signals" to describe the same limitation. *Compare, e.g.*, Ex. A ('571) at Abstract ("Programming of the cell is verified by selecting a reference signal corresponding to the information to be stored and ***comparing a signal*** of the cell with the selected reference signal.") (emphasis added) with *id*. at 8:66-9:3 ("The voltage threshold of memory cell 102 is then determined by using the comparator 202 to ***compare*** the bit line ***voltage*** at terminal 168 with the selected verify reference ***voltage*** from the verify reference voltage select circuit 222.") (emphasis added); *see also* Ex. C at ¶ 53.

Further, the '571 patent indicates that a reference voltage/signal that can be either analog or digital. For example, in the analog context, the '571 patent describes that the "verify

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[5] This claim construction also mirrors Judge Illston's claim construction order in the co-pending litigation, in which she, once again, replaced "in accordance with information indicating" with "that corresponds to." *See MLC*, 2016 WL 6563343, at *15 ("The main difference between the [parties'] proposals seems to be grammatical, not substantive. Because this difference does not change the scope of the claim, plaintiff's more concise word choice is adopted as less confusing to a jury. . . . Accordingly, the Court construes 'selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed' as ***'selecting one of a plurality of reference signals that corresponds to a memory state to which the memory cell is to be programmed.'*** (emphasis added)).

reference voltage select circuit 222 provides an ***analog*** voltage reference level ***signal*** X to one input terminal of an analog comparator 202." Ex. A ('571) at 8:26-29 (emphasis added). In the digital context, the '571 patent discloses that the reference voltage can be an encoded digital signal, as described in connection with the implementation of a digital comparator. *See id*. at 11:50-56 (the "verify reference voltage select [circuit] 222 would provide the voltage to be ***encoded*** with the input coming from the output of the n-bit input latch/buffer 224, representing the data to be programmed.") (emphasis added); *see also* Ex. C at ¶ 50. Further, the '571 patent also describes a "signal" as a digital signal. *See* Ex. A ('571) at 10:17-19 ("A low logic level state of the PGM/Write signal on signal line 212 enables the timing circuit 208."); *see also* Ex. C at ¶ 51-52.

Thus, a person of ordinary skill in the art would have interpreted this "reference voltage/signal" feature to be broad enough to include and be met by either a digital reference voltage/signal or an analog reference voltage/signal. *See* Ex. C at ¶ 54; *see also MLC*, 2016 WL 6263343, at *16 ("Despite the analog embodiment, depicted in Figure 8, that includes reference voltages as opposed to signals, the specification makes clear that the technology can be implemented using analog or digital signals.").

3. Remaining Means-Plus-Function Terms

(a) "Memory Cell Programming Means"

Claim 1 recites a "memory cell programming means for programming said multi-level memory cell in accordance with said input information." Much like the "reference voltage selecting means" discussed above and as is prescribed by MPEP 2181(I), this "memory cell programming means" term requires an appropriate structure and function for construction. Because the functional language of the claim as it stands is sufficiently clear, no modification is needed. As such, the appropriate function of the "memory cell programming means" is "programming the multi-level memory cell in accordance with the input information." For structure, the '571 patent discloses the programing of the memory cell through bit line and word line voltages, which are both provided by the program voltage switch. *See* Ex. A at 10:17-37 (The "program voltage switch 220" outputs "bit line and word line program voltage outputs" during a "programming process" to "add charge to the floating gate of the memory cell."). As such, the appropriate structure for the "memory cell programming means" is "program/verify

timing circuitry and a program voltage switch having its outputs (1) a bit line and (2) a word line." *See* Ex. C at ¶ 55. This also matches Judge Illston's claim construction ruling. *See MLC*, 2016 WL 6263343, at *6.

(b) "Comparator Means"

Similar to the above explicitly claimed means-plus-function terms above, this "comparator means" term requires proper structure and function for construction. Claim 1 requires a "comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information." The '571 patent makes clear that the structure that compares the cell voltage to the selected reference voltage is a comparator. *See, e.g.,* Ex A ('571) at 3:13-16 ("The present multi-level memory device further includes a comparator means for comparing the memory state of the multi-level cell means with the input information."); *see also id*. at 8:66-9:3 ("The voltage threshold of memory cell 102 is then determined by using the comparator 202 to compare the bit line voltage at terminal 168 with the selected verify reference voltage from the verify reference voltage select circuit 222."). The proper function for this "comparator means" term is essentially the same as the plain claim language function, but clarifies the somewhat redundant claim language – "comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information." *See* Ex. C at ¶ 56. This is the same function and structure as Judge Illston's claim construction ruling. *See MLC*, 2016 WL 6263343, at *7.

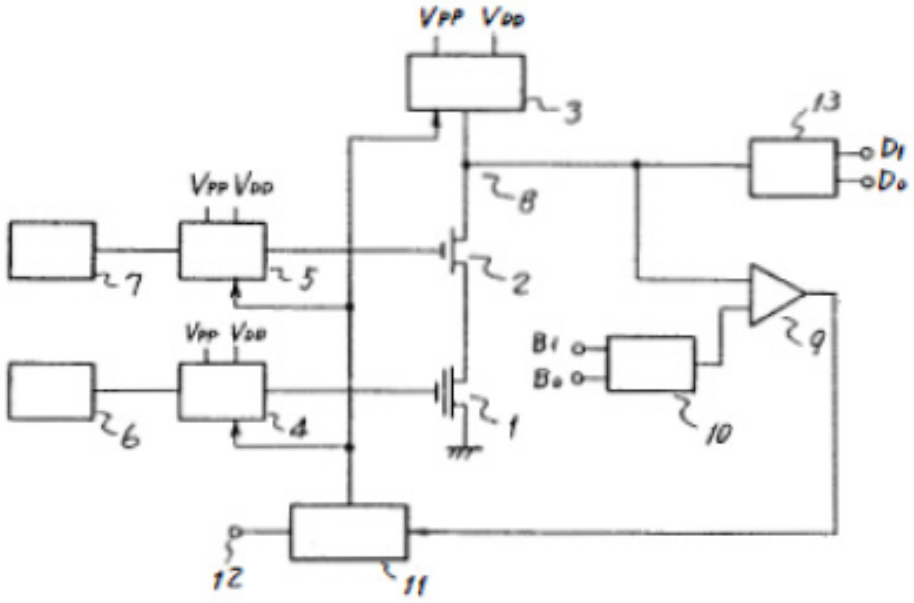
B. SNQ #1: Claims 1, 9, 12, 30, 42, and 45 are Obvious over Kitamura in view of VLSI Design

The combination of Kitamura and VLSI Design renders obvious each of claims 1, 9, 12, 30, 42, and 45 of the '571 patent. The following description and claim charts demonstrate in detail the correspondence between the elements in claims 1, 9, 12, 30, 42, and 45 and the combination of Kitamura and VLSI Design.

1. Electrically Alterable Non-Volatile Memory Cell (claims 1, 9, 12, 30, 42, 45)[6]

Kitamura discloses an electrically alterable, non-volatile memory device with a memory cell capable of storing two bits of information, requiring four memory states. *See* Ex. D at ¶¶ [01], [06], [09], [14], Ex. C at ¶¶ 68-69.

Specifically, Kitamura describes its MLC memory device, in part, with reference to Fig. 1, reproduced below.



Kitamura Fig. 1

As depicted in Fig. 1, the Kitamura memory device includes a memory cell 1 (depicted as a floating gate metal oxide semiconductor (MOS) transistor) capable of storing two bits of information corresponding to four memory states (*i.e.*, 2^2 memory states). *See* Ex. C at ¶¶ 68-69; *see also* Ex. D at ¶¶ [01], [06], [09], [13], [14]. The Kitamura memory device, like the claimed

[6] Like forms of this claim element appear in each of the Challenged Claims.

'571 memory device, can program the memory cell 1 to one of four memory states based on desired memory state input information (in the case of Kitamura, input information bits B_0 and B_1).[7] *See id*.

The Kitamura memory device programs the memory cell 1 by iteratively applying writing signals/programming pulses to the cell 1 to move the memory state of the memory cell 1 to the desired memory state (*e.g*., from memory state 0 to memory state 1, as shown in Table 1 in Section IX.B.2 below). *See* Ex. C at ¶¶ 71-75; Ex. D at ¶¶ [06]-[10], [13], [14]. Programming ceases when the Kitamura device determines that the memory cell 1 is correctly programmed to its desired memory state based on a comparison of a signal representing the current memory state of the cell 1 (*e.g*., on the bit line) with a signal representing the desired memory state, which corresponds to B_0 and B_1. *See* Ex. C at ¶¶ 77-80; *see also* Ex. D at ¶¶ [06]-[10], [13], [14].

Particularly, the Kitamura memory device includes an A/D (analog-to-digital) conversion circuit 13 to read and output the current state of the memory cell 1, a D/A (digital-to-analog) conversion circuit 10 to select (based on input bits B_0 and B_1) the reference signal/information corresponding to the desired memory state for the cell 1, and comparator 9 to compare the current memory state of the cell 1 to the desired memory state, from the D/A conversion circuit 10, to determine/verify if and when the cell 1 is correctly programmed to the desired memory state. *See* Ex. C at ¶¶ 73-80; *see also* Ex. D at ¶¶ [06]-[11], [14].

2. Reference Voltage Selecting Means (claim 1) / Selecting Device (claims 9, 12, 30) / Selecting One of a Plurality of Reference Signals (claims 42, 45)[8]

The inputs defining the desired state of the memory cell 1 (*i.e*., the memory state to which the cell 1 is to be programmed) are digital input bits B_0 and B_1. *See* Ex. D at ¶ [09], Fig. 1. Input bits B_0 and B_1 collectively define four memory states, *i.e*., 0,0; 1,0; 0,1; and 1,1. *See*

[7] The transistor 2 is used to select the memory cell 1, for example, to be read. *See* Ex. C at ¶ 71. When the memory cell 1 is selected, the transistor 2 is "turned on" to act as a direct connection (*e.g*., short) between the read point 8 and the memory cell 1. *See* Ex. C at ¶ 71.

[8] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

Ex. C at ¶¶ 68, 79. These desired memory state defining input bits are fed into the D/A conversion circuit 10. In turn, the D/A conversion circuit 10 converts the two digital bits B_0 and B_1 to an analog signal by selecting the analog signal that corresponds to bits B_0 and B_1. *See* Ex. D at ¶¶ [07], [09]; Ex. C at ¶¶ 79-82. For example, while Kitamura does not require this specific configuration, the mapping between the various values for B_0 and B_1 to their respective corresponding analog signal could be:

Table 1			
B_0, B_1	**D/A Output Voltage**	**Memory State**	**A/D Input Voltage Range[9]**
1, 1	0.5 Volts	1	0 to 1 Volts
0, 1	1.5 Volts	2	1.x to 2 Volts
1, 0	2.5 Volts	3	2.x to 3 Volts
0, 0	3.5 Volts	4	3.x to 4 Volts

Table 1

In this example, the plurality of reference signals is 0.5, 1.5, 2.5 and 3.5 Volts.[10] *See* Ex. C at ¶¶ 79-80. By way of example, if the values of input bits B_0 and B_1 are 1 and 0, respectively, the D/A conversion circuit 10 would select and provide an analog signal of 2.5 Volts to the comparator 9 to represent the memory state to which the memory cell 1 is to be programmed. *See id.* at ¶¶ 77-80.

Each of the four reference voltages output by Kitamura's D/A conversion circuit 10 corresponds to a different one of the four memory states of the memory cell. Ex. C at ¶¶ 79-80. In Kitamura's system, the different voltages output by the D/A conversion circuit 10 are clearly

[9] The A/D Input Voltage Range defines the range of analog voltages interpreted by the A/D conversion circuit 13 to be in a particular memory state. *See* Ex. C at ¶¶ 74-75. This results in the output(s) of the D/A conversion circuit 10 being in the middle of the respective memory state voltage ranges of the A/D conversion circuit 13. *See id*.

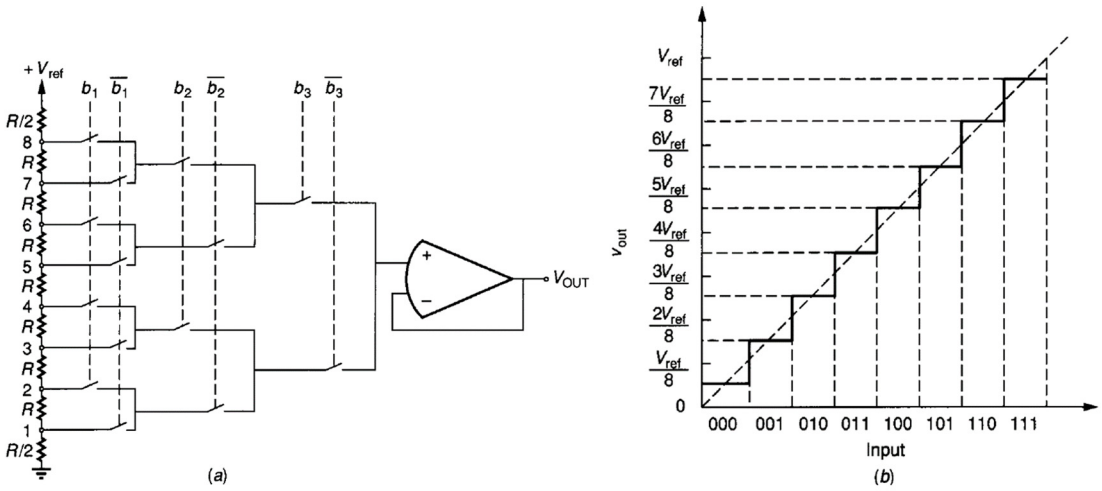
[10] Although this example configuration suggests the reference signals are linearly proportional, they need not be. Kitamura does not preclude other arrangements of spacing the reference voltages. *See* Ex. C at ¶ 76.

"reference voltages," because they serve as a references that memory cell voltage can be compared. *See id.* at ¶¶ 76-80. As discussed below, the analog signal from the D/A conversion circuit 10 is provided to the comparator 9 as a reference, and the comparator 9 indicates when the memory cell voltage has reached this reference level as an indication that the memory cell has reached the desired programming state. *Id.*

Although Kitamura is clear that the D/A conversion circuit 10 outputs the analog reference voltage for the desired memory state to be programmed, Kitamura does not specifically describe the internal operation of the D/A conversion circuit 10. Ex. C at ¶¶ 79-82. Thus, while Kitamura describes converting the 2-bit digital input to one of four predetermined voltages, Kitamura does not explicitly demonstrate how this conversion functionality *selects* the reference voltage to output.

However, it would have been obvious to a POSITA that Kitamura D/A conversion circuit 10 selects the reference voltage from among a plurality of reference voltages as part of the conversion process in view of VLSI Design. Ex. C at ¶¶ 82-91. Kitamura mentions that the D/A conversion circuit 10 has "a voltage dividing element and a reference voltage supply," but does not describe further structure of the circuit. Ex. D at ¶ [11]. As a result, a POSITA implementing the techniques of Kitamura naturally would have looked to other references, such as VLSI Design, for digital-to-analog conversion circuits and techniques to implement the D/A conversion circuit 10. Ex. C at ¶¶ 82-83.

VLSI Design is a textbook that describes circuit design techniques, including techniques for digital-to-analog conversion. Ex. E at 626-629. One well-known type of digital-to-analog converter (DAC) described by VLSI Design is the voltage-scaling D/A converter. *Id.* This DAC uses "series resistors connected between Vref and ground to selectively obtain voltages between these limits." *Id*. at 626. The series resistors have taps between them, and each tap represents a different predetermined voltage level. *Id.* at 626-629; Ex. C at ¶¶ 86-89. "Each tap is connected to a switching tree" controlled by the digital input to the converter. *Id.* at 627. Based on the digital input signal, the switching tree selects one of the predetermined voltages at the taps to connect as the analog output voltage of the circuit. *Id.* at 627-629; Ex. C at ¶¶ 86-89.



The D/A conversion circuit 10 of Kitamura, implemented as a voltage-scaling DAC as taught by VLSI design, would represent a "reference voltage selecting means" or "selecting device" according to the claims of the '571 patent. Ex. C at ¶¶ 91, 101-103. The taps between the series resistors would make available all four of the analog voltages corresponding to Kitamura's memory states, and the switching tree would select one of these analog voltages according to Kitamura's bits B_0 and B_1 that represent the input information to be stored in the memory cell. Ex. C at ¶ 90.

A POSITA would have had several reasons to implement Kitamura's D/A conversion circuit 10 using the voltage-scaling DAC techniques of VLSI Design. Ex. C at ¶¶ 83-85. First, a POSITA would have used the voltage-scaling DAC because it performs the same function performed by Kitamura's D/A conversion circuit 10. *Id.* at ¶ 83. In Kitamura, the voltage-scaling DAC would perform the well-known function of digital-to-analog conversion in the same predictable manner disclosed in VLSI Design. *Id.* at ¶¶ 83, 90-91.

A POSITA would have been motivated to use a voltage-scaling D/A converter to achieve the benefits mentioned by VLSI Design, for example, to implement a design that "is very regular and thus well suited for MOS technology." Ex. C at ¶ 84-85. The ability to easily manufacture this type of DAC, including the very small number of elements and the simplicity of those parts (e.g., switches, resistors, and a buffer amplifier), would have also motivated a POSITA to use the DAC from VLSI Design. *Id.* A POSITA would also have been motivated to use the VLSI Design DAC because it "guarantees monotonicity, since the voltage at each tap cannot be greater than the tap below it." Ex. D at 629. A POSITA would also have recognized that because

Kitamura's D/A conversion circuit 10 is a small 2-bit DAC, circuit size constraints and parasitic capacitance would not be a concern as they might be with DACs that convert many more bits. Ex. C at ¶ 85.

The VLSI Design example shown in Fig. 8.2-14 is a 3-bit DAC, and a POSITA would have found it obvious to use a 2-bit version, since that is what is used in Kitamura. Ex. C at ¶ 90. A POSITA would also have recognized that a 3-bit DAC provides 2-bit DAC functionality, e.g. when the least significant bit, b_1, is held constant. *Id.* at ¶¶ 87, 90. Thus, the full 3-bit example circuit of VLSI Design or a 2-bit version would have been obvious as a simple substitution for Kitamura's D/A conversion circuit 10. *Id.*

Thus, it would have been obvious to a POSITA to implement the D/A conversion circuit 10 of Kitamura as a voltage-scaling DAC as taught by VLSI Design. Ex. C at ¶¶ 90-91.

In this manner, Kitamura in view of VLSI Design render obvious the function and corresponding structure for the "reference voltage selection means" (claim 1). *Id.* at ¶¶ 90-91. As discussed above in Section IX.A.1(a), the corresponding function for this term is "selecting one of a plurality of reference voltages in accordance with the input information." Kitamura's D/A conversion circuit 10, implemented using the voltage-scaling technique of VLSI Design, performs this function by selecting one of the predetermined reference voltages at the taps along a series of resistors. *Id.* at ¶ 90. The D/A conversion circuit 10 makes the selection according to the input information (e.g., Kitamura's digital signals B_0 and B_1) representing the information to be stored in a memory cell. *Id.* at ¶¶ 79-82; Ex. D at ¶ [09]. The corresponding structure for the "reference voltage selecting means" includes at least the "verify reference select circuit 222." Kitamura's D/A conversion circuit 10, implemented as a voltage-scaling DAC, is equivalent to the "verify reference select circuit 222." Ex. C at ¶¶ 101-102. Both select and output the analog reference voltage encoded by a 2-bit digital input signal. Ex. A at 11:54-57, 9:11-14; Ex. D at ¶ [09]; Ex. C at ¶¶ 90-90, 101-102. Both also provide the selected analog output voltage to a comparator. Ex. A. at Fig. 8; Ex. D at Fig. 1.

Kitamura in view of VLSI Design render obvious the function and corresponding structure for the "selecting device" (claims 9, 12, and 30). The corresponding function is "selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed." The corresponding structure for the "selecting device" includes at least the "verify reference select circuit 222." Kitamura's D/A

conversion circuit 10, implemented using the voltage-scaling technique of VLSI Design, is equivalent to the "verify reference select circuit 222" as discussed above. Ex. C at ¶¶ 101-102. The output voltage selected by the D/A conversion circuit 10 is the voltage that corresponds to the memory state to be programmed, because the voltage is clearly specified by "the two-bit input digital signals **B_0 and B_1 to be written**" to the memory cell. Ex. D at ¶ [09] (emphasis added); *see also id.* at ¶ [14] (programming continues "until the output voltage . . . coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion).

Thus, the D/A conversion circuit 10 of Kitamura in view of VLSI Design has a structure that is equivalent to or at least renders obvious the corresponding structure of the claimed "reference voltage selection means" (claim 1) and "selecting device" (claims 9, 12, and 30) of the '571 patent. The D/A conversion circuit 10 performs the same function as the "verify reference select circuit 222," in substantially the same way to achieve substantially the same result. *See* MPEP 2183; Ex. C at ¶¶ 90-90, 101-102. There are also no substantial differences between the D/A conversion circuit 10 of Kitamura in view of VLSI Design compared to the "verify reference select circuit 222" that serves as corresponding structure under § 112, ¶ 6, showing equivalence under the "insubstantial differences" test. *Id.*

The evidence and testimony included in Appendix A further support the requester's positions with respect to obviousness of these "selecting" elements.

3. Memory Cell Programming Means (claim 1) / Programming Signal Source (claims 9, 12, 30) / Applying a Programming Signal [11](claims 42, 45)[12]

The memory cell programming and verification process of Kitamura is similar to that described in the '571 patent and renders the memory cell programming means, programming

[11] The discussion in this Section is applicable to terms "memory cell programming means," "programming signal source" and "applying a programming signal."

[12] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

source, and application of the programming signal obvious to one of ordinary skill in the art as described below.

(a) Memory Cell Programming in the '571 Patent

The '571 patent describes that programming a memory cell to its desired memory state involves an iterative process during which programming pulses are applied to the memory cell and, after each programming pulse, a verification process compares the current memory state of the memory cell (*e.g.*, by use of the cell's bit line voltage) to a reference signal corresponding to the desired memory state. *See, e.g.*, Ex. A at Abstract; 10:14-60 ("Programming . . . is verified by selecting a reference signal corresponding to the information to be stored and comparing a signal of the cell with the selected reference signal"); *see also* Ex. C at ¶¶ 30-43. When the verify process confirms the memory cell is programmed to the desired memory state, *e.g.*, based on a comparison indicating the bit line signal exceeds the reference signal corresponding to the desired memory state, programming is stopped. *See* Ex. A at 10:26-37, 10:52-60; *see also* Ex. C at ¶¶ 30, 37.

Figure 11 of the '571 patent shows this iterative, stair-step programming pulse and verification process, where the memory cell is being programmed to the desired memory state (1,0), as shown on the y-axis, corresponding the reference signal Vref3. *See id*. Each stair step in the illustrated time-changing voltage of the memory cell (*e.g.*, bit line voltage) represents an additional programming pulse applied to the memory cell to drive the voltage towards a reference voltage within the voltage range defining the desired memory state (*i.e.*, in between Vt2 and Vt3 defining the memory state (1,0)). *See* Ex. A at 8:26-40, Ex. C at ¶¶ 31-33. In this example, the determination of when the cell is programmed to the desired memory state is based on a comparison between the cell's bit line voltage, which is proportional to its threshold voltage, and Vref3. *See id*. In other words, the programming pulses are applied to the memory cell until the bit line voltage representing the cell's current memory state exceeds Vref3, which corresponds to memory state (1,0), indicating that the cell has been correctly programmed to the (1,0) memory state. *See id*. Figure 8 of the '571 patent shows a functional-level block diagram implementation of the memory read and program and verification processes.

(b) Memory Cell Programming in Kitamura

Kitamura describes an iterative process whereby a writing signal/programming pulse is applied to the memory cell 1 followed by a read/verification process to determine if the writing signal put the memory cell 1 into its desired memory state. *See* Ex. C at ¶¶ 69-75; Ex. D at ¶ [08] ("This write mode signal causes the read/write switching signal generation circuit 11 to generate read/write signals that **periodically repeat** a write period whose level is one binary value and a read period whose level is the other binary value.") (emphasis added), ¶ [14] "writing and reading are **repeated at short periods** until the output voltage. . . coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion") (emphasis added), ¶¶ [06]-[10], [13]. The programming process continues (*e.g.*, serial writing signals/programming pulses are applied) until the memory cell is correctly programmed, as determined by the comparator 9. *See id*.

The read/write switching signal generation circuit 11 controls the writing signals/programming pulses applied to the memory cell 1. *See id*. The read/write switching signal generation circuit 11 is enabled by the output of the comparator 9. *See* Ex. D at ¶ [09] ("[B]ut when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation."). The operation of the comparator 9 is described in more detail below in Section IX.B.4.

The read/write switching signal generation circuit 11 controls the application of programming pulses to the memory cell 1 by generating read/write signals that then cause[13] the driver circuit 4 to provide a writing signal (V_{pp}) to the memory cell 1 on its word line and the load circuit 3 to couple a writing signal (V_{pp}) to the memory cell 1 on its bit line—these three devices perform the same functions as the Program Voltage Switch 220 and Program/Verify

[13] The read/write switching signal generation circuit 11 also causes driver circuit 5 to apply either V_{pp} or V_{dd} to transistor 2, for program and read processes respectively, to enable the memory cell 1 to be programmed or read, as applicable. *See* Ex. C at ¶¶ 76-81; Ex. D at ¶¶ [07]-[10] ("In the write period, a voltage close to V_{PP} is outputted from the drivers 4 and 5 and provided to the memory cell 1 and the MOS transistor 2, and in the read period, a voltage close to V_{DD} is outputted and provided to the memory cell 1 and the MOS transistor 2.").

Timing Circuitry 208 of the '571 patent but through a multi-device, stepped process (as noted above). Ex. C at ¶¶ 93-99. The Program Voltage Switch 220 and Program/Verify Timing Circuitry 208 serve as part of the corresponding structure for the "memory cell programming means." *See* Section IX.A.3(a), *supra*. As discussed further below, the structure represented by the Program Voltage Switch 220 and Program/Verify Timing Circuitry 208 is obvious in view of Kitamura, even though Kitamura illustrates the functions of these components being performed by a greater number of circuit elements. Ex. C at ¶¶ 93-99. It would have been obvious to one of ordinary skill in the art to combine the read/write switching signal generation circuit 11, the driver circuit 4 and the load circuit 3 for use in performing the programming function *(e.g.*, applying a program signal) of the "memory cell programming means" and "programming signal source." *See* Ex. C at ¶¶ 76-78; Ex. D at ¶¶ [07]-[10] ("The switching circuit 3 supplies V_{PP} during the write period, and V_{DD} during the read period, to the read point 8;" "In the write period, a voltage close to V_{PP} is outputted from the drivers 4 and 5 and provided to the memory cell 1."). Indeed, Kitamura's disclosure explicitly uses these elements together to program its memory cell 1. *Id.* The application of these writing signals to the memory cell 1 causes the memory cell to change its threshold voltage, which, in turn, results in memory state changes. *See* Ex. D at ¶¶ [09], Fig. 2; Ex. C at ¶¶ 76-81.

The read/write switching signal generation circuit 11 also controls the reading/verification of the memory cell to, in part, determine the cell's current memory state. *See* Ex. D at ¶¶ [08], [10]. Namely, the read/write switching signal generation circuit 11 generates read/write signals that cause the driver circuit 4 to provide a reading signal (V_{dd}) to the word line and cause the load circuit 3 to couple a reading signal (V_{dd}) to the bit line. *See id.* With these signals applied, the current state of the memory cell is determined by observing (reading) the signal on the memory cell's bit line at "read point 8." *See* Ex. D at ¶¶ [08], [10] ("8 is a read point from the memory cell 1"), *see also* Ex. C at ¶¶ 77-78. These programming and read/verification steps continue until the memory cell 1 is programmed to its desired memory state. *See* Ex. C at ¶¶ 77-78; Ex. D at ¶¶ [09], [14].

Kitamura's application of control signals to a memory cell's word line and bit line for programming purposes is the same as or renders obvious the technique described in the '571 patent. *See* Ex. A at 8:46-53 ("The output signal from the analog comparator is provided on a signal line 204 as an enable/disable signal for the program voltage switch 220. An output signal

line 206 from the **program voltage switch 220 provides the word line program voltage to the control gate of the EANVM cell 102. Another output signal line 106 constitutes the bit line and provides the bit-line programming voltage to the bit-line terminal 168 of EANVM cell 102**.") (emphasis added); Ex. C at ¶ 75-78.

(c) Kitamura Renders Obvious the Function and Corresponding Structure of the "Memory Cell Programming Means"

As discussed above in Section X.A.3(a), the function of the "memory cell programming means" is "programming the multi-level memory cell in accordance with the input information." The corresponding structure for the "memory cell programming means" is "program/verify timing circuitry and a program voltage switch having its outputs (1) a bit line and (2) a word line." Kitamura at least renders obvious this function and corresponding structure. Ex. C at ¶¶ 93-101.

Kitamura's system programs the memory cell 1, which is a multi-level memory cell, based on input information, e.g., "the two-bit input digital signals B_0 and B_1 to be written." Ex. D at ¶ [09]; *see also id.* at ¶ [14] (writing continues "until the output voltage [for the memory cell] . . . coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion"). Thus, Kitamura's circuit performs the function of "programming the multi-level memory cell in accordance with the input information." Ex. C at ¶¶ 75-79, 93.

The corresponding structure for the "memory cell programming means" includes "program/verify timing circuitry." In the '571 patent, program/verify timing circuitry 208 "provides a series of program/verify timing pulses to the program voltage switch 220," to specify when to apply a programming signal and when to verify the current programming state. Ex. A at 8:53-66, 10:19-35; Ex. C at ¶ 93. The timing pulses specify a sequence of alternating programming cycles and verification cycles that continue until the memory cell is correctly programmed. *Id.* Kitamura discloses a "read/write switching signal generation circuit 11" that is equivalent to the program/verify timing circuitry 208 of the '571 patent. Ex. C at ¶¶ 93-94. Kitamura's read/write switching signal generation circuit 11 "generate[s] read/write signals that **periodically repeat a write period** whose level is one binary value **and a read period** whose level is the other binary value." Ex. D at ¶ [08] (emphasis added); Ex. C at ¶¶ 80, 93-94. Kitamura's read/write switching signal generation circuit 11 operates in the same manner as the

timing circuitry 208, by providing timing pulses (e.g., "read/write signals") that specify a repeating pattern of a program cycle (e.g., "write period") followed by a verify cycle (e.g., "read period"). In the '571 patent, the "internally controlled program/verify cycle repeats itself until the bit line voltage on terminal 168 exceeds Vref3." Ex. A at 10:27-34. Kitamura's circuit 11 defines cycles that continue in the same manner, as "writing and reading are repeated at short periods until the output voltage . . . coincides with a voltage" representing the desired memory state. Ex. D at ¶ [14].

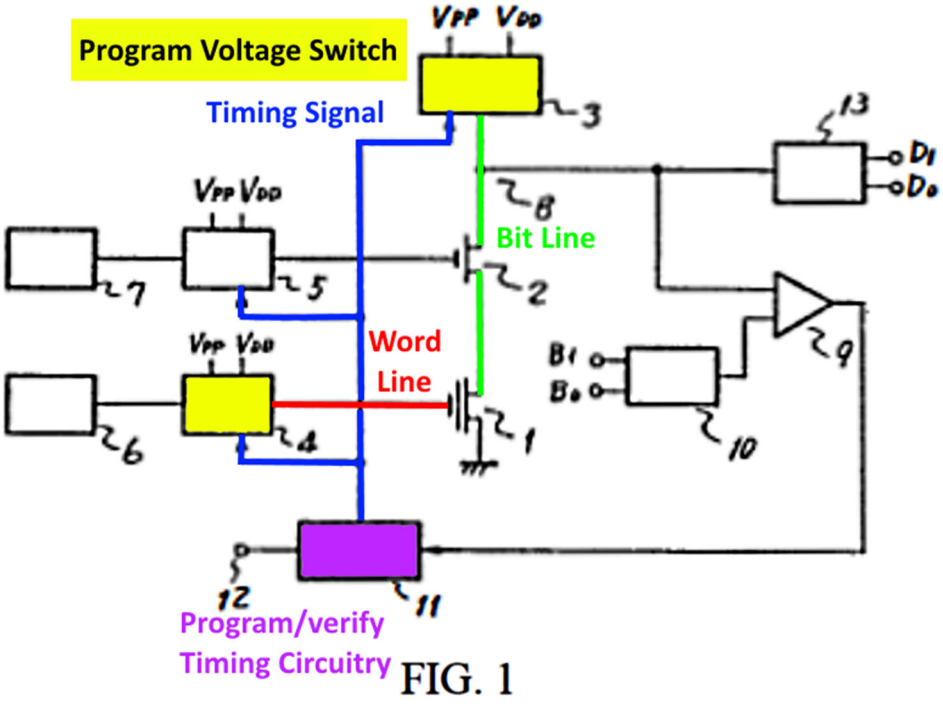
The corresponding structure for the "memory cell programming means" also includes a "program voltage switch having its outputs (1) a bit line and (2) a word line." In the '571 patent, the bit line connects to the drain of the memory cell. Ex. A at 6:55-57, Fig. 8. The word line is connected to the control gate of the memory cell. *Id.* at 6:59-61, Fig. 8. A "program voltage switch 220" receives the timing pulses from the timing circuitry 208 and responds by providing outputs on the bit line and the word line, where the outputs are different during a program cycle and a verify cycle. *Id.* at 10:27-34. For a low level of a timing pulse, the voltage switch 220 causes "voltage outputs on lines 106 and 206 [to] be raised 25 to their respective programming voltage levels." *Id.* at 10:24-26. For the high level of a timing pulse, "the programming voltages are removed and a verify cycle begins." *Id.* at 10:27-34.

Kitamura's load circuit 3 and driver circuit 4 are equivalent to the program voltage switch 220 of the '571 patent. Ex. C at ¶¶ 95-100. The load circuit 3 and driver circuit 4 both act as switches:

> [circuit] **3 is a load circuit that switches** between a write-use high voltage power supply (VPP) and a read-use low voltage power supply (V_{DD}), [circuits] **4 and 5 are driver circuits that output** a high voltage during writing and a low voltage during reading **by switching** the power supply between V_{PP} and V_{DD}. . . .

Ex. D at ¶ [07]. The load circuit 3 and the driver circuit 4 each switch between different outputs responsive to the timing signals from the read/write switching signal generation circuit 11, in the same manner that the program voltage switch 220 responds to pulses from the timing circuitry 208 of the '571 patent. Ex. C at ¶¶ 95-98; Ex. D at ¶¶ [07]-[09], Fig. 1; Ex. A at 10:22-34, Fig. 8. The load circuit 3 applies a voltage on the memory cell on a bit line, e.g., to the drain of the memory cell. Ex. D at Fig. 1; Ex. C at ¶ 70. The output of driver circuit 4 applies a voltage to the memory cell on a word line, e.g., to the control gate of the memory cell. *Id.* Thus, Kitamura's load circuit 3 and driver circuit 4 operate in substantially the same manner as the

program voltage switch 220, by switching their outputs to supply programming voltages (V_{PP}) for a write period, and applying read voltages (V_{DD}) for a read period used to assess and verify memory cell programming state. Ex. C at ¶¶ 95-98; Ex. D at ¶¶ [07]-[09]; Ex. A at 10:22-34. The correspondence is also indicated in the annotated figures below.



Annotated Fig. 1 of Kitamura

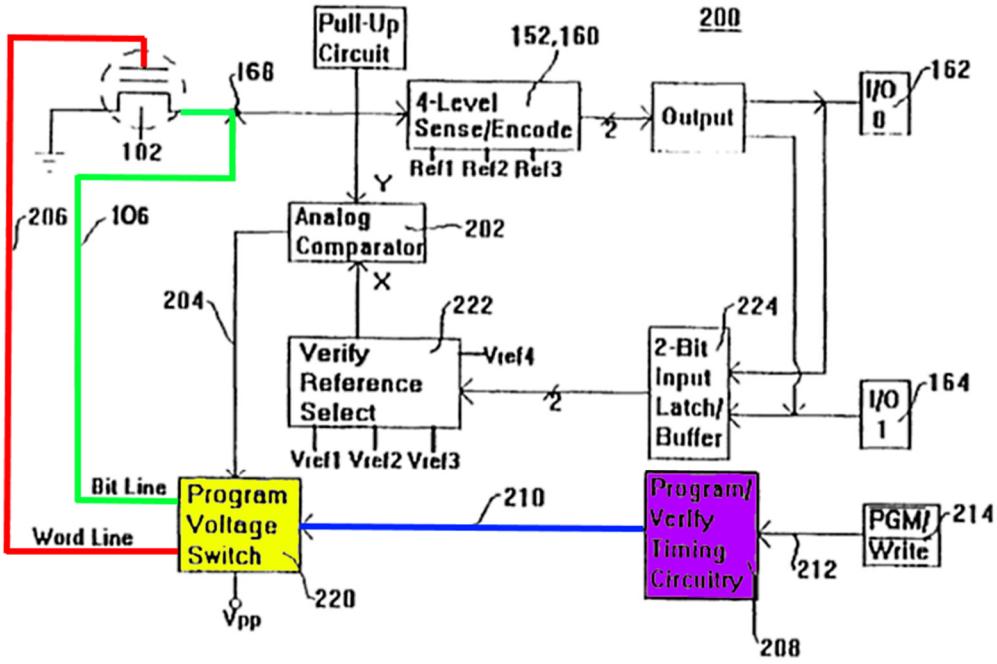


Figure 8

Annotated Fig. 8 of the '571 Patent

For these reasons, Kitamura's circuit discloses elements that are equivalent to the corresponding structure of the "memory cell programming means," by virtue of performing the same function in substantially the same way, to produce substantially the same results as the corresponding structure disclosed in the '571 patent's specification. *See* MPEP 2183; *Kemco Sales, Inc. v. Control Papers Co.*, 208 F.3d 1352, (Fed. Cir. 2000) ("two structures may be 'equivalent' for purposes of section 112, paragraph 6 if they perform the identical function, in substantially the same way, with substantially the same result.").

The Kitamura circuitry is also equivalent to the corresponding structure of the "memory cell programming means" under the insubstantial differences test. Under this test, an element is equivalent if it "results from an insubstantial change which adds nothing of significance to the structure, material[,] or acts disclosed" in the relevant patent. *Valmont Indus., Inc. v. Reinke Mfg. Co.*, 983 F.2d 1039, 1043 (Fed. Cir. 1993); *see also* MPEP 2183.

In the present case, the differences between Kitamura's circuitry and the corresponding structure for the "memory cell programming means" are insubstantial. The '571 patent uses a

single circuit for the "program voltage switch 220," and Kitamura shows two circuits: the load circuit 3 and the driver circuit 4. *See* Ex. D at Fig. 1; Ex. A at Fig. 8; Ex. C at ¶ 98. Representing the circuitry as one circuit or two circuits in a block diagram does not substantively alter the structure or operation of the circuits. Ex. C at ¶ 98. Similarly, providing comparator output to the read/write switching signal generation circuit 11 (equivalent to the '571 patent's timing circuitry 208), rather than to the program voltage switch 220 as in the '571 patent is not a significant difference. *Id.* at ¶ 99. In both systems, the comparator output causes the programming circuitry to disable further write cycles when the correct memory state is reached. Ex. C at ¶ 99; Ex. D at ¶ [09]; Ex. A at 8:53-66, 10:19-35. Although Kitamura's circuits 3, 4 do not receive the comparator output directly, the circuits 3, 4 are nonetheless stopped from applying further programming voltages on the basis of the comparator output. Ex. C at ¶ 99. This occurs because the read/write switching signal generation circuit 11 stops signaling any further write cycles when the comparator output indicates correct cell programming, which in turn stops the circuits 3, 4 from further programming operations. *Id.*; Ex. D at ¶ [09]. Thus, while Kitamura routes the comparator output slightly differently than the '571 patent, Kitamura's circuitry uses the comparator output for the same purpose to achieve the same result as in the '571 patent. *Id.* Specifically, the circuits 3, 4 that are equivalent to the "program voltage switch 220" are stopped from further applying a programming signal due to the comparator output, similar to the operation in the '571 patent. *Id.*

Therefore, Kitamura discloses or at least renders obvious the "memory cell programming means" (claim 1). The "programming signal source" (claims 9, 12, 30) and the method step of "applying a programming signal" (claims 42, 45) have not be construed as means-plus-function terms, but are nevertheless disclosed through the same elements and processes discussed above.

4. <u>Comparator Means (claim 1) / Comparator (claim 9)/ Verifying Device (claim 12) / Control Device (claim 30) / Verifying Whether Said Memory Cell is Programmed to the State Indicated by Said Information (claim 42) / Detecting a Parameter Indicating the State</u>

of the Memory Cell (claim 42) / Controlling the Application of Said Programming Signal (claim 45) [14]

After each writing signal/programming pulse in the programming and verification process of Kitamura, the comparator 9 compares the signal representing the current memory state of the memory cell (*i.e.*, by observing the voltage at "read point 8") with the signal representing the desired memory state to which the memory cell is to be programmed (*i.e.*, the analog voltage output by the D/A conversion circuit 10), in accord with input bits B_0 and B_1. *See* Ex. D at ¶ [09]; Ex. C at ¶¶ 77-78. The programming process continues until the comparison indicates that the signal at read point 8 (representing the current memory state) is higher than the output of the D/A conversion circuit 10 (representing the desired memory state):

> Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals [B_0 and B_1].

Ex. D at ¶ [09], *see also* Ex. C at ¶¶ 77-78.

Thus, when the memory cell 1 is programmed to the desired memory state, the output of comparator 9 causes the read/write switching signal generation circuit 11 to stop programming the memory cell 1. *See id*.; *see also* Ex. C at ¶¶ 79, 104. This shows that Kitamura's comparator 9 performs the same function as the "comparator means" of claim 1 of the '571 patent "comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is

[14] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

the state corresponding to the input information." *Id.* Further, Kitamura's comparator 9 is an analog comparator, the same structure that is the corresponding structure for the "comparator means." *Id.*

5. Example Comparison of Kitamura and VLSI Design with the '571 Patent

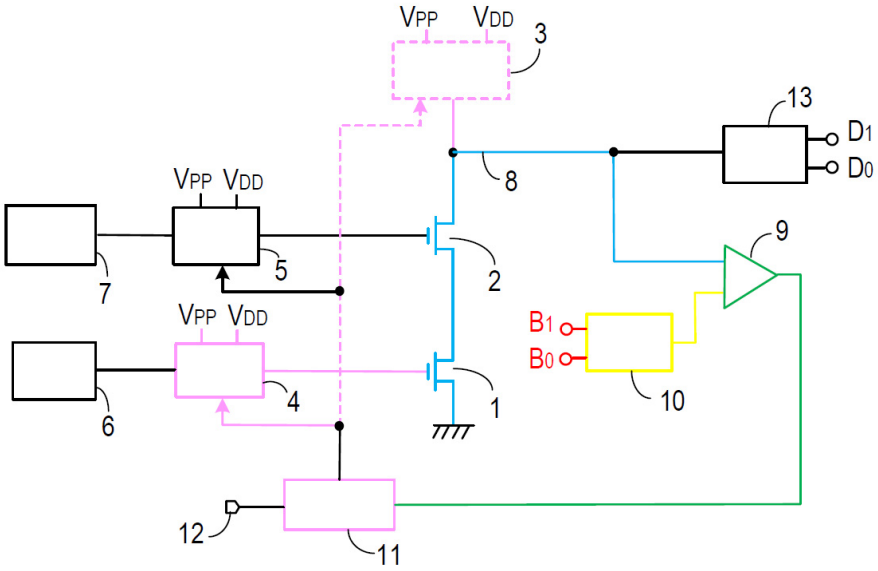
The following color-coded table and figures show the features of the '571 patent disclosed by Kitamura in the context of figures from each.[15]

Table 2		
	Kitamura	**'571 Patent**
Electrically alterable non-volatile memory cell	Memory cell 1	Memory cell 102
Input information corresponding to the desired memory state	B_0, B_1	I/O 0 (162), I/O 1 (164)
Selecting device / Selecting one of a plurality of reference signals in accordance with the input information	D/A conversion circuit 10	Verify Reference Select device 222
Verifying Device / Control Device / Verifying Whether Said Memory Cell is Programmed to the State Indicated by Said Information / Detecting a Parameter Indicating the State of the Memory Cell /	Comparator 9	Analog comparator 202

[15] This comparison does not represent Requester's full position, but is a high-level, illustrative comparison of two example figures from the '571 patent and Kitamura intended to serve as a summary for convenience.

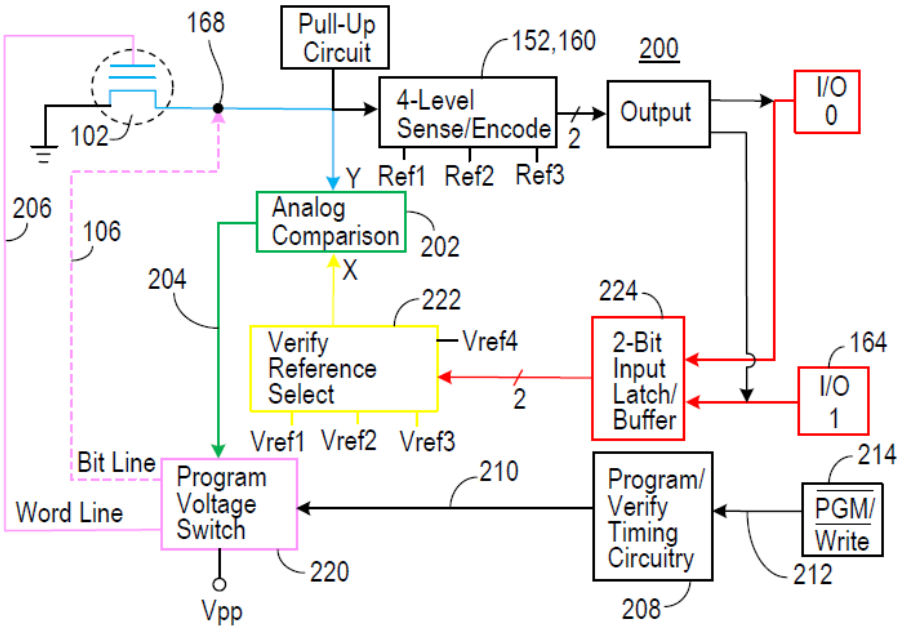
Controlling the Application of Said Programming Signal		
Memory Cell Programming Means / Programming signal source / Applying a programming signal[16]	Read/write switching signal generation circuit 11, Load circuit 3, Driver circuit 4	Program/verify timing circuitry 208, Program voltage switch 220

Table 2



Kitamura, Fig. 1 (annotated)

[16] Other components from Kitamura and the '571 patent are also involved in the programming/verification process such as, in the context of the '571 patent, verify reference select device 222 and comparator 202. *See* Ex. A at 10:14-36, 8:34-45. The use of additional components does not change the analysis. The claim constructions adopted by the District Court do not include these additional components as corresponding structure for the "memory cell programming means." Indeed, the verify reference select device 222 and comparator 202 were construed by the Court to correspond to the "reference voltage selecting means" and "comparator means," not the "memory cell programming means."



'571 patent, Fig. 8 (annotated)

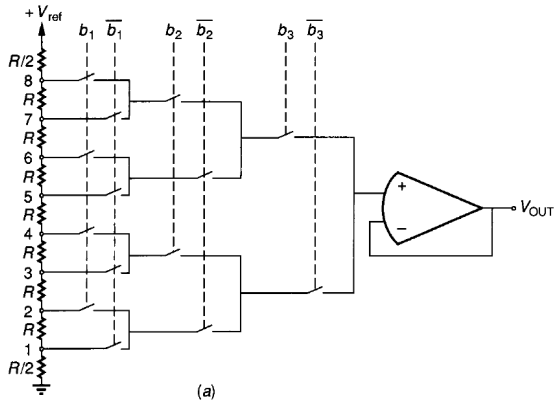
As explained in greater detail in the following Claim Chart I, the features of the Challenged Claims of the '571 patent are rendered obvious by Kitamura in view of VLSI Design, and thus, unpatentable under 35 U.S.C. § 103. *See* Ex. C at ¶¶ 64, 105.

CLAIM CHART I	
'571 Patent	**Kitamura & VLSI Design**
[1a] A multi-level memory device comprising:	Kitamura discloses a multi-level memory device. "A non-volatile memory that includes a semiconductor non-volatile memory element whose characteristic is continuously varied by writing; a circuit that alternately switches between a write mode and a read mode at regular time intervals; a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that converts an analog signal that has been read into a digital signal." Ex. D at ¶ [01]. "It is an object of the present invention to reduce the number of memory elements and lower the price by **storing a plurality of bits in a single memory element**." *Id*. at ¶ [05] (emphasis added). "Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher

	than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." *Id.* at ¶ [09]. "As described above, with the present invention, writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion, and this **allows a plurality of bits of digital data to be written to the memory cell transistor of a single element**, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). *See id.* at Fig. 1, Ex. C at ¶¶ 68-69.
[1b] an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;	Kitamura discloses an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$. "The working example in FIG. 1 shows the circuit of a **one-element, two-bit nonvolatile memory** . . . ." Ex. D at ¶ [12] (emphasis added). "It is an object of the present invention to reduce the number of memory elements and lower the price by storing **a plurality of bits in a single memory element**." *Id.* at ¶ [05] (emphasis added). "Meanwhile, **the two-bit input digital signals B_0 and B_1 to be written** are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. **Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2.**" *Id.* at ¶ [09] (emphasis added). "As described above, with the present invention, writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion, and **this allows a plurality of bits of digital data to be written to the memory cell transistor of a single**

	element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). *See id.* at Fig. 1; Ex. C at ¶¶ 68-69. As a digital system, Kitamura's device uses a binary number system so value of K is 2. Ex. C at ¶¶ 68-69. Kitamura explicitly mentions storing two bits per memory cell. As a result, $K^n = 4$, which meets the requirement of being greater than 2. *Id.*
[1c] memory cell programming means for programming said multi-level memory cell in accordance with said input information;	Kitamura discloses a memory cell programming means for programming said multi-level memory cell in accordance with said input information. "When data is written, first an address for selecting the memory cell 1 is provided from the outside to the address decoders 6 and 7, and a write mode signal is provided to the mode switching terminal 12. **This write mode signal causes the read/write switching signal generation circuit 11 to generate read/write signals that periodically repeat a write period whose level is one binary value** and a read period whose level is the other binary value. **In the write period, a voltage close to V_{PP} is outputted from the drivers 4 and 5 and provided to the memory cell 1 and the MOS transistor 2**, and in the read period, a voltage close to V_{DD} is outputted and provided to the memory cell 1 and the MOS transistor 2. The switching circuit 3 supplies VPP during the write period, and V_{DD} during the read period, to the read point 8." Ex. D at ¶ [08] (emphasis added). "Since the floating gate MOS transistor 1 and the MOS transistor 2 constitute a ratio circuit with the load circuit 3, when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3. **Meanwhile, the two-bit input digital signals B0 and B1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation**. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." *Id.* at ¶ [09] (emphasis added). "As described above, with the present invention, **writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element**, and allows a non-volatile memory to be obtained in

	which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). "The relation between the write time t of the memory cell 1 and the threshold voltage V_T of the memory cell 1 . . . is the relation shown in FIG. 2 under constant voltage conditions, and V_T rises as the write period lengthens." *Id*. at ¶ [09]. *See id.* at Figs. 1 and 2, Ex. C at ¶¶ 74-79, 93-100. Kitamura discloses structure (e.g., the read/write switching signal generation circuit 11, the load circuit 3, and driver circuit 4) that is equivalent to or at least renders obvious the corresponding structure for the "memory cell programming means." Ex. C at ¶¶ 93-100.
[1d] reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and	Kitamura and VLSI Design render obvious a reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states. **Kitamura describes:** "A non-volatile memory that includes . . . a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result . . . ." Ex. D at ¶ [01]. "[W]hen the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes . . . . Meanwhile, the **two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals**, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals [B_0 and B_1]." *Id.* at ¶ [09] (emphasis added). Kitamura's memory cell stores two bits of information, which requires the cell to have four memory states, one for each of the possible bit combinations: 1,1; 1,0; 0,1; and 0,0. Ex. C at ¶¶ 68-69, 79-80. When the D/A conversion circuit 10 receives input information bits B_0 and B_1, the digital-to-analog conversion provides one of four reference voltages that each correspond to a different one of the four memory states of the memory cell. Ex. C at 79-80.

	"As described above, with the present invention, writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting **a plurality of bits of digital signal to D/A conversion, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element**, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). *See id.* at Fig. 1, Ex. C at ¶¶ 79-82. **VLSI Design describes:** "Voltage-scaling uses series resistors connected between Vref and ground **to selectively obtain voltages between these limits**. . . . Each tap is connected to a switching tree whose switches are controlled by the bits of the digital word." Ex. E at 626-629.  *Id.* at Figure 8.2-14(a) (p. 628). It would have been obvious to a POSITA to implement the D/A conversion circuit 10 of Kitamura using the voltage-scaling DAC techniques of VLSI Design. Ex. C at ¶¶ 82-91. This would have been obvious because, among other reasons, it would use a known digital-to-analog conversion technique to achieve predictable results, specifically, the digital-to-analog conversion discussed in Kitamura. *Id.* at 82-83, 90.
[1e] comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage,	Kitamura discloses a comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage. "[T]he output voltage (V_O) of the read point 8 changes as shown in FIG. 3. Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write

	switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." Ex. D at ¶ [09]. "A non-volatile memory that includes . . . a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that converts an analog signal that has been read into a digital signal." *Id*. at ¶ [01]. "[A] D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; **a circuit that compares a read level from a memory cell to the level of the analog signal**, and ends a write operation according to this result . . . ." *Id*. at ¶ [06] (emphasis added). "The present invention will now be described through reference to the drawings. FIG. 1 is a circuit diagram of a working example of the present invention. 1 is a memory cell constituted by a floating gate MOS transistor, 2 is a MOS transistor, 3 is a load circuit that switches between a write-use high voltage power supply (V_{PP}) and a read-use low voltage power supply (V_{DD}), 4 and 5 are driver circuits that output a high voltage during writing and a low voltage during reading by switching the power supply between V_{PP} and V_{DD}, 6 and 7 are address decoders, **8 is a read point from the memory cell 1**, **9 is a comparator** . . . ." *Id.* at ¶ [07] (emphasis added). "As described above, with the present invention, **writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion**, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). *See id.* at Figs. 1 and 3; Ex. C at ¶¶ 75-80.
[1f] said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding	Kitamura discloses that said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information. "Since the floating gate MOS transistor 1 and the MOS transistor 2 constitute a ratio circuit with the load circuit 3, when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3. Meanwhile, the two-bit input

to said input information.	digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." Ex. D at ¶ [09]. "A non-volatile memory that includes . . . a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that converts an analog signal that has been read into a digital signal." *Id*. at ¶ [01]. "[A] D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, **and ends a write operation according to this result** . . . ." *Id*. at ¶ [06] (emphasis added). "The present invention will now be described through reference to the drawings. FIG. 1 is a circuit diagram of a working example of the present invention. 1 is a memory cell constituted by a floating gate MOS transistor, 2 is a MOS transistor, 3 is a load circuit that switches between a write-use high voltage power supply (V_{PP}) and a read-use low voltage power supply (V_{DD}), 4 and 5 are driver circuits that output a high voltage during writing and a low voltage during reading by switching the power supply between V_{PP} and V_{DD}, 6 and 7 are address decoders, **8 is a read point from the memory cell 1**, **9 is a comparator**, 10 is a two-bit D/A conversion circuit, 11 is a read/write switching signal generation circuit, 12 is a read/write switching terminal, and 13 is a two-bit A/D conversion circuit." *Id.* at ¶ [07] (emphasis added). "As described above, with the present invention, **writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion**, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). *See id.* at Figs. 1 and 3; Ex. C at ¶¶ 77-78.

Kitamura in view of VLSI Design also renders obvious claims 9, 12, 30, 42 and 45 of the '571 patent, as shown in Chart II below, which includes citations to Kitamura and VLSI Design for claims 9, 12, 30, 42 and 45 of the '571 patent. References to claim element citations for Kitamura and VLSI Design are provided as references to Chart I above.

CLAIM CHART II	
'571 Patent	**Kitamura & VLSI Design**
[9a] Multi-level memory apparatus, comprising:	Kitamura discloses a multi-level memory apparatus. Kitamura: *See* Chart I, element 1a.
[9b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b.
[9c] a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and VLSI Design render obvious a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. VLSI Design: *See* Chart I, element 1d.
[9d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c. Kitamura's device includes a load circuit 3 that applies a "write-use high voltage power supply (V_{PP})" signal to the bit line of the memory cell 1 to write data to the memory cell 1. Ex. D at ¶ [07]; *see also id.* ¶ [08] ("The switching circuit 3 supplies V_{PP} during the write period. . . ."). The driver circuit 4 also enables programming when it "output[s] a high voltage" to the control gate of the memory cell 1 during writing. *Id.* The load circuit 3 and driver circuit 4 each apply their signals to the memory cell 1 according to the signals from the read/write switching signal generation circuit. *Id.* *See also* Ex. C at ¶¶ 74-79, 93-100.
[9e] a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal	Kitamura discloses a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.

to verify whether said memory cell is programmed to the state indicated by said information.	Kitamura: *See* Chart I, element 1e.
[12a] Multi-level memory apparatus, comprising:	Kitamura discloses a multi-level memory apparatus. Kitamura: *See* Chart I, element 1a.
[12b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b.
[12c] a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and VLSI Design render obvious a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. VLSI Design: *See* Chart I, element 1d.
[12d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.
[12e] a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.	Kitamura discloses a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f.
[30a] Apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:	Kitamura discloses an apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b.
[30b] a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference	Kitamura and VLSI Design render obvious a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell.

signal corresponding to a different memory state of said memory cell;	Kitamura: *See* Chart I, element 1d. VLSI Design: *See* Chart I, element 1d.
[30c] a programming signal source to apply a programming signal to said memory cell; and	Kitamura discloses a programming signal source to apply a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.
[30d] a control device to control the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura discloses a control device to control the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f.
[42a] A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	Kitamura discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b and corresponding described methods.
[42b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and VLSI Design render obvious selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. VLSI Design: *See* Chart I, element 1d and corresponding described method.
[42c] applying a programming signal to said memory cell;	Kitamura discloses applying a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c and corresponding described method.
[42d] detecting a parameter indicating the state of said memory cell; and	Kitamura discloses detecting a parameter indicating the state of said memory cell. Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods.
[42e] verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.	Kitamura discloses verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods.

[45a] A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	Kitamura discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b and 1c and corresponding described methods.
[45b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and VLSI Design render obvious selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. VLSI Design: *See* Chart I, element 1d and corresponding described method.
[45c] applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura discloses applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1c, 1e and 1f and corresponding described methods.

C. SNQ #2: Claims 1, 9, 12, 30, 42, and 45 are Obvious over Kitamura in view of Connolly

The combination of Kitamura and Connolly renders obvious each of claims 1, 9, 12, 30, 42, and 45 of the '571 patent. The following description and claim charts demonstrate in detail the correspondence between the elements in claims 1, 9, 12, 30, 42, and 45 and the combination of Kitamura and Connolly.

Kitamura discloses features of claims 1, 9, 12, 30, 42, and 45 as discussed in Section IX.B. This includes an electrically alterable non-volatile memory cell (e.g., memory cell 1), memory cell programming means (e.g., read/write switching signal generation circuit 11), comparator means (e.g., comparator 9), and others. *See* Ex. D at ¶¶ [08]-[09]; Section IX.B *supra*.

Kitamura also discloses a D/A conversion circuit 10 that converts a 2-bit digital input to one of four predetermined reference voltages corresponding to different memory states. Ex. C at

¶¶ 79-82, 106. The D/A conversion circuit 10 is similar to the "reference voltage selection means" or "selecting device" of the '571 patent claims. However, as noted above, Kitamura does not explicitly mention that the D/A conversion circuit 10 performs digital-to-analog conversion by *selecting* the reference voltage to output. *Id.* at ¶ 82. Nevertheless, it would have been obvious for the D/A conversion circuit 10 of Kitamura to perform this selection in view of Connolly. *Id.* at ¶¶ 107-122.

1. Reference Voltage Selecting Means (claim 1) / Selecting Device (claims 9, 12, 30) / Selecting One of a Plurality of Reference Signals (claims 42, 45)[17]

Kitamura does not disclose the specific structure of the D/A conversion circuit 10, and so a POSITA would naturally have looked to other teachings to implement the 2-bit DAC functionality. Ex. C at ¶ 107. Connolly shows simple circuit techniques that a POSITA could use to carry out digital-to-analog conversion in Kitamura's D/A conversion circuit 10. *Id.* at ¶¶ 108-111.

Connolly describes a double digital-to-analog converter, which includes two DACs that can be used together to form a larger DAC. Ex. F at Abstract. "Each converter includes a resistor ladder and switching tree that permits coupling the output to any single tap on the ladder." *Id.* The various taps provide different voltages, and the switching tree selects the analog voltage that corresponds to the digital input. *Id.* at Abstract, 3:16-4:18; Ex. C at ¶¶ 108-111.

Connolly illustrates a device that includes two 2-bit DACs. Ex. F at 3:16-36. This device is shown in Figs. 4 and 4A below.

[17] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

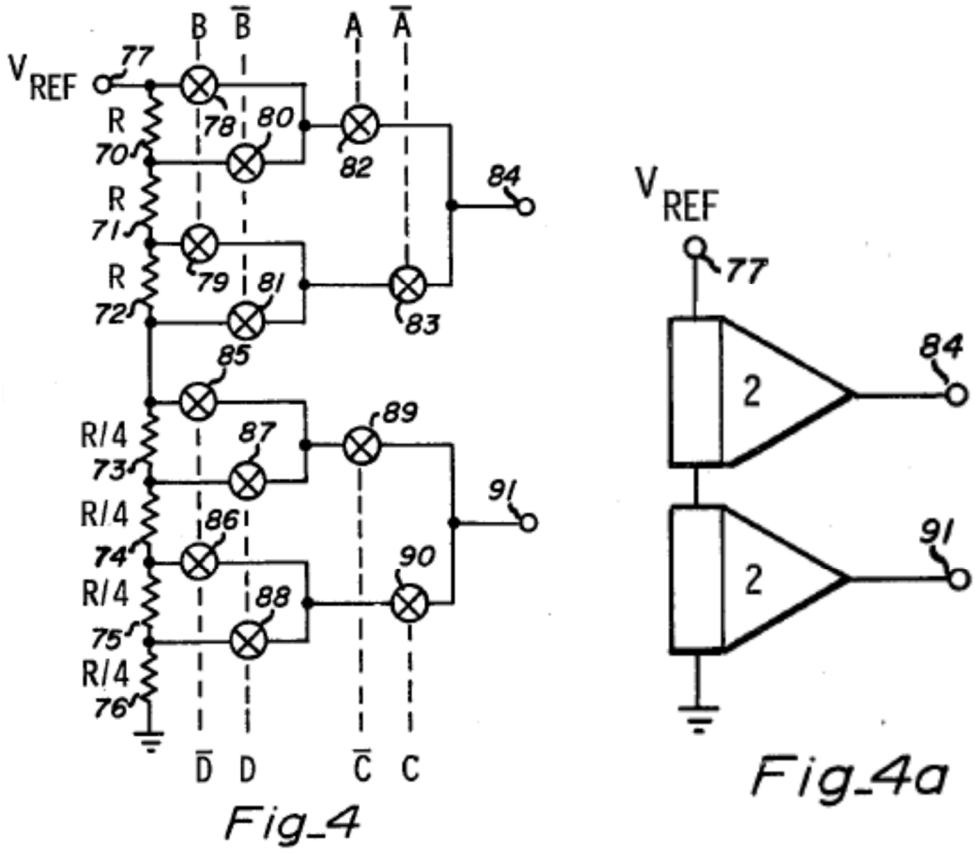


Fig. 4 and Fig. 4a of Connolly (Ex. F)

In Connolly's circuit, the upper DAC converts two bits (AB) and provides the analog output at terminal 84. *Id.* at 3:17-22. To perform the conversion, "[t]he upper portion employs resistors 70-72 which comprise a resistor ladder for a 2-bit DAC which uses switches 78-83 in a switching tree configuration to terminal 84." *Id.* The switches 78-83 operate according to the digital input to select the voltage at one of the taps of the resistor ladder to serve as the analog output. *Id.* at 3:27-28; Ex. C at ¶¶ 108-111.

Although Connolly describes using two DACs together, a POSITA would have understood that a single DAC could be used on its own. Ex. C at ¶ 111. Indeed, Connolly shows that the voltage at terminal 84, the output of the upper 2-bit DAC, is determined by bits A and B. Ex. C at ¶ 110. Thus, a POSITA would have found Connolly to teach a simple, obvious technique for implementing Kitamura's 2-bit D/A conversion circuit 10. Ex. C at ¶ 111. While a POSITA would not need to use Connolly's exact circuit configuration, it would have been obvious to use Kitamura's "two-bit input digital signals B_0 and B_1" to define input bits A and B

for Connolly's circuit, and to use the output at terminal 84 as the output of Kitamura's D/A conversion circuit 10. Ex. C at ¶¶ 111-116.

A POSITA would have had several reasons to use Connolly's techniques to implement Kitamura's D/A conversion circuit 10. Using a "resistor ladder and associated switching tree" (Ex. F at 1:14-15), as Connolly teaches, was a well-known technique that would function in Kitamura's device in the same predictable manner disclosed in Connolly. Ex. C at ¶ 118. Even Connolly describes this general DAC architecture as being a known, prior art technique as of its filing date in 1978, more than a decade before the earliest priority date of the '571 patent. *Id.* In addition, Connolly's circuit provides the exact 2-bit digital-to-analog conversion functionality needed by Kitamura, and so can be simply substituted for the D/A conversion circuit 10. *Id.* at ¶ 117. A POSITA would have been motivated to use Connolly's DAC techniques because they use very simple, widely available components (e.g., resistors and switches), and use a very small number of parts overall (e.g., only about 5 resistors and 6 switches). *Id.* at ¶ 119. The simplicity of the design provides a DAC the can be manufactured in a small circuit area and with low cost, which would further motivate a POSITA to use Connolly's technique. *Id.* at ¶ 119. Thus, using Connolly's D/A conversion techniques in Kitamura's D/A conversion circuit 10 would use a known D/A conversion technique to yield predictable results. *Id.* at ¶¶ 118-119.

In the combination of Kitamura in view of Connolly, the D/A conversion circuit 10 of Kitamura would be equivalent to, or at least render obvious, the "reference voltage selecting means" and "selecting device" as recited in the claims of '571 patent. Ex. C at ¶¶ 120-121. The resistor ladder would be set to provide, at the taps of the resistor ladder, the four reference voltages that correspond to the different memory states of Kitamura. *Id.* at ¶¶ 111-116. The 2-bit input of B_0 and B_1 of Kitamura would set the values that control a switching tree (e.g., values A, $\overline{A}$, B, and $\overline{B}$ of Connolly), and in response the switching tree would select the appropriate reference voltage by connecting the correct tap to the output terminal. *Id.*

In this manner, Kitamura in view of Connolly render obvious the function and corresponding structure for the "reference voltage selection means" (claim 1). Ex. C at ¶¶ 108-122. As discussed above in Section IX.A.1(a), the corresponding function for this term is "selecting one of a plurality of reference voltages in accordance with the input information." Kitamura's D/A conversion circuit 10, implemented using the DAC techniques of Connolly, performs this function by selecting one of the predetermined reference voltages along the

"resistor ladder" by operation of the "associated switching tree." *Id.* at ¶¶ 111-114; Ex. F at 1:14-15. The D/A conversion circuit 10 also makes the selection according to input information (e.g., Kitamura's digital signals B_0 and B_1) representing the information to be stored in a memory cell. *Id.* The corresponding structure for the "reference voltage selecting means" includes at least the "verify reference select circuit 222." Kitamura's D/A conversion circuit 10, implemented using Connolly's DAC techniques, is equivalent to the "verify reference select circuit 222" by performing the same function, in substantially the same way to achieve substantially the same result. Ex. C at ¶ 121. Both select and output the analog reference voltage encoded by a 2-bit digital input signal. Ex. A at 11:54-57, 9:11-14; Ex. D at ¶ [09]; Ex. C at ¶ 121. Both also provide the selected analog output voltage to a comparator. Ex. A. at Fig. 8, 8:26-29; Ex. D at Fig. 1.

Kitamura in view of Connolly render obvious the function and corresponding structure for the "selecting device" (claims 9, 12, 30). The corresponding function is "selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed." The corresponding structure for the "selecting device" includes at least the "verify reference select circuit 222." Kitamura's D/A conversion circuit 10, implemented using the DAC techniques of Connolly, is equivalent to the "verify reference select circuit 222" as discussed above. Ex. C at ¶ 121. The output voltage selected by the D/A conversion circuit 10 is the voltage that corresponds to "the two-bit input digital signals **B_0 and B_1 to be written**," where these input signals clearly specify the memory state to be programmed. Ex. D at ¶ [09] (emphasis added); *see also id.* at ¶ [14] (programming continues "until the output voltage . . . coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion).

Thus, the D/A conversion circuit 10 of Kitamura in view of Connolly has a structure that is at least equivalent to the corresponding structure of "reference voltage selection means" (claim 1) and "selecting device" (claims 9, 12, 30) of the '571 patent. The D/A conversion circuit 10 performs the same function as the "verify reference select circuit 222," in substantially the same way to achieve substantially the same result. Ex. C at ¶ 121; *see* MPEP 2183. There are also no substantial differences between the D/A conversion circuit 10 of Kitamura in view of VLSI Design and the "verify reference select circuit 222" that serves as corresponding structure under § 112, ¶ 6, showing equivalence under the "insubstantial differences" test. *Id.*

Thus, Kitamura's D/A conversion circuit 10, implemented as a 2-bit DAC operating in the manner disclosed in Connolly, would meet the requirements of a "reference voltage selecting means" (claim 1) and a "selecting device" (claims 9, 12, and 30). The D/A conversion circuit 10 would perform the functions of "selecting one of a plurality of reference voltages in accordance with said input information" (claim 1), and "select[ing] one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" (claims 9, 12, 30, 42, and 45).

The evidence and testimony included in Appendix A further support the requester's positions with respect to obviousness of these "selecting" elements.

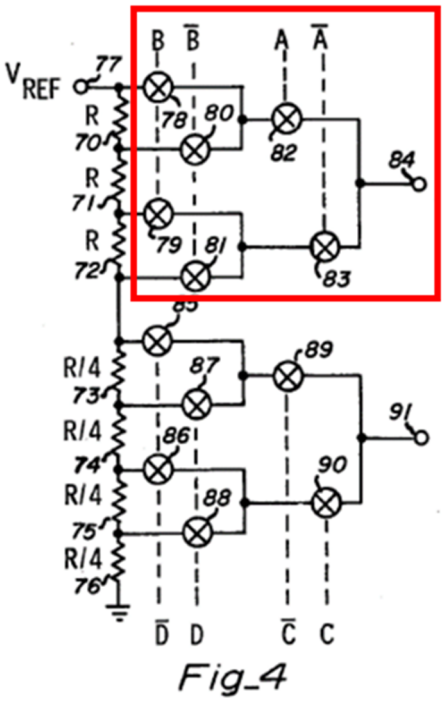
2. Example Comparison of Kitamura and Connolly with the '571 Patent

Kitamura discloses features of the '571 patent as shown above in the color-coded Table 2 and color-coded figures of Section IX.B.5, and as described throughout Section IX.B.

As explained in greater detail in the following Claim Chart III, the features of the Challenged Claims of the '571 patent are rendered obvious by Kitamura and Connolly, and thus, unpatentable under 35 U.S.C. § 103. *See* Ex. C at ¶¶ 66, 107, 123.

CLAIM CHART III	
'571 Patent	**Kitamura and Connolly**
[1a] A multi-level memory device comprising:	Kitamura discloses a multi-level memory device. Kitamura: *See* Chart I, element 1a.
[1b] an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits	Kitamura discloses an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$. Kitamura: *See* Chart I, element 1b.

stored per cell, and $K^n > 2$;	
[1c] memory cell programming means for programming said multi-level memory cell in accordance with said input information;	Kitamura discloses a memory cell programming means for programming said multi-level memory cell in accordance with said input information. Kitamura: *See* Chart I, element 1c.
[1d] reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and	Kitamura and Connolly render obvious a reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states. Kitamura: *See* Chart I, element 1d. The D/A conversion circuit 10 of Kitamura outputs a reference voltage in accordance with digital input B_0 and B_1. Ex. D at ¶ [10]. The reference voltage from the D/A conversion circuit 10 is one of four different reference voltages that each correspond to a different memory state of the memory cell, e.g., the memory states respectively representing stored data "1,1", "1,0", "0,1", and "0,0." *Id.*; Ex. C at ¶¶ 79-82. Connolly discloses: "Two digital-to-analog converters are coupled in series across a reference potential source. **Each converter includes a resistor ladder and switching tree that permits coupling the output to any single tap on the ladder.**" Ex. F at Abstract. "**The upper portion employs resistors 70-72 which comprise a resistor ladder for a 2-bit DAC which uses switches 78-83 in a switching tree configuration to terminal 84**." *Id.* at 3:19-22. Connolly discloses digital-to-analog conversion techniques that select a voltage from a set of voltages present at the taps of a resistor ladder. *Id.* at Abstract. Based on Connolly, it would have been obvious for Kitamura's D/A conversion circuit 10 to likewise use a switching tree to select from among reference voltages along a resistor ladder. Ex. C at ¶¶ 108-118. Using Connolly's technique for digital-to-analog conversion, Kitamura's D/A conversion circuit 10 would be equivalent to the claimed "reference voltage selecting means" by using an equivalent structure for "selecting" the reference voltage from among reference voltages for the four memory states of Kitamura's memory cell. *Id.* at ¶¶ 120-122.

	 Fig_4 Ex. F at Fig. 4 (annotated to show a "switching tree" operable to select a voltage for a 2-bit DAC). *See* Ex. C at ¶¶ 106-123.
[1e] comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage,	Kitamura discloses a comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage. Kitamura: *See* Chart I, element 1e.
[1f] said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.	Kitamura discloses that said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information. Kitamura: *See* Chart I, element 1f.

Kitamura in view of Connolly also renders obvious claims 9, 12, 30, 42 and 45 of the '571 patent, as shown in Claim Chart IV below, which includes citations to Kitamura and

Connolly for claims 9, 12, 30, 42 and 45 of the '571 patent. References to claim element citations for Kitamura are provided as references to Chart I in Section IX.B.5 above. References to claim element citations for Connolly are provided as references to Chart III above.

CLAIM CHART IV	
'571 Patent	**Kitamura and Connolly**
[9a] Multi-level memory apparatus, comprising:	Kitamura discloses a multi-level memory apparatus. Kitamura: *See* Chart I, element 1a.
[9b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b.
[9c] a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Connolly render obvious a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Connolly: *See* Chart III, element 1d.
[9d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.
[9e] a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.	Kitamura discloses a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information. Kitamura: *See* Chart I, element 1e.
[12a] Multi-level memory apparatus, comprising:	Kitamura discloses a multi-level memory apparatus. Kitamura: *See* Chart I, element 1a.
[12b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b.
[12c] a selecting device which selects one of a plurality of	Kitamura and Connolly render obvious a selecting device which selects one of a plurality of reference signals in

reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Connolly: *See* Chart III, element 1d.
[12d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.
[12e] a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.	Kitamura discloses a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f.
[30a] Apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:	Kitamura discloses an apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b.
[30b] a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Connolly render obvious a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Connolly: *See* Chart III, element 1d.
[30c] a programming signal source to apply a programming signal to said memory cell; and	Kitamura discloses a programming signal source to apply a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.
[30d] a control device to control the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura discloses a control device to control the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f.

[42a] A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	Kitamura discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b and corresponding described methods.
[42b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Connolly render obvious selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. Connolly: *See* Chart III, element 1d.
[42c] applying a programming signal to said memory cell;	Kitamura discloses applying a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c and corresponding described method.
[42d] detecting a parameter indicating the state of said memory cell; and	Kitamura discloses detecting a parameter indicating the state of said memory cell. Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods.
[42e] verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.	Kitamura discloses verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods.
[45a] A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	Kitamura discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b and 1c and corresponding described methods.
[45b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Connolly render obvious selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. Connolly: *See* Chart III, element 1d.

[45c] applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura discloses applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1c, 1e and 1f and corresponding described methods.

D. SNQ #3: Claims 1, 9, 12, 30, 42, and 45 are Obvious over Kitamura in view of Oshita

The combination of Kitamura and Oshita renders obvious each of claims 1, 9, 12, 30, 42, and 45 of the '571 patent. The following description and claim charts demonstrate in detail the correspondence between the elements in claims 1, 9, 12, 30, 42, and 45 and the combination of Kitamura and Oshita.

Kitamura discloses features of claims 1, 9, 12, 30, 42, and 45 as discussed in Section IX.B. This includes an electrically alterable non-volatile memory cell (e.g., memory cell 1), memory cell programming means (e.g., read/write switching signal generation circuit 11), comparator means (e.g., comparator 9), and others. *See* Ex. D at ¶¶ [08]-[09]; Section IX.B *supra*.

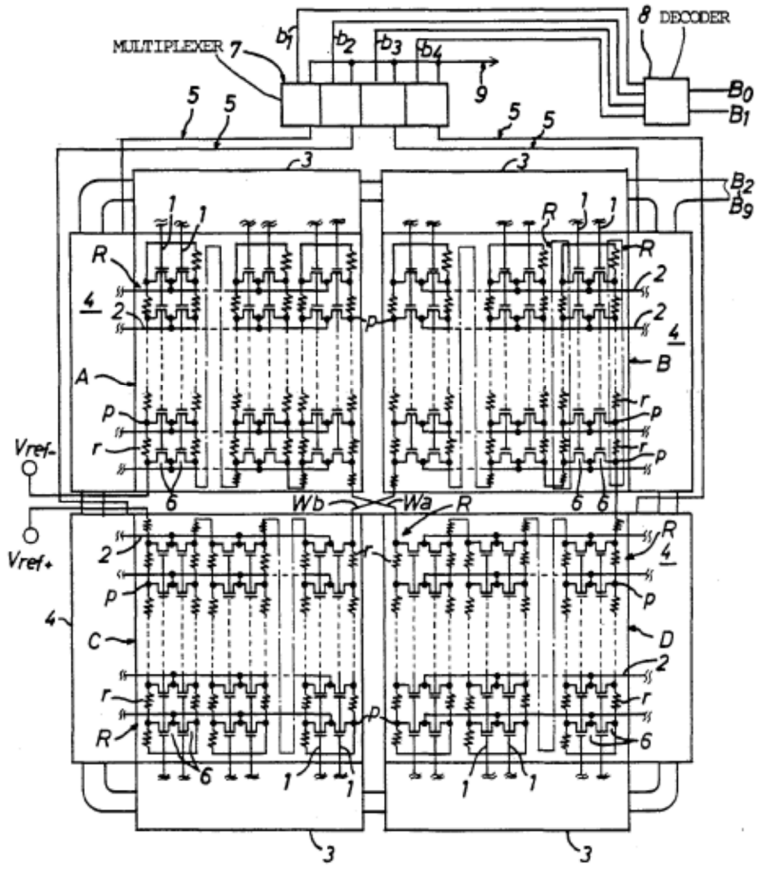
Kitamura also discloses a D/A conversion circuit 10 that converts a 2-bit digital input to one of four predetermined reference voltages corresponding to different memory states. Ex. C at ¶¶ 79-82, 124. The D/A conversion circuit 10 is similar to the "reference voltage selection means" or "selecting device" of the '571 patent claims. However, as noted above, Kitamura does not explicitly mention that the D/A conversion circuit 10 performs digital-to-analog conversion by *selecting* the reference voltage to output. *Id.* at ¶¶ 82, 124. Nevertheless, it would have been obvious for the D/A conversion circuit 10 of Kitamura to perform this selection in view of Oshita. *Id.* at ¶¶ 125-133.

1. Reference Voltage Selecting Means (claim 1) / Selecting Device (claims 9, 12, 30) / Selecting One of a Plurality of Reference Signals (claims 42, 45)[18]

Kitamura does not disclose the structure of the D/A conversion circuit 10, and so a POSITA would naturally have looked to other teachings to implement the 2-bit DAC functionality. Ex. C at ¶ 125. Oshita shows circuit techniques that a POSITA could use to carry out digital-to-analog conversion in Kitamura's D/A conversion circuit 10. *Id.* at ¶¶ 126-129.

Oshita describes a "digital-to-analog converter of the resistor string type" having "a string of resistors for dividing a reference voltage into a series of divided voltages, and a switch matrix circuit for selectively generating the divided voltages as an analog signal when activated in response to a digital signal." Ex. G at Abstract. Oshita's DAC produces several divided voltages with the resistor string, and other components of the DAC select one of these voltages to be provided as an analog output of the DAC. Ex. C at ¶¶ 126-127. Fig. 1 of Oshita, reproduced to the right, shows an example of a 10-bit DAC.

Fig. 1



[18] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

Oshita's 10-bit DAC includes a resistor string divided into four sections or arrays, marked A, B, C, and D in Fig. 1. Ex. G at 3:57-67. The eight least significant bits of a digital input (e.g., B_2 to B_9) are used to select a voltage signal from each array, so that each array provides a signal to a multiplexer 7 on an output line 5. *Id.* at 5:31-54. The circuit then uses the two most significant bits (e.g., B_0 and B_1) to control the multiplexer 7 and select which of the four signals from the resistor string to provide as the output of the DAC. *Id.*; Ex. C at ¶ 127.

Kitamura's D/A conversion circuit 10 outputs one of four different analog voltages based on Kitamura's signals B_0, B_1. Ex. C at ¶ 129. A POSITA would have recognized that the Oshita's decoder 8 and multiplexer 7 perform this same function, by selecting from among four voltages (e.g., those on output lines 5) based on Oshita's 2-bit digital input B_0, B_1. *Id*. Thus, it would have been obvious to implement Kitamura's D/A converter 10 using a decoder and multiplexer to select from four voltages from a resistor string, as taught by Oshita. *Id.* This arrangement would provide Kitamura's digital input signal B_0, B_1 to the decoder 8 of Oshita, which would communicate with the multiplexer 7 to select one of the four voltages on the output lines 5 in the same manner Oshita teaches. *Id*. The resistor string would be arranged to provide the four voltages that represent the respective memory states of Kitamura's memory cell. *Id*.

A POSITA would have been motivated to use the techniques of Oshita to implement the D/A conversion circuit 10 because Oshita provides the 2-bit digital-to-analog conversion needed in Kitamura's system. *Id*. at ¶ 130. The technique of using a decoder and multiplexer to select from among four voltages on a resistor string would function in Kitamura's device in the same manner that these components operate in Oshita, producing predictable results that match those of the D/A conversion circuit 10. Ex. G at 1:14-15; Ex. C at ¶ 130. A POSITA would also have been motivated to use a decoder and multiplexer as a DAC, as taught by Oshita, because the technique improves the speed of the converter through low settling times. Ex. G at 6:60-7:17. Additionally, the decoder and multiplexer provide a great degree of flexibility to the circuit designer in assigning the analog voltages to the digital inputs. Ex. C at ¶¶ 128-132. Indeed, a POSITA can use the decoder to assign any combination of digital inputs to any of the four analog voltages provided to the multiplexer. *Id*.

With a D/A conversion circuit 10 implemented using the principles taught by Oshita, the system of Kitamura would perform the features of "selecting one of a plurality of reference voltages in accordance with said input information" as recited in claim 1 of the '571 patent. The

divided voltages on the resistor string would provide the four voltages that correspond to the different memory states of Kitamura. Ex. C at ¶ 132. The 2-bit input of B_0 and B_1 of Kitamura would select one of the four voltages to output, because they set the decoder output that controls the selection made by the multiplexer 7. *Id*.

In this manner, Kitamura in view of Oshita render obvious the function and corresponding structure for the "reference voltage selection means" (claim 1). As discussed above in Section IX.A.1(a), the corresponding function for this term is "selecting one of a plurality of reference voltages in accordance with the input information." Kitamura's D/A conversion circuit 10, implemented using the DAC techniques of Oshita, performs this function by selecting one of the predetermined reference voltages along the "resistor string" by operation of the multiplexer or other switch matrix circuit. Ex. C at ¶¶ 130-132; Ex. G at Abstract, 5:31-541:14-15. The D/A conversion circuit 10 makes the selection according to the input information (e.g., Kitamura's digital signals B_0 and B_1) representing the information to be stored in a memory cell. *Id*. The corresponding structure for the "reference voltage selecting means" includes at least the "verify reference select circuit 222." Kitamura's D/A conversion circuit 10, implemented using Oshita's DAC techniques, is equivalent to the "verify reference select circuit 222." Both select and output the analog reference voltage encoded by a 2-bit digital input signal. Ex. A at 11:54-57, 9:11-14; Ex. D at ¶ [09]; Ex. C at ¶¶ 130-132. Both also provide the selected analog output voltage to a comparator. Ex. A. at Fig. 8; Ex. D at Fig. 1.

Kitamura in view of Oshita render obvious the function and corresponding structure for the "selecting device" (claims 9, 12, 30). The corresponding function is "selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed." The corresponding structure for the "selecting device" includes at least the "verify reference select circuit 222." Ex. C at ¶ 132. Kitamura's D/A conversion circuit 10, implemented using the DAC techniques of Oshita, is equivalent to the "verify reference select circuit 222" as discussed above. *Id*. The output voltage selected by the D/A conversion circuit 10 is the voltage that corresponds to "the two-bit input digital signals B_0 and B_1 to be written," where these input signals clearly specify the memory state to be programmed. Ex. D at ¶ [09] (emphasis added); *see also id.* at ¶ [14] (programming continues "until the output voltage . . . coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion).

Thus, the D/A conversion circuit 10 of Kitamura in view of Oshita has a structure that is at least equivalent to the corresponding structure of "reference voltage selection means" (claim 1) and "selecting device" (claims 9, 12, 30) of the '571 patent. The D/A conversion circuit 10 performs the same function as the "verify reference select circuit 222," in substantially the same way to achieve substantially the same result. *See* MPEP 2183. There are also no substantial differences between the D/A conversion circuit 10 of Kitamura in view of VLSI Design compared to the "verify reference select circuit 222" that serves as corresponding structure under § 112, ¶ 6, showing equivalence under the "insubstantial differences" test. *Id.*

Thus, Kitamura's D/A conversion circuit 10, implemented as a 2-bit DAC using a decoder and multiplexer as Oshita discloses for its most significant bits B_0 and B_1, would meet the requirements of a "reference voltage selecting means" (claim 1) and a "selecting device" (claims 9, 12, and 30). The D/A conversion circuit 10 would also perform the functions of "selecting one of a plurality of reference voltages in accordance with said input information" (claim 1), and "select[ing] one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" (claims 9, 12, 30, 42, and 45).

The evidence and testimony included in Appendix A further support the requester's positions with respect to obviousness of these "selecting" elements.

2. Example Comparison of Kitamura and Oshita with the '571 Patent

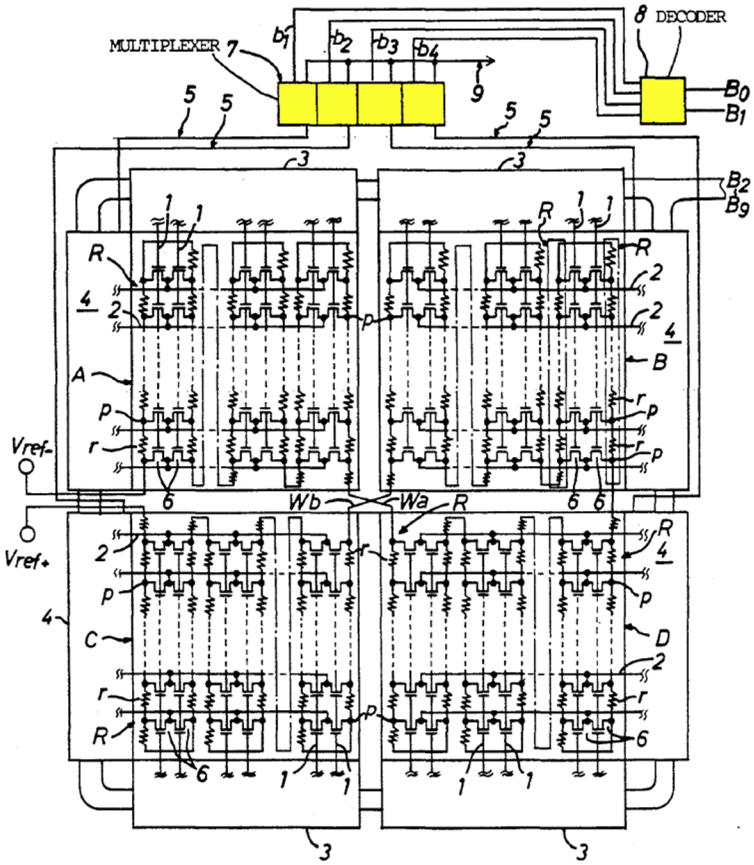
Kitamura discloses features of the '571 patent as shown above in the color-coded Table 2 and color-coded figures of Section IX.B.5, and as described throughout Section IX.B.

As explained in greater detail in the following Claim Chart V, the features of the Challenged Claims of the '571 patent are rendered obvious by Kitamura in view of Oshita, and thus, unpatentable under 35 U.S.C. § 103. *See* Ex. C at ¶¶ 124-133.

CLAIM CHART V	
'571 Patent	**Kitamura and Oshita**
[1a] A multi-level memory device comprising:	Kitamura discloses a multi-level memory device. Kitamura: *See* Chart I, element 1a.
[1b] an electrically alterable non-volatile multi-level	Kitamura discloses an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K

memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;	is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$. Kitamura: *See* Chart I, element 1b.
[1c] memory cell programming means for programming said multi-level memory cell in accordance with said input information;	Kitamura discloses a memory cell programming means for programming said multi-level memory cell in accordance with said input information. Kitamura: *See* Chart I, element 1c.
[1d] reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and	Kitamura and Oshita render obvious a reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states. **Kitamura:** *See* Chart I, element 1d. The D/A conversion circuit 10 of Kitamura outputs a reference voltage in accordance with digital input B_0 and B_1. Ex. D at ¶ [10]. The reference voltage from the D/A conversion circuit 10 is one of four different reference voltages that each correspond to a different memory state of the memory cell, e.g., the memory states respectively representing stored data "1,1", "1,0", "0,1", and "0,0." *Id.*; Ex. C at ¶¶ 78-80. **Oshita discloses:** "A digital-to-analog converter of the resistor string type comprises **a string of resistors for dividing a reference voltage into a series of divided voltages**, and a **switch matrix circuit for selectively generating the divided voltages as an analog signal when activated in response to a digital signal**. . . . Furthermore, **a selector is responsive to the digital signal for selecting one of the respective one divided voltages** from the four decoder circuits . . . to generate the selected one divided voltage as the analog signal." Ex. G at Abstract. Oshita discloses digital-to-analog conversion techniques that select a voltage to output, from a set of divided voltages along a string of resistors. *Id.* at Abstract. Based on Oshita, it would have been obvious

	for Kitamura's D/A conversion circuit 10 to likewise select a reference voltage for output from among reference voltages generated as divided voltages along a string of resistors. Using Oshita's technique for digital-to-analog conversion, Kitamura's D/A conversion circuit 10 would be a "reference voltage selecting means" performing the function of "selecting" a reference voltage from among reference voltages for the four memory states of Kitamura's memory cell. Oshita further discloses: ". . . said switch matrix circuit means includes . . . **selection means responsive to the digital signal for selecting one of the respective divided voltages** . . . ." *Id.* at 3:1-5. ". . . the **multiplexer 7 cooperates with the decoder 8 responsive to signals appearing on the input lines B_0, B_1** to permit electrical connection between the external line 9 and the output line 5 of line decoder 4 for one of the square arrays A, B, C and D. **This means that the multiplexer 7 cooperates with decoder 8 to select one of the square arrays A to D on a basis of the signals appearing on the input lines B_0, B_1.**" *Id.* at 5:46-54. "In this instance, the multiplexer 7 selects one of the square arrays A to D on a basis of signals appearing on the input lines B_0, B_1. **In selective operation of multiplexer 7, a divided voltage indicative of zero(V) is produced from one of the common terminals p, . . . , p in the square array A, a divided voltage indicative of V_{ref} /4 is produced from one of the common terminals p, . . . , p in the square array D, a divided voltage indicative of V_{ref} /2 is produced from one of the common terminals p, . . . , p in the square array B, or a divided voltage indicative of 3 V_{ref} /4 is produced from one of the common terminals p, . . . , p in the square array C**." *Id.* at 6:65 to 7:8.

	Fig. 1  *Id.* at Fig. 1 (annotated to highlight decoder 8 and multiplexer 7). Although Oshita describes a 10-bit DAC, a POSITA would have found it obvious to use Oshita's techniques to implement a 2-bit DAC. Ex. C at ¶ 128. In particular, the decoder 8 and multiplexer 7 cooperate to perform digital-to-analog conversion of the two most significant bits in Oshita's circuit. Ex. G at 5:46-54, 11:6-11; Ex. C at ¶¶ 128-129. For Kitamura's D/A conversion circuit 10, where only a 2-bit conversion is needed, it would have been obvious to use Oshita's decoder 8 and multiplexer 7 to select a voltage to outputs from four divided voltages, as Oshita discloses. Ex. C at ¶¶ 128-129. *See* Ex. C at ¶¶ 126-133.
[1e] comparator means for comparing a voltage of said multi-level memory cell with	Kitamura discloses a comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage. Kitamura: *See* Chart I, element 1e.

the selected reference voltage,	
[1f] said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.	Kitamura discloses that said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information. Kitamura: *See* Chart I, element 1f.

Kitamura and Oshita also render obvious claims 9, 12, 30, 42 and 45 of the '571 patent, as shown in Chart VI below, which includes citations to Kitamura and Oshita for claims 9, 12, 30, 42 and 45 of the '571 patent. References to claim element citations for Kitamura are provided as references to Chart I in Section IX.B.5 above. References to claim element citations for Oshita are provided as references to Chart V above.

CLAIM CHART VI	
'571 Patent	**Kitamura and Oshita**
[9a] Multi-level memory apparatus, comprising:	Kitamura discloses a multi-level memory apparatus. Kitamura: *See* Chart I, element 1a.
[9b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b.
[9c] a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Oshita render obvious a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Oshita: *See* Chart V, element 1d.
[9d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.

[9e] a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.	Kitamura discloses a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information. Kitamura: *See* Chart I, element 1e.
[12a] Multi-level memory apparatus, comprising:	Kitamura discloses a multi-level memory apparatus. Kitamura: *See* Chart I, element 1a.
[12b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b.
[12c] a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Oshita render obvious a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Oshita: *See* Chart V, element 1d.
[12d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.
[12e] a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.	Kitamura discloses a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f.
[30a] Apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:	Kitamura discloses an apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b.
[30b] a selecting device which selects one of a plurality of reference signals in accordance	Kitamura and Oshita render obvious a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to

with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Oshita: *See* Chart V, element 1d.
[30c] a programming signal source to apply a programming signal to said memory cell; and	Kitamura discloses a programming signal source to apply a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c; Chart II, element 9d.
[30d] a control device to control the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura discloses a control device to control the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f.
[42a] A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	Kitamura discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b and corresponding described methods.
[42b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Oshita render obvious selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. Oshita: *See* Chart V, element 1d and corresponding described method.
[42c] applying a programming signal to said memory cell;	Kitamura discloses applying a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c and corresponding described method.
[42d] detecting a parameter indicating the state of said memory cell; and	Kitamura discloses detecting a parameter indicating the state of said memory cell. Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods.
[42e] verifying whether said memory cell is programmed to the state indicated by said information based on the detected	Kitamura discloses verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.

parameter and the selected reference signal.	Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods.
[45a] A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	Kitamura discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b and 1c and corresponding described methods.
[45b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Oshita render obvious selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. Oshita: *See* Chart V, element 1d and corresponding described method.
[45c] applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura discloses applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1c, 1e and 1f and corresponding described methods.

E. SNQ #4: Claims 1, 9, 12, 30, 42, and 45 are Invalid for Obviousness-Type Double Patenting in view of the ’851 Patent

The ’851 patent provides a substantial new issue of patentability with respect to claims 1, 9, 12, 30, 42, and 45 of the ’571 patent, as the ’571 patent represents an improper extension of patent rights in the earlier-expired ’851 patent. Thus, these claims of the ’571 patent are invalid under the doctrine of obviousness-type double patenting (“OTDP”). The following description and claim charts demonstrate in detail the correspondence between the claims of the ’851 patent and the claims of the ’571 patent.

1. Overview of Invalidity for Obviousness-Type Double Patenting

While the patent laws and PTO regulations permit an inventor to pursue multiple patents stemming from an original application in certain circumstances, an inventor is not allowed to

extend her property rights beyond the expiration in accordance with statutory time limits on the patent monopoly of her patents that claim the same invention or obvious variants. Article I, Section 8 of the United States Constitution provides that patents grant to inventors a monopoly over a particular invention, but for a limited time only. Congress, through several successive statutes, set time limits on each patent grant. Once a patent expires, the public is entitled to use that invention without interference. Where an inventor attempts to extend her monopoly by filing additional patents covering minor variations of expired subject matter, any such patents whose term extends beyond the expiration of her patent directed to the same invention or obvious variants are invalid due to obviousness-type double patenting.

That is precisely the case at hand, where '571 patent inventor Jerry Banks pursued substantially the same subject matter in the now expired '851 patent. When the '851 patent expired, any further patent term remaining in the '571 patent became invalid as an improper extension of the statutory monopoly grant.

(a) Background Facts

Named inventor Jerry Banks[19] filed a patent application entitled an "Electrically Alterable Non-Volatile Memory with N-Bits per Memory Cell" on February 8, 1991, to which the '571 patent claims priority. Ex. A ('571 patent). The '571 patent issued on June 9, 1998. *Id.* When Banks filed the '571 patent application, the patent statute set the term of U.S. patents at 17 years from issuance. Thus, if the '571 patent remained valid for its full term, it would have expired on June 9, 2015.[20]

With the 1996 Uruguay Round Agreements Act ("URAA"), amendments to the patent statute changed the patent term to 20 years from the earliest effective priority date, instead of the prior fixed 17 years from issuance term. 35 U.S.C. § 154(a)(2). The now-expired '851 patent

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[19] On information and belief, the named inventor of the '571 patent and related patents legally changed his name from "Gerald Banks" to "Jerry Banks."

[20] Although the '571 patent has expired, MLC, in co-pending litigation, seeks past damages for the period before expiration, and thus the validity of the '571 patent remains at issue.

was filed in October 2007, and thus is subject to a patent term of twenty years from the earliest effective priority date. Ex. H ('851 patent). The '851 patent claimed priority to the '571 patent (filed on February 27, 1995) and thus expired on February 27, 2015. *Id.* There is therefore a gap of more than three months between the expiration of the '571 and '851 patents. Moreover, the '851 patent issued containing claims directed to alleged inventions that are fully encompassed by the '571 patent claims. Because the '571 patent claims cover the same subject matter as the '851 patent, the earlier-expiring '851 patent renders the '571 patent claims invalid. *Gilead v. Natco Pharma,* 753 F.3d 1208 (Fed. Cir. 2014); *Ex Parte Pfizer, Inc.*, 2010 WL 532133 (BPAI Feb. 12, 2010) (finding that a later-expiring patent with an earlier priority date (like the '571 patent here) was invalid based on OTDP in view of an earlier-expiring patent with a later priority date (like the '851 patent here))

When the '851 patent expired on February 27, 2015, the public was entitled to practice the full scope of its claims. The asserted '571 patent claims, however, fully encompass the invention claimed in the '851 patent and therefore improperly prevented the public from practicing the expired '851 patent claims.

To avoid invalidity, the PTO allows a patent owner to "disclaim" that portion of a patent term that extends beyond the expiration of patent claims that cover common subject matter. *See* 37 C.F.R. § 1.321(d). However, the patent owner here filed no such disclaimer. The patentee obtained an improper extension of exclusivity, and therefore the asserted '571 patent claims are invalid for obviousness-type double patenting.

(b) Legal Standards

The obviousness-type double patenting analysis consists of two steps. The first step is to determine the differences between the claims of the subject patent and the double patenting reference. *Abbvie Inc. v. Mathilda & Terence Kennedy Inst. of Rheumatology Trust*, 764 F.3d 1366, 1374 (Fed. Cir. 2014). The second step is to "determine[] whether those differences render the claims patentably distinct." *Id.* (quoting *Sun Pharm. Indus.*, 611 F.3d at 1385). Determining whether the claims are patentably distinct is "analogous to an obviousness analysis under 35 U.S.C. § 103." *Id.* at 1378 (quoting *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1361 (Fed. Cir. 2009)). Minor linguistic variations between the challenged and reference patents do not create a patentable distinction. *See Logic Devices, Inc. v. Apple Inc.*, No. C 13-

02943-WHA, 2014 WL 5305979, at *3 (N.D. Cal. Oct. 16, 2014). The limitations recited in a method claim can be disclosed by or rendered obvious in view of an apparatus claim. *In re Lonardo*, 119 F.3d 960, 968 (Fed. Cir. 1997) ("We do not agree that there is a patentable distinction between the method of using the device and the device itself. The claimed structure of the device suggests how it is to be used and that use thus would have been obvious."). Later-issued but earlier-expiring patents render invalid any claims to obvious variants contained in later-expiring patents filed by the same inventor. *See Gilead v. Natco Pharma*, 753 F.3d 1208, 1214 (Fed. Cir. 2014); *Abbvie*, 764 F.3d at 1374 ("We now make explicit what was implicit in *Gilead*: the doctrine of obviousness-type double patenting continues to apply where two patents that claim the same invention have different expiration dates."); *Ex Parte Pfizer, Inc.*, 2010 WL 532133 (BPAI Feb. 12, 2010). In *Pfizer*, the Board analyzed whether a later-expiring patent with an earlier priority date was invalid in light of an earlier-expiring patent with a later priority date—*i.e.*, the precise situation in this case. *Pfizer, Inc.*, 2010 WL 532133, at *25 (sustaining rejection of a claim of a patent filed on May 13, 1994 under obviousness-type double patenting over claims of patents filed on October 16, 1995). The Board found that the later-expiring pre-URAA patent (like the '571 patent here) would "extend the Appellant's right to exclude the public from practicing" the already-expired invention (like the '851 patent here). *Id*. at *21. This, the Board concluded, was "precisely what obviousness-type double patenting was intended to prevent." *Id*.

The MPEP also sets forth the doctrine behind double patenting and recognizes the Federal Circuit's holding in the *Gilead* decision as supporting this doctrine:

> The doctrine of double patenting seeks to prevent the unjustified extension of patent exclusivity beyond the term of a patent. The public policy behind this doctrine is that:
>
> > The public should . . . be able to act on the assumption that upon the expiration of the patent it will be free to use not only the invention claimed in the patent but also modifications or variants which would have been obvious to those of ordinary skill in the art at the time the invention was made, taking into account the skill in the art and prior art other than the invention claimed in the issued patent.
>
> *In re Zickendraht*, 319 F.2d 225, 232, 138 USPQ 22, 27 (CCPA 1963) (Rich, J., concurring). Double patenting results when the right to exclude granted by a first patent is unjustly extended by the grant of a later issued patent or patents. *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982). **Note that in *Gilead***

> ***Sciences, Inc. v. Natco Pharma Ltd.*, 753 F.3d 1208, 110 USPQ2d 1551 (Fed. Cir. 2014), the court found an earlier-expiring patent, which was issued after the later-expiring patent, may be used to invalidate the later-expiring patent.**

MPEP § 804 (emphasis added).

An obviousness-type double-patenting evaluation encompasses not only the language of the claims, but also the entire specification. Although this evaluation requires comparing the claims of the subject patent to the claims of the reference patent, *Pfizer, Inc. v. Teva Pharm.*, 518 F.3d 1353, 1363 n.8 (Fed. Cir. 2008); *In re Vogel*, 422 F.2d 438, 441-42 (C.C.P.A. 1970), the claim terms must be considered both in the context of surrounding claim language as well as the context of the entire patent, including the specification. *Sun Pharms.*, 611 F.2d at 1388 (citing *ICU Med., Inc. v. Alaris Med. Sys., Inc.*, 558 F.3d 1368, 1374 (Fed. Cir. 2009) ("*Phillips*, as well as the rest of our claim construction precedent, expounds that a 'POSITA in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the *entire patent, including the specification*.'")) (emphasis in original); *see also Gilead*, 753 F.3d at 1210 (noting that "[t]he written descriptions of the patents are very similar and, in substantial parts, identical").

Later-issued but earlier-expiring patents render invalid any claims to obvious variants contained in later-expiring patents filed by the same inventor because it is a "bedrock principle of our patent system that when a patent expires, the public is free to use not only the same invention claimed in the expired patent but also obvious or patentably indistinct modifications of that invention." *Id.* at 1214 (citing *In re Longi*, 759 F.2d at 892 (Fed. Cir. 1985) ("The public should . . . be able to act on the assumption that upon the *expiration* of [a] patent it will be free to use not only the invention claimed in the patent but also [any] modifications or variants [thereof] which would have been *obvious* to those of ordinary skill in the art at the time the invention was made.")) (emphasis in original). "The double patenting doctrine has always been implemented to effectively uphold that principle." *Id.* (citing *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1372 (Fed. Cir. 2005)). "And that [bedrock] principle is violated when a patent expires and the public is nevertheless barred from practicing obvious modifications of the invention claimed in that patent because the inventor holds another later-expiring patent with claims for obvious modifications of the invention." *Gilead*, 753 F.3d at 1214. This double-patenting principle similarly serves to invalidate broad claims in view of earlier-expiring narrow claims. *See, e.g.*, *Geneva Pharm., Inc. v. GlaxoSmithKline PLC*, 349 F.3d 1373, 1384 (Fed. Cir. 2003)

(invalidating claims based on obviousness-type double patenting, explaining "The '352 and '552 patents claim subject matter that encompasses a substantial part of the subject matter of the Crowley claim. The '352 and '552 claims are thus generic to a substantial part of the scope of the Crowley claim. This genus-species relationship makes the claims patentably indistinct, because the earlier species within the Crowley claim anticipates the later genus of the '352 and '552 claims."); *In re Emert,* 124 F.3d 1458, 1462 (Fed. Cir. 1997) (noting that "[t]he PTO insists that the claims stand in a genus ('887 application) and species ('624 patent) relationship" and affirming the Board's rejection based on obviousness-type double patenting because "[a]lthough [applicant] included some new subject matter that might have been patentable had it been separately claimed, the broad claims [applicant] sought in the '887 application would have been obvious in view of the prior art '624 patent."). The Federal Circuit deems the obviousness-type double-patenting doctrine an "important check on improper extension of patent rights through the use of divisional and continuation applications." *Boehringer Ingelheim Int'l GmBH v. Barr Labs.*, 592 F.3d 1340, 1346 (Fed. Cir. 2010).

(c) The '851 Patent

The '851 patent is entitled "Memory Apparatus Including Programmable Non-Volatile Multi-Bit Memory Cell, and Apparatus and Method for Demarcating Memory States of the Cell." It includes a single independent claim (claim 1), which—like the claims of the '571 patent—is directed to a multi-level non-volatile memory device having more than two predetermined memory states for performing certain methods and functions. *See, e.g.*, Ex. H ('851) at 19:39-20:4 (claiming, in part, ". . . a programming signal source *which applies a programming signal to said memory cell*" and "having more than two predetermined memory states" (multi-level)) (emphasis added).

Dependent claim 7 of the '851 patent, which incorporates all the elements of claims 1, 2, and 6, recites the same memory device components and functions as claimed in '571 patent claim 1: (1) multi-level memory cell, (2) memory cell programming means—*i.e.*, a "programming signal source" to program the memory cell; (3) reference parameter selecting means—*i.e.*, "control circuitry which . . . *selects* among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed"; (4) and comparator means—*i.e.*, "a comparator which compares said

parameter corresponding to the state of said memory cell with the selected reference parameter" and "stop[ping]" application of a programming signal "after said memory state reaches the memory state to which said memory cell is to be programmed." *Id.* at 19:40-20:30. Claim 7, through its incorporation of the elements of claim 1, further recites "read circuitry" which compares a parameter corresponding to the state of the memory cell with read reference parameters as part of reading the state of the memory cell. *Id.* at 19:54-58.

The inclusion of the additional "read circuitry" limitation in claim 7 of the '851 patent makes the claim narrower than the claims of the '571 patent. However, this does not save the claims of the '571 patent because a narrower claim invalidates a claim that encompasses the narrower claim. *See Eli Lilly & Co. v. Barr Labs., Inc.*, 251 F.3d 955, 971 (Fed. Cir. 2001) ("Our case law firmly establishes that a later genus claim limitation is anticipated by, and therefore not patentably distinct from, an earlier species claim."); *Logic Devices*, 2014 WL 5305979, at *3 (explaining that a broader claim which expired later was not patentably distinct from an earlier-expiring narrower claim). That is the situation here.

As demonstrated below, the memory device components and functions/methods claimed in the narrower '851 patent are directed to an embodiment claimed in '571 patent claims and thus are the same as, or at least render obvious, the memory device components and their attendant functions/methods recited by the asserted claims of the '571 patent. *See also* Ex. C at ¶ 134. The minor linguistic differences in the claims of the '571 patent do not make them sufficiently distinct from the claims in the '851 patent. The public was entitled to practice the claims of the '851 patent upon its expiration prior to the expiration of the '571 patent. Because MLC failed to terminally disclaim the improper extension of patent rights created by the '571 patent claims, the challenged '571 patent claims are invalid.

(d) Requester's Motion for Summary Judgment in the Co-Pending Litigation

In litigation pending before the U.S. District Court for the Northern District of California, *MLC Intellectual Property, LLC v. Micron Technology, Inc.*, Case No. 3:14-cv-03657-SI, Requester filed a Motion for Summary Judgment of Invalidity, asserting that the challenged claims of the '571 patent are invalid for obviousness-type double patenting in view of the '851 patent. The patent owner may raise this as a reason for the PTO to deny institution of the

requested *ex parte* reexamination. However, while the district court denied the motion for summary judgment, that ruling should have no effect on the PTO's review of, and decision on, the instant request for *ex parte* reexamination.

As an initial matter, the district court did not determine that the claims of the '571 patent are patentably distinct from the claims of the '851 patent. Rather, the district court merely held that, viewing the evidence in the light most favorable to the patent owner, Requester had not met its burden on summary judgment of showing the absence of a genuine issue of material fact. *See, e.g.*, Ex. AF (*MLC v. Micron*, Case No. 3:14-cv-03657-SI, Dkt. No. 128 at 15 (April 26, 2017) ("On the current record, the Court cannot hold that the asserted claims of the '571 patent are not patentably distinct and/or are obvious in view of the '851/'814 patents. The parties have submitted dueling expert reports which detail, at length, the experts' conflicting opinions about the inventions claimed in the '571 and '851/'814 patents and whether the asserted claims of the '571 patent are distinct from and obvious in view of the '851/'814 patents."); *id.* at 4 ("In deciding a summary judgment motion, the evidence of the non-movant is to be believed, and all justifiable inferences are to be drawn in his favor." (citing *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 255 (1986))); Fed. R. Civ. P. 56(a) ("The court shall grant summary judgment if the movant shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law."). Thus, the district court did not decide whether the claims of the '571 patent are patentably distinct from the claims of the '851 patent. The issue of OTDP therefore remains pending and unresolved in the litigation.

Moreover, the district court's denial of Requester's motion for summary judgment was premised on its decision not to resolve certain issues that the PTO can, and must, resolve. ***First***, the district court expressly declined to resolve the threshold question of "the proper direction" of the "one-way" OTDP analysis. Ex. AF at 16 n.6. In opposing Requester's motion, the patent owner argued that "the proper one-way OTDP inquiry is whether the later-filed patent [*i.e.*, the '851 patent] claims an obvious variation of the invention claimed in the earlier-filed patent [*i.e.*, the '571 patent]." *Id.* However, as Requester argued to the district court and as discussed in more detail in Section IX.E.7 below, "the proper inquiry is whether the later-expiring patent [*i.e.*, the '571 patent] claims an obvious variation of the invention claimed in the earlier-expiring patent [*i.e.*, the '851 patent]." *Id.* That is precisely how the Board of Patent Appeals and Interferences (BPAI) applied the one-way OTDP test in a case with identical circumstances as

this case. *See Ex Parte Pfizer, Inc.*, 2010 WL 532133 (BPAI Feb. 12, 2010) (finding that a later-expiring patent with an earlier priority date (like the '571 patent here) was invalid based on OTDP in view of an earlier-expiring patent with a later priority date (like the '851 patent here)). The district court declined to resolve this issue, but the PTO can and must decide the issue in order to resolve the instant *ex parte* reexamination, and it should apply the one-way OTDP analysis the same way the BPAI applied it in *Ex Parte Pfizer*.

The district court's decision not to resolve this threshold issue infected the remainder of its analysis. In particular, the court cited various alleged "improvements" in the '851 patent compared to the '571 patent. *See* Ex. AF at 15 ("The '851/'814 patents purport to be improvements on the inventions in previous applications. The '851/'814 patents state that their points of novelty are (i) new concepts of programming reference signal generation and memory state demarcation and (ii) the use of reference cells for programming reference signal generation."). However, these alleged differences are irrelevant to the OTDP analysis if applied in the correct direction. Under the proper analysis, what matters is whether the claims of the *later-expiring* '571 patent are patentably indistinct from the claims of the *earlier-expiring* '851 patent. *See* Section IX.E.7, *infra*.

Second, perhaps because it did not decide which direction to compare the claims, the district court also declined to resolve allegedly "conflicting [expert] opinions about the inventions claimed in the '571 and '851/'814 patents and whether the asserted claims of the '571 patent are distinct from and obvious in view of the '851/'814 patents." Ex. AF at 15. But while it might be proper for a district court judge to deny summary judgment and let the factfinder (*e.g.*, a jury) consider competing expert opinions, in an *ex parte* reexamination, the PTO is the factfinder and is well equipped to consider any competing expert opinions and reach a decision. Moreover, as explained in the following sections, when the OTDP analysis is applied in the correct direction, the only proper conclusion is that the claims of the '571 patent are patentably indistinct from the claims of the '851 patent and therefore invalid.

2. The '571 Patent Claims the Same Components and Functions that Are Recited in the Earlier-Expiring '851 Patent

This section introduces the four major components and functions claimed by the '571 and '851 patents: (1) multi-level memory cell, (2) memory cell programming means, (3) reference

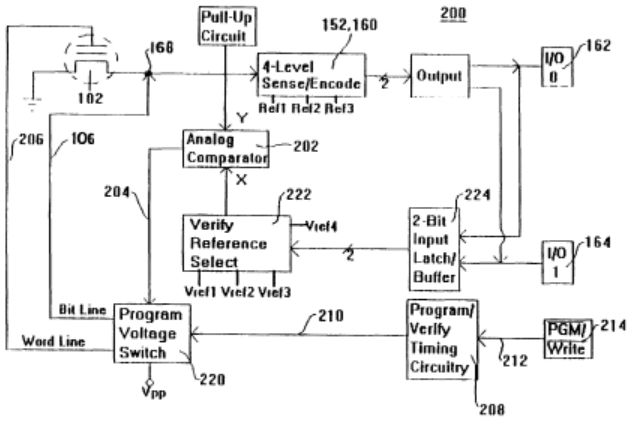
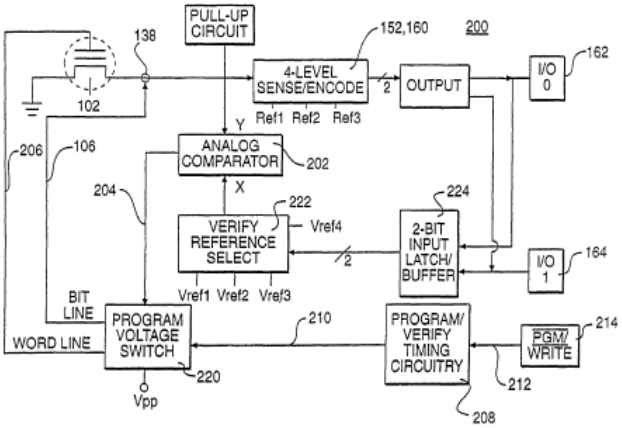
voltage section, and (4) voltage comparison. Sections IX.E.3-5 below provide an element-by-element comparison demonstrating that each element of the '571 patent claims is contained in the claims of the earlier-expiring '851 patent.

(a) Element 1 – Multi-level Memory Cell

Both patents claim a multi-level memory cell structure, defined as having more than two predetermined memory states. Claim 1 of the '571 patent claims this as a "multi-level memory cell for storing input information in a corresponding one" of "predetermined memory states." Ex. A ('571) at 12:7-12. With only slightly different language, claim 1 of the '851 patent recites "an electrically-alterable non-volatile memory cell having more than two predetermined memory states." Ex. H ('851) at 19:40-41. This is the same structure claimed by the '571 patent, including the plurality of memory states. Ex. H ('851) at 4:26-28 ("The invention also provides a programmable multi-level memory apparatus, which comprises an EANVM cell having more than two memory states…."). The '851 patent further recites that the memory cells are to be programmed "in accordance with information indicating a memory state." Ex. H ('851) at 19:46-47.

(b) Element 2 – Memory Cell Programming Means

The '571 and '851 patents each claim a programming structure to program the memory cell. Claim 1 of the '571 patent claims this as a "memory cell programming means," which functions to program the multi-level memory cell. Ex. A ('571) at 12:13. The function of this term is "programming the multi-level memory cell in accordance with the input information," and the corresponding structure is "program/verify timing circuitry and a program voltage switch having its outputs (1) a bit line and (2) a word line." *Id.* at 10:38-60, 11:5-26. Similarly, claim 1 of the '851 patent claims "a programming signal source which applies a programming signal to said memory cell." Ex. H ('851) at 19:42-43. Both patent specifications refer to Fig. 8 as defining the specific programming circuitry. *Compare* Ex. A ('571) at 3:52-53 ("FIG. 8 is a block diagram of a multi-bit per cell system combining program/verify and read circuitry.") *with* Ex. H ('851) at 10:11-12 ("FIG. 8 is a block diagram of circuitry 200 for programming and reading memory cell 102."). At least because Fig. 8 of each patent depicts the same structure (shown below), the structure for programming claimed by each patent is the same.

’571 Patent	’851 Patent
 Figure 8	 FIG. 8

(c) Element 3 – Reference Voltage Selection

The ’571 and ’851 patents also each claim a structure for selecting a reference voltage, where the selected reference voltage is determined by the memory state to which the memory cell is to be programmed. Claim 1 of the ’571 patent claims this as a “reference voltage selecting means,” which functions to select “one of a plurality of reference voltages in accordance with the input information” with the corresponding structure of a “verify reference select circuit.” Ex. A (’571) at 12:16-20. Claim 1 of the ’851 patent recites the same reference voltage selection structure using the term “control circuitry,” whose claimed function is “select[ing] among [a] plurality of programming reference parameters in accordance with information indicating a memory state to which [the] memory cell is to be programmed.” Ex. H (’851) at 19:44-53.

Although the ’851 patent refers to a “reference parameter” rather than “reference voltage,” the specification explains the alleged inventions “in terms of voltage-based memory systems which utilize voltage signals from the memory and reference cells.” Ex. H (’851) at 19:31-37. Thus, while a reference current may also be within the scope of the ’851 patent claims, there can be no dispute that the claims also encompass a reference voltage (the term “parameter” being broader than and including the term “voltage”).

Because the only reference parameters disclosed in the ’851 patent are voltage and current, the term “reference parameter” renders obvious the ’571 patent’s claimed “reference

voltage." *See Abbvie*, 764 F.3d at 1379-80 (Fed. Cir. 2014) ("[W]hen a genus is so limited that a POSITA in the art can at once envisage each member of this limited class a reference describing the genus anticipates every species within the genus.") Indeed, a POSITA in the art would understand voltage and current to be the realistic choices for the reference parameter, and that voltage would be the more common choice. Ex. C at ¶ 150. As in the '571 patent claims, the programming reference parameter corresponds to the memory state to which the cell is to be programmed. Ex. H ('851) at 19:49-50. Despite slightly different verbiage, the structure and function claimed for selecting a reference voltage is the same across both patents.

(d) Element 4 – Voltage Comparison

The '571 and '851 patents claim structure for comparing the voltage of the memory cell with the selected reference voltage to verify when the memory cell has been programmed to the proper memory state. Claim 1 of the '571 patent claims the structure for this as a "comparator means" functioning to compare a voltage of the multi-level memory cell with the selected reference voltage. Ex. A ('571) at 12:21-26. Just like the '571 patent, claim 2 of the '851 patent, which depends from claim 1, claims "control circuitry [that] includes a comparator which compares [a] parameter corresponding to the state of [a] memory cell with the selected programming reference parameter." Ex. H ('851) at 20:5-9. In both patents, the comparator verifies whether the memory cell has been programmed to the proper memory state. *Compare* Ex. A ('571) at 8:43-53, 8:66-9:7, Fig. 8 *with* Ex. H ('851) at 10:44-53, 10:67-11:8, Fig. 8.

Further, and as explained in more detail in section IX.E.3(d) below, the '851 patent's "control circuitry" does not require additional claim construction because such construction is irrelevant to the obviousness-type double patenting analysis in view of the proper comparison – the '851 patent's "comparator" to the '571 patent's "comparator."

Even further, there is no patentable distinction between the "reference voltage" of the '571 patent and the "programming reference parameter" of the '851 patent. The differences between these terms represent mere linguistic changes that do not change the substance of what is claimed. *See* Ex. C at ¶ 150. As demonstrated below, the patentee's edits from the '571 patent specification to the '851 patent specification merely renamed the "verify reference voltage" of the '571 patent to become the "programming reference voltage" of the '851 patent. *Compare* Ex. A ('571) at 8:66-9:7 *with* Ex. H ('851) at 10:67-11:8.

> The voltage threshold of memory cell **102** is then determined by using the comparator **202** to compare the bit line voltage at terminal ~~168~~ 138 with the selected ~~verify~~ programming reference voltage from the verify reference ~~voltage~~ select circuit **222**. When the bit line voltage ~~exceeds that~~ has reached the level of the programming reference voltage supplied by the verify reference ~~voltage~~ select circuit **222**, the output signal ~~204~~ from the comparator ~~202~~ on line **204** will ~~then~~ disable the program voltage switch **220**, ending the programming cycle.

Moreover, as detailed in section IX.E.3(c) below, this slight difference in verbiage does not require additional claim construction of the '851 patent's "reference parameter" because the patents' specifications and claims themselves make clear that the '851 patent's "reference parameter" is synonymous with the '571 patent's "reference voltage." In total, the '571 patent claims the same structure and function, or obvious variants, compared to what is claimed by the '851 patent. *See also* Ex. C at ¶ 156.

(e) Trivial linguistic differences do not create a patentable distinction

Trivial linguistic discrepancies, such as those between the '571 and '851 patent claims, do not avoid invalidity under obvious-type double patenting. Here, the '851 patent's narrower "species" claims, which expired earlier, invalidate the '571 patent's broader "genus" claims. *See, e.g.*, *Geneva Pharm.*, 349 F.3d at 1384 (affirming district court's decision finding invalid, based on obviousness-type double patenting, "later genus" claims that "encompasse[d] a substantial part of the subject matter of" an "earlier species" claim).

3. ’571 Patent Claim 1 Is Obvious over Claims 3, 7 and 14 of the ’851 patent

Claims 3, 7 and 14 of the ’851 patent invalidate the claims of the ’571 patent under the doctrine of obviousness-type double patenting. As demonstrated below,[21] claim 1 of the ’571 patent is obvious in view of, and therefore invalid for obviousness-type double patenting over claims 3, 7 and 14 of the ’851 patent. *See also* Ex. C (Baker decl.) at ¶¶137-162.

(a) ’571 Patent Claim 1, Element 1A

’571 Claim Language	’851 Claim Language
1A: A multi-level memory device comprising:	1. A non-volatile memory apparatus, comprising:
an electrically alterable non-volatile multi-level memory cell...	an electrically-alterable non-volatile memory cell having more than two predetermined memory states
...for storing input information	a programming signal source which applies a programming signal to said memory cell; control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter;

[21] The emphasis marked in the charts is intended to be illustrative and is not offered in any way to limit the scope of arguments made. Obviousness is judged based on the subject matter of the claim *as a whole*. *KSR Int’l v. Teleflex*, 550 U.S. 398, 405 (2007) (citing 35 U.S.C. § 103(a) “. . . such that the subject matter *as a whole* would have been obvious . . .”) (emphasis added).

'571 Claim Language	'851 Claim Language
in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;	...memory cell having more than two predetermined memory states; 14. Non-volatile memory apparatus according to claim 1, said memory cell has an erased state and three further states.

Element 1A of '571 patent claim 1 recites an electrically alterable non-volatile memory cell for storing input information corresponding to one of K^n predetermined memory states, where K^n is more than 2. Likewise, claim 1 of the '851 patent, from which claim 14 depends, recites "an electrically-alterable non-volatile memory cell having more than two predetermined memory states" and explains that the memory cell may be programmed in accordance with information indicating a desired memory state.

Claim 1 of the '851 patent recites control circuitry which, among other things, controls the application of programming signals to a memory cell based on the selected programming reference parameter chosen in accordance with information indicating a memory state to which said memory cell is to be programmed. Thus, element 1A of the '571 patent is indistinct from the claimed elements of claim 14, and its independent claim 1, of the '851 patent. *See also* Ex. C at ¶¶ 137-144.

(b) '571 Patent Claim 1, Element 1B

'571 Claim Language	'851 Claim Language
1B: memory cell programming means for programming said multi-level memory cell	1. . . . a programming signal source which applies a programming signal to said memory cell; . . . control circuitry controlling the application of said programming signal . . . . 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed.

'571 Claim Language	'851 Claim Language
in accordance with said input information;	1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell …. and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter;

'571 patent element 1B is also indistinct from the elements of claim 7, and its independent claim 1, of the '851 patent. Element 1B recites a "memory cell programming means for programming" the memory cell. Claim 1 of the '851 patent recites "a programming signal source which applies a programming signal to said memory cell." Element 1B of the '571 patent further requires that programming is done in accordance with input information. Claim 1 of the '851 patent likewise recite that application of the programming signal to the memory cell is controlled based on the "programming reference parameter," which parameter is selected in accordance with information indicating a memory state to which the memory cell is to be programmed. Consistently, the '851 specification explain that the verify reference select circuit 222 supplies the selected programming reference voltage ("programming reference parameter") [Ex. H ('851) at 10:67-11:4, Fig. 8] where "[t]he verify reference selected circuit 222 is controlled by the two output bits from a 2-bit input latch/buffer circuit 224, which receives binary input bits from the I/O [input/output] terminals 162 and 164." Ex. H ('851) at 10:41-44, Fig. 8. Claim 6 of the '851 patent confirms that the memory cell of claim 1 is in fact programmed in response to the applied programming signal. Ex. C at ¶146. Thus, the claims of the '851 patent clearly recite programming the memory cell in accordance with the input information.

Thus, element 1B of the '571 patent is indistinct from the claimed features of claim 7, and its independent claim 1, of the '851 patent. *See also* Ex. C at ¶¶ 145-148.

(c) '571 Patent Claim 1, Element 1C

'571 Claim Language	'851 Claim Language
1C: reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information,	1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed,
each of said reference voltages corresponding to a different one of said predetermined memory states; and	each programming reference parameter corresponding to a different memory state of the memory cell . . . 3. Non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said parameter corresponding to the state of said memory cell are voltages. 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. 7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator.

'571 patent element 1C is also indistinct from the recited features of claim 7, and independent claim 1, of the '851 patent. Element 1C recites a "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information," which should be construed under 35 U.S.C. § 112 ¶ 6 as having "verify reference select circuit" as its structure and "selecting one of a plurality of reference voltages in accordance with the input information" as its function. Ex. C at ¶ 153. Further, element 1C recites "reference voltages … each of said reference voltages corresponding to a different one of said predetermined memory states," which should be construed as "verify reference voltage(s), each verify reference voltage corresponding to a different one of the predetermined memory states." Ex. C at ¶¶ 150-152. Likewise, claim 1 of the '851 patent, from which claim 7 depends, recites

"control circuitry" which "selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell." The two limitations are indistinct: the specifications of both patents disclose that the corresponding structure for both the "reference voltage selecting means" and the "control circuitry" is the same "verify reference select circuit." Ex. A ('571) at 8:66-9:3; Ex. H ('851) at 10:67-11:4. Further, the claim language of the limitations themselves disclose the same function: selecting one of a plurality of reference voltages in accordance with the input information.

The inclusion of a "voltage" reference parameter in element 1C of the '571 patent does not save element 1C from being obvious in view of claim 7 of the '851 patent. Indeed, not only does the '851 patent focus almost exclusively on embodiments that use voltage as a reference parameter, *see, e.g.*, Ex. H ('851) at 10:54-11:8; *id.* at 19:32-37, but persons of ordinary skill in the art understood that voltages were the most common reference parameters used in programming multi-level memory cells, and therefore would have been obvious reference parameters to employ in the programming process. Ex. C at ¶ 150. "[W]hen a genus is so limited that a POSITA in the art can at once envisage each member of this limited class a reference describing the genus anticipates every species within the genus." *Abbvie*, 764 F.3d at 1379-80 (Fed. Cir. 2014) (internal quotation marks omitted) (affirming finding that species claimed by challenged patent was not patentably distinct from genus in reference patent). Further, claim 3 of the '851 patent expressly states that the reference parameters can be voltages. Ex. A at claim 3.

A simple comparison of the claim language surrounding the "programming reference parameter" from the '851 patent and the "reference voltage" limitation in the '571 patent shows there is no patentable difference between these terms. Claim 1 of the '851 patent shows the "programming reference parameters" to have two distinct requirements: (1) they are selected in accordance with information related to the memory cell's programming state, and (2) they correspond to a different memory state of the cell:

> control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter; and

Ex. H ('851) at 19:44-53 (claim 1) (annotation added). Identically, the "reference voltages" claimed in the '571 patent have the same two requirements:

> reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and

Ex. A ('571) at 12:16-20 (claim 1) (annotation added). No further claim construction for "programming reference parameter" is needed because it is clear that the inventor merely substituted the phrase "programming reference parameter" for "reference voltage" in the later-filed '851 patent.

Additionally, any argument by MLC that the '851 patent describes additional benefits beyond the '571 patent because of these claimed "programming reference parameters" is irrelevant because the proper question is whether the '851 claims render obvious the '571 claims. In any event, such argument would be baseless because the phrase "programming reference parameter" only appears in the '851 patent claims and not in the body of the specification. If MLC argues that "programming reference parameters" is the same as the "programming reference ***signals***" or "programming reference ***voltages***" actually disclosed in the body of the '851 patent specification, such a contention fails because the '851 patent specification makes clear that both are the same as the '571 patent's "reference voltage." *See, e.g.,* Ex. H ('851) at 6:6-10 (describing Fig. 20 as a circuit for generating "programming reference voltages"); 13:50 (referring to "programming reference voltage signals"); 17:51-18:2 (identifying the

"programming reference signals" as "Vref1-Vref4," mirroring to the '571 patent's identification of "verify reference voltages" as "Vref1-Vref4").

In the co-pending litigation, MLC argued that the '851 patent's claimed "programming reference parameter" required additional claim construction as part of the OTDP analysis, and the Court ordered additional briefing as to that claim term. *See* Exs. AH (Court's Order); AI (Micron's letter brief and exhibits to the Court regarding claim construction of "programming reference parameter" in the '851 patent); AJ (MLC's letter brief). The parties proposed the following constructions of "programming reference parameter":

MLC's Construction	Micron's Construction
"reference signal having a level unique to its corresponding memory state used to generate state-demarcating signals"	Plain and ordinary meaning—*i.e.*, "reference voltage[22] or signal used for programming"

Ex. AI (Micron's Letter Br. at 2). As noted, Micron's position was, and remains, that "programming reference parameter" should be given its plain and ordinary meaning, i.e., reference voltage or signal used for programming. In any event, regardless of which party's construction of the phrase "programming reference parameter" is used for the OTDP analysis, the '851 patent claims disclose that the "programming reference parameter" is used in a program/verify cycle, just like is claimed in the '571 patent. Ex. C at ¶ 154. For example, claim 7 of the '851 patent, which depends from and includes the limitations of claims 1, 2, and 6, recites that the selected programming reference parameter is compared to a parameter (*e.g.*, a voltage) corresponding to a state of the memory cell. And further recites that, "after [the] memory cell reaches the memory state to which [the] memory cell is to be programmed," the

[22] The last sentence of the '851 patent states that "the principles of the invention are equally applicable to current-based memory systems in which current levels rather than voltage levels are utilized." '851 patent at 19:35-37. Use of current is irrelevant to the OTDP analysis, and neither party has identified any other issue to which current could be relevant. Thus, Micron has omitted "current" from its construction; but the analysis is the same either way.

"programming signal is stopped." Thus, claim 7 of the '851 patent discloses using the programming reference parameter to verify the contents of the memory cell. *Id*.

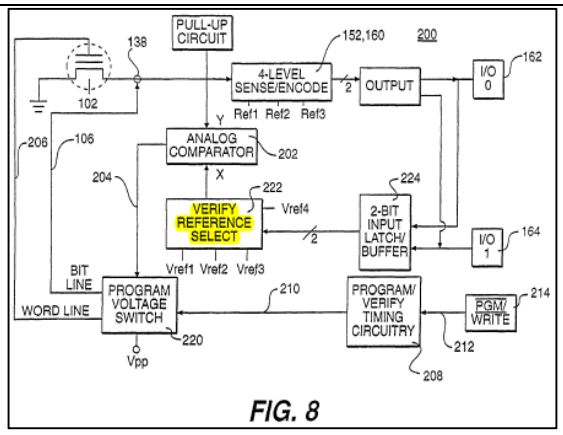
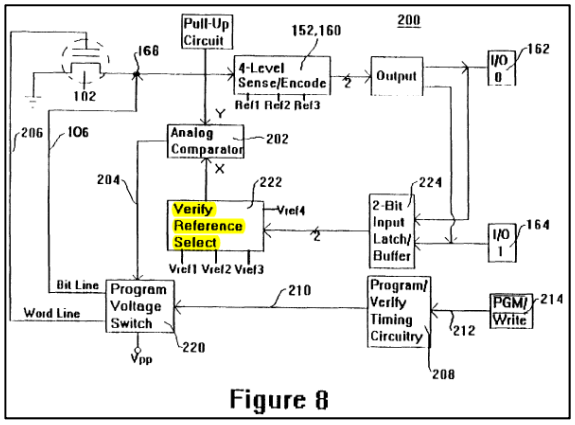
Similarly, the claims of the '571 patent recite that the selected reference voltage/signal is compared to a voltage/signal corresponding to a state of the memory cell. The claims further recite that this comparison verifies that the memory cell has reached the memory state to which it is to be programmed. *Id*. Thus, the claims of the '571 patent, like claim 7 of the '851 patent, recite using the reference voltage/signal to verify the contents of the memory cell. *Id*.

As a result, even if "programming reference parameter" were construed to require that it be "used to generate state-demarcating signals," as MLC has proposed in the co-pending litigation, this additional functionality does not change the fact that the '851 patent claims also disclose the functionality claimed in the '571 patent. Accordingly, the "reference voltages/signals" (and associated functionality) of the '571 patent claims are rendered obvious by the "programming reference parameters" (and associated functionality) of the '851 patent claims. *Id*.

As for MLC's additional arguments that because "programming reference parameters" can be dynamic and have a dependent relationship with "read reference parameters," such an argument is irrelevant because the proper question is whether the '851 claims render obvious the '571 claims, —*i.e.*, asserting that the '851 patent claims recite improvements over the '571 patent does not save the '571 claims from obviousness in view of the narrower, allegedly improved, '851 claim limitation. In any event, such an argument, in addition to being irrelevant, would not withstand scrutiny. The '851 patent purports to encompass "reference signals" without regard to how they are generated: "the system of FIG. 8 ***is not limited as to the manner in which the programming and read reference signals are established***." Ex. H ('851) at 13:59-61 (emphasis added). Dependent claim 9 of the '851 patent recites that ***one*** "of said programming reference parameters and said read reference parameters is generated using a reference cell," which indicates that the independent claims 1 and dependent claims 2, 3, 6, and 7, which form the bases for Requester's invalidity positions, are not limited to "programming reference parameters" generated in a particular manner. The proper construction of "reference voltage/signals" does not impose any requirement that the signals must be generated in any particular manner or that they cannot be used to generate "read reference parameters." Thus, the verify "reference voltages/signals" of the '571 patent would still encompass (and therefore be

rendered obvious by) the "programming reference parameters" of the '851 patent without any additional construction of the '851 patent's "programming reference parameters."

Finally, in its summary judgment briefing in the district court litigation, MLC, and its expert Dr. Jack Lee claimed that Figure 8 from the '851 patent was necessarily modified to work with the allegedly new "programming reference parameter" and that this change demonstrated a need to construe "programming reference parameter." To the extent that MLC argues the same here, a plain comparison of Figure 8 from '851 patent to Figure 8 from the '571 patent dispels this argument:

'851 Patent at Fig. 8	'571 Patent at Fig. 8
 FIG. 8	 Figure 8

As can be seen, Figure 8 from the '571 patent shows the very same "verify reference select" component with the same Vref1-Vref4 inputs, the same input from the "2-bit input latch/buffer" component, and the same output to the "analog comparator" component. No additional claim construction is needed to see that the patents themselves make clear that the '851 patent's "programming reference parameter" is broad enough to include the '571 patent's "reference voltage."

Finally, '571 patent, claim element 1C is also indistinct from claim 3 of the '851 patent. Claim 3, which depends from claims 1 and 2, claims that the programming reference parameters and the parameter corresponding to the memory cell's state are voltages.

Thus, element 1C of claim 1 of the '571 patent is indistinct from claims 3 and 7 of the '851 patent. *See also* Ex. C at ¶¶ 149-154.

(d) ’571 Patent Claim 1, Element 1D

’571 Claim Language	’851 Claim Language
1D: comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage,	2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. 3. Non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said parameter corresponding to the state of said memory cell are voltages. 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. 7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator.

’571 patent element 1D recites a comparator means for comparing a voltage of the multi-level memory cell with the selected reference voltage, which is indistinct from claim 7 of the ’851 patent, and claim 2 from which claim 7 depends. Claim 2 of the ’851 patent recites that the “control circuitry” of claim 1 includes a comparator which compares a parameter corresponding to the state of the memory cell with the selected programming reference parameter. This is indistinct from a proper 35 U.S.C. § 112 ¶ 6 construction of elements 1D and 1E of the ’571 patent—corresponding structure of “the comparator,” which performs the function of “comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information.”

'571 patent element 1D is indistinct from claim 3 of the '851 patent. Claim 3, which depends from claims 1 and 2, specifically recites that the programming reference parameters and the parameter corresponding to the state of the memory cell are voltages. And as noted above in the immediately preceding section (which is incorporated by reference into this section), claim 2 recites that the "control circuitry" of claim 1 includes a comparator which compares a parameter corresponding to the state of the memory cell with the selected programming reference parameter—a similar recitation of the function of element 1D of the '571 patent.

Thus, element 1D of claim 1 of the '571 patent is indistinct from claims 3 and 7 of the '851 patent. *See also* Ex. C at ¶¶ 155-157.

As it did with respect to the claimed "programming reference parameter" of the '851 patent, in the co-pending litigation, MLC argued that the '851 patent's claimed "control circuitry" required additional claim construction as part of the OTDP analysis, and the Court ordered additional briefing as to that claim term. *See* Exs. AH (Court's Order); AI (Micron's letter brief and exhibits to the Court regarding claim construction of "control circuitry" in the '851 patent); AJ (MLC's letter brief). The parties proposed the following constructions of "control circuitry":

MLC's Construction	Micron's Construction
"a circuit for generating and selecting among a plurality of [programming reference parameters] and which controls the application of a programming signal based on the [programming reference parameter]"	Plain and ordinary meaning—*i.e.*, "electronic circuitry for control"

Ex. AI (Micron's Letter Br. at 4). As noted, Micron's position was, and remains, that "control circuitry" should be given its plain and ordinary meaning, *i.e.*, electronic circuitry for control. Ultimately, however, the construction of "control circuitry" does not impact the OTDP analysis when performed in the correct direction (*i.e.*, assessing whether the later-expired '571 patent claims are obvious variants of the earlier-expired '851 patent claims). Micron's position is that the "comparator" expressly recited in dependent claims 2, 6, and 7 of the '851 patent, ***not the "control circuitry,"*** is the same as the "comparator" claimed in the '571 patent. Ex. C at ¶ 157. Whether the "control circuitry" of the '851 patent contains additional elements or features, as MLC proposes, beyond the comparator is irrelevant to evaluating whether the expressly recited comparator describes or renders obvious the comparator of the '571 patent claims. *Id.*

MLC's arguments are a mere diversionary tactic that sidesteps the fact that the "comparator" in the '851 patent is indistinct from the "comparator" in the '571 patent. As demonstrated above, the "comparator" expressly recited in claims 2, 6, and 7 of the '851 patent, ***not the "control circuitry,"*** is the same as the "comparator" in the '571 patent.

Moreover, any argument that the "control circuitry" may include more than just a comparator is irrelevant to a properly applied one-way test for OTDP, as described in more detail in section IX.E.7 below. In short, Requester need only establish the '571 patent claims are obvious in view of the '851 patent. The '851 patent claims expressly recite a comparator. Thus, even if MLC were to argue that "control circuitry" includes more than a "comparator," this is irrelevant. As Requester clearly describes above, the "comparator" limitations from the '571 patent are obvious in view of dependent claim 7 of the '851 patent and, in the alternative, dependent claim 3.

Further, in addition to being irrelevant, any argument that the '851 patent's "comparator" is distinct from that of the '571 patent because '851 patent's "comparator" helps perform programming whereas the '571 patent's "comparator" does not is plainly incorrect because the "comparator" claimed in both patents performs a comparison to verify whether programming is complete. *Compare* Ex. H ('851) at 10:67-11:9 *with* Ex. A ('571) at 8:64-9:7. Regardless, even if the '851 patent's "comparator" performed additional functions, this is irrelevant because it is indisputable that it performs at least the same function as the '571 patent "comparator." *See Magna Elecs., Inc. v. TRW Auto. Holdings Corp.*, 2015 WL 11430786, at *5 (explaining that the Federal Circuit has noted that the failure to claim a limitation in the later expiring patent, making the non-expired claim broader, does not create a patentable distinction). Thus, any argument that the '851 patent's "control circuitry" requires claim construction falls short because it ignores the proper analysis set forth above – the '851 patent's "comparator" to the '571 patent's "comparator.

(e) '571 Patent Claim 1, Element 1E

'571 Claim Language	'851 Claim Language
1E: **said comparator means** further <u>generating a control signal</u> indicating	2. Non-volatile memory apparatus according to claim 1, wherein said **control circuitry includes a comparator** which compares said parameter

’571 Claim Language	’851 Claim Language
whether the state of said multi-level memory cell is the state corresponding to said input information.	corresponding to the state of said memory cell with the selected programming reference parameter. 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. 7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator.

Element 1E of claim 1 of the ’571 patent recites that the comparator means generates a control signal that indicates whether the state of the memory cell has reached the state corresponding to the input information. Ex. A (’571) at 8:63-9:7, 12:22-26. Thus, the control signal indicates whether programming is complete. *Id*. Likewise, claim 7 of the ’851 patent, which incorporates the limitations of claims 1, 2, and 6, recites that the output generated by the comparator (*i.e.*, the signal) changes state once the memory cell has reached the memory state to which the memory cell is to be programmed. Ex. H (’851) at 11:4-8, 20:23-26. The claimed comparator of the ’851 patent is just like the claimed comparator of the ’571 patent: both provide an output that changes from one state to another upon completion of programming to the required memory state. Claim 7 of the ’851 patent also recites the effect of the comparator signal output changing state: the programming signal is no longer applied when the desired memory state is reached. Ex. H (’851) at 20:27-30.

Element 1E of claim 1 of the ’571 patent is also indistinct from claim 3 of the ’851 patent. Claim 2, from which claim 3 depends, requires that the control circuitry include a comparator which compares a parameter corresponding to the state of the memory cell with the selected programming reference parameter. That requirement must be understood in the context of the control circuitry requirements of claim 1 of the ’851 patent. The control circuitry of claim 1 controls “the application of said programming signal to said memory cell *based on the selected programming reference parameter*.” Ex. H (’851) at 19:44-53 (emphasis added). A POSITA in the art would understand that since the comparator is used as part of the control circuitry—and

the control circuitry controls application of the programming signal to the memory cell based on the selected programming reference parameter—then the comparator would output a control signal that indicates whether the memory cell has been programmed to the memory state indicated by the input information. Ex. C at ¶ 158-160. This is clear based on the context of the requirements of claims 1 and 2 of the '851 patent, including claim 2's requirement that the comparator compares two signals: (1) the parameter that corresponds to the current state of the memory cell and (2) the programming reference parameter. *Id.* A POSITA would understand that the comparator performs this comparison operation.

Thus, element 1E of claim 1 of the '571 patent is indistinct from claims 3 and 7 of the '851 patent. *See* Ex. C at ¶¶ 158-162.

4. '571 Patent Claims 9, 12, and 30 Are Obvious over Claims 3 and 7 of the '851 patent

Independent claims 9, 12, and 30 of the '571 patent essentially claim the same substance as claim 1, using functional descriptions of elements to described a claimed apparatus. Thus, claims 9, 12, and 30 are also obvious in view of, and patentably indistinct from, the '851 patent claims. *See* Ex. C at ¶ 163. Thus, each claim is also invalid for obviousness-type double patenting. The first portions of each of these claims are virtually identical and generally recite (1) multi-level memory cells, (2) a selecting device, and (3) a programming signal source. The last portions of each claim recite some aspect of the programming/verifying operation described with respect to claim elements 1B, 1D, and 1E.

(a) '571 Patent Claim 9, Element 9A; Claim 12, Element 12A; Claim 30, Element 30A

'571 Claim Language	'851 Claim Language
9A/12A: Multi-level memory apparatus, comprising: an electrically alterable non-volatile memory cell having more than two predetermined memory states; 30A: Apparatus **for programming** an electrically alterable non-volatile memory cell having more than two	1. A non-volatile memory apparatus, comprising: an electrically-alterable non-volatile memory cell having more than two predetermined memory states;

predetermined memory states, comprising:	. . . a programming signal source which applies a programming signal to said memory cell; **control circuitry . . . controlling the application of said programming signal to said memory cell based on the selected programming reference parameter**;

’571 Patent elements 9A, 12A, and 30A track element 1A and demonstrate the patentee’s strategy of patenting claims with meaningless linguistic variations. In these claim elements, the patentee renames the “device” of element 1A of claim 1 of the ’571 patent as an “apparatus” and no longer redundantly describes a memory cell with multiple memory states as “multi-level.”

While the preamble of element 30A recites an “apparatus for programming,” rather than the “multi-level memory apparatus” recited by elements 9A and 12A, this difference does not patentably distinguish the claim over claim 7 of the ’851 patent for several reasons. First, the context of the ’851 patent claim 1 clearly recites a non-volatile memory apparatus that includes a circuitry for programming. Broadening ’571 claim 30 to omit “multi-level” does not save such claim from invalidity. Moreover, the remaining elements of claim 30 make clear that the claimed apparatus is “multi-level” (because it comprises memory cells with multiple memory states) and “for programming” (because it applies a programming signal to memory cells per element 30C). These remaining elements, moreover, are the same general elements previously claimed within the same patent and, importantly, within the ’851 patent. Thus, elements 9A, 12A, and 30A of the ’571 patent are indistinct from claim 7 of the ’851 patent. *See also, supra* § III.E.1; Ex. C at ¶¶165-168.

(b) '571 Patent Claim 9, Element 9B; Claim 12, Element 12B; Claim 30, Element 30B

'571 Claim Language	'851 Claim Language
9B: a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, **each reference signal corresponding to a different memory state of said memory cell**; 12B/30B: a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, **each reference signal corresponding to a different memory state of said memory cell**;	1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, **each programming reference parameter corresponding to a different memory state of the memory cell** 3. Non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said parameter corresponding to the state of said memory cell are voltages.

Elements 9B, 12B, and 30B of the '571 patent track element 1C except that they more broadly claim "reference *signals*" rather than "reference *voltages*." *See supra*, §§ IX.D.3(c), IX.D.3(d); IX.D.3(e). And as compared to claim 1, from which claim 7 depends, of the '851 patent, the "reference *signals*" of claims 9, 12, and 30 do not patentably distinguish from the claimed "reference *parameters*" of the '851 patent. Ex. C at ¶ 170. Further, merely changing the label of the claim term does not make that term patentably distinct. *See Logic Devices*, 2014 WL 5305979, at *3.

Element 9B purports to further limit the claimed "reference signals" by requiring those "reference signals" be "predetermined," whereas elements 12B and 30B do not. This term is yet another example of a meaningless limitation in view of surrounding claim language. Claim 1 of the '851 patent recites "predetermined" memory states and reference parameters corresponding to those predetermined memory states. Ex. H ('851) at 19:40-54. The reference parameters must be predetermined if they correspond to the predetermined memory states. Ex. C ¶ 171. Thus, elements 9B, 12B, and 30B are indistinct from claim 1 of the '851 patent, from which claim 7 depends. *See also supra*, §§ IX.D.3(d); IX.D.3(e); *see also* Ex. C at ¶¶ 169-172.

(c) '571 Patent Claim 9, Element 9C; Claim 12, Element 12C; Claim 30, Element 9C

'571 Claim Language	'851 Claim Language
9C/12C: a programming signal source which applies a programming signal to said memory cell; and 30C: a programming signal source to apply a programming signal to said memory cell; and	1. . . . a programming signal source which applies a programming signal to said memory cell;

Claim 1 of the '851 patent, from which claim 7 depends, recites elements 9C and 12C verbatim. Element 30C modifies the active phrase "which applies" to "to apply," but otherwise does not differ from elements 9C and 12C. Accordingly, elements 9C, 12C, and 30C are indistinct from claim 7 of the '851 patent. *See also* Ex. C at ¶¶ 173-175.

(d) '571 Patent Claim 9, Element 9D

'571 Claim Language	'851 Claim Language
9D: a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal **to verify whether said memory cell is programmed to the state indicated by said information**.	1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter…. 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. 6. Non-volatile memory apparatus according to claim 2, wherein an **output of said comparator changes state after**

'571 Claim Language	'851 Claim Language
	said memory cell reaches the memory state to which said memory cell is to be programmed. 7. Non-volatile memory apparatus according to claim 6, wherein **the application of said programming signal is stopped in response to the change of state of the output of said comparator**.

The language of element 9D closely parallels the language of elements 1D and 1E, which were discussed above at sections IX.E.3(d) and IX.E.3(e). Element 9D trivially paraphrases element 1E by renaming the action of "indicating" of element 1E to "verifying" in element 9D. Claim 7 of the '851 patent, which includes the limitations of claims 1, 2, and 6 from which it depends, recite that the comparator receives at least two input signals: (1) a parameter corresponding to the state of the memory cell and (2) a programming reference parameter, and compares those signals. Based on the comparison, claim 7 recites that the output signal of the comparator changes state, upon verifying that the memory cell has reached the memory state to which it is to be programmed (*see* claim 6). At this point, claim 7 recites that the programming signal is no longer applied, since the memory cell has reached the memory state to which it is to be programmed. Thus, element 9D is indistinct from claim 7 of the '851 patent. *See supra* §§ IX.D.3(d); IX.D.3(e); *see also* Ex. C at ¶¶ 176-179.

(e) '571 Patent Claim 12, Element 12D

'571 Claim Language	'851 Claim Language
12D: a verifying device which detects a parameter indicating the state of said memory cell and which **verifies whether said memory cell is programmed to the state indicated by said information** based on the detected parameter and the selected reference signal.	1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter…. read circuitry which reads the state of the memory cell by comparing a parameter corresponding to the state of the

	memory cell with a plurality of read reference parameters having values that are different from values of said programming reference parameters . . . . 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. 6. Non-volatile memory apparatus according to claim 2, wherein an **output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed**. 7. Non-volatile memory apparatus according to claim 6, wherein **the application of said programming signal is stopped in response to the change of state of the output of said comparator**.

The language of element 12D of the ’571 patent also closely parallels that of elements 1D and 1E, which are discussed above in sections IX.E.3(d) and IX.E.3(e). Element 12D trivially paraphrases or broadens elements 1D and 1E (claiming a “comparator means”) and element 9D (claiming a “comparator”) by renaming the “comparator” to its functional equivalent: “a verifying device.” *See* Ex. H (’851) at 10:54-11:8. There is no question that the verifying device functionality of element 12D is recited by claim 7 of the ’851 patent. Claim 7, and claims 1, 2, and 6 from which it depends, recite a comparator and its performance of verification operations to verify whether the memory cell is programmed to the proper state indicated by the information based on a comparison of a parameter indicating a memory state and the selected reference signal. Thus, element 12D is indistinct from claim 7 of the ’851 patent. *See supra*, §§ IX.D.3(d); IX.D.3(e); *see also* Ex. C at ¶¶ 180-183.

(f) ’571 Patent Claim 30, Element 30D

’571 Claim Language	’851 Claim Language
30D: a control device to control the application of said	1. . . . a programming signal source which applies a programming signal to said memory cell; control circuitry which generates a plurality of programming reference

programming signal to said memory cell based on the selected reference signal.	parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell ….and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter; 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. 7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator.

Claim 1 of the ’851 patent recites “control circuitry” which performs the same functionality as the “control device” recited in element 30D. As can be seen from the plain claim language of the ’851 patent, the claimed “control circuitry” “control[s] the application of said programming signal to said memory cell.” This is the same claim function as the claimed “control device” in the ’571 patent: “to control the application of said programming signal to said memory cell.” Further, as described above, the use of a “selected reference signal” in the ’571 patent is not different from using the “selected programming reference parameter” in the ’851 patent; both are used to control the programming signal to the target memory cell. *See* Ex. C ¶ 185. Thus, element 30D is indistinct from claim 7 of the ’851 patent. *See* Ex. C ¶¶ 184-187.

5. ’571 Patent Claims 42 and 45 Are Obvious in View of the ’851 patent

Independent claims 42 and 45 of the ’571 patent essentially claim the same substance as claim 1, but in method form. Because the limitations recited in a method claim can be disclosed

by or rendered obvious in view of an apparatus claim, *In re Lonardo*, 119 F.3d at 968; *Unova*, 2006 WL 5434550, at *1, claims 42 and 45 are obvious in view of the '851 patent claims. *See* Ex. C at ¶188. The first portions of each of claims 42 and 45 are identical and generally recite (1) selecting a reference signal and (2) applying a programming signal. The last portions of each claim recite some aspect of the programming/verifying operation described in sections IX.E.3(d) and IX.E.3(e).

(a) '571 Patent Claim 42, Element 42A; Claim 45, Element 45A

'571 Claim Language	'851 Claim Language
42A/45A: A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	1. A non-volatile memory apparatus, comprising: an electrically-alterable non-volatile memory cell having more than two predetermined memory states; a programming signal source which applies a programming signal to said memory cell;

'571 patent claim elements 42A and 45A closely parallel element 1A, and for the same reasons discussed above for element 1A, claim elements 42A and 45A are indistinct from at least claim 7 of the '851 patent. *See supra*, § IX.E.3(a); *see also* Ex. C at ¶¶ 190-193.

(b) '571 Patent Claim 42, Element 42B; Claim 45, Element 45B

'571 Claim Language	'851 Claim Language
42B/45B: selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed,	1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed,
each reference signal corresponding to a different	each programming reference parameter corresponding to a different memory state of the memory cell

memory state of said memory cell;	3. Non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said parameter corresponding to the state of said memory cell are voltages.

Claim elements 42B and 45B of the ’571 patent are shown in the operation of the control circuitry in claim 1 of the ’851 patent (“control circuitry...selects among said plurality…”). *See* Ex. H (’851) at 19:44-53. Thus, claim elements 42B and 45B of the ’571 patent are disclosed by or obvious in view of at least claim 7 of the ’851 patent. *See* Ex. C at ¶¶ 194-196.

(c) ’571 Patent Claim 42, Element 42C; Claim 45, Element 45C

’571 Claim Language	’851 Claim Language
42C/45C: applying a programming signal to said memory cell;	1. . . . a programming signal source which applies a programming signal to said memory cell;

’571 patent claim elements 42C and 45C, are nearly identical to the claimed “programming signal source” function in claim 1 of the ’851 patent and thus are at least obvious in view of the same. *See* Ex. C at ¶¶ 197-199.

(d) ’571 Patent Claim 42, Element 42D

’571 Claim Language	’851 Claim Language
42D: detecting a parameter indicating the state of said memory cell; and	1. . . . read circuitry which reads the state of the memory cell by comparing a parameter corresponding to the state of the memory cell with a plurality of read reference parameters having values that are different from values of said programming reference parameters . . . .

verifying whether said memory cell is programmed to the state indicated by said information based on **the detected parameter and the selected reference signal.**	2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares **said parameter corresponding to the state of said memory cell with the selected programming reference parameter.** 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. 7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator.

As explained above, the control circuitries of the '851 patent include a comparator. *See supra*, §§ IX.E.3(d); IX.E.3(e). That claimed comparator receives as its inputs at least a parameter corresponding to the state of the memory cell along with the selected programming reference parameter ("reference signal"). Upon detecting those parameters, the two are compared for purposes of verifying whether the memory cell has been programmed to the proper state (claim 6). If it is verified that the memory cell has reached the correct state, the state of the comparator's output signal changes and application of the programming signal to the memory cell is stopped (claims 6 and 7). Claim element 42D discloses this same "detecting" and "verifying." Thus, claim element 42D is obvious over and indistinct from at least claim 7 of the '851 patent. *See* Ex. C at ¶¶ 200-203.

(e) '571 Patent Claim 45, Element 45D

'571 Claim Language	'851 Claim Language
45D: and controlling the application of said programming signal to said memory cell based on the selected reference signal.	1. . . . a programming signal source which applies a programming signal to said memory cell; control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each

	programming reference parameter corresponding to a different memory state of the memory cell . . . and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter; 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.

As explained above, the '851 patent' control circuitries control the application of the programming signal based on a selected reference signal. *See supra,* §§ IX.E.3(d); IX.E.3(e). Besides the immaterial replacement of "selected *programming* reference *parameter*" in the '851 patent with the "selected reference *signal*" in the '571 patent, this '571 patent limitation in mirrored in the '851 patent. Thus, claim element 45D is obvious over and indistinct from at least claim 7 of the '851 patent. *See* Ex. C at ¶¶ 204-207.

For the reasons discussed above, claims 1, 9, 12, 30, 42, and 45 of the '571 patent are invalid under the judicially-created doctrine of obviousness-type double patenting over the '851 patent.

6. The "Safe Harbor" Provision of 35 U.S.C. § 121 Does Not Apply to the '571 Patent

(a) Introduction

In the co-pending litigation before the U.S. District Court for the Northern District of California, *MLC Intellectual Property, LLC v. Micron Technology, Inc*., Case No. 3:14-cv-03657-SI, the current assignee of the '571 patent, MLC Intellectual Property, LLC ("MLC"), filed a Motion for Summary Judgment asserting the safe-harbor of 35 U.S.C. § 121 as a defense to OTDP. Following briefing by both parties, the Court held that "consonance is lacking," and MLC therefore did not meet its burden of demonstrating that it is entitled to summary judgment that the § 121 safe harbor applies, "as the challenged/alleged divisional '571 patent claims the same invention elected in the restricted '816 application." Ex. AF (*MLC v. Micron*, Case No. 3:14-cv-03657-SI, Dkt. No. 128) at 7-8 (April 26, 2017). In addition, the Court rejected MLC's

motion because "[MLC] has not met its summary judgment burden of demonstrating that patents descending ultimately from an application originally filed as a CIP can be 'divisional applications' for § 121 purposes." *Id*. at 8-9. As the Court correctly decided in the co-pending litigation, the '571 patent is not entitled to protection afforded by 35 U.S.C. § 121, and to the extent Patent Owner MLC attempts to make such arguments in defense of an instituted *ex parte* reexamination, such arguments should be rejected by the PTO as they were by the Court.

In order to invoke § 121's safe harbor, the reference patent (here, the '851 patent) must have issued either on an application in which a restriction requirement was made, or on an application filed as a result of such requirement. In the co-pending litigation, Patent Owner MLC did not dispute that there was no restriction requirement made in the application for the '851 patent. Instead, MLC argued, and will likely argue in any instituted *ex parte* reexamination, that the '851 patent was filed "as a result of" a restriction requirement made more than thirteen years earlier during prosecution of the '816 application. But the '851 patent was not filed "as a result of" the restriction requirement made during the '816 application for two key reasons. First, the '851 patent claims are not the claims that were restricted out of the '816 application—rather, the '851 patent discloses and claims new subject matter that was not part of the '816 application. Second, the '851 patent fails to claim priority to the '816 patent application and therefore does not trace its "lineage" back to the '816 application. A patent that is not related to, and does not refer to, the application in which a restriction requirement was made cannot be said to have been filed "as a result of" that restriction requirement.

The safe harbor provision requires the patent being challenged, here the '571 patent, to have issued from an application filed "as a result of" the same restriction as the reference patent. *Boehringer*, 592 F.3d at 1352 ("We have repeatedly held that the 'as a result of' requirement applies to the challenged patent as well as the reference patent."); 35 U.S.C. § 121. Thus, for a challenged divisional patent to qualify for the § 121 safe harbor, it must also contain claims that were restricted and removed from an earlier application and that reappear in the subsequent divisional application. *Geneva Pharm*., 349 F.3d at 1379. The '571 fails to satisfy the requirements for safe harbor protection for at least these reasons and the additional reasons discussed below.

(b) The Safe Harbor of 35 U.S.C. § 121

Section 121, titled "Divisional applications," provides in relevant part (with numbers in brackets added for ease of reference):

> [1] If two or more independent and distinct inventions are claimed in one application, the Director may require the application to be restricted to one of the inventions. [2] If the other invention is made the subject of a divisional application which complies with the requirements of section 120 of this title it shall be entitled to the benefit of the filing date of the original application. [3] A patent issuing on an application with respect to which a requirement for restriction under this section has been made, or on an application filed as a result of such a requirement, shall not be used as a reference either in the Patent and Trademark Office or in the courts against a divisional application or against the original application or any patent issued on either of them, if the divisional application is filed before the issuance of the patent on the other application.

Section 121 relates to the Patent Office's ability to impose "restriction requirements" during examination when it determines that an applicant seeks to claim multiple inventions in the same application. *St. Jude Med., Inc. v. Access Closure, Inc.,* 729 F.3d 1369, 1376 (Fed. Cir. 2013). For example, if the Patent Office determines that an application seeks to claim "invention A and invention B," it can require the applicant to select either A or B for prosecution in that application. *Id.* If the applicant selects invention A, she can then "remove[] claims to invention B from the restricted application and file[] those claims in a subsequent application," referred to as a divisional application, claiming priority to the filing date of the original application. *Id.* "The restricted application and the subsequent application later issue as patents." *Id.* This practice of filing divisional applications as a result of a restriction requirement is codified in the first and second sentences of § 121 above.

Before § 121 was enacted in the 1952 Patent Act, this practice of filing divisional applications presented some risk to patent applicants. In particular, the restricted parent application could be used to invalidate subsequent divisional applications under the doctrine of double patenting. *See id.* at 1376-77; *Boehringer Ingelheim Int'l GmbH v. Barr Labs., Inc.,* 592 F.3d 1340, 1350 (Fed. Cir. 2010) ("Prior to the 1952 Patent Act, courts and patentees were aware of the unfairness that resulted when the Patent Office required restriction or division between

claims in a patent application, thus requiring that a second patent application be carved out of the first, and then rejected the second application on the basis of the first.").

To avoid this problem, a "safe harbor" provision was included in the third sentence of § 121. This safe harbor "protects a divisional application, the original application, or any patent issued on either of them from validity challenges based on a patent issuing on an application subjected to a restriction requirement or on an application filed as a result of a restriction requirement. In effect, the third sentence of § 121 shields patents that issue on applications filed as a result of a restriction requirement from double patenting invalidation." *Amgen Inc. v. F. Hoffman-La Roche Ltd,* 580 F.3d 1340, 1350 (Fed. Cir. 2009).

Section 121 thus prevents the unfairness that can result from a restriction requirement. However, divisional practice also raises the possibility of a patentee using this process to extend its patent in time, especially under the patent statute at the time the '571 challenged patent application was filed, when the lifetime of U.S. patents extended 17 years from issuance, rather than the current 20 years from the earliest effective priority date. *See, e.g.*, 35 U.S.C. § 154(a)(2), (c); Manual of Patent Examining Procedure ("MPEP") § 2701, *available at* https://www.uspto.gov/web/offices/pac/mpep/. There is a possibility that by simply filing a divisional and claiming the safe-harbor of § 121, the patentee would have two patents covering the same subject matter for well beyond the 17-year statutory period. The Federal Circuit recognized this risk and so has "appl[ied] a 'strict test' for application of section 121, given the potential windfall a patent term extension could provide to a patentee." *G.D. Searle LLC v. Lupin Pharm., Inc.,* 790 F.3d 1349, 1354 (Fed. Cir. 2015) (quoting *Geneva Pharm., Inc. v. GlaxoSmithKline PLC,* 349 F.3d 1373, 1382 (Fed. Cir. 2003)) (emphasis added).

Indeed, there are numerous specific requirements that must be met to satisfy the "strict test" for the § 121 safe harbor. For example, "the protection afforded by section 121 to applications (or patents issued therefrom) filed as a result of a restriction requirement is limited to divisional applications," and therefore does not apply to continuation-in-part applications (i.e.,

an application that adds subject matter not disclosed in the earlier application) or even to continuation applications (i.e., an application that does not add new matter). *Pfizer, Inc. v. Teva Pharm. USA, Inc.,* 518 F.3d 1353, 1362 (Fed. Cir. 2008) (emphasis added); *see also Amgen*, 580 F.3d at 1353 ("[T]he § 121 safe harbor provision does not protect continuation applications or patents descending from only continuation applications."). Moreover, to invoke the § 121 safe harbor, ***both the challenged patent and the reference patent must have issued "as a result of" a restriction requirement***. *See Boehringer,* 592 F.3d at 1352 ("We have repeatedly held that the 'as a result of' requirement applies to the challenged patent as well as the reference patent.").

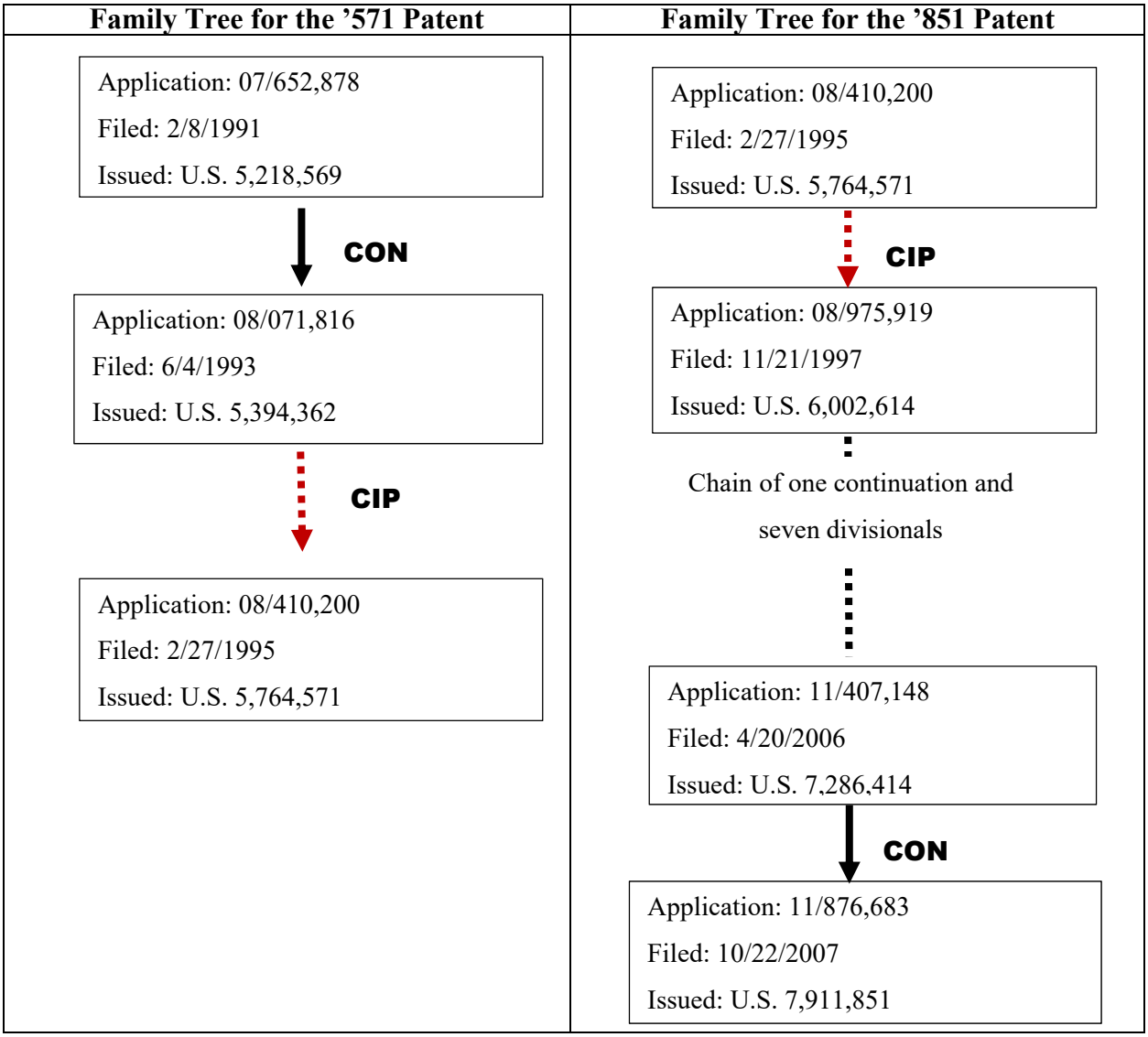
Section 121 further imposes both requirements and restrictions as to what claims appear in the divisional patents filed "as a result of" a restriction requirement. For example, ***a divisional application "must contain formally entered claims that are restricted and removed" from the earlier application*** and that "reappear in [the] separate divisional application after the restriction." *Geneva Pharm.,* 349 F.3d at 1379 (emphasis added). It is not enough for "the original application merely . . . to provide some support for claims that are first entered formally in the later divisional application." *Id.* On the other hand, ***"a divisional application filed as a result of a restriction requirement may not contain claims drawn to the invention set forth in the claims elected and prosecuted to patent in the parent application.*** The divisional application must have claims drawn only to the 'other invention.'" *Gerber Garment Tech., Inc. v. Lectra Sys., Inc.,* 916 F.2d 683, 687 (Fed. Cir. 1990) (emphasis added). This is a concept known as "consonance," and it applies to both the challenged patent and the reference patent. *See St. Jude Med.,* 729 F.3d at 1377. Thus, in a case like this, where the challenged patent (i.e., the '571 patent) and the reference patent (i.e., the '851 patent) are both allegedly divisional patents, "[c]onsonance . . . requires that the challenged patent, the reference patent, and the patent in which the restriction requirement was imposed (the restricted patent) do not claim any of the same inventions identified by the examiner." *Id.* (emphasis in original).

Finally, the burden is on the patent holder to prove that § 121 applies. *See Geneva Pharm.,* 349 F.3d at 1381; *Medtronic, Inc. v. AGA Med. Corp.,* No. C-07-0567 MMC, 2009 WL 1068884, at *3 (N.D. Cal. Apr. 21, 2009). As is evident, the § 121 safe harbor requirements are strict and its protection is purposely reserved for very limited circumstances. Not only does MLC fail to meet its burden of showing application of the § 121 safe harbor in this case, MLC simply ignores and omits the facts and law that establish it is not entitled to safe harbor protection.

(c) Relevant Factual Background

In prosecuting the ’571 challenged and ’851 reference patents (and other patent family members), MLC[23] did not follow the § 121 safe harbor requirements. To see why, a more detailed review of the prosecution histories is necessary. Relevant portions of the prosecution histories are illustrated in the diagrams below, which illustrate continuations as a solid arrow, divisionals as a black dotted arrow, and continuations-in-part as a red dotted arrow.

[23] Although the patents were prosecuted by inventor, Jerry Banks, and BTG, their actions during prosecution can now be attributed to MLC as the successor-in-interest. This is consistent with MLC’s treatment of its position in the co-pending litigation.



The '571 challenged patent claims priority all the way back to a patent application filed on February 8, 1991, U.S. Patent Application No. 07/652,878, which issued as U.S. Patent No. 5,218,569 (the '569 patent). Ex. N. Following this application, MLC filed application number 08/071,816 (the '816 application, also referred to as "the '816 restricted application"), which issued as U.S. Patent No. 5,394,362 (the '362 patent, also referred to as "the '362 restricted patent"). Ex. O. On June 7, 1994, during prosecution of the '816 application, the patent examiner issued a restriction requirement, requiring MLC to select one of three identified groups

of claims: "I. Claims 31, 33 and 35, drawn to memory system, classified in Class 365, subclass 189.07"; "II. Claim 37, drawn to method of operation [of] a FET, classified in Class 365, subclass 185"; or "III. Claim 39, drawn to FET Device, classified in Class 257, subclass 213." Ex. P (Restriction Requirement).[24] MLC elected to pursue Group I, "a memory system." *See id.*

[24] Claim 31 from Group I, claim 37 from Group II, and claim 39 from Group III are shown below:

> 31. An electrically alterable non-volatile multi-level memory device, comprising:
>
> a non-volatile, multi-level memory cell means for storing input information for an indefinite period of time as a discrete state of said memory cell means, said memory cell means includes more than two memory states;
>
> memory cell programming means for programming the memory state of said multi-level memory cell means to a predetermined state corresponding to input information to be stored in said memory cell means; and
>
> comparator means for comparing the memory state of said memory cell means with the input information to be stored in said memory and for generating a control signal indicative of the memory state of said memory cell;
>
> wherein said memory cell includes a gate which has an applied voltage being set to one of a plurality of voltage levels by said memory cell programming means corresponding to the input information.

> 37. A method of writing and reading an electrically alterable non-volatile memory, comprising the steps of:
>
> providing a multi-level memory cell including a floating gate FET having a channel region coupled between a cell output terminal and a terminal for a first reference voltage, and having a floating gate for storing electrons and for controlling the conductivity of the channel region of the FET, said memory cell includes more than two memory states; and
>
> setting the floating gate to an applied voltage at one of a plurality of voltage levels corresponding to input information, said setting step storing electrons on the floating gate to get the voltage threshold of said memory cell so that the conductivity of said channel region is within one of a plurality of predetermined ranges of conductivity of said channel region; and

(Response to Restriction Requirement). Claims 31, 33, and 35 in the '816 restricted application issued as claims 1-3 of the '362 patent on June 4, 1993. *See id.* (May 5, 1994 Amendment at 1-4); *id.* (Notice of Allowance).

The day before the '362 patent issued, MLC filed application number 08/410,200 (the '200 application), which eventually issued as the '571 patent. Rather than file a divisional application with claim 37 or claim 39 from the '816 restricted application, MLC instead filed the '200 application as a continuation-in-part application with a number of changes, including new figures (Figs. 15-20) and accompanying text, and an entirely new set of claims directed to "[a] multi-level memory device" and "[a]n integrated circuit." Ex. B at 51-57, 84-89 (original application as filed at pages 21-34 and Figs. 15-20, respectively). Two years later, on June 19, 1997, MLC amended the '200 application in an attempt to remove the new material from the application and convert it from a continuation-in-part to a divisional. *See id.* at 144, 164 (June 17, 1997 Office Action Response). MLC also replaced the pending claims with a new set of claims. Even still, MLC failed to include claim 37 or claim 39 from the '816 application, which were the restricted claims from the parent application, as required by the safe harbor provision of § 121. The new set of claims issued as the claims of the '571 challenged patent on June 9, 1998. *See* Ex. A ('571 Patent) at Claims 1-47.

While the application for the '571 patent was still pending, MLC filed application number 08/975,919 (the '919 application), also as a continuation-in-part. MLC added Figs. 15-20 and accompanying text from the prior '200 application back into this '919 application, as well

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> comparing the voltage of a bit line connected to the cell output terminal of said memory cell with an n-bit digital input signal which represents an n-bit world [sic] to be stored in the memory cell.
>
> 39. The device for the method of claim 37.

Ex. P (May 5, 1994 Amendment at 1-4).

as new figures (Figs. 21-23) and accompanying text. The ’919 application eventually issued as U.S. Patent No. 6,002,614 (the ’614 patent, also referred to as “the ’614 CIP patent”). Ex. Q. The ’614 patent is thus a continuation-in-part of the ’571 patent.

Following the ’614 CIP patent, MLC filed a series of related patent applications. The first application in this series claimed priority via the ’614 patent all the way back to the parents of the ’571 challenged patent, including the ’816 application (i.e., the application with the restriction requirement). *See* Ex. R (U.S. 6,246,613) at (60), 1:9-16. However, beginning with application number 09/493,139 (the ’139 application), none of the applications claimed priority to the parent applications of the ’571 patent. Instead, the ’139 application and each subsequent application therefrom claimed priority—via the ’614 CIP patent—only to the ’571 challenged patent. *See* Exs. S-Z and H, U.S. App. 09/493,139 at 9-10; U.S. Patent Nos. 6,353,554 at (63), 1:9-17; 6,434,050 at (60), 1:10-19; 6,714,455 at (60), 1:9-19; 7,006,384 at (60), 1:10-23; 7,068,542 at (60), 1:10-24; 7,286,414 at (60), 1:11-27; 7,911,851 at (60), 1:11-28; 8,570,814 at (60), 1:11-30. Thus, from the ’139 application forward, no patent that is relevant here ever claimed priority to the ’816 application / ’362 patent, where the restriction requirement at issue was entered.

Eventually, on October 22, 2007, through a series of additional applications, MLC filed application number 11/876,683, which issued as the ’851 reference patent (Ex. H) (i.e., the reference patent for the OTDP analysis here). Like the several applications before it, the ’851 reference patent claimed priority only to the ’571 challenged patent, and not the ’816 application / ’362 patent in which the original restriction requirement was issued. *See* Ex. H, ’851 Patent at (60), 1:11-28. The effect of MLC’s decision to break the priority chain was to extend the term of the ’851 patent by several years. Importantly, the ’851 reference patent claimed priority to the ’571 challenged patent via the ’614 CIP patent, and included the new material added by that patent. *See id.* And like the applications before it, the ’851 reference patent did not include either claim 37 or claim 39, the original restricted claims, from the ’816 restricted application.

Instead, all of the claims of the ’851 reference patent are directed to “[a] non-volatile memory apparatus.” *See* Ex. H (’851 Reference Patent) at Claims 1-15.

In total, there were ten patent applications leading up to the ’851 reference patent, all of which claim priority to the ’571 challenged patent via a continuation-in-part.

(d) Argument

The ’571 patent and the ’851 patent both fail to meet the requirements of § 121 for several independently dispositive reasons. As explained below, both patents fail—on multiple grounds—to meet § 121’s requirement that they have issued from an application filed “as a result of” the restriction requirement originally issued during prosecution of the ’816 restricted application. In addition, both patents violate the consonance requirement of § 121. Accordingly, to the extent MLC argues during the *ex parte* reexamination that the § 121 safe harbor applies, the reexamination unit should deny any such argument.

(i) The ’851 Patent Does Not Qualify for the § 121 Safe Harbor Because It Was Not Filed “As a Result of” the Restriction Requirement in the ’816 Restricted Application

To the extent MLC attempts to argue that the § 121 Safe Harbor applies to the reference ’851 patent as it did previously in support of its rejected motion for summary judgment in the co-pending district court litigation, under the plain language of § 121, in order for the ’851 reference patent to qualify for the safe harbor as MLC claims, it must have been filed “as a result of” the restriction requirement in the ’816 restricted application. MLC cannot show that to be the case for several reasons. First, the claims of the ’851 patent did not appear in the ’816 application and thus were not restricted out of that application and later pursued in the ’851 patent, as is required to qualify under § 121. In fact, the claims of the ’851 patent could not have appeared in the ’816 application because the ’851 patent claims priority via a continuation-in-part that discloses new subject matter and the ’851 patent relies on that new matter to support its claims. Moreover, the ’851 patent cannot possibly have issued from an application filed “as a result of” the restriction

requirement in the '816 application because it does not even claim priority to the '816 application. For each of these reasons, the '851 patent fails to qualify for the § 121 safe harbor.

a. The Claims of the '851 Patent Were Not, and Could Not Have Been, Included in the '816 Restricted Application

i. The Claims of the '851 Patent Were Not Restricted Out of the '816 Application, As Is Required for the § 121 Safe Harbor

The Federal Circuit has held that for a subsequent patent to qualify for the § 121 safe harbor, it "must contain formally entered claims that are restricted and removed" from an earlier application and that "reappear in a separate divisional application after the restriction." *Geneva Pharm.,* 349 F.3d at 1379 ("The text of § 121 does not suggest that the original application merely needs to provide some support for claims that are first entered formally in the later divisional application."); *see also Medtronic*, 2009 WL 1068884, at *3 (citing the above holding from *Geneva Pharmaceuticals* in support of its conclusion that the § 121 safe harbor did not apply because the patentee failed to show that claims in a patent were the subject of an earlier restriction requirement). That is not what happened here. Neither restricted claim 37 nor restricted claim 39 from the '816 restricted application ever "reappear[ed]" during prosecution of the '851 reference patent. Likewise, the claims of the '851 patent never appeared in the '816 application. Therefore, the claims of the '851 patent "could not have been subject to [the] restriction requirement." *Geneva Pharm*., 349 F.3d at 1379. If MLC "sought the benefit of § 121, [it] "should have requested entry of the claims [of the '851 patent during prosecution of the '816 application] so that the PTO could issue a formal restriction requirement." *Id.* at 1379-80. MLC failed to do so. In fact, the claims of the '851 patent were not entered until an amendment during prosecution on December 16, 2009—***more than 15 years*** after the June 7, 1994 restriction requirement. *Cf. Geneva Pharm*., 349 F.3d at 1382 (concluding that a "thin and insufficient record" could not shield under § 121 patents that "took about a quarter-century to prosecute").

Because the ’851 patent claims were not pursued in and restricted out of the ’816 restricted application, the ’851 patent did not issue “as a result of” the restriction requirement in the ’816 application. Therefore, the ’851 patent does not qualify for the § 121 safe harbor. This alone is fatal to MLC’s motion for summary judgment.

ii. The ’851 Patent Discloses and Claims New Matter That Could Not Have Been Pursued in the ’816 Restricted Application

In fact, not only were the claims of the ’851 patent not pursued in the ’816 restricted application, but they ***could not have been*** pursued in the ’816 application because the ’851 patent (1) claims priority via a continuation-in-part that discloses new subject matter and (2) relies on that new matter to support its claims.

The Federal Circuit has made clear “that the protection afforded by section 121 to applications (or patents issued therefrom) filed as a result of a restriction requirement is limited to divisional applications,” and therefore does not protect CIP applications. *Pfizer, Inc.,* 518 F.3d at 1362. While *Pfizer* specifically held that the challenged patent cannot be a continuation-in-part, the same must also be true for the reference patent. Both must be “divisional applications,” and this is supported by the text of the statute and by *Pfizer* and other Federal Circuit cases.

As the title of the statute suggests, § 121 is all about “Divisional applications.” The first two sentences contemplate that an applicant will file one or more divisional applications to claim “the other invention[s]” that were restricted out of the original application. 35 U.S.C. § 121. Thus, when the third sentence of § 121 refers to the “reference” patent as being issued “on an application filed as a result of [a restriction] requirement,” the only plausible interpretation is that the reference patent must issue from a divisional application—just like the challenged patent. *Id.*; *see also, e.g., Pfizer,* 518 F.3d at 1360 (“[T]he third sentence of the statute provides a safe harbor ***(for patents or applications derived as the result of a restriction requirement)*** from attack . . . based on applications or patents ***similarly derived*** from the same restriction

requirement." (emphasis added)). Indeed, as the Federal Circuit has explained, "[t]he safe harbor is provided to protect an applicant from losing rights when an application is ***divided***." *Boehringer*, 592 F.3d at 1350 (emphasis in original). Any reasonable reading of § 121 indicates that the reference patent—just like the challenged patent—cannot be a continuation-in-part.

Here, the '851 patent indisputably claims priority to the '571 patent via the '614 CIP patent. In the district court litigation, MLC attempted to conceal this fact by focusing instead on the so-called "divisional" '139 application in the priority chain between the '571 patent and the '851 patent. However, the '139 application—as well as every other intervening application—includes numerous figures and accompanying text that were not included in the '571 patent. *Compare* Ex. S ('139 Application) at Figs. 15-23 and pages 34-49 *and* Ex. H ('851 Patent) at Figs. 15-23, Cols. 13:47-19:37 *with* Ex. A ('571 Patent). Thus, while a particular application in the chain might be deemed a "divisional" of the immediately preceding application, every single application in the chain, as well as the resulting '851 reference patent, is a continuation-in-part with respect to the '571 patent. *See Pfizer,* 518 F.3d at 1359 ("A CIP . . . partly continues subject matter disclosed in a prior application, but it adds new subject matter not disclosed in the prior application."). Moreover, the Federal Circuit has made clear that an application cannot merely be designated divisional when it contains new matter that was not present in the parent application. *G.D. Searle*, 790 F.3d at 1354-55 ("The '113 application cannot be a divisional of the '594 application, despite being designated as such in the reissue patent, because it contains new matter that was not present in the '594 application.").[25] Because the '851 patent

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[25] In support of its motion for summary judgment in the co-pending litigation, MLC relied upon the *Amgen* and *Boehringer* cases. Those cases merely establish that ***intervening continuation or***

indisputably claims priority to the ’571 patent via a continuation-in-part, it cannot qualify for the § 121 safe harbor.

Even if claiming priority via a continuation-in-part were not dispositive by itself, the ’851 patent still fails under § 121 because it claims subject matter added after the ’816 application and therefore could not have been filed “as a result of” the restriction requirement in the ’816 application. As explained above, several of the figures and accompanying text of the ’851 patent were added by the ’614 CIP patent. *See, e.g.,* ’851 Patent at Figs. 15-23, Cols. 13:47-19:28. This new matter is claimed by the ’851 patent, as MLC explained when it added the claims during prosecution: “Claim 1 has been cancelled without prejudice or disclaimer in favor of newly presented Claims 23-37. The newly presented claims are supported by ***Figs.* 8** and ***15-23 and the related description***.” Ex. M (’851 Patent File History, December 16, 2009 Amendment at 7) (emphasis added). For example, the concept of a “reference cell,” which is claimed in dependent claims 9-13 of the ’851 patent, is not mentioned in the ’571 patent but is described at length in the new matter in the ’851 patent. *See, e.g.,* Ex. H (’851 patent) at Col. 14:17-21 (“These embodiments employ ***reference cells*** which substantially track changes in operating characteristics of the memory cell (and thus its bit line signal) with changing conditions that

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divisional applications do not render a patent ineligible for § 121 protection so long as the patent descended from a divisional application filed as a result of a restriction requirement. *Amgen*, 580 F.3d at 1354; *Boehringer*, 592 F.3d at 1352. Neither case says anything about an intervening continuation-in-part application, which, unlike an intervening continuation or divisional, adds new subject matter. Thus, neither case dealt with the scenario here, where the ’851 reference patent contains new material that was not included in either the ’816 restricted application or the ’571 challenged patent.

affect the operating characteristics, such as temperature, system voltages, or mere passage of time."). Thus, MLC could not have pursued all the claims of the '851 patent in the '816 Application.[26] *See, e.g., Boehringer*, 592 F.3d at 1352-53; *see also id.* at 1353 (holding that the "as a result of" requirement means that "but for the restriction requirement, [the applicant] could have pursued all the claims of the [divisional application] in the [original] application").

Because the '851 patent claims priority via a continuation-in-part and discloses and claims new matter, it cannot have issued "as a result of" the restriction requirement.

b. The '851 Patent Does Not Claim Priority to the '816 Restricted Application

Another reason the '851 patent does not have the benefit of the safe harbor is readily apparent from the face of the '851 patent: it does not contain a specific reference of priority to the '816 application, in which the restriction requirement was issued. Therefore, it cannot claim the benefit of the § 121 safe harbor. *See* 35 U.S.C. §§ 120, 121.

The second sentence of § 121 provides that if a restricted-out "invention is made the subject of a divisional application ***which complies with the requirements of*** *section 120* of this title it shall be entitled to the benefit of the filing date of the original application." 35 U.S.C. § 121 (emphasis added). Section 120, in turn, provides that a patent application claiming the benefit of an earlier filed application must contain "***a specific reference***" to that earlier

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[26] If it were true that MLC could have pursued the '851 patent claims in the '816 application (*i.e.*, that the '851 patent claims do not have new matter as compared to the '816 application and its parent, the '569 patent, which was published on June 8, 1993), then all of the '851 patent claims would be indisputably invalid over the '569 patent under 35 U.S.C. § 102(b). On the other hand, because the '851 patent claims do have new matter compared to the '569 patent and '816 application, it is indisputable that MLC could not have pursued the claims of the '851 patent in the '816 application.

application, and that failure to do so will result in a ***waiver*** of the benefit of the earlier application:

> An application for patent for an invention disclosed in the manner provided by section 112(a) . . . in an application previously filed in the United States, . . . which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, as though filed on the date of the prior application, if filed before the patenting or abandonment of or termination of proceedings on the first application or on an application similarly entitled to the benefit of the filing date of the first application and ***if it contains or is amended to contain a specific reference to the earlier filed application.*** No application shall be entitled to the benefit of an earlier filed application under this section unless an amendment containing the specific reference to the earlier filed application is submitted at such time during the pendency of the application as required by the Director. ***The Director may consider the failure to submit such an amendment within that time period as a waiver of any benefit under this section***. . . .

35 U.S.C. § 120 (emphasis added). The Patent Office's rules echo this requirement, providing:

> (d) *Claims under 35 U.S.C. 120, 121, 365(c), or 386(c) for the benefit of a prior-filed nonprovisional application . . . .*
>
> (2) . . . [A]ny nonprovisional application . . . that claims the benefit of one or more prior-filed nonprovisional applications . . . must contain or be amended to contain ***a reference to each such prior-filed application, identifying it by application number (consisting of the series code and serial number)*** . . . . The reference also must identify the relationship of the applications, namely, whether the later-filed application is a continuation, divisional, or continuation-in-part of the prior-filed nonprovisional application . . . .

37 C.F.R. § 1.78(d) (emphasis added). Section 1.78(d) goes on to explain that "failure to timely submit the reference required by 35 U.S.C. 120 and paragraph (d)(2) of this section ***is considered a waiver of any benefit under 35 U.S.C.*** 120, ***121,*** 365(c), or 386(c) to the prior-filed application." *Id.* § 1.78(d)(3)(iii) (emphasis added); *see also Ex Parte Clifford L. Jordan,* No. 2011-007291, 2013 WL 4495949, at *3 (Patent Trial and Appeal Bd. Aug. 22, 2013) (finding that a patent applicant waived the benefit of § 121 by failing to timely submit the reference required by § 120).

Here, the undisputed facts show that the '851 patent application does not contain "a specific reference" to the '816 restricted application (or the '362 patent that issued from that application). Rather, the earliest application to which the '851 patent claims priority is the application for the '571 patent. This is shown by the '851 patent itself and the Patent Office's

Patent Application Information Retrieval (PAIR) website. *See* Ex. H and Ex. AA. Having failed to refer specifically to, or even attempt to claim priority to the '816 restricted application, the '851 patent cannot claim the benefit of the '816 application under § 121.

This result serves important policies. First, as the Federal Circuit has explained, there are "reasons for the required precision" of § 120:

> The patentee is the person best suited to understand the genealogy and relationship of her applications; a requirement for her to clearly disclose this information should present no hardship. . . . Allocating the responsibility of disclosure through specific references to the patentee eliminates the inefficiencies associated with having the public expend efforts to unearth information when such information is readily available to the patentee.

Medtronic CoreValve, LLC v. Edwards Lifesciences Corp., 741 F.3d 1359, 1366 (Fed. Cir. 2014) (citations omitted). Second, a different result here could lead to abuse of the patent system, as this case vividly illustrates. If the '851 patent had claimed priority to the '816 restricted application, it would have expired on June 4, 2013—20 years after the filing date of the '816 application. And if the '851 patent had claimed priority to the very first application filed on February 8, 1991, any potential patent term would have expired before the '851 patent ever issued on March 22, 2011. By claiming priority only to the '571 patent, MLC was able to obtain a patent that did not expire until February 27, 2015, obtaining almost four full years of extra patent term.[27] Having avoided the downsides of claiming priority to the earlier '816 restricted application, MLC must also forfeit the benefits under § 121.

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[27] Notably, an earlier expiration date for the '851 patent also would have had implications for the '571 patent—at least, that is, if MLC had properly monitored its portfolio and filed a terminal disclaimer to avoid invalidity of the '571 patent based on OTDP. In particular, an earlier expiration date for the '851 patent would have meant MLC would have had to disclaim an even greater portion of the term of the '571 patent to avoid OTDP.

For each of the above reasons, the ’851 patent was not filed “as a result of” the restriction requirement in the ’816 application and thus does not qualify for the § 121 safe harbor.

(ii) The ’571 Patent Also Does Not Qualify for the § 121 Safe Harbor

a. The ’571 Patent Was Not Filed “As a Result” of the Restriction Requirement in the ’816 Restricted Application

The safe harbor provision requires the patent being challenged, here the ’571 patent, to have issued from an application filed “as a result of” the same restriction as the reference patent. *Boehringer,* 592 F.3d at 1352 (“We have repeatedly held that the ‘as a result of’ requirement applies to the challenged patent as well as the reference patent.”); 35 U.S.C. § 121. Thus, for a challenged divisional patent to qualify for the § 121 safe harbor, it must also contain claims that were restricted and removed from an earlier application and that reappear in the subsequent divisional application. *Geneva Pharm.*, 349 F.3d at 1379.

Like the ’851 patent discussed above, the ’571 patent does not meet this requirement. The restricted claims from the ’816 application—claim 37, directed to a “method of operation [of] a FET,” and claim 39, directed to a “device for the method of claim 39”—never reappeared during prosecution of the ’571 patent. Likewise, the claims of the ’571 patent did not appear in the ’816 application. Thus, just like the ’851 patent, the claims of the ’571 patent were not subject to the restriction requirement. *See id*. In fact, if the claims of the ’571 patent had been entered during prosecution of the ’816 application, they likely would not have been restricted out because they are most similar to the Group I claims that were selected for prosecution, as

illustrated by the table below.[28] Therefore, the application for the '571 patent was not filed "as a result of" the restriction requirement.

'816 Restricted App. Group I, Claim 31	'571 Challenged Patent Original Claim 1
31. An electrically alterable non-volatile multi-level memory device, comprising: a non-volatile, multi-level memory cell means for storing information for an indefinite period of time as a discrete state of said memory cell means, said memory cell means includes more than two memory states; and memory cell programming means for programming the memory state of said multi-level memory cell means to a pre-determined state corresponding to input information to be stored in said memory cell means; comparator means for comparing the memory state of said memory cell means with the input information to be stored in said memory and for generating a control signal indicative of the memory state of said memory cell; wherein said memory cell includes a gate which has an applied voltage being set to one of a plurality of voltage levels by said memory cell programming means corresponding to the input information.	1. A multi-level memory device comprising: a multi-level cell means for storing input information for an indefinite period of time as a discrete state of said multi-level cell means, said multi-level cell means storing information in K^n memory states, where K is a base of a predetermined number system and n is a number of bits stored per cell, wherein $K^n > 2$; programming means for programming said multi-level cell means to a memory state corresponding to said input information; comparator means for comparing said memory state of multi-level cell means with said input information, said input information corresponding to one of a plurality of reference voltages, said comparator means further generating a control signal indicative of said memory state as compared to said input information.

This analysis is not impacted by the fact that the '571 patent claims on its face to be a "division" of the '816 application. The "division" label does not signify that the '571 patent was

[28] The table below compares Group I claim 33 to the '571 patent claims as originally filed. Subsequent amendments to the claims did not bring the '571 patent claims any closer to introducing the Group II or III claims from the '816 application. *See generally* '571 Patent at Claims 1-47.

filed "as a result of" a restriction requirement. The PTO defines "divisional application . . . as '[a] later application for an independent or distinct invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in the earlier or parent application . . . .'" *Pfizer,* 518 F.3d at 1360 (quoting MPEP § 201.06). While "[a] divisional application 'is ***often*** filed as a result of a restriction requirement made by the examiner,'" *id.* (emphasis added), "a ***continuation application*** can satisfy the definition of a 'divisional application' in MPEP § 201.06" as well.[29] *Amgen*, 580 F.3d at 1353 (emphasis). The '571 patent is, at best, a continuation of the '816 restricted application.[30] The Patent Office never determined that the '571 patent was filed "as a result of" the restriction requirement in the '816 application, and the "division" label does not indicate otherwise. Rather, as shown above, the '571 patent was not filed "as a result of" a restriction requirement, so it does not qualify for the § 121 safe harbor.

b. The '571 Patent Is Not a Proper Divisional of the '816 Restricted Application

[29] The Patent Office tried to update its definition of "divisional application" to align with § 121 when it proposed a set of new rules in 2007. *See* 72 Fed. Reg. 46,716, 46,729 (Aug. 21, 2007) ("Section 1.78(a)(2) defines a 'divisional application' as a continuing application that discloses and claims only an invention or inventions that were disclosed and claimed in a prior-filed application, but were subject to . . . a requirement for restriction under 35 U.S.C. § 121 in the prior-filed application, and were not elected for examination and were not examined in any prior-filed application. This definition is more precise than the definition of 'divisional application' currently found in MPEP § 201.06."). However, the Patent Office later rescinded the new rules following litigation. *See Tafas v. Kappos*, 586 F.3d 1369, 1371 (Fed. Cir. 2009).

[30] Even this is being generous because, as discussed in the next section, the '571 patent is, in reality, a continuation-in-part of the '816 restricted application.

For § 121's safe harbor to apply, the '571 patent must be a divisional filed as a result of the restriction requirement. *See Amgen*, 580 F.3d at 1353–54 (explaining that a patent must ultimately descend from at least one divisional application to qualify for safe harbor protection); *Pfizer*, 518 F.3d at 1362 (stating that patents issuing from CIP applications cannot claim the benefit of the § 121 safe harbor). It is not. Although the face of the '571 patent states that it is a divisional of the '816 application, the evidence establishes that it is in fact a CIP.

The patentee originally filed the application leading to the '571 patent as a CIP, and later purported to amend the application so as to convert it to a divisional application. *See* Ex. AE ('571 Patent File History) at 1 (June 17, 1997 amendment). Yet that amendment was not effective—it did not entirely eliminate new matter from the '571 patent specification. *See* Ex. AB (Redline comparison between the '362 and '571 patent specifications). For example, the '571 patent introduces the concept of "programming and/or verifying programming of a multi-level NVM device with stable reference voltages." '571 Patent at Col. 1:17-21. The concept of "stable" reference voltages is not disclosed in the parent '362 patent. *See, e.g.*, Ex. O ('362 Patent) at Col. 1:11-14.

Furthermore, the patentee has acquiesced to labelling the '571 patent as a CIP. The first column of the '571 patent specification states that it is a CIP. *See* Ex. A ('571 Patent) at Col. 1:5-13; *see also* 37 C.F.R. 1.78(h) (for patents filed before September 16, 2012, claims of priority should be made in application data sheets or in "the first sentence(s) of the specification"). Likewise, the Patent Office's PAIR website confirms that the '571 patent is a CIP of the '816 application. *See* Ex. AC. Although MLC attempted to amend the first sentence of the specification to claim a divisional, it did nothing to correct these issues upon issuance of the patent. As the party "best suited to understand the genealogy and relationship" of the patent portfolio, MLC is responsible to ensure the public is on notice of its metes and bounds. *Medtronic,* 741 F.3d at 1366.

Even if the '571 patent issued as a divisional, it was originally filed as a CIP. The plain language of § 121 requires the filing of a ***divisional*** "before the issuance of the patent on the other application." The '571 patent's purported conversion to a divisional did not occur until July 1997—more than two years after the parent '362 restricted patent issued in February 1995. Thus, even if MLC's attempt to convert the '571 patent to a divisional was successful, it came too late to qualify for safe-harbor protection under the plain language of the statute. *Cf. G.D. Searle LLC,* 790 F.3d at 1355 (deleting new matter via reissue and designating reissue as a divisional did not retroactively alter the nature of an application filed as a CIP).

MLC further argued in support of its motion for summary judgment in the district court proceeding that there is no requirement that the challenged patent be a divisional. But this is in direct conflict with the Federal Circuit's ruling in *Pfizer*. Just like the '571 patent, the challenged patent in *Pfizer* was a continuation-in-part of the application in which a restriction requirement was made. The Federal Circuit held that the challenged patent was ineligible for the safe harbor because it was a CIP that disclosed new matter, not a divisional. *Pfizer*, 518 F.3d at 1362. In accordance with *Pfizer*, the reexamination unit should find that the '571 patent is not eligible for the safe harbor because it is not a divisional patent.[31] *See id.*

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[31] MLC may likely try to argue that *Pfizer* is distinguishable because the patentee in *Pfizer* did not file any divisional patents and thus the challenged continuation-in-part patent could never have descended from a divisional patent/application. This is false. The patentee in *Pfizer* did in fact file a divisional patent. The reference patent in *Pfizer*, U.S. Patent No. 5,563,165, was a divisional of the original application in which the restriction requirement was made. *See Pfizer*, 518 F.3d at 1357; U.S. Patent No. 5,563,165. Nevertheless, the court found that the safe harbor could not apply to *the challenged patent* because, like the '571 patent, it was a continuation-in-part of the original application in which the restriction requirement was made. *Id.* at 1362.

(iii) The ’571 and ’851 Patent Claims Violate the Consonance Requirement

In addition to the reasons above, the ’571 and ’851 patents also do not qualify for protection under § 121’s safe harbor because they both violate the consonance requirement of § 121. The consonance requirement is “[i]n addition to the express terms of section 121.” *Pfizer,* 518 F.3d at 1359. “The judicially-created consonance concept derives from the safe harbor’s ‘as a result of’ requirement and specifies that the ‘line of demarcation between the independent and distinct inventions that prompted the restriction requirement be maintained.’” *St. Jude Med.,* 729 F.3d at 1377 (quoting *Gerber Garment*, 916 F.2d at 688 (“Where that line is crossed the prohibition of the third sentence of Section 121 does not apply.”)). Further, “[p]lain common sense dictates that a divisional application filed as a result of a restriction requirement may not contain claims drawn to the invention set forth in the claims elected and prosecuted to patent in the parent application. The divisional application must have claims drawn only to the ‘other invention.’” *Gerber Garment*, 916 F.2d at 688. Therefore, “[c]onsonance in a case like this requires that the challenged patent, the reference patent, and the patent in which the restriction requirement was imposed (the restricted patent) do not claim any of the same inventions identified by the examiner.” *St. Jude Med.,* 729 F.3d at 1377.

Here, the ’571 patent fails the consonance requirement. MLC previously argued in support of its summary judgment motion in the co-pending litigation that the ’571 and ’362 Patents fall within the branch of the family tree covering an invention within Class 365, Subclass 189 (assigned to Group I by the restriction requirement), and that the ’571 Patent is directed to Group I (Class 365, Subclass 189). Because the ’571 patent and the ’362 patent (i.e., the restricted patent) both claim the same Group I invention, consonance is violated and the § 121 safe harbor cannot apply. *See St. Jude Med.,* 729 F.3d at 1377.

The ’851 patent claims fare no better in complying with the consonance requirement. As explained above, the claims of the ’851 patent rely on new matter added after the ’362 and ’571

patents. Thus, as a threshold matter, the '851 patent cannot possibly claim the non-elected inventions that were subject to a restriction requirement during prosecution of the '362 patent.

Even if that weren't the case, the Federal Circuit instructs that the "presence or absence of consonance will necessarily depend upon analysis of the involved claims." *Gerber Garment*, 916 F.2d at 688; *see also St. Jude Med.*, 729 F.3d at 1377. Even a rudimentary analysis reveals that the '851 patent's claims are most similar to Group I in the restriction requirement. The restriction requirement identified the following three groups of claims: a "memory system, classified in Class 365, subclass 189.07," a "method of operation [of] a FET, classified in Class 365, subclass 185," and a "FET Device, classified in Class 257, subclass 213." If the '851 patent were the "result of" this restriction requirement, the '851 claims would have been directed to a method of operation of a FET (as in claim 37 of the '816 application) or to a device for performing such a method (as in claim 39 of the '816 application). Instead, every claim in the '851 patent is directed to a "non-volatile memory apparatus." *See* '851 Patent at claims 1-15. The '851 patent contains no method claims. *Id.* The '851 claims are much more like the claims of the '571 patent, which are directed to alleged inventions such as "[a] multi-level memory device," "[a] multi-level memory apparatus," and an "[a]pparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states." *See, e.g.*, '571 Patent at claims 1, 9, 12, 30.

In lieu of actual analysis of the '571 or '851 patent claim terms, MLC previously relied in its summary judgment briefing ***solely*** on the classification codes of the patents—and those identified in the restriction requirement of the '816 application—to support its safe harbor defense. MLC cited no authority indicating that the USPTO's classification codes are relevant to a "consonance" analysis and the requester of the instant ex parte reexamination has found none. This novel theory cannot displace the "as a result of" and "consonance" tests applied by the Federal Circuit. As noted above, "[t]he presence or absence of consonance will necessarily

depend upon analysis of the involved claims." *Gerber Garment*, 916 F.2d at 688. MLC's motion wholly eschews any such analysis.

(iv) Policy Does Not Support the Use of the § 121 Safe Harbor to Protect the '571 Patent

"Because section 121 can extend the patent term for inventions that are not patentably distinct," the Federal Circuit applies a "strict test for application of § 121." *Boehringer,* 592 F.3d at 1356.

MLC and its predecessors engaged in an excessive prosecution campaign to generate an unduly large patent portfolio. Partway through generating this portfolio, BTG, MLC's predecessor in-interest to the '571 patent, severed the priority claim to the original '569 patent and '816 application (the application in which the original restriction requirement issued), thereby extending the statutory term of several patents, including the '851 patent. MLC cannot sever the priority claim to earlier applications to extend the life of the '851 patent and simultaneously claim the benefit of that same severed priority under the safe harbor provision.

As explained above, the '851 patent was not filed as a result of a restriction requirement in the '816 application. Rather, it was filed to claim new matter added in a subsequent application and to obtain a patent term extending several years beyond that which would have applied to any claims filed in the '816 application.

7. The Relevant Inquiry Is Whether the Claims of the ’571 Patent Are Patentably Indistinct from the Claims of the ’851 Patent, Not Vice Versa

Finally, Requester believes it is necessary to address one other argument Patent Owner MLC has made in the co-pending litigation regarding the proper application of the OTDP test. Specifically, MLC has argued at various times that Requester was required to apply either a two-way OTDP test or a reverse one-way test, and therefore, according to MLC, the relevant inquiry is whether the earlier-expiring ’851 patent claims are patentably indistinct from the claims of the ’571 patent. The district court is currently considering the issue of the proper direction of the OTDP test, and Requester anticipates that the district court will issue its decision in due course. In any event, to the extent MLC attempts to make such arguments in defense of an instituted *ex parte* reexamination, they should be rejected by the reexamination unit.Following controlling Federal Circuit precedent, Requester has correctly demonstrated invalidity of the ’571 patent by showing that the later-*expiring* ’571 patent claims are not patentably distinct from the earlier-*expiring* claims of the ’851 patent. *See Gilead*, 753 F.3d at 1217 (“[I]f it does indeed claim obvious variants of the invention claimed in the [earlier-expiring] patent, the [later-expiring] patent would violate the doctrine against double patenting.”); *see also Abbvie*, 764 F.3d at 1374 (“A later[-expiring] claim that is not patentably distinct from, *i.e.*, is obvious over or anticipated by, an earlier[-expiring] claim is invalid for obviousness-type double patenting.”) (original alterations omitted).

In the face of this controlling, modern case law, MLC premises its argument for a two-way or reverse one-way test evaluating whether the earlier-expiring ’851 patent claims are patentably indistinct from the claims of the ’571 patent on a misapplication of the *Borah*/*Calvert*/*Braat* line of cases. The Federal Circuit has addressed these cases by explaining that they addressed a “two-way” OTDP test that applies only in “unusual circumstances.” *In re Berg,* 140 F.3d 1428, 1432 (Fed. Cir. 1998). The Federal Circuit explained that “[t]he essential

concern [in *Braat*, *Borah*, and *Calvert*] was to prevent rejections for obviousness-type double patenting when the applicants filed first for a basic invention and later for an improvement, but, through no fault of the applicants, the PTO decided the applications in reverse order of filing." *Id*. The court further clarified that this "narrow exception to the general rule of the one-way test" applies only in the "unusual case" where (1) "the PTO is solely responsible for the delay in causing the second-filed application to issue prior to the first" and (2) "the two applications could not have been filed as one." *Id.* at 1432-37; *see also In re Hubbell*, 709 F.3d 1140, 1149-50 (Fed. Cir. 2013) (rejecting patent applicant's argument that the two-way test should apply). The "unusual circumstances" that led to the "narrow exception" described in *Borah*, *Calvert*, and *Braat* are plainly not present here. The '571 patent is an issued patent, not a pending application that was filed before, but decided after, a later-filed but earlier-issued application like in *Borah*, *Calvert*, and *Braat*. In fact, the application for the '851 patent was filed, through a long chain of applications, ***years*** after the filing and issuance of the '571 patent. *See* Ex. ??? at 6 (showing patent family tree). The order of filing and examination was a result of MLC's patent prosecution strategy, and not related to any PTO delay. Under the circumstances here, the PTO is not "***solely*** responsible for the delay in causing [a] second-filed application to issue prior to [a] first." *Eli Lilly & Co. v. Barr Labs., Inc.*, 251 F.3d 955, 969 n.7 (Fed. Cir. 2001) (finding that the two-way test did not apply); *see also Smith & Nephew, Inc. v. Arthrex, Inc.*, 355 F. App'x 384, 388 n.4 (Fed. Cir. 2009) ("We apply the one-way test for double patenting because the '557 patent came from multiple continuations-in-part, which means that the Patent and Trademark Office was not solely responsible for the delay in issuing the patent." (citing *Eli Lilly*, 251 F.3d at 969 n.7)). Moreover, although MLC has claimed in the co-pending litigation that the '851 patent is an "improvement" to the '571 patent, MLC has not argued that the invalidating claims of the '851 patent "could not have been filed as one" application with the '571 patent. For all of these reasons, the circumstances here do not remotely resemble the "unusual circumstances" required for the two-way test, and the one-way test Requester has applied above is the proper test and is

consistent with Federal Circuit precedent.MLC has further argued in the co-pending litigation that "***no court has ever compared patents in the direction Micron is proposing in this case***, *i.e.*, analyzing whether the patent with the earlier priority date is invalid in light of the patent with the later priority-date." *MLC v. Micron*, Case No. 3:14-cv-03657-SI, Dkt. No. 137 at 2 (June 1, 2017) (emphasis in original). However, that is exactly the type of comparison that was performed by the BPAI in *Ex Parte Pfizer, Inc.*, 2010 WL 532133 (BPAI Feb. 12, 2010). Significantly, the Federal Circuit and district courts have relied upon, and favorably cited, the BPAI's *Pfizer* decision and rationale. *See, e.g., Gilead Sciences, Inc. v. Natco Pharm. Ltd.*, 753 F.3d 1208, 1211 n.2 (Fed. Cir. 2014) (citing *Pfizer* and directly quoting the BPAI's reasoning); *Novartis Pharm. Corp. v. Breckenridge Pharm., Inc.*, 2017 WL 1278672, at *6 (D. Del. Apr. 3, 2017) (finding the BPAI's reasoning persuasive); *Janssen Biotech, Inc. v. Celltrion Healthcare Co.*, 210 F. Supp. 3d 278, 281 (D. Mass. 2016) (same). In *Pfizer*, the Board analyzed whether a later-expiring patent with an earlier priority date was invalid in light of an earlier-expiring patent with a later priority date—*i.e.*, the precise situation in this case. *Pfizer, Inc.*, 2010 WL 532133, at *25 (sustaining rejection of a claim of a patent filed on May 13, 1994 under obviousness-type double patenting over claims of patents filed on October 16, 1995). The Board found that the later-expiring pre-URAA patent (like the '571 patent here) would "extend the Appellant's right to exclude the public from practicing" the already-expired invention (like the '851 patent here). *Id*. at *21. This, the Board concluded, was "precisely what obviousness-type double patenting was intended to prevent." *Id*. The Federal Circuit, citing *Pfizer*, applied this same reasoning when reaffirming the "bedrock principle" of ensuring the public's free use of an invention (and obvious variants thereof) disclosed in an expired patent. *See Gilead*, 753 F.3d at 1214; *see also Abbvie*, 764 F.3d at 1374 ("We now make explicit what was implicit in *Gilead*: the doctrine of obviousness-type double patenting continues to apply where two patents that claim the same invention have different expiration dates."). Accordingly, the proper inquiry in the OTDP test is to determine whether the later-expiring claims of the '571 patent are patentably indistinct from

the earlier-expiring claims of the ’851 patent. Whether the earlier-expiring claims of the ’851 patent are patentably indistinct from the later-expiring claims of the ’851 patent is irrelevant for purposes of OTDP, and any such argument by MLC to the contrary should be rejected.

X. CONCLUSION

For the foregoing reasons, substantial new questions of patentability have been raised with respect to claims 1, 9, 12, 30, 42, and 45 of the ’571 patent. The references cited above render issued claims 1, 9, 12, 30, 42, and 45 of the ’571 patent unpatentable under 35 U.S.C. § 103(a) and for obviousness-type double patenting. Reexamination of issued claims 1, 9, 12, 30, 42, and 45 is hereby requested.

Respectfully submitted,

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