UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BROADCOM LIMITED

Petitioners

v.

INVENSAS CORPORATION

Patent Owners

PETITION FOR *INTER PARTES* REVIEW OF

U.S. PATENT NO. 6,278,653

TABLE OF CONTENTS

LIST OF EXHIBITS

1001	U.S. Patent No. 6,278,653 (“the ‘653 Patent”)
1002	File History of U.S. Patent No. 6,278,653
1003	U.S. Patent No. 4,916,670 (“Suzuki”)
1004	Johnson, Howard W., *High-Speed Digital Design*. Englewood Cliffs, NJ: Prentice-Hall (1993). (“Johnson”)
1005	Prince, Betty, *Semiconductor Memories: A Handbook of Design, Manufacture, and Application*. New York, NY: John Wiley & Sons (1997). (“Prince”)
1006	Declaration of Dr. Jacob Baker

I. INTRODUCTION

Broadcom Limited (collectively, "Petitioner"), asks that the Board review the accompanying prior art and analysis, institute trial of *inter partes* review of claims 1-20 (the "Challenged Claims") of U.S. Patent No. 6,278,653 ("the '653 patent") (Ex. 1001), and render a final written decision finding the Challenged Claims unpatentable.

II. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the '653 patent is available for *inter partes* review. Petitioner is not barred or estopped from requesting review of the Challenged Claims on the grounds identified in this petition.

B. Challenge and Relief Requested

This petition requests a determination that claims 1-20 are unpatentable due to anticipation under 35 U.S.C. § 102 by U.S. Patent No. 4,916,670 ("Suzuki"), designated as Exhibit 1003. This petition also requests a determination that claims 2-3, 10-11, and 17-18 are unpatentable as obvious under 35 U.S.C. § 103 over Suzuki in view of Johnson (Exhibit 1004). This petition also requests a determination that claims 12 and 16 are unpatentable as obvious under 35 U.S.C. § 103 in view of Suzuki in combination with Prince (Exhibit 1005).

The following table summarizes the grounds for unpatentability set forth in detail in this petition:

Ground	’653 Claims	Basis
Ground 1	1-7 and 9-19	Anticipated by Suzuki
Ground 2	2-3, 10-11, and 17-18	Obvious over Suzuki in view of Johnson
Ground 3	12 and 16	Obvious over Suzuki in view of Prince

Suzuki discloses a self-timed random access memory (STRAM) device in the form of a chip, having a function of generating a write signal (pulse) within the chip in response to an external clock and an external write enable signal. (Ex. 1003 at 1:9-14.) Suzuki was filed on January 31, 1989, and thus is prior art under at least 35 U.S.C. § 102(b). (Ex. 1006, ¶ 17.)

Johnson, Howard W., *High-Speed Digital Design*. Englewood Cliffs, NJ: Prentice-Hall (1993) (“Johnson”) is a handbook for high-speed digital design. It is a combination of digital and analog circuit theory meant to help engineers who work with digital systems to shorten their product development cycles and fix high-speed design problems. Johnson is of practical use to digital logic designers and all those interested in digital design. Johnson was published in 1993 by PTR Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 07632. Therefore, Johnson is prior art under at least 35 U.S.C. § 102(b). (Ex. 1006, ¶ 18.)

Prince, Betty, *Semiconductor Memories: A Handbook of Design, Manufacture, and Application*. New York, NY: John Wiley & Sons (1997) ("Prince") is a handbook of design, manufacture, and applications of semiconductor memories. Prince provides a basic handbook of the various aspects of semiconductor memories including history, market, applications, technology, design, various product types, manufacturing, and testing. Prince was published in 1983, 1991, and 1995 by John Wiley & Sons, New York, NY 10158. Therefore, Prince is prior art under at least 35 U.S.C. § 102(b). (Ex. 1006, ¶ 19.)

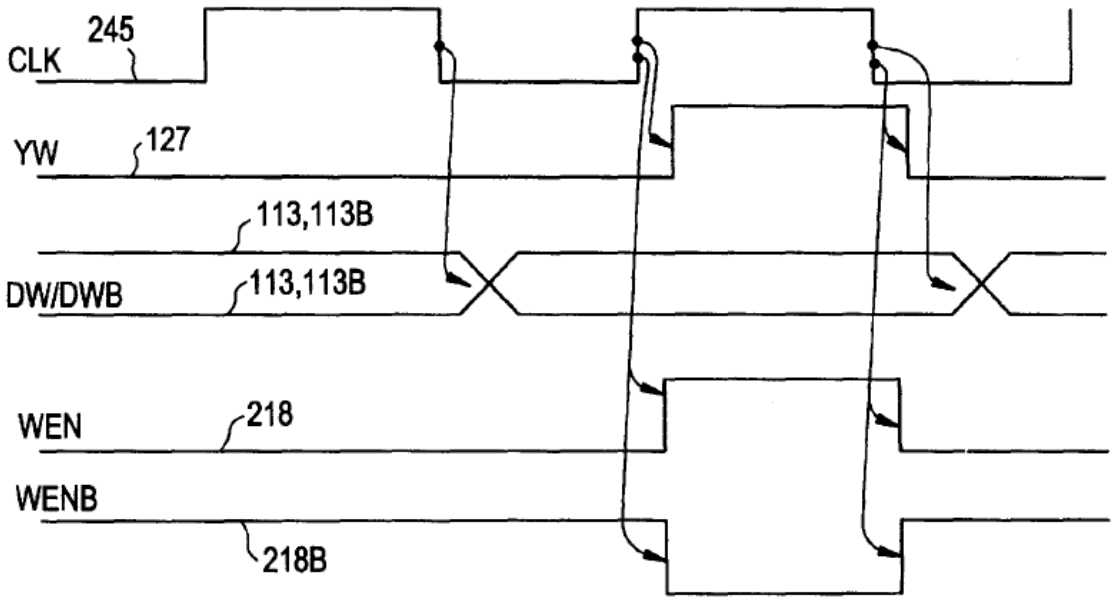
III. BACKGROUND

A. Overview of the '653 Patent

Generally, the '653 patent relates to a reduced skew write timing scheme for memory circuits where the signals present on the write data lines and the signals present on the write column select lines are clocked on opposite edges of the clock signal. (Ex. 1001 at 2:41-45.) As a result, the timing sensitivity during writing is relaxed. (Ex. 1001 at 2:45-46.) For example, signals present on write data lines can be clocked by the negative edge ("H"-to-"L" transition) of the clock signal, while signals present on a write column select line, along with the signals present on the write enable lines, can be clocked by the positive edge ("L"-to-"H" transition) of the clock signal. (Ex. 1001 at 2:47-52.) (Ex. 1006, ¶ 20.)

In a memory cell array architecture, the performance of the chip might be limited during a write operation due to a potential skew between the timing of the data signal written to a particular memory cell and the address signal present on a write column select line. (Ex. 1001 at 12:64-13:1.) For example, the global write data lines can extend laterally across the memory cell banks, while the column select lines can extend longitudinally through the sense amp bands. (Ex. 1001 at 13:5-8.) Accordingly, it is possible that the distances traveled by signals on those lines might be appreciably different and any consequential skew in the timing of those signals could limit performance of the circuit, particularly where the memory circuit is high speed. (Ex. 1001 at 13:8-11.) The performance of the circuit is limited because the write operation can only properly occur during the time overlap when the write enable control lines and the write column select line are active and the data on the data lines is valid. (Ex. 1001 at 13:11-16.) (Ex. 1006, ¶ 21.)

A timing diagram showing a timing scheme for writing data to storage locations in a memory circuit is illustrated in FIG. 12 of the ‘653 patent below. (Ex. 1006, ¶ 22.)



Ex. 1001 at FIG. 12

In write operations, global write data lines 113, 113B, which carry write data signals DW and DWB, respectively, are responsive to the negative edge of a clock signal 245, while write enable control lines 218, 218B, which carry write enable control signals WEN and WENB, respectively, and write column select line 127, which carries write column select signal YW, are responsive to the positive edge of the clock signal. (Ex. 1001 at 13:17-25.) This timing scheme relaxes the timing sensitivity during a writing operation. (Ex. 1001 at 13:25-26.) In particular, the timing is no longer dependent on the global write data lines 113, 113B. (Ex. 1001 at 13:26-28.) Rather, the critical timing is only between the write column select line 127 and write enable control lines 218, 218B. (Ex. 1001 at 13:28-30.) Because the signals YW, WEN and WENB on those lines are generated locally in

the same area of the array and because those lines all extend longitudinally through the sense amp band 118, any timing skew is minimal. (Ex. 1001 at 13:30-32.) This timing scheme is feasible because the duty cycle of clock 245 preferably is close to fifty percent, or at least within five percent thereof. (Ex. 1001 at 13:32-35.) (Ex. 1006, ¶ 23.)

B. Priority Date

The ’653 patent is a continuation-in-part of U.S. Application No. 09/644,928 filed on June 17, 2000. (Ex. 1006, ¶ 24.)

C. Prosecution History Summary of the ’653 Patent

Patent Owner filed the application that eventually issued as the ’653 patent, U.S. Application No. 09/644,928, with 20 claims on August 23, 2000. (Ex. 1003 at pp. 1-63.) The patent office issued a Notice of Allowance on February 27, 2001 (Ex. 1003 at pp. 64-68) and the ‘653 patent issued on August 21, 2001 (Ex. 1003 at cover page). No office actions were issued. No amendments were made. (Ex. 1006, ¶ 25.)

D. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the filing date of the ’653 patent would have been someone with at least an undergraduate degree in electrical engineering or similar field, and three to five years of industry experience in the field of memory circuit design. (Ex. 1006, ¶ 26.)

E. Claim Construction

In *inter partes* review, claim terms are interpreted under a "broadest reasonable construction" standard. *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1279 (Fed. Cir. 2016); *see* 37 C.F.R. §42.100(b). Under 37 C.F.R. § 1.42.104(b)(4), the "claim terms are presumed to take on their ordinary and customary meaning." *See* 77 Fed. Reg. 48699, 2012 WL 3276880, at *48700 (2012), Response to Comment 35. Unless otherwise addressed below, no express construction of any term is believed to be needed to resolve the challenges herein.

IV. FULL STATEMENT OF THE REASONS FOR THE RELIEF REQUESTED

A. Ground #1: Claims 1-20 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Suzuki.

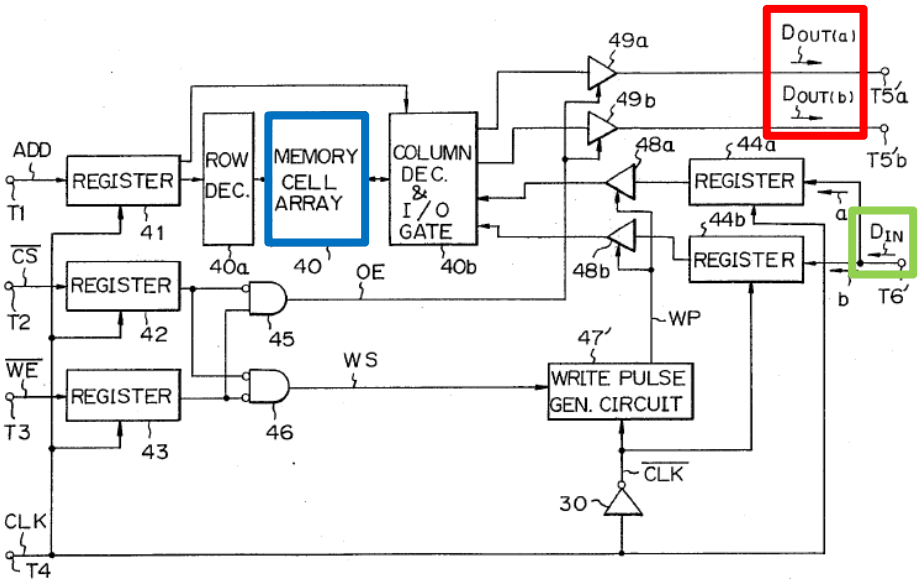
Suzuki discloses each and every element of claims 1-20 as described in this section. (Ex. 1006, ¶ 28.)

1. Claim 1 is unpatentable as anticipated by Suzuki

Claim 1(a)	
1(a) A method for processing data in a memory circuit, comprising the steps of:	Not limiting. Alternatively, Ex. 1003, FIG. 14; 2:31-34, 1:9-11, 6:62-63, 6:44-46, 12:64-13:13.

The preamble of claim 1 is not limiting. Alternatively, even if the preamble is found to be limiting, Suzuki discloses "a method for processing data in a memory circuit," namely "a semiconductor memory device" that processes data

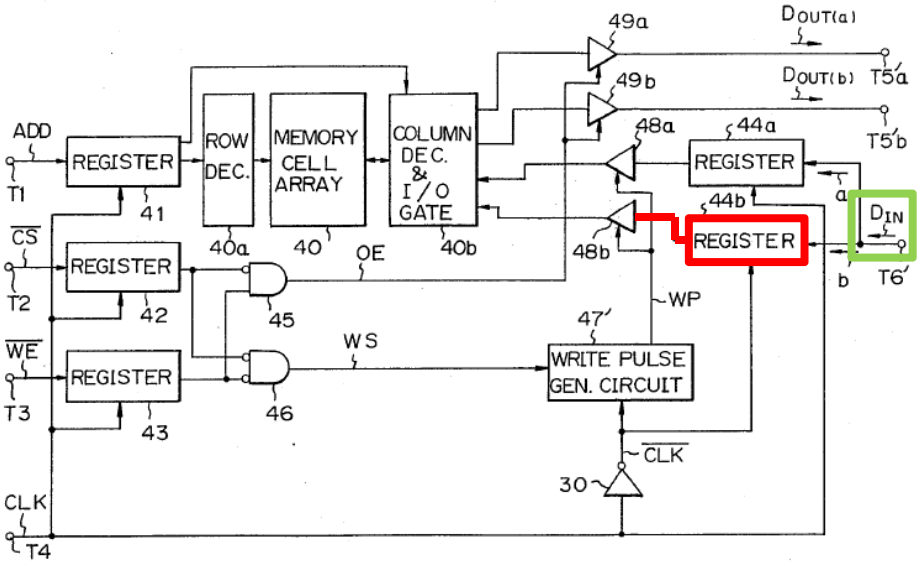
through "a data input terminal and a data output terminal." (Ex. 1003 at 2:31-34.1006) Specifically, Suzuki teaches "a self-timed random access memory (STRAM) device in the form of a chip." (Ex. 1003 at 1:9-11.) FIG. 14 of Suzuki reproduced below illustrates an embodiment of the STRAM. where "an ordinary static type memory cell array" (blue) (Ex. 1003 at 6:62-63) processes data by storing write data provided at an input terminal (green) (Ex. 1003 at 6:44-45) and retrieving data provided at output terminals (red) (Ex. 1003 at 6:45-46). Therefore, the STRAM "memory circuit" of Suzuki "processes data" as recited by the preamble of claim 1 by storing/retrieving data between the input and output terminals. (Ex. 1003 at 12:64-13:13.) (Ex. 1006, ¶¶ 29-30.)



Ex. 1003 at FIG. 14

Claim 1(b)	
1(b) generating a data signal;	Ex. 1003 at 6:44-45; 12:56-59; FIG. 14.

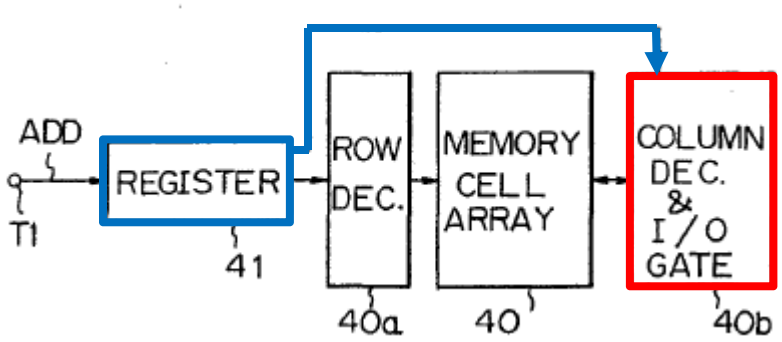
Suzuki generates a "data signal" on the output of register 44b. "[T]he inverted clock $\overline{CLK}$ is made 'H' level at a time of t_2, [and] data b is taken into the register 44*b* as the write data D_{IN} from the terminal T6'." (Ex. 1003 at 12:56-58.) FIG. 14 of Suzuki below shows the data signal on the output of register 44b. The input write data is received at the data input terminal T6' (green). (Ex. 1003 at 6:44-45.) The input "data b is taken into the register 44*b* as the write data D_{IN} from the terminal T6'." (Ex. 1003 at 12:58-59.) The output of the register 44b becomes "valid" at the rise of the CLK signal. (Ex. 1003 at 12:58-59.) Therefore, the output of the register 44b (red) functions as a generated "data signal" as recited by claim 1(b). (Ex. 1006, ¶¶ 31-32.)



Ex. 1003 at FIG. 14

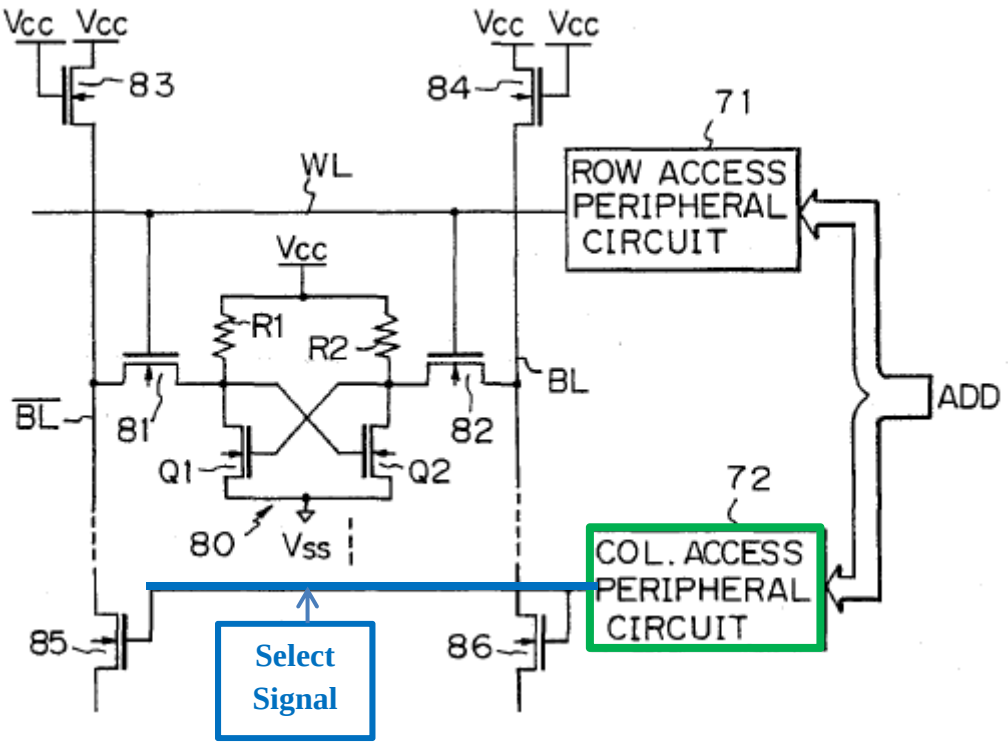
Claim 1(c)	
1(c) generating a select signal;	Ex. 1003 at 7:10-13; 6:66-7:2; 8:59-64; FIG. 7; FIG. 14.

Suzuki generates a "select signal" as the output of register 41 that selects a single memory cell in the memory cell array 40 for a write operation. "A register 41, connected between the terminal Tl and the row decoder 40*a* and column decoder and I/O gate 40*b*, has a function of latching the address signal ADD in response to the clock CLK." (Ex. 1003 at 7:10-13.) "[R]eference 40*b* denotes a column decoder and input/output (I/O) gate for selecting one of the pairs of bit lines based on the address signal." (Ex. 1003 at 6:66-7:2 (emphasis added).) Referencing the portion of FIG. 14 of Suzuki reproduced below, the output of register 41 (blue) is routed directly into the column decoder 40b (red) to select a column of memory cells in the memory cell array 40 for a write operation. (Ex. 1006, ¶ 33.)



Ex. 1003 at FIG. 14

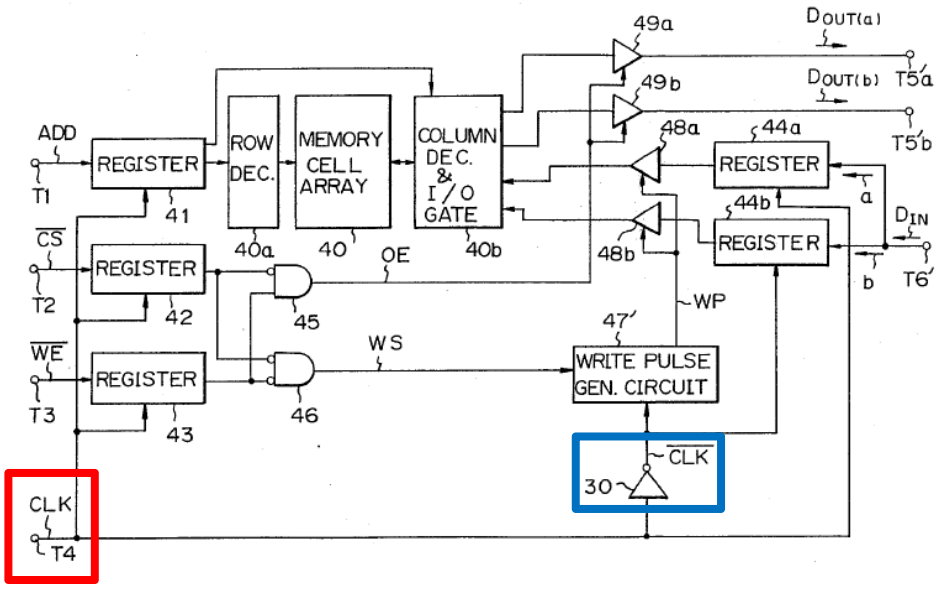
After entering the column decoder 40b, the address select signal is decoded to select individual bit lines for a memory operation. Referencing the portion of Suzuki FIG. 7 reproduced below, "reference 72 denotes a column access peripheral circuit for selecting one of the pairs of bit lines BL, $\overline{BL}$ in response to the address signal ADD." (Ex. 1003 at 8:61-64 (emphasis added).) After register 41 latches an ADD value on the rising clock edge, the ADD value is decoded by the column access peripheral circuit 72 (green) to generate an individual column select signal (blue) for each column in the memory array 40. Therefore, the column select signal (blue) that enables the bit line for each column functions as a generated "select signal" as recited by claim 1(c). (Ex. 1006, ¶¶ 34-35.)



Ex. 1003 at FIG. 7

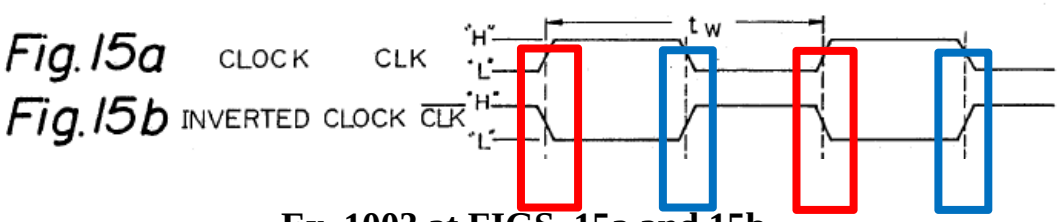
Claim 1(d)	
(d) generating a clock signal having a first transition wherein said clock signal moves from a first state to a second state distinct from said first state and a second transition wherein said clock signal moves from said second state to said first state;	Ex. 1003 at 2:49-51; 7:25-29; FIG. 14; FIG. 15.

Suzuki generates two "clock signals" that each meet this claim limitation. First, the T4 input of Suzuki generates a CLK signal from the T4 pin. "[T]here is provided a semiconductor memory device receiving an external clock having a rising edge and a falling edge." (Ex. 1003 at 2:49-51.) Second, a $\overline{\text{CLK}}$ signal is generated from the CLK signal. "An inverter 30, connected between the register 44 and the terminal T4, has a function of inverting the external clock CLK input from the terminal T4 and outputting an inverted clock $\overline{\text{CLK}}$." (Ex. 1003 at 7:25-29.) FIG. 14 of Suzuki below shows the CLK signal (red) and $\overline{\text{CLK}}$ signal (blue). (Ex. 1006, ¶ 36.)



Ex. 1003 at FIG. 14

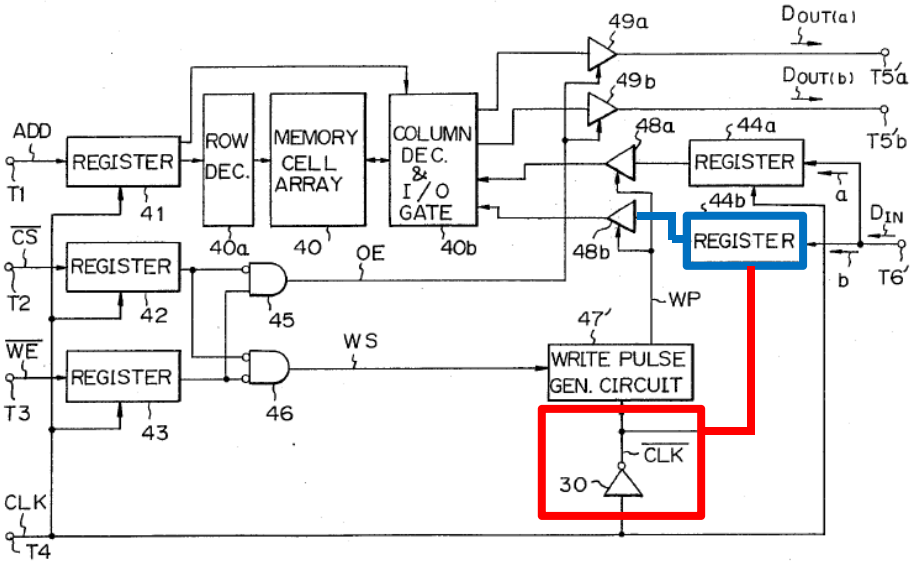
FIGS. 15a and 15b of Suzuki below show how the timing of the CLK signal and the $\overline{CLK}$ signal are synchronized and inverted. A first state ("H") of CLK corresponds to a first state ("L") of $\overline{CLK}$. A second state ("L") of CLK corresponds to a second state ("H") of $\overline{CLK}$. Therefore, the generated clock signal of claim 1(d) of the '653 patent corresponds to either CLK or $\overline{CLK}$ (being based on the same timing signal). The "first transition" (blue) is from the first state ("H") to the second state ("L") for CLK and from the first state ("L") to the second state ("H") for $\overline{CLK}$. Similarly, the "second transition" (red) is from the second state ("L") to the first state ("H") for CLK and from the second state ("H") to the first state ("L") for $\overline{CLK}$. (Ex. 1006, ¶¶ 37-38.)



Ex. 1003 at FIGS. 15a and 15b

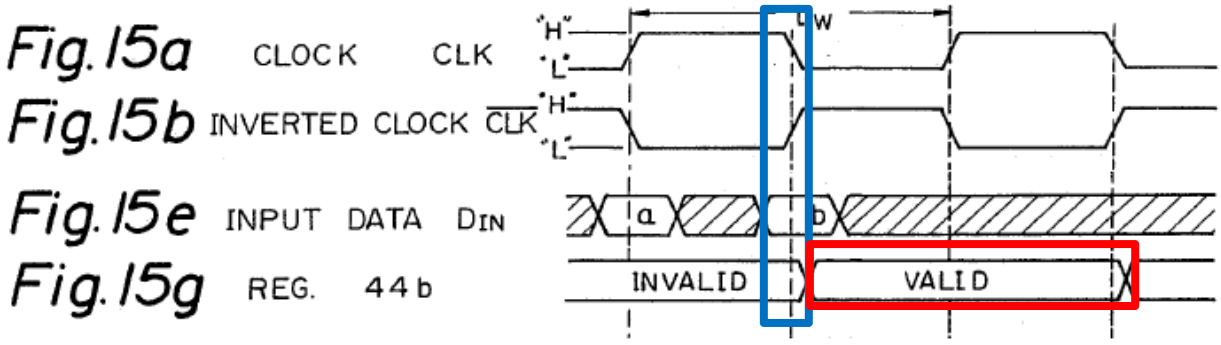
Claim 1(e)	
1(e) conditioning said data signal to be responsive to said first transition of said clock signal and to selectively become active upon the occurrence of said first transition;	Ex. 1003 at 12:56-59; FIG. 14; FIG.15.

The "data signal" output from register 44b of Suzuki identified above in claim 1(b) is conditioned to be responsive to the first transition, or falling edge, of the CLK signal (and the first transition, or rising edge, of the $\overline{CLK}$ signal) and to become active upon the occurrence of this first transition. "[T]he inverted clock $\overline{CLK}$ is made 'H' level at a time of t_2, data b is taken into the register 44*b* as the write data D_{IN} from the terminal T6'. Namely, the register 44*b* becomes 'valid.'" (Ex. 1003 at 12:56-59.) FIG. 14 of Suzuki below shows the data output of register 44b (blue) being activated by the first transition, the rising edge of the $\overline{CLK}$ signal (red) or falling edge of the CLK signal. (Ex. 1006, ¶ 39.)



Ex. 1003 at FIG. 14

Figures 15a, 15b, 15e, and 15g of Suzuki below show the data signal output of register 44b (red) becoming active/valid in response to the first transition (blue) the CLK and $\overline{\text{CLK}}$ signals. Therefore, the data signal output of register 44b is conditioned to be responsive to the first transition of the CLK signal and to selectively become active upon the occurrence of the first transition as recited by claim 1(e). (Ex. 1006, ¶¶ 40-41.)

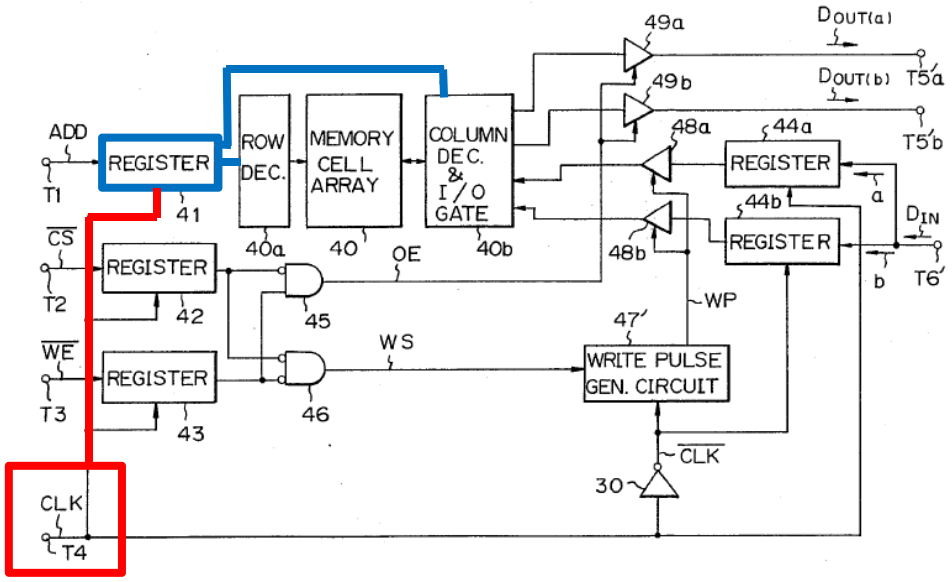


Ex. 1003 at FIG. 15

Claim 1(f)	
1(f) conditioning said select signal to be responsive to said second transition of said clock signal and to selectively become active upon the occurrence of said second transition.	Ex. 1003 at 7:10-13; FIG. 14.

The "select signal" from the column access peripheral circuit identified above in claim 1(c) is conditioned to be responsive to the second transition, or rising edge, of the CLK signal. "[R]egister 41, connected between the terminal T1 and the row decoder 40*a* and column decoder and I/O gate 40*b*, has a function of latching the address signal ADD in response to the clock CLK." (Ex. 1003 at 7:10-13.) FIG. 14 of Suzuki below shows the data output of register 41 (blue) being activated by the second transition, or rising edge, of the CLK signal (red). On the rising CLK edge, the ADD signal is asynchronously (without additional clock signals) fed through the column access peripheral to generate the individual column select line for each column. Therefore, the column select signal identified

above in claim 1(c) is conditioned to be responsive to the second transition of the CLK signal and to selectively become active upon the occurrence of the second transition as recited by claim 1(f). (Ex. 1006, ¶¶ 42-43.)

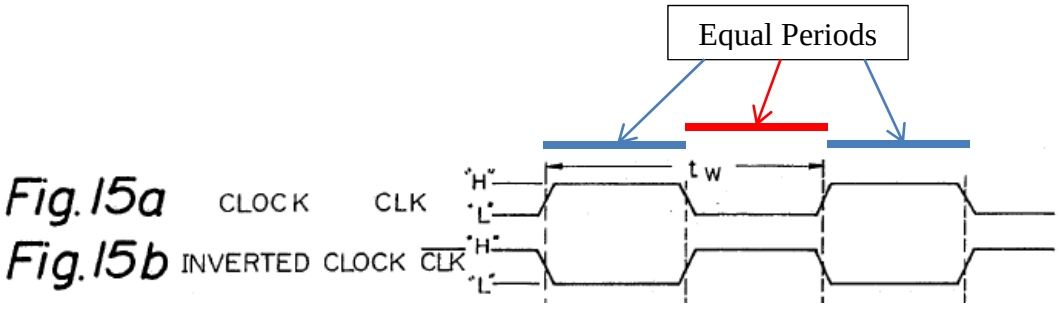


Ex. 1003 at FIG. 14

2. Claims 2 and 3 are unpatentable as anticipated by Suzuki.

Claim 2	
2. The method of claim 1 wherein said clock signal is conditioned to have between a forty-five percent duty cycle and a fifty-five percent duty cycle.	Ex. 1003 at FIG. 15a, FIG. 15b.
Claim 3	
3. The method of claim 1 wherein said clock signal is conditioned to have a fifty percent duty cycle.	Ex. 1003 at FIG. 15a, FIG. 15b.

As described above, Suzuki discloses all the elements of claim 1. Additionally, the CLK and $\overline{CLK}$ signals of Suzuki as shown by FIGS. 15a and 15b below have a fifty percent duty cycle as recited by claim 3 of the '653 patent. This is visually evident in FIGS. 15a and 15b, which shows the time between the H-to-L transitions being equal to the L-to-H transitions. Therefore, the CLK and $\overline{CLK}$ signals of Suzuki have the fifty percent duty cycle of claim 2. (Ex. 1006, ¶¶ 44-45.)



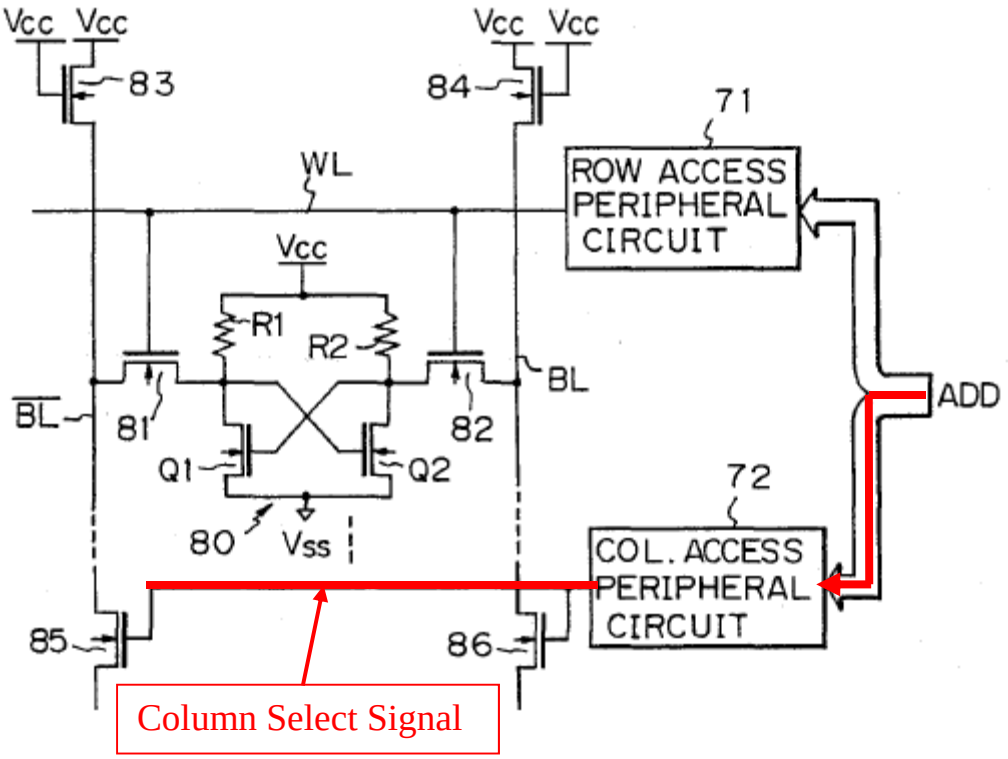
Ex. 1003 at FIGS. 15a and 15b

This fifty percent duty cycle of Suzuki also anticipates claim 2 of the '653 patent because the fifty percent duty cycle falls within the claimed forty-five percent to fifty-five percent duty cycle range of claim 2. (Ex. 1006, ¶¶ 46-47.)

3. Claim 4 is unpatentable as anticipated by Suzuki.

Claim 4	
4. The method of claim 1 wherein said select signal comprises a column select signal.	Ex. 1003 at 8:61-64; FIG. 7.

As described above, Suzuki discloses all the elements of claim 1. Additionally, the "select signal" identified above in claim 1(c) is routed from the address "ADD" stored in register 41 which is fed through the column access peripheral circuit 72 to generate a column select signal. "[R]eference 72 denotes a column access peripheral circuit for selecting one of the pairs of bit lines BL, $\overline{BL}$ in response to the address signal ADD." (Ex. 1003 at 8:61-64 (emphasis added).) FIG. 7 of Suzuki reproduced below illustrates the select signal functioning as a "column select signal" (red) as recited by claim 4. One of ordinary skill in the art would readily understand that the select line output from the column access peripheral circuit 72 is used to select a memory cell column in a memory array in the memory device. (Ex. 1006, ¶¶ 48-50.)



Ex. 1003 at FIG. 7

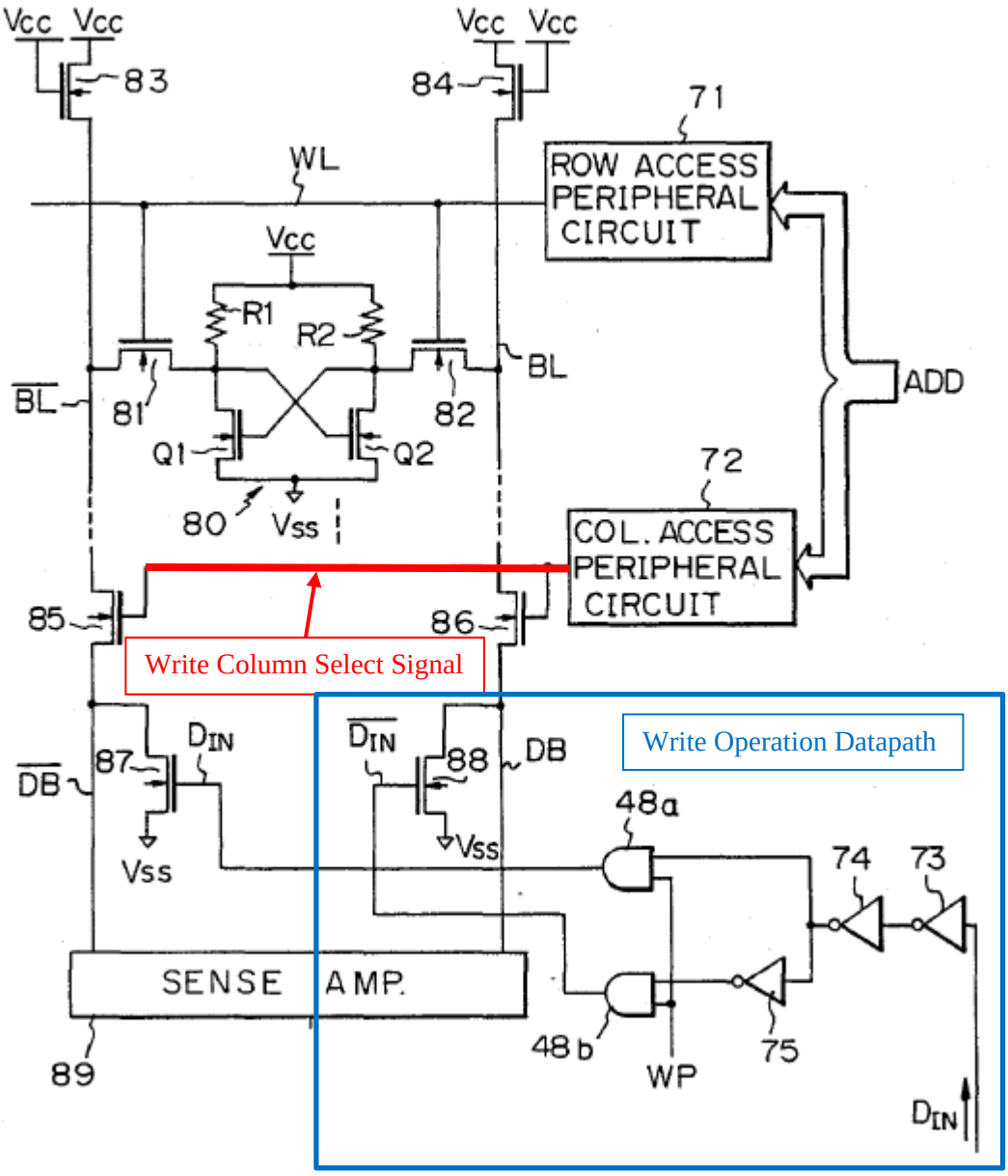
4. Claim 5 is unpatentable as anticipated by Suzuki.

Claim 5	
5. The method of claim 4 wherein said column select signal comprises a write column select signal.	Ex. 1003 at 9:9-18; FIG. 7.

As described above, Suzuki discloses all the elements of claim 4, including the column select signal. Additionally, the column select signal of Suzuki also functions as a "write column select signal" by selecting a particular column of the memory cell array during a write operation. "[T]ransistors 87 and 88 are connected to the data lines DB and $\overline{DB}$, respectively, which are turned ON in the data write operation. In this case, the write data D_{IN} input from the I/O terminal T5

is fed via an inverter 73, an inverter 74, and an AND gate 48a to the gate of the transistor 87 (gate signal D_{IN}), while the write data D_{IN} input from the I/O terminal T5 is fed via the inverter 73, the inverter 74, an inverter 75, and an AND gate 48b to the gate of the transistor 88 (gate signal $\overline{D}_{IN}$)." (Ex. 1003 at 9:9-18.) (Ex. 1006, ¶¶ 51.)

In the portion of FIG. 7 of Suzuki reproduced below, the write column select signal (red) selects the column of the memory cell as described above during a write operation on the write operation datapath (blue). One of ordinary skill in the art would readily understand that the column select line output from the column access peripheral circuit 72 is used to select a memory cell column in a memory array in the memory device during all write operations. Therefore, the column select signal of Suzuki functions a "write column select signal" as recited by claim 5. (Ex. 1006, ¶¶ 52-54.)

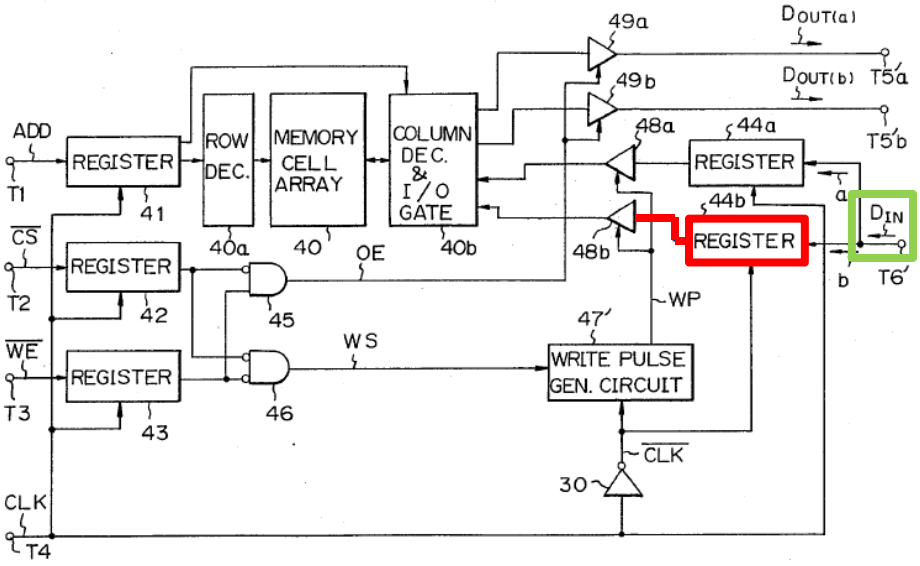


Ex. 1003 at FIG. 7

5. Claim 6 is unpatentable as anticipated by Suzuki.

Claim 6	
6. The method of claim 1 wherein said data signal comprises a write data signal.	Ex. 1003 at 12:56-13:3; FIG. 14.

As described above, Suzuki discloses all the elements of claim 1 of the '653 patent, including the data signal latched in register 44b identified in claim 1(b). Additionally, the data signal of Suzuki also functions as a "write data signal" by providing write data to the memory cell during a write operation. "[T]he inverted clock $\overline{CLK}$ is made 'H' level at a time of t_2, data b is taken into the register 44*b* as the write data D_{IN} from the terminal T6'. . . . When the 'H' level write pulse WP is generated, both the buffer 48*a* and the buffer 48*b* function, so that the data 'a' and 'b' latched in the registers 44*a* and 44*b*, respectively, are fed via the corresponding buffer and the column decoder and I/O gate 40*b* to the memory cell array 40. Namely, at this time, . . . data 'b' [is] . . . written into the memory cell array." (Ex. 1003 at 12:56-13:3 (emphasis added).) One of ordinary skill in the art would readily understand that the data signal of a memory is used for all write operations. The portion of FIG. 14 of Suzuki reproduced below illustrates the data signal (red) functioning as a "write data signal" as recited by claim 6 of the '653 patent by providing input data (green) to be written to the memory cell array 40. (Ex. 1006, ¶¶ 55-57.)



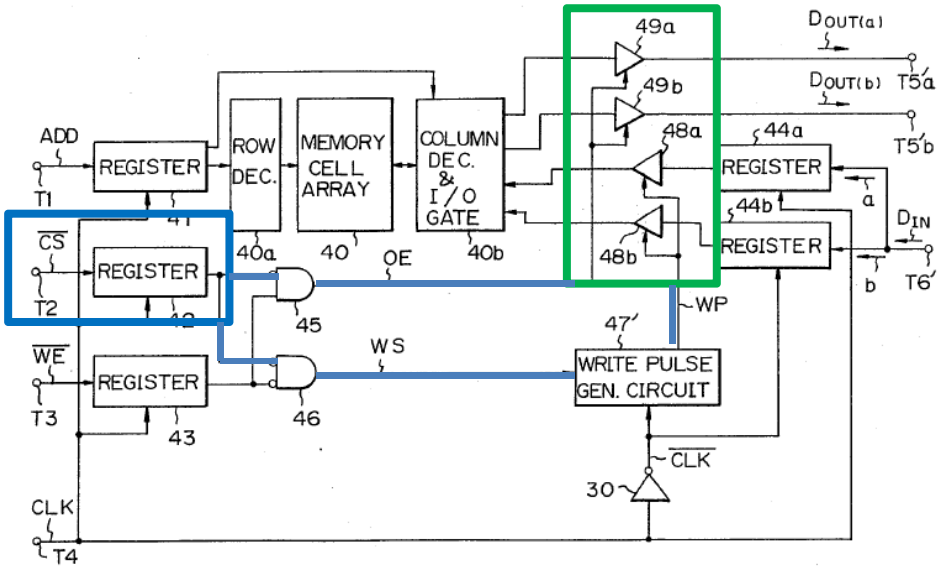
Ex. 1003 at FIG. 14

6. Claim 7 is unpatentable as anticipated by Suzuki.

Claim 7	
7. The method of claim 1 further comprising the step of generating an enable control signal selectively indicative of an enable state, and wherein said data is selectively processed only if said enable control signal indicates said enable state.	Ex. 1003 at 12:43-48; FIG. 14.

As described above, Suzuki discloses all the elements of claim 1 of the '653 patent. Additionally, Suzuki also discloses the $\overline{CS}$ signal that functions as an "enable control signal." For the $\overline{CS}$ signal, an "L" indicates an enable state where read/write operations are enabled. "First, a chip select signal CS of 'L' level is applied to the terminal T2. In this state, when the write enable signal $\overline{WE}$ of 'L' level is applied to the terminal T3 and the clock CLK is applied to the terminal T4,

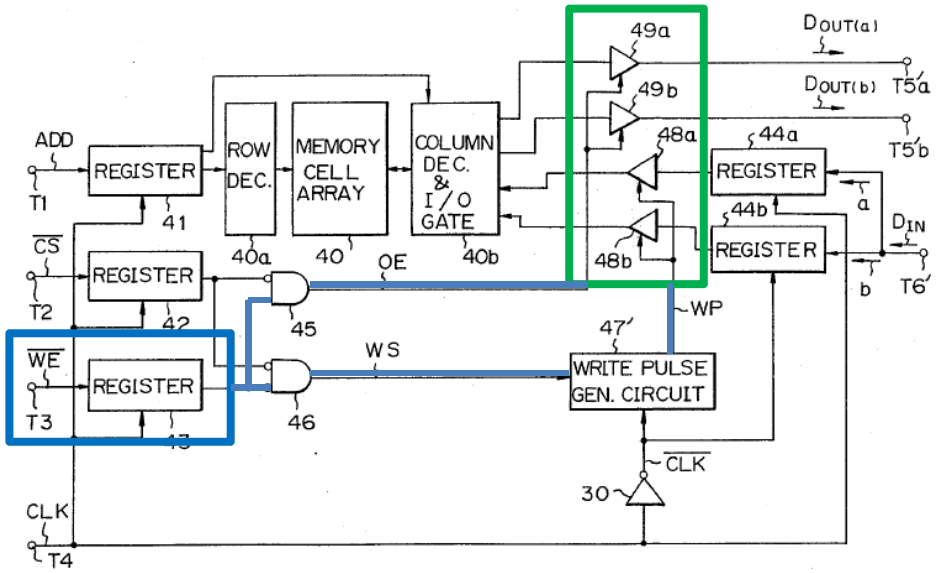
a write cycle t_w is defined in synchronization with the rising edge of the clock CLK." (Ex. 1003 at 12:43-48 (emphasis added).) Conversely, an "H" on the $\overline{CS}$ signal (blue) indicates a disabled state where read/write operations are disabled by forcing an "L" output on AND gates 45 and 46, which in turn disables output buffers 49a and 49b for read operations and the input buffer 48a and 48b (green) for write operations, as illustrated in FIG. 14 below of Suzuki. Therefore, the $\overline{CS}$ signal of Suzuki functions as the "enable control signal" recited by claim 7 of the '653 patent. (Ex. 1006, ¶ 58, ¶ 60.)



Ex. 1003 at FIG. 14

Alternatively, Suzuki also discloses the $\overline{WE}$ signal that functions as an "enable control signal." For the $\overline{WE}$ signal, an "L" initiates a write operation when the memory cell is enabled by the select signal from register 41. "[W]hen the write

enable signal $\overline{WE}$ of 'L' level is applied to the terminal T3 and the clock CLK is applied to the terminal T4, a write cycle t_w is defined in synchronization with the rising edge of the clock CLK." (Ex. 1003 at 12:43-48.) Referencing FIG. 14 of Suzuki below, the output of $\overline{WE}$ register 43 is an "enable control signal" (blue) that selectively allows data to be processed in read/write operations by enabling the input buffers 48*a* and 48*b* and/or output buffers 49*a* and 49*b* (green). Therefore, the output of the $\overline{WE}$ register 43 functions as the "enable control signal" of claim 7. (Ex. 1006, ¶¶ 59-60.)



Ex. 1003 at FIG. 14

7. Claims 8 and 20 are unpatentable as anticipated by Suzuki.

Claim 8	
8. The method of claim 1 wherein said first transition comprises a high-to-low transition and said second transition comprises a low-to-high transition.	Ex. 1003 at FIG. 15a.
Claim 20	
20. The method of claim 1 wherein said first transition comprises a high-to-low transition and said second transition comprises a low-to-high transition.	Ex. 1003 at FIG. 15a.

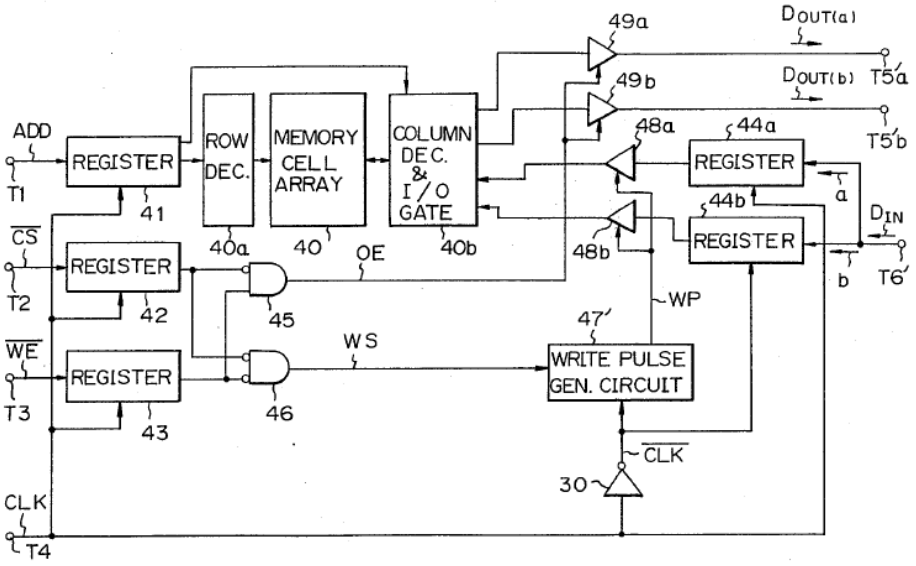
Claim 8 and claim 20 are duplicate claims dependent on claim 1. As described above, Suzuki discloses all the elements of claim 1 of the '653 patent. As also described above for claim 1(d), Suzuki discloses the CLK signal having a first transition that is a high-to-low transition and a second transition that is a low-to-high transition. FIG. 15a of Suzuki below shows the "first transition" (blue) from the first state ("H") to the second state ("L") for the CLK signal upon which the data signal becomes active in claim 1(e). Similarly, the "second transition" (red) is from the second state ("L") to the first state ("H") for the CLK signal upon which the select signal becomes active as described above in claim 1(f). Therefore, Suzuki discloses the first transition being a high-to-low transition and the second transition being a low-to-high transition as recited by claim 8 and claim 20. (Ex. 1006, ¶¶ 61-62.)

Ex. 1003 at FIG. 15a

8. Claim 9 is unpatentable as anticipated by Suzuki

Claim 9(a)	
9(a) A memory circuit, comprising:	Not limiting. Alternatively, Ex. 1003, at 1:9-11; 2:31-34; FIG. 14.

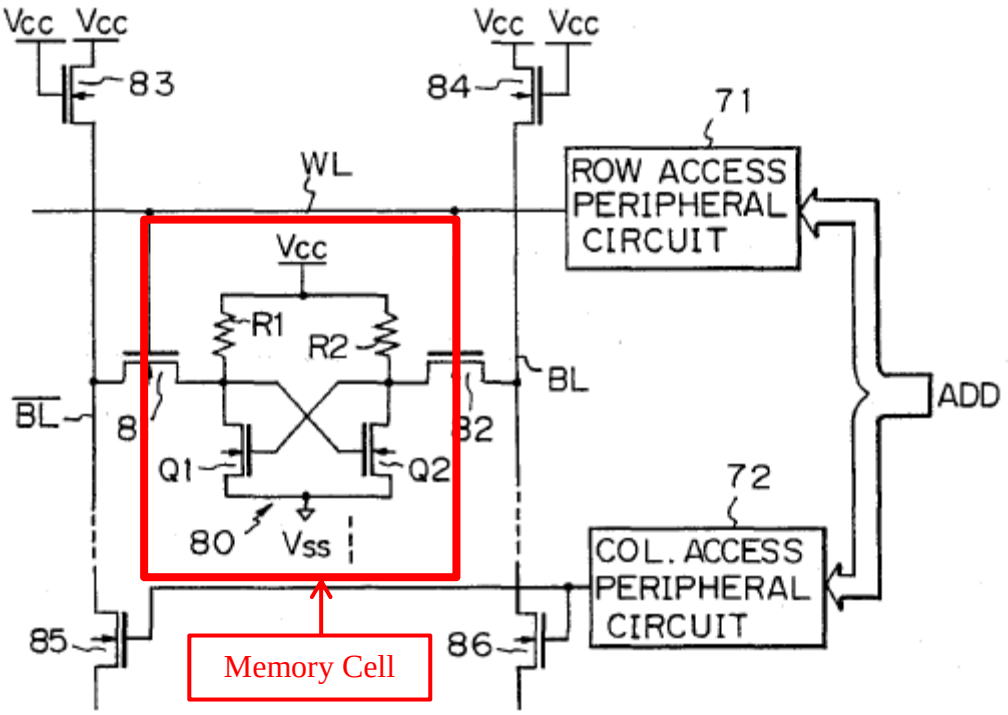
The preamble of claim 1 is not limiting. Alternatively, even if the preamble is found to be limiting, Suzuki discloses a ememory circuit, namely, a "semiconductor memory device." (Ex. 1003 at 2:31-34.) 1003Specifically, Suzuki teaches "a self-timed random access memory (STRAM) device in the form of a chip." (Ex. 1003 at 1:9-11.) FIG. 14 of Suzuki reproduced below illustrates an embodiment of the STRAM chip. Therefore, the circuit of FIG. 14 of Suzuki is a "memory circuit" as recited by claim 9(a). (Ex. 1006, ¶¶ 63-64.)



Ex. 1003 at FIG. 14

Claim 9(b)	
9(b) a memory cell;	Ex. 1003 at 6:62-65; 8:64-66; FIG. 7; FIG. 14.

The memory circuit of Suzuki FIG. 14 above includes an array of memory cells 40. "[R]eference 40 denotes an ordinary static type memory cell array having a memory cell provided at each intersection between a plurality of word. lines . . . and a plurality of pairs of bit lines." (Ex. 1003 at 6:62-65.) Specifically, with respect to the memory cell array 40, FIG. 7 of Suzuki, "reference 80 denotes a memory cell having a flip-flop structure comprising two drive transistors Q1, Q2 and two load [resistors] R1, T2." (Ex. 1003 at 8:64-66.) Therefore, the memory circuit of Suzuki includes a "memory cell" as recited by claim 9. (Ex. 1006, ¶¶ 65-66.)

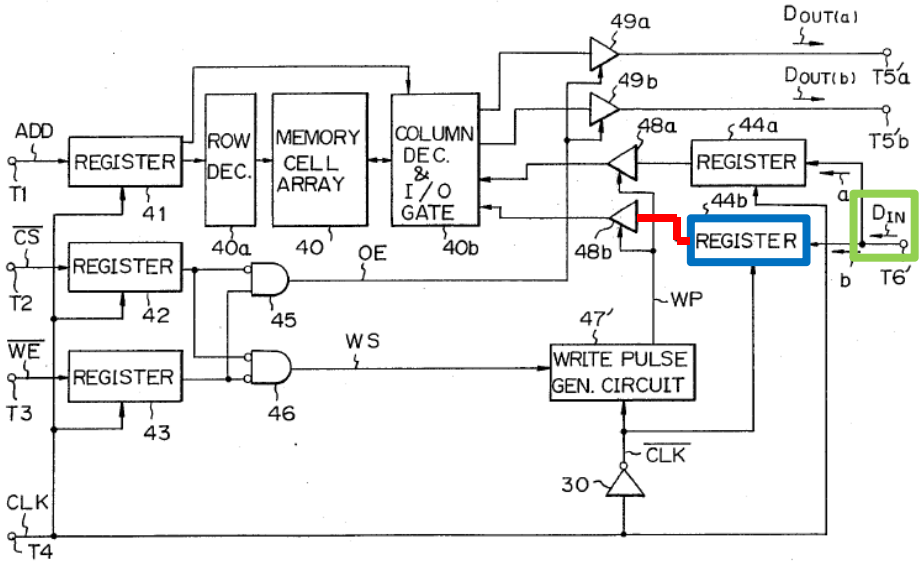


Ex. 1003 at FIG. 7

Claim 9(c)	
9(c) a data line associated with said memory cell and adapted to carry a data signal;	Ex. 1003 at 12:56-59; 6:44-45; 12:58-59; FIG. 14.

Suzuki generates a "data signal" on the output "data line" of register 44b. "[T]he inverted clock $\overline{CLK}$ is made 'H' level at a time of t_2, data b is taken into the register 44*b* as the write data D_{IN} from the terminal T6'." (Ex. 1003 at 12:56-58.) FIG. 14 of Suzuki below shows the data line (red) on the output of register 44b (blue) that carries the data signal stored in register 44b. This is a "data signal" because the input to register 44b is the D_{IN} data input terminal (green) of the memory device. (Ex. 1003 at 6:44-45.) "[D]ata b . . . is taken into the register 44*b*

as the write data D_{IN} from the terminal T6.'" (Ex. 1003 at 12:58-59 (emphasis added).) Therefore, this output line of register 44b is a "data line" associated with the memory cell 40, and adapted to carry a "data signal" as recited by claim 9. (Ex. 1006, ¶¶ 67-68.)

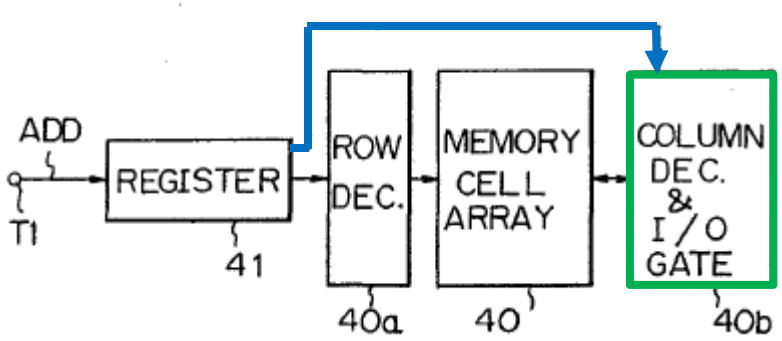


Ex. 1003 at FIG. 14

Claim 9(d)	
(d) a select line associated with said memory cell and adapted to carry a select signal for enabling said memory cell;	Ex. 1003 at 7:10-13; Ex. 1003 at 8:59-64; FIG. 7; FIG. 14.

Suzuki generates a "select signal" on the "select line" from the output of register 41 that enables a single memory cell in the memory cell array 40 for a write operation. "A register 41, connected between the terminal Tl and the row decoder 40*a* and column decoder and I/O gate 40*b*, has a function of latching the

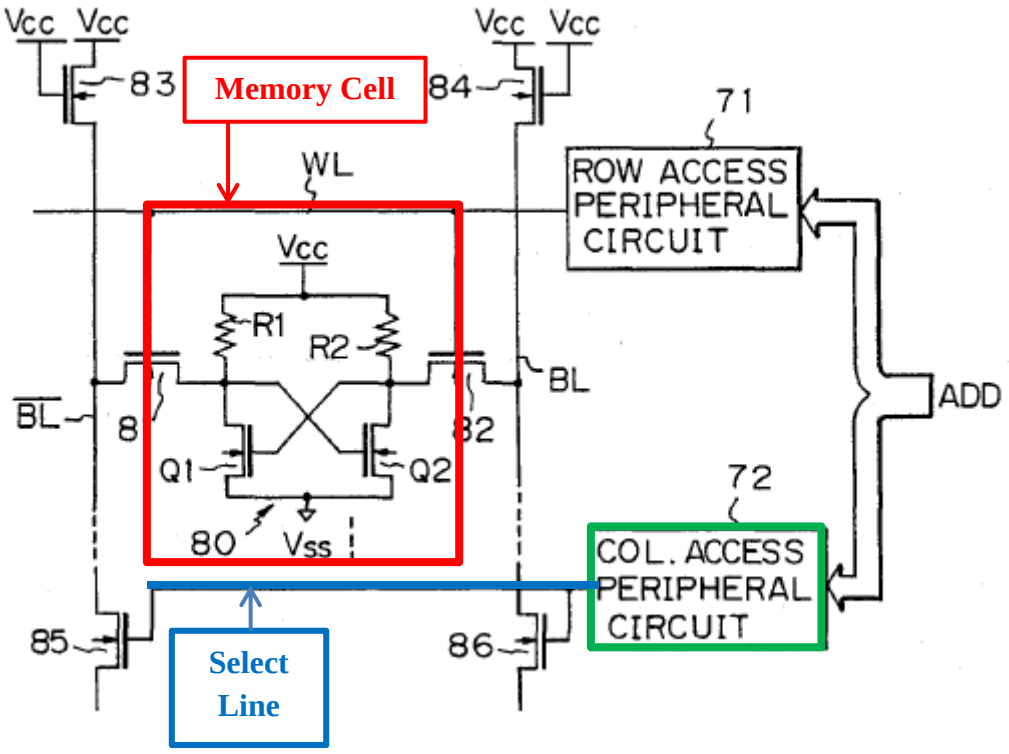
address signal ADD in response to the clock CLK." (Ex. 1003 at 7:10-13.) "[R]eference 40*b* denotes a column decoder and input/output (I/O) gate for selecting one of the pairs of bit lines based on the address signal." (Ex. 1003 at 6:66-7:2 (emphasis added).) Referencing the portion of FIG. 14 of Suzuki reproduced below, the "select line" is generated from the output line of register 41 (blue), which is routed directly into the column decoder 40b (green) to select and enable a single memory cell in the memory cell array 40 for a write operation. (Ex. 1006, ¶ 69.)



(Ex. 1003 at FIG. 14)

After entering the column decoder 40b, the address select signal is decoded to select individual bit lines for a memory operation. Referencing the portion of Suzuki FIG. 7 reproduced below, "reference 72 denotes a column access peripheral circuit for selecting one of the pairs of bit lines BL, $\overline{BL}$ in response to the address signal ADD." (Ex. 1003 at 8:61-64 (emphasis added).) After register 41 latches an ADD value on the rising clock edge, the ADD value is decoded by the column

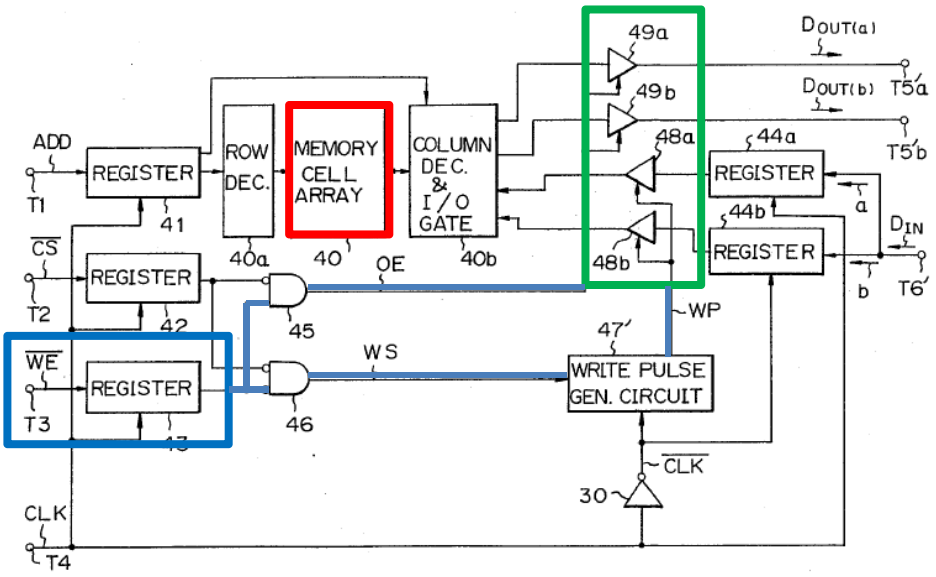
access peripheral circuit 72 (green) to generate an individual column select signal on a select line (blue) for each column in the memory array 40. Therefore, the "select line" (blue) associated with the "memory cell" 80 (red) carries a "select signal" that enables the "memory cell" 80 (red) as recited by claim 9(d). (Ex. 1006, ¶¶ 70-71.)



Ex. 1003 at FIG. 7

Claim 9(e)	
9(e) an enable control line associated with said memory cell and adapted to carry a control signal for selectively initiating an operation respecting said memory cell when said memory cell is enabled by said select signal;	Ex. 1003 at 12:43-48; FIG. 14.

Suzuki discloses the $\overline{WE}$ signal that functions as an "enable control signal." For the $\overline{WE}$ signal, an "L" initiates a write operation when the memory cell is enabled by the select signal from claim 9(d) above. "[W]hen the write enable signal $\overline{WE}$ of 'L' level is applied to the terminal T3 and the clock CLK is applied to the terminal T4, a write cycle t_w is defined in synchronization with the rising edge of the clock CLK." (Ex. 1003 at 12:43-48.) Referencing FIG. 14 of Suzuki below, the memory cell is enabled when the column select signal activates the bit lines as described in claim 9(d). Then, the output of $\overline{WE}$ register 43 acts as an "enable control line" (blue) associated with the memory cell 40 (red) that carries a control signal for initiating a write operation by enabling the input buffers 48*a* and 48*b* (green). Therefore, the output of the $\overline{WE}$ register 43 is an "enable control line" adapted for carrying a "control signal" for selectively "initiating" a write operation on the memory cell as recited by claim 9. (Ex. 1006, ¶¶ 72-73.)

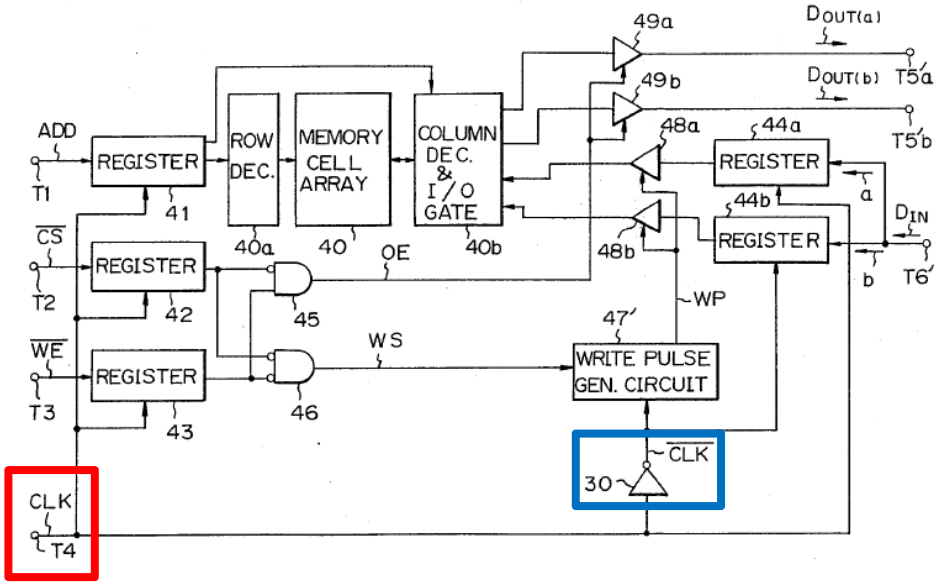


Ex. 1003 at FIG. 14

Claim 9(f)	
9(f) a clock line associated with said memory cell and adapted to carry a clock signal having a first transition wherein said clock signal moves from a first state to a second state distinct from said first state and a second transition wherein said clock signal moves from said second state to said first state; and	Ex. 1003 at 2:49-51; 7:25-29; FIG. 14; FIG. 15a; FIG. 15b.

Suzuki generates two "clock signals" each associated with a "clock line." First, the T4 input of Suzuki generates a CLK signal from the T4 pin on a clock line associated with the memory cell. "[T]here is provided a semiconductor memory device receiving an external clock having a rising edge and a falling edge." (Ex. 1003 at 2:49-51.) Second, a $\overline{CLK}$ signal is generated from the CLK signal on a clock line associated with the memory cell. "An inverter 30, connected

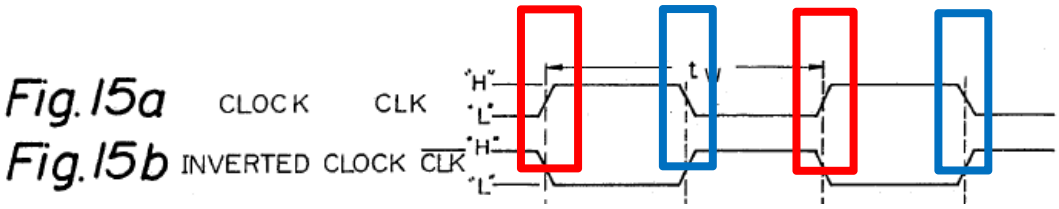
between the register 44 and the terminal T4, has a function of inverting the external clock CLK input from the terminal T4 and outputting an inverted clock $\overline{CLK}$." (Ex. 1003 at 7:25-29.) Figure 14 of Suzuki below shows the CLK signal (red) and $\overline{CLK}$ signal (blue). (Ex. 1006, ¶ 74.)



Ex. 1003 at FIG. 14

FIGS. 15a and 15b of Suzuki below show how the timing of the CLK signal and the $\overline{CLK}$ signal are synchronized and inverted. A first state ("H") of CLK corresponds to a first state ("L") of $\overline{CLK}$. A second state ("L") of CLK corresponds to a second state ("H") of $\overline{CLK}$. Therefore, the generated clock signal of claim 9(f) of the '653 patent corresponds to either CLK or $\overline{CLK}$ (being based on the same timing signal). The "first transition" (blue) is from the first state ("H") to the second state ("L") for CLK and from the first state ("L") to the second state ("H")

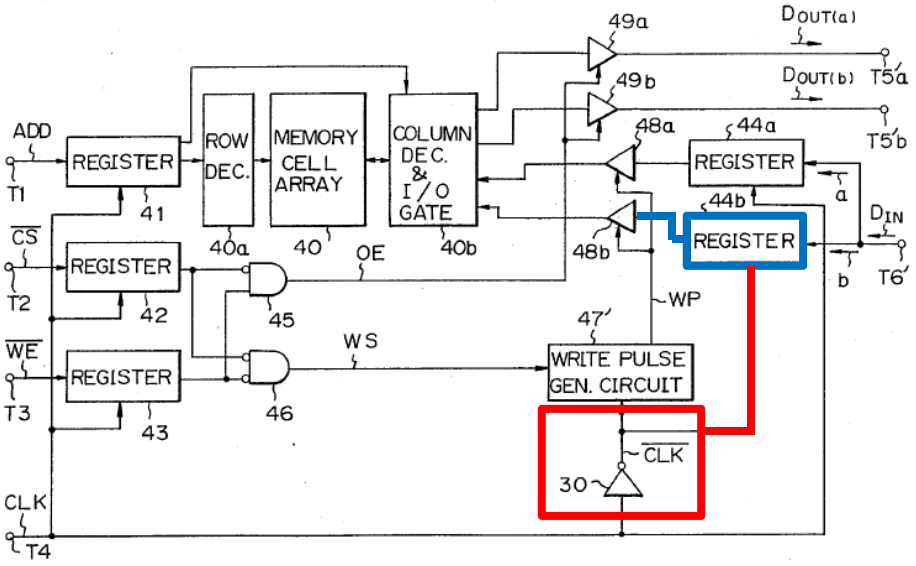
for $\overline{CLK}$. Similarly, the "second transition" (red) is from the second state ("L") to the first state ("H") for CLK and from the second state ("H") to the first state ("L") for $\overline{CLK}$. (Ex. 1006, ¶¶ 75-76.)



Ex. 1003 at FIGS. 15a and 15b

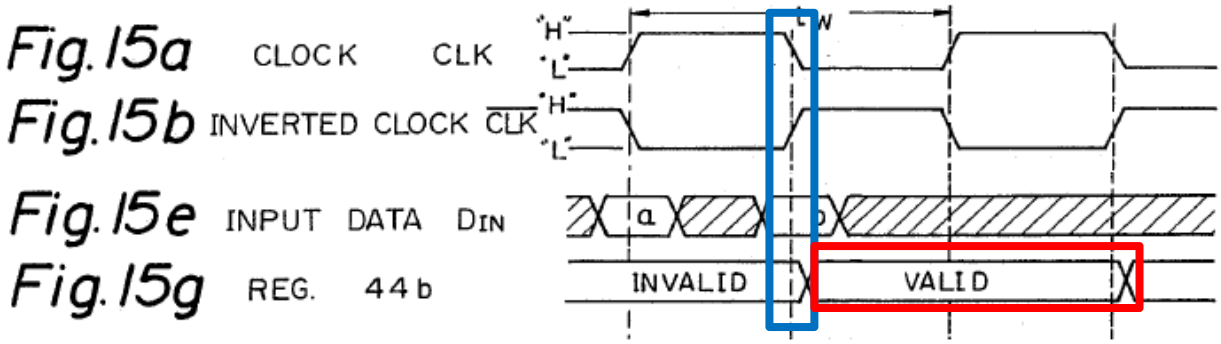
Claim 9(g)	
(g) wherein said data signal is conditioned to be responsive to said first transition of said clock signal and to selectively become active upon the occurrence of said first transition,	Ex. 1003 at 12:56-59; FIG. 14; FIG. 15a; FIG. 15; FIG. 15e; FIG. 15g.

The "data signal" output from register 44b of Suzuki identified above in claim 9(c) is conditioned to be responsive to the first transition, or falling edge, of the CLK signal (and the first transition, or rising edge, of the $\overline{CLK}$ signal). "[T]he inverted clock $\overline{CLK}$ is made 'H' level at a time of t_2, data b is taken into the register 44*b* as the write data D_{IN} from the terminal T6'. Namely, the register 44*b* becomes 'valid.'" (Ex. 1003 at 12:56-59.) FIG. 14 of Suzuki below shows the data output of register 44b (blue) being activated by the first transition, the rising edge of the $\overline{CLK}$ signal (red) or falling edge of the CLK signal. (Ex. 1006, ¶ 77.)



Ex. 1003 at FIG. 14

Figures 15a, 15b, 15e, and 15g of Suzuki below show the data signal output of register 44b (red) becoming active/valid in response to the first transition (blue) the CLK and $\overline{CLK}$ signals. Therefore, the data signal output of register 44b is conditioned to be responsive to the first transition of the CLK signal and to selectively become active upon the occurrence of the first transition as recited by claim 9(g). (Ex. 1006, ¶¶ 78-79.)



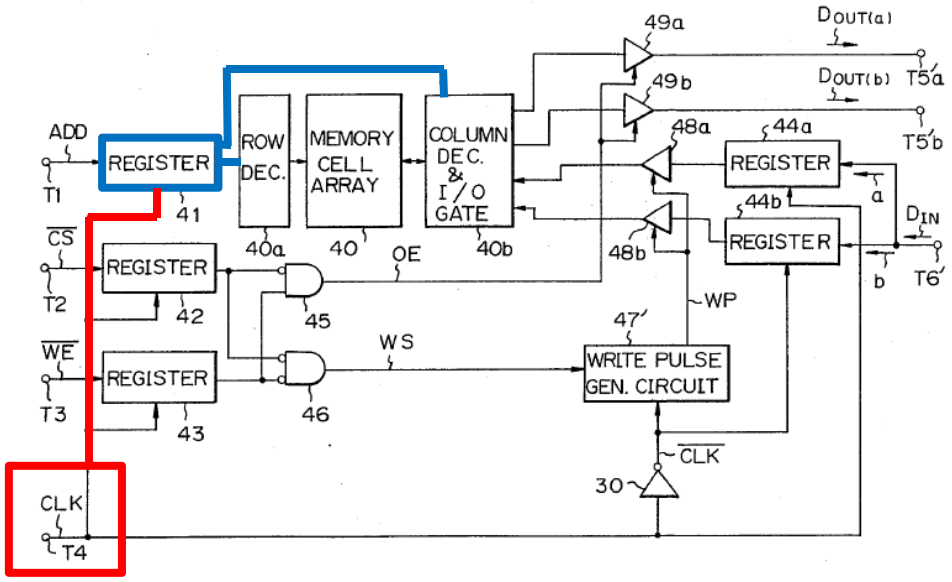
Ex. 1003 at FIG. 15

Claim 9(h)	
(h) and said column select signal is conditioned to be responsive to said second transition of said clock signal and to selectively become active upon the occurrence of said second transition	Ex. 1003 at 7:10-13; FIG. 14.

The "select signal[1]" from the column access peripheral circuit identified above in claim 9(d) is conditioned to be responsive to the second transition, or rising edge, of the CLK signal. "[R]egister 41, connected between the terminal T1 and the row decoder 40*a* and column decoder and I/O gate 40*b*, has a function of latching the address signal ADD in response to the clock CLK." (Ex. 1003 at 7:10-13 (emphasis added).) FIG. 14 of Suzuki below shows the data output of register 41 (blue) being activated by the second transition, or rising edge, of the CLK signal (red). On the rising CLK edge, the ADD signal is asynchronously (without additional clock signals) fed through the column access peripheral to generate the individual column select line for each column. Therefore, the column select signal

[1] Claim 9(h) includes an antecedent basis error by reciting "said column select signal" when only a "select signal" was previously introduced in claim 9(d). This error is further evident when claim 13 later recites "wherein . . . said select signal comprises a column select signal." Regardless, Suzuki's select signal also functions as a column select signal as described below in relation to claim 13.

identified above in claim 9(d) is conditioned to be responsive to the second transition of the CLK signal and to selectively become active upon the occurrence of the second transition as recited by claim 9(h). (Ex. 1006, ¶¶ 80-81.)



Ex. 1003 at FIG. 14

9. Claims 10 and 11 are unpatentable as anticipated by Suzuki.

Claim 10	
10. The memory circuit of claim 9 wherein said clock signal is conditioned to have between a forty-five percent duty cycle and a fifty-five percent duty cycle.	Ex. 1003 at FIG. 15a, FIG. 15b.
Claim 11	
11. The memory circuit of claim 9 wherein said clock signal is conditioned to have a fifty percent duty cycle.	Ex. 1003 at FIG. 15a, FIG. 15b.

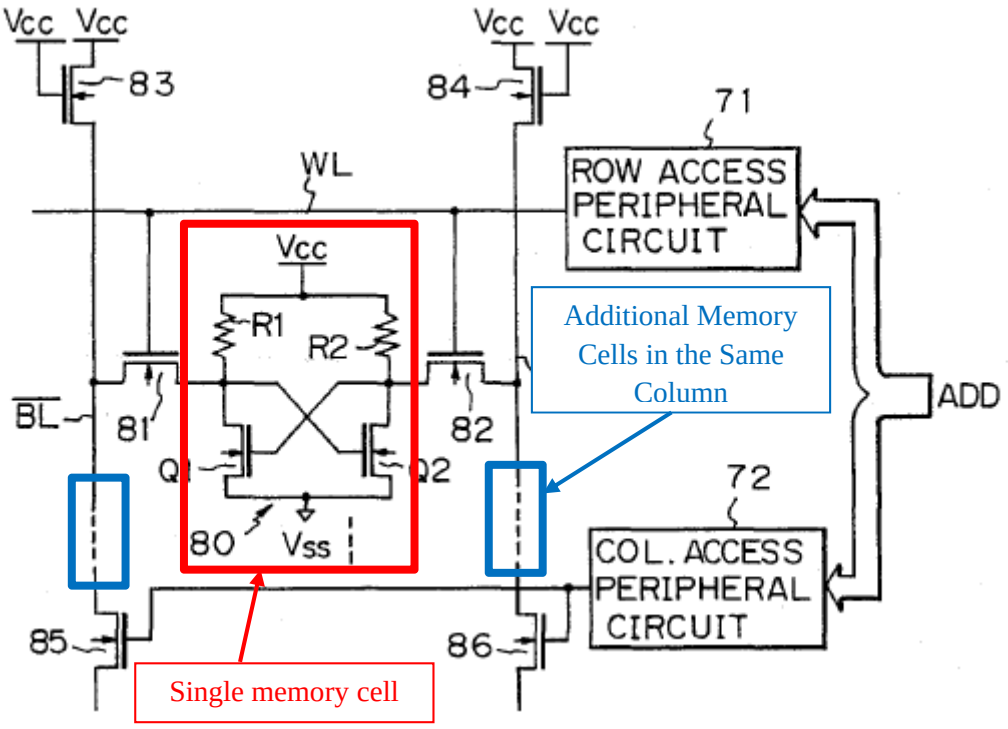
As described above, Suzuki discloses all the elements of claim 9. Suzuki also discloses a clock signal having between a forty-five percent duty cycle and a fifty-five percent duty cycle of claim 10 as described above for claim 2. Additionally, Suzuki discloses a clock signal having a fifty percent duty cycle as described above for claim 3. (Ex. 1006, ¶¶ 82-83.)

10. Claim 12 is unpatentable as anticipated by Suzuki.

Claim 12	
12. The memory circuit of claim 9 further comprising a plurality of additional memory cells all sharing a common column address with said memory cell.	Ex. 1003 at 8:55-58; 9:4-8; FIG. 7..

As described above, Suzuki discloses all the elements of claim 9. Additionally, FIG. 7 of Suzuki below shows an individual memory cell 80 (red) in the memory cell array 40 in FIG. 14 of Suzuki. However, "for simplification of the explanation, the illustration of FIG. 7 shows only the constitution corresponding to one column of the memory cell array." (Ex. 1003 at 8:55-58.) One of ordinary skill in the art would readily understand that the dashed lines (blue) in the memory column of FIG. 7 of Suzuki indicate omitted additional memory cells that are omitted "for simplification of explanation." (Ex. 1006, ¶ 84). One of ordinary skill in the art would also readily understand that the column/row selection circuitry would be meaningless without additional memory

cells in the column. (Ex. 1006, ¶ 85.) The additional memory cells in the column of the array indicated by the dashed lines (blue) share the same transistors 85 and 86 that are enabled by the same column address. (Ex. 1003 at 9:4-8.) Therefore, Suzuki discloses a plurality of additional memory cells sharing the same column address as recited by claim 12. (Ex. 1006, ¶¶ 84-86.)

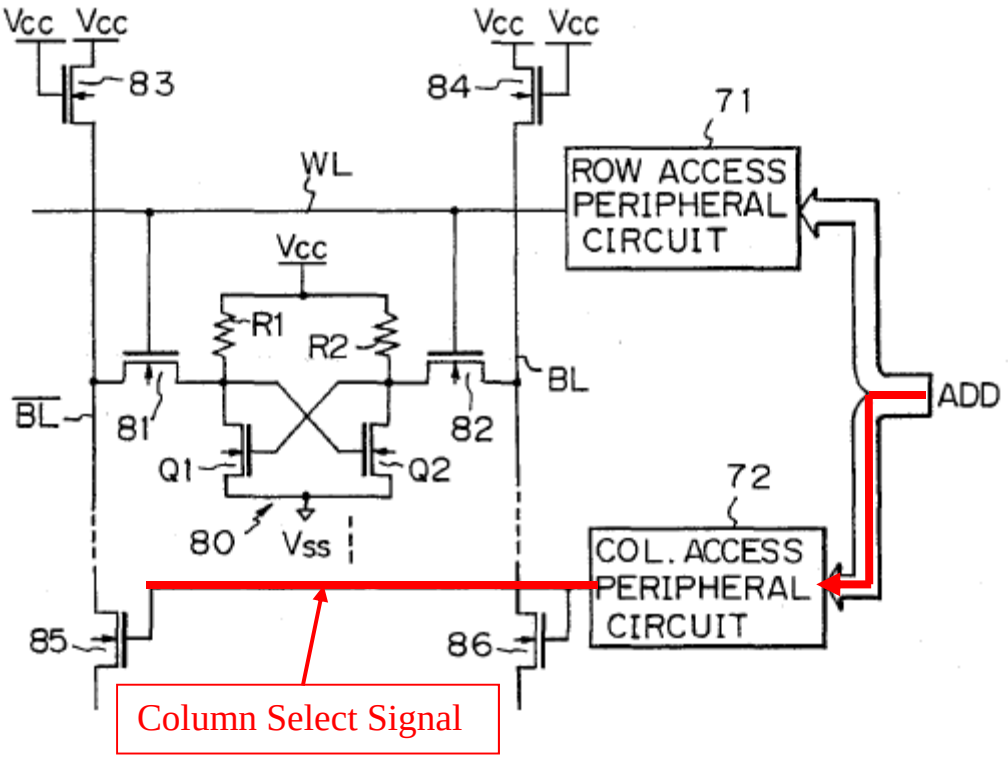


(Ex. 1003 at FIG. 7)

11. Claim 13 is unpatentable as anticipated by Suzuki.

Claim 13	
13. The memory circuit of claim 12 wherein said select line comprises a column select line, and said select signal comprises a column select signal.	Ex. 1003 at 8:61-64; FIG. 7.

As described above, Suzuki discloses all the elements of claim 12. Additionally, the "select signal" and the "select line" identified above in claim 9(d) is routed from the address "ADD" stored in register 41 which is fed through the column access peripheral circuit 72 to generate a column select signal. "[R]eference 72 denotes a column access peripheral circuit for selecting one of the pairs of bit lines BL, $\overline{BL}$ in response to the address signal ADD." (Ex. 1003 at 8:61-64 (emphasis added).) One of ordinary skill in the art would readily understand that the column select line is used to select a memory cell column in all read/write operations. (Ex. 1006, ¶ 88.) FIG. 7 of Suzuki reproduced below illustrates the select line functioning as a "column select line" (red) carrying a "column select signal" as recited by claim 13. (Ex. 1006, ¶¶ 87-89.)



Ex. 1003 at FIG. 7

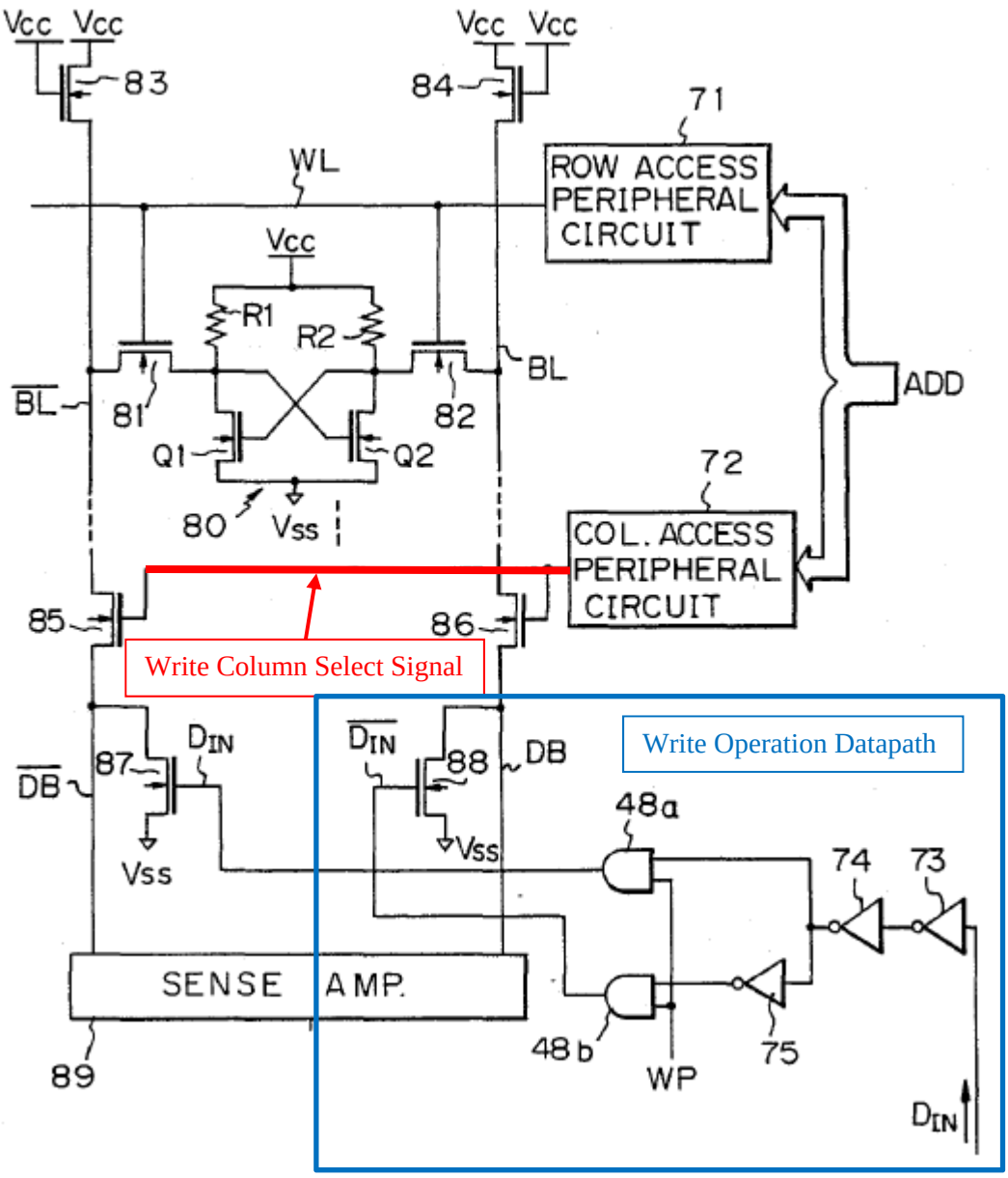
12. Claim 14 is unpatentable as anticipated by Suzuki.

Claim 14	
14. The memory circuit of claim 13 wherein said column select line comprises a write column select line, and said column select signal comprises a write column select signal.	Ex. 1003 at 9:9-18; FIG. 7.

As described above, Suzuki discloses all the elements of claim 13, including the column select line and column select signal. Additionally, the column select line of Suzuki also functions as a "write column select line" by selecting a particular column of the memory cell array during a write operation. "[T]ransistors 87 and 88 are connected to the data lines DB and $\overline{DB}$, respectively, which are

turned ON in the data write operation. In this case, the write data D_{IN} input from the I/O terminal T5 is fed via an inverter 73, an inverter 74, and an AND gate 48a to the gate of the transistor 87 (gate signal D_{IN}), while the write data D_{IN} input from the I/O terminal T5 is fed via the inverter 73, the inverter 74, an inverter 75, and an AND gate 48*b* to the gate of the transistor 88 (gate signal $\overline{D}_{IN}$)." (Ex. 1003 at 9:9-18.) One of ordinary skill in the art would readily understand that the column select line is used to select a memory cell column in all read/write operations. (Ex. 1006, ¶ 90-92.)

In the portion of FIG. 7 of Suzuki reproduced below, the write column select line (red) selects the column of the memory cell as described above during a write operation using the write operation datapath (blue). Therefore, the column select line of Suzuki functions a "write column select line " carrying a "write column select signal" as recited by claim 14. (Ex. 1006, ¶¶ 91-93.)



Ex. 1003 at FIG. 7

13.Claim 15 is unpatentable as anticipated by Suzuki.

Claim 15	
15. The memory circuit of claim 9 wherein said data line comprises a write data line, and said data signal comprises a write data signal.	Ex. 1003 at 12:56-13:3.

As described above, Suzuki discloses all the elements of claim 9, including the data signal latched in register 44b on an output data line. Additionally, the data signal of Suzuki also functions as a "write data signal" by providing write data to the memory cell during a write operation. "[T]he inverted clock $\overline{CLK}$ is made 'H' level at a time of t_2, data b is taken into the register 44*b* as the write data D_{IN} from the terminal T6'. . . . When the 'H' level write pulse WP is generated, both the buffer 48*a* and the buffer 48*b* function, so that the data 'a' and 'b' latched in the registers 44*a* and 44*b*, respectively, are fed via the corresponding buffer and the column decoder and I/O gate 40*b* to the memory cell array 40. Namely, at this time, both data 'a' and data 'b' are simultaneously written into the memory cell array." (Ex. 1003 at 12:56-13:3.) One of ordinary skill in the art would readily recognize that the data line of a memory is used for all write operations. (Ex. 1006, ¶ 95.) Therefore, the data line and the data signal of Suzuki function as a "write data line" and a "write data signal" as recited by claim 15. (Ex. 1006, ¶¶ 94-96.)

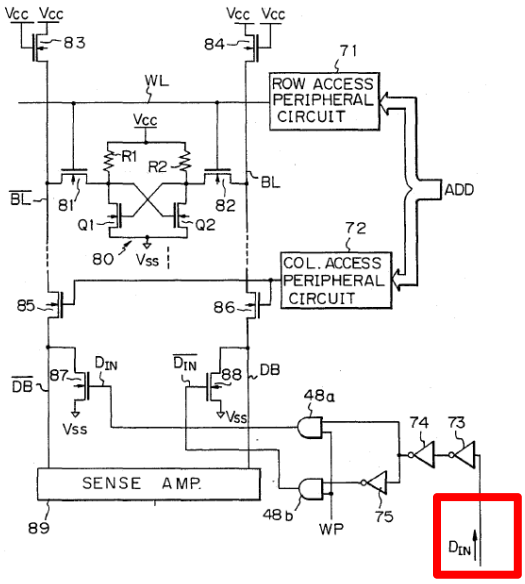
14. Claim 16 is unpatentable as anticipated by Suzuki

Claim 16(a)	
16(a) A method for writing data to memory cells in a circuit, comprising the steps of:	Not limiting. Alternatively, Ex. 1003, FIG. 14; 2:31-34, 1:9-11, 6:62-63, 6:44-46, 12:64-13:13.

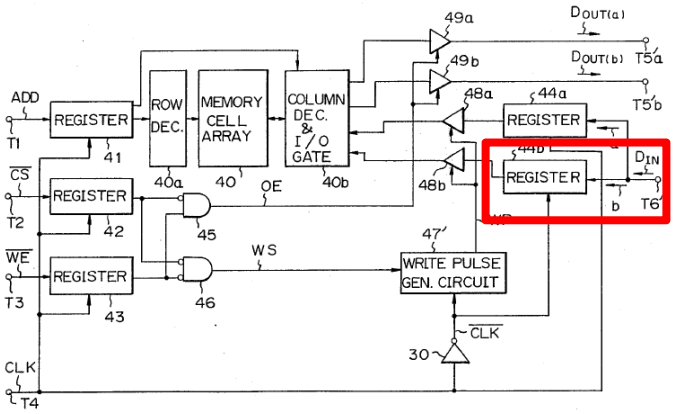
The preamble of claim 16 is not limiting as described above for claim 1(a). Alternatively, even if the preamble is found to be limiting, Suzuki discloses a "method for writing data to memory cells in a circuit" as also described above for claim 1(a). (Ex. 1006, ¶¶ 97-98.)

Claim 16(b)	
(b) generating a write data signal in a first area of said circuit;	Ex. 1003 at 12:56-13:3; 6:44-45; 12:58-59; FIG. 14.

Suzuki generates a "write data signal" on the output of register 44b as described above for claim 1(b) and claim 6. Additionally, the write data signal is generated in a "first area" (red) of Suzuki's memory circuit as shown at the gate/transistor level in FIG. 7 below (left), as well as at the block level in FIG. 14 below (right). (Ex. 1006, ¶¶ 99-100.)



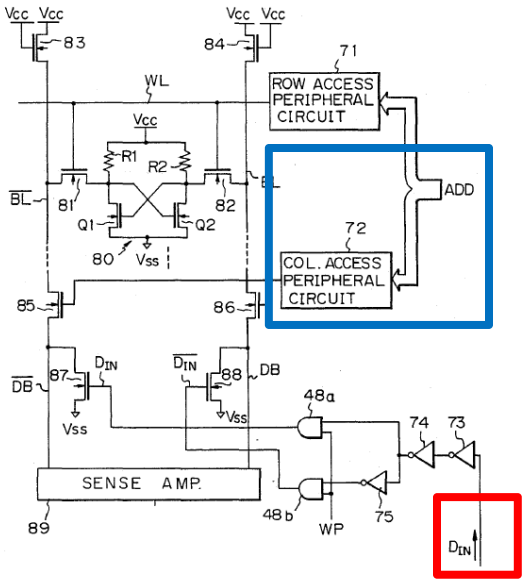
Ex. 1003 at Figure. 7



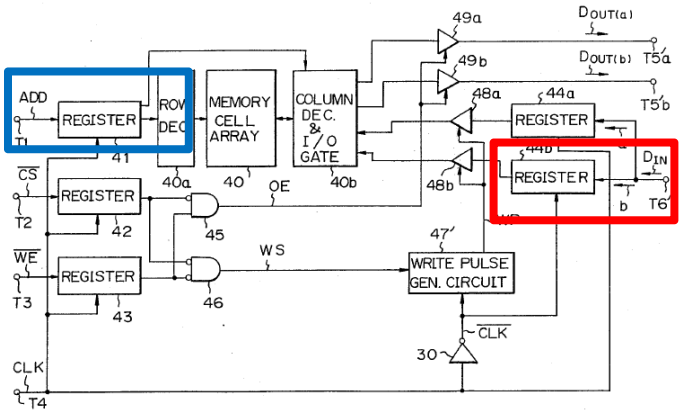
Ex. 1003 at FIG. 14

Claim 16(c)	
16(c) generating a write column select signal in a second area of said circuit;	Ex. 1003 at 7:10-13; 6:66-7:2; 8:59-64; 9:9-18; FIG. 7; FIG. 14.

Suzuki generates a "write column select signal" from the output of register 41 as described above for claim 1(c) and claim 5. Additionally, the write column select signal is generated in a "second area" (blue) of Suzuki's memory circuit as shown at the gate/transistor level in FIG. 7 below (left), as well as at the block level in FIG. 14 below (right). One of ordinary skill in the art would readily understand that the write data signal and the right column select signal are different signals that have to come from different circuits and different areas. (Ex. 1006, ¶ 102.) The second area can be contrasted with the "first area" (red) of the write data signal described above for claim 16(b). (Ex. 1006, ¶¶ 101-103.)



Ex. 1003 at FIG. 7



Ex. 1003 at FIG. 14

Claim 16(d)	
16(d) generating a clock signal having a first transition wherein said clock signal moves from a first state to a second state distinct from said first state and a second transition wherein said clock signal moves from said second state to said first state;	Ex. 1003 at 2:49-51; 7:25-29; FIG. 14; FIG. 15.

Suzuki generates a clock signal having a first transition from a first state to a second state and a second transition from the second state to the first state as described above for claim 1(d). (Ex. 1006, ¶¶ 104-105.)

Claim 16(e)	
16(e) conditioning said write data signal to be responsive to said first transition of said clock signal and to selectively become active upon the occurrence of said first transition; and	Ex. 1003 at 12:56-59; FIG. 14; FIG.15.

Suzuki conditions the data signal to be responsive to the first transition of the clock signal and to selectively become active upon the occurrence of the first transition as described above for claim 1(e). Suzuki also shows the data signal of claim 1(e) to be a "write data signal" as described above for claim 6. (Ex. 1006, ¶¶ 106-107.)

Claim 16(f)	
16(f) conditioning said write column select signal to be responsive to said second transition of said clock signal	Ex. 1003 at 7:10-13; FIG. 14.

and to selectively become active upon the occurrence of said second transition.	

Suzuki conditions the select signal to be responsive to the second transition of the clock signal and to selectively become active upon the occurrence of the second transition as described above for claim 1(f). Suzuki also shows the select signal of claim 1(e) to be a "write column select signal" as described above for claim 5. (Ex. 1006, ¶¶ 108-109.)

15. Claims 17 and 18 are unpatentable as anticipated by Suzuki.

Claim 17	
17. The method of claim 16 wherein said clock signal is conditioned to have between a forty-five percent duty cycle and a fifty-five percent duty cycle.	Ex. 1003 at FIG. 15a, FIG. 15b.
Claim 18	
18. The method of claim 16 wherein said clock signal is conditioned to have a fifty percent duty cycle.	Ex. 1003 at FIG. 15a, FIG. 15b.

As described above, Suzuki discloses all the elements of claim 16. Suzuki also discloses a clock signal having between a forty-five percent duty cycle and a fifty-five percent duty cycle of claim 17 as described above for claim 2. Additionally, Suzuki discloses a clock signal having a fifty percent duty cycle of claim 18 as described above for claim 3. (Ex. 1006, ¶¶ 110-111.)

16. Claim 19 is unpatentable as anticipated by Suzuki.

Claim 19	
19. The method of claim 16 further comprising the step of generating an enable control signal selectively indicative of an enable state, and wherein said data is selectively processed to select memory cells only if said enable control signal indicates said enable state.	Ex. 1003 at 12:43-48; FIG. 14.

As described above, Suzuki discloses all the elements of claim 16 of the '653 patent. Suzuki also discloses the $\overline{CS}$ signal and the $\overline{WE}$ signal that each function as an enable control signal that is selectively indicative of an enable state, where data is selectively processed to select memory cells only if the enable control signal indicates the enable state as described above for claim 7. (Ex. 1006, ¶¶ 112-113.)

B. Ground #2: Claims 2-3, 10-11, and 17-18 are unpatentable under 35 U.S.C. § 103 as obvious in view of Suzuki in combination with Johnson

1. Claims 3, 10, and 18 are unpatentable as obvious in view of Suzuki in combination with Johnson

Claims 3, 10, and 18	
wherein said clock signal is conditioned to have a fifty percent duty cycle.	Ex. 1003 at 1:10-11; 1:24-28; 3:40-64. Ex. 1004 at p. 361.

Suzuki discloses a "self-timed" memory that uses a clock signal to latch data and select signals on opposite clock edges. (Ex. 1003 at 1:10-11; 3:40-64.) To utilize opposite clock edges, Suzuki also includes a "means for inverting the clock to an inverted clock." (Ex. 1003 at 1:47-51.) In the same field, Johnson teaches that "the ideal duty cycle for a clock signal is 50%. The falling edge of an ideal clock signal precisely bisects successive rising edges. This feature permits use of the inverted clock." (Ex. 1004 at p. 361 (emphasis added).) . (Ex. 1006, ¶ 114.)

It would be readily understood by one of ordinary skill in the art that when transmitting data that is synchronized with both the rising and falling edges of a clock the highest speed transmission can be attained by using a clock signal with a 50% duty cycle. If the time the clock is high is different than the time the clock is low the timing budget is reduced and bit errors occur. Not having a 50% duty cycle clock results in data that has to change, and become valid, sooner when clocked on one edge versus the data clocked other on the other edge. . (Ex. 1006, ¶ 115.)

A person of ordinary skill in the art at the priority date of the '653 patent would have understood that in order to enable the use of the inverted clock in Suzuki, the duty cycle of the clock signal should be 50% as taught by Johnson. A person of ordinary skill in the art would have been motivated to combine Johnson with Suzuki because the STRAM of Suzuki was designed to provide timing margins when "high-speed operation is demanded." (Ex. 1003 at 1:24-28.) When

designing a high-speed memory circuit, one having ordinary skill in the art would naturally turn to a handbook of high-speed digital design, such as Johnson. Therefore, the combination of Suzuki's clock signal and Johnson's 50% duty cycle would be obvious to one having ordinary skill in the art. . (Ex. 1006, ¶¶ 116-117.)

2. Claims 2, 9, and 17 are as obvious in view of Suzuki in combination with Johnson

Claims 2, 9, and 17	
wherein said clock signal is conditioned to have between a forty-five percent duty cycle and a fifty-five percent duty cycle.	Ex. 1003 at 1:10-11; 1:24-28; 3:40-64. Ex. 1004 at p. 361.

As described above, Suzuki in combination with Johnson teaches a clock signal having a 50% duty cycle. This 50% duty cycle of the combination of Suzuki and Johnson also renders claims 2, 9, and 17 of the '653 patent obvious by falling within the claimed forty-five percent to fifty-five percent duty cycle range of claims 2, 9, and 17. . (Ex. 1006, ¶¶ 118-119.)

C. Ground #3: Claims 12 and 16 are unpatentable under 35 U.S.C. § 103 as obvious in view of Suzuki in combination with Prince

1. Claim 12 is unpatentable as obvious in view of Suzuki in combination with Prince

Claim 12	
The memory circuit of claim 9 further comprising a plurality of additional memory cells all sharing a common	Ex. 1005 at *Introduction*, p. 20; sec. 5.4.2., pp. 31-32, 160; FIG. 5.8, p. 35.

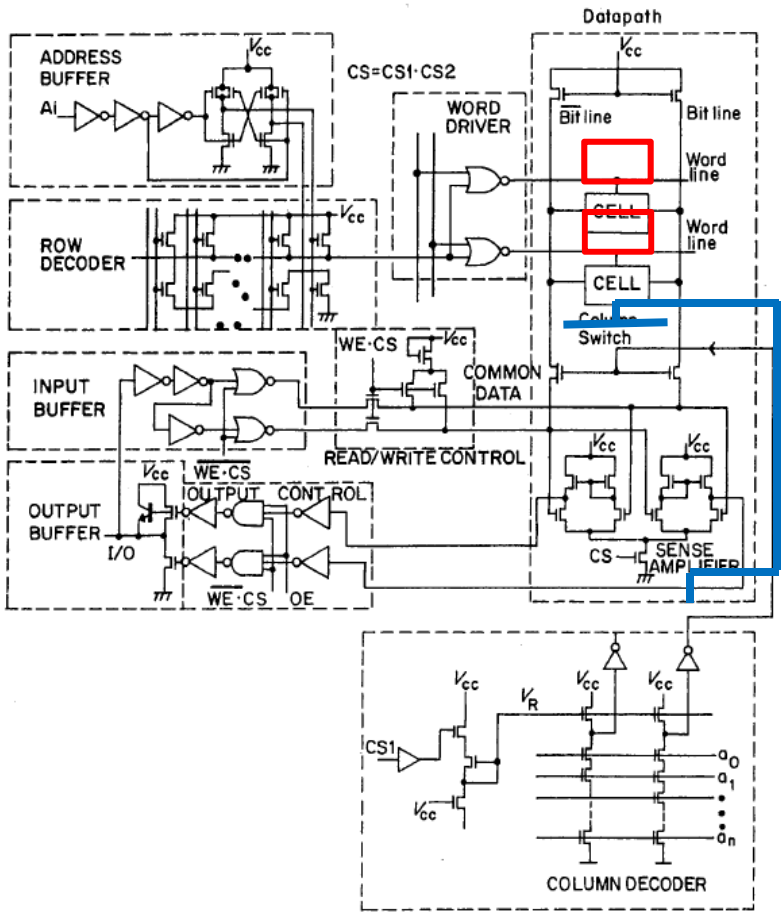
column address with said memory cell.	

As described above, Suzuki discloses all the elements of claim 9. The additional limitation of claim 12 is disclosed by, or inherent in, Suzuki as also described previously. But even if it was not, Prince discloses a "basic SRAM cell." (Ex. 1005 at sec. 5.4.2., p. 31.) According to Prince, "all MOS static RAMs have in common a basic cell . . . embedded in an array of similar cells which are accessed by . . . a column decoder circuit." (Ex. 1005 at sec. 5.4.2., pp. 31-32.) "The column address decoder translates the column address and makes a connection to the bit line B and the inverse bit line $\overline{B}$ of all the cells in the column addressed." (Ex. 1005 at sec. 5.4.2., p. 34 (emphasis added).) Thus, FIG. 5.8 of Prince shows a plurality of memory cells (red) sharing a common column address (blue) as recited by claim 12. (Ex. 1006, ¶ 120.)

It would be readily understood by one of ordinary skill in the art that a column address signal is used to access a plurality of memory cells. If there was only one memory cell in a column, then no column address or column address decoder would be required. Thus the use of a column address indicates the existence of a plurality of memory cells that share that column address. (Ex. 1006, ¶ 121.)

One having ordinary skill in the art would be motivated to consult Prince as a handbook of semiconductor memories, the goal of which "is to provide a basic

handbook of the various aspects of semiconductor memories." (Ex. 1005 at *Introduction*, p. 20.) Because "all MOS static RAMs have in common a basic cell" (Ex. 1005 at sec. 5.4.2., p. 31), one having ordinary skill in the art would be motivated to use the basic SRAM structure of Prince as a starting point before adding the timing mechanisms of Suzuki. (Ex. 1006, ¶¶122-123.)



Prince at FIG. 5.8

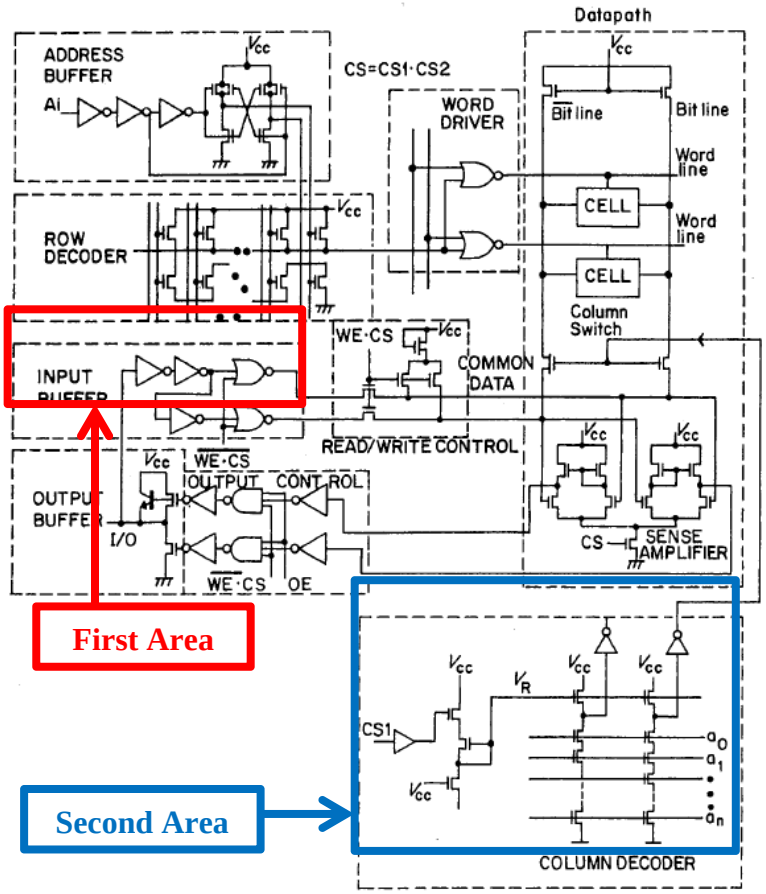
2. Claim 16 is unpatentable as obvious in view of Suzuki in combination with Prince

Claim 16(b)(c)	
(b) generating a write data signal in a first area of said circuit; (c) generating a write column select signal in a second area of said circuit;	Ex. 1005 at sec. 5.4.2., p. 31; FIG. 5.8, p. 35.

As described above, Suzuki discloses all the elements of claim 16(a) and 16(d)-16(f). Additionally, the basic SRAM schematic in FIG. 5.8 of Prince shows the "write data signal" (red) being generated in a first area of the memory circuit and traversing the memory array laterally, and the "write column select signal" (blue) being generated in a second area of the circuit and traversing the memory array longitudinally. As described above, one having ordinary skill in the art would be motivated to consult Prince as a handbook of semiconductor memories to use the basic SRAM structure of Prince as a starting point before adding the timing mechanisms of Suzuki, because "all MOS static RAMs have in common a basic cell" (Ex. 1005 at sec. 5.4.2., p. 31). Therefore, the combination of Suzuki and Prince discloses the limitations of claim 16(b) and 16(c). (Ex. 1006, ¶ 124.)

It would be readily understood by one of ordinary skill in the art that the write data signal and the write column select signal are different signals that they have to come from different circuits and different areas. As such, elements 16(b)

and (c) are rendered obvious by Suzuki in view of Prince, in addition to being disclosed and/or inherent in Suzuki standing alone. (Ex. 1006, ¶¶ 125-126.)



Prince at FIG. 5.8

V. CONCLUSION

For the reasons set forth above, the Challenged Claims of the ’653 patent are unpatentable and Petitioners request institution of trial on *inter partes* review of the Challenged Claims.

VI. MANDATORY NOTICES UNDER 37 C.F.R. §42.8(A)(1)

A. Real Parties-in-Interest

Pursuant to 37 C.F.R. §42.8(b)(1), the real parties in interest are Broadcom Limited.

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner is not aware of any pending matters, which may affect, or be affected by, a decision in this proceeding

C. Fee

This petition is accompanied by a payment of $25,000 and requests review of 20 claims of the ’653 patent. *See* 37 C.F.R. §42.15. Thus, this petition meets the fee requirements under 35 U.S.C. §312(a)(1). The Board is hereby authorized to charge any additional fees required by this action to Deposit Account No. 20-1430.

D. Designation of Counsel

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioners identify the following designated counsel:

Lead Counsel	Back-Up Counsel
Kristopher L. Reed Registration No. 58,694 KReed@kilpatricktownsend.com Postal and Hand-Delivery Address: Kilpatrick Townsend & Stockton LLP 1400 Wewatta Street, Suite 600 Denver, CO 80202 (303) 571-4000 (telephone) (303) 571-4321 (facsimile)	Matthew C. Holohan Registration No. 73,288 mholohan@kilpatricktownsend.com Postal and Hand-Delivery Address: Kilpatrick Townsend & Stockton LLP 1400 Wewatta Street, Suite 600 Denver, CO 80202 (303) 571-4000 (telephone) (303) 571-4321 (facsimile)

E. Service Information

As shown in the Certificate of Service, a copy of the present petition and exhibits is being served to the correspondence address of record, with a courtesy copy to Invensas Corporation at its corporate address. Petitioners may be served via email to their lead and back-up counsel.

Respectfully submitted,

Dated: October 31, 2016

By: *Kristopher Reed*
Kristopher Reed
Registration No. 58,694
Kilpatrick Townsend & Stockton LLP
1400 Wewatta St, #600
Denver, CO 80202

Lead Counsel for Petitioner

CERTIFICATION UNDER 37 CFR §42.24(d)

Under the provisions of 37 CFR §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 9,748, which is less than the 14,000 allowed under 37 CFR §42.24(a)(i).

Respectfully submitted,

Dated: October 31, 2016

By: *Kristopher Reed*
Kristopher Reed
Registration No. 58,694
Kilpatrick Townsend & Stockton LLP
1400 Wewatta St, #600
Denver, CO 80202

Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on October 31, 2016, a complete and entire copy of this Petition for *Inter Partes Review* and all supporting exhibits were provided via UPS, to the Patent Owner by serving the correspondence address of record as follows:

Daryl K. Neff
Lerner David Littenberg Krumholz & Mentlik, LLP
600 South Avenue West
Westfield, NJ
07090-1497

Invensas Corporation
3025 Orchard Parkway
San Jose, CA 95134

By: *Kristopher Reed*
Kristopher Reed
Kilpatrick Townsend & Stockton LLP
1400 Wewatta St, #600
Denver, CO 80202