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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,195,302

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,195,302

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Ex. 1007 Schuster *et al.*, "A 15-ns CMOS 64K RAM," *IEEE J. of Solid-State Circuits*, Vol. SC-21, No. 5, Oct. 1986, pp.704-12 ("*Schuster*")

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Ex. 1012 Amrutur et al., "A Replica Technique for Wordline and Sense Control in Low-Power SRAM's," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 8, Aug. 1998, pp. 1208-19 ("*Amrutur*")

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-6, 10-12, and 14-18 ("the challenged claims") of U.S. Patent No. 6,195,302 ("the '302 patent") (Ex. 1001), which is currently assigned to ProMOS Technologies, Inc. ("Patent Owner") according to USPTO records. For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

Related Matters: Patent Owner has asserted the '302 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Petitioner is concurrently filing a petition challenging claims 1-6 and 10-12 of the '302 patent. Petitioner respectfully requests that the Board institute each petition, as each presents distinct and non-redundant grounds. Patent Owner has also asserted U.S. Patent Nos. 6,849,897 ("the '897 patent"), 6,020,259 ("the '259 patent"), 6,699,789 ("the '789 patent"), 6,088,270 ("the '270 patent"), and 5,761,112 ("the '112 patent") in this action. Petitioner is also concurrently filing IPR petitions on the '897, '259, '789, '270,

and ’112 patents.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-Promos1-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the ’302 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1-6, 10-12, and 14-18 of the ’302 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following

grounds:

Ground 1: Claims 14-15 are unpatentable under pre-AIA 35 U.S.C. §103(a) based on UK Patent GB2246005B ("*Min*") (Ex. 1005);

Ground 2: Claims 1-5 and 10-12 are unpatentable under pre-AIA 35 U.S.C. §103(a) in view of *Min* and U.S. Patent No. 5,140,199 to *Seo* ("*Seo*") (Ex. 1004);

Ground 3: Claim 6 is unpatentable under 35 U.S.C. § 103(a) in view of *Min, Seo,* and Schuster *et al.*, "A 15-ns CMOS 64K RAM," *IEEE J. of Solid-State Circuits*, Vol. SC-21, No. 5, Oct. 1986, pp.704-12 ("*Schuster*") (Ex. 1007);

Ground 4: Claims 16 and 17 are unpatentable under 35 U.S.C. § 103(a) in view of *Min* and U.S. Patent No. 4,980,799 to *Tobita* ("*Tobita*"); and

Ground 5: Claim 18 is unpatentable under 35 U.S.C. § 103(a) in view of *Min* and *Schuster*.

The challenged claims are not entitled to a filing date earlier than February 5, 1999.[1] *Min* was published on August 31, 1994. *Seo* was issued on August 18, 1992. *Schuster* was published in October 1986. *Tobita* was published on

[1] Petitioner takes no position on whether that the claims of the '302 patent are supported by the provisional application (U.S. 60/118,737 filed on February 5, 1999). Each of the prior art references that form the basis of the grounds asserted in this petition are prior art to the '302 patent regardless of whether the claims of the '302 patent are entitled to the February 5, 1999 provisional filing date.

December 25, 1990. Therefore, *Min*, *Seo*, *Schuster*, and *Tobita* are prior art to the '302 patent at least under pre-AIA 35 U.S.C. § 102(b).

Schuster was published in October 1986 in the *IEEE Journal of Solid-State Circuits*, Volume SC-21, Issue No. 5. This can be seen, for example, at the top of each page of *Schuster*. (Ex. 1007, 704-712.) Given that it was published in a well-known journal in October 1986, over a decade before the filing date of the '302 patent (*id.*), *Schuster* qualifies as prior art under pre-AIA 35 U.S.C. § 102(b). In fact, *Schuster* was cited by other articles well-before the '302 patent was filed. (Ex. 1011, 363 (reference 7); Ex. 1012, 1219 (reference 21).)

Among the references relied upon in this Petition, *Min* and *Schuster* were never considered by the Patent Office during prosecution of the '302 patent. (Ex. 1001, References Cited.) *Seo* is, however, listed on the face of the '302 patent and was submitted in an information disclosure statement during prosecution. But Petitioner presents *Seo* in a new light never considered by the Office. (*Infra* Section IX.) Moreover, Petitioner presents testimony from R. Jacob Baker, Ph.D., P.E., (Ex. 1002), an expert in the field of the '302 patent, who confirms that the relevant teachings of *Seo* alone or in combination with the other cited references discloses or suggests what is recited by the challenged claims. (Ex. 1002.) As such, consideration of *Seo* by the Patent Office during prosecution of the '302 patent should not preclude the Office from considering and adopting the grounds in

this petition that involve this reference.

C. Statement of Non-Redundancy

Petitioner is filing a second IPR petition against the '302 patent concurrent with the filing of this petition. However, Petitioner's proposed grounds for institution in the two petitions are not redundant and the Board should institute review in both proceedings. The primary references applied in the two petitions disclose features of the challenged claims in different ways, and are based on different combinations of references. For example, the primary reference in this petition (*Min*) does not explicitly disclose a circuit component that delays a signal, as required by claim elements 10(e) and 1(f). Instead, a secondary reference is relied upon to disclose that feature. In contrast, the primary reference at issue in the other petition discloses these claimed features. As such, Petitioner respectfully requests that the Board adopt all proposed Grounds in both of the petitions.

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention ("POSITA") of the '302 patent would have had at least a Bachelor's degree in electrical engineering or equivalent thereof, and at least two to three years of

experience in design of semiconductor memory circuits. (Ex. 1002, ¶19)[2] More education can supplement practical experience and vice versa. (*Id*.)

VII. OVERVIEW OF THE TECHNOLOGY, '302 PATENT, AND PRIOR ART

A. Technology Background

At the time of the alleged invention of the '302 patent, it was well known that integrated circuit memories could include memory cell arrays consisting of thousands of memory cells arranged in a matrix of rows (word lines) and columns (bit lines), with each memory cell located at or near the crossing of a bit line and word line. (Ex. 1002, ¶37-38, citing Ex. 1009.) To read and write to the memory cells of a DRAM, other circuitry was known to be provided. (*Id*., ¶39.) For instance, the bit lines were often coupled into complementary bit line pairs, with each pair associated with a sense amplifier that amplifies the signal on the bit lines during a read operation and drives/controls the bit lines when data is being written into the memory cells. (*Id*.)

B. The '302 Patent

The '302 patent issued from U.S. application no. 09/492,276 filed on January 27, 2000 (Ex. 1003 at 4-26) and is directed to a memory device with sense

[2] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E., (Ex. 1002), an expert in the field of the '302 patent. (Ex. 1002, ¶5-15.)

amplifiers 101a-101c that are coupled to a high voltage line Vcc and ground via driver transistors 104 and 106, respectively, as shown in FIG. 1. (Ex. 1002, ¶40.):

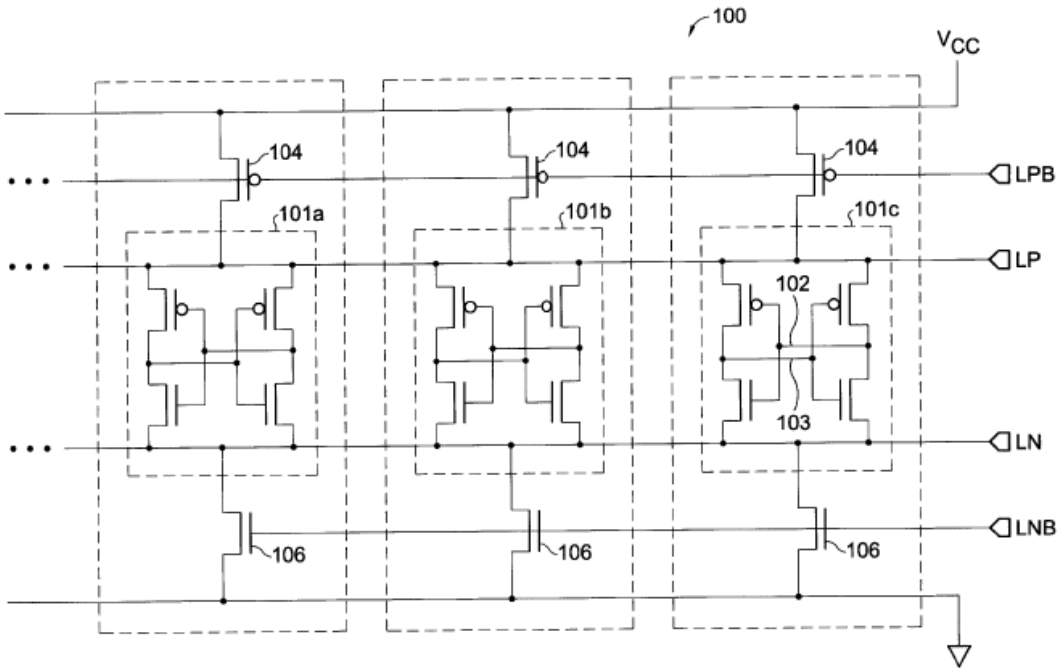


FIG. 1

(Ex. 1001, FIG. 1; *see also id.*, 4:40-5:4; Ex. 1002, ¶¶40-48.)

The '302 patent discloses circuitry for generating the LPB and LNB signals (FIG. 1 above). (Ex. 1002, ¶¶43-48.)

C. *Min*

Min discloses in FIG. 1A a conventional sense amplifier driving circuit (including driving transistors Q1 and Q2, and INV1 and INV2) that drives a plurality of sense amplifiers SA_1-SA_n. (Ex. 1005, 1:6-8, FIG. 1, 2:5-29.)

The sense amplifiers SA_1-SA_n in *Min* are connected to one another at node LA_P and at LA_N and are connected to Vcc and Vss by driving transistors Q1 and

Q2, respectively. (Ex. 1005, FIG. 1A, 2:17-19; Ex. 1002, ¶54.) In this configuration, "the sense amplifiers are controlled by turn on and off operations of the driving transistors Q1, Q2." (Ex. 1005, 3:17-20.)

Min discloses a variation of the FIG. 1A sense amplifier driving circuit arrangement in FIG. 1B where the sense amplifier driving circuitry now includes a driving transistor $Q1_1$-$Q1_n$ and $Q2_1$-$Q2_n$ for each sense amplifier SA_1-SA_n. (Ex. 1005, FIG. 1B, 4:13-23; Ex. 1002, ¶55.)

The sense amplifier driving circuits in both FIG. 1A and FIG. 1B, however, had some disadvantages. (Ex. 1005, 5:11-34; Ex. 1002, ¶56.) To overcome these disadvantages, *Min* discloses several exemplary sense amplifier driving circuits. (Ex. 1005, 12:5-13:15; Ex. 1002, ¶¶56-64.) One such sense amplifier driving circuit is disclosed in FIG. 9 and another sense amplifier driving circuit is shown in FIG. 10. (Ex. 1005, 13:5-15, 27:22-30, 30:5-8.)

VIII. CLAIM CONSTRUCTION

The claims of the '302 patent should be given their broadest reasonable construction because it has not and will not expire before a final written decision is issued in this proceeding. 37 C.F.R. § 42.100(b).

Furthermore, to determine whether a claim should be interpreted under § 112, ¶6, "[t]he standard is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the

name for structure. *Williamson v. Citrix Online LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015). "[T]he failure to use the word 'means' [in a claim] creates a rebuttable presumption . . . that § 112, para. 6 does not apply." *Id.* at 1348. "[T]he presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function." *Id.* (internal quotes omitted).

As set forth herein, Petitioner provides the broadest reasonable construction for certain claim terms below. Any term not interpreted below should be interpreted in accordance with its plain and ordinary meaning under the broadest reasonable interpretation standard.[3]

[3] Because of the different claim interpretation standards used in this proceeding and in district courts, any claim interpretations submitted or implied herein for the purpose of this proceeding are not binding upon Petitioners in any litigation related to the '302 patent. Specifically, any interpretation or construction of the claims presented herein, either implicitly or explicitly, should not be viewed as constituting, in whole or in part, Petitioner's interpretation of such claims in any underlying litigations involving the '302 patent. Moreover, Petitioner does not concede that the challenged claims are not indefinite, which is something that cannot be pursued in this proceeding under the Rules.

A. "timer unit . . . generating a control signal"

Claim 1 recites the term "timer unit . . . generating a control signal."[4] The term "timer unit" is a means-plus function term under 35 U.S.C. § 112, ¶6.

Claim 1 recites that "a timer unit having an output coupled to the control electrode and generating a control signal." This claim recites function ("generating a control signal") without reciting sufficient structure for performing that function. A timer unit as recited in claim 1 does not connote any structure. Indeed, the identified function for this term, "having an output coupled to the control electrode" only specifies where the output of the timer unit is coupled and does not specify structure for the timer unit itself. Like the term "module" in *Williamson*, the recitation of a timer "unit" in claim 1 does not provide a sufficiently definite structure for performing the function of "generating a control signal." *Williamson*, 792 F.3d at 1350 ("the word 'module' does not provide any indication of structure

[4] The term "the timer unit output" in claim 12 does not have any antecedent basis, and thus claim 12 is indefinite. However, for purposes of this proceeding, Petitioner assumes that the term "timer unit output" in claim 12 means an output from a clock or timer, such as a "clock signal." Under that assumption, however, "the timer unit output" in claim 12 should not be construed in a manner similar to the recited "timer unit . . . generating a control signal" in claim 1 discussed above.

because it sets forth the same black box recitation of structure for providing the same specified function as if the term 'means' had been used.").

Although claim 1 recites "a first component" and "a second component" that are both "within the timer unit," those "component[s]" are specified in the claim using purely functional language, *i.e.*, describing what they do. Therefore, those "component[s]" do not impart sufficient structure for performing the recited function of the "timer unit." Therefore, although "means" is not recited in this claim, the presumption that § 112, ¶6 does not apply is overcome in this instance, and "timer unit" is a means-plus-function term.

Construing a means-plus-function claim term requires that the function recited in the claim term be first identified; then, the written description of the specification must be consulted to identify the corresponding structure that performs the identified function and equivalents thereof. *Williamson*, 792 F.3d 1339 at 1351; *see also Gracenote, Inc. v. Iceberg Indus., LLC*, IPR2013-00551, Paper No. 6 at 15 (Feb. 28, 2014).

The written description of the '302 patent discloses that the function of "generating a control signal" is performed by at least a pair of transistors and one or more circuit components that delay a signal. For example, the '302 patent discloses that the pair of transistors 303, 308 and delay element 307 generate control signal LPB, and that the pair of transistors 313, 308 and delay unit 317

generate control signal LNB. (Ex. 1001, 5:57, 6:7-21, FIG. 3.)

For purposes of this proceeding, resistors 306 and 316 should not be considered as part of the corresponding structure, because the specification of the '304 patent discloses that that "resistors 306 and 316 can be eliminated and rise time of the first and second stage controlled by relative transistor sizes." (*Id.*, 6:31-33.)

Therefore, for purposes of this proceeding, the corresponding structure for the identified function for this term is "at least a pair of transistors and one or more circuit components that delay a signal" and its equivalents.

B. "first component . . . causing the control signal to change from a first logic level towards a second logic level at a first rate"

This term, which appears in claim 1, is a means-plus-function term under § 112, ¶6. The term "component" is a nonce word and does not connote any structure. Moreover, the identified function for this term "causing the control signal to change from a first logic level towards a second logic level at a first rate" does not provide any description structure for the "component." Indeed, as discussed above regarding "timer unit," although the "first component" is recited as being "within the timer unit," the "first component" in claim 1 is specified using purely functional language. (*Supra* section VIII.A.) Therefore, claim 1 does not recite sufficiently definite structure for performing the above function. Accordingly, the claimed "first component" is a means-plus-function term.

Looking to the specification, the '302 patent discloses that transistor 303 causes control signal LPB to change from VCCI ("first logic level") towards ground ("second logic level") at an initial rate where the rate is the change in voltage (dv/dt) over time for LPB. (Ex. 1001, 6:8-13, 6:31-33, FIG. 3.) The '302 patent also discloses that transistor 313 causes control signal LNB to change from ground ("first logic level") towards VCCI ("second logic level") at an initial rate where the rate is the change in voltage (dv/dt) over time for LNB. (*Id.*, 6:11-13, 6:31-33, FIG. 3.) Accordingly, for both the LPB and LNB control signals, the corresponding structure is transistor 303 and transistor 313, respectively.

Therefore, for purposes of this proceeding, the corresponding structure for the identified function the claimed "first component" is "a first transistor" and its equivalents.

C. "second component . . . causing the control signal to change to the second logic level at a second rate"

This term, which appears in claim 1, is a means-plus-function term under § 112, ¶6. As noted above, "component" does not connote any structure. Also, the identified function for this term, "causing the control signal to change to the second logic level at a second rate," does not provide any indication of the structure for the "second component." As discussed above regarding "timer unit," although the "second component" is recited as being "within the timer unit," the "second component" in claim 1 is specified using purely functional language.

(*Supra* section VIII.A.) Therefore, the claimed "second component" is a means-plus-function term.

The '302 patent discloses that transistor 308, when turned on, causes control signal LPB to be pulled down toward ground ("change to the second logic level"), which causes LPB to "fall to the ground voltage with a high dv/dt." (Ex. 1001, 6:17-18; *see also id.*, FIG. 3.) The '302 patent also discloses that transistor 318, when turned on, causes control signal LNB to be pulled up to VCCI rapidly without the dv/dt limiting effect of resistor 316. (*Id.*, 6:18-21; *see also id.*, FIG. 3.) Accordingly, for both the LPB and LNB control signals, the corresponding structure is transistor 308 and transistor 318, respectively.

Therefore, for purposes of this proceeding, the corresponding structure for the identified function the claimed "second component" is "a second transistor" and its equivalents.

D. "delay unit . . . generating a delayed sense control signal"

This term, which appears in claim 10, is a means-plus-function term under § 112, ¶6. The term "delay unit" does not connote any structure and the identified function for this term, "generating a delayed sense control signal," provides no guidance as to the structure. The "delay unit" is specified as being "coupled to the sense control signal node," but that does not specify structure for the "delay unit" itself, and the "delay unit" is specified using purely functional language.

Therefore, claim 10 does not recite sufficient structure for performing the above function. Accordingly, the term "delay unit" is a means-plus-function term.

The '302 patent discloses that delay element 307 performs the above function regarding generating a signal at the gate of transistor 308 ("delayed sense control signal") that controls signal LPB, and that delay unit 317 performs the above function regarding generating a signal at the gate of transistor 318 ("delayed sense control signal") that controls signal LNB. (Ex. 1001, 6:15-21, FIG. 3.)

The '302 patent does not specify the circuit components that constitute delay element 307. That is, the '302 patent does not specify delay 307 and delay 317 as anything more than a black box. To the extent the Board finds such disclosure in the '302 patent as describing sufficient structure for the claimed "delay unit," and that claim 10 is somehow capable of being construed, Petitioner proposes that "delay unit" be construed as one or more circuit components that delay a signal. (Ex. 1001, 6:15-21, FIG. 3.) Therefore, for purposes of this proceeding, the corresponding structure for the identified function for this term is "one or more circuit components that delay a signal" and its equivalents.

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: *Min* Renders Obvious Claims 14 and 15

1. Claim 14

a) A method for generating a control signal for controlling the operation of sense amplifier driver transistors in an integrated circuit memory device comprising:

To the extent that the preamble is determined to be limiting, *Min* discloses this feature. (Ex. 1002, ¶¶75-78.)

With respect to FIG. 9, *Min* discloses a "sense amplifier driving circuit[]" where transistor Q110 drives "a plurality of sense amplifiers." (Ex. 1005, 27:22-30, FIG. 9.) *Min* discloses a method for operating the driving circuit. (Ex. 1005, 29:15-30:3.) For example, *Min* explains that the driving circuit controls "the current Icca flowing through the driver transistor Q110," which controls the voltage at node LA_P. (*Id*., 29:15-30:3, FIG. 9.) A POSITA would have understood that the current Icca depends on the gate voltage ("control signal") of transistor Q110 and the driving circuit of FIG. 9 controls the gate voltage of Q110. (Ex. 1002, ¶76; *supra* Section VII.C.) Driving transistor Q110 is a "sense amplifier driver transistor" because it "driv[es] a plurality of sense amplifiers." (Ex. 1005, 27:28-30.) *Min* also discloses the driving circuit of FIG. 9 may control the gate voltage of more than one driving transistor instead a single driving transistor Q110. (Ex. 1005, 28:4-8.) Accordingly, *Min* discloses "[a] method for generating a control signal for controlling the operation of sense amplifier driver transistors"

(emphasis added). (Ex. 1002, ¶76.)

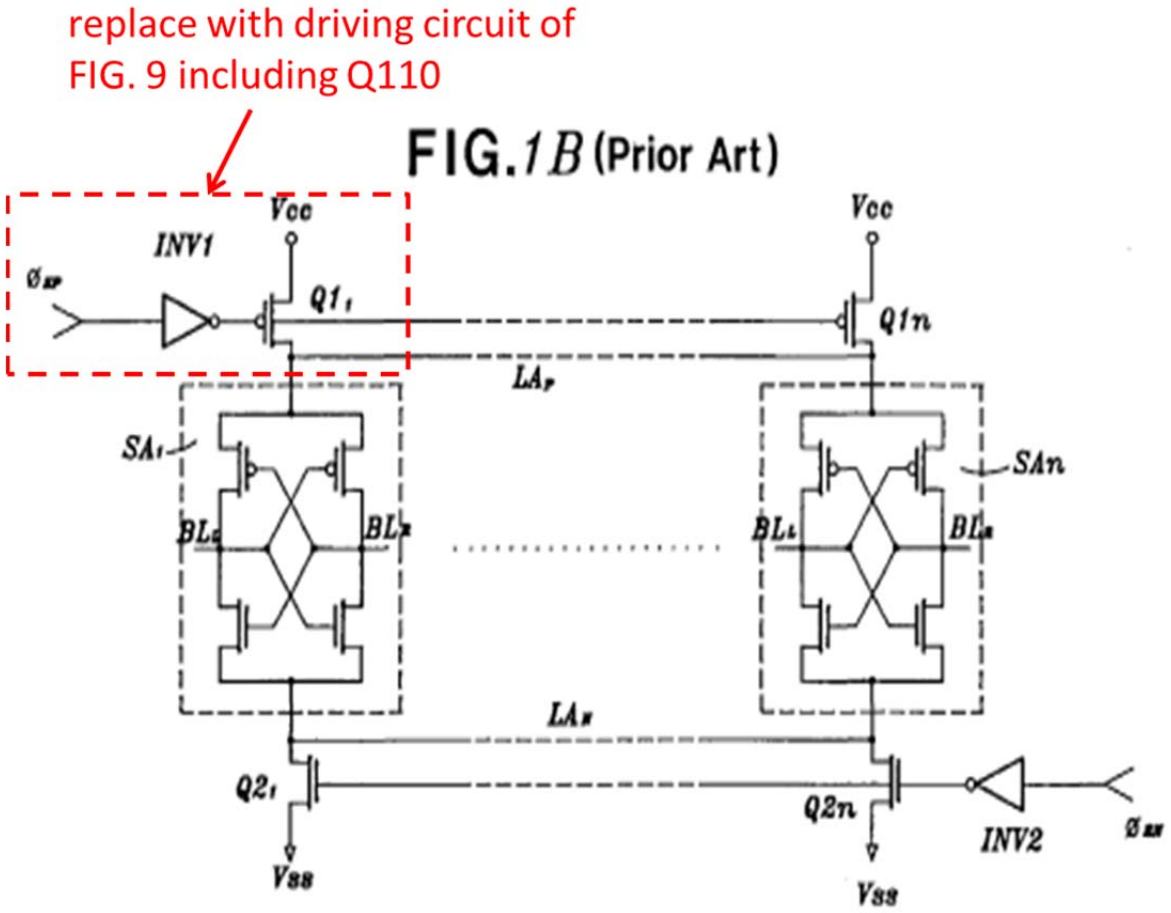
A POSITA would have understood *Min* discloses the driving transistors ("sense amplifier driver transistors") are "in an integrated circuit memory device," because *Min* relates to a "sense amplifier driving circuit which is suitable for use in a high density semiconductor memory device." (Ex. 1005, 1:4-9; *see also id*., 12:12-13; Ex. 1002, ¶78; *supra* section VII.C; citations and analysis below for the remaining elements of this claim.)

> b) providing a sense amplifier drive transistor having a control terminal coupled to receive the control signal and having a power node for supplying current to a preselected number of sense amplifiers;

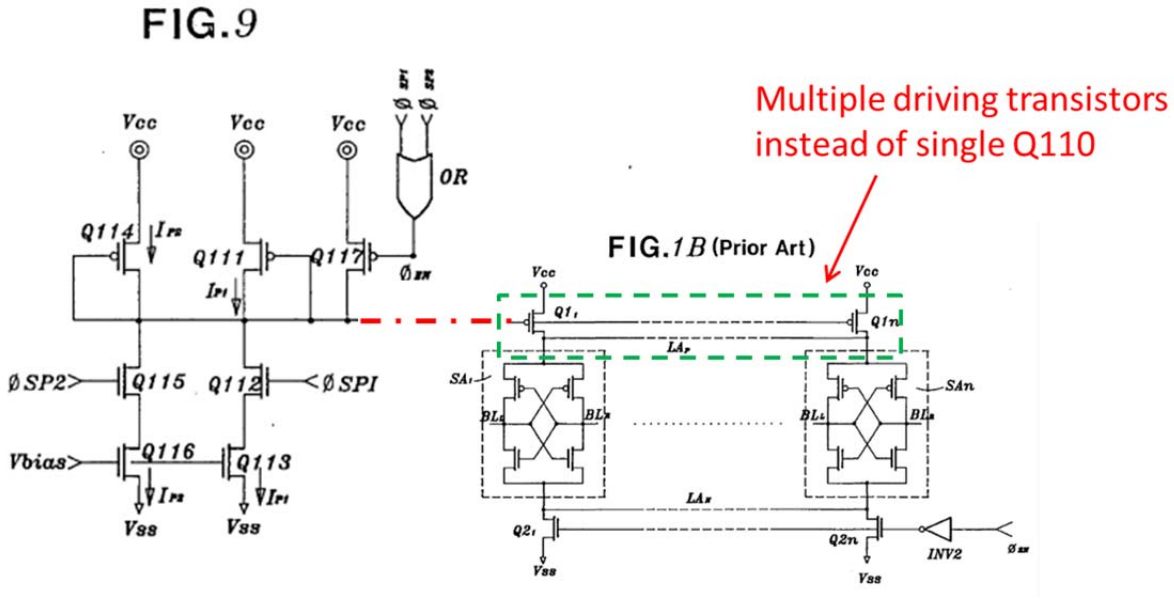
Min discloses or suggests this feature. (Ex. 1002, ¶¶79-84.) As discussed above for claim 14(a), the driving circuit of FIG. 9 controls the gate voltage of transistor Q110, or a plurality of driving transistors, which drives a "plurality of sense amplifiers." (Ex. 1005, 27:28-30, 28:4-8; Ex. 1002, ¶79.)

FIG. 9 does not provide explicit details regarding how the plurality of driving transistors would be connected to the "plurality of sense amplifiers." (*Id*.) However, FIG. 1B discloses such a configuration. (Ex. 1005, FIG. 1B.) In particular, *Min* identifies problems with the driving circuitry that drives sense amplifiers SA_1-SA_n in the conventional sense amplifier driving circuit of FIG. 1B. (Ex. 1005, 5:11-34.) To overcome these disadvantages, *Min* discloses several

exemplary sense amplifier driving circuits, one of which is the sense amplifier driving circuit of FIG. 9. (*Id*., 12:5-13:15, 27:22-26; Ex. 1002, ¶80.) A POSITA would have been motivated to replace, and would have known how to replace, the conventional driving circuitry in the top half of FIG. 1B with the driving circuit of FIG. 9 such that the driving circuitry of FIG. 9 drives a plurality of driving transistors $Q1_1$-$Q1_n$. (Ex. 1002, ¶80.) A POSITA would have known how to combine the driving circuit of FIG. 9 with the sense amplifier configuration of FIG. 1B because driving transistor Q110 in FIG. 9 drives latch node LA_P, which is also the latch node that is driven by the "plurality of driving transistors $Q1_1$-$Q1_N$" in FIG. 1B. (*Id.*, ¶80; Ex. 1005, 29:21-29, FIG. 9, 4:13-23, FIG. 1B; *supra* Section VII.C.) The combination may be pictorially represented as follows:



(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶80.) The same configuration can also be pictorially represented as:

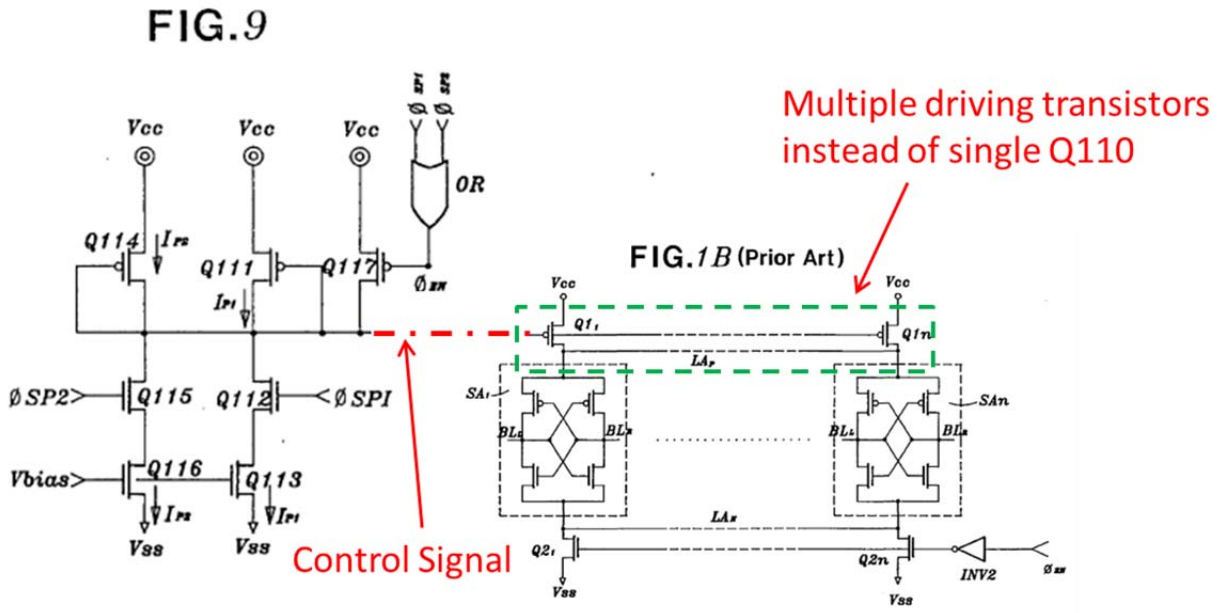


(Ex. 1005, FIG. 1B, FIG. 9 (annotated), 28:4-8 (explaining that Q110 can be replaced by multiple driving transistors); Ex. 1002, ¶80.)

A POSITA would have found the above combination of FIG. 9 and FIG. 1B obvious because the driving circuit of FIG. 9 solves some of the problems associated with conventional driving circuits (*e.g.*, conventional driving circuit in FIG. 1B) and allows the "sense amplifiers [to be] driven in a stable and rapid manner . . . ." (Ex. 1005, 5:11-34, 30:1-3; Ex. 1002, ¶81.) *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007). Moreover, the above modification of the configuration of FIG. 1B with the driving circuit of FIG. 9 would have been a mere combination of known prior art components (driving circuit of FIG. 9 and the sense amplifier configuration of FIG. 1B) according to known methods (connecting the driving transistors in the circuit of FIG. 9 with sense amplifiers

SA_1-SA_n at the LA_P latch node) to yield predictable results (a sense amplifier configuration with a driving circuit that is able to drive the sense amplifiers in a stable and rapid manner). (Ex. 1002, ¶81.)

In the combined FIG. 9 – FIG. 1B system, each of the driving transistors $Q1_1$-$Q1_n$ ("a sense amplifier drive transistor") has a gate terminal ("control terminal"). (*Id.*, ¶82.) The gate terminals of driving transistors $Q1_1$-$Q1_n$ receive the same signal ("control signal"; *supra* Section IX.A.1(a)) that was received by the gate terminal of transistor Q110. (*See* illustration below for the combined system.)



(Ex. 1005, FIG. 1B, FIG. 9 (annotated), Ex. 1002, ¶82.)

Therefore, each driving transistor $Q1_1$-$Q1_n$ ("a sense amplifier drive transistor") has a gate terminal ("control terminal") that receives "the control

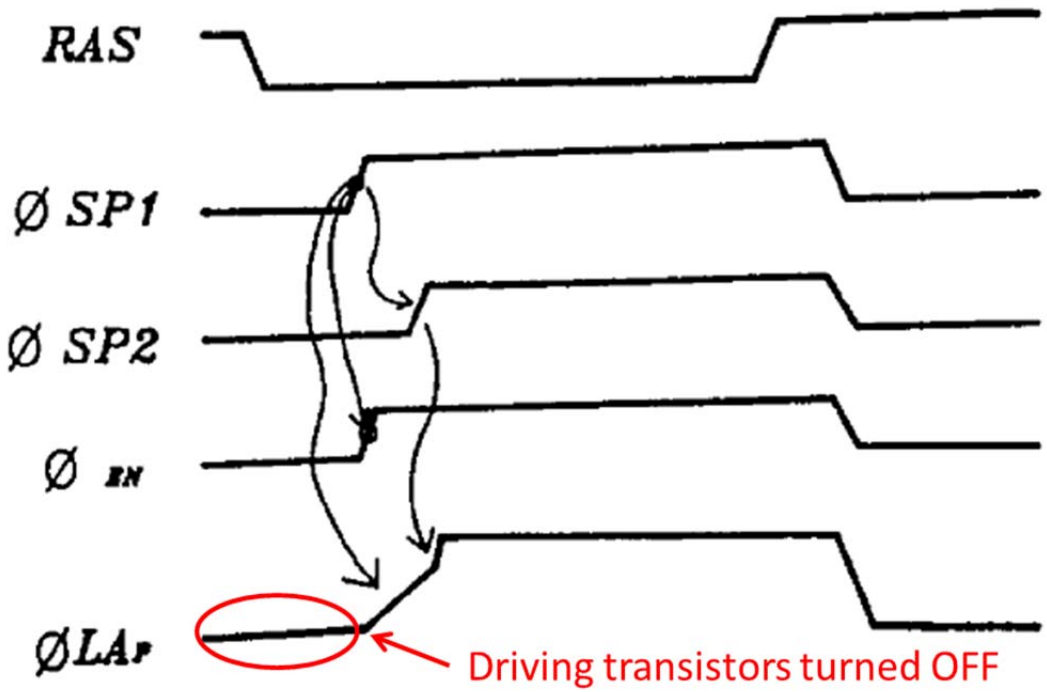
signal." (Ex. 1002, ¶83.) That is, *Min* discloses "providing a sense amplifier driver transistor having a control terminal coupled to receive the control signal," as claimed. (*Id*.)

Moreover, as seen from the above illustration, each driving transistor $Q1_1$-$Q1_n$ is connected to sense amplifiers SA_1-SA_n at the latch node LA_P. The latch node LA_P is "a power node for supplying current to a preselected number of sense amplifiers" because the driving transistors $Q1_1$-$Q1_n$ drive the sense amplifiers SA_1-SA_n by providing a current to latch node LA_P, which current is then supplied to the sense amplifiers to drive sense amplifiers SA_1-SA_n. (Ex. 1005, 29:24-30:3, 27:28-30; Ex. 1002, ¶84.) A POSITA would have understood that the node LA_P supplies the current (and therefore power) to the sense amplifiers because current from the power supply Vcc to the sense amplifiers SA_1-SA_n will pass through node LA_P. (*See* illustration above; Ex. 1002, ¶84.)

c) placing the control signal at a level selected to turn off the driver transistors;

Min discloses or suggests this feature. (Ex. 1002, ¶¶85-86.) *Min* discloses "turning on the driving transistor Q110" and therefore turning on the multiple driving transistors $Q1_1$-$Q1_n$ (*supra* section IX.A.1(a)) when signal "ϕ_{SP1} is set to have a high level." (Ex. 1005, 29:18-25, Ex. 1002, ¶85.) Accordingly, a POSITA would have understood that Q110 (or the multiple driving transistors $Q1_1$-$Q1_n$) were previously turned off. (Ex. 1002, ¶85.) This understanding is confirmed by

the lower part of FIG. 9, which shows that signal ϕLA_P (voltage at node LA_P) is initially at a low voltage level, which corresponds to pull-up transistor Q110 (or pull-up transistors $Q1_1$-$Q1_n$ in the combined system) being off, because if transistor Q110 (or transistors $Q1_1$-$Q1_n$) were on, then ϕLA_P would have started increasing to Vcc and would not be at low voltage initially. (Ex. 1005, FIG. 9; Ex. 1002, ¶85.)



(Ex. 1005, FIG. 9 (excerpted and annotated); Ex. 1002, ¶85.)

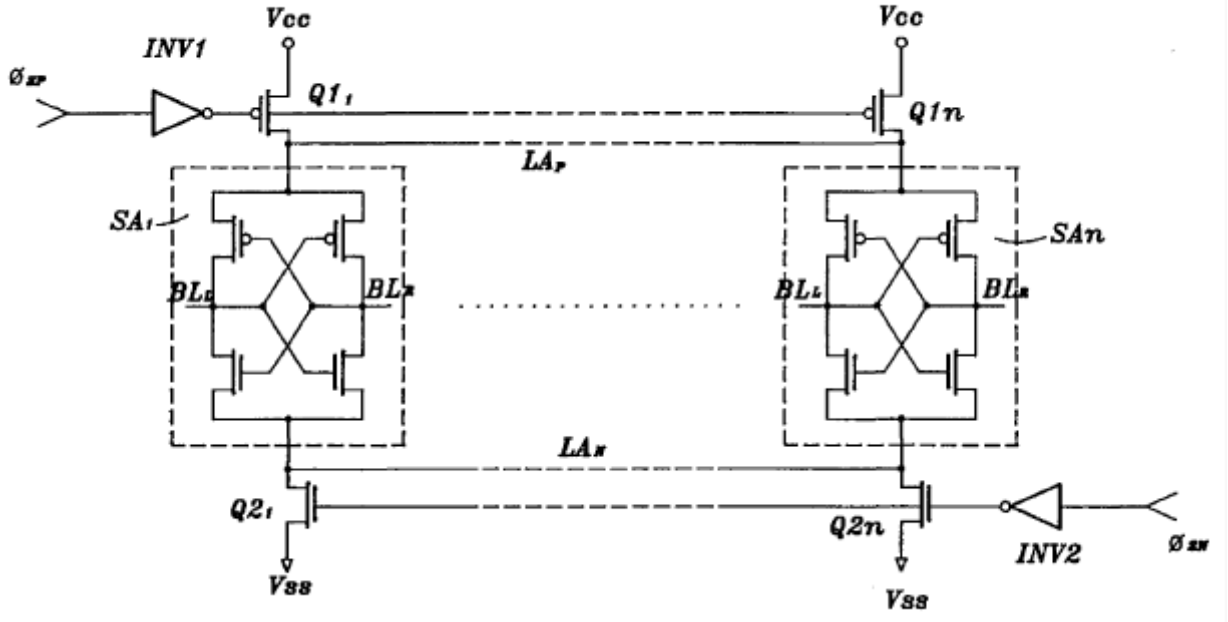
A POSITA would have understood that such driving transistors would have been configured to be turned off by placing the signal at the gate of the driving transistors in the combined FIG. 9 – FIG. 1B system ("placing the control signal")

at a sufficiently high voltage ("a level selected to turn off the driver transistors"). (Ex. 1002, ¶86.)

d) coupling a signal to be sensed to a latch node of the sense amplifier;

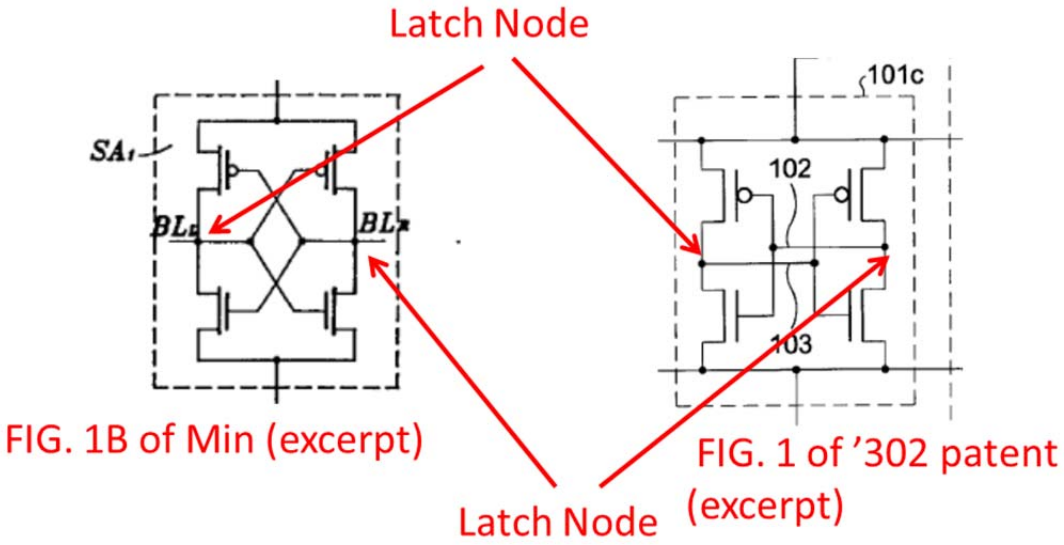
Min discloses or suggests this feature. (Ex. 1002, ¶¶87-97.) As discussed above, the combined FIG. 9 – FIG. 1B system discloses a plurality of sense amplifiers SA_1-SA_n, which are the sense amplifiers illustrated in FIG. 1B. (*Supra* Section IX.A.1(b).) *Min* discloses that each sense amplifier SA_1-SA_n in FIG. 1B is coupled to a pair of bit lines BL_L and BL_R because the bit lines "are connected to gate terminals of the corresponding NMOS and PMOS transistors" of the sense amplifiers. (Ex. 1005, 2:8-13, FIG. 1B.)

FIG. 1B (Prior Art)



(Ex. 1005, FIG. 1B.)

The nodes at which the bit lines are coupled to the sense amplifiers would have been understood by a POSITA to be "latch nodes" for the same reasons that the '302 patent explains that nodes 102 and 103 are "latch nodes." (Ex. 1002, ¶88; Ex. 1001, 4:46-51.)



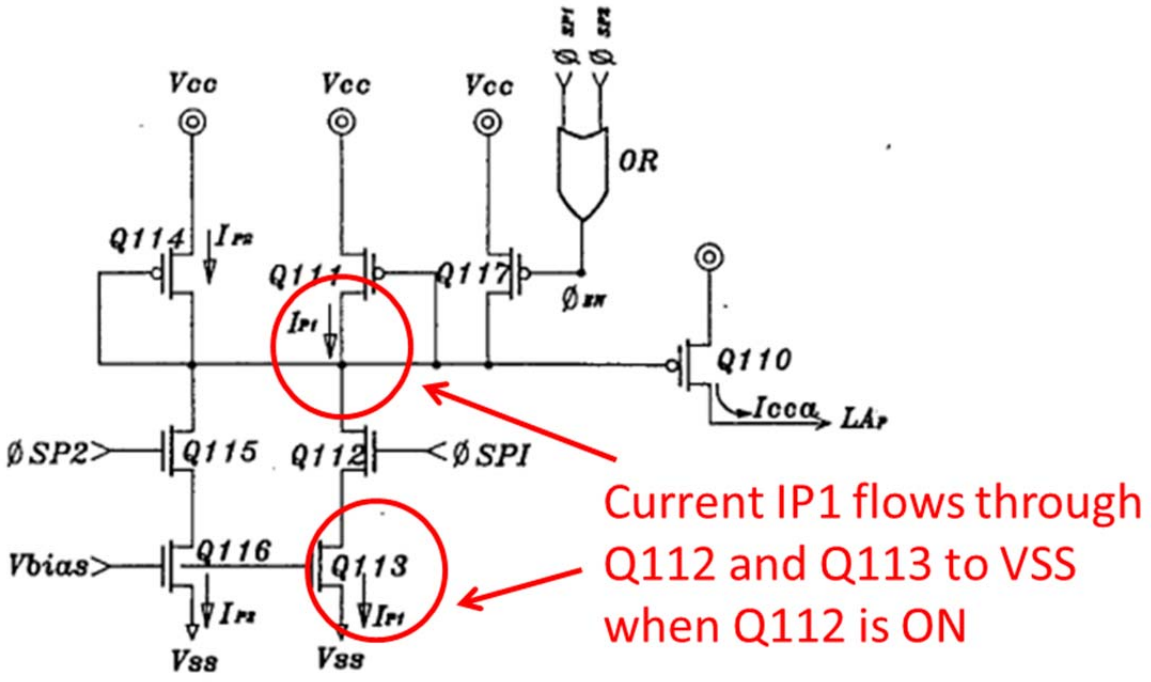
(Ex. 1005, FIG. 1B (annotated); Ex. 1001, FIG. 1 (annotated); Ex. 1002, ¶88.)

As shown in FIG. 1B of *Min*, each latch node of sense amplifiers SA_1-SA_n is coupled to a bit line. (Ex. 1005, FIG. 1B.) Also, it was well known to a POSITA that a bit line carries a signal, which represents the voltage stored in a memory cell and that the sense amplifier amplifies the signal on the bit line. (Ex. 1002, ¶89; Ex. 1001, 1:15-37; *see also* Ex. 1005, 1:10-13.) Therefore, a POSITA would have understood from the disclosure of *Min* that *Min* discloses "coupling a signal" (the memory cell voltage on the bit lines) "to be sensed to a latch node of the sense amplifier" as discussed above. (Ex. 1002, ¶90.)

> e) supplying the charge from an external power supply to the sense amplifier driver transistor through a first impedance at a first rate; and

Min discloses or suggests this feature. (Ex. 1002, ¶¶91-97.) For example, *Min* discloses that signal "ϕ_{SP1} is set to have a high level," which turns on NMOS transistor Q112. (Ex. 1005, 29:21-24, FIG. 9.) Therefore, transistor Q112 will start conducting current because it is turned on. (Ex. 1002, ¶91.) Because NMOS transistor Q113 is a "constant current source" as a result of the voltage Vbias applied to its gate, Q113 is also on. (Ex. 1005, 28:21-27.) Therefore, current I_{P1} flows through Q112 and Q113 to V_{SS} as shown in FIG. 9. (*Id.*, FIG. 9 (annotated below); Ex. 1002, ¶91.)

FIG. 9



(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶91.)

A POSITA would have understood that when current I_{P1} flows through Q112 and Q113 to V_{SS}, electrons from V_{SS} will flow at a rate corresponding to I_{P1} ("supplying the charge from an external power supply") towards the gate of the driving transistors (*e.g.*, Q110 shown in FIG. 9) ("to the sense amplifier driver transistor"). (Ex. 1002, ¶92.) The electrons are provided at a rate ("first rate") corresponding to I_{P1}. (*Id.*) Therefore, the combined FIG. 9-1B configuration discloses "supplying the charge from an external power supply to the sense amplifier driver transistor . . . at a first rate." (*Id.*)

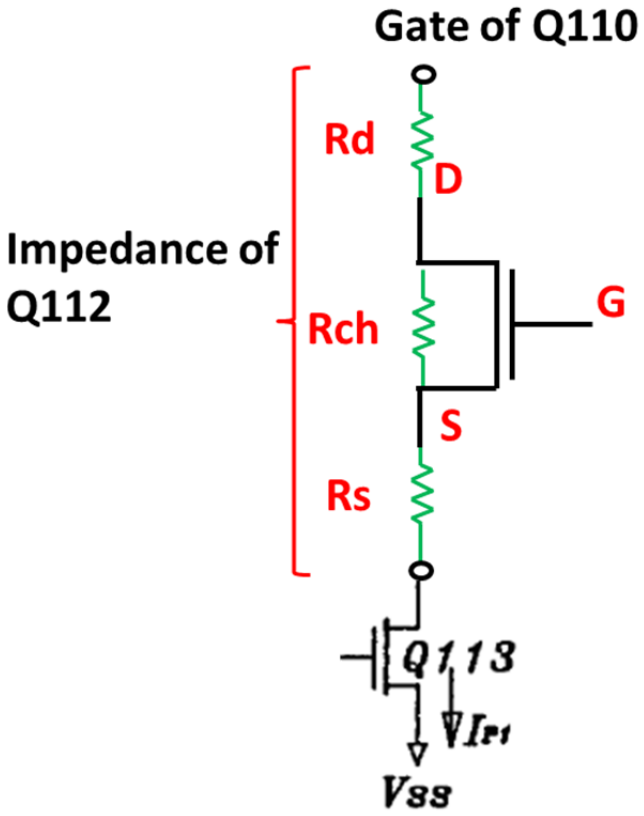
A POSITA would have further recognized that current I_{P1} has to flow through the impedance of Q112 because every MOSFET (Q112 is an N-type MOSFET or NMOS) has an associated impedance. (Ex. 1002, ¶¶93-96.) In particular, a POSITA would have known that the resistance R_{tot} of a transistor is given by the following equation:

$$R_{tot} = \frac{V_{ds}}{\mu_{eff} C_{ox} \frac{W}{L}\left((V_{gs} - V_t)V_{ds} - \frac{m}{2}V_{ds}^2\right)}$$

(Ex. 1008, 120, 206; Ex. 1002, ¶¶32,93-96,140-143.) A POSITA would have further recognized that the total device resistance of transistor Q112 is the sum of a

parasitic impedance[5] R_{sd} across the source and drain terminals of transistor Q112 and a channel resistance. (Ex. 1002, ¶¶33-35.)

Based on known characteristics of MOSFETs at that time, transistor Q112 may be represented as below:



(Ex. 1002, ¶96; Ex. 1005, FIG. 9 (representation of transistor Q112).)

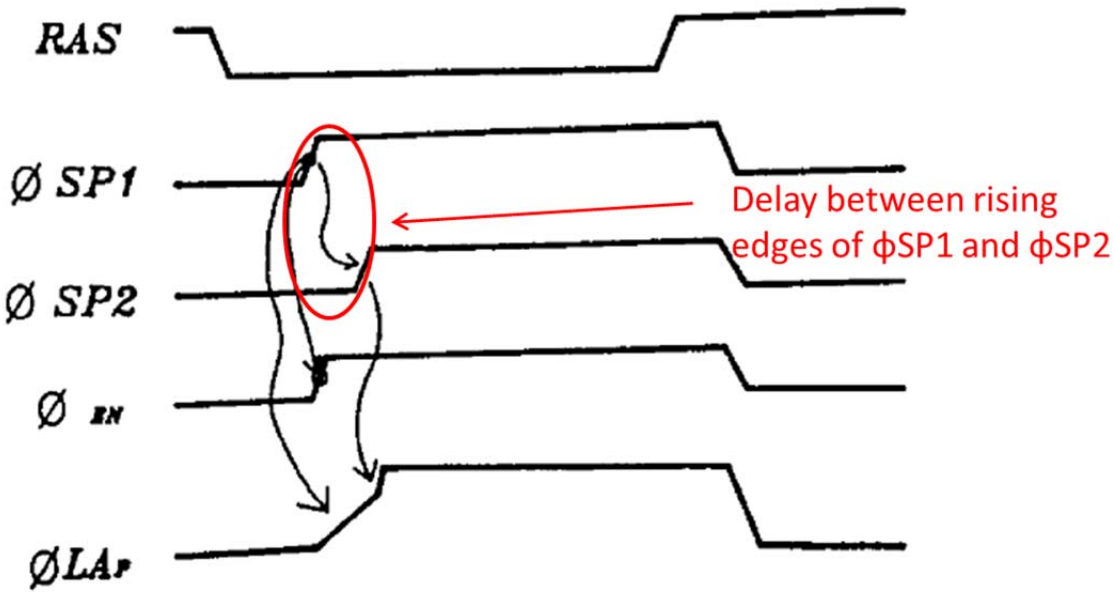
Therefore, a POSITA would have understood from the disclosure of *Min* that the resistance of transistor Q112 (*e.g.*, R_{tot}) is a "first impedance" as recited in

[5] The '302 patent confirms this inherent characteristic of a MOSFET. (Ex. 1001, 6:26-30.)

claim element 14(e) and the current I_{P1} (and the opposite flow of electrons) that flows through Q112 has to flow through R_{tot}. (Ex. 1002, ¶97.) A resistance associated with transistor Q112 would have been understood to be an "impedance." (Ex. 1002, ¶97; *see also* Ex. 1001, 6:10 ("resister [*sic*] 306"), 6:30 ("impedance provided by resistors 306 and 316").) Therefore, the combined FIG. 9-1B system discloses "supplying the charge from an external power supply to the sense amplifier driver transistor *through a first impedance* at a first rate" (emphasis added). (Ex. 1002, ¶97.)

> f) after a delay, supplying charge to the sense amplifier driver transistor through a second impedance at a second rate in addition to continuing to supply charge through the first impedance.

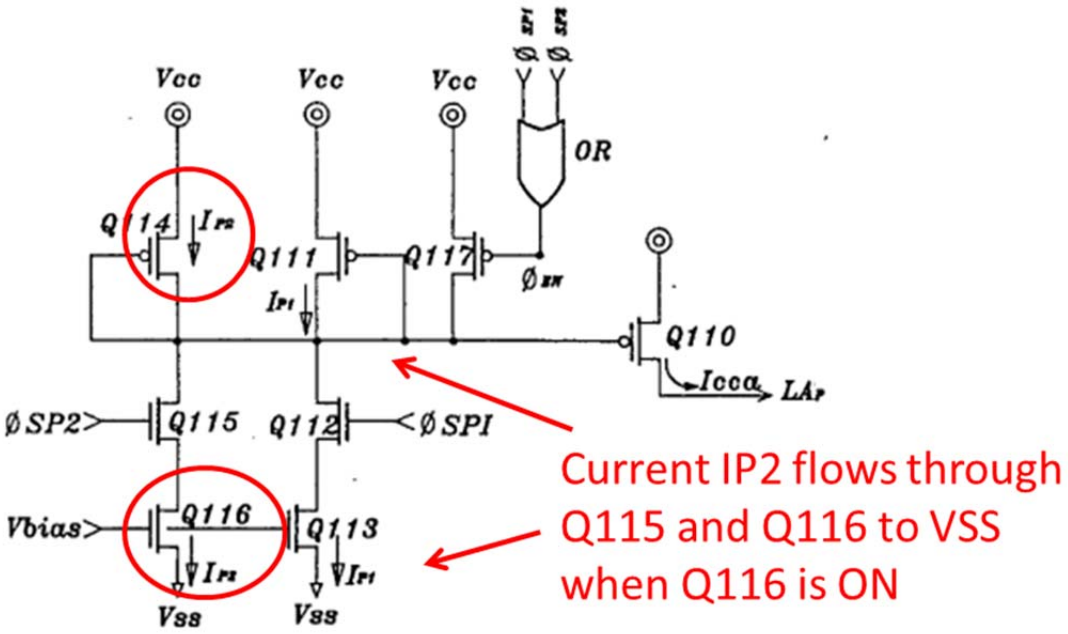
Min discloses or suggests this feature. (Ex. 1002, ¶¶98-104.) As discussed above in Section IX.A.1(e), *Min* discloses that when signal "ϕ_{SP1} is set to have a high level," NMOS transistor Q112 turns on. (Ex. 1005, 29:21-24, FIG. 9.) "After a certain period of time" has elapsed from when signal ϕ_{SP1} was set to a high level, "the second active restore enable signal ϕ_{SP2} goes to a high level, and the transistor Q115 . . . is turned on . . . ." (*Id.*, 29:29-34; Ex. 1002, ¶98.) That is, turning on of Q115 is delayed for a certain period of time after Q112 turns on. (Ex. 1002, ¶98.) This "delay" is illustrated in FIG. 9 of *Min*. (*Id.*)



(Ex. 1005, FIG. 9 (excerpt, annotated); Ex. 1002, ¶98.)

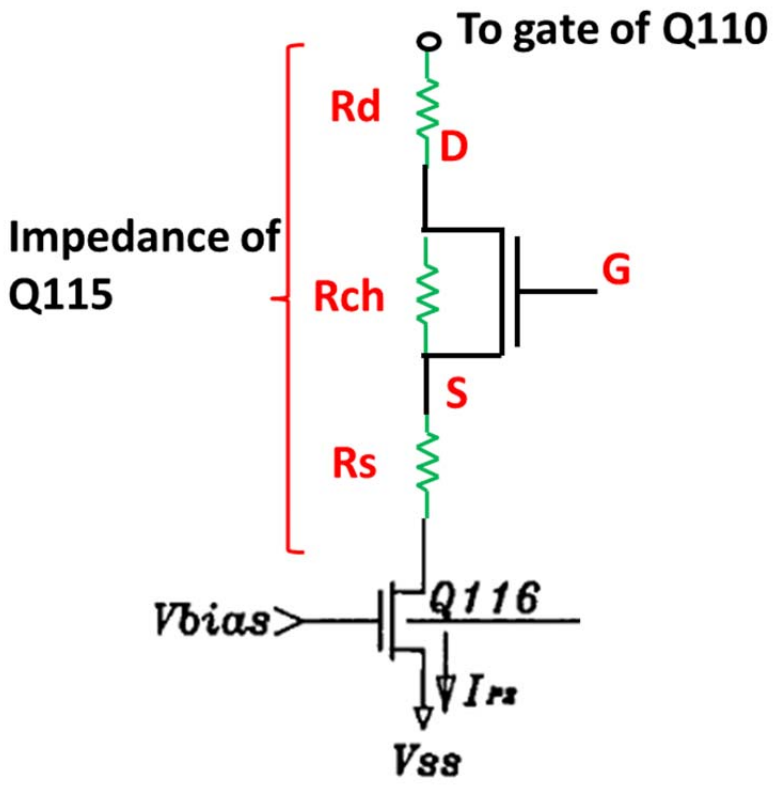
Once transistor Q115 is turned on after the delay, it conducts current I_{P2}, which flows through transistor Q116 to V_{SS}. (Ex. 1005, FIG. 9 (annotated below); Ex. 1002, ¶99.)

FIG. 9



(Ex. 1005, FIG. 9 (excerpt, annotated); Ex. 1002, ¶99.)

A POSITA would have understood that when current I_{P2} flows through Q115 and Q116 to V_{SS}, electrons from V_{SS} will flow at a rate corresponding to I_{P1} ("supplying charge") towards the gate of the driving transistors (*e.g.*, Q110 shown in FIG. 9) ("to the sense amplifier driver transistor"). (Ex. 1002, ¶100.) The electrons are supplied at a rate ("supplying charge . . . at a second rate second rate") corresponding to I_{P2}. (*Id.*) Furthermore, these electrons (and current I_{P2}) have to flow through the impedance of transistor Q115, which may be represented as below:



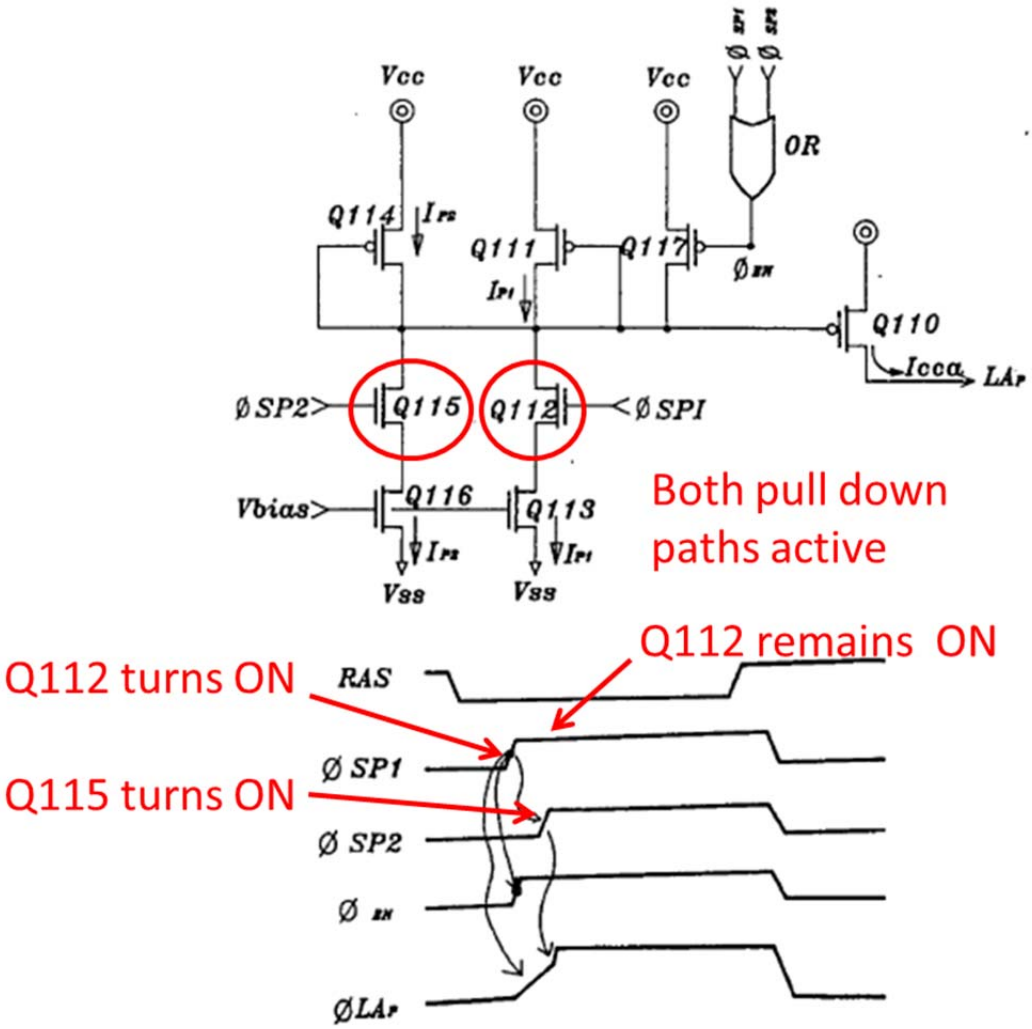
(Ex. 1002, ¶101; Ex. 1005, FIG. 9 (representation of transistor Q115); *supra* Section IX.A.1(e).)

Therefore, *Min* discloses "after a delay, supplying charge to the sense amplifier driver transistor through a second impedance at a second rate" because a certain time period after Q112 turns on, Q115 turns on and electrons from Vss are supplied to the gate of driving transistors (*e.g.*, Q110) through the impedance of Q115 at a rate corresponding to I_{P2}. (Ex. 1002, ¶102.)

Moreover, signals ϕ_{SP1} and ϕ_{SP2} are both high (at Vcc) after the rising edge of signal ϕ_{SP2} as shown below in FIG. 9. (*Id.*, ¶103; Ex. 1005, FIG. 9.) Therefore, both current paths (*i.e.*, the path thru Q112 and the path thru Q115) are

concurrently active because ϕ_{SP1} being high turns on Q112 and ϕ_{SP2} being high turns on Q115. (Ex. 1002, ¶103; *see* discussion above.) The timing diagram in FIG. 9 confirms this feature:

FIG. 9



(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶103.)

Therefore, electrons will flow to the gate of Q110 through Q112 and then continue to flow to the gate of Q110 through both Q115 and Q112 when Q115

turns on because both I_{P1} and I_{P2} are flowing into Vss from the gate of Q110. (Ex. 1002, ¶104.) Therefore, *Min* discloses that the driving circuit of FIG. 9 provides electrons to the gate of Q110 through Q115 at the rate corresponding to I_{P2} "in addition to continuing to supply charge through" the impedance of Q112 ("through the first impedance"). (*Id*.)

2. Claim 15

a) The method of claim 14 wherein the first rate is less than the second rate.

Min discloses or suggests this feature. (Ex. 1002, ¶¶105-107.) As discussed above regarding claim 14, *Min* discloses that the "first rate" corresponds to current I_{P1} and the "second rate" corresponds to current I_{P2} in the sense amplifier driving circuit of FIG. 9. (*Supra* Sections IX.A.1(e)-(f); Ex. 1005, FIG. 9; Ex. 1002, ¶105.)

Min further discloses that current I_{P1} is generated by a "first current mirror circuit" including transistor Q111, and current I_{P2} is generated by a "second current mirror circuit" including transistor Q114. (Ex. 1005, 27:31-34, 28:10-14, 32:4-15; FIG. 9; Ex. 1002, ¶106.) "In [the circuit of FIG. 9], the first current mirror circuit is activated first and is arranged to provide a *smaller current* than that of the second current mirror circuit which is activated later." (Ex. 1005, 32:31-35 (emphasis added).) Thus, current I_{P1}, which corresponds to the claimed "first rate,"

is less than I_{P2}, which corresponds to the claimed "second rate." (Ex. 1005, 32:31-35, 32:9-11[6]; Ex. 1002, ¶106.)

B. Ground 2: *Min* and *Seo* Render Obvious Claims 1-5, and 10-12[7]

1. Claim 10

a) "A sense amplifier clock driver circuit for an integrated circuit memory, the driver circuit providing at least one clock signal for controlling the operation of sense amplifier driver transistors and comprising:"[8]

Min discloses or suggests this feature. (Ex. 1002, ¶108-113; *see also* citations and analysis below for the remaining claim elements.) *Min* discloses a "sense amplifier driving circuit[]" in which transistor Q110 drives "a plurality of

[6] *Min* contains a typographical error at 32:11 in stating that the currents flowing through transistors Q111, Q114, Q121, and Q124 are "I_{P2}, I_{P2}, I_{N1}, and I_{N2}," respectively. A POSITA would have understood that the current flowing through transistor Q111 is I_{P1}. (Ex. 1005, FIG. 9; Ex. 1002, ¶106n.6.)

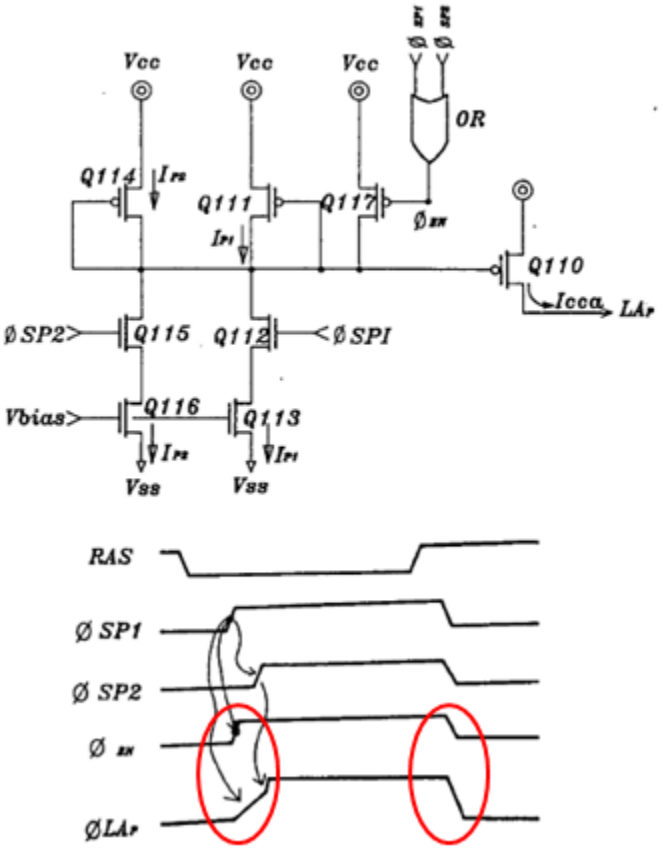
[7] Petitioner addresses claims 10-12 (Sections IX.B.1-B.3) before addressing claims 1-5 (Section IX.B.4-B.8) to provide context for the positions for the analysis of claims 1-5.

[8] The preamble of claim 10 is limiting because it is necessary to breathe life and meaning into claim 10. For instance, the term "clock signal" that is recited in the preamble is referenced back in the body of claim 10. (Ex. 1001, claim 10 "drive the clock signal".)

sense amplifiers." (Ex. 1005, 27:22-30, FIG. 9; *supra* Section VII.C; Ex. 1002, ¶108.)

The driving circuit of FIG. 9 generates a signal that controls the operation of driving transistor Q110. (*Supra* Sections VII.C, IX.A.1(a).) *Min* discloses that the driving circuit of FIG. 9 controls "the current Icca flowing through the driver transistor Q110," which controls the voltage at node LA_P. (Ex. 1005, 29:15-30:3.) A POSITA would have understood that the current Icca depends on the gate voltage of transistor Q110. (Ex. 1002, ¶109.) The POSITA would have also understood that the gate voltage of Q110 is a clock signal because it is generated from a "driving control *clock* ϕ_{EN}" (emphasis added) and follows "driving control clock ϕ_{EN}" in timing as discussed below. (*Id.*; Ex. 1005, 29:9-11, FIG. 9.) As seen below from the timing diagram of FIG. 9, the signal ϕLA_P starts rising when ϕ_{EN} starts rising and starts falling when ϕ_{EN} starts falling.

FIG. 9



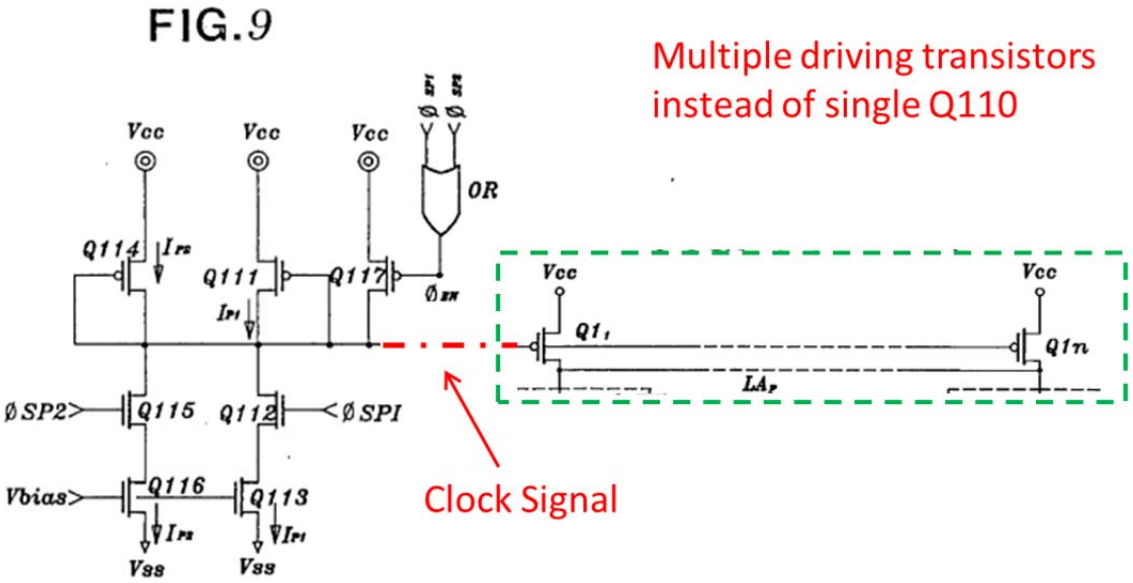
(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶109.)

But the voltage at node ϕLA_P depends on the gate voltage of Q110 because an increase in ϕLA_P requires a corresponding decrease in the gate voltage. (Ex. 1002, ¶110.) Therefore, a POSITA would have understood that the timing of the rise and fall of gate voltage of Q110 corresponds to the rise and fall of ϕ_{EN}, which *Min* discloses is a "driving control *clock*" (emphasis added).[9]

[9] A POSITA would have understood that as ϕ_{EN} begins to rise, ϕLA_P would begin to fall, and vice-versa. (Ex. 1002, ¶111n.8.)

In view of the above, a POSITA would have understood that *Min*'s FIG. 9 circuit is "a sense amplifier clock driver circuit." (Ex. 1002, ¶¶111-112.) Furthermore, a POSITA would have understood that *Min*'s FIG. 9 circuit is for "an integrated circuit memory," because *Min* discloses its invention relates to a "sense amplifier driving circuit which is suitable for use in a high density semiconductor memory device." (Ex. 1005, 1:4-9; *see also id*., 12:12-13; *infra* Section IX.B.4(b); Ex. 1002, ¶112.)

Min also discloses that the above clock signal (which is provided to the gate of Q110) is "at least one clock signal for controlling the operation of sense amplifier driver transistors" because *Min* discloses that transistor Q110 drives "a plurality of sense amplifiers" but that voltage at the gate of Q110 may be provided to the gate of more than one driving transistor. (Ex. 1005, 27:22-30, 28:4-8, FIG. 9; *supra* Section VII.C.) Each of the driving transistors is a "sense amplifier driver transistor," as discussed above. (*Supra* Section IX.A.1(a).) A POSITA would have understood that replacing Q110 with a plurality of driving transistors as disclosed in *Min* would be pictorially represented as follows:



(Ex. 1005, FIG. 1B, FIG. 9 (excerpted and annotated), 28:4-8 (explaining that Q110 can be replaced by multiple driving transistors); Ex. 1002, ¶113.)

> b) "a sense control signal node receiving an externally generated sense control signal indicating when sensing is to occur;"

Min discloses this feature. (Ex. 1002, ¶114-140.) *Min* discloses "turning on the driving transistor Q110" and therefore turning on the multiple driving transistors (*supra* section IX.A.1(a)) when signal "ϕ_{SP1} is set to have a high level." (Ex. 1005, 29:18-25, Ex. 1002, ¶114.) Because driving transistor Q110 "driv[es] a plurality of sense amplifiers" (*i.e.*, the sense amplifiers would not be active without Q110 being active), and ϕ_{SP1} activates Q110[10], a POSITA would have understood

[10] As explained above regarding the preamble of claim 10, *Min* discloses that Q110 can be replaced by more than one driving transistor. (*See supra* Section

that ϕ_{SP1} is a "sense control signal indicating when sensing is to occur." (Ex. 1005, 27:29-30, 29:21-25; Ex. 1002, ¶114.)

Min discloses that the gate terminal of transistor Q112 receives ϕ_{SP1} and therefore, the gate terminal of Q112 is "a sense control signal node." (Ex. 1005, FIG. 9, 28:19-21.) The circuitry for generating signal ϕ_{SP1} is not disclosed in FIG. 9 of *Min*, so a POSITA would have understood it to be an "externally generated sense control signal." (Ex. 1002, ¶115.)

c) "a first impedance having a terminal coupled to a selected logic level signal;"

Min discloses this feature. (Ex. 1002, ¶116-118.) For example, *Min* discloses that the resistance ("a first impedance") of transistor Q112 has a terminal coupled to Vss ("a selected logic level signal") through transistor Q113. (Ex. 1002, ¶118.)

As discussed above for claim 14(e), the resistance R_{tot} of transistor Q112 is a "first impedance" and one "terminal" of this impedance is the node at the bottom of Rs. (*Supra* Section IX.A.1(e).) As seen from the illustration at claim 14(e), the bottom node of Rs is coupled to Vss ("selected logic level signal") because current

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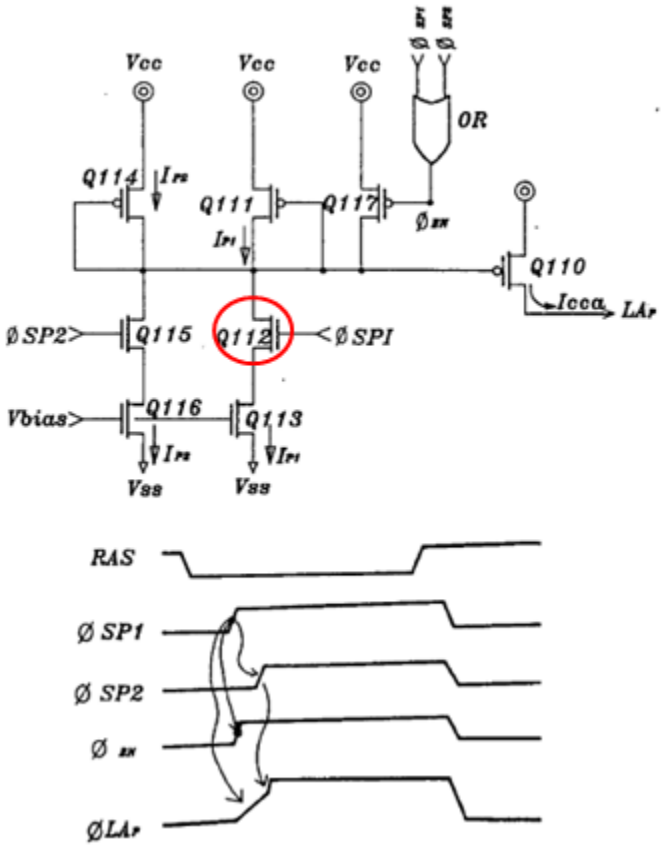
IX.B.1(a).) The operation of the circuit of FIG. 9 described in this section remains the same regardless of whether there is a single driving transistor Q110 or a plurality of driving transistors. (Ex. 1002, ¶114n.9.)

I_{P1} flows through Q112 (including bottom node of Rs) to Vss. (Ex. 1002, ¶118.) Therefore, *Min* discloses "a first impedance having a terminal coupled to a selected logic level signal." (*Id*.)

> d) "a first switch having current carrying electrodes coupled to drive the clock signal to a selected logic level through the first impedance, the first switch controlled by the sense control signal;"

Min discloses this feature. (Ex. 1002, ¶¶119-122.) For example, *Min* discloses a transistor Q112 ("a first switch") having source and drain terminals ("current carrying electrodes"). (Ex. 1005, FIG. 9.) Transistor Q112 is shown in FIG. 9 of *Min*:

FIG. 9



(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶119.)

As seen from FIG. 9, *Min* discloses that a current I_{P1} flows through switch Q112. (Ex. 1005, FIG. 9.) Accordingly, a POSITA would have understood that in order for Q112 to draw current I_{P1}, it has to pull down the gate of transistor Q111, which as seen from FIG. 9, is also connected to the gate of transistor Q110 ("the clock signal"; *supra* Section IX.B.1(a)). (Ex. 1002, ¶121; Ex. 1005, FIG. 9.) That is, in order for Q112 to draw current I_{P1}, it has to pull the gate of Q111 (which is connected to the gate of Q110) towards Vss ("to a selected logic level") through the resistance of transistor Q112 ("first impedance"). (Ex. 1002, ¶121.) The gate

voltage of Q110 ("clock signal") is therefore driven down towards Vss through the resistance of Q112 because the flow of current across the source and drain terminals of transistor Q112 requires that the current flow through the resistance (R_{tot}) of transistor Q112 (*see* annotated representation of Q112 above at claim 14(e)). (Ex. 1002, ¶121; *supra* Sections IX.B.1(c) and IX.A.1(e) (explaining the resistance associated with a transistor).) Therefore, *Min* discloses "a first switch having current carrying electrodes coupled to drive the clock signal to a selected logic level through the first impedance." (Ex. 1002, ¶121.)

Min further discloses that transistor Q112 is controlled by ϕ_{SP1} ("the first switch controlled by the sense control signal") because ϕ_{SP1} is provided to the gate of transistor Q112. (Ex. 1005, FIG. 9; Ex. 1002, ¶122.)

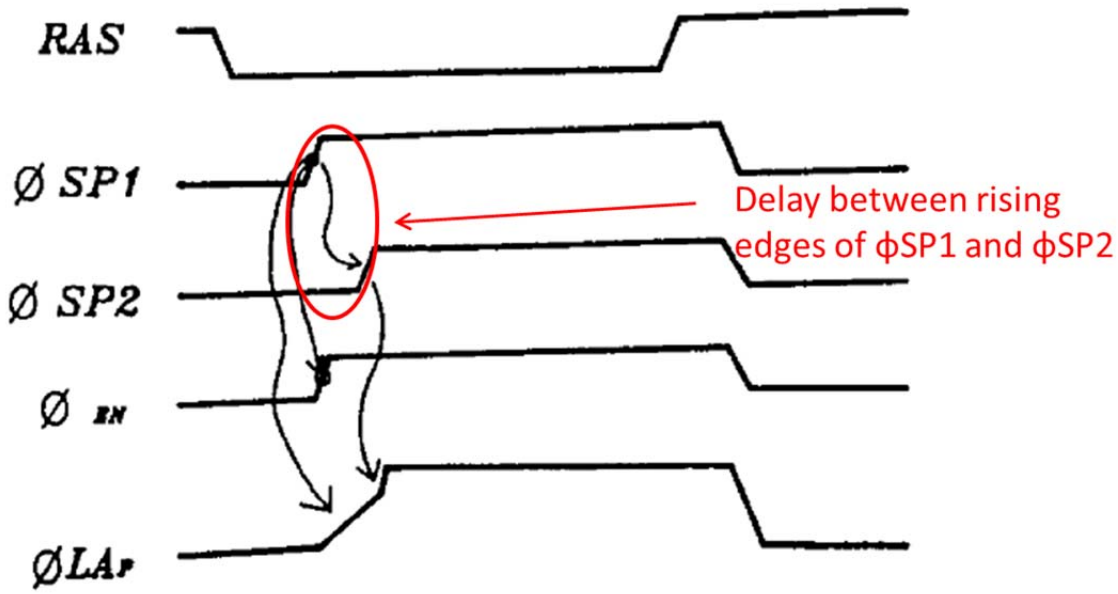
e) "a delay unit coupled to the sense control signal node and generating a delayed sense control signal"

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶123-130.) As explained above, this claim limitation is a means-plus-function term which has the function of "generating a delayed sense control signal" and the corresponding structure of "one or more circuit components that delay a signal and equivalents thereof." (*Supra* Section VIII.D.)

As discussed above for claim 10(b), ϕ_{SP1} is a "sense control signal" because ϕ_{SP1} controls the turning on of driving transistor Q110 ("sense amplifier driving transistor"). (*Supra* Section IX.B.1(b).) For similar reasons, ϕ_{SP2} is also a "sense

control signal" because it also controls the current conducted by driving transistor Q110. (Ex. 1002, ¶124.) *Min* confirms this because when "the second active restore enable signal ϕ_{SP2} goes to a high level, . . . the transistor Q115. . . is turned on so that the current Icca flowing through the driving transistor Q110 is *increased*." (Ex. 1005, 29:18-34,(emphasis added); Ex. 1002, ¶124.)

Min, however, discloses that ϕ_{SP2} goes to a high level "[a]fter a certain period of time" has elapsed from when signal ϕ_{SP1} was set to a high level. (Ex. 1005, 29:29-34; Ex. 1002, ¶125.) This delay between ϕ_{SP1} and ϕ_{SP2} is illustrated in FIG. 9:

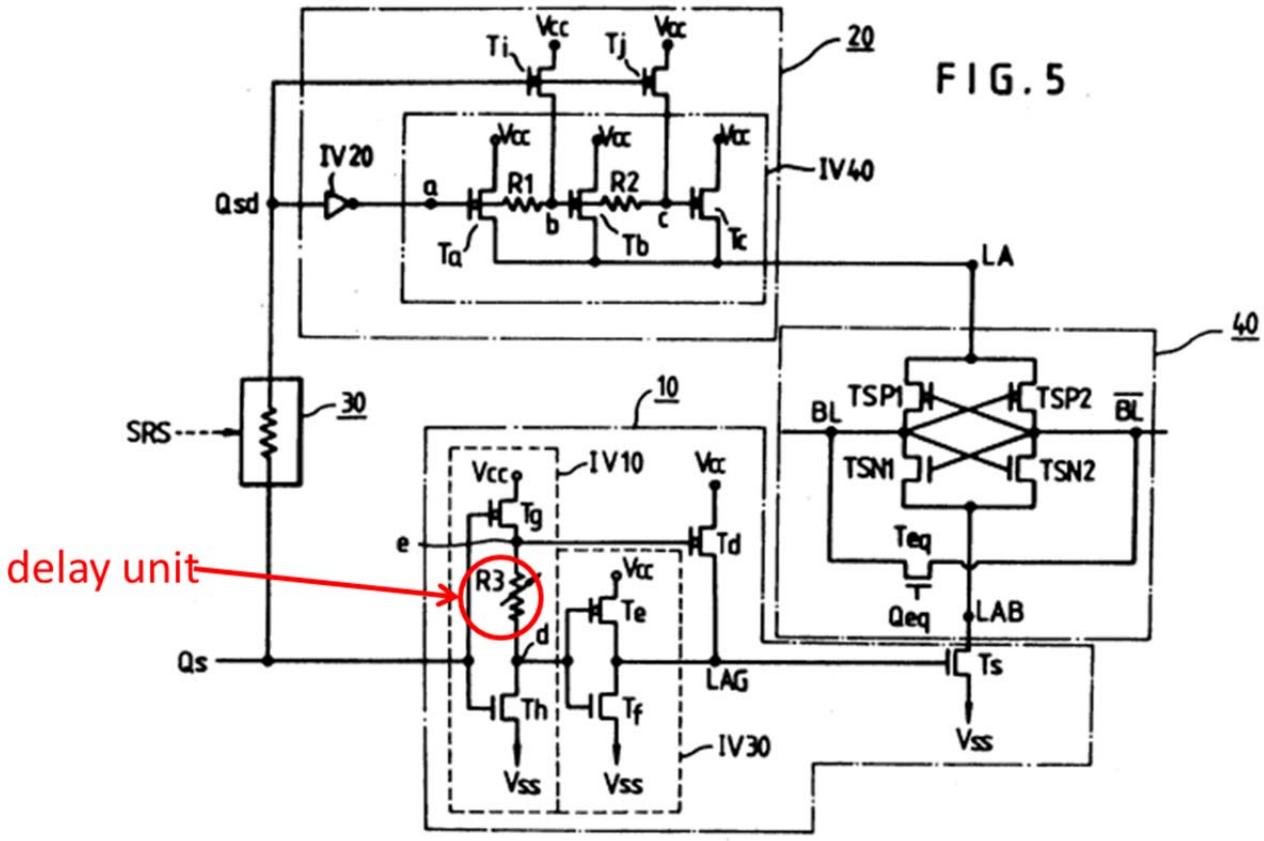


(Ex. 1005, FIG. 9 (excerpt, annotated Ex. 1002, ¶125.)

Therefore, ϕ_{SP2} is a "delayed sense control signal" given that, as explained above, there is a delay between ϕ_{SP1} and ϕ_{SP2}. (Ex. 1002, ¶126.) By generating a delay between ϕ_{SP1} and ϕ_{SP2}, *Min* discloses the function of "generating a delayed sense control signal," as recited in claim 1(e). (*Id.*)

While *Min* does not explicitly disclose the corresponding structure that generates the delayed sense control signal (one or more circuit components that delay a signal and equivalents thereof), it would have been obvious to implement such features in light of the disclosure of *Seo*. (Ex. 1002, ¶127.)

Seo discloses sense amplifier driver circuitry in FIG. 5. (Ex. 1004, 5:50-11.) The sense amplifier driver circuitry includes a resistance R3 that delays the signal between nodes e and d. (*Id.*, 6:59-7:2.) Specifically, resistance R3 delays the signal d, which falls "to Vss level immediately owing to the function of . . . inverter IV10," to generate a delayed signal at node e. (*Id.*; Ex 1002, ¶128.) Therefore, resistance R3 is "one or more circuit components that delay a signal." (Ex. 1002, ¶128.)



(Ex. 1005, FIG. 5 (annotated); Ex. 1002, ¶128.)

A POSITA would have looked to *Seo* to refine the teachings of *Min*, because both references are directed to sense amplifiers for memory. (Ex. 1002, ¶129.) Having looked to *Seo*, such a person would have been motivated to modify *Min* to include circuit components for implementing a delay using a circuit component similar to delaying resistance R3 in order to generate a delay between ϕ_{SP1} and ϕ_{SP2} in *Min*. (*Id.*) For example, such a person would have recognized the need to implement the above delay functionality (*i.e.*, delay between ϕ_{SP1} and ϕ_{SP2}) using some structure in a circuit, and would have been motivated to include a delaying

resistance R3 between ϕ_{SP1} and ϕ_{SP2} (with ϕ_{SP1} as the input node to the resistance R3 and ϕ_{SP2} as the output node of the resistance R3) to meet this need. (*Id*.) Indeed, the above modification of *Min* based on *Seo* would have been a mere combination of known elements (*Seo*'s delaying resistance R3 and *Min*'s gates of respective transistors Q112, Q115) according to known methods (*e.g.*, connecting R3 between ϕ_{SP1} and ϕ_{SP2}), to yield predictable results (*e.g.*, yield ϕ_{SP2} as a delayed version of ϕ_{SP1}). (*Id.*) *KSR*, 550 U.S. at 416. Given that the above modification of *Min* based on *Seo* would not have adversely affected the operation of the sense amplifier driving circuitry in *Min* and would have been within the realm and knowledge of a POSITA, the modification would have been obvious. (Ex. 1002, ¶129.) *KSR*, 550 U.S. at 416-21.

As discussed above, the combined *Min-Seo* system would have included a delaying resistance (*e.g.*, a resistance such as resistance R3 in *Seo*) coupled between ϕ_{SP1} (*i.e.*, gate of Q112) and ϕ_{SP2} (*i.e.*, gate of Q115) to delay ϕ_{SP1} and generate ϕ_{SP2}. As such, the combined system discloses "a delay unit" (R3) "coupled to the sense control signal node" (the gate of Q112; *supra* Section IX.B.1(b)) "and generating a delayed sense control signal" (generating ϕ_{SP2} as a delayed version of ϕ_{SP1}). (Ex. 1002, ¶130.)

f) "a second impedance having a terminal coupled to the selected logic level signal; and"

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶131.) For example, *Min* discloses that the resistance ("a second impedance") of transistor Q115 has a terminal coupled to Vss ("the selected logic level signal") through transistor Q116. (Ex. 1002, ¶131; Ex. 1005, FIG. 9.)

As discussed above for claim 14(f), the resistance R_{tot} of transistor Q115 is a "second impedance" and one "terminal" of this impedance is the node at the bottom of Rs. (*Supra* Section IX.A.1(f).) The impedance of transistor Q115 may be represented as shown above for claim 14(f). (Ex. 1002, ¶132; Ex. 1005, FIG. 9 (representation of transistor Q115); *supra* Section IX.A.1(f).)

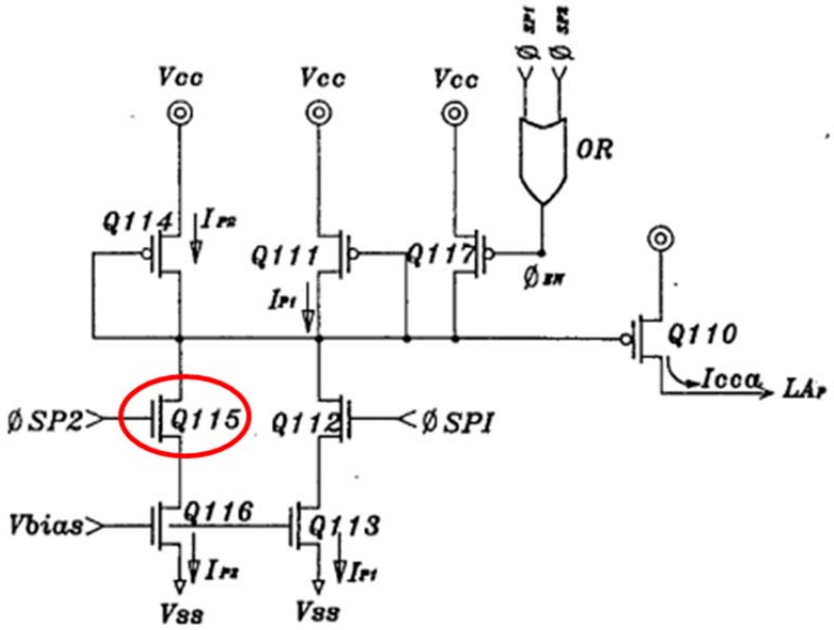
As seen from the illustration in Section IX.A.1(f), the bottom node of Rs is coupled to Vss ("selected logic level signal") because current I_{P1} flows through Q115 (including bottom node of Rs) to Vss. (Ex. 1002, ¶133.) Therefore, *Min* discloses "a second impedance having a terminal coupled to the selected logic level signal." (*Id*.)

g) "a second switch having current carrying electrodes coupled to drive the clock signal to the selected logic level through the second impedance,"

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶134-136.) For example, *Min* discloses a transistor Q115 ("a second switch") having source

and drain terminals ("current carrying electrodes"). (Ex. 1005, FIG. 9.) Transistor Q115 is shown in FIG. 9 of *Min*:

FIG. 9



(Ex. 1005, FIG. 9 (excerpted and annotated); Ex. 1002, ¶134.)

The source and drain terminals ("current carrying electrodes") of transistor Q115 ("second switch") along with the various parasitic and channel resistances are described above for claim 14(f). (Ex. 1002, ¶135; Ex. 1005, FIG. 9 (representation of transistor Q115); *supra* Section IX.A.1(f).)

As seen from FIG. 9, *Min* discloses that a current I_{P2} flows through switch Q115. (Ex. 1005, FIG. 9.) Accordingly, a POSITA would have understood that in order for Q115 to draw current I_{P2}, it has to pull down the gate of transistor Q114,

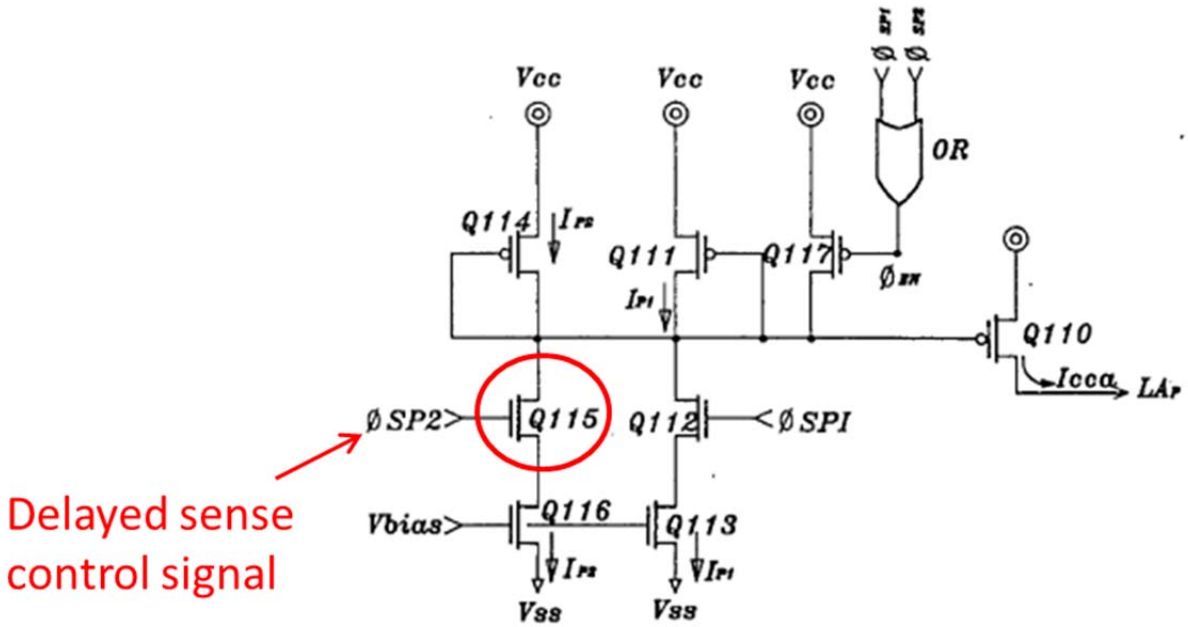
which as seen from FIG. 9, is also connected to the gate of transistor Q110[11] ("clock signal"; *supra* Section IX.B.1(a)). (Ex. 1002, ¶136; Ex. 1005, FIG. 9.) That is, in order for Q115 to draw current I_{P2}, it has to pull the gate of Q114 (which is connected to the gate of Q110) towards Vss ("to a selected logic level") through the resistance of transistor Q115 ("second impedance"). (Ex. 1002, ¶136.) The gate voltage of Q110 ("clock signal") is therefore driven down towards Vss through the resistance of Q115 because the flow of current across the source and drain terminals of transistor Q115 requires that the current flow through the resistance (R_{tot}) of transistor Q115 (*see* annotated representation of Q115 above). (Ex. 1002, ¶136; *supra* Section IX.B.1(f).) Therefore, *Min* discloses "a second switch having current carrying electrodes coupled to drive the clock signal to the selected logic level through the second impedance." (Ex. 1002, ¶136.)

[11] As explained above regarding the preamble of claim 10, *Min* discloses that Q110 can be replaced by more than one driving transistor. (*Supra* Section IX.B.1(b).) The operation of the circuit of FIG. 9 described in this section remains the same regardless of whether there is a single driving transistor Q110 or a plurality of driving transistors. (Ex. 1002, ¶136fn.12..)

h) "the second switch controlled by the delayed sense control signal such that the first switch and the second switch are concurrently activated after the delayed sense control signal is generated.

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶137-140.) As discussed above, signal ϕ_{SP2} is a "delayed sense control signal." (*Supra* section IX.B.1(e).) Further, *Min* discloses that transistor Q115 ("second switch") is controlled by signal ϕ_{SP2} ("controlled by the delayed sense control signal"). (Ex. 1005, FIG. 9, 29:29-34.)

FIG. 9

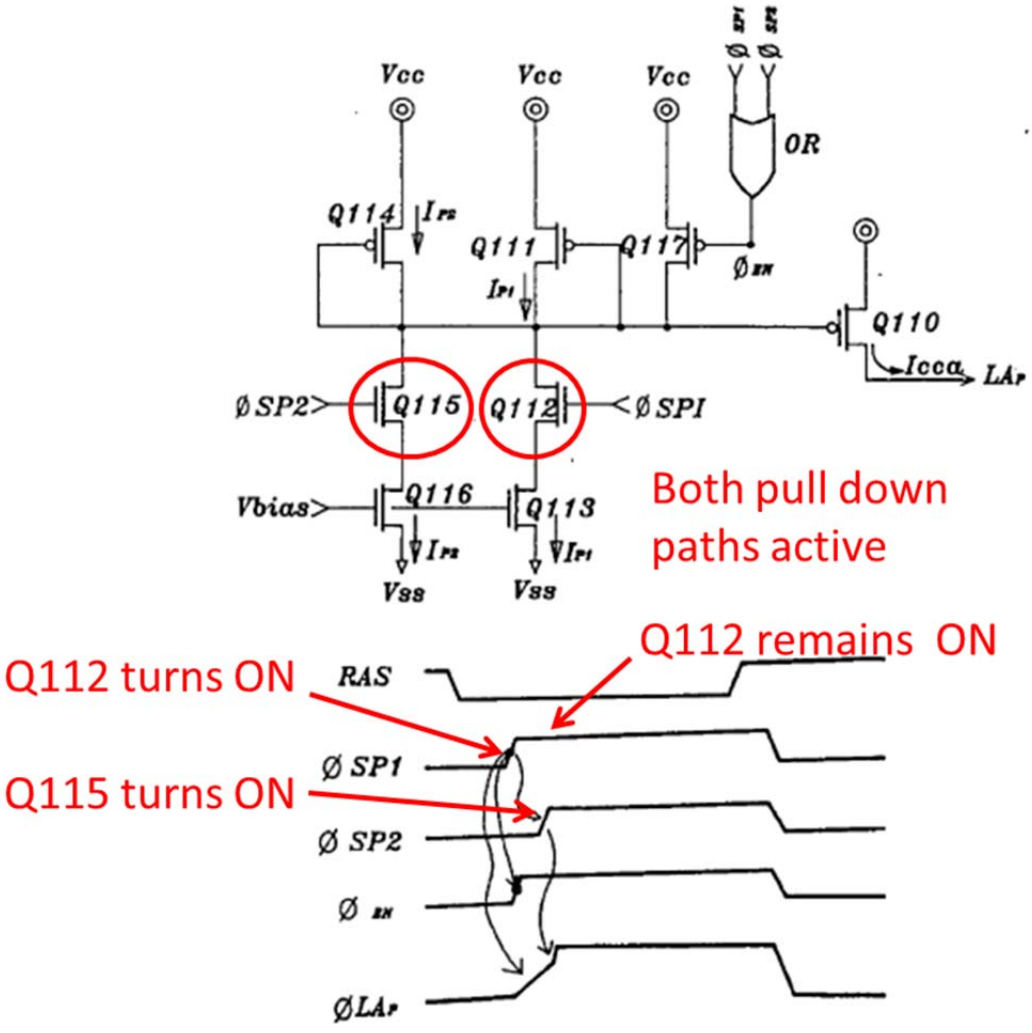


(Ex. 1005, FIG. 9 (excerpted and annotated); Ex. 1002, ¶137.)

Moreover, as discussed above in Section VII.C, signals ϕ_{SP1} and ϕ_{SP2} are both high (at Vcc) after the rising edge of signal ϕ_{SP2} as shown in the annotated

version of FIG. 9 below. Therefore, both current paths (*i.e.*, the path thru Q112 and the path thru Q115) are concurrently active because ϕ_{SP1} being high turns on Q112 and ϕ_{SP2} being high turns on Q115. (Ex. 1002, ¶138; *supra* Section IX.A.1(e)-IX.A.1(f).) The timing diagram in FIG. 9 confirms this feature:

FIG. 9



(Ex. 1005, FIG. 9 (excerpted and annotated); Ex. 1002, ¶138.)

As such, a POSITA would have understood that transistors Q112 ("the first switch") and Q115 ("the second switch") are "concurrently activated after the delayed sense control signal is generated." (Ex. 1002, ¶139.) In this respect, the disclosure in *Min* (*i.e.*, transistor Q112 turns on first, then transistor Q115 turns on, and transistor Q112 remains on) is identical to the disclosure in the '302 patent (*i.e.*, transistor 303 turns on first, then transistor 308 turns on, and transistor 303 remains on). (Ex. 1002, ¶139; Ex. 1001, 6:8-36, FIG. 3.)

2. Claim 11

a) "The clock driver circuit of claim 10 wherein the second impedance is less than the first impedance."

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶140-145.) As discussed above regarding claim elements 10(c) and 10(f), *Min* discloses transistors Q112 and Q115 which each have a resistance ("first impedance" and "second impedance," respectively). A POSITA would have known that the resistance R_{tot} of a transistor is given by the following equation:

$$R_{tot} = \frac{V_{ds}}{\mu_{eff} C_{ox} \frac{W}{L}\left((V_{gs} - V_t)V_{ds} - \frac{m}{2}V_{ds}^2\right)}$$

(Ex. 1008, 120, 206; Ex. 1002, ¶¶140-142.)

In other words, the resistance of a transistor such as *Min*'s transistors Q112 and Q115 is a function of the width-to-length ratio (*i.e.*, size) of the transistor. (Ex.

1002, ¶143.) Given *Min*'s disclosure of a pair of transistors Q112, Q115, a POSITA would have known that there are exactly three possible relationships between their sizes: transistors Q112 and Q115 have the same W/L ratio; transistor Q112 has a larger W/L ratio than Q115; or transistor Q112 has a smaller W/L ratio than Q115. (Ex. 1008, FIG. 9; Ex. 1002, ¶143.) Therefore, a POSITA would have known, based on the equation above, that depending on the relative W/L ratios of the transistors (whether they are equal or whether one is larger than the other), the transistors' relative resistances also have three possibilities: the resistance of Q112 equals the resistance of Q115; resistance of Q112 is less than the resistance of Q115; or resistance of Q115 is less than the resistance of Q112. (Ex. 1002, ¶143.)

It was within the capability of a POSITA to design and implement transistors of various sizes (W/L ratios), and such a person would have been motivated to try different relative sizes for *Min*'s transistors Q112 and Q115 in order to achieve a working, stable sense amplifier driver circuit for a particular implementation. (Ex. 1002, ¶144.) Because *Min* teaches the need for a stable, rapid driving of sense amplifiers (Ex. 1005, 30:1-3) and because of the finite number (3) of identified predictable solutions in terms of size relationships between transistors Q112 and Q115 as explained above, a POSITA would have had good reason to try all three possible size relationships. (Ex. 1002, ¶144.) *KSR*, 550 U.S. at 421. It would therefore have been obvious to try all three possible size

relationships for this pair of transistors, and it would therefore have been obvious to have the second impedance be less than the first impedance by virtue of the above-described relationship between relative sizes and relative resistances for transistors. (Ex. 1002, ¶144.) *KSR*, 550 U.S. at 421.

3. Claim 12

a) "The clock driver circuit of claim 10 wherein the first switch and the second switch are coupled to drive the timer unit output in parallel."

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶145.) Although claim 12 recites "the timer unit output," that term does not have antecedent basis. Therefore, claim 12 is indefinite under 35 U.S.C. § 112(b). To the extent Patent Owner contends that the term "timer unit output" should be interpreted as "the clock signal," *Min* discloses that transistors Q112 ("the first switch") and Q115 ("the second switch") are coupled to drive the signal at the gate of transistor Q110 ("the clock signal") in parallel. (*Supra* Section IX.B.1(h).) As discussed above for claim 10(h), *Min* discloses that both transistors Q112 and Q115 concurrently drive the signal at the gate of transistor Q110 to a low value (*i.e.*, drive that signal "in parallel") once transistor Q115 is turned on. (Ex. 1005, 29:21-30:3; Ex. 1002, ¶145; *supra* section IX.B.1(h).)

4. Claim 1

a) "A memory device comprising:"

To the extent that the preamble is determined to be limiting, *Min* discloses this feature. (Ex. 1002, ¶146.) For example, *Min* discloses that the driving circuit of FIG. 9 is suitable for use in a "high density semiconductor memory device." (Ex. 1005, 1:4-9.) Based on such disclosure, a POSITA would have understood that *Min* discloses "a memory device." (Ex. 1002, ¶146; citations and analysis below for the remaining elements of this claim.)

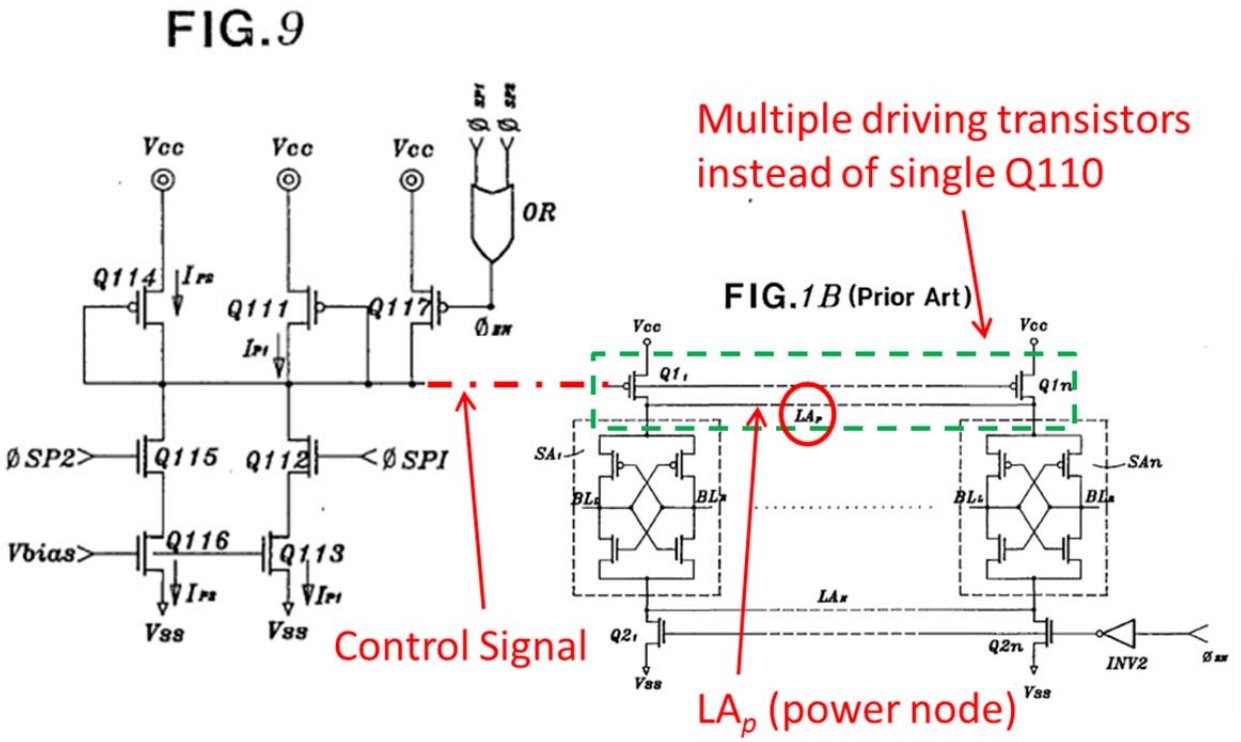
b) "a plurality of sense amplifiers distributed about an integrated circuit chip, each sense amplifier having a power node for receiving current;"

Min discloses or suggests this feature. (Ex. 1002, ¶¶147-151.) With respect to FIG. 9, *Min* discloses a "sense amplifier driving circuit[]" in which transistor Q110 drives "a plurality of sense amplifiers." (Ex. 1005, 27:22-30, FIG. 9; *supra* Section VII.C.) Furthermore, instead of a single driving transistor Q110, the circuit of FIG. 9 may drive a plurality of driving transistors. (Ex. 1005, 28:4-8.) But FIG. 9 does not provide explicit details regarding the distribution of the sense amplifiers and does not explicitly illustrate the sense amplifiers and their power nodes. (Ex. 1002, ¶147.) Nor does FIG. 9 explicitly illustrate how the plurality of driving transistors would have been connected to the "plurality of sense amplifiers." (*Id*.) It would have been obvious to a POSITA, however, to combine the circuit of

FIG. 9 and the conventional sense amplifier configuration of FIG. 1B, which includes a plurality of driving transistors $Q1_1$-$Q1_n$ that are connected to a plurality of sense amplifiers SA_1-SA_n. (*Id*.; *supra* Section IX.A.1(b) (explaining in detail the combination of FIG. 9 and FIG. 1B along with the reasons for combination).) The combination may be pictorially represented as shown above with respect to claim 14(b). (*Supra* Section IX.A.1.b.) The combined FIG. 9 – FIG. 1B system discloses "a plurality of sense amplifiers" SA_1-SA_n as illustrated above and *Min* discloses providing the sense amplifiers in "a high density semiconductor memory device," which a POSITA would have understood to be an "integrated circuit chip." (Ex. 1005, 1:4-9; *see also id*., 12:12-13; Ex. 1002, ¶¶148-149.) Therefore, a POSITA would have understood that sense amplifiers SA_1-SA_n in such "a high density semiconductor memory device" would have been distributed about the memory device in accordance with design and layout needs. (Ex. 1002, ¶150.) Indeed, each of the sense amplifiers SA_1-SA_n would have had to be placed somewhere on the chip in the memory device and they would therefore have had to be "distributed." (*Id*.)

Min discloses that each of the sense amplifiers SA_1-SA_n has a node (LA_P) that a POSITA would have understood to be a "power node for receiving current," because when the driving transistors $Q1_1$-$Q1_n$ are on, the node LA_P would receive current flowing from the positive power terminal Vcc. (Ex. 1005, FIG. 1B, FIG. 9

(annotated below); Ex. 1002, ¶151.) *Min* confirms that node LA_P would receive current flowing from the positive power terminal Vcc when it explains that current Icca from power supply Vcc is provided to latch node LA_P through driving transistor Q110. (Ex. 1005, 29:18-34, FIG. 9.)



(Ex. 1005, FIG. 9, FIG. 1B (excerpted and annotated); Ex. 1002, ¶151.)

c) "a low-impedance power supply conductor;"

Min discloses or suggests this feature. (Ex. 1002, ¶¶152-155.) For instance, *Min* discloses a power supply conductor Vcc as shown in FIG. 9. (Ex. 1005, FIG. 9; Ex. 1002, ¶¶152.) It was well known to a POSITA that parasitic resistance

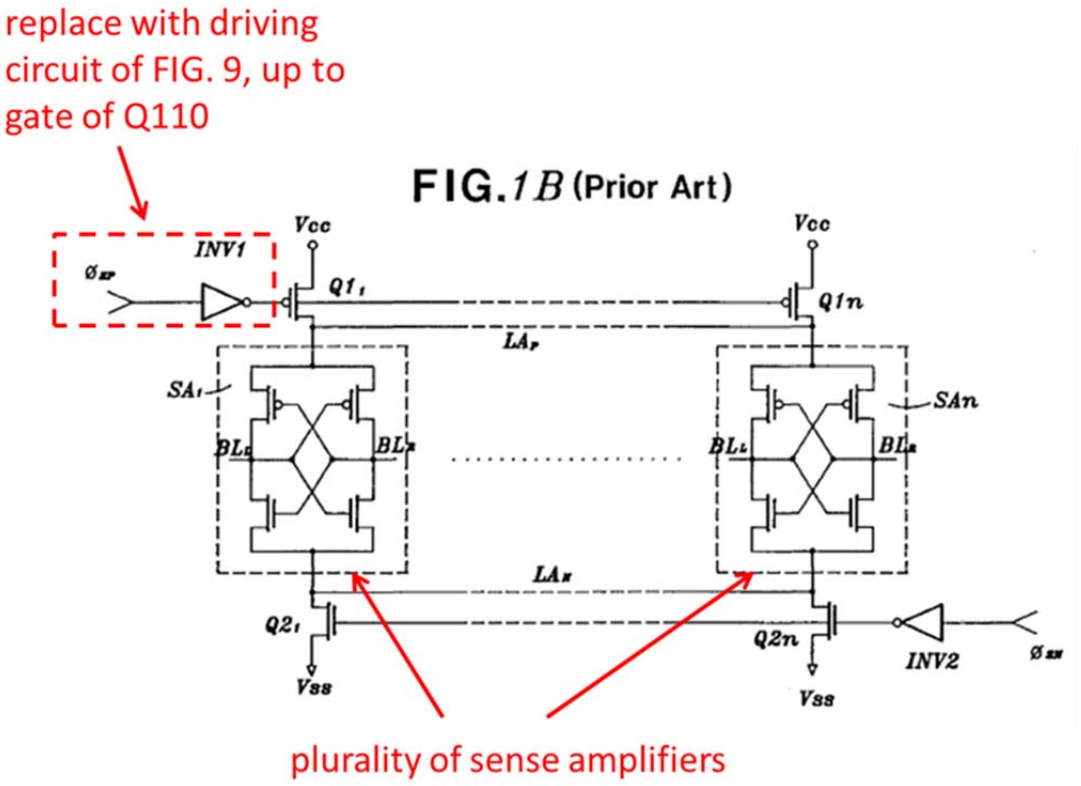
("impedance") is present along any conductor. (Ex. 1002, ¶153; *see also* Ex. 1006, 2:24-3:2, FIG. 1.)

It was well known to a POSITA that because of a parasitic resistance 34, the voltage along the conductor will drop such that a different voltage is provided to different devices that share that conductor. (Ex. 1002, ¶154; Ex. 1006, 2:33-44.) In fact, it was well known that a higher parasitic resistance would have resulted in greater delays for the signal propagating along the conductor or for a sense amplifier. (Ex. 1002, ¶154.) Therefore, it was nothing new at the time of the invention of the '302 patent to design a power supply conductor (*e.g.*, the power supply conductor in *Min* that provides Vcc to the driving transistors $Q1_1$-$Q1_n$) to have a lower parasitic resistance. (*Id*.) That is, given the well-known problem of parasitic resistance along a power supply conductor, a POSITA would have been motivated to decrease this parasitic resistance to lower the voltage variation along the conductor and also to reduce the signal delay resulting from the higher parasitic resistance. (Ex. 1002, ¶154.)

Therefore, a POSITA would have been motivated to use a "low-impedance" power supply conductor *(e.g.*, a conductor with a lower parasitic resistance) for *Min*'s Vcc power supply conductor given that a high impedance conductor would have caused the issues discussed above. (Ex. 1002, ¶155.) *KSR*, 550 U.S. at 401.

d) "at least one drive transistor having a first current carrying electrode coupled to the power supply conductor, a second current carrying electrode coupled to the power nodes of a preselected number of the sense amplifiers, and a control electrode;"

Min discloses or suggests this feature. (Ex. 1002, ¶¶156-157.)



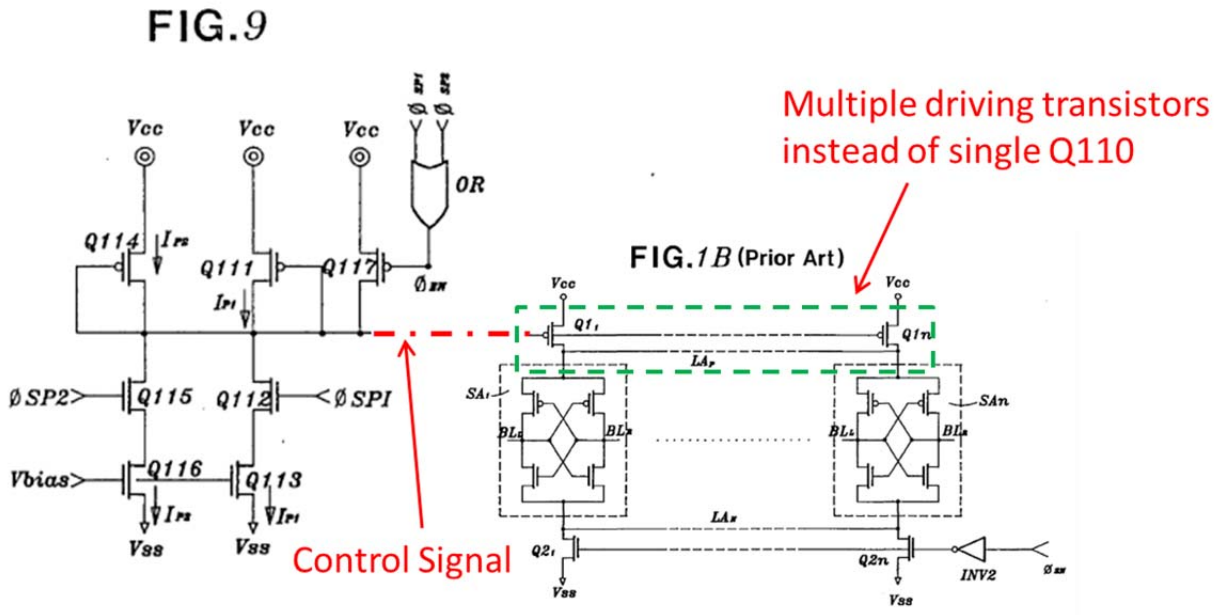
(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶156.)

As seen from the above illustration, in the combined FIG. 9-FIG. 1B system each driving transistor $Q1_1$-$Q1_n$ ("at least one drive transistor") has a source terminal ("having a first current carrying electrode") coupled to power source Vcc ("power supply conductor,") and a gate terminal ("a control electrode"). (Ex. 1002, ¶157.) A POSITA would have understood that node LA_P constitutes the "power

nodes" of n sense amplifiers SA_1-SA_n ("preselected number of the sense amplifiers") as shown in above FIG. 1B, because node LA_P provides current from power supply (Vcc) to the sense amplifiers when the driving transistor(s) $Q1_1$-$Q1_n$ are on. (Ex. 1002, ¶157; *supra* Section IX.A.1(b).)

e) "a control line coupled to the control electrode;"

Min discloses or suggests this feature. (Ex. 1002, ¶158.) As can be seen in the illustration below for the combined FIG. 9-FIG. 1B system, a control signal is coupled to the gate ("control electrode") of each of the driving transistors $Q1_1$-$Q1_n$.



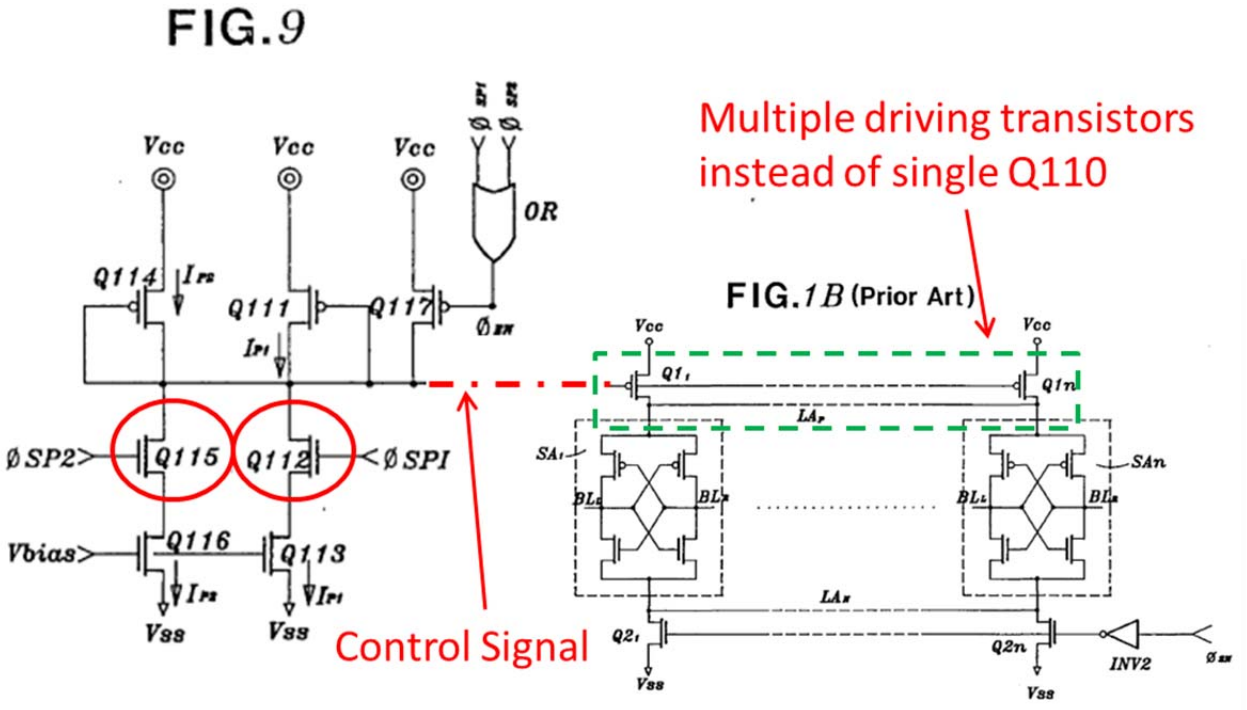
(Ex. 1005, FIG. 1B, FIG. 9 (annotated), Ex. 1002, ¶158.)

f) "a timer unit having an output coupled to the control electrode and generating a control signal;"

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶159-162.) As explained above, this claim limitation is a means-plus-function term which has

the function of "generating a control signal" and the corresponding structure of at least a pair of transistors and one or more circuit components that delay a signal. (*Supra* Section VIII.A.)

As discussed above for claim 1(b), the combined FIG. 9 – FIG. 1B system (*see* annotated illustration below) includes, *inter alia*, the sense amplifier driving circuit of FIG. 9 controlling a plurality of driving transistors $Q1_1$-$Q1_n$ that drive a plurality of sense amplifiers SA_1-SA_n where the driving transistors $Q1_1$-$Q1_n$ are connected to the sense amplifiers at the power node LA_P. (*Supra* Section IX.B.4(b).)



(Ex. 1005, FIG. 1B, FIG. 9 (annotated), Ex. 1002, ¶160.)

Therefore, as illustrated above, the combined FIG. 9 – FIG. 1B system includes transistors Q115 and Q112, which constitute "at least a pair of transistors." Moreover, as discussed above for claim 10(e), it would have been obvious to combine the sense amplifier driving circuit of FIG. 9 with *Seo* to provide a delaying resistance between ϕ_{SP1} and ϕ_{SP2} to generate ϕ_{SP2} as a delayed version of ϕ_{SP1}. (*Supra* Section IX.B.1(e.) Therefore, the combined *Min-Seo* system discloses a delaying resistance ("one or more circuit components that delay a signal") between ϕ_{SP1} and ϕ_{SP2}. Accordingly, the combined *Min-Seo* system discloses the corresponding structure for "timer unit." (Ex. 1002, ¶161.)

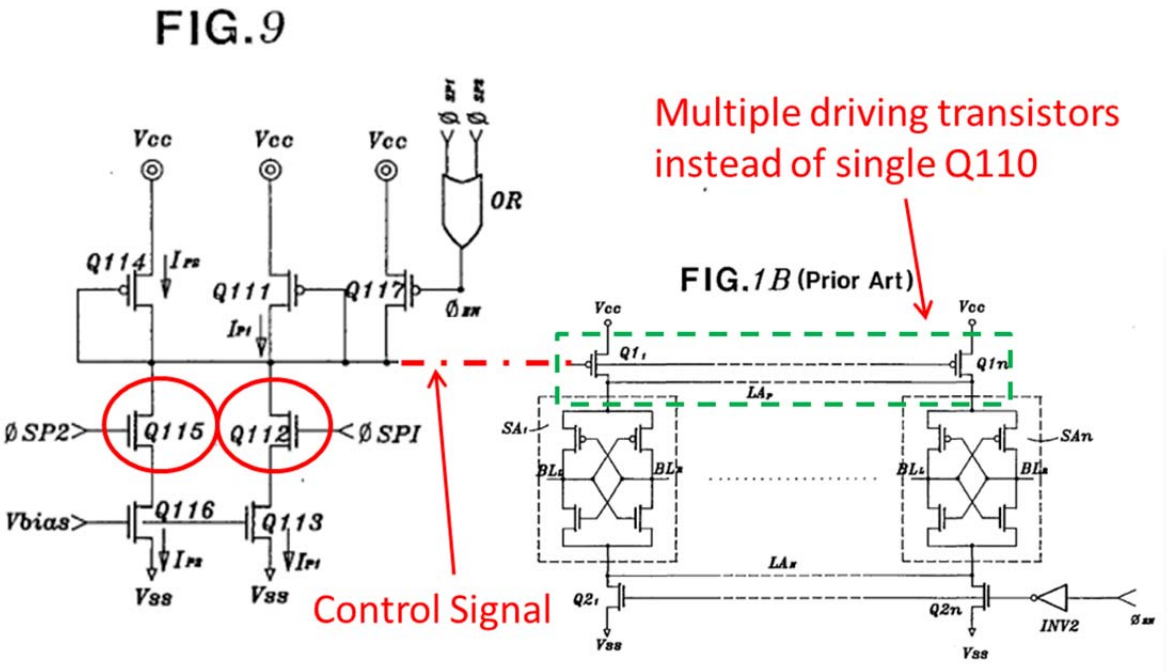
As can be readily seen from the above illustration, transistors Q115 and Q112 are coupled to the control signal, which is also the signal provided to the gate terminals ("control electrode") of the driving transistors $Q1_1$-$Q1_n$. (Ex. 1005, FIG. 9; *see also supra* Section IX.B.4(e).) Moreover, transistors Q112 and Q115 drive the control signal by pulling down on the gate terminal ("control electrode") of the driving transistors $Q1_1$-$Q1_n$. (*Supra* Sections IX.B.1(d) and IX.B.1(g), explaining that switches Q112 and Q115 drive the signal provided to the gate terminal of driving transistors $Q1_1$-$Q1_n$.) Therefore, the combined *Min-Seo* system discloses "the timer unit having an output coupled to the control electrode." (Ex. 1002, ¶162.) Because transistors Q112 and Q115 drive the control signal by pulling down on the gate terminal ("control electrode") of the driving transistors $Q1_1$-$Q1_n$,

the combined *Min*-Seo system discloses the claimed function of "generating a control signal," which is the signal at the gate terminals of driving transistors $Q1_1$-$Q1_n$. (Ex. 1002, ¶162.)

> g) "a first component within the timer unit causing the control signal to change from a first logic level towards a second logic level at a first rate; and"

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶163-169.) As explained above, this claim limitation is a means-plus-function term which has the function of "causing the control signal to change from a first logic level towards a second logic level at a first rate" and the corresponding structure of "a first transistor" and its equivalents. (*Supra* Section VIII.B.)

As discussed above (*supra* Section IX.A.4(f)), the combined *Min-Seo* system includes the combined FIG. 9 – FIG. 1B system with a delaying resistance coupled between ϕ_{SP1} and ϕ_{SP2} to generate ϕ_{SP2} as a delayed version of ϕ_{SP1}. Other than the delaying resistance, the illustration below pictorially illustrates the combined *Min-Seo* system. (Ex. 1002, ¶164.)



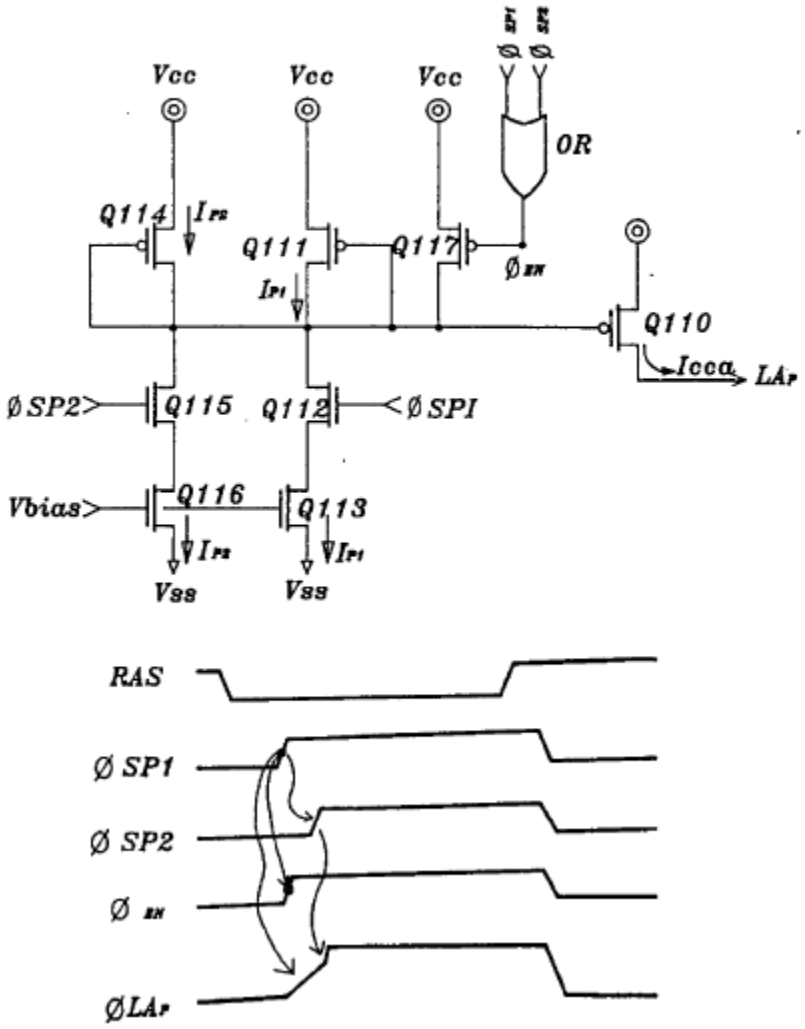
(Ex. 1005, FIG. 1B, FIG. 9 (excerpted and annotated), Ex. 1002, ¶164.)

As seen above, the combined *Min-Seo* system includes transistor Q112, which is a "first transistor within the timer unit" where the timer unit, as discussed above, is the combination of Q112, Q115, and a delaying resistance. (Ex. 1002, ¶165; *supra* Section IX.B.4(f).)

Moreover, in the combined *Min-Seo* system, Q112 causes the voltage at the gate of the driving transistors $Q1_1$-$Q1_n$, *i.e.*, the "control signal," to change from Vcc ("first logic level") towards Vss ("second logic level"). (Ex. 1005, 29:18-29, FIG. 9; Ex. 1002, ¶166.) For instance, a POSITA would have understood that because signals ϕ_{SP1} and are ϕ_{SP2} are both initially at low voltage as shown in FIG. 9, the output of the OR logic gate shown in FIG. 9 is initially a logic low ('0'),

which turns on PMOS pull-up transistor Q117, thereby charging the node at the gate of transistor Q110 to Vcc. (Ex. 1005, FIG. 9; Ex. 1002, ¶167.)

FIG. 9

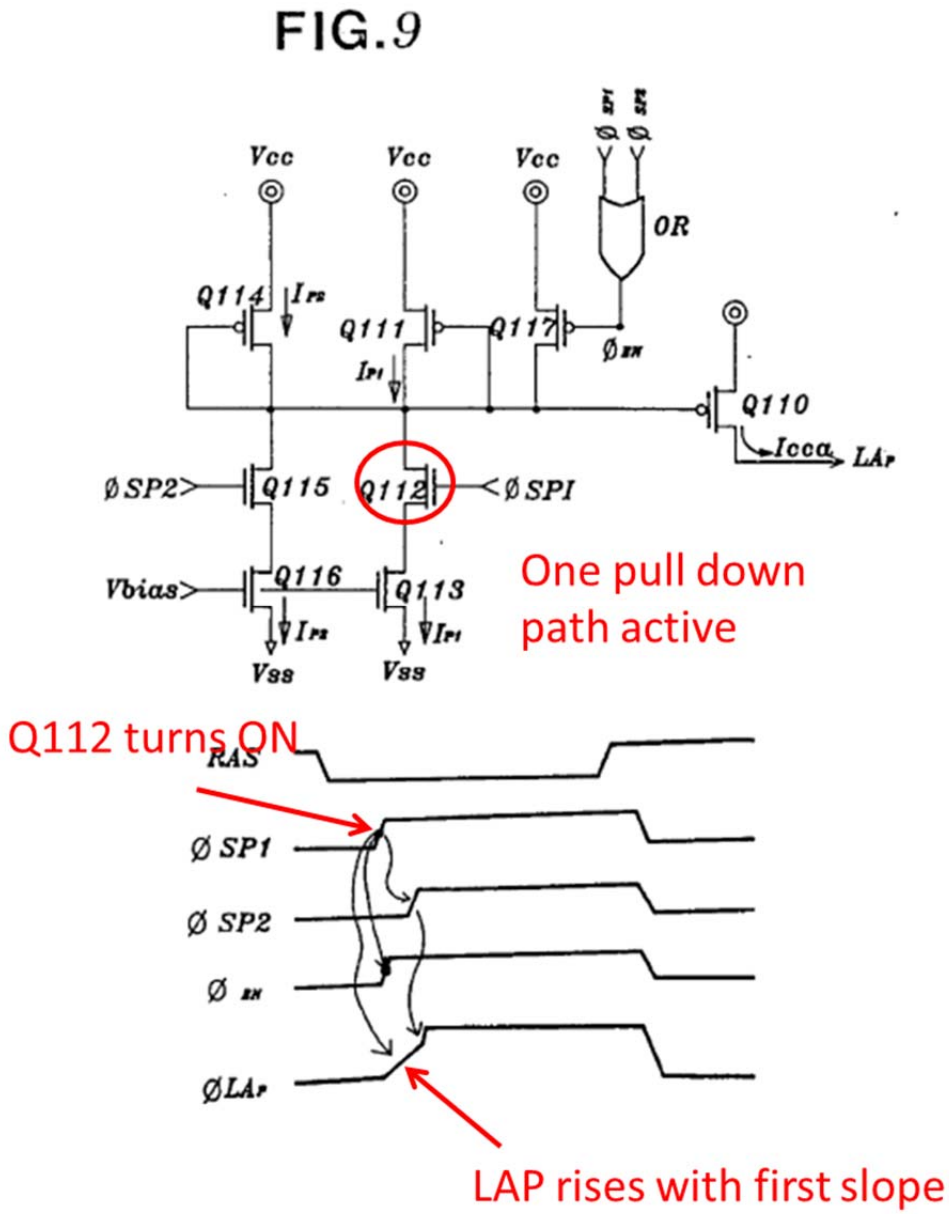


(Ex. 1005, FIG. 9.)

When signal ϕ_{SP1} is set to a high level, transistor Q112 is turned on, and because transistor Q113 is also on due to the voltage Vbias applied to its gate, a pull-down path is enabled to pull down the voltage at the gate voltage ("control

signal") of transistor Q110 from Vcc ("first logic level") towards Vss ("second logic level"). (*Supra* Section IX.B.1(d), explaining that the gate voltage of Q110 ("clock signal") is driven down towards Vss by Q112; Ex. 1002, ¶168.)

The pull-down of the voltage at the gate of transistor Q110 (and therefore, at the gate of driving transistors $Q1_1$-$Q1_n$ in the combined system) occurs at a rate corresponding to the "first slope" (shown in the annotated figure below) associated with the rising voltage of node LA_p because as the gate voltage of transistor Q110 falls (*i.e.*, the "control signal" falls at a "first rate"), transistor Q110 turns on to increase the voltage at node LA_P. (Ex. 1005, 29:28-29 ("node LA_P begins to gradually rise with a first slope"), FIG. 9; Ex. 1002, ¶168.) Therefore, *Min* discloses Q112 "causing the control signal to change from a first logic level towards a second logic level at a first rate." (Ex. 1002, ¶168.)



(Ex. 1005, FIG. 1B, FIG. 9 (excerpted and annotated); Ex. 1002, ¶168.)

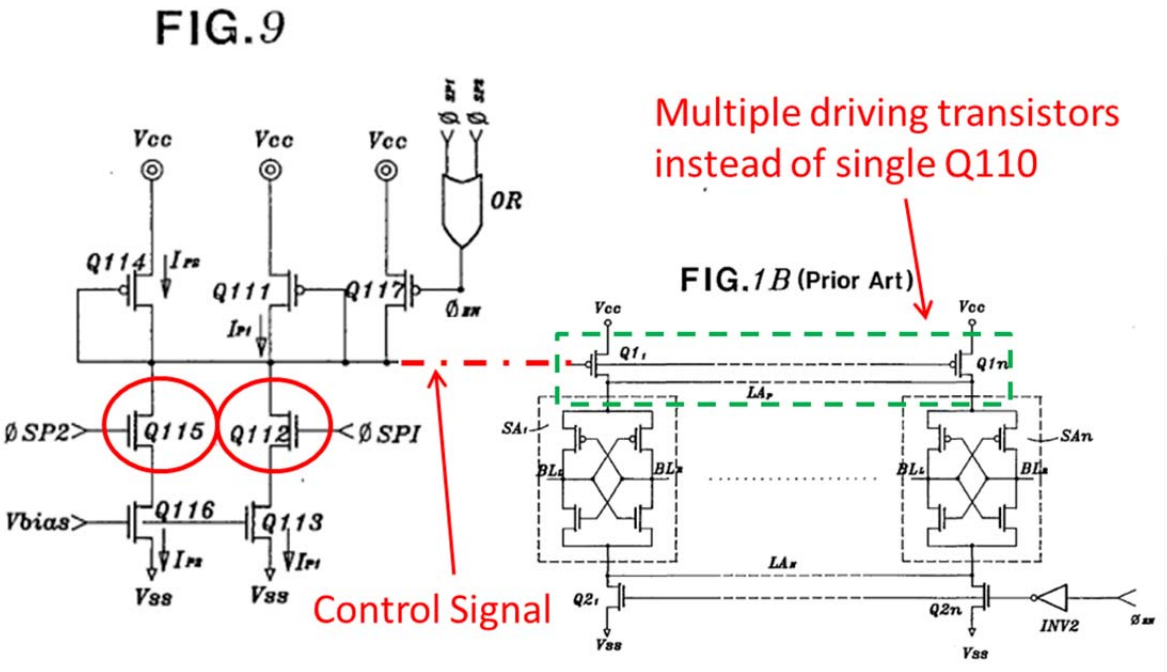
Thus, *Min* discloses the recited function of this means-plus-function term ("causing the control signal to change from a first logic level towards a second logic level at a first rate") and also discloses the structure corresponding to that

recited function, ***i.e.***, transistor Q112 ("first transistor"), which is "within the timer unit" as shown in FIG. 9. (Ex. 1005, FIG. 9; Ex. 1002, ¶169.)

> h) "a second component within the timer unit causing the control signal to change to the second logic level at a second rate, wherein the second rate is greater than the first rate"

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶170-174.) As explained above, this limitation is a means-plus-function which has the function of "causing the control signal to change to the second logic level at a first rate" and the corresponding structure of "a second transistor" and its equivalents. (*Supra* Section VIII.C.)

As discussed above (*supra* Section IX.B.4(f)), the combined *Min-Seo* system includes the combined FIG. 9 – FIG. 1B system with a delaying resistance coupled between ϕ_{SP1} and ϕ_{SP2} to generate ϕ_{SP2} as a delayed version of ϕ_{SP1}. Other than the delaying resistance, the illustration below pictorially illustrates the combined *Min-Seo* system. (Ex. 1002, ¶171.)



(Ex. 1005, FIG. 1B, FIG. 9 (excerpted and annotated), Ex. 1002, ¶171.)

As seen above, the combined *Min-Seo* system includes transistor Q115, which is a "second transistor within the timer unit" where the timer unit, as discussed above, is the combination of Q112, Q115, and a delaying resistance. (Ex. 1002, ¶173; *supra* Section IX.B.4(f).)

Min discloses that "[a]fter a certain period of time, the second active restore enable signal ϕ_{SP2} goes to a high level, and the transistor Q115 . . . is turned on." (Ex. 1005, 29:29-34.) Because transistor Q116 is also in the on (conducting) state due to the voltage Vbias applied at its gate, a pull-down path including transistors Q115 and Q116 is enabled, which pulls down the voltage at the gate of transistor Q110. (Ex. 1005, FIG. 9; Ex. 1002, ¶173.) As a result, "the current Icca flowing

through the driving transistor Q110 is increased. The voltage ϕLA_P of the active restore driving signal increases with *a second slope*." (Ex. 1005, 29:33-30:1 (emphasis added).) Therefore, a POSITA would have understood that the turn-on of transistor Q115 causes the voltage at the gate of transistor Q110 ("causing the control signal") to change to Vss ("to change the second logic level") at a second rate corresponding to the "second slope" disclosed in *Min*. (Ex. 1002, ¶173.) Moreover, as seen from the timing diagram of FIG. 9, the second slope is greater than the first slope and therefore, *Min* discloses that "the second rate is greater than the first rate." (Ex. 1005, 29:27-30:3, FIG. 9; Ex. 1002, ¶173.)

Thus, *Min* discloses the recited function of this means-plus-function term ("causing the control signal to change to the second logic level at a second rate") and also discloses the structure corresponding to that recited function, ***i.e.***, transistor Q115 ("second transistor"), which is "within the timer unit" as shown in FIG. 9. (Ex. 1005, FIG. 9; Ex. 1002, ¶174.)

> i) "such that the first component and the second component are concurrently activated to cumulatively affect the rate of change to the second logic level."

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶175.) As discussed above at Section IX.B.1(h), *Min* discloses that transistors Q112 ("first component") and Q115 ("second component") are concurrently activated so that they both pull down the gate voltage ("control signal") of transistor Q110 to Vss

("selected second logic level signal"). Therefore, Q112 and Q115 "cumulatively affect the rate of change [of the control signal] to the second logic level." (*Supra* Section IX.B.1(h); Ex. 1005, 29:18-34, FIG. 9; Ex. 1002, ¶175.)

5. Claim 2

a) "The memory device of claim 1 further comprising a conductor coupling the power nodes of a number of sense amplifiers."

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶176-177.) In the system as set forth above (*supra* section IX.B.4(b)), the power nodes of the sense amplifiers SA_1-SA_n are coupled by a conductor (the line LA_p). (Ex. 1002, ¶177 (discussing annotated FIG. 1B of Ex. 1005).)

6. Claim 3

a) "The memory device of claim 2 wherein the at least one drive transistor is provided for each sense amplifier."

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶178-179.) In the system as set forth above (*supra* Section IX.B.4(b)), each sense amplifier among SA_1-SA_n is provided with a respective driver transistor $Q1_1$-$Q1_n$. (Ex. 1002, ¶179 (discussing annotated FIG. 1B of Ex. 1005); Ex. 1005, 4:5-17.)

7. Claim 4

a) "The memory device of claim 2 wherein the at least one drive transistor comprises a drive transistor that is shared by each of the number of sense amplifiers coupled to the conductor."

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶180-181.)

In the system as set forth above (*supra* Section IX.B.4(b)), each sense amplifier among SA_1-SA_n receives current from more than one of driving transistors $Q1_1$-$Q1_n$ because each of the sense amplifiers is connected to the common LA_P node. (Ex. 1002, ¶181 (discussing annotated FIG. 1B of Ex. 1005).) Thus, a POSITA would have understood that "each sense amplifier" in *Min*'s system "receives current from more than one drive transistor." (Ex. 1002, ¶181.)

8. Claim 5

a) "The memory device of claim 2 wherein each sense amplifier receives current from more than one drive transistor."

Min in view of *Seo* discloses or suggests this feature. (Ex. 1002, ¶¶182-183.) In the system as set forth above (*supra* section IX.B.4(b)), each sense amplifier among SA_1-SA_n receives current from more than one of driving transistors $Q1_1$-$Q1_n$ because each of the sense amplifiers is connected to the common LA_P node. (Ex. 1002, ¶183 (discussing annotated FIG. 1B of Ex. 1005).) Thus, a POSITA would have understood that "each sense amplifier" in *Min*'s system "receives current from more than one drive transistor." (*Id.*)

C. Ground 3: *Min, Seo,* and *Schuster* Render Obvious claim 6

1. Claim 6

a) "The memory device of claim 1 further comprising:
a data line;
a latch node in the sense amplifier to hold a signal generated by the sense amplifier; and
a pass transistor coupled between the latch node and the data line."

Min in view of *Seo* and *Schuster* discloses or suggests this feature. (Ex. 1002, ¶¶184-191.) As discussed above (*supra* Section IX.A.4(f)), the combined *Min-Seo* system includes the combined FIG. 9 – FIG. 1B system with a delaying resistance coupled between ϕ_{SP1} and ϕ_{SP2} to generate ϕ_{SP2} as a delayed version of ϕ_{SP1}.

In the combined system, each sense amplifier SA_1-SA_n includes two latch nodes, each of which is connected to a left bit line BL_L, or a right bit line BL_R. (Ex. 1005, FIGS. 1A, 1B, 2:11-13; Ex. 1002, ¶¶186-197.) The latch node holds a signal generated by the sense amplifier. (Ex. 1002, ¶187.)

While *Min* and *Seo* do not expressly disclose a data line and a pass transistor coupled between the latch node and the data line, *Schuster*, in the same field of endeavor as *Min* and *Seo*, discloses those features. *Schuster* discloses "p-channel decoupling devices between the small capacitance nodes of the sense amplifier (SA and SAN) and the high capacitance I/O lines." (Ex. 1007, 706, FIG. 5.)

A POSITA would have understood that each decoupling device is a PMOS transistor and in particular is a "pass transistor coupled between [a] latch node and [a] data line." (Ex. 1002, ¶189.) Each of *Schuster*'s nodes SA and SAN of the sense amplifier is a latch node and holds a signal generated by the sense amplifier. (*Id*.) Each decoupling device is a transistor that operates as a switch to pass logic levels between a latch node of sense amplifier SA and an I/O line ("data line"), and thus would have been understood by a POSITA to be a "pass transistor." (*Id.*; *see also* Ex. 1001, 1:45-46.)

It would have been obvious to a POSITA to modify *Min*'s circuit in the combined *Min-Seo* system to include a data line and a pass transistor coupled between *Min-Seo*'s latch node and the data line, as taught by *Schuster*. For example, a POSITA would have understood such a modification would have enabled *Min*'s techniques for driving one or more sense amplifiers to be implemented in a practical application involving a data line, as suggested by *Min* in view of *Seo*. (Ex. 1005, 1:4-9; Ex. 1002, ¶190.) This modification would have been a mere combination of known prior art elements (*Min-Seo*'s sense amplifier and *Schuster*'s I/O line and decoupling device) according to known methods (*e.g.*, coupling the components in the way disclosed at FIG. 5 of *Schuster*), to yield predictable results (*e.g.*, controllable access between the data line and the latch node, by way of the pass transistor, in the same manner as disclosed by *Schuster*).

KSR, 550 U.S. at 416. (Ex. 1002, ¶190.)

D. Ground 4: *Min* and *Tobita* Render Obvious Claims 16 and 17

1. Claim 16

> a) The method of claim 14 wherein before coupling the signal to be sensed to a latch node the method further comprises precharging the latch node to a selected intermediate voltage between a logic high and a logic low.

Min in view of *Tobita* discloses this feature. (Ex. 1002, ¶¶193-195.) As discussed above, the sense amplifiers SA_1-SA_n amplify the voltage signal from the memory cells received on the bit lines. (*Supra* Section IX.A.1(d).) *Min* does not explicitly disclose all the features of claim 16. However, it would have been obvious to implement such features in light of *Tobita*. (Ex. 1002, ¶¶193-195.)

Tobita discloses features for a DRAM device that includes an array of memory cells connected to word lines and bit lines. (Ex. 1009, FIGS. 1-4, 1:20-22, 2:5-11, 9:6-10:2, 10:10-30.) *Tobita* discloses precharging the bit lines that connect to a sense amplifier latch node to a predetermined precharge potential Vcc/2 prior to connecting the memory cell to a bit line. (*Id*., 4:21-60, FIGS. 3, 4; Ex. 1002, ¶194.) Precharging the bit line to Vcc/2 as described by *Tobita* is precharging a latch node to a selected intermediate voltage between a logic high and a logic low, because the bit line that is connected to the latch node is precharged to a selected value (*i.e.*, VCC/2), which a POSITA would have understood is between a logic high and a logic low level. (Ex. 1002, ¶194.) *Tobita* further discloses this

precharging occurs prior to the bit line voltage changing as a result of the memory cell voltage. (Ex. 1009, 4:21-60, FIGS. 3, 4.)

A POSITA would have found it obvious to modify the *Min*'s device to precharge a latch node like that discussed above in *Tobita* to allow adequate sensing of the data in the memory cell of *Min*'s memory device. (Ex. 1002, ¶195.) A POSITA would have been motivated to combine the teachings of *Min* and *Tobita* because the modification would have been the application of a known technique (as described in *Tobita* and further acknowledged by the '302 patent (Ex. 1001, 1:11-25)) to improve similar devices (both *Tobita* and *Min* disclose sense amplifiers connected to bit lines) in the same way (by using *Tobita*'s precharging for *Min*'s bit lines) to yield predictable results (the precharging of *Min*'s bit lines), which was a common feature in such memory devices at the time of the alleged invention (*see Tobita* above and Ex. 1001, 1:22-25). (Ex. 1002, ¶195.) *KSR*, 550 U.S. at 416.

2. Claim 17

a) The method of claim 16 wherein the second rate is selected to rapidly provide low impedance paths to the external power supply after initial sensing.

Min and *Tobita* disclose or suggest this feature. (Ex. 1002, ¶¶196-197.) As discussed above, *Min* discloses that after the first current path through Q112 is activated and transistor Q110 begins to turn on, a second current path is activated

through thru Q115 such that two current paths to Vss ("external power supply") are concurrently active. (*Supra* Section IX.A.1(f).) As discussed above, the second current path draws current at a rate ("second rate") corresponding to I_{P2}. (*See id*.) A POSITA would have understood the paths (shown below) to be "low-impedance" paths. (Ex. 1002, ¶196.)

The low-impedance paths are provided after the voltage at node LA_P has begun to rise from Vss toward Vcc, because FIG. 9 shows that the rise in ϕ_{SP2} (which controls transistor Q115) from low to high voltage occurs after ϕLA_P has begun to rise. (Ex. 1005, FIG. 9; Ex. 1002, ¶197.) As such, a POSITA would have understood that *Min* discloses that the second rate is selected to rapidly provide low impedance paths to the external power supply "after initial sensing." (Ex. 1002, ¶197.)

E. Ground 5: *Min* and *Schuster* Render Obvious Claim 18

3. Claim 18

> a) The method of claim 14 further comprising while changing the magnitude of the control signal at a second rate coupling the sense amplifier latch node to a data line using a pass transistor.

Min and *Schuster* discloses or suggests this feature. (Ex. 1002, ¶¶199-200.) As discussed above for claim 6, it would have been obvious to a POSITA to modify the circuit of *Min* to include a data line and a pass transistor coupled between *Min*'s latch node and the data line, as in *Schuster*. (*See* discussion of *Min*

and *Schuster* combination in Section IX.C.) One skilled in the art would have recognized that in the combined FIG. 9 – FIG. 1B system of *Min* as modified with *Schuster*, the "control signal" is the gate voltage of driver transistors $Q1_1$-$Q1_n$. (*Supra* Section IX.A.1(b).)

Furthermore, as discussed above, the "control signal" is changed by a cumulative effect to two current paths (one through Q115 and another through Q112). (*See* discussion of *Min* in Sections IX.B.4(h), IX.B.4(i); Ex. 1002, ¶200.) Thus, one skilled in the art would have understood that in the combined *Min*-*Schuster* device, the magnitude of the "control signal" would have been changed at a second rate and the sense amplifier latch node is connected to a data line using a pass transistor. (Ex. 1002, ¶200.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-6, 10-12, and 14-18 of the '302 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: October 7, 2016 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,195,302 contains, as measured by the word-processing system used to prepare this paper, 13,939 words. This word count does not include the items excluded by 37 C.F.R. § 42.24(a).

Respectfully submitted,

Dated: October 7, 2016

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on October 7, 2016, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,195,302 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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