Paper No. ____
Filed: October 7, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC
Patent Owner

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U.S. Patent No. 6,195,302

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**PETITION FOR *INTER PARTES* REVIEW**
**OF U.S. PATENT NO. 6,195,302**

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## I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-6 and 10-12 ("the challenged claims") of U.S. Patent No. 6,195,302 ("the '302 patent") (Ex. 1001), which is currently assigned to ProMOS Technologies, Inc. ("Patent Owner") according to USPTO records. For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

## II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

**Real Parties-in-Interest**: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

**Related Matters**: Patent Owner has asserted the '302 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Petitioner is concurrently filing a petition challenging claims 1-6, 10-12 and 14-18 of the '302 patent. Petitioner respectfully requests that the Board institute each petition, as each presents distinct and non-redundant grounds. Patent Owner has also asserted U.S. Patent Nos. 6,849,897 ("the '897 patent"), 6,020,259 ("the '259 patent"), 6,699,789 ("the '789 patent"), 6,088,270 ("the '270 patent"), and 5,761,112 ("the '112 patent") in this action. Petitioner is also concurrently filing IPR petitions on the '897, '259, '789, '270, and '112 patents.

**Counsel and Service Information**: Lead counsel is Naveen Modi (Reg. No. 46,224), and backup counsel are (1) Joseph E. Palys (Reg. No. 46,508) and (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-Promos1-IPR@paulhastings.com. Petitioner consents to electronic service.

## III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

## IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the '302 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

## V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

### A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1-6 and 10-12 ("challenged claims") of the '302 patent, and cancellation of these claims as unpatentable. (Ex. 1002, ¶173.)

### B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following

grounds:

**Ground 1**: Claims 1-5 and 10-12 are unpatentable under pre-AIA 35 U.S.C. §103(a) in view of U.S. Patent No. 5,140,199 ("*Seo*") (Ex. 1004) and UK Patent GB2246005B ("*Min*") (Ex. 1005);

**Ground 2**: Claims 10-12 are unpatentable under pre-AIA 35 U.S.C. §102(b) based on *Seo*; and

**Ground 3**: Claim 6 is unpatentable under pre-AIA 35 U.S.C. § 103(a) in view of *Seo, Min,* and Schuster *et al.*, "A 15-ns CMOS 64K RAM," *IEEE J. of Solid-State Circuits*, Vol. SC-21, No. 5, Oct. 1986, pp.704-12 ("*Schuster*") (Ex. 1007).

The challenged claims are not entitled to a filing date earlier than February 5, 1999.[1] *Seo* was issued on August 18, 1992. *Min* was published on August 31, 1994. *Schuster* was published in October 1986. Therefore, *Seo*, *Min*, and *Schuster* are prior art to the '302 patent at least under pre-AIA 35 U.S.C. § 102(b).

*Schuster* was published in October 1986 in the IEEE Journal of Solid-State

[1] Petitioner takes no position on whether that the claims of the '302 patent are supported by the provisional application (U.S. 60/118,737 filed on February 5, 1999). Each of the prior art references that form the basis of the grounds asserted in this petition are prior art to the '302 patent regardless of whether the claims of the '302 patent are entitled to the February 5, 1999 provisional filing date.

Circuits, Volume SC-21, Issue No. 5. This can be seen, for example, at the top of each page of *Schuster*. (Ex. 1007, 704-712.) Given that it was published in a well-known journal in October 1986, over a decade before the filing date of the '302 patent (*id*.), *Schuster* qualifies as prior art under pre-AIA 35 U.S.C. § 102(b). In fact, *Schuster* was cited by other articles well-before the '302 patent was filed. (*See, e.g.*, Ex. 1011, 363 (reference 7); Ex. 1012, 1219 (reference 21).)

Among the references relied upon in this Petition, *Min*, and *Schuster* were never considered by the Patent Office during prosecution of the '302 patent. (*See* Ex. 1001, References Cited.) *Seo* is, however, listed on the face of the '302 patent and was submitted in an information disclosure statement during prosecution. But Petitioner presents *Seo* in a new light never considered by the Office. (*See infra* Section IX.) Moreover, Petitioner presents testimony from R. Jacob Baker, Ph.D., P.E., an expert in the field of the '302 patent, who confirms that the relevant teachings of *Seo* alone or in combination with the other cited references discloses or suggests what is recited by the challenged claims. (*See* Ex. 1002.) As such, consideration of *Seo* by the Patent Office during prosecution of the '302 patent should not preclude the Office from considering and adopting the grounds in this petition that involve this reference.

### C. Statement of Non-Redundancy

Petitioner is filing a second IPR petition against the '302 patent concurrent

with the filing of this petition. However, Petitioner's proposed grounds for institution in the two petitions are not redundant and the Board should institute review in both proceedings. The primary references applied in the two petitions disclose features of the challenged claims in different ways, and are based on different combinations of references. For example, the primary reference in this petition (*Seo*) does not explicitly disclose a circuit component that delays a signal, as required by claim elements 10(e) and 1(f). Instead, a secondary reference is relied upon to disclose that feature. In contrast, the primary reference at issue in the other petition discloses these claimed features. As such, Petitioner respectfully requests that the Board adopt all proposed Grounds in both of the petitions.

## VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '302 patent would have had at least a Bachelor's degree in electrical engineering, or equivalent thereof, and at least two to three years of experience in design of semiconductor memory circuits. (Ex. 1002, ¶19.)[2] More education can supplement practical experience and vice versa. (*Id*.)

[2] Petitioner submits the declaration of Dr. R. Jacob Baker (Ex. 1002), an expert in the field of the '302 patent. (Ex. 1002, ¶19.)

## VII. OVERVIEW OF THE TECHNOLOGY, '302 PATENT, AND PRIOR ART

### A. Technology Background

At the time of the alleged invention of the '302 patent, it was well known that integrated circuit memories could include memory cell arrays consisting of thousands of memory cells arranged in a matrix of rows (word lines) and columns (bit lines), with each memory cell located at or near the crossing of a bit line and word line. (Ex. 1002, ¶37-39, citing Ex. 1009.) To read and write to the memory cells of a DRAM, other circuitry was known to be provided. (*Id*.) For instance, the bit lines were often coupled into complementary bit line pairs, with each pair associated with a sense amplifier that amplifies the signal on the bit lines during a read operation and drives/controls the bit lines when data is being written into the memory cells. (*Id*.) Several different techniques had been disclosed in the prior art at the time of the alleged invention of the '302 patent for driving the sense amplifiers. (*Id*.) As discussed below, the '302 patent claims a known prior art technique that drives transistors (referred to in the '302 patent as sense amplifier driver transistors), which control activation of the sense amplifiers. (*Id*.; *see also id.* at ¶¶21-29.)

### B. The '302 Patent

The '302 patent issued from U.S. application no. 09/492,276 filed on January 27, 2000 (Ex. 1003 at 4-26) and is directed to a memory device with sense

amplifiers 101a-101c that are coupled to a high voltage line Vcc and ground via driver transistors 104 and 106, respectively. (*See id.* at ¶¶40-48.) Driver transistors 104, which are PMOS pull-up transistors, and driver transistors 106, which are NMOS pull-down transistors, are controlled by control signals LPB and LNB, respectively and are shown in FIG. 1 of the '302 patent:

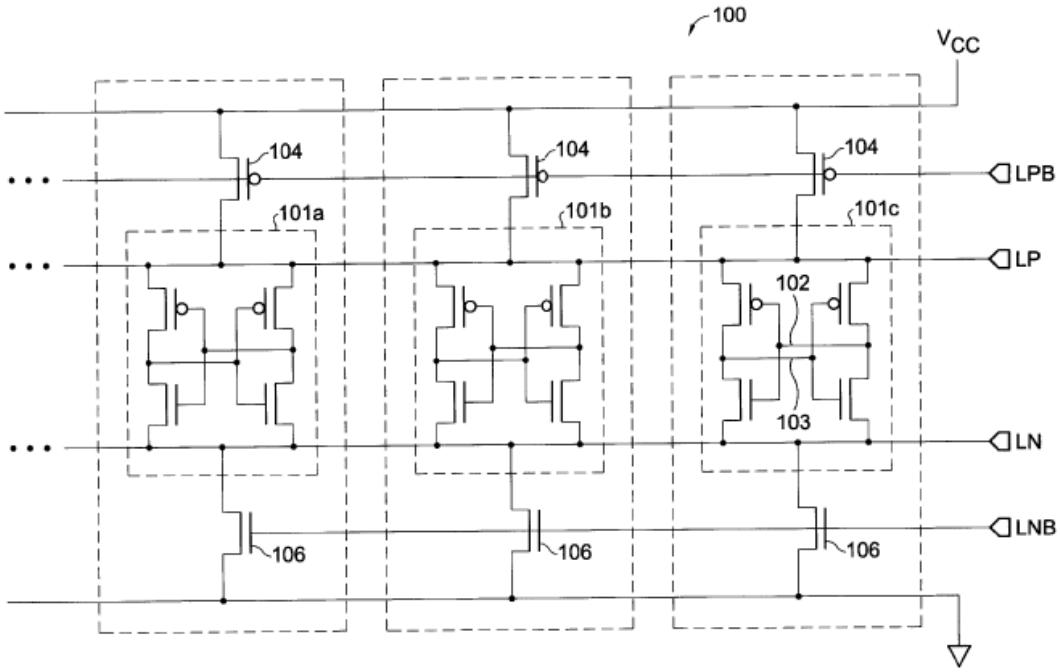



*FIG. 1*

(Ex. 1001, FIG. 1; *see also id.* at 4:40-5:4; Ex. 1002, ¶40.)

The '302 patent discloses functionality of sense amplifiers 101 with respect to FIG. 2 (shown below):

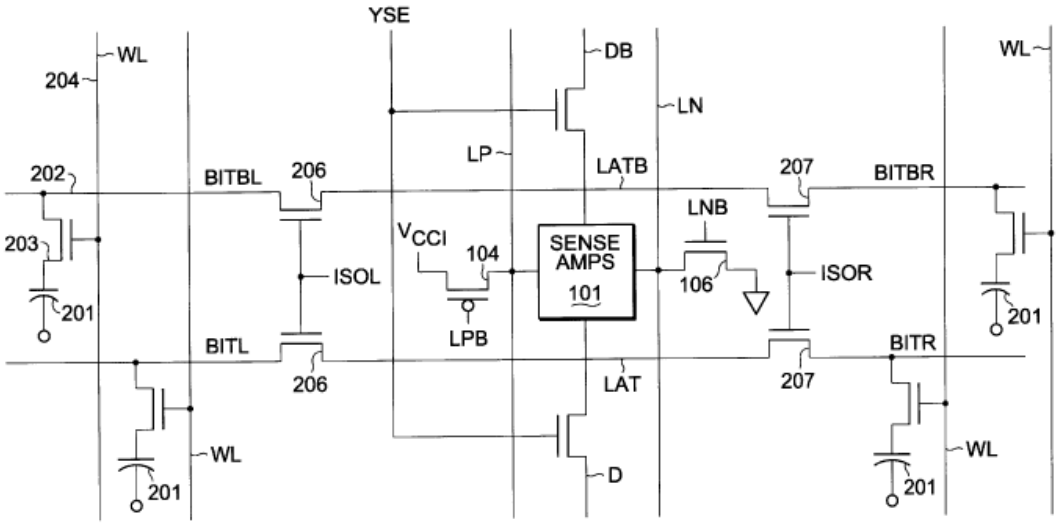



*FIG. 2*

(*Id.* at FIG. 2; *see also id.* at 5:5-55.)

The ’302 patent discloses that for a “sense amplifier 101 with associated circuitry typical in a DRAM application,” “[s]torage capacitors 201 are selectively coupled to bit lines 202 through access switches 203 in response to address signals supplied to word lines 204.” (Ex. 1001, 5:5-9.) Prior to a read operation, a pair of bit lines 202 are “equalized at some voltage between a logic high and a logic low signal,” and a word line (WL) signal is activated. (*Id.* at 5:18-21, 5:35-37.) After the WL signal is activated, “the LPB signal is driven to a logic low coupling VCCI to sense amp 101 through drive transistor 104 [and] [s]imilarly, the LNB signal is driven high to couple sense amp 101 to ground or $V_{SS}$ through drive transistor 106.” (*Id.* at 5:38-42.) The ’302 patent discloses that ““[p]referably, LNB and LPB are

generated by a circuit such as that shown in FIG. 3 that generates LNB and LBP both as dual slope signals." (*Id.* at 5:45-47.) The circuit for generating LNB and LBP is shown below:

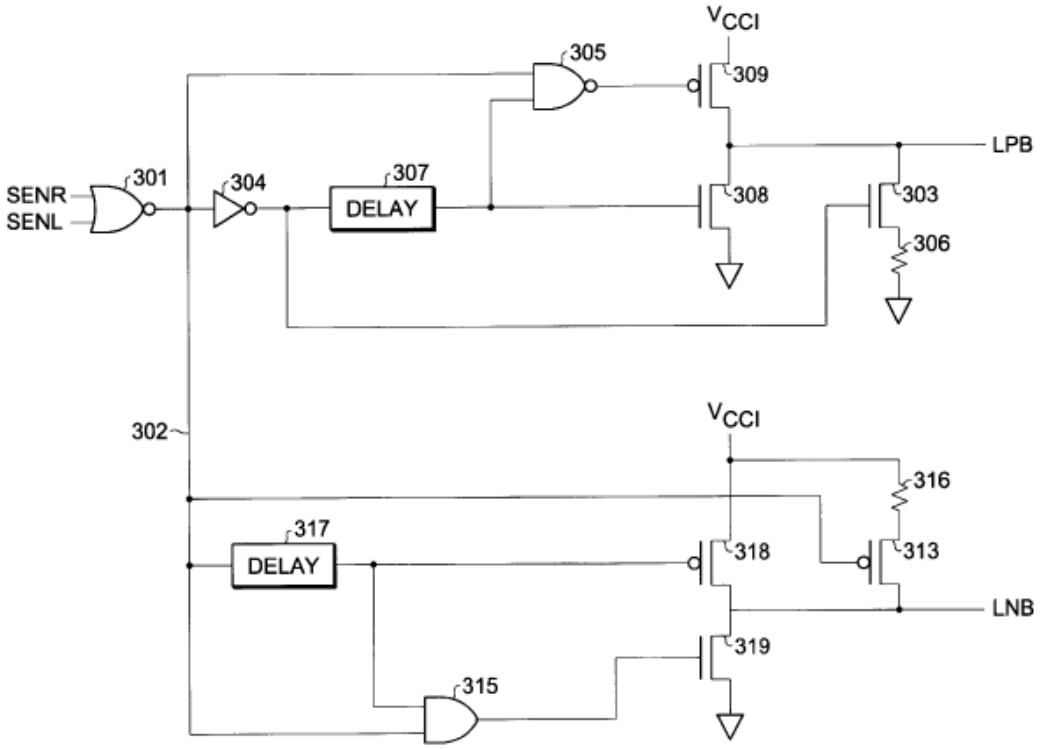



*FIG. 3*

(*Id.* at FIG. 3; Ex. 1002, ¶43.)

The '302 patent discloses that when sensing is to begin, "one of the input signals SENR or SENL will go to a logic high," which causes signal 302 to transition to a logic low because of NOR gate 301 and inverter 304. (*Id.* at FIG. 3, 5:66-6:6; Ex. 1002, ¶¶44-45.) Signal LPB is disclosed as being generated as follows:

> [S]hortly after either SENR or SENL goes high, transistor 303 is turned on pulling the LPB signal low through resist[o]r 306. . . . Resistor 316 controls the rate of change or dv/dt of LNB while resistor 306 controls the dv/dt of LPB. After a delay determined by delay element 307, transistor 308 will be turned on pulling LPB to ground with a much lower resistance. When transistor 308 is turned on, LPB will fall to the ground voltage with a high dv/dt.

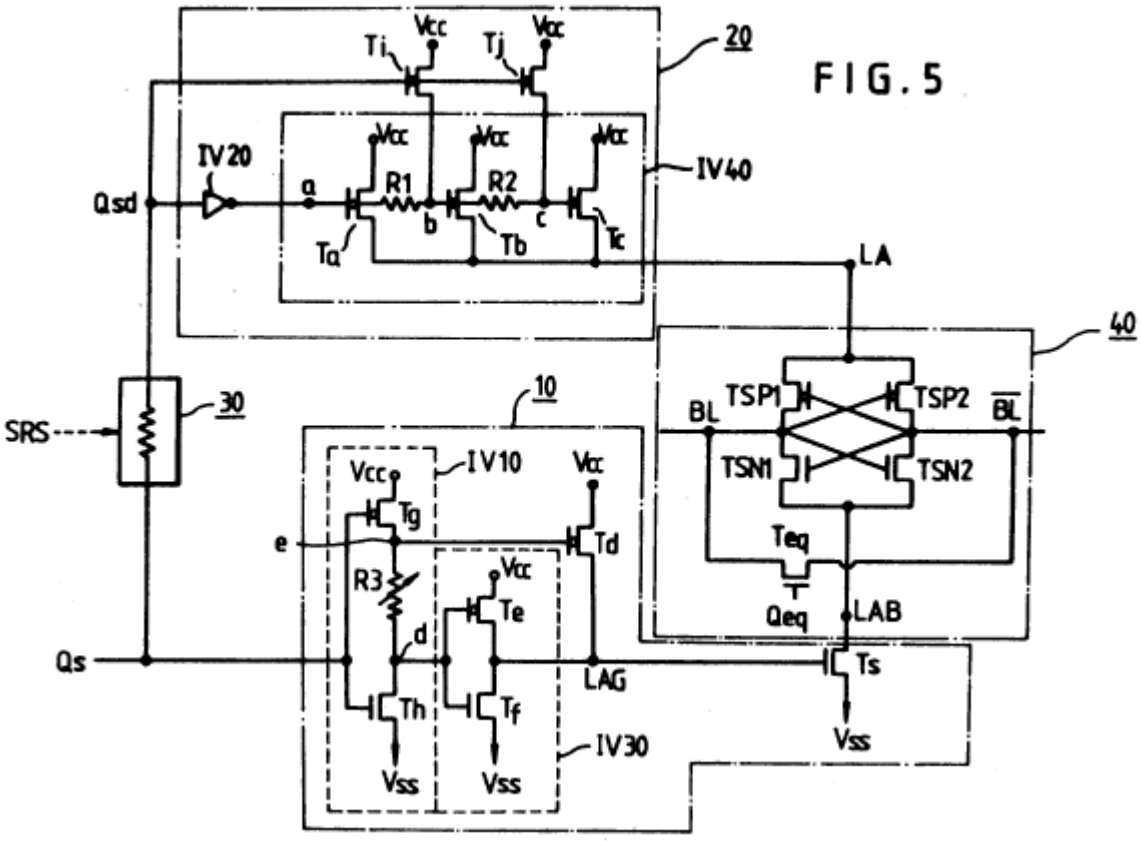
(*Id.* at 6:8-18; *see also id.* at FIG. 3.)

Signal LNB is generated in a similar manner, using circuit components shown in the lower part of FIG. 3. (*Id.* at 6:11-13, 6:18-21.) Signals LNB and LPB are generated as "dual slope signals." (*Id.* at 5:45-47.)

Thus, the '302 patent discloses that signal LPB, which controls drive transistor 104, is generated by turning on transistor 308 to pull down LPB, then after a delay, turning on transistor 303 so that LPB is pulled down two separate paths corresponding to transistors 308 and 303. (*Id.* at 6:33-36, FIG. 3; Ex. 1002, ¶48.) Signal LNB is generated in an analogous manner using staggered pull-up paths (*i.e.*, a first pull-up path corresponding to transistor 313 is enabled, and then after a delay, a second pull-up path corresponding to transistor 318 is enabled, while the first pull-up path is still enabled). (Ex. 1001, 6:33-36, FIG. 3; Ex. 1002, ¶48.)

### C. *Seo*

*Seo* discloses "sense amplifier circuitry for sensing data from memory cells." (Ex. 1004, 1:7-8; *see also* Ex. 1002, ¶¶53-58.) *Seo* shows a sense amplifier driver in FIG. 5:




(*Id.* at FIG. 5; Ex. 1002, ¶53; *see also id.* at ¶¶54-58.)

The circuit of FIG. 5 includes a sensing clock driver 10 that generates a signal at node LAG that drives the gate of NMOS transistor Ts to a high value, which turns on transistor Ts and thereby connects sense amplifier 40 to Vss. (Ex. 1004, FIG. 5, 5:55-58, 7:4-10; Ex. 1002, ¶¶54-58.)

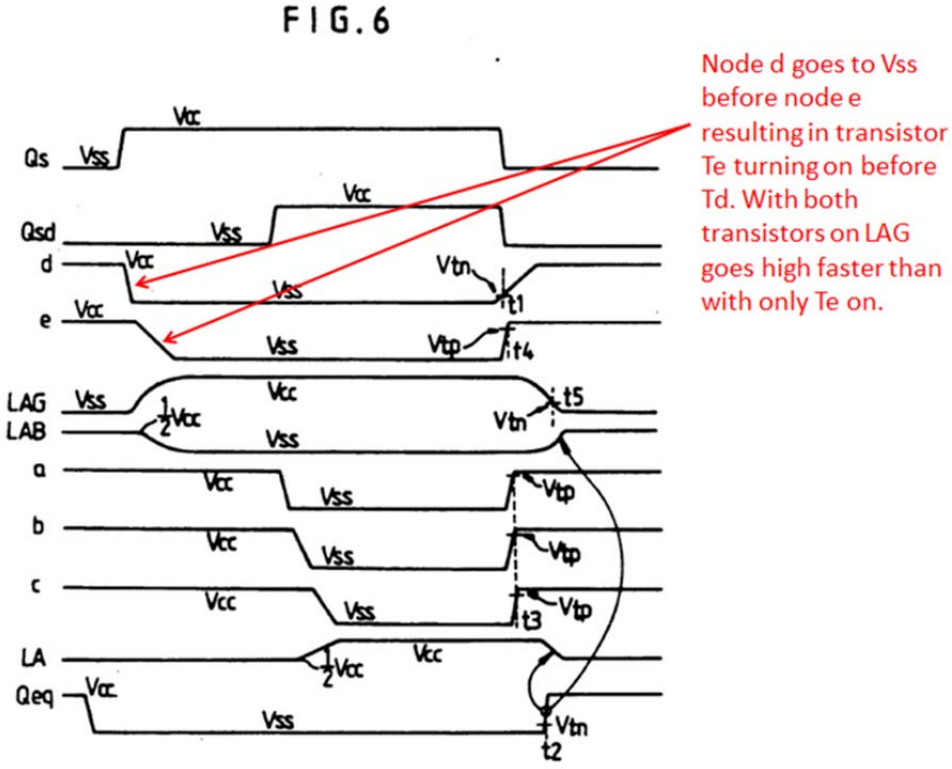
As discussed below, the LAG signal in *Seo* has a "multi-slope" characteristic like the LNB signal in the '302 patent. (Ex. 1002, ¶55; *see supra* Section VII.B (explaining the dual-slope nature of LNB).) *Seo* discloses that "[i]f a sensing enable state is established by the equalization control clock Qeq being at the Vss level and the sensing clock signal Qs being at the Vcc level, then node 'd' of sensing clock driver 10 [falls][3] to Vss level immediately owing to the function of n-channel MOS transistor Th of inverter IV10." (Ex. 1004, 6:56-61.) "Therefore, the p-channel MOS transistor Te of the inverter IV30 immediately turns on." (*Id.* at 6:61-63.) However, transistor Ts is not turned on completely "since transistor Te has small current driving capability" and is therefore unable to pull up signal LAG immediately to "high level, i.e., to the Vcc level" to completely turn on transistor Ts. (*Id*. at 6:63-66.)

"[T]he potential of node 'e' is lowered to Vss level after having been delayed for a certain period of time due to the function of resistance R3 of inverter IV10," and the PMOS transistor Td having a "large current driving capability turns on." (*Id.* at 6:67-7:4.) "Therefore, the potential of node LAG raises to Vcc level with a multi-slope characteristics, so that it can completely turn on the n-channel MOS sense transistor Ts." (*Id.* at 7:4-7.) "The resultant sensing signal LAB of the

[3] The omission of the word "falls" in this sentence of *Seo* is a drafting error but it is clear from FIG. 6 that node d "falls" to Vss. (Ex. 1002, ¶55, fn.4.)

Vss level . . . carries out the sensing operation for the data stored in the memory cell." (*Id.* at 7:7-10.)

In other words, *Seo* discloses that transistor Te turns on first to pull up the voltage at node LAG, and then, after a delay associated with "delaying resistance R3" (*id.* at 5:59-60), transistor Td turns on to provide a second pull-up path for pulling up node LAG. (Ex. 1002, ¶57.) FIG. 6 of *Seo* discloses that nodes d and e are both at low voltage after the falling transition at node e; hence, transistors Te and Td are both on, and provide separate pull-up paths for signal LAG, after transistor Td is turned on. (*Id.*; Ex. 1004, FIG. 6.)

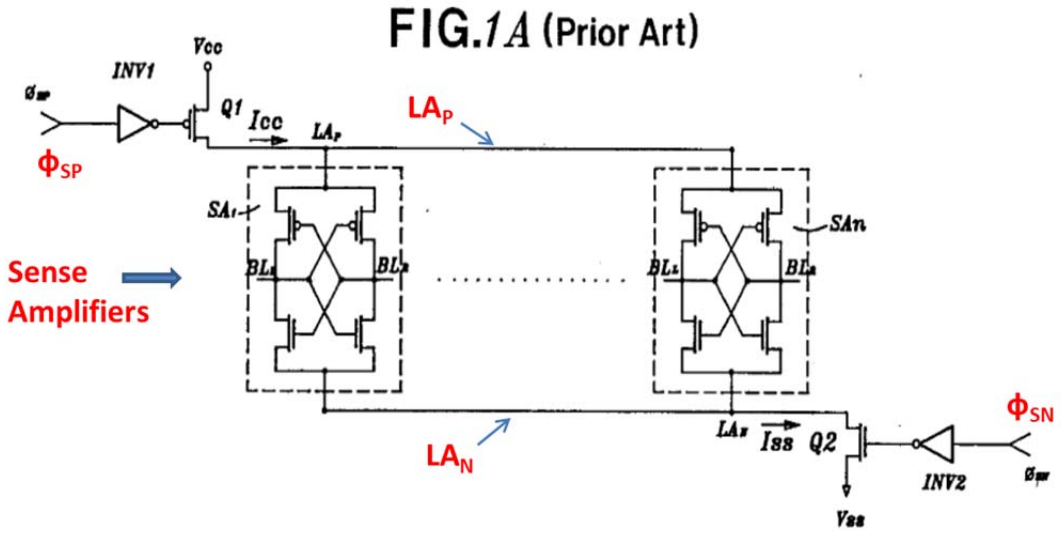



(Ex. 1002, ¶56, citing Ex. 1004, FIG. 6 (annotated).)

In summary, *Seo*'s technique of sequentially activating pull-up paths (*i.e.*, a first pull-up path through transistor Te and a second pull-up path through transistor Td) for generating a dual-slope control signal (LAG) is very similar to the sequential activation of pull-up paths disclosed in the '302 patent, as further explained below in section IX. (Ex. 1002, ¶58; *infra* section IX.)

### D. *Min*

*Min* describes a "sense amplifier driving circuit which is suitable for use in a high density semiconductor memory device." (Ex. 1005, 1:6-8; *see also* Ex. 1002, ¶¶59-70.) *Min* discloses at FIG. 1A a sense amplifier driving circuit that was conventional at the time of *Min*:

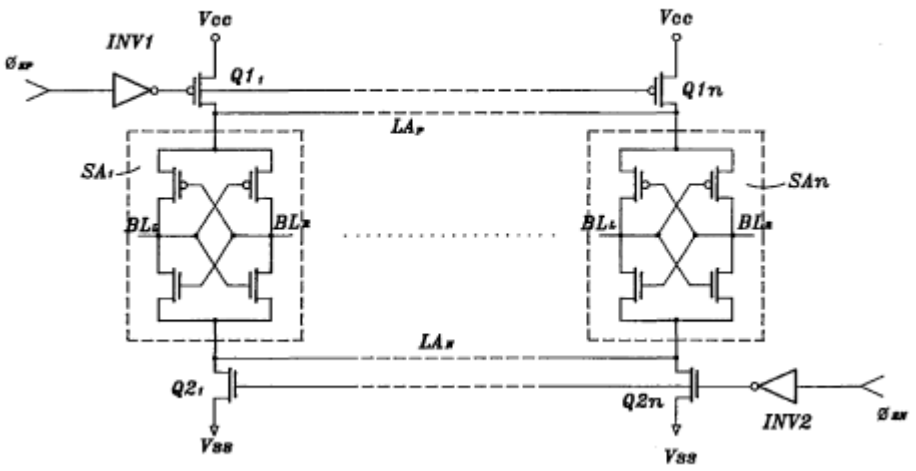



(Ex. 1005, FIG. 1A (annotated); Ex. 1002, ¶59.)

The sense amplifiers $SA_1$-$SA_n$ in *Min* are connected to one another at node $LA_P$ and at $LA_N$ and are connected to Vcc and Vss by driving transistors Q1 and Q2, respectively. (Ex. 1005, FIG. 1A.)

*Min* discloses a variation of the FIG. 1A sense amplifier driving circuit arrangement in FIG. 1B where now each sense amplifier is provided with its own respective driving transistor $Q1_i$ connected to $V_{CC}$ and $Q2_i$ connected to $V_{SS}$:

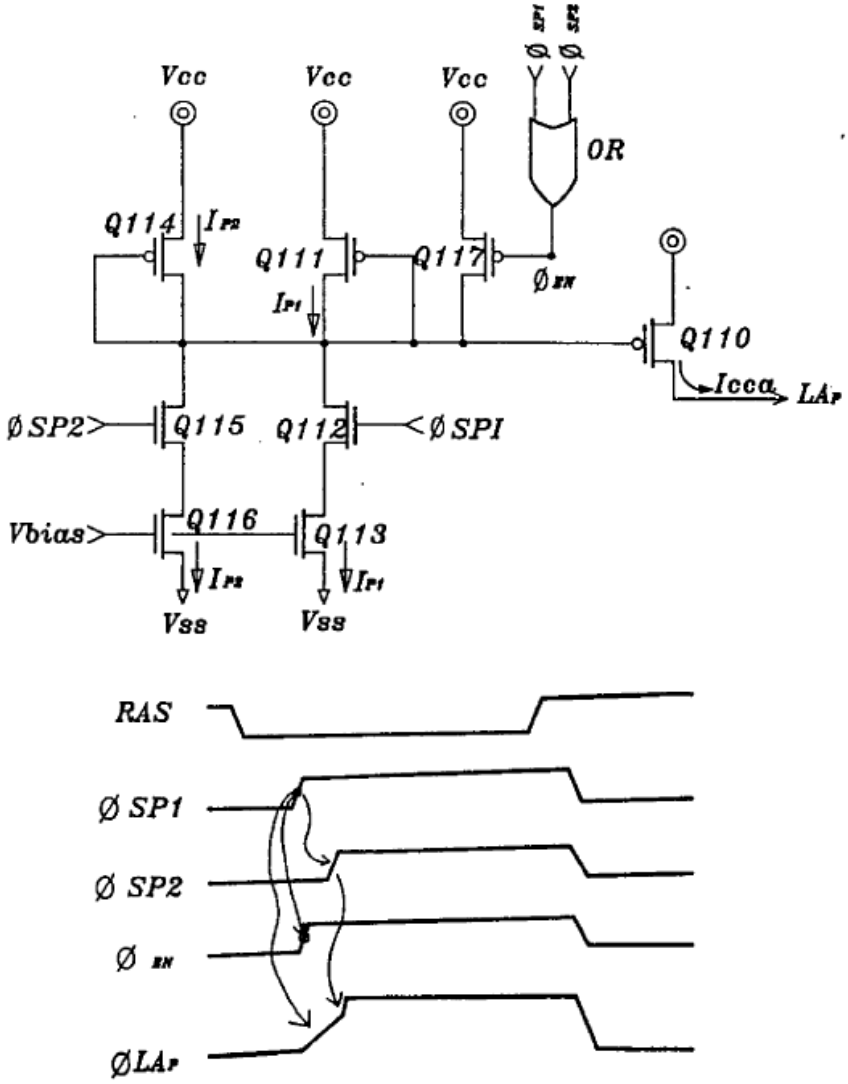
FIG. 1B (Prior Art)




(Ex. 1005, FIG. 1B; Ex. 1002, ¶63.)

*Min* discloses, in an embodiment corresponding to FIG. 9, an improved driver circuit for driving the conventional sense amplifiers shown in FIGS. 1A and 1B. The improved driving circuit and a corresponding timing diagram are shown in FIG. 9:

FIG.9




(Ex. 1005, FIG. 9.)

*Min* explains that a dual slope characteristic for signal $\phi LA_P$ (voltage at node $LA_P$) is achieved by a sequential pull-down approach by which a first pull-down path is activated to pull down the voltage at the gate of PMOS transistor Q110, and then after a delay a second pull-down path is activated. (Ex. 1005, 29:18-30:3; Ex. 1002, ¶66.) *Min* discloses that "signal $\phi_{SP1}$ is set to have a high level," which turns

on NMOS transistor Q112. (Ex. 1005, 29:21-25.) "After a certain period of time, the second active restore enable signal $\phi_{SP2}$ goes to a high level, and the transistor Q115 . . . is turned on so that the current Icca flowing through the driving transistor Q110 is increased." (Ex. 1005, 29:29-34.)

Turning on transistor Q112 activates a first pull-down path for pulling down the voltage at the gate of transistor Q110, and subsequently turning on transistor Q115 activates a second pull-down path for pulling down that same gate voltage. (Ex. 1005, FIG. 9; Ex. 1002, ¶67.)

Thus, *Min* discloses a technique of sequentially activating pull-down paths and sequentially activating pull-up paths that is similar to the sequential activation of pull-up paths and sequential activation of pull-down paths disclosed in the '302 patent, as further explained below in section IX. (Ex. 1002, ¶¶68-70; *infra* section IX.)

## VIII. CLAIM CONSTRUCTION

A claim in an unexpired patent that will not expire before a final written decision is issued in an IPR receives the "broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). The '302 patent has not expired and will not expire before a final written decision will be issued. Thus, for purposes of this proceeding, the claims of the '302 patent should be given their broadest reasonable construction.

Furthermore, to determine whether a claim should be interpreted under § 112, ¶6, "[t]he standard is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure. (*Williamson v. Citrix Online LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015).) "[T]he failure to use the word 'means' [in a claim] creates a rebuttable presumption . . . that § 112, para. 6 does not apply." (*Id.* at 1348.) "[T]he presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function." (*Id.* (internal quotes omitted).)

As set forth herein, Petitioner provides the broadest reasonable construction for certain claim terms below. Any term not interpreted below should be interpreted in accordance with its plain and ordinary meaning under the broadest reasonable interpretation standard.[4]

[4] Because of the different claim interpretation standards used in this proceeding and in district courts, any claim interpretations submitted or implied herein for the purpose of this proceeding are not binding upon Petitioners in any litigation related to the '302 patent. Specifically, any interpretation or construction of the claims presented herein, either implicitly or explicitly, should not be viewed as constituting, in whole or in part, Petitioner's interpretation of such claims in any

**A. "timer unit . . . generating a control signal"**

Claim 1 recites the term "timer unit . . . . . generating a control signal."[5] The term "timer unit" is a means-plus function term under 35 U.S.C. § 112, ¶6.

Claim 1 recites that "a timer unit having an output coupled to the control electrode and generating a control signal." This claim recites function ("generating a control signal") without reciting sufficient structure for performing that function. A timer unit as recited in claim 1 does not connote any structure. Indeed, the identified function for this term, "having an output coupled to the control electrode" only specifies where the output of the timer unit is coupled and does not specify structure for the timer unit itself. Like the term "module" in *Williamson*, the recitation of a timer "unit" in claim 1 does not provide a sufficiently definite

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underlying litigations involving the '302 patent. Moreover, Petitioner does not concede that the challenged claims are not indefinite, which is something that cannot be pursued in this proceeding under the Rules.

[5] The term "the timer unit output" in claim 12 does not have any antecedent basis, and thus claim 12 is indefinite. However, for purposes of this proceeding, Petitioner assumes that the term "timer unit output" in claim 12 means an output from a clock or timer, such as a "clock signal." Under that assumption, however, "the timer unit output" in claim 12 should not be construed in a manner similar to the recited "timer unit . . . generating a control signal" in claim 1 discussed above.

structure for performing the function of "generating a control signal." *Williamson*, 792 F.3d at 1350 ("the word 'module' does not provide any indication of structure because it sets forth the same black box recitation of structure for providing the same specified function as if the term 'means' had been used.").

Although claim 1 recites "a first component" and "a second component" that are both "within the timer unit," those "component[s]" are specified in the claim using purely functional language, *i.e.*, describing what they do. Therefore, those "component[s]" do not impart sufficient structure for performing the recited function of the "timer unit." Therefore, although "means" is not recited in this claim, the presumption that § 112, ¶6 does not apply is overcome in this instance, and "timer unit" is a means-plus-function term.

Construing a means-plus-function claim term requires that the function recited in the claim term be first identified; then, the written description of the specification must be consulted to identify the corresponding structure that performs the identified function and equivalents thereof. *See Williamson*, 792 F.3d 1339 at 1351; *see also Gracenote, Inc. v. Iceberg Indus., LLC*, IPR2013-00551, Paper No. 6 at 15 (Feb. 28, 2014).

The written description of the '302 patent discloses that the function of "generating a control signal" is performed by at least a pair of transistors and one or more circuit components that delay a signal. For example, the '302 patent

discloses that the pair of transistors 303, 308 and delay element 307 generate control signal LPB, and that the pair of transistors 313, 308 and delay unit 317 generate control signal LNB. (Ex. 1001, 5:57 (describing LPB and LNB as "control signals"), 6:7-21 (disclosing that transistor 303 is first turned on to pull signal LPB low, then after delay element 307 delays the signal at its input, transistor 308 is turned to pull down signal LPB; and providing similar disclosure regarding transistors 313, 308 and delay unit 317, but regarding pull up paths), FIG. 3.)

For purposes of this proceeding, resistors 306 and 316 should not be considered as part of the corresponding structure, because the specification of the '304 patent discloses that that "resistors 306 and 316 can be eliminated and rise time of the first and second stage controlled by relative transistor sizes." (*Id.* at 6:31-33.)

Therefore, for purposes of this proceeding, the corresponding structure for the identified function for this term is "at least a pair of transistors and one or more circuit components that delay a signal" and its equivalents.

### B. "first component . . . causing the control signal to change from a first logic level towards a second logic level at a first rate"

This term, which appears in claim 1, is a means-plus-function term under § 112, ¶6. The term "component" is a nonce word and does not connote any structure. Moreover, the identified function for this term "causing the control

signal to change from a first logic level towards a second logic level at a first rate" does not provide any description structure for the "component." Indeed, as discussed above regarding "timer unit," although the "first component" is recited as being "within the timer unit," the "first component" in claim 1 is specified using purely functional language. (*See supra* section VIII.A.) Therefore, claim 1 does not recite sufficiently definite structure for performing the above function. Accordingly, the claimed "first component" is a means-plus-function term.

Looking to the specification, the '302 patent discloses that transistor 303 causes control signal LPB to change from VCCI ("first logic level") towards ground ("second logic level") at an initial rate where the rate is the change in voltage (dv/dt) over time for LPB. (Ex. 1001, 6:8-13, 6:31-33, FIG. 3.) The '302 patent also discloses that transistor 313 causes control signal LNB to change from ground ("first logic level") towards VCCI ("second logic level") at an initial rate where the rate is the change in voltage (dv/dt) over time for LNB. (*Id.* at 6:11-13, 6:31-33, FIG. 3.) Accordingly, for both the LPB and LNB control signals, the corresponding structure is transistor 303 and transistor 313, respectively.

Therefore, for purposes of this proceeding, the corresponding structure for the identified function the claimed "first component" is "a first transistor" and its equivalents.

### C. "second component . . . causing the control signal to change to the second logic level at a second rate"

This term, which appears in claim 1, is a means-plus-function term under § 112, ¶6. As noted above, "component" does not connote any structure. Also, the identified function for this term, "causing the control signal to change to the second logic level at a second rate," does not provide any indication of the structure for the "second component." As discussed above regarding "timer unit," although the "second component" is recited as being "within the timer unit," the "second component" in claim 1 is specified using purely functional language. (*See supra* section VIII.A.) Therefore, the claimed "second component" is a means-plus-function term.

The '302 patent discloses that transistor 308, when turned on, causes control signal LPB to be pulled down toward ground ("change to the second logic level"), which causes LPB to "fall to the ground voltage with a high dv/dt." (Ex. 1001, 6:17-18; *see also id.* at FIG. 3.) The '302 patent also discloses that transistor 318, when turned on, causes control signal LNB to be pulled up to VCCI rapidly without the dv/dt limiting effect of resistor 316. (*Id.* at 6:18-21; *see also id.* at FIG. 3.) Accordingly, for both the LPB and LNB control signals, the corresponding structure is transistor 308 and transistor 318, respectively.

Therefore, for purposes of this proceeding, the corresponding structure for the identified function the claimed "second component" is "a second transistor" and its equivalents.

**D. "delay unit . . . generating a delayed sense control signal"**

This term, which appears in claim 10, is a means-plus-function term under § 112, ¶6. The term "delay unit" does not connote any structure and the identified function for this term, "generating a delayed sense control signal," provides no guidance as to the structure. The "delay unit" is specified as being "coupled to the sense control signal node," but that does not specify structure for the "delay unit" itself, and the "delay unit" is specified using purely functional language. Therefore, claim 10 does not recite sufficient structure for performing the above function. Accordingly, the term "delay unit" is a means-plus-function term.

The '302 patent discloses that delay element 307 performs the above function regarding generating a signal at the gate of transistor 308 ("delayed sense control signal") that controls signal LPB, and that delay unit 317 performs the above function regarding generating a signal at the gate of transistor 318 ("delayed sense control signal") that controls signal LNB. (*See* Ex. 1001, 6:15-21, FIG. 3.)

The '302 patent does not specify the circuit components that constitute delay elements 307 and 317. That is, the '302 patent does not specify delay 307 and delay 317 as anything more than a black box. To the extent the Board finds such

disclosure in the '302 patent as describing sufficient structure for the claimed "delay unit," and that claim 10 is somehow capable of being construed, Petitioner proposes that "delay unit" be construed as one or more circuit components that delay a signal. (*See* Ex. 1001, 6:15-21, FIG. 3.) Therefore, for purposes of this proceeding, the corresponding structure for the identified function for this term is "one or more circuit components that delay a signal" and its equivalents.

## IX. DETAILED EXPLANATION OF GROUNDS

### A. Ground 1: *Seo* in view of *Min* Renders Obvious Claims 10-12 and 1-5[6]

#### 1. Claim 10

a) "A sense amplifier clock driver circuit for an integrated circuit memory, the driver circuit providing at least one clock signal for controlling the operation of sense amplifier driver transistors and comprising:"[7]

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶77-118.)

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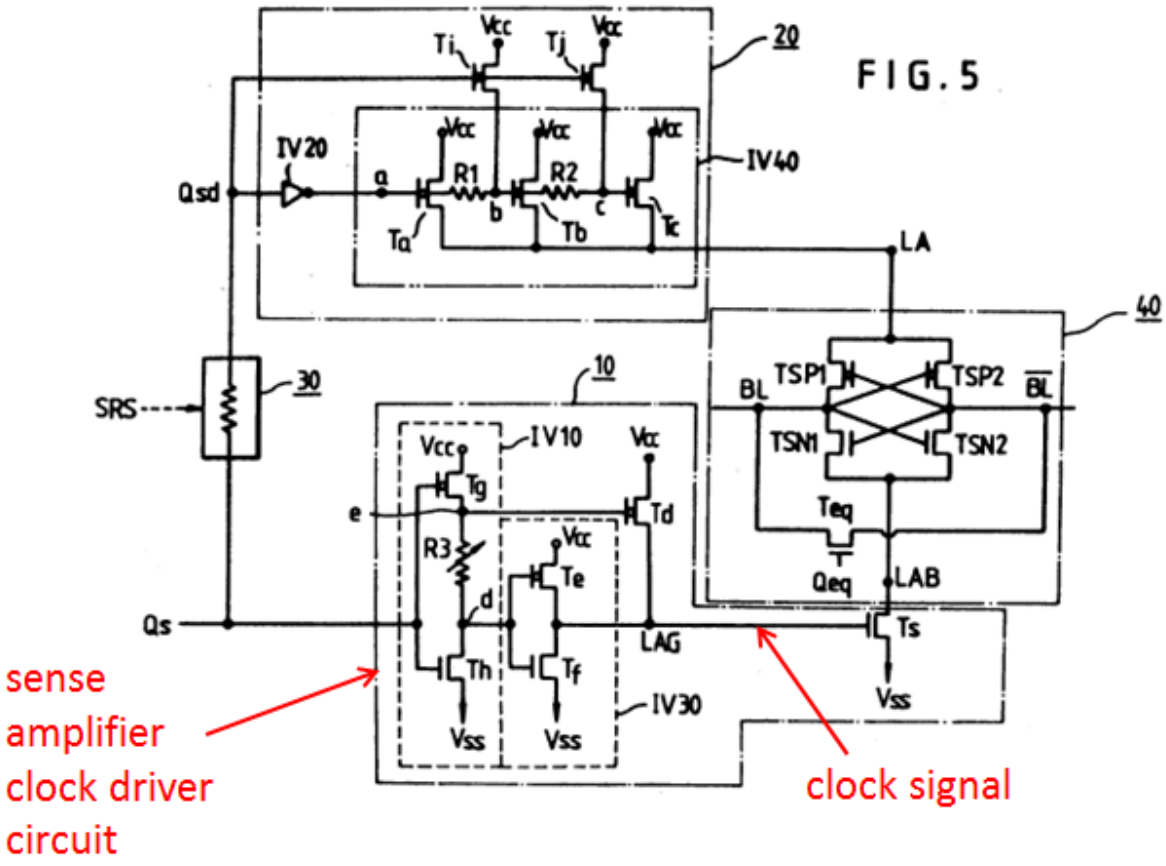
[6] Petitioner addresses claims 10-12 (Sections IX.A.1-A.3) before addressing claims 1-5 (Section IX.A.4-A.8) to provide context for the positions for the analysis of claims 1-3.

[7] The preamble of claim 10 is limiting because it is necessary to breathe life and meaning into claim 10. For instance, the term "clock signal" that is recited in the preamble is referenced back in the body of claim 10. (Ex. 1001, claim 10 "drive the clock signal".)

*Seo* discloses a sensing clock driver 10 ("sense amplifier clock driver circuit") for a CMOS DRAM cell ("integrated circuit memory"), the sensing clock driver 10 providing a clock signal at node LAG ("at least one clock signal") for controlling operation of an NMOS transistor Ts ("sense amplifier driver transistor"), as shown in FIG. 5:




(Ex. 1004, FIG. 5 (annotated); Ex. 1002, ¶78.)

As can be seen in FIG. 5, sensing clock driver 10 is connected to sense amplifier 40. (Ex. 1004, FIG. 5, 6:41-45). Sensing clock driver 10 generates a signal LAG that drives the gate terminal of transistor Ts. (Ex. 1004, FIG. 5.).

When signal LAG is high, transistor Ts pulls down the signal at node LAB to Vss to enable/activate sense amplifier 40. (Ex. 1004, FIG. 5, 7:4-10; Ex. 1002, ¶80.) As such, one of ordinary skill in the art would have understood that *Seo*'s sensing clock driver 10 shown in FIG. 5 is a "sense amplifier clock driver circuit." (Ex. 1002, ¶80.)

*Seo* discloses that the circuit of FIG. 5 is used for sensing data stored in a "CMOS DRAM cell." (Ex. 1004, 1:7-13.) One of ordinary skill in the art would have understood that CMOS is a technology for constructing integrated circuits and that a CMOS DRAM is implemented using an integrated circuit. (Ex. 1002, ¶81.) In other words, the CMOS DRAM cell in *Seo* is a type of integrated circuit memory. (*Id.*) As such, sensing clock driver 10 is "for an integrated circuit memory." (*Id.*)

*Seo* also discloses that sensing clock driver 10 "provid[es] at least one clock signal." With respect to signal LAG, *Seo* explains that it is generated by way of a sensing clock signal Qs. (Ex. 1004, FIG. 5, 6:56-7:7.) In particular, sensing clock signal Qs is inverted and then used to turn on PMOS pull-up transistors Te and Td in succession. (Ex. 1004, FIG. 5, 6:56-7:4.) This causes the voltage at node LAG to be pulled up to Vcc. (Ex. 1004, 7:4-7, FIG. 6.) As such, one of ordinary skill in the art would have understood that the signal at node LAG (the gate of transistor Ts) is "at least one clock signal." (Ex. 1002, ¶82.)

Moreover, *Seo* discloses that the LAG signal ("at least clock signal") is "for controlling the operation of sense amplifier driver transistor[]." For instance, as discussed above, the LAG signal controls the turning on/off of transistor Ts. (Ex. 1004, 7:4-7, FIGS. 5-6.) When transistor Ts is turned on by a sufficiently high voltage applied at its gate terminal (*e.g.*, by signal LAG), it pulls down the LAB node of sense amplifier 40 to Vss. (Ex. 1004, 7:4-10, FIGS. 5-6.; Ex. 1002, ¶83.) Accordingly, one of ordinary skill in the art would have understood that transistor Ts is a "sense amplifier driver transistor." (*Id*.) This is further confirmed by the '302 patent, which discloses that a transistor which connects the latch portion of the sense amplifier to Vss is a "low-side" driver transistor and the transistor which connects the latch portion of the sense amplifier to VDD is a "high-side" driver transistor. (Ex. 1001, 1:55-62.) Indeed, a comparison of FIG. 5 of *Seo* with FIG. 1 of the '302 patent shows that transistor Ts is a "sense amplifier driver transistor" just like transistor 106, which the '302 patent discloses as a driver transistor for the sense amplifier (*Id.* at 4:55-5:3):

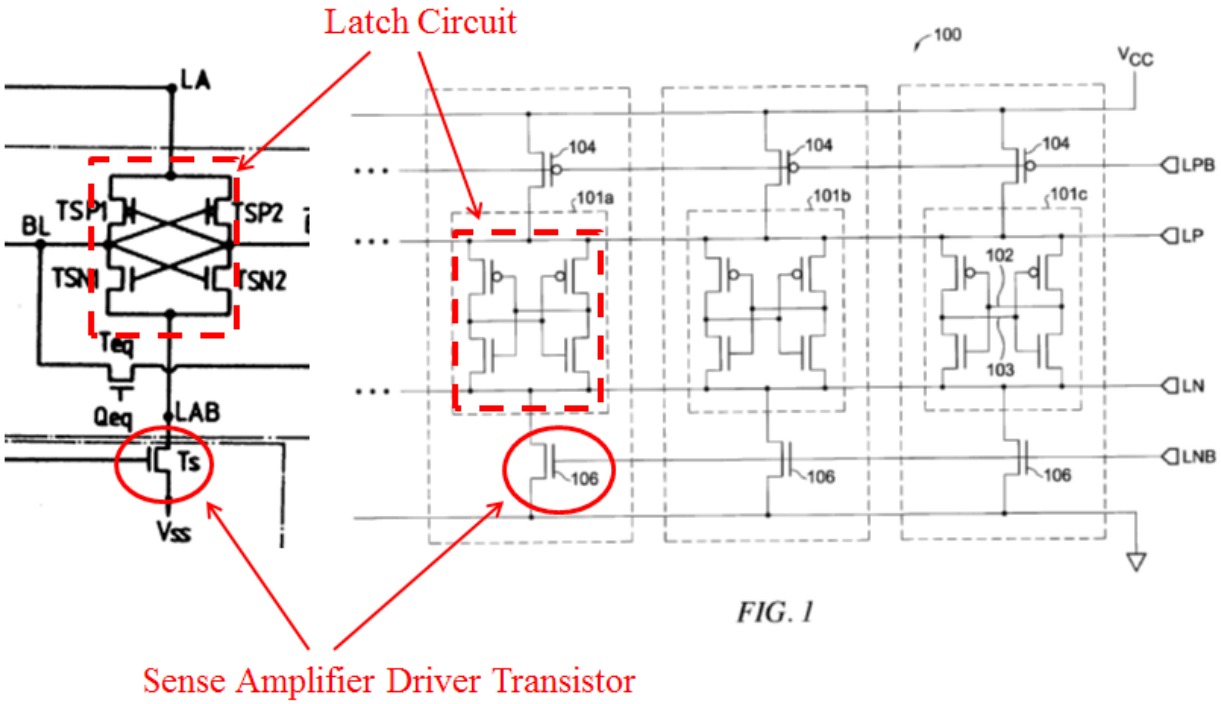



*FIG. 1*

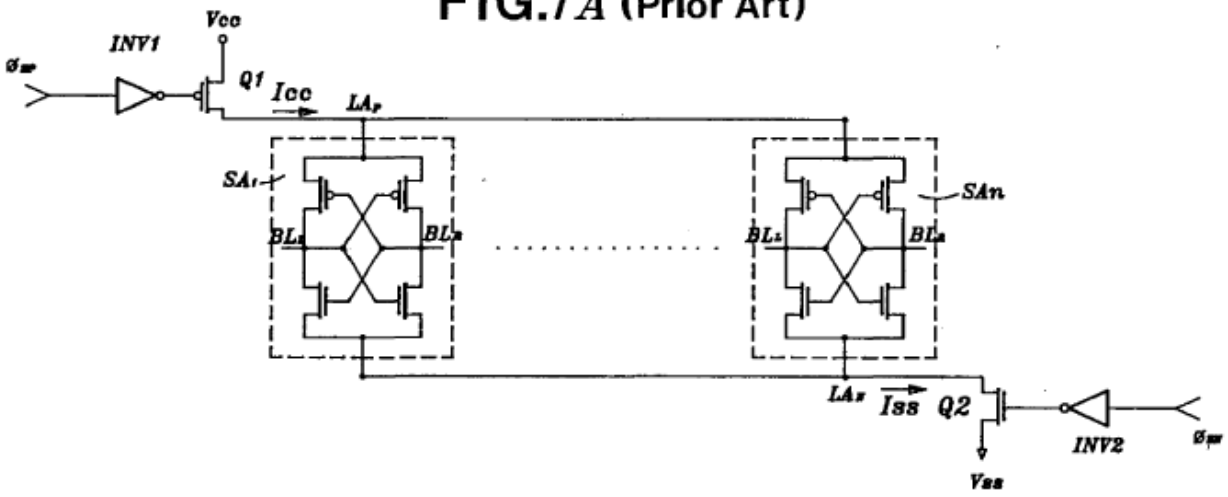
(Ex. 1004, FIG. 5 (excerpt) and Ex. 1001, FIG. 1, both annotated; Ex. 1002, ¶83.)

*Seo* discloses a single "sense amplifier driver transistor," *i.e.*, transistor Ts, and discloses a clock signal at node LAG for controlling operation of that transistor but *Seo* does not explicitly disclose multiple "sense amplifier driver transistors," as recited in the preamble of claim 10. That is, *Seo* does not explicitly disclose that the LAG signal controls the turning on/off of more than one sense amplifier driver transistor Ts. (Ex. 1002, ¶84.) *Min* discloses multiple sense amplifier driver transistors, and as discussed below, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '302 patent to implement *Seo*'s sense amplifier clock driver 1 to provide the LAG signal ("at least one clock signal") for controlling the operation of multiple sense amplifier driver transistors

as in *Min*.

*Min* is in the same field of endeavor as *Seo* (*i.e.*, sense amplifier driving circuitry for a memory device). (Ex. 1005, Title, Abstract.) One of ordinary skill would have looked to *Min* for guidance regarding possible implementations and uses of sense amplifier driver circuits. (Ex. 1002, ¶85.) *Min* discloses at FIG. 1A a sense amplifier driving circuit that was conventional at the time of *Min*:

FIG.*1A* (Prior Art)

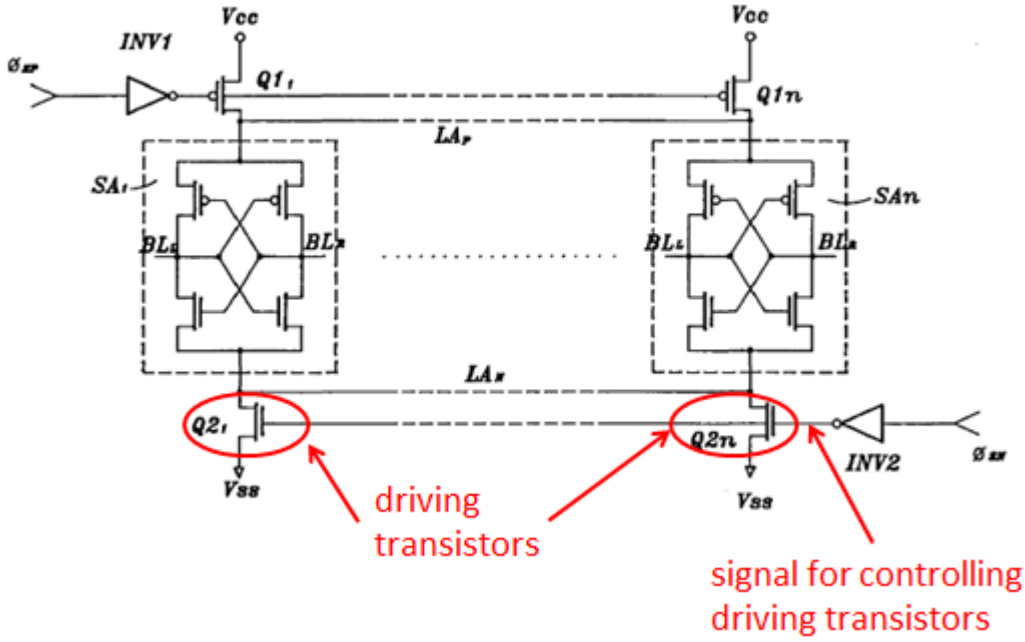



(Ex. 1005, FIG. 1A.) The circuit of FIG. 1A has multiple sense amplifiers, which one of ordinary skill would have understood to be a conventional feature of a memory system. (*Id.* at 2:5-6 ("a plurality of conventional miniaturized sense amplifiers $SA_1$ – $SA_N$"); Ex. 1002, ¶86.) For example, it was well known at the time of the alleged invention of the '302 patent to organize memory cells into an array of rows and columns, with each column being served by a respective sense amplifier. (Ex. 1002, ¶86; Ex. 1006, 2:24-30 (explaining that in a 16 megabit

DRAM, there are thousands of columns of bit line pairs with a sense amplifier provided for each bit line pair).)

*Min* discloses that "[i]n order to improve the stability of the sense amplifiers" the MOS driving transistors Q1 and Q2 in FIG. 1A can be "replaced by smaller MOS transistors." (Ex. 1005, 3:32-4:12.) This configuration with multiple driving transistors $Q2_1$-$Q2_n$ is shown in FIG. 1B:

FIG. 1B (Prior Art)



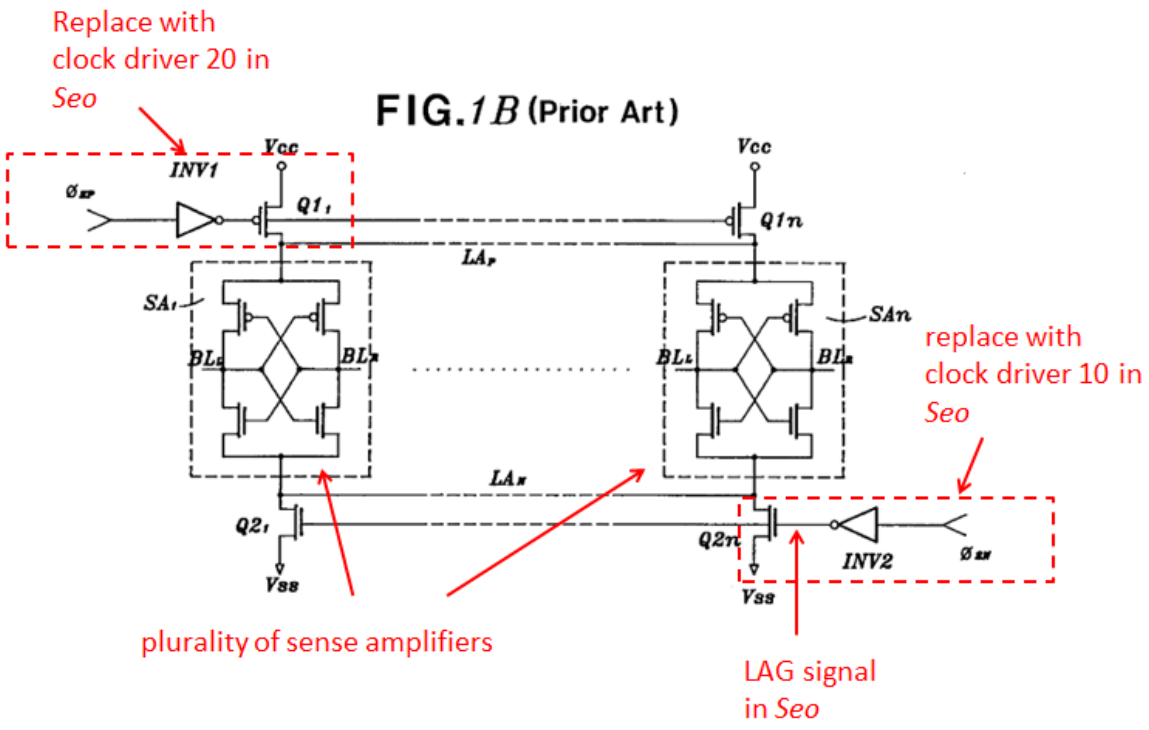

(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶87; *see also* Ex. 1004, 2:15-35.) Thus, *Min* discloses a benefit associated with using multiple smaller driving transistors $Q2_1$-$Q2_n$ instead of a single large driving transistor Q2. (Ex. 1002, ¶88; *compare* Ex. 1005, FIG. 1A, *with id.* at FIG. 1B.) *Min* therefore discloses a sense amplifier driving circuit that provides a control signal (signal at gate of transistors $Q2_1$-$Q2_n$

in FIG. 1B) for controlling the operation of "sense amplifier driver transistors," ($Q2_1$-$Q2_n$ in FIG. 1B) as recited in claim 1 of the'302 patent. (Ex. 1002, ¶88.)

In view of *Min*, one of ordinary skill in the art would have been motivated to combine the teachings of FIG. 5 in *Seo* with FIG. 1B in *Min* such that *Seo*'s sensing clock driver 10 output signal LAG is used to drive a plurality of sense amplifier drive transistors, each of which corresponds to a sense amplifier. (*Id*.) For example, one of ordinary skill would have known to make this modification by coupling node LAG to one or more additional NMOS transistors $Q2_1$-$Q2_n$ that (like *Seo*'s transistor Ts) have their respective source terminals coupled to Vss and that have their drain terminals coupled to respective sense amplifiers like in FIG. 1B of

*Min*. (Ex. 1002, ¶89.) The combination may be conceptually visualized as follows[8]:

[8] The following visual representation of the *Seo* and *Min* combination shows conceptually the result of combining the techniques for driving sense amplifiers as disclosed in *Seo* with *Min*'s well known configuration of a plurality of sense amplifiers each having their own driver transistor. (Ex. 1002, ¶89, fn.6.) It will be understood that not every feature necessary to build a fully functional system is disclosed by this visual representation. (*Id*.) Rather, it would have been within the skill of an ordinarily skilled artisan to combine the teachings of *Seo* and *Min* as shown in the above representation along with any necessary modifications to obtain a functioning system. (*Id*.)




(Ex. 1005, FIG. 1B (annotated to show an exemplary combination of *Min* and *Seo*); Ex. 1002, ¶89.)

One of ordinary skill in the art would have found such a modification obvious for the following reasons. For instance, this modification would have been a mere combination of known prior art elements (driving circuitry as in FIG. 5 of *Seo*, and multiple driving transistors and sense amplifiers as in FIG. 1B of *Min*), according to known methods (driving multiple transistors with a single node, as in FIG. 1B of *Min*) that yields predictable results (multiple driving transistors that are turned on by a sufficiently high gate voltage, and multiple sense amplifiers that are connected to Vss by such driving transistors). (Ex. 1002, ¶90.) *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

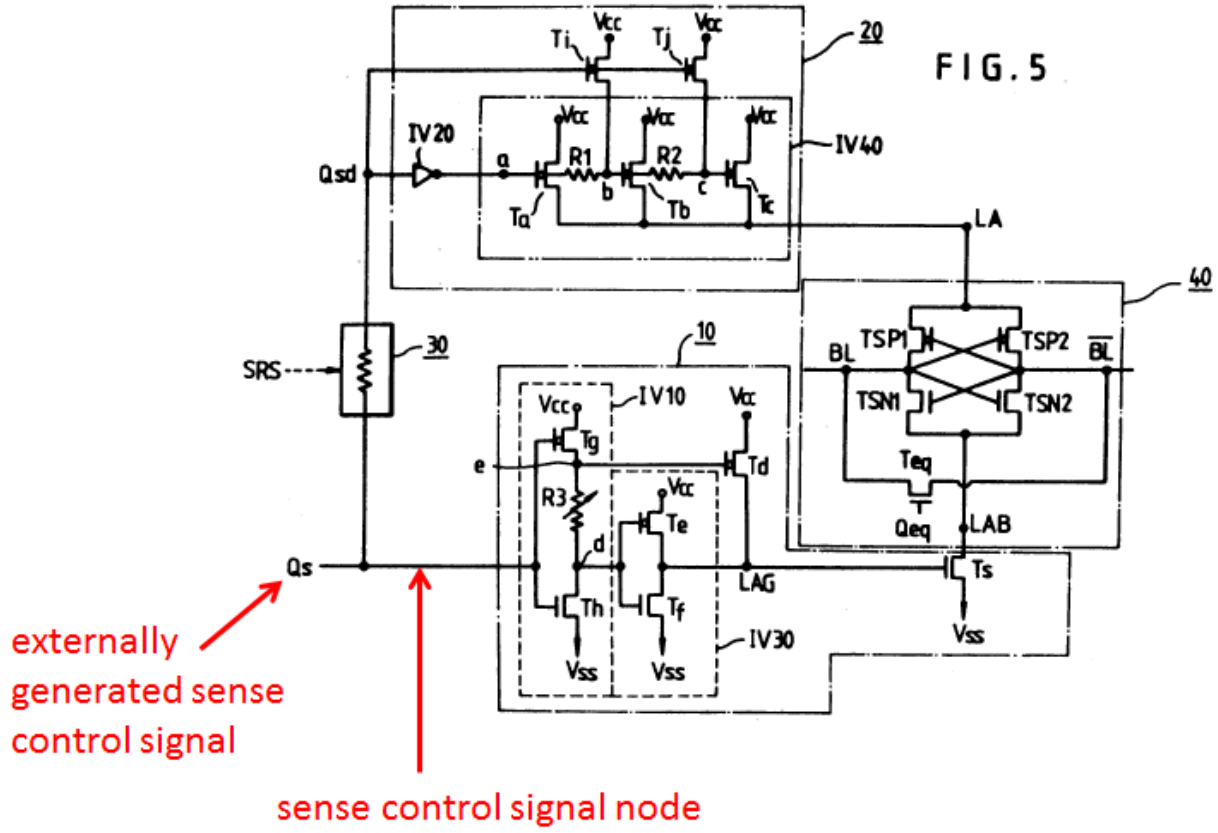
Moreover, one of ordinary skill would have recognized that the above modification would have improved the performance of *Seo*'s memory device by increasing the number of sense amplifiers as taught by *Min*, which would have enabled *Seo*'s technique of driving a sense amplifier to be implemented in a memory device having many columns of memory cells, as was common at the time of the alleged invention of the '302 patent. (Ex. 1002, ¶91.) Memory devices typically had thousands of columns of bit lines with several sense amplifiers, with the possibility of a sense amplifier being provided for each bit line pair. (*Id.*) Indeed, the inventor of the '302 patent (*i.e.*, Kim Hardee) acknowledged this fact in an earlier patent. (Ex. 1006, 1:32-39, 2:24-30.) Because such a modification would have been within the realm of knowledge and capability of an ordinary skilled artisan, and would have provided the benefit of increasing the utility of the sense amplifier arrangement in FIG. 5 of *Seo*, the above modification of *Seo* based on *Min* would have been obvious to one of ordinary skill. *See KSR*, 550 U.S. at 401 ("When a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, § 103 likely bars its patentability.").

> b) "a sense control signal node receiving an externally generated sense control signal indicating when sensing is to occur;"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶92-95.) For example, *Seo* discloses that a node at the input to inverter IV10 ("sense control signal node") receives sensing clock signal Qs ("externally generated sense control signal") indicating when sensing is to occur. (*Id.*)

Sensing clock signal Qs is asserted at a value of Vcc to initiate a sensing enable state. (Ex. 1004, 6:56-61.) Specifically, after clock signal Qs rises to Vcc, transistor Ts is turned on, as a result of which sensing signal LAB is pulled to Vss thereby enabling the sensing operation of the sense amplifier. (*Id.* at 6:56-7:10, FIG. 5; Ex. 1002, ¶93.) Therefore, sensing clock signal Qs is a "sense control signal." (Ex. 1002, ¶93.) Because sensing clock signal Qs is received at the input to inverter IV10, the node at the input of inverter IV10 is a "sense control signal node." (*Id.*)

Because setting signal Qs to Vcc initiates the pulling down of the LAB signal that ultimately lead to sensing data (Ex. 1004, 6:56-7:10), one of ordinary skill would have understood that signal Qs "indicat[es] when sensing is to occur." (Ex. 1002, ¶94.) Indeed, *Seo* discloses that by setting signal Qs to Vcc a "sensing enable state is established." (Ex. 1004, 6:56-59.)



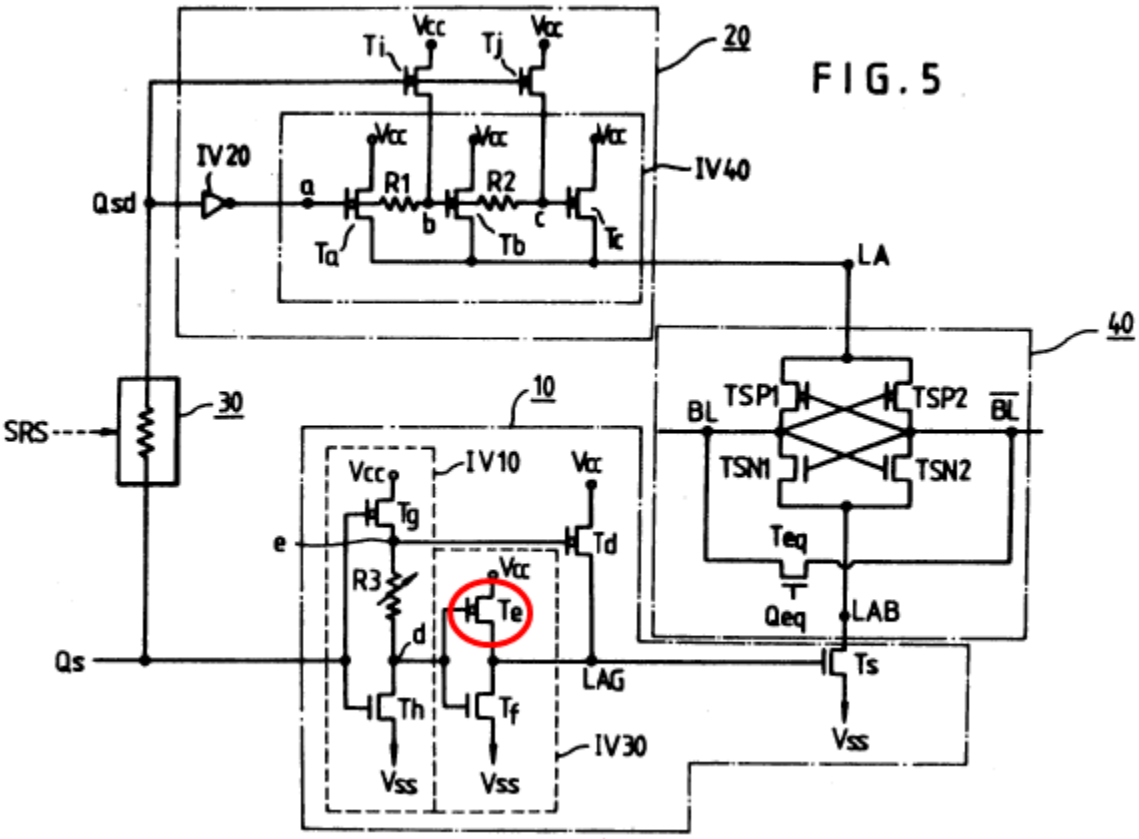

(*Id.* at FIG. 5 (annotated); Ex. 1002, ¶94.)

One of ordinary skill would have understood that sensing clock signal Qs is an "*externally generated* sense control signal" (emphasis added) because it is received by and generated externally relative to the sensing clock driver 10 shown in FIG. 5 of *Seo*. (Ex. 1002, ¶95.)

c) "a first impedance having a terminal coupled to a selected logic level signal;"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶96-101.) *Seo* discloses that the resistance ("first impedance") of transistor Te has a terminal

coupled to Vcc ("a selected logic level signal"). (*Id.*) Transistor Te is shown below:

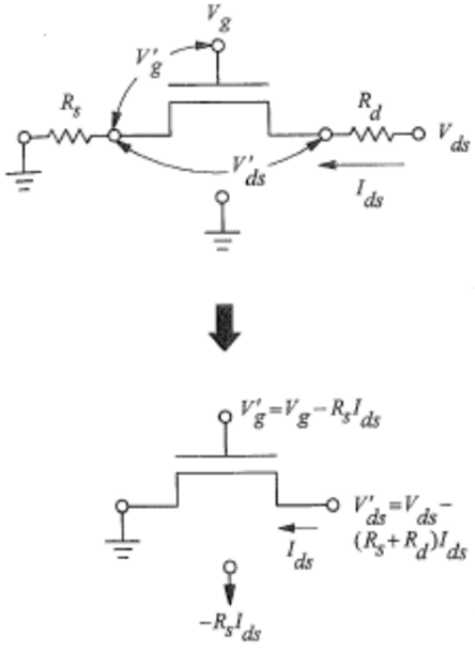



(*Id.* at FIG. 5 (annotated); Ex. 1002, ¶96.) Transistor Te has its source coupled to Vcc and its drain coupled to the LAG line. (Ex. 1002, ¶97.) Transistor Te also has an intrinsic impedance, a characteristic of all MOS transistors, that is coupled to Vcc. (*Id.*)

One of ordinary skill would have known that every MOSFET has associated parasitic resistance and a channel resistance. (*Id.* at ¶98.) This inherent

characteristic is described in Taur[9], Fundamentals of Modern VLSI Devices ("*Taur*"), which describes the total resistance associated with a MOSFET as the sum of three series resistances: a source resistance $R_{s,}$ a drain resistance $R_d$, and a channel resistance $R_{ch}$. (Ex. 1008, 205-06; Ex. 1002, ¶98.) The source resistance $R_s$ and a drain resistance $R_d$ are assumed to connect the MOSFET to the external terminals where a drain-source voltage $V_{ds}$ and gate voltage $V_g$ are applied. (Ex. 1008, 205-06; Ex. 1002, ¶98.) *Taur* shows these resistances schematically in an equivalent circuit as follows:

[9] While this ground relies on *Seo (*Ex. 1004) and *Min* (Ex. 1005), Petitioner discusses other references (e.g., *Taur*) to simply show the inherent characteristics of a MOSFET. *See, e.g.*, *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015) (explaining that prior art should be considered "even though it was not one of the three pieces of prior art presented as the basis for obviousness"); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) (relying on "critical background information that could easily explain why an ordinarily skilled artisan would have been motivated to combine or modify the cited references").




(Ex. 1008, 205, FIG. 4.20; Ex. 1002, ¶98.)

Because the source and drain regions are normally symmetrical, the sum of $R_s$ and $R_d$ may be denoted by $R_{sd}$. (Ex. 1008, 206; Ex. 1002, ¶99.) The total resistance for a MOSFET is captured by the following equation:

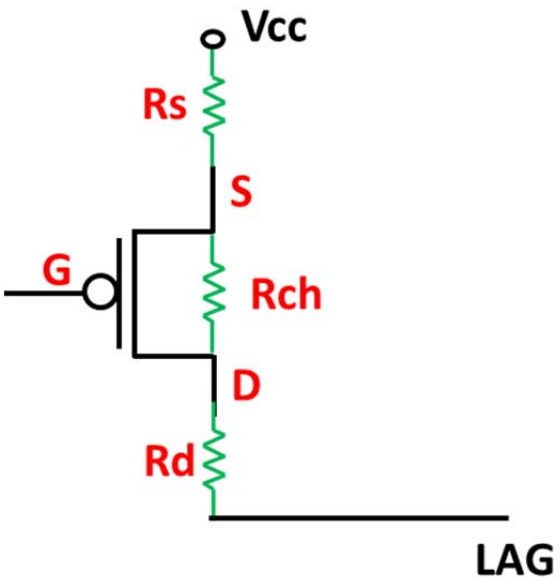
$$R_{tot} \equiv \frac{V_{ds}}{I_{ds}} = R_{sd} + R_{ch} = R_{sd} + \frac{L_{mask} - \Delta L}{\mu'_{eff} C_{ox} W (V_g - V_{on} - m V_{ds}/2)}. \qquad (4.72)$$

(Ex. 1008, 206; Ex. 1002, ¶99.)

Thus, one of ordinary skill would have recognized that the total device resistance of transistor Te is the sum of a parasitic impedance[10] $R_{sd}$ across the

[10] The '302 patent confirms this inherent characteristic of a MOSFET. (*See* Ex. 1001 patent at 6:26-30; Ex. 1002, ¶100, fn.7.)

source and drain terminals of transistor Te and a channel resistance $R_{ch}$. (*Id.*) Based on the transistor model described in *Taur*, transistor Te may be represented as below:

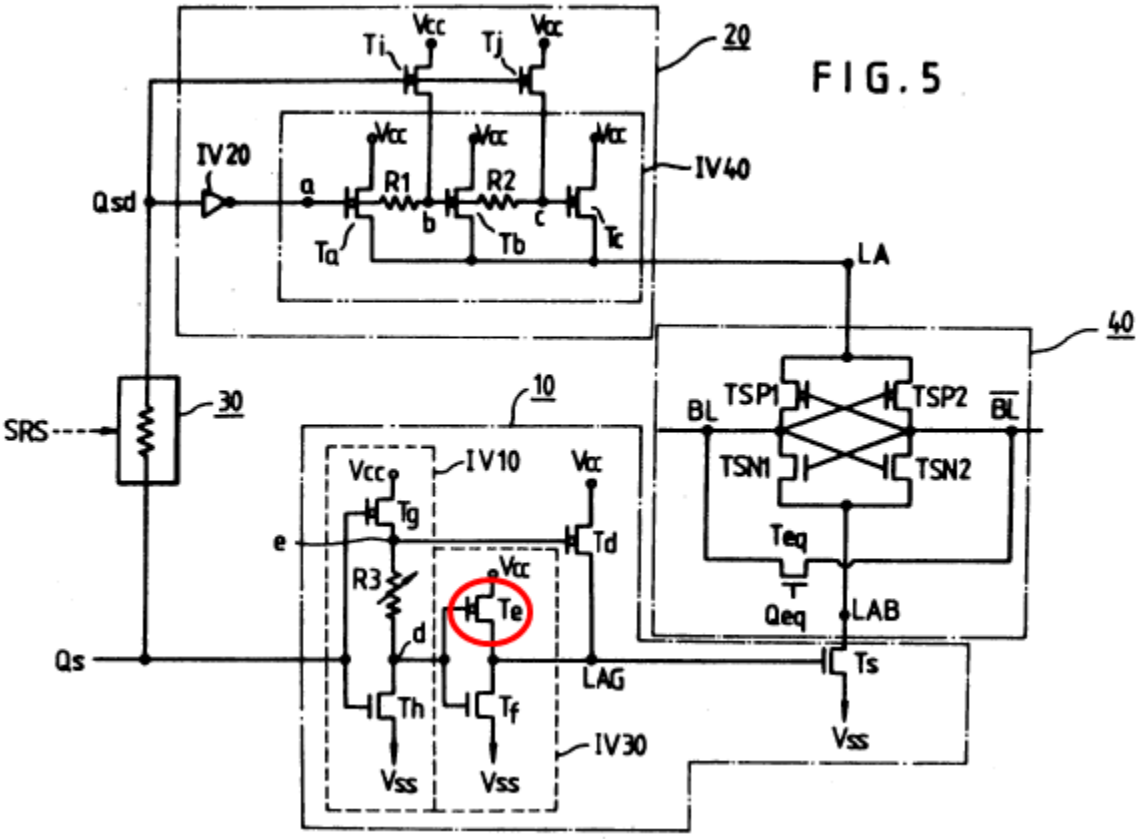



(Ex. 1002, ¶100; Ex. 1004, FIG. 5 (representation of transistor Te).)

Therefore, resistance $R_{tot}$ of transistor Te is a "first impedance" as recited in claim element 10(c), and one "terminal" of this impedance (*i.e.*, the node at the top Rs) is coupled to Vcc, which such a person would have understood to be "a selected logic level signal." (Ex. 1002, ¶101.) A resistance associated with transistor Te would have been understood to be an "impedance" in the context of the '302 patent. (*See* Ex. 1001, 6:10 ("resister [*sic*] 306"), 6:30 ("impedance provided by resistors 306 and 316").)

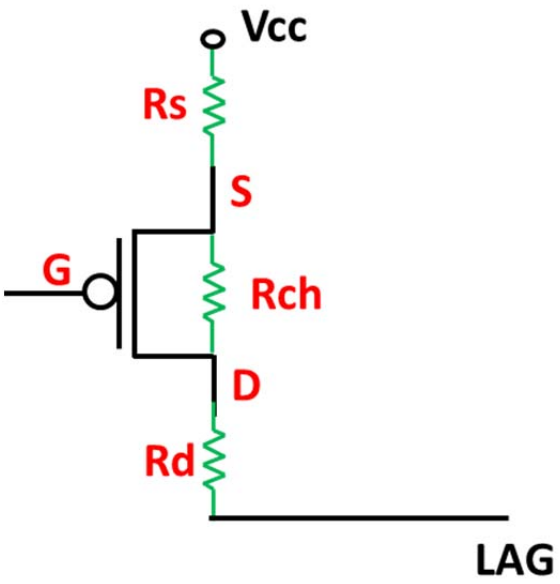
d) "a first switch having current carrying electrodes coupled to drive the clock signal to a selected logic level through the first impedance, the first switch controlled by the sense control signal;"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶102-105.) For example, *Seo* discloses that transistor Te ("a first switch") has a source and drain ("current carrying electrodes") coupled to drive the signal on line LAG ("clock signal") to Vcc ("selected logic level") when transistor Te is turned on by Qs ("sense control signal") being at Vcc. Transistor Te is shown in FIG. 5 of *Seo*:




(Ex. 1004, FIG. 5 (annotated); Ex. 1002, ¶102.)

The source and drain terminals ("current carrying electrodes") of transistor Te ("first switch") along with the various parasitic and channel resistances are shown in the illustration below:




(Ex. 1002, ¶103; Ex. 1004, FIG. 5 (representation of transistor Te).)

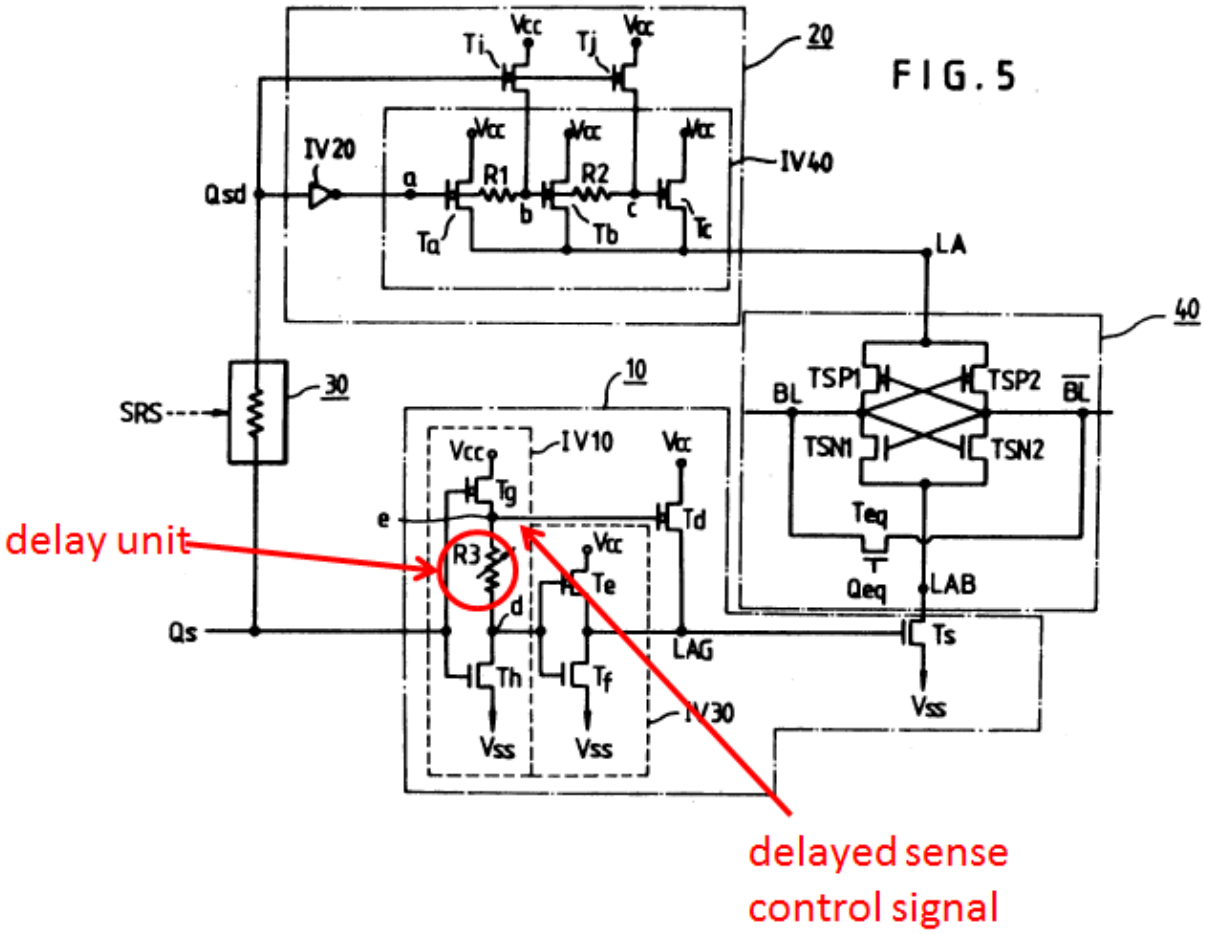
*Seo* discloses that the gate of transistor Ts receives the signal on line LAG ("the clock signal"). (Ex. 1004, FIG. 5; *see supra* Section IX.A.1(a).) *Seo* further discloses that transistor Te ("first switch") acts as a pull-up transistor that drives the gate of transistor Ts towards Vcc ("a selected logic level") through the resistance of transistor Te ("first impedance"). (*Id.* at 6:61-66; *see also id.* at FIGS. 1-2; Ex. 1002, ¶104.) One of ordinary skill in the art would have understood that the flow of current from Vcc to line LAG across the source and drain of transistor Te to pull up the voltage of LAG requires that the current flow through

the resistance ($R_{tot}$) of transistor Te (*see* annotated representation of Te above). (Ex. 1002, 104; *see supra* Section IX.A.1(c) (explaining the resistance associated with a transistor).) As can be readily seen from the above annotated representation of Te, current that flows from Vcc to the LAG node to pull up the voltage at LAG must flow through the resistance presented by transistor Te. (Ex. 1002, ¶105.)

Furthermore, transistor Te is controlled by signal Qs ("the sense control signal") because a high logic level (Vcc) for signal Qs results in a low logic level at the gate of transistor Te that turns on transistor Te. (*Id.* at ¶105; Ex. 1004, 6:56-63, FIGS. 1-2.)

e) "a delay unit coupled to the sense control signal node and generating a delayed sense control signal"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶106-109.) For example, *Seo* discloses a resistance R3 ("delay unit") that a skilled artisan would have understood is coupled, via node d, to the node at which Qs is received ("coupled to the sense control signal"), because when Qs is at Vcc (high), node d falls to Vss immediately. (Ex. 1004, FIG. 5, 6:56-61; Ex. 1002, ¶106.) Resistance R3 delays the signal d, which falls "to Vss level immediately owing to the function of . . . inverter IV10," to generate a delayed signal at node e ("generating a delayed sense control signal"). (*Id.* at 6:59-7:2.) Resistance R3 is shown below:




(Ex. 1004, FIG. 5 (annotated); Ex. 1002, ¶106.)

*Seo* discloses that R3 is a "delaying resistance" and that it causes delay between signals at nodes d and e "for a certain period of time." (Ex. 1004, 5:59-60, 6:67-7:2; *see also id*. at FIG. 6 (showing that R3 delays signal d to generate signal e).)

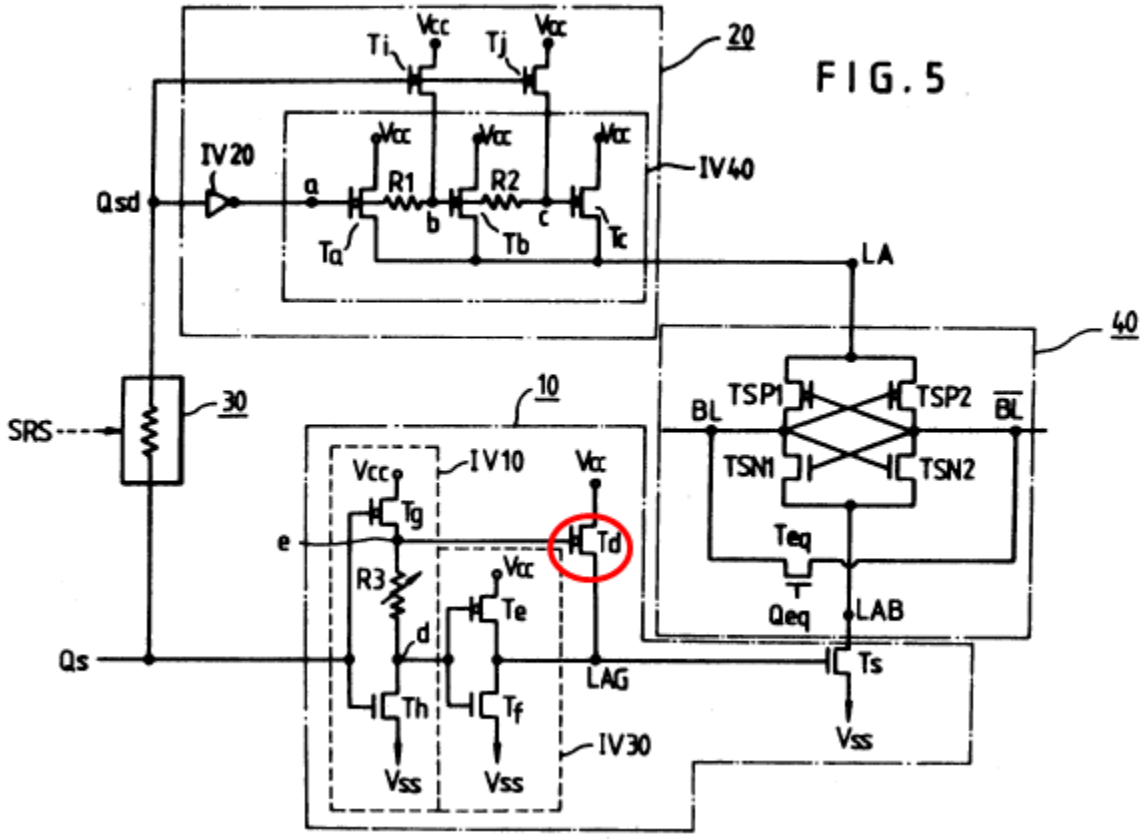
One of ordinary skill would have understood the generating of the signal at node e to be "generating a delayed sense control signal," as claimed, because as shown in FIG. 5 of *Seo*, the signal at node e is a delayed version of the signal at

node d (delayed by delaying resistance R3) and is used to control the voltage at the gate of sense transistor Ts and to control sensing performed by the sense amplifier 40. (Ex. 1004, 6:67-7:10 (disclosing "time delay caused by resistance R3" that controls voltage at node e), FIGS. 5 (showing node e), 6 (showing voltage at node e); Ex. 1002, ¶108.)

*Seo* also discloses the structure (resistor R3) corresponding to the function ("generating a delayed control signal") recited in this limitation. (*Id.* at ¶109; *supra* section VIII.D (structure corresponding to this function is "one or more circuit components that delay a signal"; Ex. 1004, FIG. 5 (showing R3 with circuit symbol for a resistor).) *Seo* discloses that "delaying resistance R3" delays the signal at node d to generate the signal at node e ("delayed sense control signal"). (Ex. 1004, 5:59-60, 6:67-7:2, FIGS. 5-6.) As such, resistor R3 is a circuit component that delays a signal.

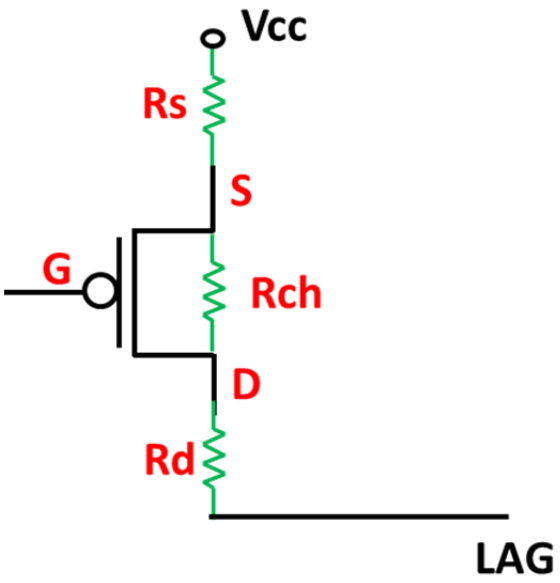
f) "a second impedance having a terminal coupled to the selected logic level signal; and"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶110-112.) *Seo* discloses that the resistance ("a second impedance") of transistor Td has a terminal coupled to Vcc ("having a terminal coupled to the selected logic level signal"). Transistor Td is shown below:




(*Id*. at FIG. 5 (annotated); Ex. 1002, ¶110.)

Like transistor Te (*see supra* Section IX.A.1(c)), transistor Td has its source coupled to Vcc ("selected logic level signal") and its drain coupled to the LAG line. (Ex. 1004, FIG. 5; Ex. 1002, ¶111.) Similar to transistor Te, transistor Td also has an intrinsic impedance. (Ex. 1002, ¶111.) Based on the transistor model described in *Taur* (*see supra* Section IX.A.1(c)), transistor Td may be represented as below:




(*Id.*; Ex. 1002, ¶111; Ex. 1004, FIG. 5 (representation of transistor Td)[11].)

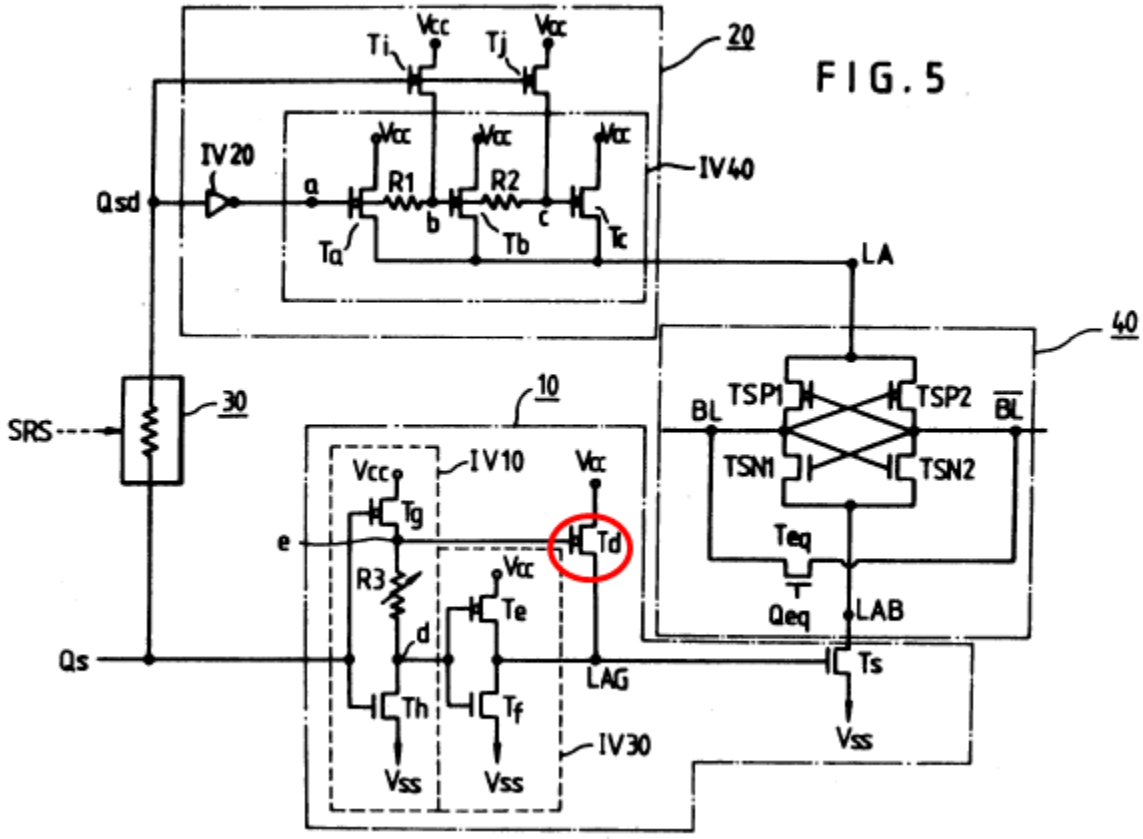
Therefore, resistance $R_{tot}$ (sum of series resistances $R_s$, $R_d$, and $R_{ch}$; *see supra* Section IX.A.1(c)) of transistor Td is a "second impedance" as recited in claim element 10(c), and one "terminal" of this impedance (*i.e.*, the node at the top

[11] While the representation of transistor Td and transistor Te (*see supra* Sections IX.A.1(c), (g)) appear similar because they are both connected in a similar manner between Vdd and LAG, one of ordinary skill in the art would have understood that the values of $R_s$, $R_{ch}$, and $R_d$ may be different for the two transistors. For instance, the $R_{tot}$ of transistor Td will be less than the $R_{tot}$ of transistor Te because *Seo* discloses that "transistor Te has small current driving capability" whereas "transistor Td [has] a large current driving capability." (Ex. 1002, ¶111, fn.8; Ex. 1004, 6:63-64, 7:2-3; *see infra* Section IX.A.2.)

of Rs) is coupled to Vcc ("the selected logic level signal".) (Ex. 1002, ¶112.) A resistance associated with transistor Td would be understood to be an "impedance" in the context of the '302 patent. (*See* Ex. 1001, 6:10 ("resister [*sic*] 306"), 6:30 ("impedance provided by resistors 306 and 316").)

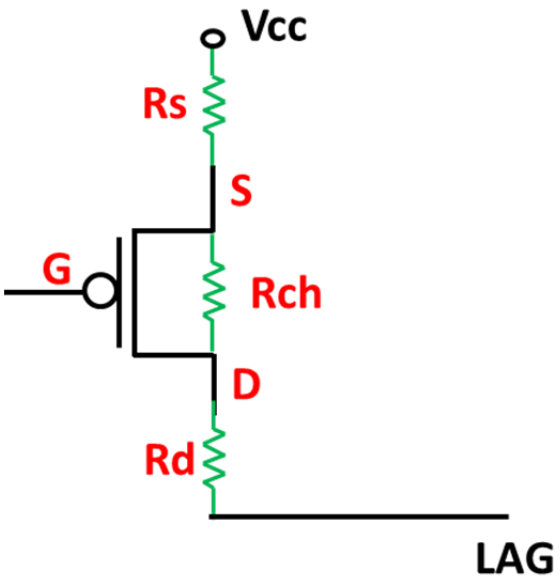
> g) "a second switch having current carrying electrodes coupled to drive the clock signal to the selected logic level through the second impedance,"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶113-115.) For example, *Seo* discloses that transistor Td ("a second switch") has a source and drain ("current carrying electrodes") coupled to drive the signal on line LAG ("clock signal") to Vcc ("selected logic level") when transistor Td is turned on by the delayed sense control signal at node e. Transistor Td is shown below:




(*Id*. at FIG. 5 (annotated); Ex. 1002, ¶113.)

Furthermore, as seen from the representation of Td in Section IX.A.1(f), Td has a source and drain ("current carrying electrodes") coupled to Vcc and LAG, respectively:




(Ex. 1002, ¶114; Ex. 1004, FIG. 5 (representation of transistor Td).)

*Seo* discloses that the gate of transistor Ts receives the signal on line LAG ("the clock signal"). (Ex. 1004, FIG. 5.) *Seo* further discloses that transistor Td acts as a pull-up transistor that drives the gate of transistor Ts to Vcc ("the selected logic level") through the resistance of transistor Td ("second impedance"). (*Id.* at 6:67-7:7; *see also id.* at FIG. 6; Ex. 1002, ¶115.) One of ordinary skill in the art would have understood that the flow of current from Vcc to line LAG across the source and drain of transistor Td to pull up the voltage of LAG requires that the current flow through the resistance ($R_{tot}$) of transistor Td (see annotated representation of Td above). (Ex. 1002, ¶115; *see supra* Section IX.A.1(f) (explaining the resistance associated with transistor Td).) That is, transistor Td

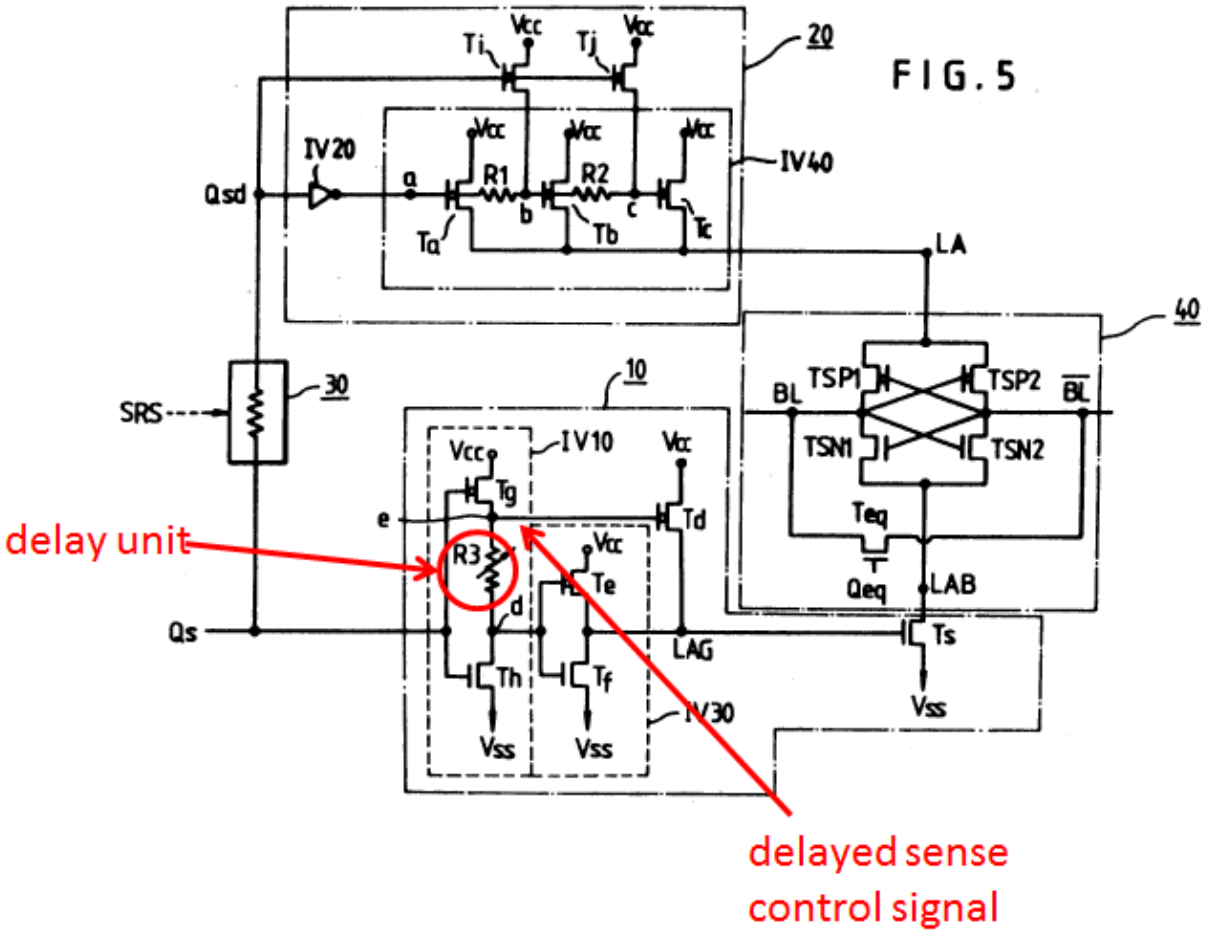
"drive[s] the clock signal to the selected logic level through the second impedance."

(Ex. 1002, ¶115.)

> h) "the second switch controlled by the delayed sense control signal such that the first switch and the second switch are concurrently activated after the delayed sense control signal is generated."

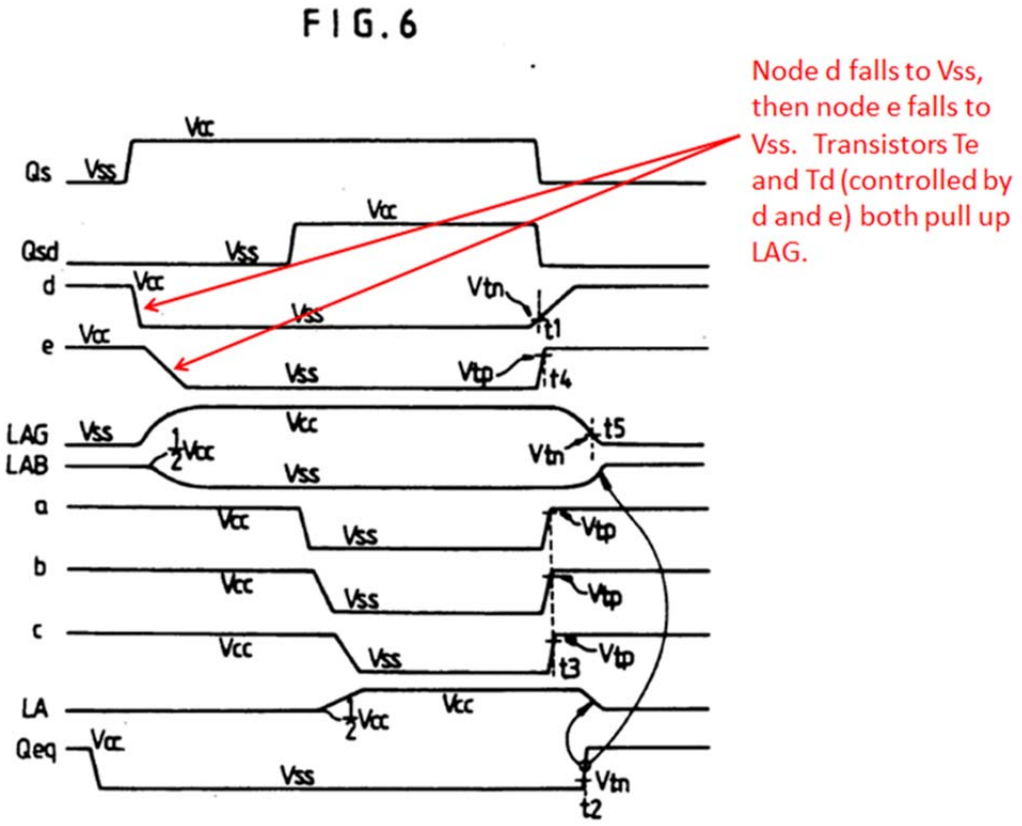
*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶116-118.)

As discussed above, the signal at node e (i.e., the gate of transistor Td) of *Seo* is a "delayed sense control signal." (*See supra* Section IX.A.1(e).)




(Ex. 1004, FIG. 5 (annotated); Ex. 1002, ¶116.)

*Seo* discloses that transistor Td ("the second switch") is controlled by the signal at node e ("controlled by the delayed sense control signal"). (Ex. 1004, 6:67-7:4.) *Seo* further discloses that both transistors Td and Te are in a conducting state to drive the LAG signal to Vcc after the signal at node e drops to Vss to turn on transistor Td ("such that the first switch and the second switch are concurrently activated after the delayed sense control signal is generated"). (Ex. 1004, FIG. 6; Ex. 1002, ¶117.) As seen from FIG. 6 of *Seo*, once the voltage at node e reaches Vss, PMOS transistor Td will be turned ON. (Ex. 1004, FIG. 6; Ex. 1002, ¶117.) At that time, voltage at node d is also at $V_{SS}$ implying that Td is also on and conducting current into node LAG. (Ex. 1002, ¶117.) As such, one of ordinary skill would have understood that transistors Te ("the first switch") and Td ("the second switch") are "concurrently activated after the delayed sense control signal is generated." (*Id*. at ¶117, Ex. 1004, FIG. 6.)




(Ex. 1004, FIG. 6 (annotated) (showing that signals at nodes d and e are both at Vss, and thus both PMOS transistors Td and Te are on after the potential of node e reaches a value of Vss); Ex. 1002, ¶117.)

Once Td is turned ON, transistors Td and Te together drive node LAG to Vcc to "completely turn on the n-channel MOS sense transistor Ts." (Ex. 1004, 7:4-7, FIG. 6.) In this respect, the disclosure in *Seo* (*i.e.*, transistor Te turns on first, then transistor Td turns on, and transistor Te remains on) is identical to the disclosure in the '302 patent (*i.e.*, transistor 313 turns on first, then transistor 318

turns on, and transistor 313 remains on). (Ex. 1002, ¶118; Ex. 1001, 6:10-36, FIG. 3.)

**2. Claim 11**

a) The clock driver circuit of claim 10 wherein the second impedance is less than the first impedance.

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶119-121.) *Seo* discloses that the resistance of transistor Td ("second impedance") is less than the resistance associated of transistor Te ("first impedance"). For example, *Seo* discloses that "transistor Te has small current driving capability" whereas "transistor Td [has] a large current driving capability." (Ex. 1004, 6:63-64, 7:2-3.) One of ordinary skill understood that there is an inverse relationship between resistance and current for a given voltage by virtue of the well-known Ohm's Law, which may be expressed as follows:

$$R_{tot} \equiv \frac{V_{ds}}{I_{ds}} = R_{sd} + R_{ch} = R_{sd} + \frac{L_{mask} - \Delta L}{\mu'_{eff} C_{ox} W (V_g - V_{on} - m V_{ds}/2)}. \qquad (4.72)$$

(Ex. 1008, 206; Ex. 1002, ¶119.)

The two leftmost terms in the above equation express resistance of a transistor as a ratio of voltage to current conducted across the drain and source terminals (*i.e.*, current driving capability of a transistor). (Ex. 1002, ¶120.) A consequence of this equation is that a larger current driving capability (*i.e.,* larger

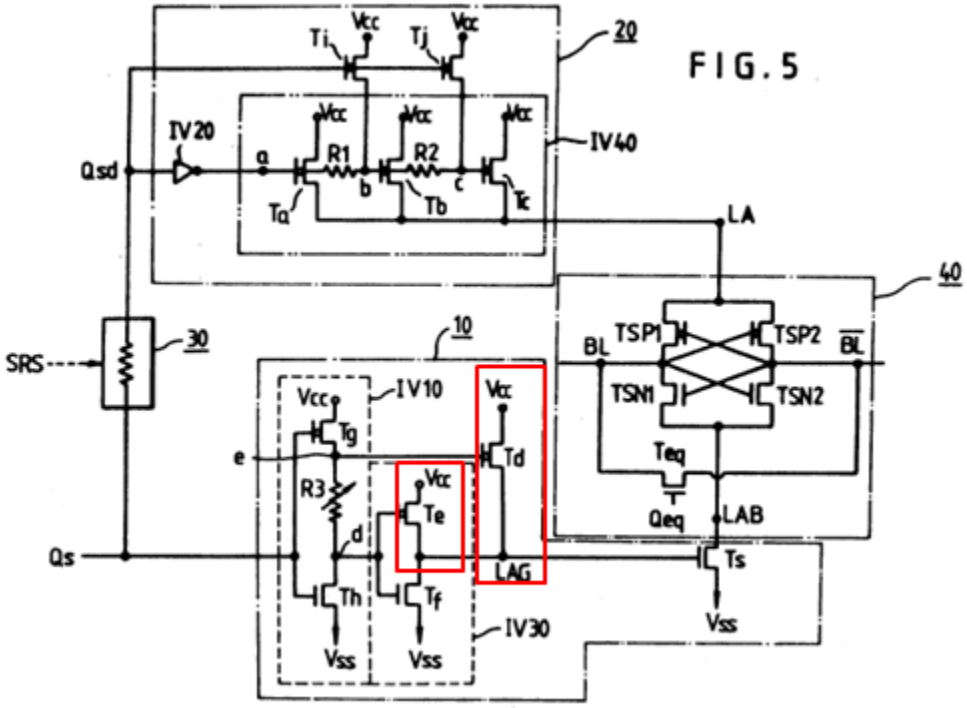
denominator in the V/I ratio in the equation) corresponds to a smaller resistance (*i.e.*, smaller impedance). (*Id.* at ¶120.)

Based on the above disclosure of *Seo* and the inverse relationship between impedance and current for a given voltage, one of ordinary skill would have understood that the current driving capability of transistor Td, which is relatively larger than that of the transistor Te, corresponds to the second impedance (associated with transistor Td) being less than the first impedance (associated with transistor Te) ("the second impedance is less than the first impedance"). (Ex. 1002, ¶121.)

**3. Claim 12**

a) The clock driver circuit of claim 10 wherein the first switch and the second switch are coupled to drive the timer unit output in parallel.

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶122.) Although claim 12 recites "the timer unit output," that term does not have antecedent basis. Therefore, claim 12 is indefinite under 35 U.S.C. § 112(b). To the extent Patent Owner contends that the term "timer unit output" should be interpreted as "the clock signal," *Seo* discloses that transistors Te ("the first switch") and Td ("and the second switch") are coupled to drive the signal at node LAG ("the clock signal") in parallel. This parallel arrangement is shown below:




(Ex. 1004, FIG. 5 (annotated to show transistors Td and Te coupled to drive LAG to Vcc in parallel); Ex. 1002, ¶122.) As discussed above with respect to claim element 10(h), *Seo* discloses that both transistors Td and Te concurrently drive the LAG signal to Vcc (*i.e.*, "in parallel") when the signal at node e turns on transistor Td. (*Id*. at FIG. 6; *supra* Section IX.A.1(h); Ex. 1002, ¶122.)

**4. Claim 1**

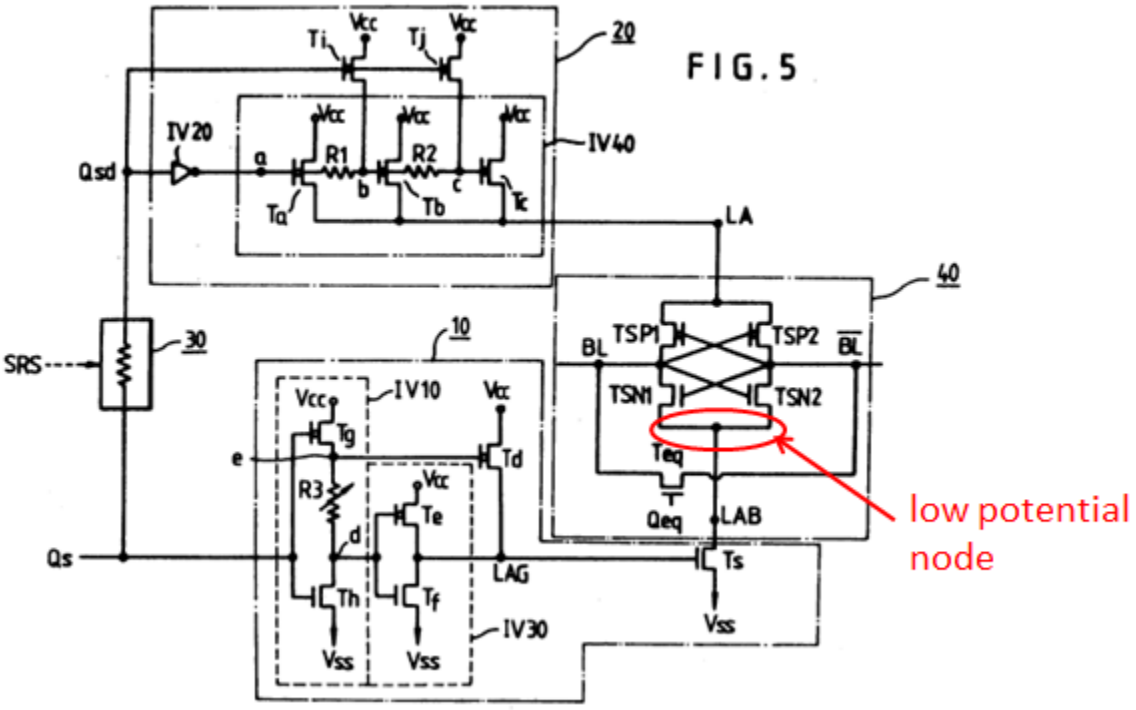
a) "A memory device comprising:"

To the extent that the preamble is determined to be limiting, *Seo* discloses this feature. (Ex. 1002, ¶123.) For example, *Seo* discloses an "improved sense amplifier driver for sensing and restoring data in *memory cells*" and that a "sensing signal LAB of the Vss level obtained through the turning-on operation of the n-

channel MOS sense transistor Ts carries out the sensing operation for the data stored in the memory cell" (Ex. 1004, Abstract, 7:7-10 (emphasis added).) Regarding a specific type of memory, *Seo* discloses "sensing the data from the memory cell of a CMOS *DRAM*." (*Id.* at 1:13-18 (emphasis added).) Based on such disclosure, one of ordinary skill would have understood that *Seo* discloses "a memory device." (Ex. 1002, ¶123; *see also* discussion above in Section VII.C; citations and analysis below for the remaining elements of this claim.)

> b) "a plurality of sense amplifiers distributed about an integrated circuit chip, each sense amplifier having a power node for receiving current;"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶124-131.) *Seo* discloses a sense amplifier 40 having a node for receiving current ("power node for receiving current"). Referring to FIG. 5 (shown below), *Seo* discloses that "sensing and restoring output signals LAB and LA . . . are supplied to *sense amplifier 40*" (Ex. 1004, 6:41-45 (emphasis added), FIG. 5.) *Seo* discloses a low potential node of sense amplifier 40 ("power node"), as shown below:




(*Id.* at FIG. 5 (annotated), 6:40-50 ("signals LAB, LA are respectively supplied to the common source (a lower potential node) of two n-channel MOS transistors TSN1, TSN2, and to the common source (a higher potential node) of two p-channel MOS transistors TSP1, TSP2"); Ex. 1002, ¶124.)

The low potential node at which signal LAB is supplied is a "power node for receiving current," because it receives current flowing from the sense amplifier. (Ex. 1004, FIG. 5 (showing LAB connected to Vss via transistor Ts, whereas LA is connected to Vcc via transistors Ta, Tb, and Tc; hence, current flows from sense amplifier 40 to LAB; Ex. 1002, ¶125.) This interpretation is consistent with the Specification and FIG. 1 of the '302 patent. (*See* Ex. 1001, 1:62-65 ("latch power

supply nodes are designated herein as an LN node (*i.e.*, a node coupling the low-side driver switch to the N-channel FET devices within the latch) and an LP node"); Ex. 1002, ¶125.)

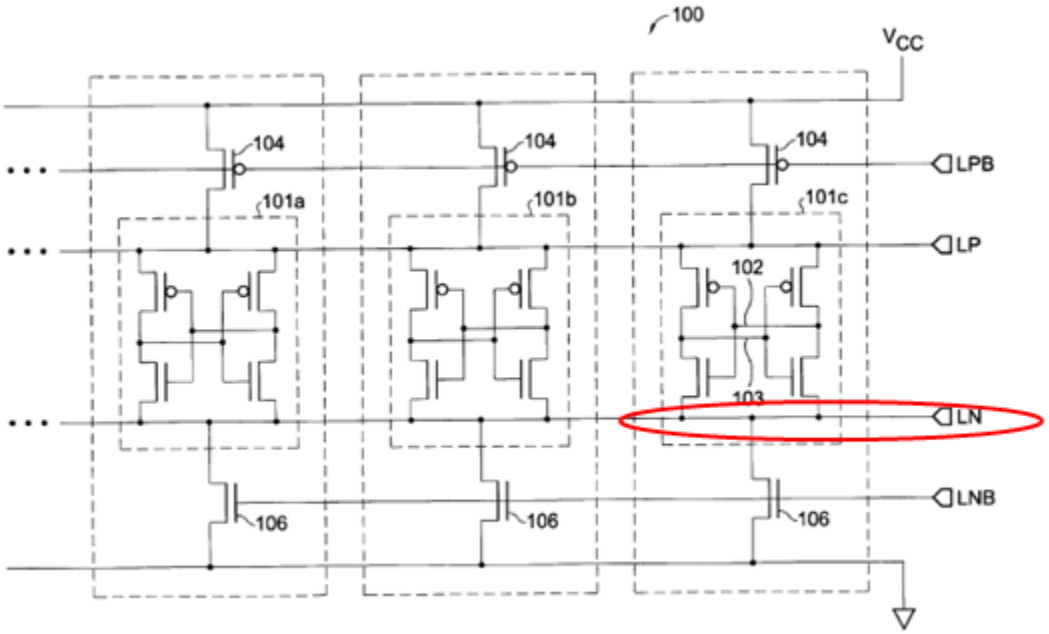


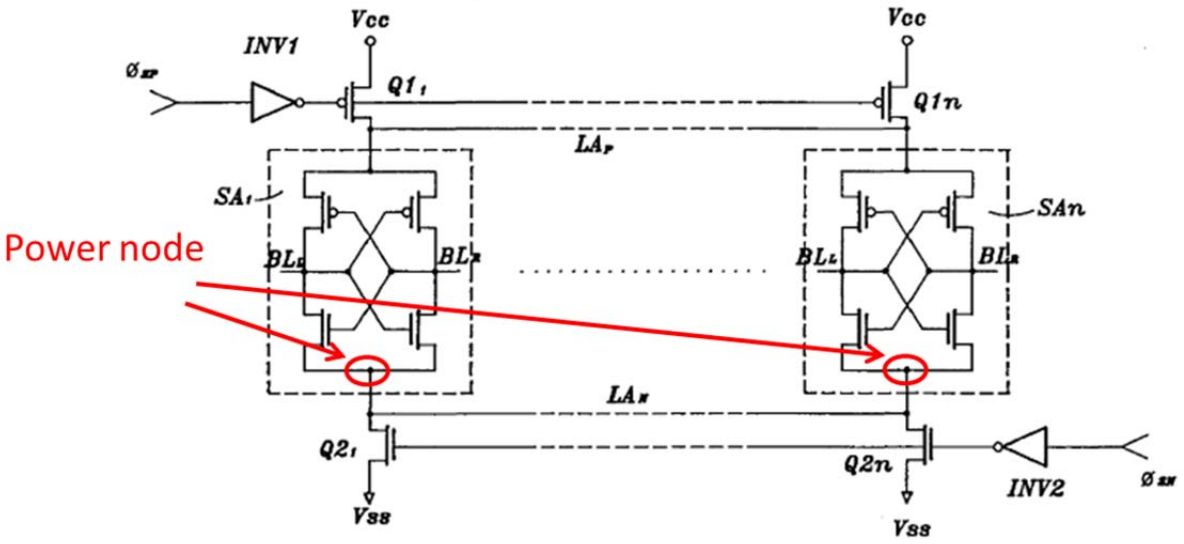

*FIG. 1*

(Ex. 1001, FIG. 1 (annotated to identify power supply node LN, which is in the same relative position as *Seo*'s low potential node); Ex. 1002, ¶125.)

*Seo* does not explicitly disclose or suggest "a plurality of sense amplifiers distributed about an integrated circuit chip, each sense amplifier having a power node for receiving current." But *Min*, which is in the same field of endeavor as *Seo*, discloses this feature. (Ex. 1005, 1:4-9; 12:12-13, FIGS. 1A, 1B, 3A, 3B; Ex. 1002, ¶126.) *Min* discloses in FIG. 1A "the conventional sense amplifier and a driving circuit . . . both of which are used generally." (Ex. 1005, 1:32-34.) *Min*

discloses that "[i]n order to improve the stability of the sense amplifiers" $SA_1$-$SA_n$, the MOS driving transistors Q1 and Q2 in FIG. 1A can be "replaced by smaller MOS transistors." (Ex. 1005, 1:64-21.) This configuration with multiple driving transistors $Q2_1$-$Q2_n$ is shown in FIG. 1B:

FIG. 1B (Prior Art)



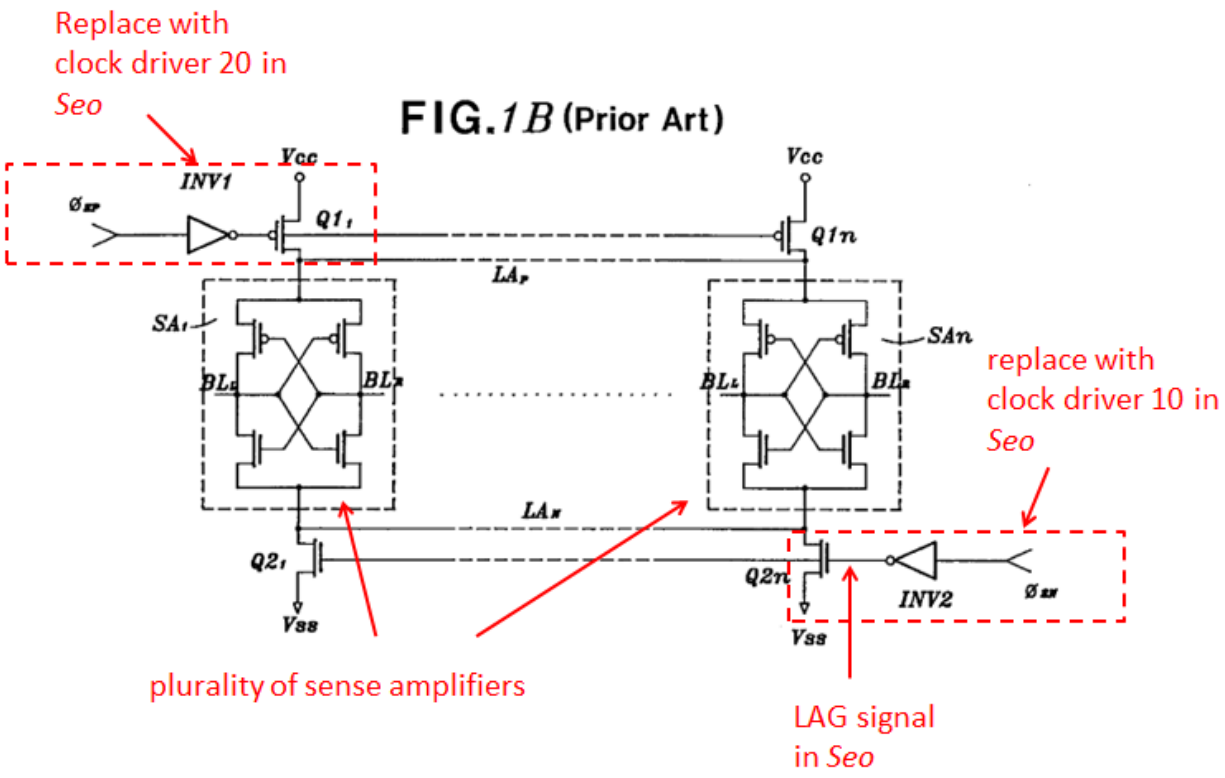

(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶ 126.) Thus, *Min* discloses a plurality of sense amplifiers ($SA_1$-$SA_n$) each of which has a power node that receives current. (*See* annotated FIG. 1B in *Min* above.) (Ex. 1002, ¶127.)

Furthermore, *Min* discloses "sense amplifiers of the *semiconductor memory device*" (Ex. 1005, 14:1-2 (emphasis added)), and one of ordinary skill would have understood that the semiconductor memory requires an integrated circuit chip. (Ex. 1002, ¶128.) One of ordinary skill would have understood that the sense amplifiers $SA_1$-$SA_n$ would have to be "distributed" about the memory device because these

circuits would be provided in a distributed manner on a circuit chip (*e.g.*, adjacent to each other). (*Id*.)

One of ordinary skill would have turned to *Min* for guidance regarding implementation of *Seo*'s sense amplifier driver circuitry given that *Seo* and *Min* are both directed to driving sense amplifiers. (*Id.* at ¶129.) Having turned to *Min*, such a person would have been motivated to modify *Seo* to include "a plurality of sense amplifiers distributed about an integrated circuit chip," with each sense amplifier having a power node (as in *Seo*) for receiving current. (*Id*.) For example, as discussed above in Section IX.A.1(a), one or ordinary skill in the art would have found it obvious to combine *Seo*'s sense amplifier driving circuitry with the conventional sense amplifier configuration disclosed in FIG. 1B of *Min*. (*See supra* Section IX.A.1(a); Ex. 1002, ¶129.)

The combined *Seo-Min* system may be conceptually visualized as follows:

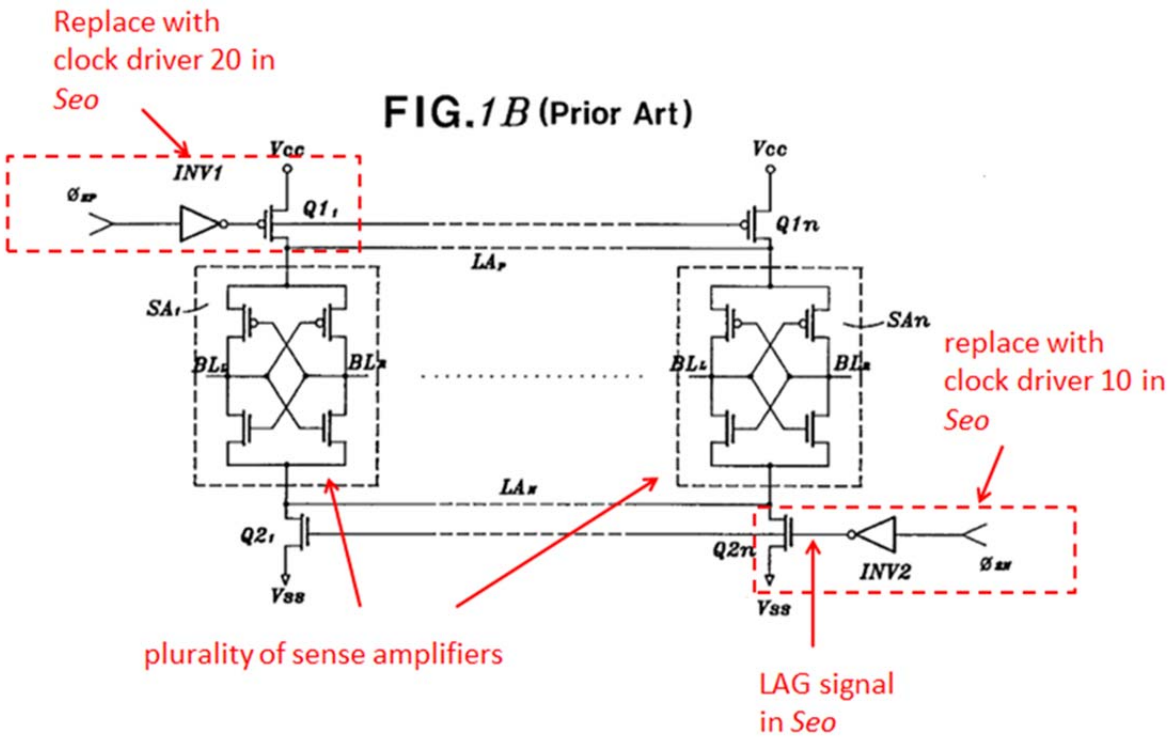



(Ex. 1005, FIG. 1B (annotated to show an exemplary combination of *Min* and *Seo*); Ex. 1002, ¶130.)

As seen from the above annotated FIG. 1B of *Min*, the combined *Seo-Min* system includes a plurality of sense amplifiers $SA_1$-$SA_n$ distributed about an integrated circuit chip, each sense amplifier having a power node $LA_N$ for receiving current. (Ex. 1002, ¶131.)

c) "a low-impedance power supply conductor;"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶132-135.) As discussed above with respect to claim element 1(b), the combined Seo-*Min* system may be pictorially illustrated as follows:

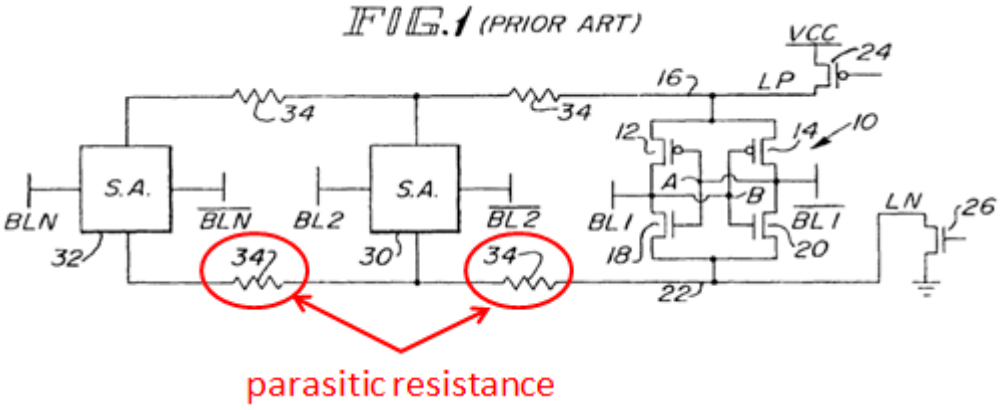



(Ex. 1002, ¶132; Ex. 1005, FIG. 1B (annotated); *supra* Section IX.A.1(b).)

The line conducting Vss in both *Seo* (Ex. 1004, FIG. 5) and *Min* (Ex. 1005, FIG. 1B) is a "power supply conductor" because one of ordinary skill understood that "Vcc" and "Vss" are traditionally used as labels for power supply lines corresponding to positive power and ground, respectively. (Ex. 1002, ¶133.)

*Seo* and *Min* do not explicitly disclose that the line Vss is a "low-impedance" power supply conductor. It was well known, however, to one of ordinary skill in the art at the time of the alleged invention of the '302 patent that parasitic resistance ("impedance") is present along any conductor. (Ex. 1002, ¶134.) This inherent characteristic of a conductor (including a conductor that provides the power supply Vss) is acknowledged by the inventor (Kim Hardee) of the '302

patent in one of his prior patent applications. For instance, *Hardee EP* admits that a conductor (*e.g.*, line 22) that provides power supply Vss to the sense amplifiers will have an associated parasitic resistance (*e.g.*, parasitic resistance 34). (Ex. 1006, 2:24-3:2, FIG. 1.):




(*Id*. at FIG. 1 (annotated); Ex. 1002, ¶134.)

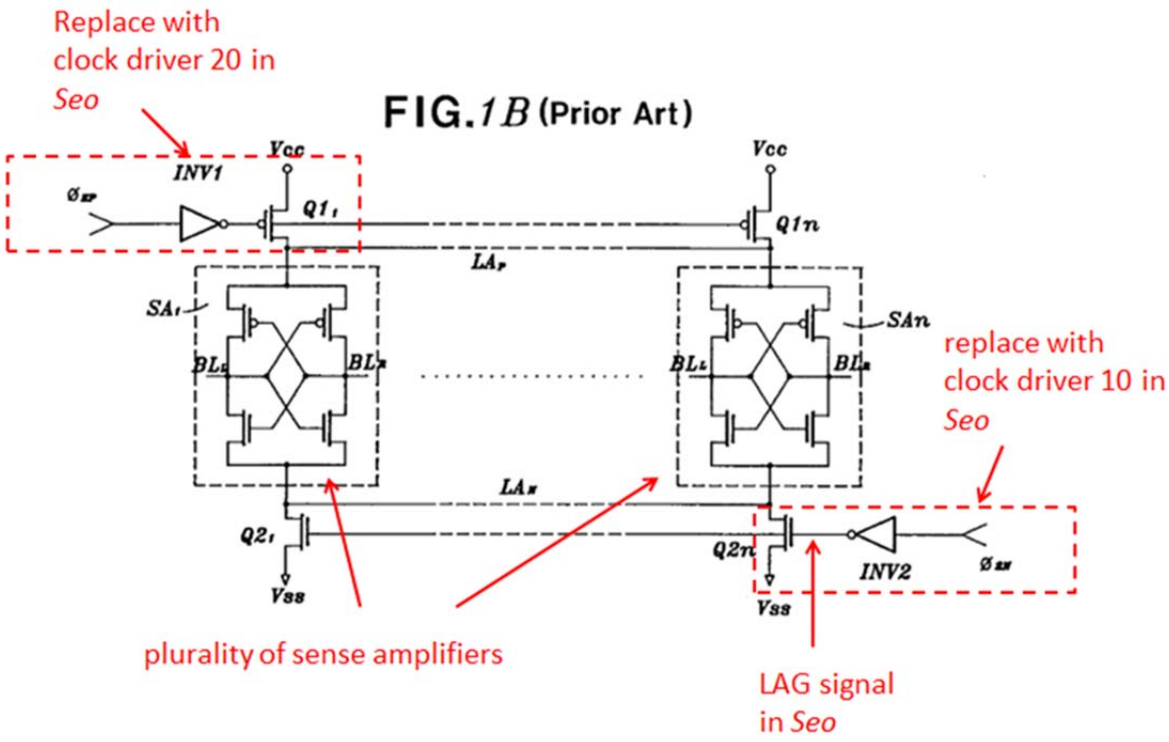
It was well known to one of ordinary skill and as acknowledged by *Hardee EP* that because of the parasitic resistance 34, the voltage along the conductor will drop such that a different voltage is provided to different devices that share that conductor. (Ex. 1002, ¶135; Ex. 1006, 2:33-44.) In fact, it was well known that a higher parasitic resistance would have resulted in greater delays for the signal propagating along the conductor. (Ex. 1002, ¶135.) Therefore, it was nothing new at the time of the invention of the '302 patent to design a power supply conductor (*e.g.*, the power supply conductor in the combined *Seo-Min* system that provides Vss to the driving transistors $Q2_1$-$Q2_n$) to have a lower parasitic resistance. (*Id*.) That is, given the well-known problem of parasitic resistance along a power supply

conductor, one of ordinary skill would have been motivated to decrease this parasitic resistance to lower the voltage variation along the conductor and also to reduce the signal delay resulting from the higher parasitic resistance. Therefore, one of ordinary skill would have been motivated to use a "low-impedance" power supply conductor *(e.g.*, a conductor with a lower parasitic resistance) for the Vss power supply conductor given that a high impedance conductor would have caused the issues discussed above. (*Id.* at ¶135.) *See KSR*, 550 U.S. at 401 ("When a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, § 103 likely bars its patentability.").

> d) "at least one drive transistor having a first current carrying electrode coupled to the power supply conductor, a second current carrying electrode coupled to the power nodes of a preselected number of the sense amplifiers, and a control electrode;"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶136-137.)

As discussed above with respect to claim element 1(b), the combined *Seo-Min* system may be pictorially illustrated as follows:




(Ex. 1002, ¶136; Ex. 1005, FIG. 1B (annotated).)

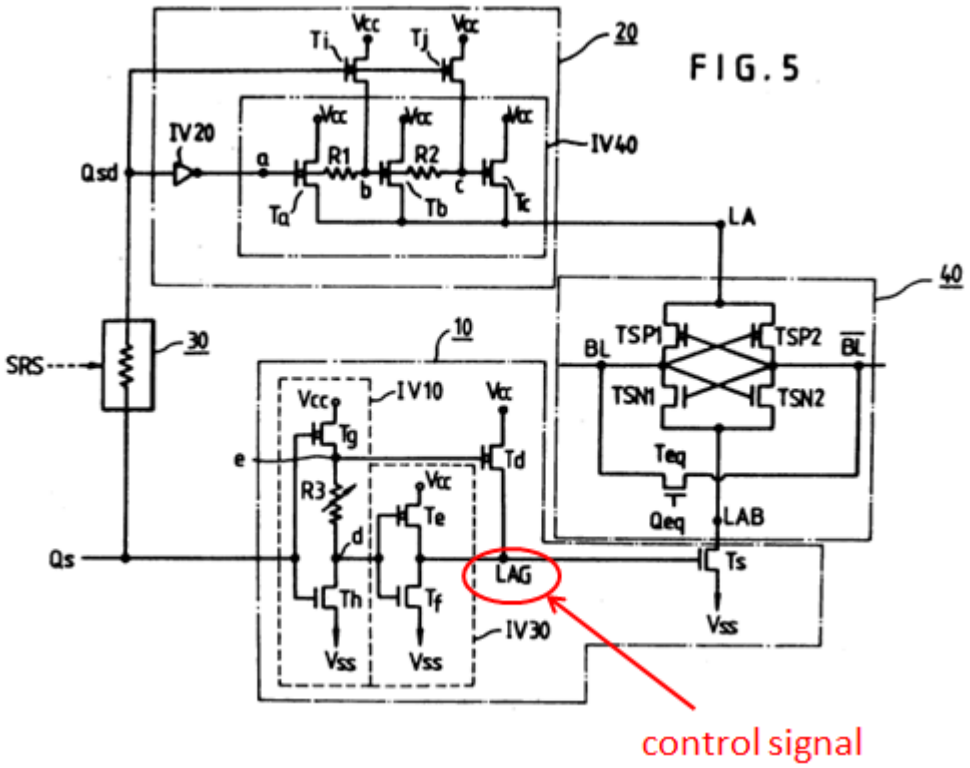
As seen from the above illustration, in the combined Seo-*Min* system, each of driving transistors $Q2_1$-$Q2_n$ ("at least one drive transistor") has a source terminal ("first current carrying electrode") coupled to Vss ("power supply conductor"). (Ex. 1002, ¶137.) Furthermore, the drain terminal ("second current carrying electrode") of each transistor $Q2_1$-$Q2_n$ is coupled to respective latch nodes $LA_N$ ("power nodes") of n sense amplifiers $SA_1$-$SA_n$ ("preselected number of the sense amplifiers". Also, each transistor $Q2_1$-$Q2_n$ has a gate terminal ("control electrode") coupled to the LAG signal. (*See* illustration above; Ex. 1002, ¶137.)

e) "a control line coupled to the control electrode;"

*Seo* in view of *Min* discloses or suggests this feature. For example, in the combined *Seo-Min* system, the line along which the LAG signal is provided is a "control line." (*See supra* Section IX.A.4(b); Ex. 1002, ¶138.)

f) "a timer unit having an output coupled to the control electrode and generating a control signal;"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶139-141.) This limitation includes a means-plus-function term, as discussed above at section VIII.A. The combined *Seo-Min* system (*see* claim element 1(b)) discloses generating a signal at node LAG ("generating a control signal"). (*See* Ex. 1004, 6:63-66, 7:4-7, FIGS. 1-2.) In the combined system, the signal at node LAG is generated by clock driver 10 shown in FIG. 5 of *Seo* that includes transistors Td and Te and resistor R3, which delays a signal at node d to generate a signal at node e.




(Ex. 1004, FIG. 5 (annotated); Ex. 1002, ¶139.)

Signal LAG controls transistor Ts and therefore is a "control signal." (Ex. 1004, FIG. 5, 7:4-7; Ex. 1002, ¶140.) Similarly, in the combined *Seo-Min* system illustrated above (*see* claim element 1(b)), signal LAG is provided to the gate terminal of driving transistors $Q2_1$-$Q2_n$ and controls their operation. Therefore, generating the LAG signal discloses "generating a control signal" in the combined system. (Ex. 1002, ¶140.)

*Seo* also discloses the structure corresponding to the recited function of this means-plus-function term, *i.e.* transistors Td and Te ("pair of transistors") and delaying resistance R3 ("one or more circuit components that delay a signal"). (Ex.

1004, FIG. 5, 6:56-7:7.) In the combined *Seo-Min* system, the output of that structure is the LAG signal (Ex. 1004, FIG. 5), which is coupled to the gate ("the control electrode") of driving transistors $Q2_1$-$Q2_n$. (Ex. 1002, ¶141.)

> g) "a first component within the timer unit causing the control signal to change from a first logic level towards a second logic level at a first rate; and"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶142-143.) This limitation includes a means-plus-function term, as discussed above at section VIII.B. The combined *Seo-Min* system (*see* claim element 1(b)) discloses generating a signal at node LAG. In the combined system, the LAG signal is generated by clock driver 10, which includes transistor Te causing the LAG signal ("control signal") to change from Vss towards Vcc at a rate corresponding to the current driving capability of transistor Te ("causing the control signal to change from a first logic level towards a second logic level at a first rate"). (Ex. 1004, 6:56-66, FIGS. 5 (showing transistor Te), 6 (showing change over time for signal LAG); Ex. 1002, ¶142.)

*Seo* also discloses the structure corresponding to the recited function of this means-plus-function term. For example, as discussed above with respect to claim element 1(f), *Seo* discloses transistor Te ("a first transistor"), which performs the recited function and is "within the timer unit" comprising Te, Td, and delaying resistance R3. (Ex. 1004, FIG. 5; *see supra* section IX.A.4.f; Ex. 1002, ¶143.)

h) "a second component within the timer unit causing the control signal to change to the second logic level at a second rate, wherein the second rate is greater than the first rate"

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶144-146.) This limitation includes a means-plus-function term, as discussed above at section VIII.C. The combined *Seo-Min* system (*see* claim element 1(b)) discloses generating a signal at node LAG using the clock driver 10 in *Seo*. In the combined system, the LAG signal is generated by clock driver 10. (*See supra* IX.A.4(b).) Clock driver 10 includes transistor Td, which causes the LAG signal to change to Vcc at a rate corresponding to its current driving capability ("causing the control signal to change to the second logic level at a second rate"). (Ex. 1002, ¶144; Ex. 1004, FIGS. 5 (showing transistor Td), 6, 6:67-7:7.)

Furthermore, *Seo* discloses that "since transistor Te has small current driving capability, the common output node LAG is not immediately raised to high level" and that "transistor Td [has] a large current driving capability. . . ." (Ex. 1004, 3:19-29.) Therefore, the "second rate" is greater than the "first rate." (Ex. 1002, ¶145.) This is confirmed by *Seo*, which discloses that the voltage at node LAG first changes slowly toward Vcc because the current driving capability of the transistor Te is relatively small when transistor Te turns on. (Ex. 1004, 6:61-7:7, FIG. 6.) When transistor Td is turned on after a delay caused by resistor R3, the voltage of node LAG changes more rapidly towards Vcc. (*Id*.)

*Seo* also discloses the structure corresponding to the recited function of this means-plus-function term. For example, as discussed above with respect to claim element 1(f), *Seo* discloses transistor Td ("a second transistor"), which performs the recited function and is "within the timer unit" comprising Td, Te, and delaying resistance R3. (Ex. 1004, FIG. 5, 6:67-7:7; *see supra* section IX.A.4(f); Ex. 1002, ¶146.)

> i) "such that the first component and the second component are concurrently activated to cumulatively affect the rate of change to the second logic level."

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶147-148.) *Seo* discloses that transistor Te ("first component") is already turned on when transistor Td ("second component") is later turned on, and that transistor Te remains turned on ("such that the first component and the second component are concurrently activated"). (Ex. 1004, 6:56-7:7, FIG. 6; Ex. 1002, ¶147.) In this respect, the disclosure in *Seo* is identical to the disclosure in the '302 patent (*i.e.*, transistor 303 turns on first, then transistor 308 turns on, and transistor 303 remains on). (Ex. 1002, ¶147; *see supra* section IX.A.1(h).)

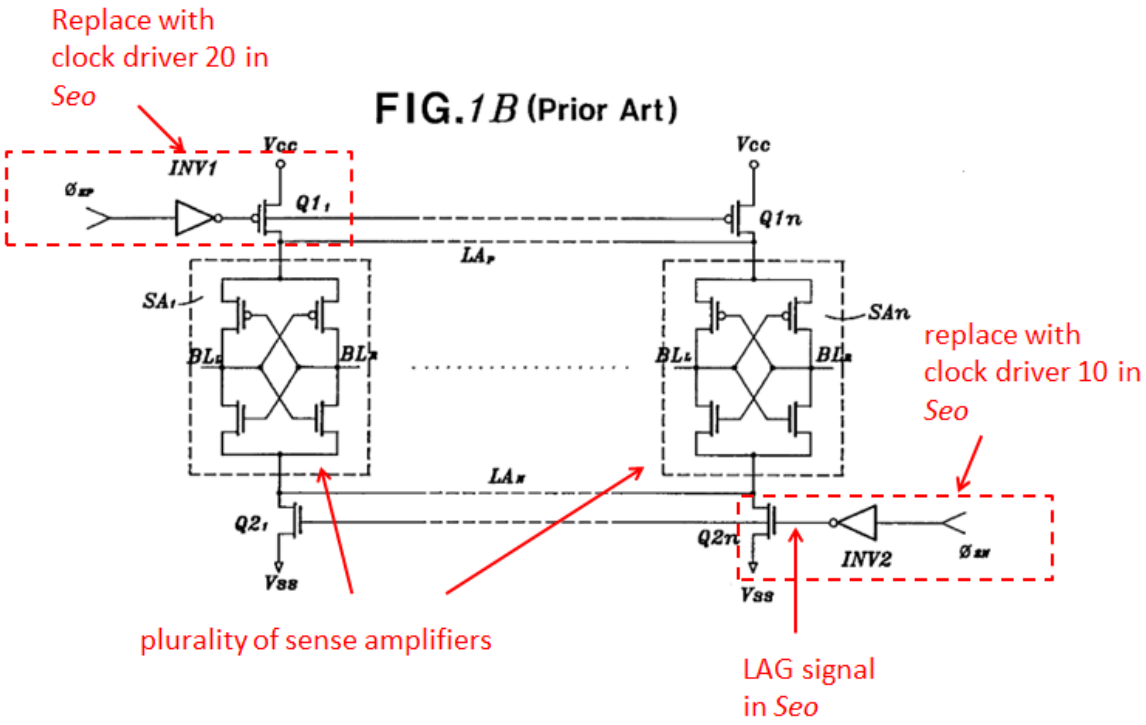
As discussed above at section IX.A.1(h), *Seo* discloses that transistors Te and Td are concurrently activated so that they both pull up the voltage at node LAG to Vcc, as opposed to only one of those transistors pulling up the voltage at

LAG ("cumulatively affect the rate of change to the second logic level"). (*See supra* section IX.A.1(h); Ex. 1002, ¶148.)

**5. Claim 2**

a) "The memory device of claim 1 further comprising a conductor coupling the power nodes of a number of sense amplifiers."

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶149.) As discussed above (*supra* Section IX.A.4(b)), the combined *Seo-Min* system may be represented as follows:

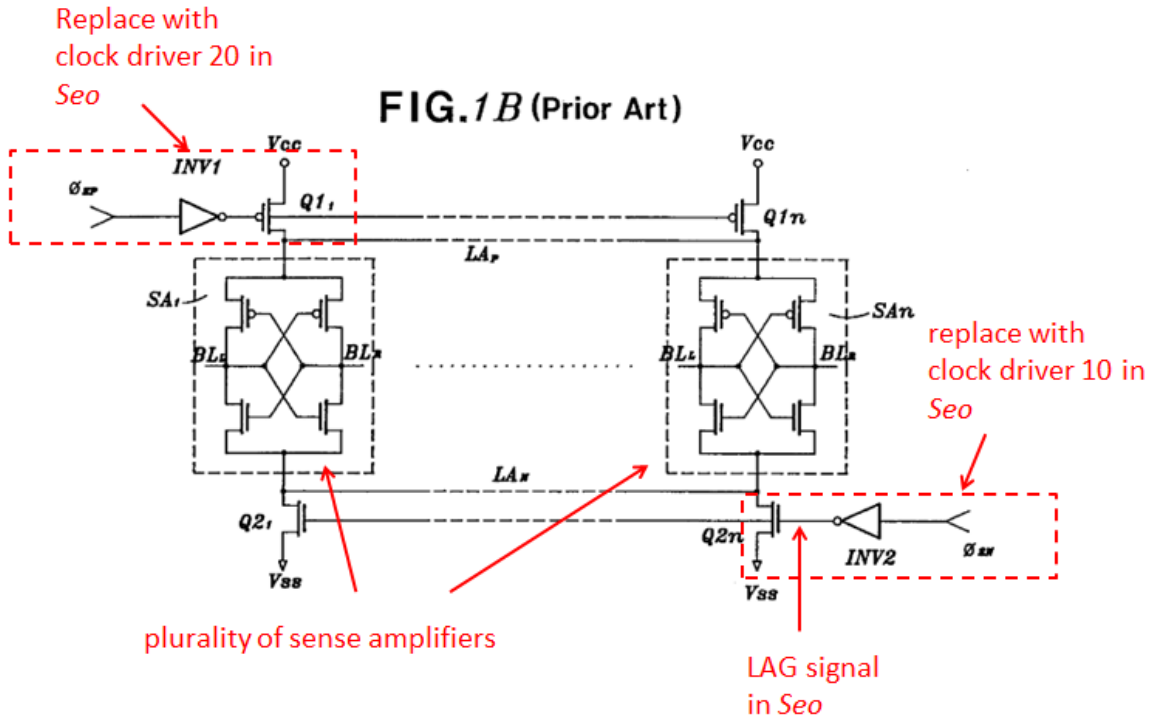



(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶149.) In the combined system as set forth above, the power nodes of the sense amplifiers $SA_1$-$SA_n$ are coupled by a conductor (the line $LA_N$). (Ex. 1002, ¶149.)

### 6. Claim 3

a) The memory device of claim 2 wherein the at least one drive transistor is provided for each sense amplifier.

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶150-151.) As discussed above (*supra* Section IX.A.4(b)), the combined *Seo-Min* system may be represented as follows:



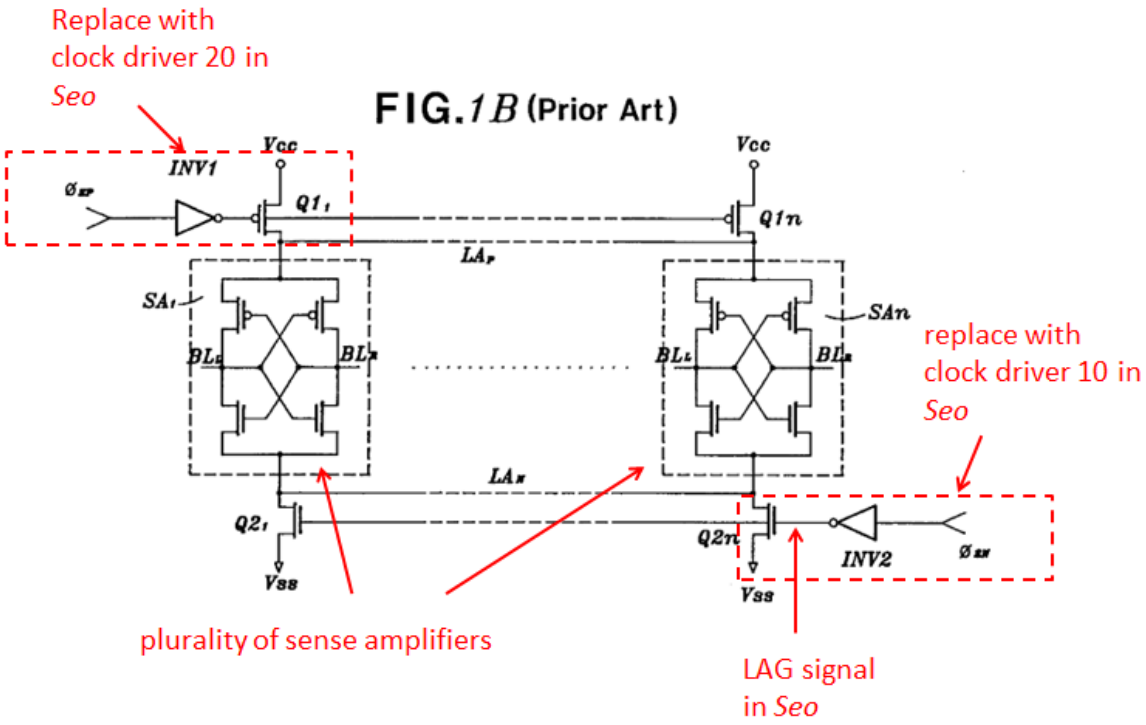

(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶150.)

In the combined system as set forth above, each sense amplifier among $SA_1$-$SA_n$ is provided with a respective driver transistor $Q2_1$-$Q2_n$. (Ex. 1002, ¶151; Ex. 1005, 4:5-17.)

### 7. Claim 4

a) The memory device of claim 2 wherein the at least one drive transistor comprises a drive transistor that is shared by each of the number of sense amplifiers coupled to the conductor.

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶152-153.) As discussed above (*supra* Section IX.A.4(b)), the combined *Seo-Min* system may be represented as follows:




(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶152.)

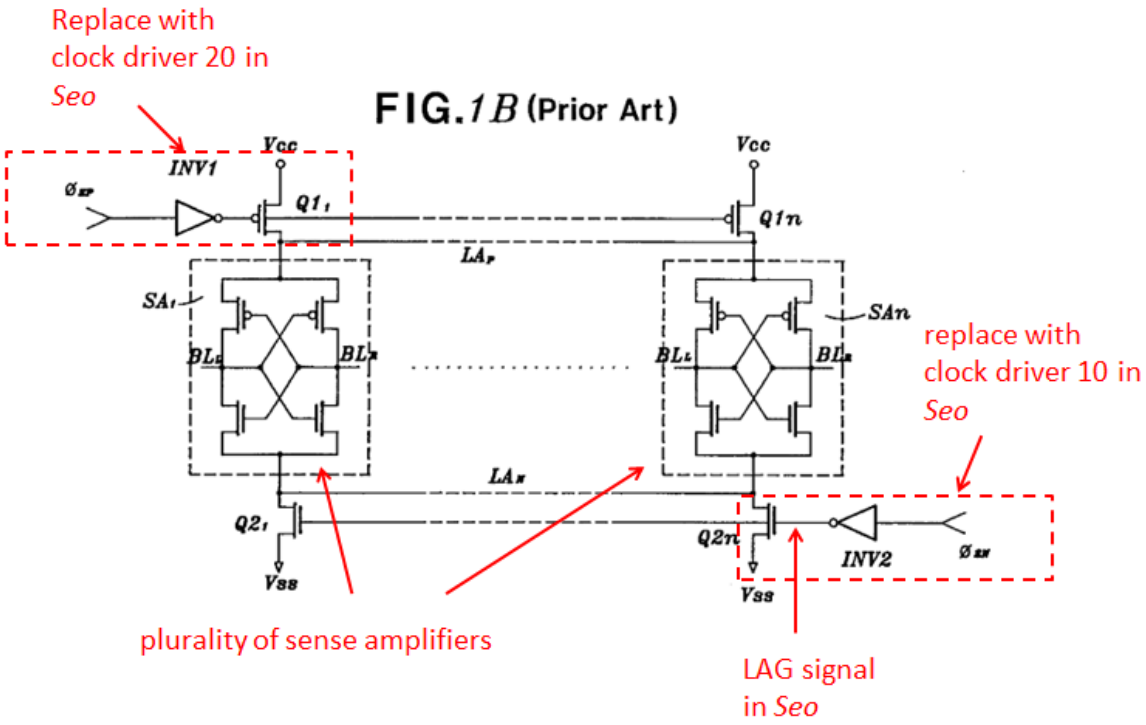
One of ordinary skill in the art would have understood that in the combined system as set forth above, each sense amplifier among $SA_1$-$SA_n$ provides current to driver transistors $Q2_1$-$Q2_n$. That is, each of $Q2_1$-$Q2_n$ is shared between the sense amplifiers $SA_1$-$SA_n$ and each of $Q2_1$-$Q2_n$ pulls the common conductor $LA_N$ ("the

conductor") to Vss. (Ex. 1002, ¶153.)

**8. Claim 5**

a) The memory device of claim 2 wherein each sense amplifier receives current from more than one drive transistor.

*Seo* in view of *Min* discloses or suggests this feature. (Ex. 1002, ¶¶154-155.) As discussed above (*supra* Section IX.A.4(b)), the combined *Seo-Min* system may be represented as follows:




(Ex. 1005, FIG. 1B (annotated); Ex. 1002, ¶154.)

In the combined system as set forth above, each sense amplifier among $SA_1$-$SA_n$ receives current from more than one of driving transistors $Q1_1$-$Q1_n$ because all driving transistors are connected to the same node $LA_P$, which is shared by the sense amplifiers $SA_1$-$SA_n$. Thus, one of ordinary skill would have understood that

"each sense amplifier" in the combined system "receives current from more than one drive transistor." (Ex. 1002, ¶155.)

### B. Ground 2: *Seo* Anticipates Claims 10-12

In the corresponding district court litigation, Patent Owner has taken the position that the preamble of claims 10-12 is not limiting. To the extent the Board agrees with Patent Owner that the preamble of claims 10-12 is not limiting, *Seo* anticipates claims 10-12. (Ex. 1002, ¶¶156-166.) This is because as discussed above (*see supra* Section IX.A.1(a)), *Seo* is combined with *Min* only to address the preamble's limitation that a clock signal controls the operation of more than one sense amplifier driver transistor. Therefore, ground 2 (which does not consider the preamble to be limiting) tracks ground 1 and differs from ground 1 with respect to ground 1's analysis of the preamble of claims 10-12.

#### 1. Claim 10

> a) A sense amplifier clock driver circuit for an integrated circuit memory, the driver circuit providing at least one clock signal for controlling the operation of sense amplifier driver transistors and comprising:

To the extent Patent Owner argues that the preamble is not limiting, *Seo* need not disclose the preamble. Regardless, *Seo* discloses a sensing clock driver 1 ("sense amplifier clock driver circuit") for a CMOS DRAM cell ("integrated circuit memory"), the sensing clock driver 1 providing a clock signal at node LAG ("at least one clock signal") for controlling operation of an NMOS sense transistor

Ts ("sense amplifier driver transistor"). (*See supra* Section IX.A.1(a); Ex. 1002, ¶157.)

> b) a sense control signal node receiving an externally generated sense control signal indicating when sensing is to occur;

*Seo* discloses this feature. (*See supra* Section IX.A.1(b); Ex. 1002, ¶158.)

> c) a first impedance having a terminal coupled to a selected logic level signal;

*Seo* discloses this feature. (*See supra* Section IX.A.1(c); Ex. 1002, ¶159.)

> d) a first switch having current carrying electrodes coupled to drive the clock signal to a selected logic level through the first impedance, the first switch controlled by the sense control signal;

*Seo* discloses this feature. (*See supra Section* IX.A.1(d); Ex. 1002, ¶160.)

> e) a delay unit coupled to the sense control signal node and generating a delayed sense control signal

*Seo* discloses this feature. (*See supra* Section IX.A.1(e); Ex. 1002, ¶161.)

> f) a second impedance having a terminal coupled to the selected logic level signal; and

*Seo* discloses this feature. (*See supra* Section IX.A.1(f); Ex. 1002, ¶162.)

> g) a second switch having current carrying electrodes coupled to drive the clock signal to the selected logic level through the second impedance,

*Seo* discloses this feature. (*See supra* Section IX.A.1(g); Ex. 1002, ¶163.)

h) the second switch controlled by the delayed sense control signal such that the first switch and the second switch are concurrently activated after the delayed sense control signal is generated.

*Seo* discloses this feature. (*See supra* Section IX.A.1(h); Ex. 1002, ¶164.)

**2. Claim 11**

a) The clock driver circuit of claim 10 wherein the second impedance is less than the first impedance.

*Seo* discloses this feature. (*See supra* Section IX.A.2; Ex. 1002, ¶165.)

**3. Claim 12**

a) The clock driver circuit of claim 10 wherein the first switch and the second switch are coupled to drive the timer unit output in parallel.

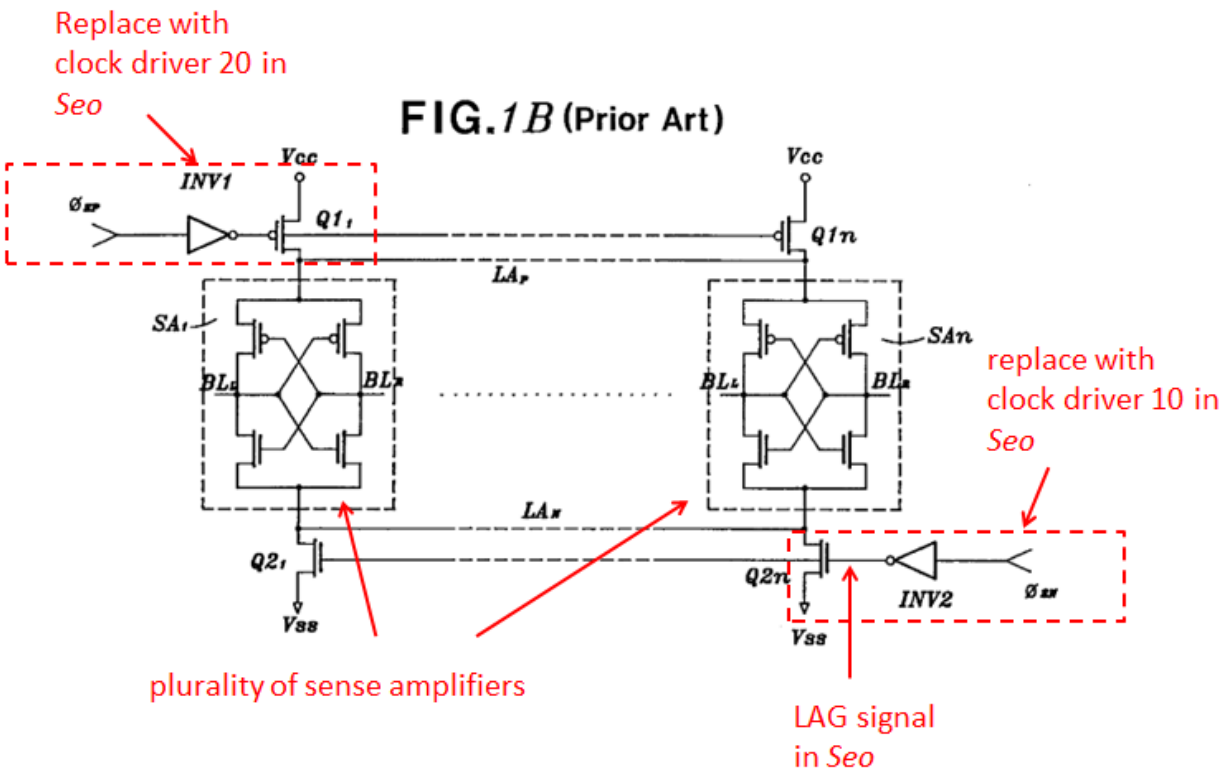
*Seo* discloses this feature. (*See supra* Section IX.A.3; Ex. 1002, ¶166.)

### C. Ground 3: *Seo, Min,* and *Schuster* Render Obvious Claim 6

**1. Claim 6**

a) The memory device of claim 1 further comprising:
a data line;
a latch node in the sense amplifier to hold a signal generated by the sense amplifier; and
a pass transistor coupled between the latch node and the data line.

*Seo*, in view of *Min* and *Schuster* discloses or suggests these limitations. (Ex. 1002, ¶¶167-172.) As discussed above (*supra* Section IX.A.4(b)), the combined *Seo-Min* system may be illustrated as follows:




(Ex. 1005, FIG. 1B (annotated to show an exemplary combination of *Min* and *Seo*); Ex. 1002, ¶¶167.)

*Min* discloses that each sense amplifier $SA_1$-$SA_n$ includes two internal nodes to which a pair of bit lines $BL_L$, $BL_R$ are connected. (Ex. 1005, 2:8-13, 4:13-17, FIGS. 1A, 1B.) It was well known at the time of the alleged invention that when one of those sense amplifiers is connected to Vcc (at node $LA_P$, via a corresponding driving transistor $Q1_i$) and Vss (at node $LA_N$, via a corresponding driving transistor $Q2_i$), a small difference between voltages at $BL_L$ and $BL_R$ becomes amplified by the sense amplifier, such that the sense amplifier latches into a stable state with one of the latch nodes at Vcc and the other latch node at Vss.

(Ex. 1002, ¶168.) As such, one of ordinary skill would have understood that each of those internal nodes is "a latch node in the sense amplifier to hold a signal generated by the sense amplifier." (*Id.*)

While the combined *Seo-Min* system does not expressly disclose a data line and a pass transistor coupled between the latch node and the data line, *Schuster*, in the same field of endeavor as *Seo* and *Min* (sense amplifier circuitry for a memory), discloses those features. (Ex. 1002, ¶169.) *Schuster* discloses "p-channel decoupling devices between the small capacitance nodes of the sense amplifier (SA and SAN) and the high capacitance I/O lines." (Ex. 1007, 706.) The decoupling devices are shown in FIG. 5 of *Schuster*:

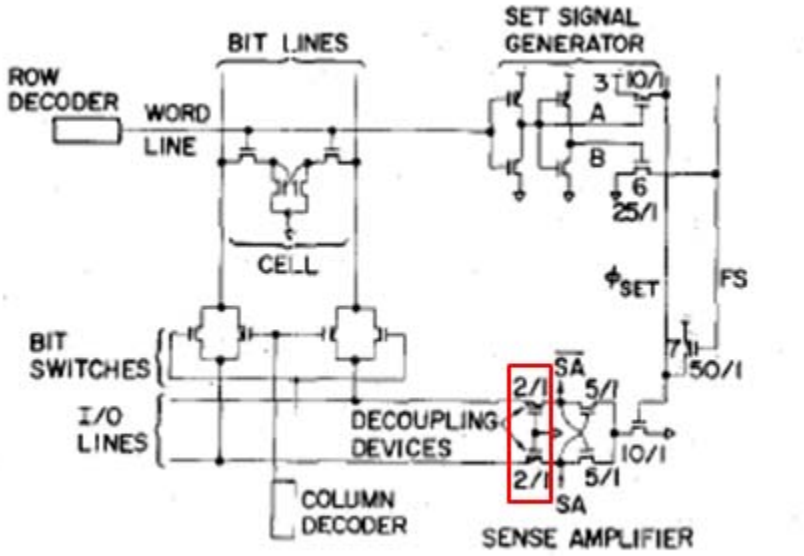



Fig. 5. Array and self-timed sense-amplifier circuitry.

(*Id.* at 706, FIG. 5; Ex. 1002, ¶169.)

One of ordinary skill would have understood that each decoupling device is

a PMOS transistor and in particular is a "pass transistor coupled between [a] latch node and [a] data line." (Ex. 1002, ¶170.) Each of *Schuster*'s nodes SA and SAN of the sense amplifier is a latch node and holds a signal generated by the sense amplifier. (*Id*.) Each decoupling device is a transistor that operates as a switch to pass logic levels between a latch node of sense amplifier SA and an I/O line ("data line"), and thus would have been understood by one of ordinary skill to be a "pass transistor." (*Id.*) This interpretation is consistent with the specification of the '302 patent. (*See id.*; Ex. 1001, 1:45-46 ("each latch output is coupled to a data input/output (I/O) line by a pass transistor").)

It would have been obvious to one of ordinary skill at the time of the alleged invention of the '302 patent to modify the combined *Seo-Min* system to include a data line and a pass transistor coupled between the latch node and the data line, as in *Schuster*. (Ex. 1002, ¶171.) For example, one of ordinary skill would have understood such a modification would have enabled the combined *Seo-Min* system to be implemented in a practical application involving a data line, as suggested by *Seo*. (Ex. 1004, 1:7-13 ("CMOS DRAM").) This modification would have been a mere combination of known prior art elements (the sense amplifiers in the combined system and *Schuster*'s I/O line and decoupling device) according to known methods (*e.g.*, coupling the components in the way disclosed at FIG. 5 of *Schuster*), to yield predictable results (*e.g.*, controllable access between the data

line and the latch node, by way of the pass transistor, in the same manner as disclosed by *Schuster*). *KSR*, 550 U.S. at 416. (Ex. 1002, ¶171.)

Furthermore, this would have been a simple modification within the skill of an ordinary artisan, because it would have been merely the use of a pass transistor for its ordinary purpose (selectively providing coupling between two nodes) to achieve a working system where data can be selectively read and written stored in memory. (Ex. 1002, ¶172.)

## X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-6 and 10-12 of the '302 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: October 7, 2016 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

## CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,195,302 contains, as measured by the word-processing system used to prepare this paper, 13,910 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: October 7, 2016

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

**CERTIFICATE OF SERVICE**

I hereby certify that on October 7, 2016, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,195,302 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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