Paper No. __
Filed: October 7, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,088,270

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,088,270

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-19, 30-32, and 34-39 ("the challenged claims") of U.S. Patent No. 6,088,270 ("the '270 patent") (Ex. 1001), which is currently assigned to ProMOS Technologies, Inc. ("Patent Owner") according to USPTO records. For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Austin Semiconductor, LLC, and Samsung Semiconductor, Inc.

Related Matters: Patent Owner has asserted the '270 patent against Petitioner and the above real parties-in-interest in *ProMOS Technologies, Inc. v. Samsung Electronics, Ltd., Co.*, Case No. 1:15-cv-00898-SLR-SRF (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 6,849,897 ("the '897 patent"), 6,020,259 ("the '259 patent"), 6,699,789 ("the '789 patent"), 6,195,302 ("the '302 patent"), and 5,761,112 ("the '112 patent") in this action. Petitioner is concurrently filing IPR petitions on the '897, '259, '789, '302, and '112 patents.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No.

46,224), and backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-Promos1-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the ’270 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

A. Claims for Which Review is Requested

Petitioner respectfully requests review of claims 1-19, 30-32, and 34-39 (“challenged claims”) of the ’270 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following grounds:

Ground 1: Claims 1-3, 8-11, 30-32, 34-36, and 38 are unpatentable under

pre-AIA 35 U.S.C. § 102(b) based on Japanese Patent Publication JPS58-128087 to Inoue *et al.* ("*Inoue*") (Ex. 1005)[1];

Ground 2: Claims 4-6, 12-14, 17, 19, 37, and 39 are unpatentable under pre-AIA 35 U.S.C. § 103(a) in view of *Inoue* and U.S. Patent No. 5,293,347 to Ogawa ("*Ogawa*") (Ex. 1006);

Ground 3: Claims 7 and 15 are unpatentable under pre-AIA 35 U.S.C. § 103(a) in view of *Inoue*, *Ogawa*, and Okamura *et al.*, "Decoded-Source Sense Amplifier for High-Density DRAM's," *IEEE Journal of Solid-State Circuits*, Vol. 25., No. 1, February 1990 ("*Okamura*") (Ex. 1007); and

Ground 4: Claims 16 and 18 are unpatentable under pre-AIA 35 U.S.C. § 103(a) in view of *Inoue*.

The '270 patent issued from U.S. Application No. 08/284,183 filed August 2, 1994, which claims the priority of U.S. Application No. 07/976,312 filed November 12, 1992. *Inoue* was published on July 30, 1983. *Okamura* was

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[1] Ex. 1005 is a compilation containing the English-language translation of *Inoue* (Ex. 1005, 1-5), followed by the Japanese language version (*id.*, 6-10), an affidavit required by 37 C.F.R. § 42.63(b) (in the form of a declaration as permitted by 37 C.F.R. § 42.2) follows the Japanese-language version (*id.*, 11) and a certification of correction to the certified translation follows the declaration (*id*., 12.)

published in *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 1 in February, 1990. (*See* Ex. 1007, 18; *see also* Ex. 1011, 496 (reference 2) (providing evidence that *Okamura* was cited by other articles prior to August 2, 1994).) Thus, both *Inoue* and *Okamura* are prior art to the '270 patent at least under pre-AIA 35 U.S.C. § 102(b). *Ogawa* was filed on December 30, 1991 and is prior art to the '270 patent at least under pre-AIA 35 U.S.C. § 102(e).

Inoue and *Ogawa* were never considered by the Patent Office during prosecution of the '270 patent. (*See* Ex. 1001, 1 (References Cited).) *Okamura* is referenced in the specification and was listed in an IDS submitted during prosecution. (*Id.*, 3:28-31; Ex. 1003, 62.) However, *Okamura* is presented in a new light here and supported by the testimony of Dr. R. Jacob Baker (Ex. 1002). (*See, e.g.*, Section IX.C.) As such, consideration of *Okamura* by the Patent Office during prosecution should not preclude the Office from adopting the invalidity ground in this Petition involving *Okamura*.

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '270 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering or a similar field, and at least two to three years of

experience in design of semiconductor memory circuits. (Ex. 1002, ¶19.)[2] More education can supplement practical experience and vice versa. (*Id*.)

VII. OVERVIEW OF THE TECHNOLOGY, '270 PATENT, AND PRIOR ART

A. Technology Background

At the time of the alleged invention of the '270 patent, it was well known that integrated circuit memories could include memory cell arrays consisting of thousands of memory cells arranged in a matrix of rows (word lines) and columns (bit lines), with each memory cell located at or near the crossing of a bit line and word line. (Ex. 1002, ¶¶20-34; Ex. 1001, 1:14-30, 1:35-36, 2:14-15.) The basic architecture of such integrated circuit memories can be understood by looking at the structure of a dynamic random access memory (DRAM), which was a type of known integrated circuit memory. (Ex. 1002, ¶32.)

A DRAM includes a memory cell array consisting of memory cells arranged in a matrix of rows of word lines and columns of bit lines. (Ex. 1008, 1:22-34.)

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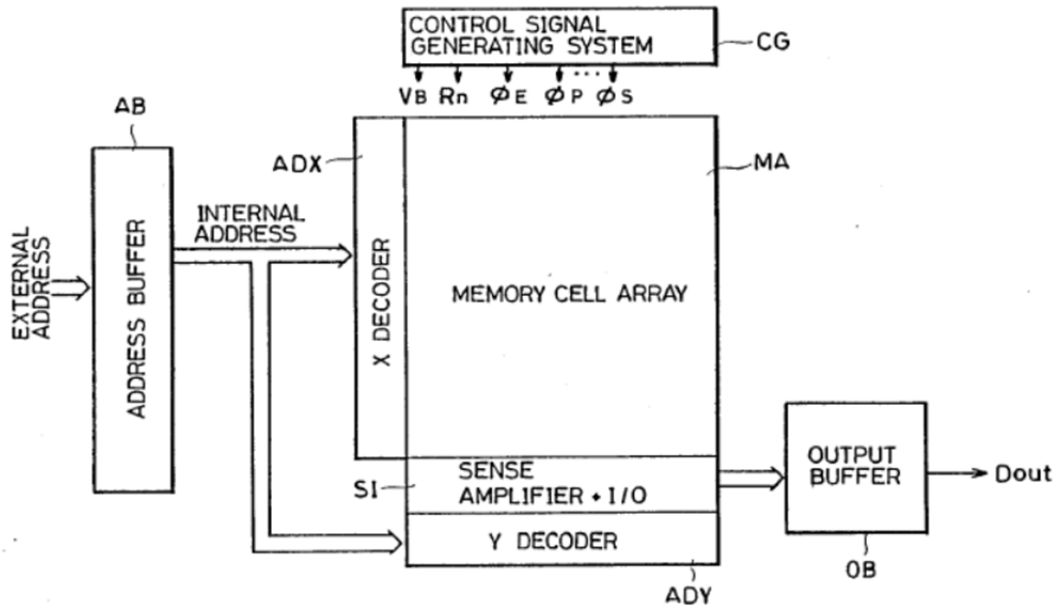
[2] Petitioner submits the declaration of Dr. R. Jacob Baker (Ex. 1002), an expert in the field of the '270 patent. (Ex. 1002, ¶¶5-15.)

FIG.1 PRIOR ART



(Ex. 1008, FIG. 1, showing a conventional DRAM.)

Circuitry was known to be used to read and write to the memory cells of a DRAM. (Ex. 1008, 1:20-34, FIGS. 1-2.) For instance, it was known to configure a DRAM circuit with an address buffer AB that may receive an externally applied external address and generate an internal address, which is provided to an X decoder ADX and Y decoder ADY that decode the internal address and select a corresponding row and column, respectively, in the memory cell array MA. (*Id*.) The bit lines were often coupled into complementary bit line pairs, with each pair associated with a sense amplifier that amplifies the signal on the bit lines during a read operation and drives/controls the bit lines when data is being written into the

memory cells. (*See, e.g.*, Ex. 1001, 1:36-45; *see also* Ex. 1008, FIG. 2.) (Ex. 1002, ¶¶34, 21-23 (discussing MOSFETs and referring to Ex. 1009.)

B. The '270 Patent

The '270 patent relates to a "sense amplifier for a very high density integrated circuit memory using CMOS technology." (Ex. 1002, ¶¶35-37; Ex. 1001, Abstract.) The '270 patent is titled "Sense Amplifier with Local Write Drivers" and acknowledges that sense amplifiers were known at the time of the alleged invention. (Ex. 1001, Title, FIG. 1, 1:47-2:13.) The '270 patent further acknowledges that it was known for integrated circuit memories to be organized into rows and columns and for a sense amplifier to be connected to each column of the memory. (*Id.*, 1:14-41.) For example, "FIG. 1 illustrates a prior art configuration" in which sense amplifiers are connected to respective pairs of bit lines, with each sense amplifier implemented using transistors that are arranged to latch into a stable state. (*Id.*, 1:47-48, 2:12-14, FIG. 1.) (Ex. 1002, ¶35.)

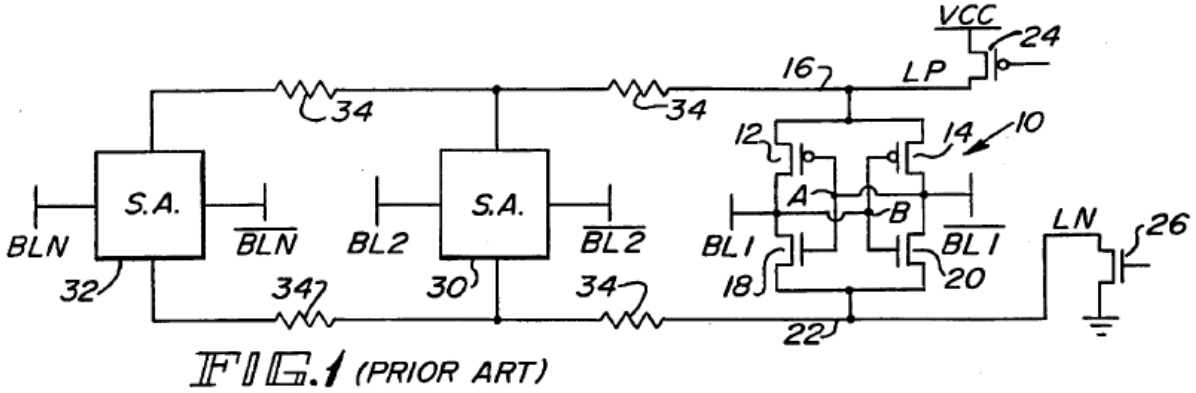


FIG. 1 (PRIOR ART)

(Ex. 1001, FIG. 1; *see also id.*, 1:47-2:13.)

Regarding the preferred embodiment of the '270 patent, "FIG. 5 illustrates a preferred sense amplifier 100." (*Id.*, 6:2-6.) The embodiment of figure 5 includes a latch (transistors 112, 114, 118, and 120) that was known in the prior art, as noted by the '270 patent in its background section regarding sense amplifier 10 shown. (*Id.*, 1:46-62, FIG. 1.) The '270 patent discloses that the latch of figure 5 is coupled to respective power supply lines VCC and VSS by local sense amplifier drive transistors 140 and 142 (*id.*, 6:56-63, FIG. 5.), and to a local column read amplifier at the bottom of figure 5 (*id.*, 6:66-7:13, FIG. 5.)

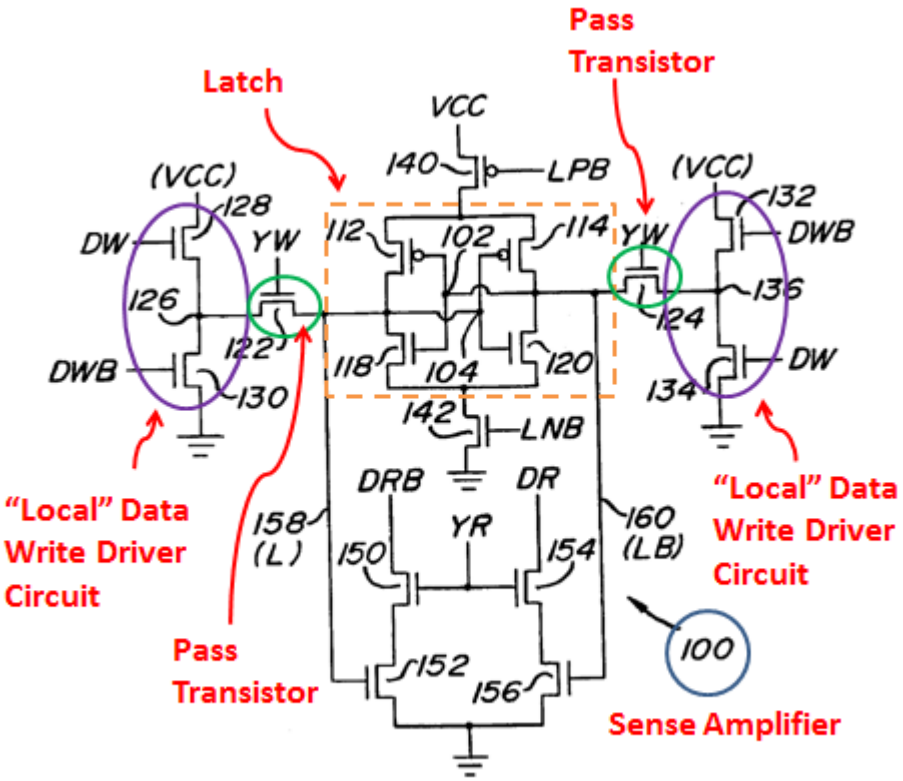


FIG. 5

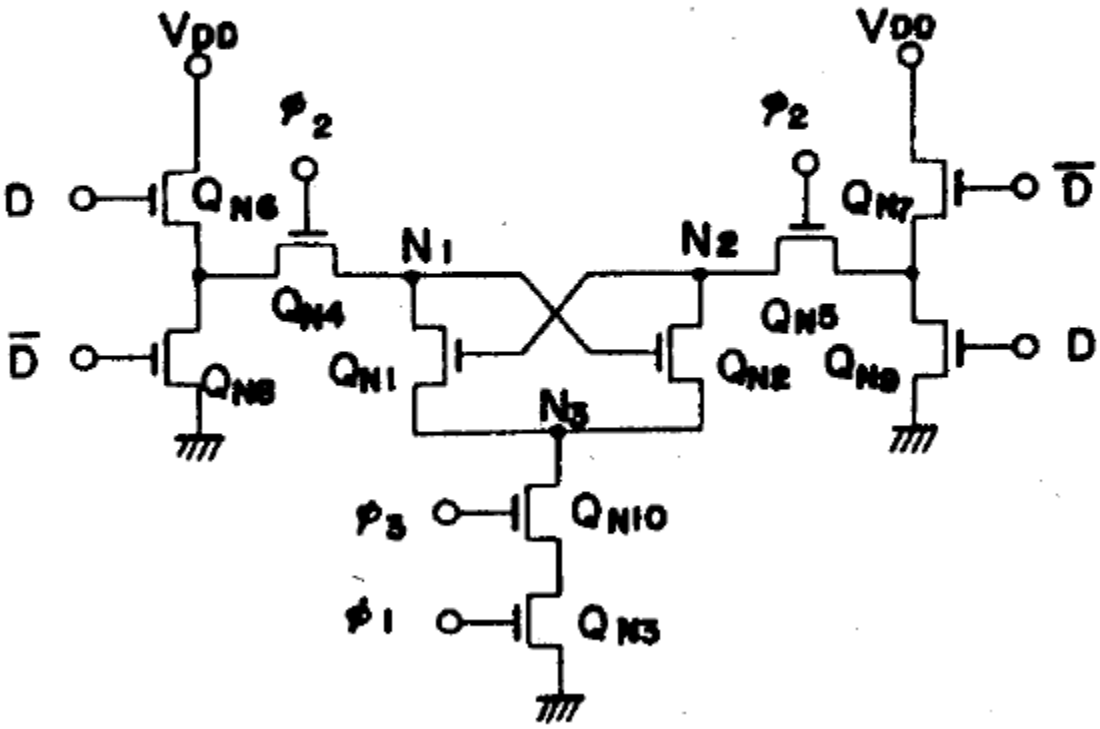
(Ex. 1002, ¶36, citing Ex. 1001, FIG. 5 (annotated); *see also* Ex. 1001, 6:5-7:13 (describing the sense amplifier of FIG. 5).)

As seen above, the latch circuit (orange) is also coupled to a pair of local data write driver transistors 128, 130 (purple) having their source-drain paths coupled in series at the left portion of figure 5, and to a similarly arranged pair of local data write driver transistors 132, 134 (purple) at the right portion of figure 5. (Ex. 1001, FIG. 5, 6:32-52, 6:66-7:13.). The pairs of local data write driver transistors are coupled to the latch by a pair of pass transistors 122 and 124 (green), which are driven by a column write select signal YW. As discussed in Section VIII, the '270 patent discloses that transistors 128, 130, 132, and 134 are associated with a single latch circuit, *i.e.*, they are "local." As discussed in detail in Section IX, these features, too, were known in the prior art. (*Id*.) (Ex. 1002, ¶37.)

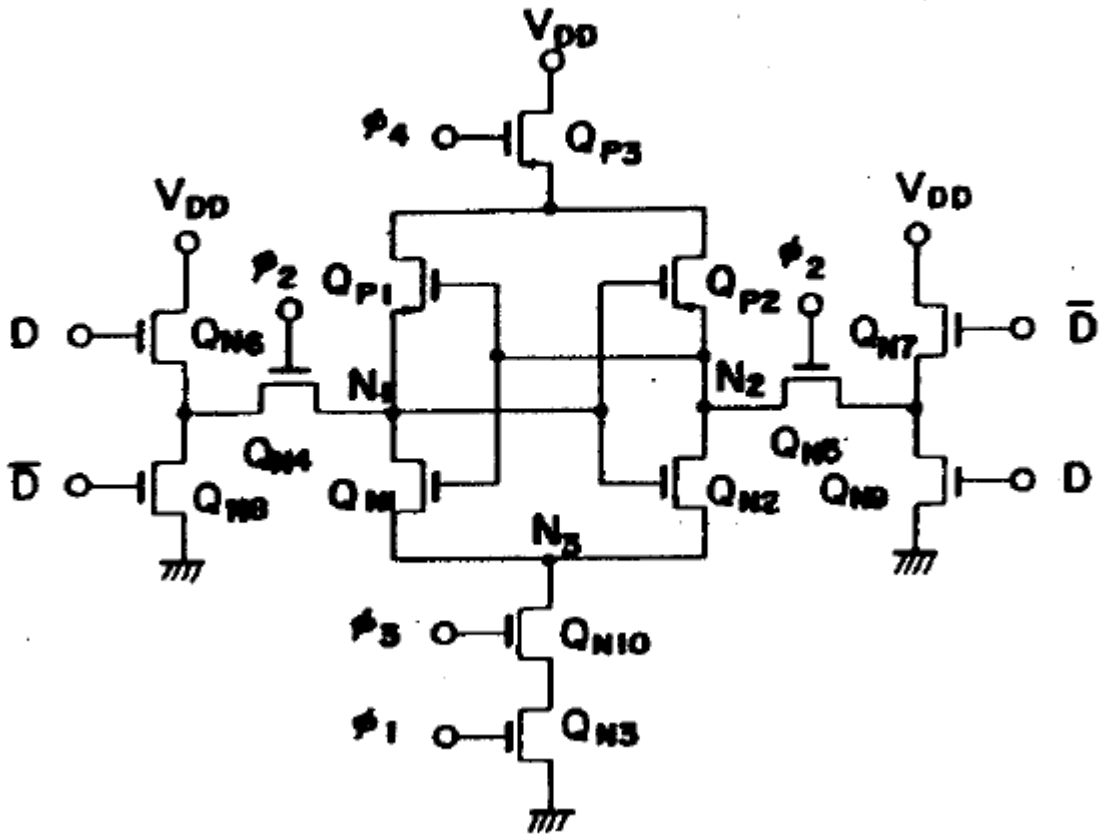
C. *Inoue*

Inoue discloses a semiconductor device including a sense amplifier with internal nodes and a flip-flop circuit capable of assuming two states (states I and II). (Ex. 1005, 1 (Claim 1), 3; Ex. 1002, ¶¶43-54.) *Inoue* discloses two configurations in figures 4 and 6 that are designed to consume a small amount of transient power when writing to a flip-flop. (Ex. 1005, 3.) (Ex. 1002, ¶43.)

第 4 図


VDD
VDD
φ2
φ2
D
D
QN6
QN7
N1
N2
QN4
QN5
QN1
QN2
QN8
QN9
N3
φ3
QN10
φ1
QN3

第 6 図



(Ex. 1005, FIGs. 4, 6[3].)

The two embodiments in figures 4 and 6 of *Inoue* build on conventional flip-flops shown in figures 1 and 3, respectively. (Ex. 1002, ¶45.)

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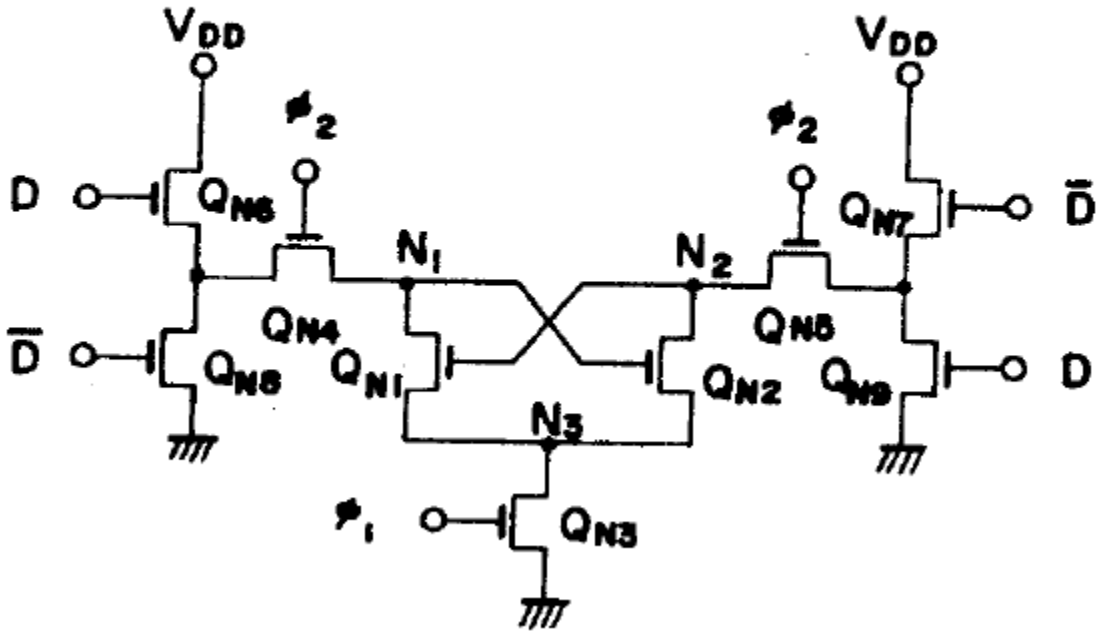
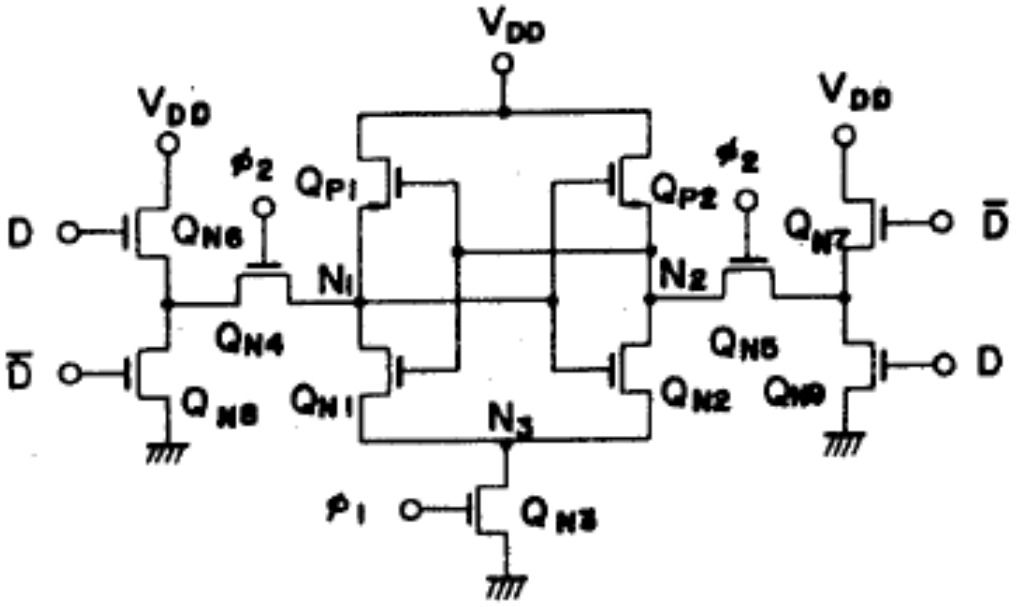
[3] In this Petition, Petitioner refers to the text of the English translation of *Inoue*, but sometimes may show figures from the Japanese version because the figures in are clearer.

第 1 図


VDD
VDD
φ2
φ2
D
QN6
QN7
D̄
N1
N2
QN4
QN5
D̄
QN8
QN1
QN2
QN9
D
N3
φ1
QN3

第 3 図


VDD
VDD
VDD
φ2
φ2
QP1
QP2
D
QN6
QN7
D̄
N1
N2
QN4
QN5
D̄
QN8
QN1
QN2
QN9
D
N3
φ1
QN3

(*Id.*, 5, FIGs. 1, 3.) (Ex. 1002, ¶45.)

Inoue's embodiment in figure 4 adds to the conventional flip-flop of FIG. 1 a transistor QN10 for pulling down node N3. (*Id.*, 4, 5, FIGS. 1, 4; Ex. 1002, ¶49.) The "embodiment [of FIG. 6] differs from FIG. 4 in the addition of a P-channel transistor QP3" which is controlled by clock ϕ_4, and also in the addition of PMOS transistors QP1 and QP2 as in the circuit of FIG. 3. (Ex. 1005, 4, 5, FIGS. 3, 4, 6; Ex. 1002, ¶52.) Much of the functionality of figure 6 is described at the portion of *Inoue* pertaining to figure 4, so *Inoue* does not repeat that description when describing FIG. 6. (*Id.*, 4 (explaining that the circuit of figure 6 "operates in a manner similar to that in FIG. 4"); Ex. 1002, ¶52.) FIG. 6 of *Inoue* differs from the circuit of FIG. 3 in the addition of pull-up transistor QP3 and pull-down transistor QN10. (Ex. 1005, 5, FIGS. 3, 6; Ex. 1002, ¶52.)

VIII. CLAIM CONSTRUCTION

The '270 patent is set to expire on July 11, 2017. Therefore, the '270 patent will expire within 18 months from entry of the notice of filing date issued in this proceeding. *See* 37 C.F.R. § 42.100(b) (Apr. 1, 2016). Accordingly, the claims of the '270 patent should be construed under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See, e.g.*, *Square Inc. v. J. Carl Cooper*, IPR2014-00156, Paper No. 38 at 7 (May 14, 2015) (citing *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)). Under *Phillips*, claim terms are given their

ordinary and customary meanings, as would be understood by a POSITA, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *See, e.g.*, *Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 20 at 2-3 (July 10, 2014). The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Any term not construed below should be interpreted in accordance with their plain and ordinary meaning.

A. "local data write driver circuit"

For purposes of this proceeding[4], the phrase "local data write driver circuit," which appears in each independent claim (claims 1, 11, and 30), should be construed as "a data write driver circuit that is associated with only one latch circuit." The intrinsic record supports adoption of Petitioner's construction. (Ex.

[4] Petitioner reserves all rights to raise claim construction and other arguments in the pending district court litigation. For example, Petitioner has not necessarily raised all challenges to the '270 patent, including challenges to the claims under 35 U.S.C. § 112, given the limitations placed by the Rules.

1002, ¶¶38-41.)

For instance, the plain language of the claims states that a pair of local data write driver circuits generate data write output signals and are coupled to ***a*** latch circuit. (Ex. 1001, 1 (Claim 1).) Moreover, throughout the specification, a local write driver circuit or its constituent components are described as being connected to, or associated with, a single latch circuit. For instance, figure 5 of the '270 patent discloses a sense amplifier 100 including data write driver circuits (transistors 128/130 and 132/134) connected to a single latch circuit (transistors 112, 114, 118, 120) of sense amplifier 100. (Ex. 1001, 6:5-13, 7:15-16; *see also id*., FIG. 5 (annotated below).)

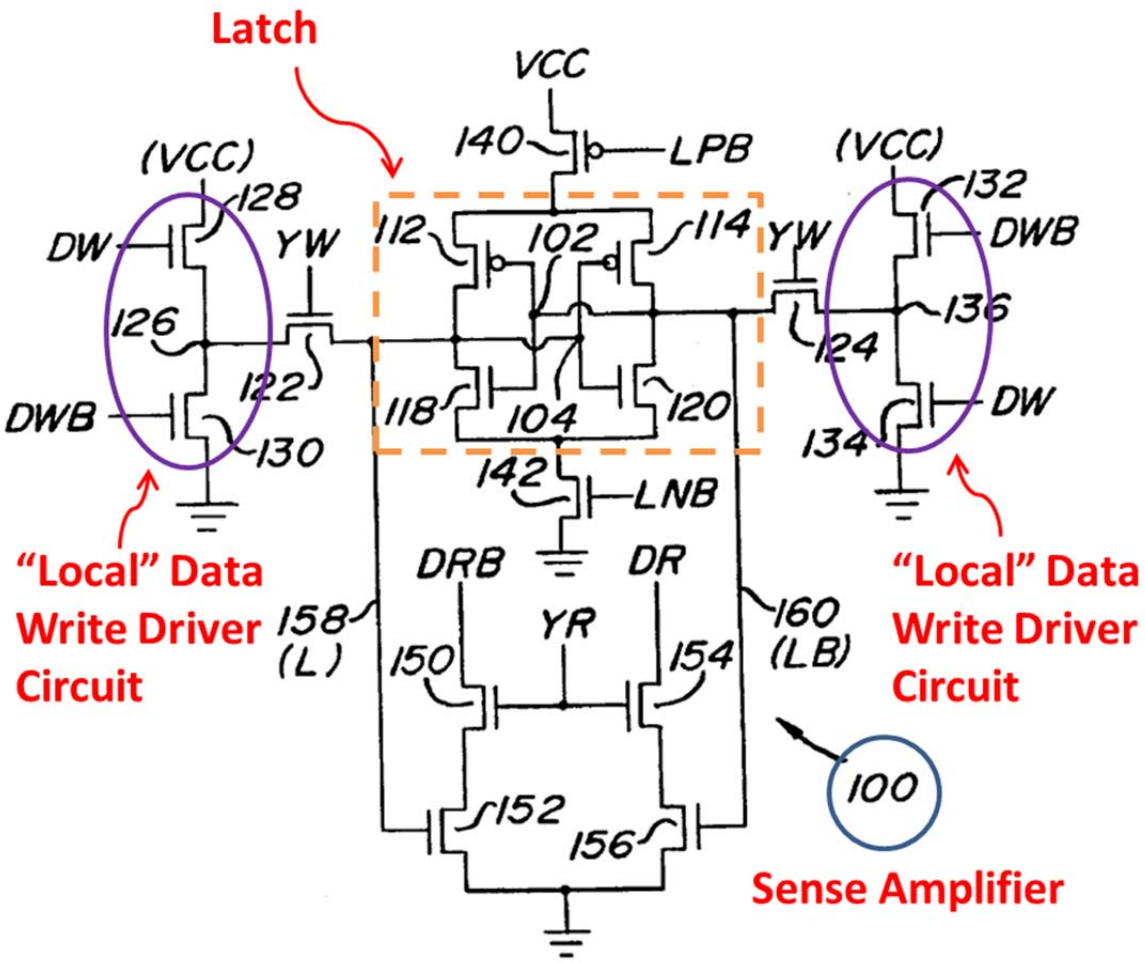


FIG. 5

(Ex. 1002, ¶41, citing Ex. 1001, FIG. 5 (annotated).)

The '270 patent also defines the term "global" as "connected to several sense amps," which suggests that "local" demotes an association with only *one* sense amplifier (and thereby, a single latch circuit). (Ex. 1001, 11:25-31 (emphasis added); Ex. 1002, ¶42.)

Because each sense amplifier includes a latch circuit (*see id.*, 1:46-62, FIGS. 1, 2) and each independent claim recites "a latch circuit," Petitioner's proposed

construction includes the phrase "only one latch circuit" rather than "only one sense amplifier" for consistency with the claim language.

The patentee unequivocally confirmed this interpretation of "local" data write driver circuits during the prosecution history of the '270 patent. For instance, patentee argued that the association with a single latch circuit defined the "local" aspect of the claimed data write circuits and cited to the above identified figure 5 of the patent. (Ex. 1003, 274.) The prosecution history of the parent application of the '270 patent is also consistent. There, the patentee clarified the difference between "local" and "global" and explained that a transistor is "local" when it associated with only *one* sense amplifier. (Ex. 1004, 166-68.)[5] *See Verizon Services Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1306 (Fed. Cir. 2007). Thus, the prosecution history is consistent with Petitioner's proposed construction above and shows a clear and intentional disavowal of claim scope regarding a data write circuit that is associated with more than one latch circuit.[6] *See Abbott*

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[5] While the statement in the prosecution history is "transistors 24 and 26 in Figs. 1-4," it is apparent that patentee was referring to transistors 44 and 46 in figures 1-4 of the parent of the '270 patent. (*See* Ex. 1005, 43, 166-68.)

[6] Patent Owner may argue against Petitioner's construction because in an *ex parte* appeal, the Board stated that "local" means something that has "a definite spatial

Laboratories v. Sandoz, Inc., 566 F.3d 1282, 1290 (Fed. Cir. 2009) (en banc).

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: *Inoue* Anticipates Claims 1-3, 8-11, 30-32, 34-36, and 38

The *Inoue* grounds in this petition focus on the disclosure of figure 6 in *Inoue*. But the disclosure of figure 6 builds on the circuits disclosed in figures 1, 3, and 4 of *Inoue*. (Ex. 1002, ¶¶43-54.) For instance, when describing figure 6, *Inoue* does not repeat details previously discussed for common aspects between figures 1, 3, 4, and 6. (*Id*.) Below, Petitioner refers to the common aspects of figures 1, 3, 4, and 6 when describing aspects of figure 6. (*See* Section VII.C.)

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form or location." (Ex. 1003, 7.) But the Board's interpretation was based on the "broadest reasonable interpretation" of "local." (*Id*.) Here, under *Phillips*, the Board should adopt Petitioner's construction, which is based on Patent Owner's characterization of its alleged invention in the specification and file history. Further, while specification discloses that the local data write driver transistors 128-134 can be shared with other column circuits (Ex. 1001, 7:55-57), the patentee's unequivocal characterization of "local" data write driver circuit during prosecution confirms the above proposed interpretation and is consistent with the specification's description of "global."

1. Claim 1

a) "A sense amplifier arrangement for an integrated circuit memory comprising"

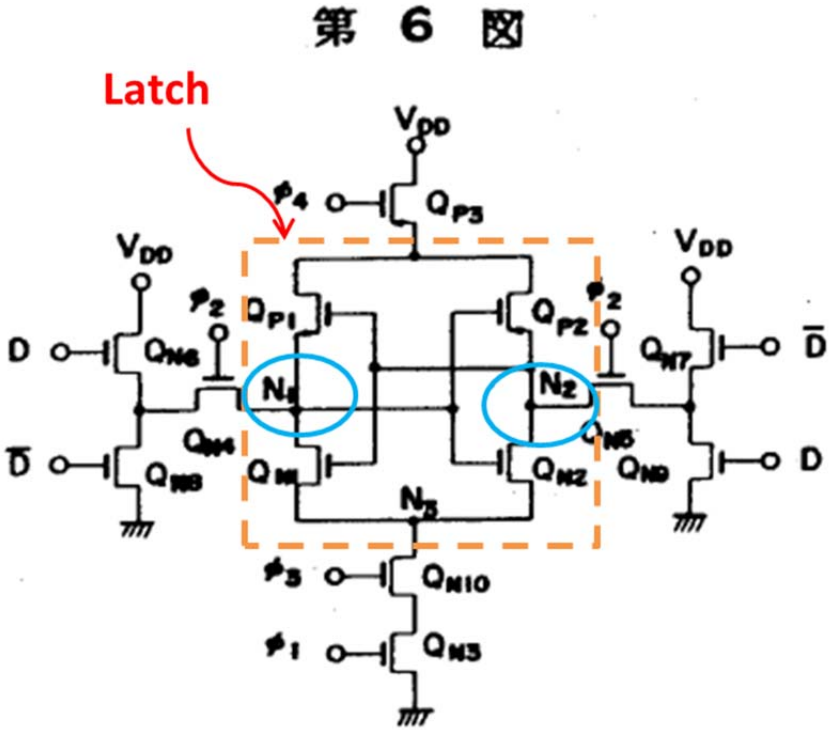
To the extent the preamble is limiting, *Inoue* discloses this feature. (Ex. 1002, ¶66.) For example, *Inoue* discloses "a semiconductor device" comprising a sense amplifier with a flip-flop circuit. (Ex. 1005, 1 (Claim 1).) The circuit in figure 6 is applicable to a sense amplifier in dynamic memory. (*See id.*, 4; *see also* Section VII.C.) A POSITA would have understood that "dynamic memory" in *Inoue* refers to a DRAM, which is an integrated circuit memory. (Ex. 1002, ¶66; *see also supra* Section VII.A; citations and analysis below for the remaining elements of this claim.)

b) "a latch circuit having internal nodes for coupling to a respective bit line pair"

Inoue discloses this feature. (Ex. 1002, ¶¶67-70.) For example, *Inoue* discloses a CMOS flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} which is a "latch circuit" having internal nodes $N_1$and N_2 that couple to a respective bit line pair N_1 and N_2. (Ex. 1005, FIG. 6; *id*., 3, 4.)

As discussed above, the circuit of figure 6 in *Inoue* builds on the circuits disclosed in figures 1, 3 and 4 of *Inoue*. (Ex. 1002, ¶¶43-54, 67-68.) *Inoue* discloses that PMOS or P-Channel transistors Q_{P1}, Q_{P2}, and NMOS or N-Channel transistors Q_{N1}, Q_{N2} form a flip-flop ("latch circuit"). (Ex. 1005, 3.) A flip-flop is a "latch circuit" as acknowledged by the '270 patent and as would be readily

understood by a POSITA. (Ex. 1002, ¶¶68-70, Ex. 1001, 1:58-62, 2:6-14, 6:5-13, FIGS. 1, 5.) Figure 6 discloses that the Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} flip-flop has nodes N_1 and N_2 where when applied to a sense amp in the memory, "*N_1 and N_2 correspond to bit lines*." (Ex. 1005, 4 (emphasis added).)



(Ex. 1002, ¶69, citing Ex. 1005, FIG. 6 (annotated to show internal nodes (blue) of the latch circuit (orange).)

The '270 patent discloses an identical configuration and states that "transistors 112, 114, 118, and 120" form a "latch" (Ex. 1001, 6:5-8), where the internal nodes in *Inoue* (blue above) are similar to the internal nodes in figure 5 of the '270 patent (blue below).

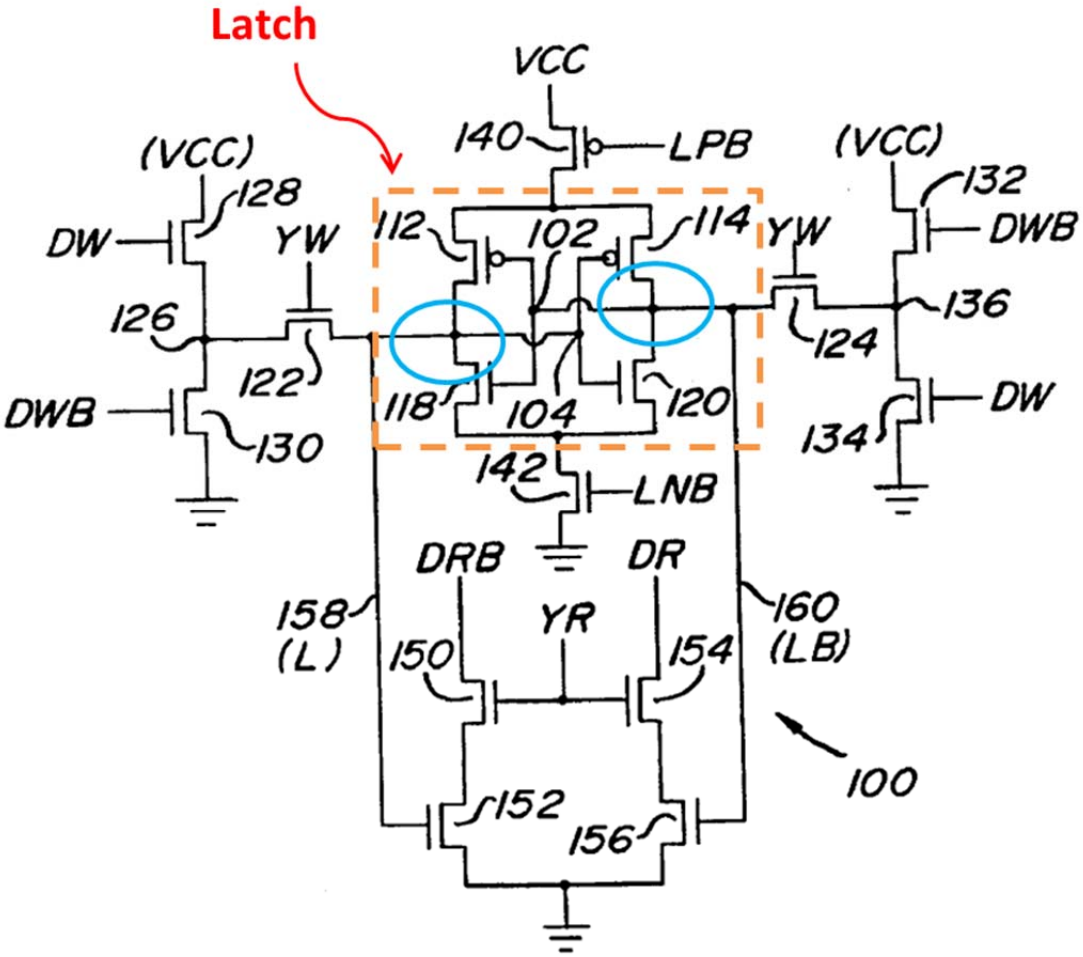


FIG. 5

(Ex. 1002, ¶70, citing Ex. 1001, FIG. 5 (annotated).) (Section VII.B.)

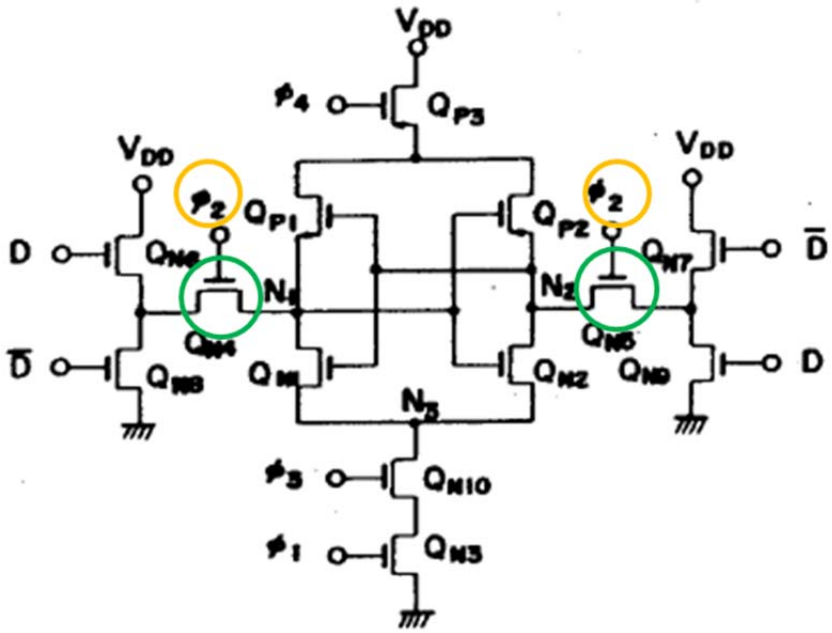
c) "a pair of pass transistors each coupled to a respective one of said internal nodes, the pass transistors having a control electrode coupled to receive a first control signal;"

Inoue discloses this feature. (Ex. 1002, ¶¶71-73.) *Inoue* discloses transistors Q_{N4} and Q_{N5} ("a pair of pass transistors") each coupled to respective one of N_1 or N_2 ("a respective one of said internal nodes"), Q_{N4} and Q_{N5} ("the pair of

pass transistors") having a gate terminal ("a control electrode") coupled to receive write control clock ϕ_2 ("a first control signal").

A POSITA would have understood that transistors Q_{N4} and Q_{N5} are "pass transistors" and are "coupled" to nodes N_1 and N_2, respectively, because, for example, when conductive they allow current to flow into and out of nodes N_1 and N_2. (Ex. 1005, 3, "when clock ϕ_2 rises, Q_{N4} becomes conducting, and the current flows from V_{DD} to the node N_1 through Q_{N6} and Q_{N4}, while the current flows out from N_2 to GND through Q_{N5} and Q_{N9}.") *Inoue* discloses that clock ϕ_2 controls the conductivity of Q_{N4} and Q_{N5} and is therefore, a "first control signal." (*Id.*, 3, "clock ϕ_2 is allowed to rise, thereby causing Q_{N4} and Q_{N5} to be conducting.") Finally, as seen from figure 6, clock ϕ_2 is provided to the gate terminal ("control electrode") of Q_{N4} and Q_{N5}. (*Id.*, FIG. 6.)

第 6 図



(Ex. 1002, ¶72, citing Ex. 1005, FIG. 6 (annotated to show a pair of pass transistors in green, with control electrodes of such transistors in orange).)

The ’270 patent discloses an identical configuration, where the pass transistors in *Inoue* (green above) correspond to the “pass transistors 122, 124” in figure 5 of the ’270 patent (green below) that receive column write signal YW (orange below). (*Id.*; Ex. 1001, 6:14-15, FIG. 5.)

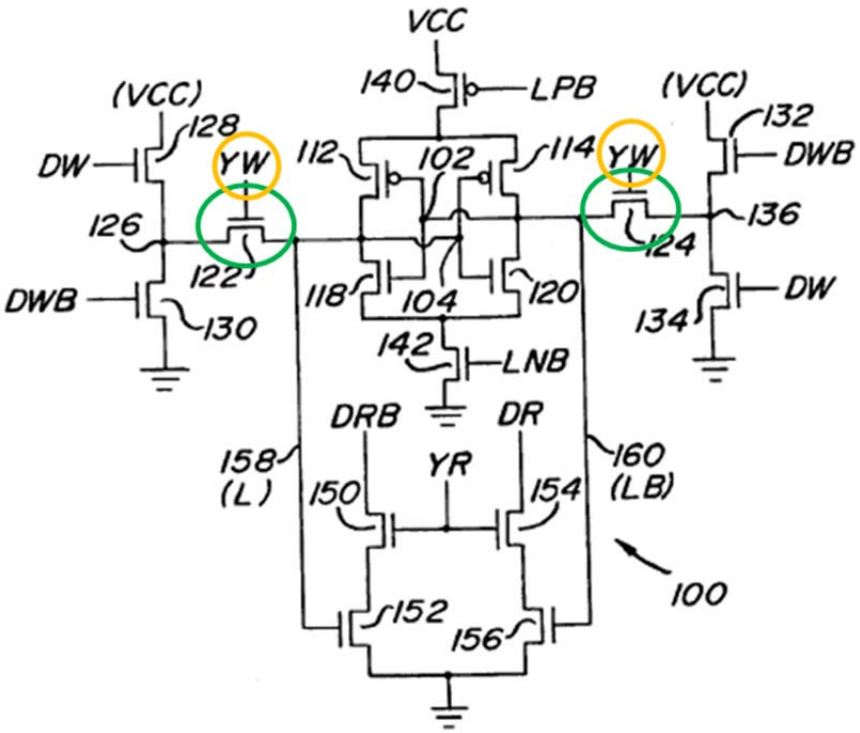


FIG. 5

(Ex. 1002, ¶73, citing Ex. 1001, FIG 5 (annotated).) (Section VII.B.)

d) "a pair of local data write driver circuits having respective control electrodes coupled to receive second write control signals for data write operations and to provide a pair of data write output signals"

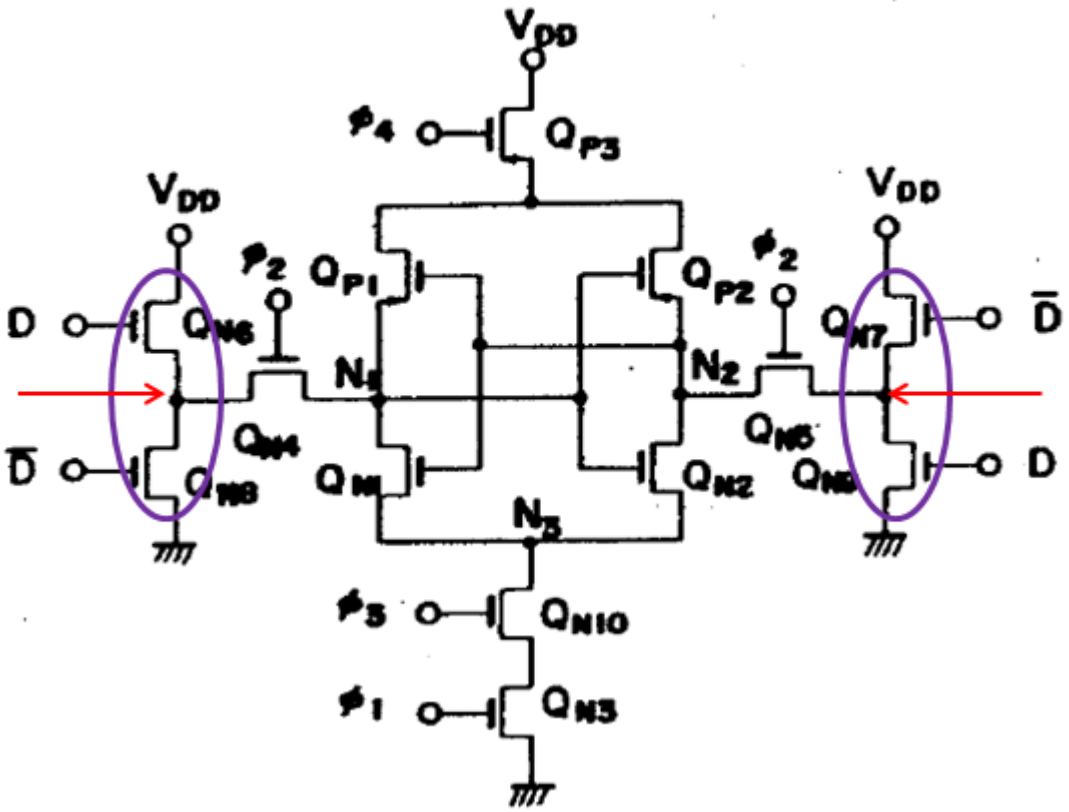
Inoue discloses this feature. (Ex. 1002, ¶¶74-77.) *Inoue* discloses two data write circuits: Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} ("a pair of local data write driver circuits") that are associated with only a single latch circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}). The gates ("control electrodes") of Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} are coupled to receive the signals at write data input terminals D and $\overline{D}$ ("second write control

signals") that write to nodes N_1 and N_2 ("receive second write control signals for data write operations and to provide a pair of data write output signals").

For instance, *Inoue* discloses that "D, $\overline{D}$ [are] write data input terminals used to write data to F/F" where F/F refers to a flip-flop. (Ex. 1005, 3.) Signals at terminals D and $\overline{D}$ are "second write control signals for data write operations." Terminal D is the gate terminal of Q_{N6} and Q_{N9}, and terminal $\overline{D}$ is the gate terminal of Q_{N8} and Q_{N7}. (*Id.*, Fig. 6.) Thus, Q_{N6}, $Q_{N8,}$ Q_{N7} and Q_{N9} have "respective control electrodes coupled to receive second write control signals for data write operations," as claimed. (Ex. 1002, ¶75.)

Inoue discloses that "Q_{N5}, Q_{N7}, Q_{N9} and Q_{N4}, Q_{N6}, Q_{N8} are write circuits that determine the state of the F/F." (*Id.*, 3, FIG. 6.) As seen from figure 6, Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} are associated with only a single latch circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}). (*Id.*, FIG. 6; *see also* analysis above in Section IX.A.1.b ("latch circuit" in *Inoue*).) Therefore, Q_{N6}, $Q_{N8,}$ and $Q_{N7,}$ Q_{N9} constitute "a pair of local data write driver circuits." (Ex. 1002, ¶76; *see also* Section VIII.) The output of the write circuits, as shown by a red arrow below, constitutes a "data write output signal" because it is the output of the data write circuits. Therefore, Q_{N6}, $Q_{N8,}$ and $Q_{N7,}$ Q_{N9} "provide a pair of data write output signals."

第 6 図



(Ex. 1002, ¶76, citing Ex. 1005, FIG. 6 (annotated to show local data write driver circuits (purple) and an output (red arrow).)

The ’270 patent discloses the same configuration:

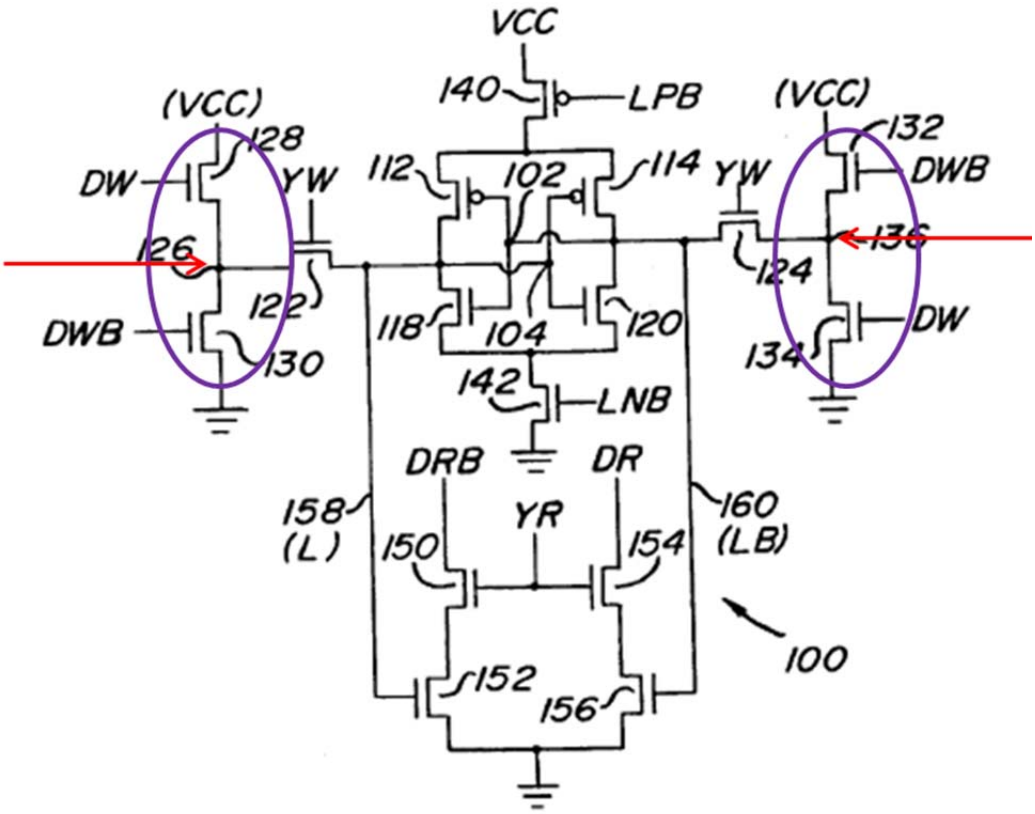


FIG. 5

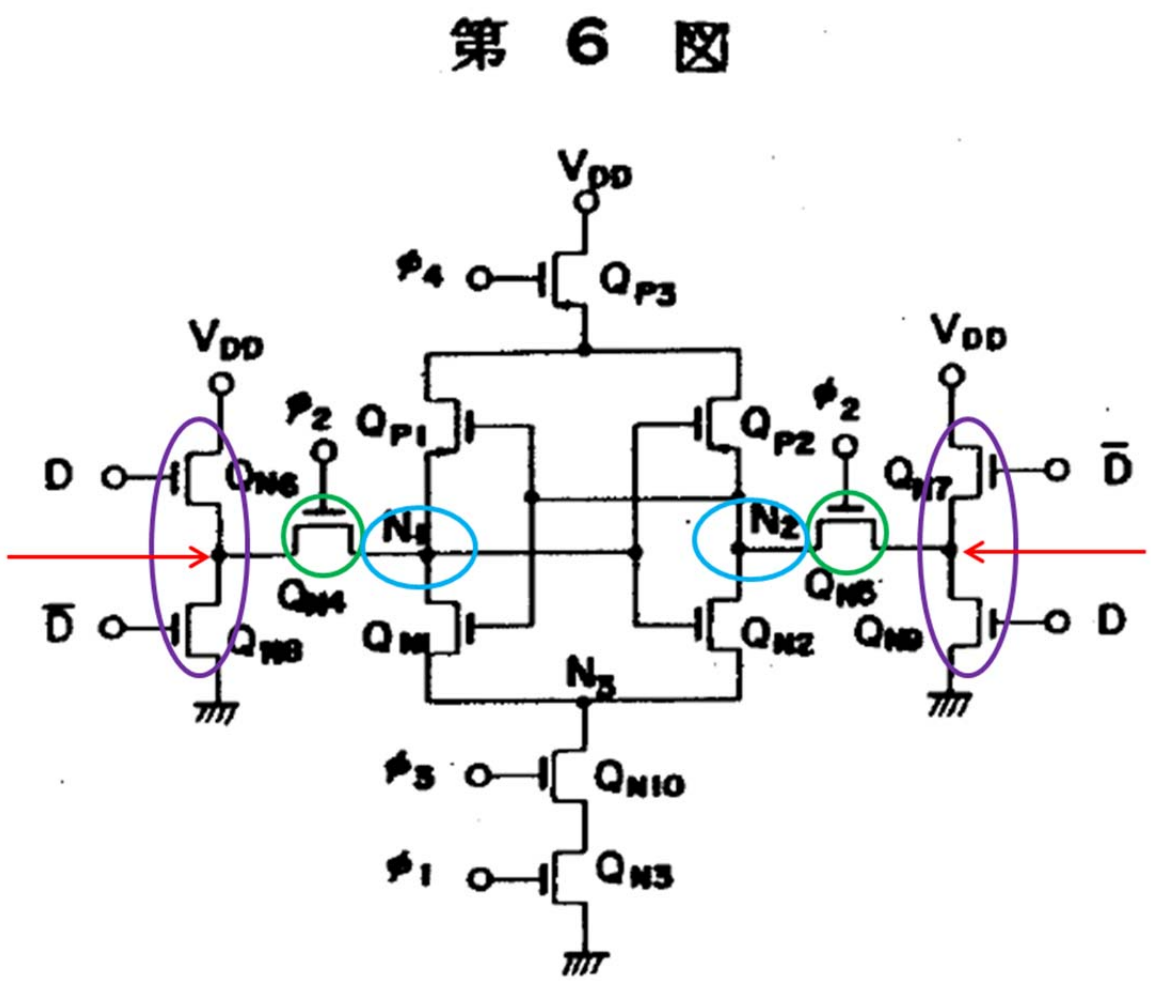
(Ex. 1002, ¶77, citing Ex. 1001, FIG. 5 (annotated).) (Section VII.B.)

e) "each local data write driver circuit being coupled to its corresponding pass transistor so that the pass transistor, when conductive, couples one of said output signals from the local data write driver circuit to the corresponding internal node of the latch circuit and to a corresponding bit line."

Inoue discloses this feature. (Ex. 1002, ¶¶78-81.) *Inoue* discloses that Q_{N6}/Q_{N8}[7] and Q_{N7}/Q_{N9} ("each local data write driver circuit") are coupled to Q_{N4} and $Q_{N5,}$ respectively ("its corresponding pass transistor"), so that Q_{N4} or Q_{N5} when conductive, couples the output signal from Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} to N_1 or N_2 ("the corresponding internal node of the latch circuit and to a corresponding bit line").

As seen from figure 6 (annotated below), Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("each local data write driver circuit") are coupled to Q_{N4} and $Q_{N5,}$ respectively ("its corresponding pass transistor").

[7] Q_{N6}/Q_{N8} refers to the combination of Q_{N6} and Q_{N8} and Q_{N7}/Q_{N9} refers to the combination of Q_{N7} and Q_{N9}.



(Ex. 1002, ¶79, citing Ex. 1005, FIG. 6 (annotated to show the output (red arrow) of local data write driver circuits (purple) are connected to respective nodes N1, N2 (blue) through corresponding pass transistors (green).)

Inoue discloses that when clock ϕ_2 rises, Q_{N4} and Q_{N5} become conducting. (Ex. 1005, 3.) As a result, "the current flows from V_{DD} to the node N_1 through Q_{N6} and Q_{N4}, while the current flows out from N_2 to GND through Q_{N5} and Q_{N9}" thereby charging node N1 to a level "H" (V_{DD}) and discharging node N2 to "L" (GND). (*Id.*, 3.) Therefore, the output (V_{DD}) of Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} (GND) is

provided to nodes N_1 and N_2, which, as discussed above with respect to claim element 1.b, correspond to bit lines. (*See supra* Section IX.A.1.b.) That is, *Inoue* discloses this claim element.

The '270 patent discloses the same configuration:

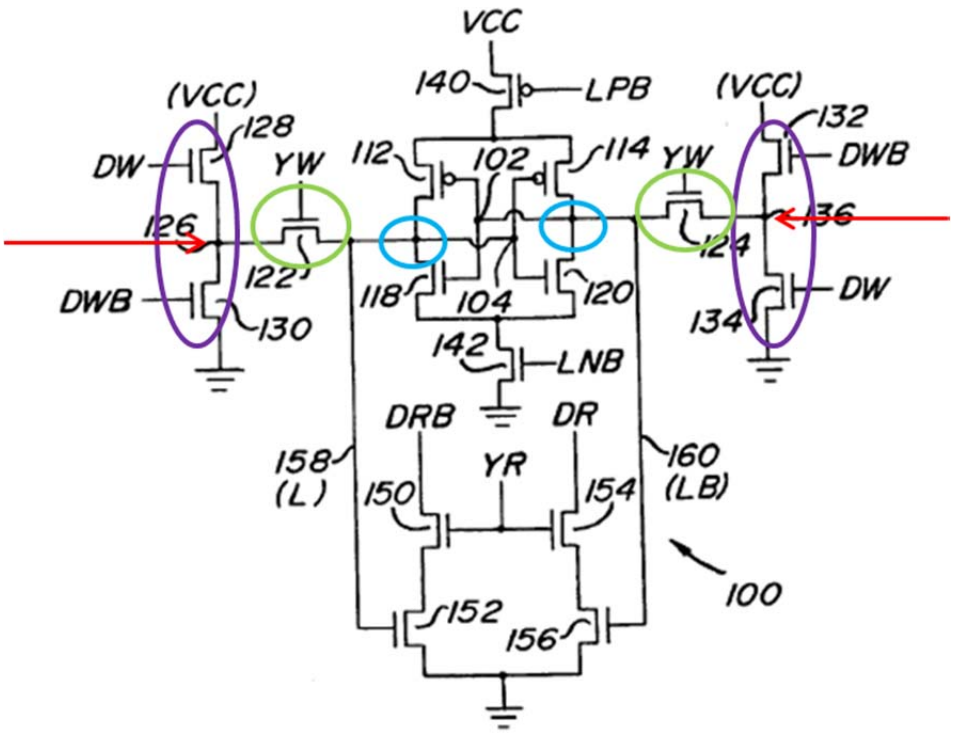


FIG. 5

(Ex. 1002, ¶¶80-81, citing Ex. 1001, FIG. 5 (annotated with write driver circuits in purple, their outputs in red, internal nodes of the latch circuit in blue, and pass transistors in green).) (*See also* Section VII.B.)

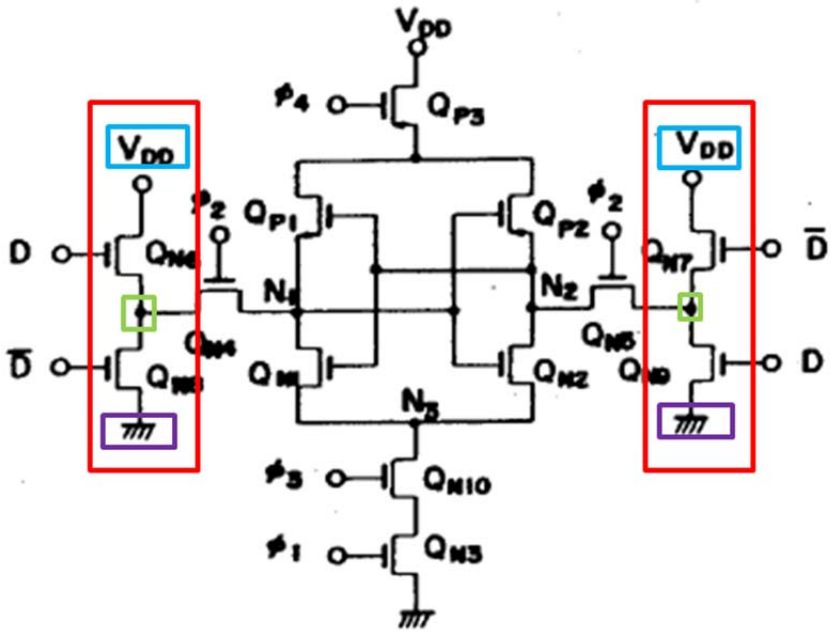
2. Claim 2

a) "The sense amplifier arrangement according to claim 1 wherein each of said local data write driver circuits

> comprises a pull-up transistor and a pull-down transistor having their source-drain paths coupled in series and forming an output node therebetween, said output node being coupled to the corresponding pass transistor, said source-drain paths being coupled between first and second voltages."

Inoue discloses this feature. (Ex. 1002, ¶¶82-84.) *Inoue* discloses write circuits Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("each of said local data write driver circuits"), each of which is comprised by Q_{N6} or Q_{N7} ("a pull-up transistor") and Q_{N8} or Q_{N9} ("a pull-down transistor") having their source-drain paths coupled in series (red below) and forming an output node therebetween (green below), said output node being coupled to the corresponding pass transistor Q_{N4} or Q_{N5}, said source-drain paths being coupled between V_{DD} (blue below) and GND (purple below) ("first and second voltages").

第 6 図



(Ex. 1002, ¶82, citing Ex. 1005, FIG. 6 (annotated).)

A POSITA would have understood that Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} have their source-drain paths connected in series just like the source-drain paths are connected in series for transistors 128 and 130 in the '270 patent. (Ex. 1002, ¶83, citing Ex. 1001, 6:35-36.) A POSITA would have also understood that Q_{N6} and Q_{N7} are "pull-up" transistors because when conductive they pull the voltage of the output node (annotated in green) to V_{DD}. (*Id.*; *see also* Ex. 1005, 3.) A POSITA would have also understood that Q_{N8} and Q_{N9} are "pull-down" transistors because when conductive they pull the voltage of the output node (annotated in green) to GND. (Ex. 1002, ¶83.)

The '270 patent discloses the same configuration:

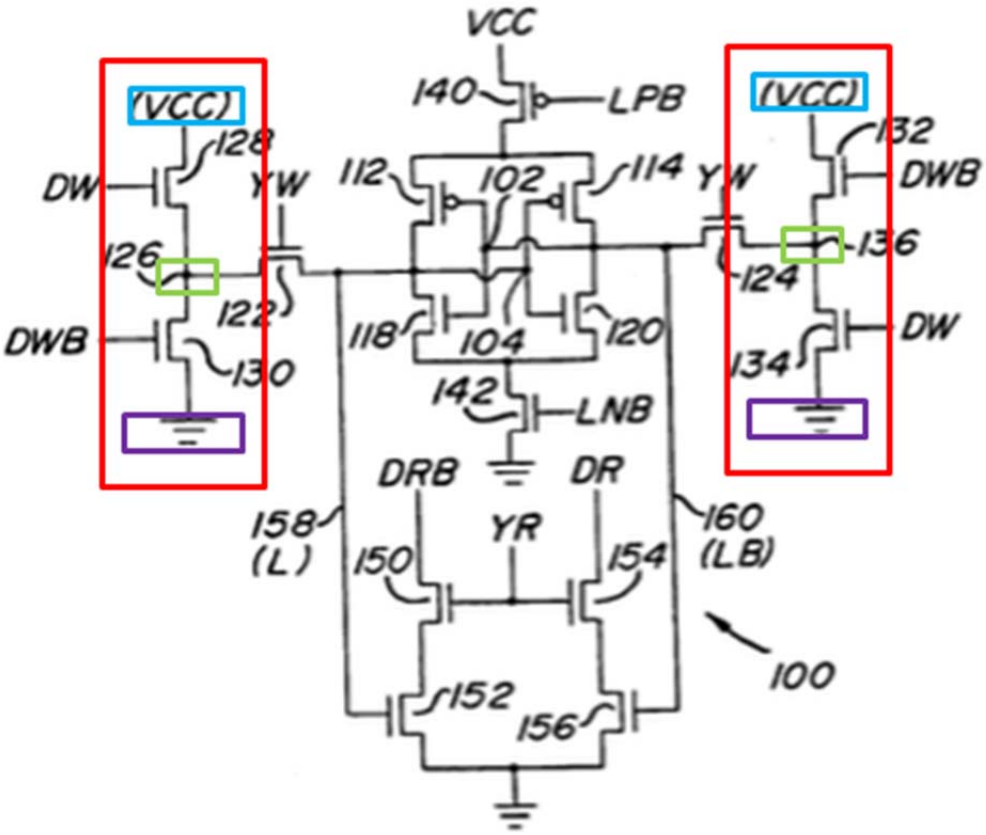


FIG. 5

(Ex. 1002, ¶84, citing Ex. 1001, FIG. 5 (annotated).) (*See also* Section VII.B.)

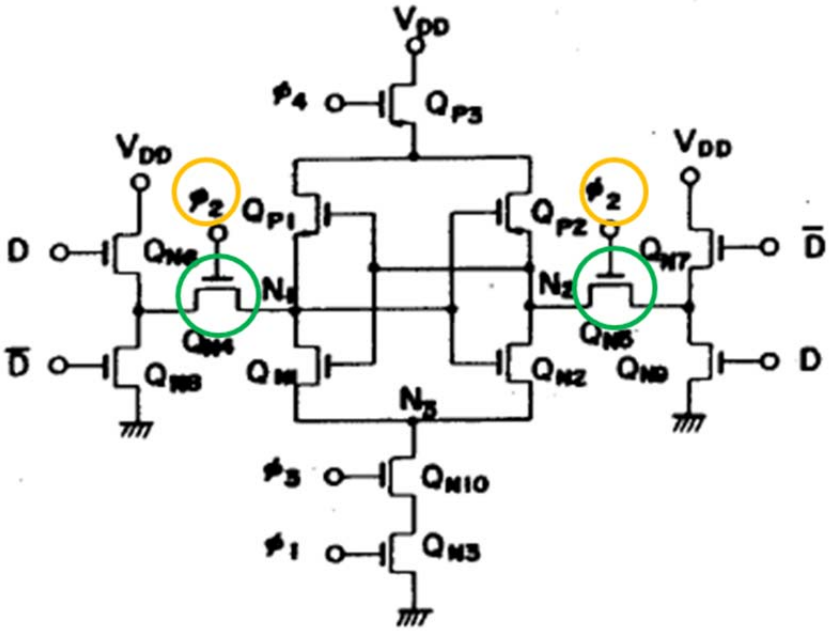
3. Claim 3

a) "The sense amplifier arrangement according to claim 2 wherein said first control signal is a write control signal, and wherein said pass transistor is connected to receive said write control signal at its control electrode."

Inoue discloses this feature. (Ex. 1002, ¶¶85-86.) *Inoue* discloses that ϕ_2 ("first control signal") (orange below) is a write control clock ("a write control

signal") and that Q_{N4} or Q_{N5} ("said pass transistor") (green below) is connected to receive this write control signal at its gate terminal ("control electrode"). For example, *Inoue* discloses that "ϕ_2 [is] a write control clock," and that "when terminals D and $\overline{D}$ write to the nodes N_1 and N_2 . . . clock ϕ_2 is allowed to rise, thereby causing Q_{N4} and Q_{N5} to be conducting." (Ex. 1005, 4.) As noted above, because clock ϕ_2 controls the conductivity of Q_{N4} and Q_{N5}, it is a "first control signal."

第 6 図



(Ex. 1002, ¶85, citing Ex. 1005, FIG. 6 (annotated).) The '270 patent discloses the same configuration:

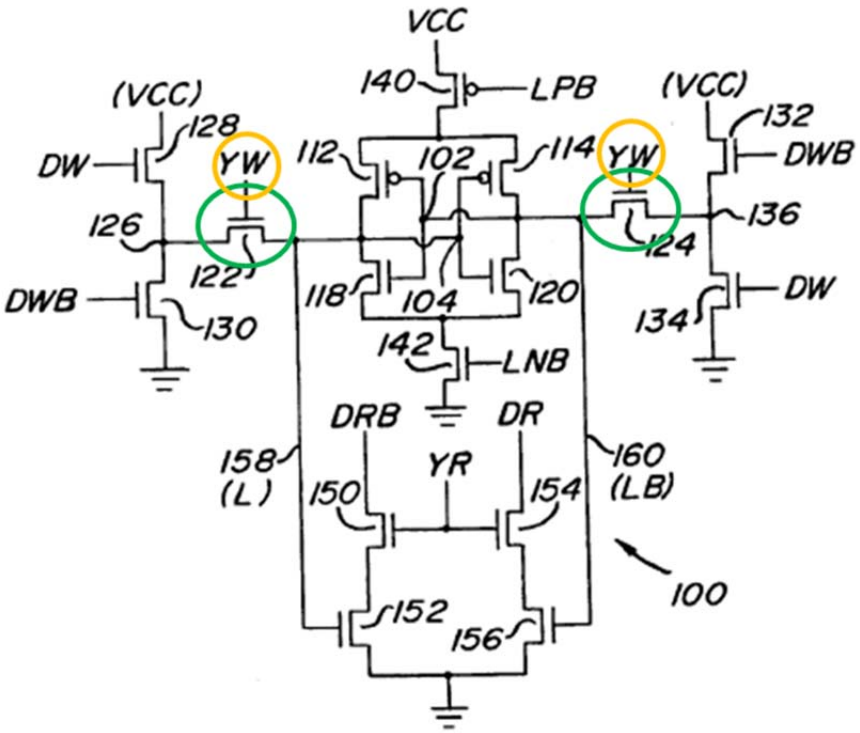


FIG. 5

(Ex. 1002, ¶86, citing Ex. 1001, FIG. 5 (annotated).) (*See also* Section VII.B.)

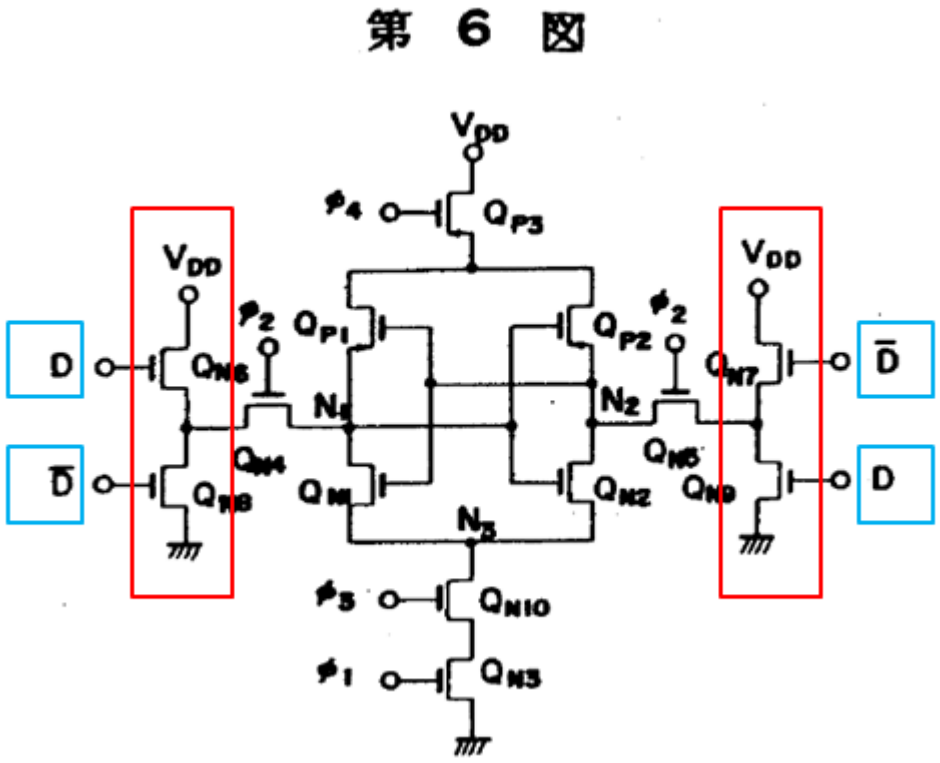
4. Claim 8

a) "The sense amplifier arrangement according to claim 2 wherein said local data write driver circuits receive said second write control signals at control terminals of said pull-up and pull-down transistors."

Inoue discloses this feature. (Ex. 1002, ¶¶87-89.) *Inoue* discloses that Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("said local data write driver circuits") receive write signals D and $\overline{D}$ ("said second write control signals") at the gates ("control terminals") of Q_{N6} or Q_{N7} ("said pull-up transistors") and Q_{N8} or Q_{N9} ("said pull-down transistors"). The gates of Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} are shown to directly receive write control

signals D and $\overline{D}$ ("second write control signals"). (Ex. 1005, FIG. 6; Ex. 1002, ¶87.)

As shown below, the local data write driver circuits (red) receive the second write control signals (blue) at control terminals (gates) of the pull-up (Q_{N6}/ Q_{N8}) and pull-down transistor pairs (Q_{N6}/ Q_{N8}).



(Ex. 1002, ¶88, citing Ex. 1005, FIG. 6 (annotated).)

The '270 patent discloses the same configuration:

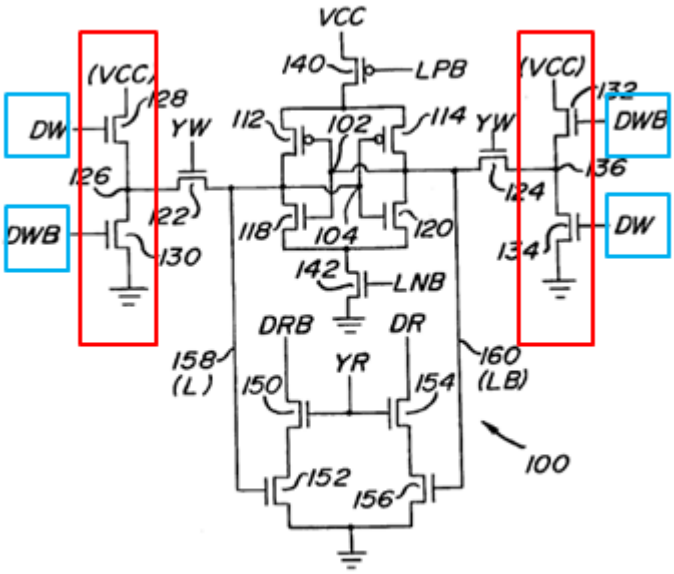


FIG. 5

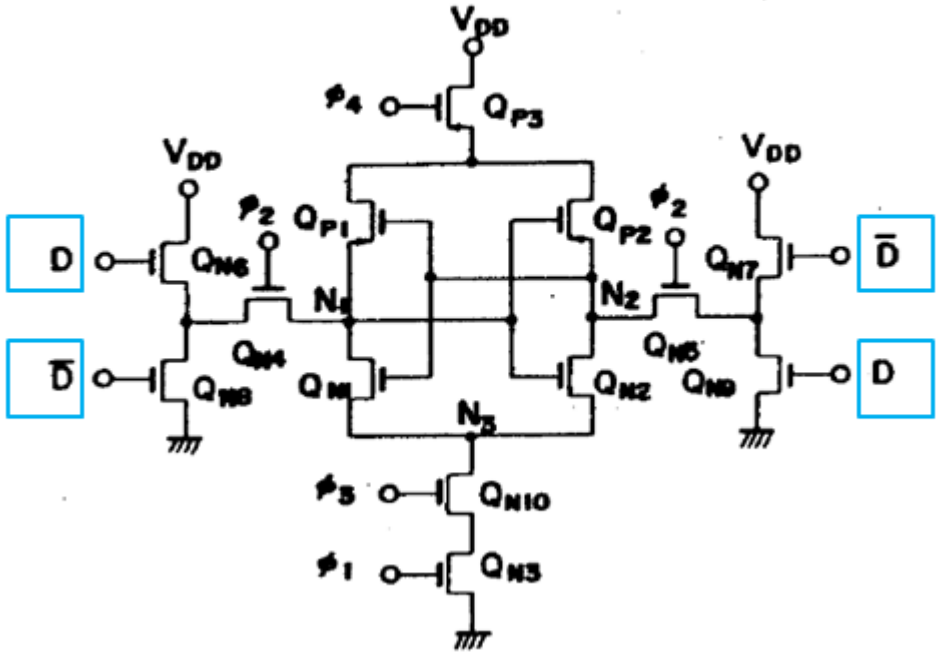
(Ex. 1002, ¶89, citing Ex. 1001, FIG. 5 (annotated).)

5. Claim 9

a) "The sense amplifier arrangement according to claim 8 wherein said second write control signals comprise first and second data write signals; and"

Inoue discloses this feature. (Ex. 1002, ¶¶90-91.) *Inoue* discloses that the signals D, $\overline{D}$ ("said second write control signals") comprise a signal at write data input terminal D ("first . . . data write signal[]") and a signal at write data input terminal $\overline{D}$ ("second data write signal[]"). (Ex. 1005, FIG. 6.)

第 6 図



(Ex. 1002, ¶90, citing Ex. 1005, FIG. 6 (annotated to show that the second write control signals (blue) include first and second data write signals at D, $\overline{D}$, respectively).)

The ’270 patent discloses the same configuration:

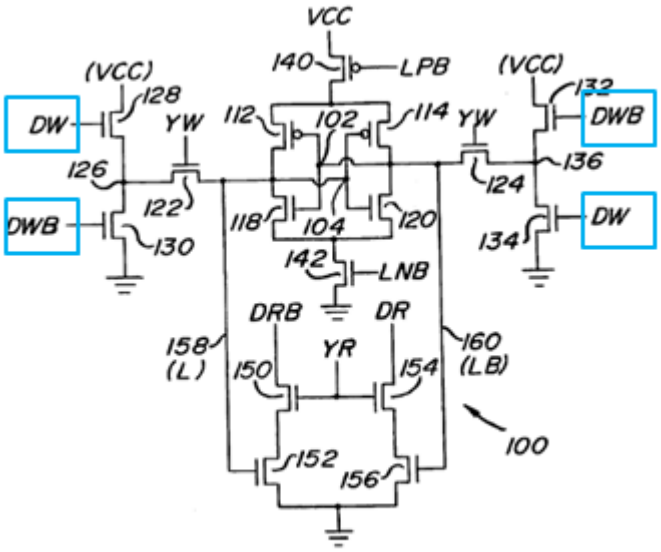


FIG. 5

(Ex. 1002, ¶91, citing Ex. 1001, FIG. 5.)

b) "wherein one said pull-up transistor in the local data write driver circuits for the corresponding latch circuit receives the first data write signal and the other said pull-up transistor receives the second data write signal."

Inoue discloses this feature. (Ex. 1002, ¶92.) *Inoue* discloses that Q_{N6} ("one said pull-up transistor in the local data write driver circuits for the corresponding latch circuit") receives the signal at terminal D ("the first data write signal") and Q_{N7} ("the other said pull-up transistor") receives the signal at terminal $\overline{D}$ ("second data write signal"). (Ex. 1005, FIG. 6; Ex. 1002, ¶¶24-30.)

6. Claim 10

a) "The sense amplifier arrangement according to claim 9 wherein one said pull-down transistor in the local data write driver circuits for the corresponding latch circuit receives the first data write signal and the other said pull-down transistor receives the second data write signal."

Inoue discloses this feature. *Inoue* discloses that Q_{N9} ("one said pull-down transistor in the local data write driver circuits for the corresponding latch circuit") receives D ("the first data write signal") and Q_{N8} ("the other said pull-down transistor") receives $\overline{D}$ ("second data write signal"). (Ex. 1005, FIG. 6; ; Ex. 1002, ¶¶93, 24-30.)

7. Claim 11

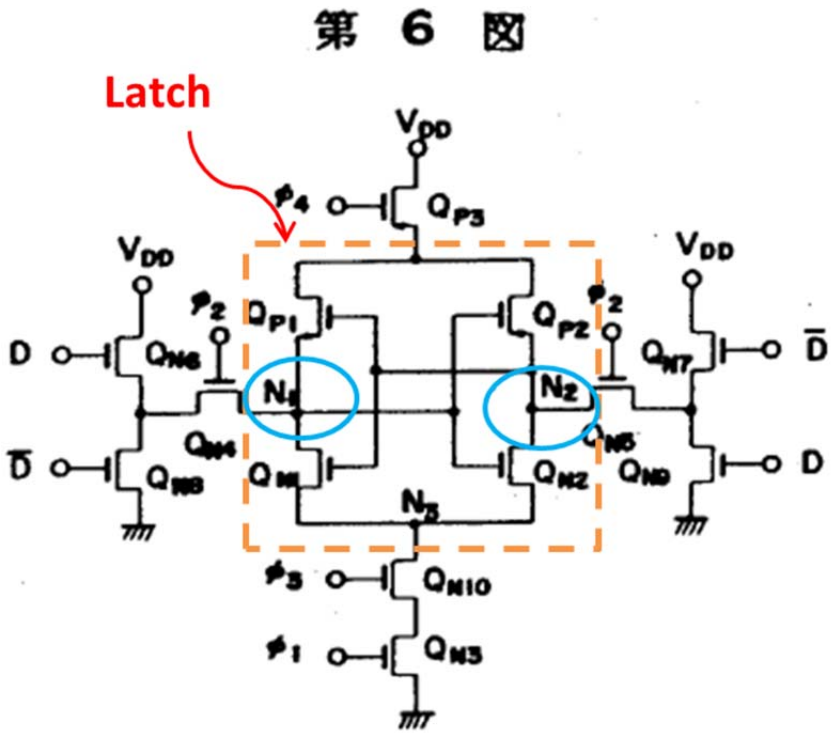
a) "A sense amplifier arrangement for an integrated circuit memory comprising:"

To the extent the preamble is limiting, *Inoue* discloses this feature for reasons discussed above for claim element 1(a). (Ex. 1002, ¶94; Section IX.A.1(a).)

b) "a latch circuit coupled directly or indirectly to a pair of corresponding bit lines;"

Inoue discloses this feature. (Ex. 1002, ¶¶95-96.) As discussed above for claim element 1(b), transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} constitute a "latch circuit" having internal nodes N_1 and N_2 that couple to a respective bit line pair. For instance, *Inoue* discloses that in the FIG. 6 configuration "nodes N_1 and N_2" may correspond

to bit lines. (Ex. 1005, 4; *see also id.*, FIG. 6 (annotated below); *see* Section IX.A.1(b).)



(Ex. 1002, ¶95, citing Ex. 1005, FIG. 6 (annotated to show internal nodes (blue) of the latch circuit (orange).)

The ’270 patent discloses the same configuration:

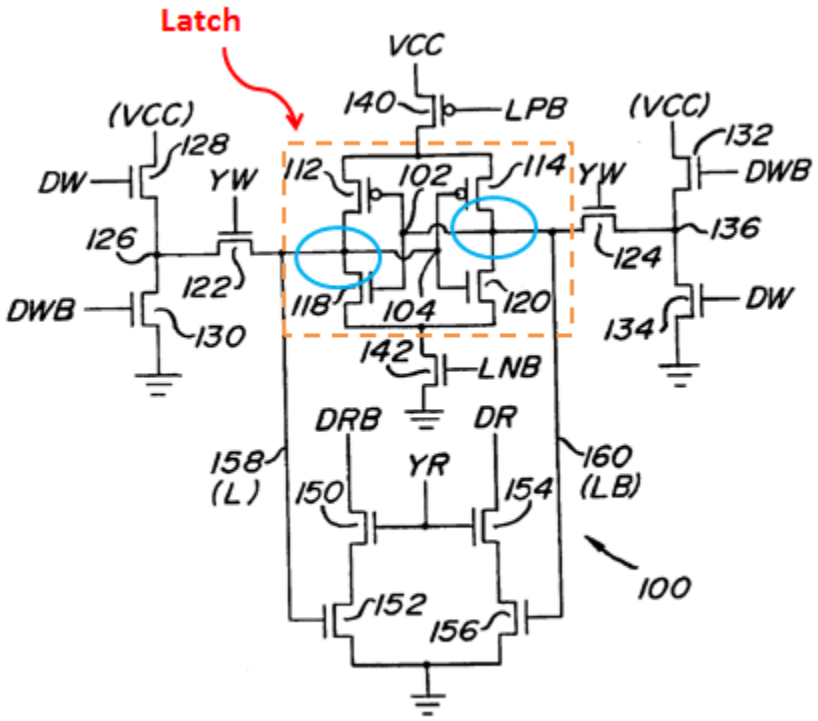


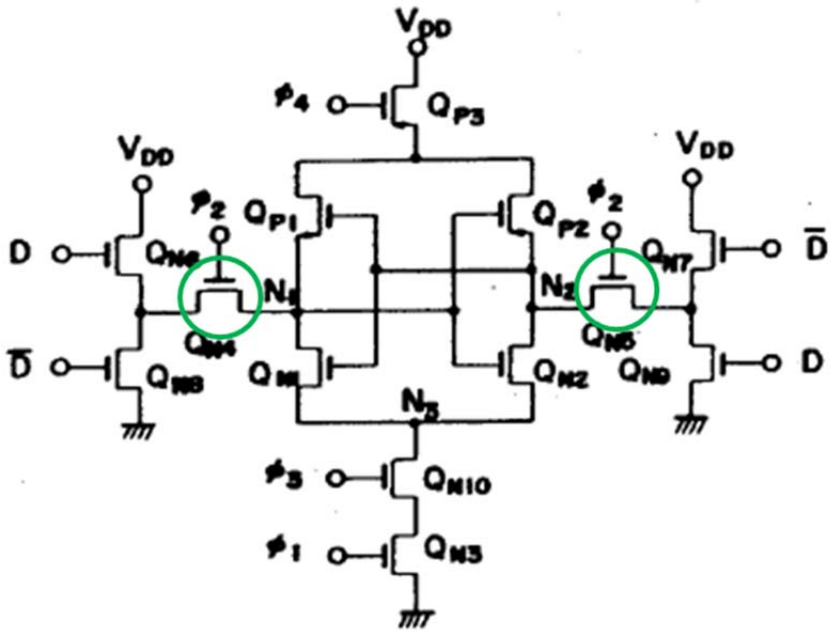
FIG. 5

(Ex. 1002, ¶96, citing Ex. 1001, FIG. 5 (annotated).)

c) "first and second pass transistors"

Inoue discloses this feature. (Ex. 1002, ¶¶97-98.) As discussed above for claim element 1(c), *Inoue* discloses Q_{N4} ("first") and Q_{N5} ("second") pass transistors. (Ex. 1005, 3, 4; *see also id.*, FIG. 6; Section IX.A.1(c).)

第 6 図



(Ex. 1002, ¶97, citing Ex. 1005, FIG. 6 (annotated to show first and second pass transistors (green).)

The ’270 patent discloses the same configuration:

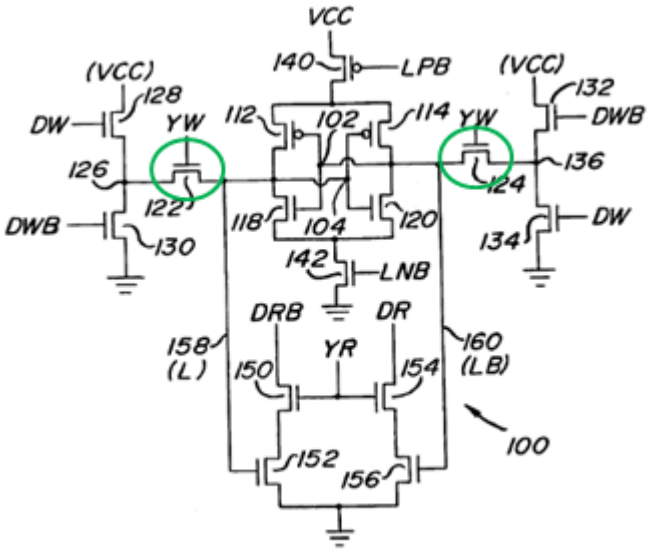


FIG. 5

(Ex. 1002, ¶98, citing Ex. 1001, FIG. 5 (annotated).)

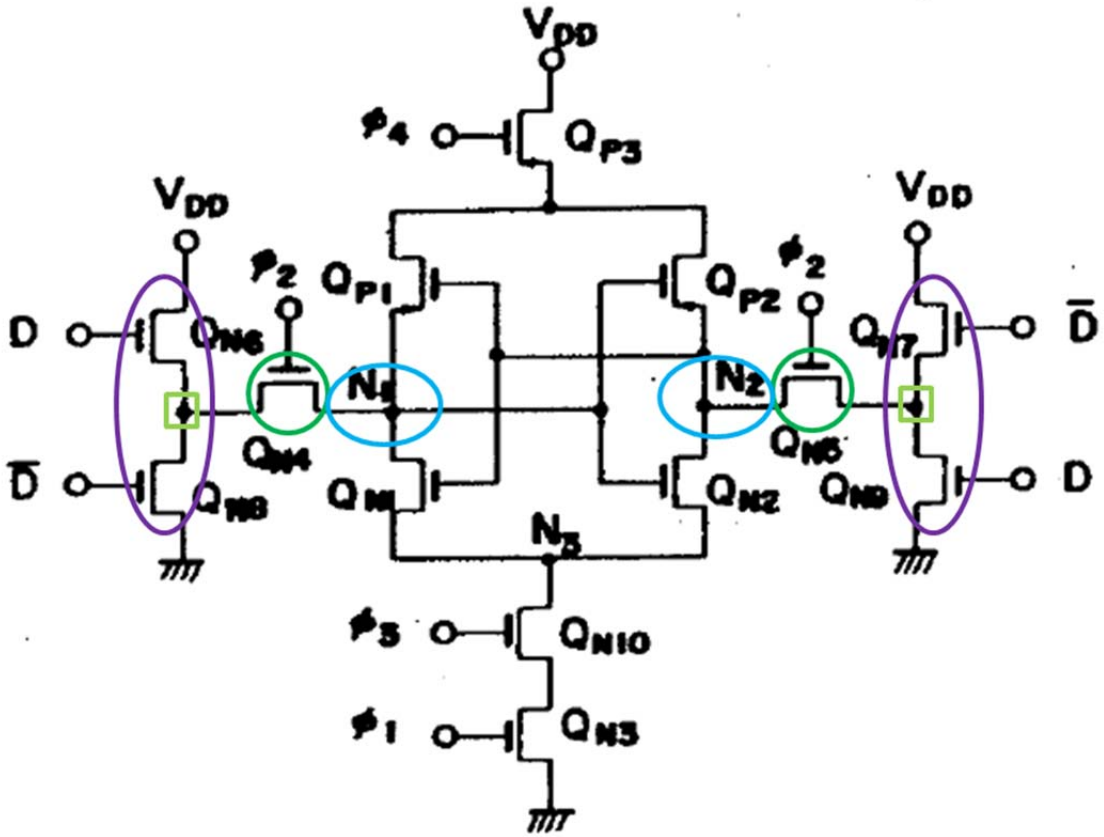
d) "first and second local data write driver circuits each having a first transistor, a second transistor, and an output node coupled selectively by a corresponding one of the first and second pass transistors to the latch circuit and to a corresponding bit line;"

Inoue discloses this feature. (Ex. 1002, ¶¶99-101.) As discussed above for claim element 1(d), *Inoue* discloses that Q_{N6} /Q_{N8} and Q_{N7}/Q_{N9} constitute "local data write driver circuits." (Ex. 1005, 3, 4; *see also id.*, FIG. 6; Section IX.A.1(d).) Therefore, *Inoue* discloses Q_{N6}/Q_{N8} ("first local data write driver circuits") and Q_{N7}/Q_{N9} ("second local data write driver circuits") each having Q_{N6} or Q_{N7} ("a first transistor"), and Q_{N8} or Q_{N9} ("a second transistor").

Moreover, as discussed above for claim 2, each of Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} has an output node (*e.g.*, the common node between Q_{N6} and Q_{N8}, and the common

node between Q_{N7} and Q_{N9}). (Ex. 1005, 3, 4; *see also id.*, FIG. 6; Section IX.A.2(a).) As discussed above for claim element 1(e), these output nodes are coupled to a corresponding bit line (node N_1 or N_2) of Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} ("the latch circuit") by a corresponding one of Q_{N4} ("the first pass transistor") and Q_{N5} ("the second pass transistor") when Q_{N4} and Q_{N5} are conducting, *i.e.*, "coupled selectively." (Ex. 1005, 3, 4; *see also id.*, FIG. 6; Section IX.A.1(e).)

第 6 図



(Ex. 1002, ¶100, citing Ex. 1005, FIG. 6 (annotated to show that the output node (light green) of local data write driver circuits (purple) are selectively connected to respective nodes N1, N2 (blue) through corresponding pass transistors (dark green).)

The '270 patent discloses the same configuration:

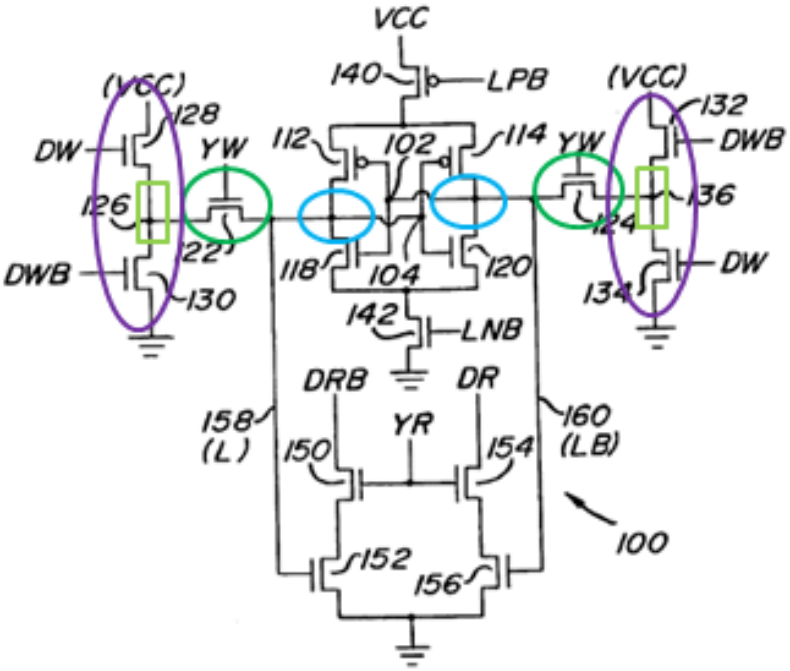


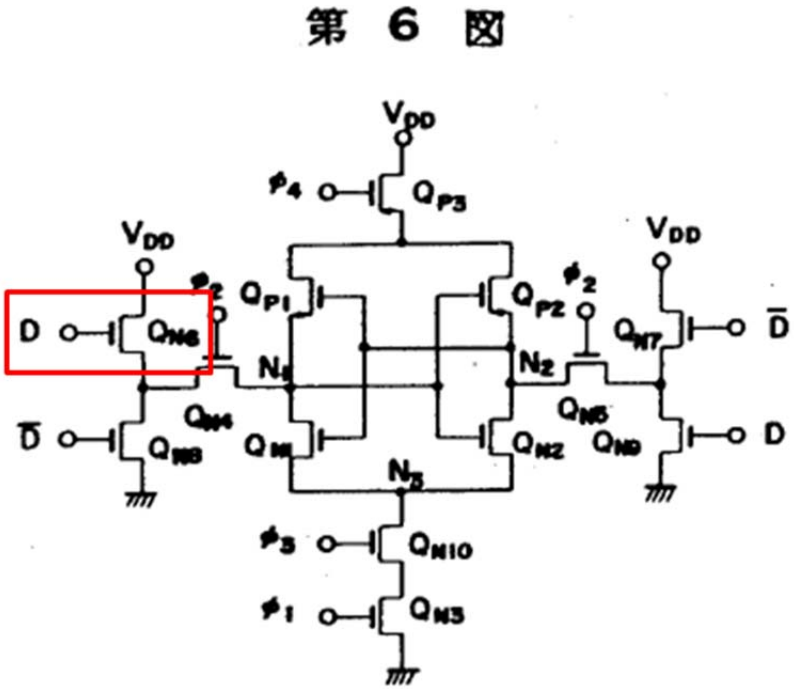
FIG. 5

(Ex. 1002, ¶101, citing Ex. 1001, FIG. 5 (annotated).)

e) "said first transistor of said first local data write driver circuit having a control electrode connected to receive a first data write signal;"

Inoue discloses this feature. (Ex. 1002, ¶¶102-103.) *Inoue* discloses Q_{N6} ("said first transistor") of Q_{N6}/Q_{N8} ("said first local data write driver circuit")

having a gate terminal ("control electrode") connected to receive a signal at terminal D ("a first data write signal"). (Ex. 1005, FIG. 6.) For instance, *Inoue* discloses that "D, $\overline{D}$ [are] write data input terminals used to write data to F/F." (*Id.*, 3.) Therefore, the signal at terminal D is a "first data write signal."



(Ex. 1002, ¶102, citing Ex. 1005, FIG. 6 (annotated to show the first transistor Q_{N6} receiving a first data write signal D at its gate terminal).)

The '270 patent discloses the same configuration:

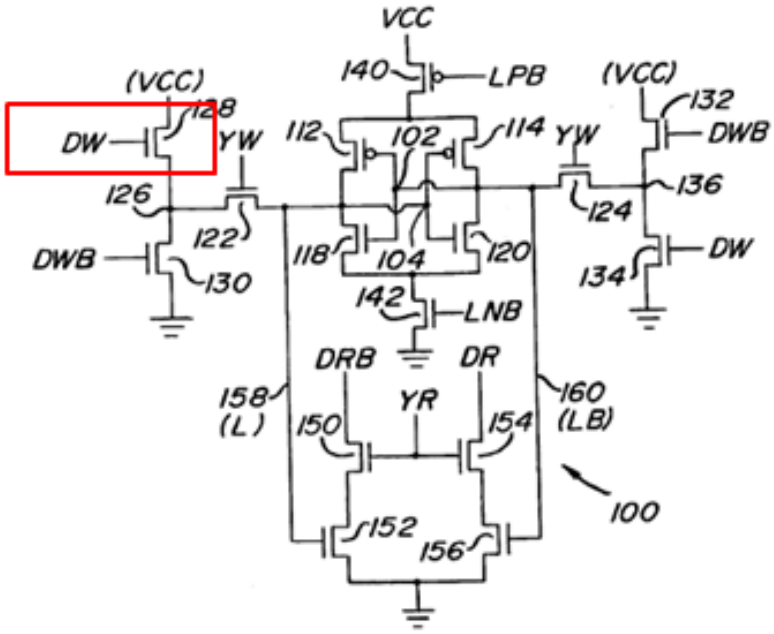


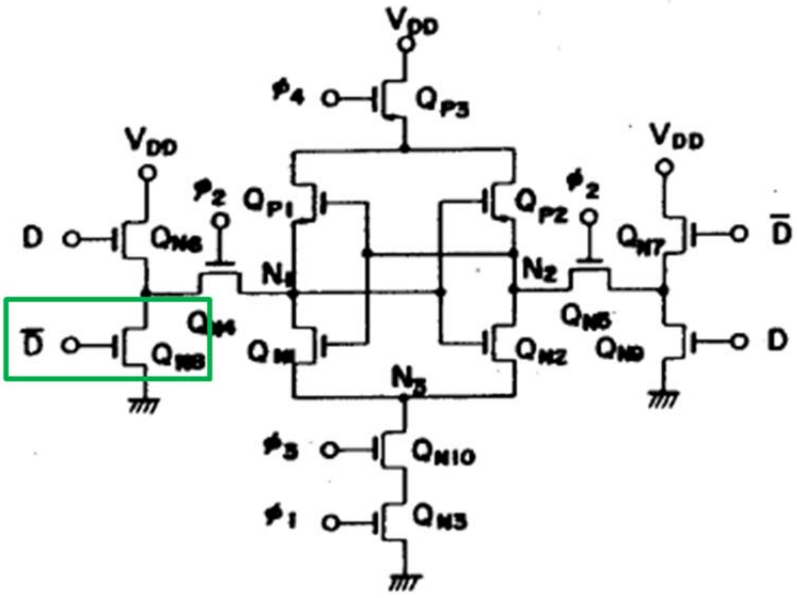
FIG. 5

(Ex. 1002, ¶103, citing Ex. 1001, FIG. 5 (annotated).)

f) "said second transistor of said first local data write driver circuit having a control electrode connected to receive a second data write signal;"

Inoue discloses this feature. (Ex. 1002, ¶¶104-105.) *Inoue* discloses Q_{N8} ("said second transistor") of Q_{N6} /Q_{N8} ("said first local data write driver circuit") having a gate terminal ("control electrode") connected to receive a signal at write data input terminal $\overline{D}$ ("a second data write signal"). (Ex. 1005, FIG. 6.) For instance, *Inoue* discloses that "D, $\overline{D}$ [are] write data input terminals used to write data to F/F." (Ex. 1005, 3.) Therefore, the signal at terminal $\overline{D}$ is a "second data write signal."

第 6 図



(Ex. 1002, ¶104, citing Ex. 1005, FIG. 6 (annotated to show the second transistor Q_{N8} receiving a second data write signal $\overline{D}$ at its gate terminal).)

The ’270 patent discloses the same configuration:

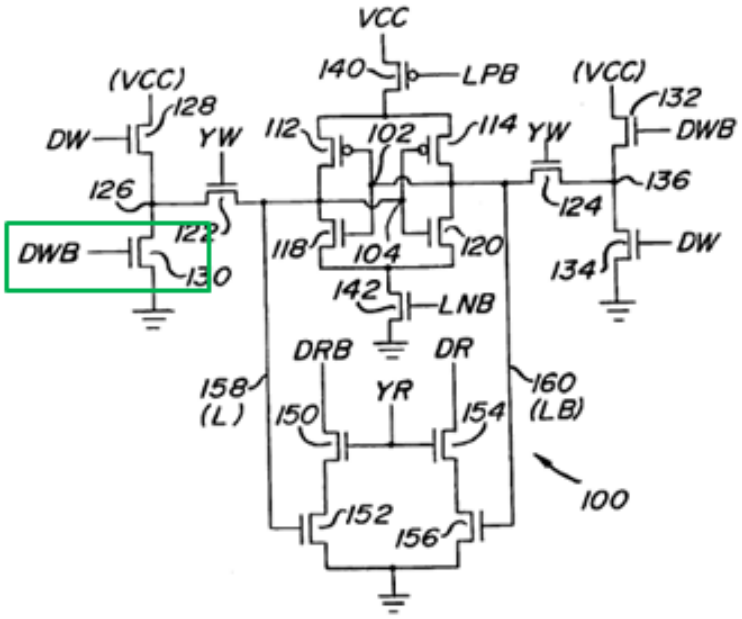


FIG. 5

(Ex. 1002, ¶105, citing Ex. 1001, FIG. 5 (annotated).)

g) "said first transistor of said second local data write driver circuit having a control electrode connected to receive said second data write signal;"

Inoue discloses this feature. (Ex. 1002, ¶¶106-107.) *Inoue* discloses Q_{N7} ("said first transistor") of Q_{N7}/Q_{N9} ("said second local data write driver circuit") having a gate terminal ("control electrode") connected to receive a signal at write data input terminal $\overline{D}$ ("second data write signal"). (Ex. 1005, FIG. 6.)

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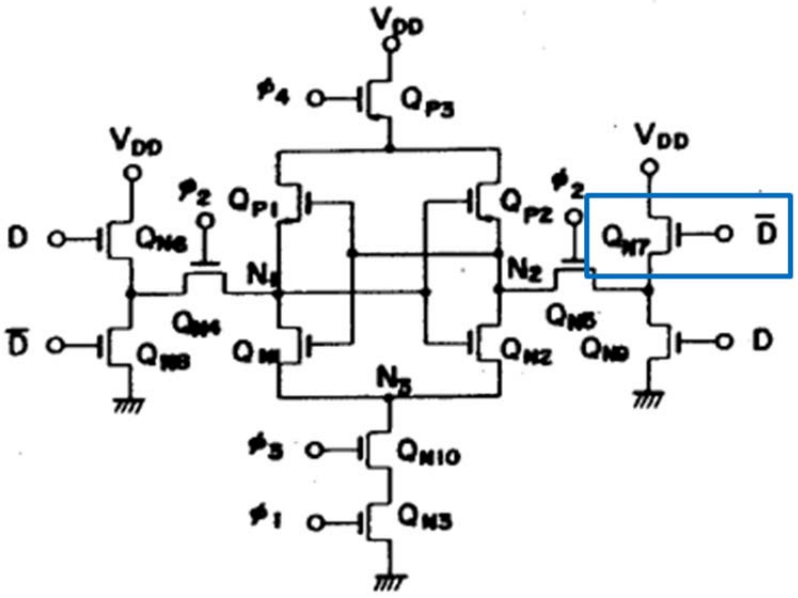

(Ex. 1002, ¶106, citing Ex. 1005, FIG. 6 (annotated to show the first transistor Q_{N7} receiving a second data write signal $\overline{D}$ at its gate terminal).)

The ’270 patent discloses the same configuration:

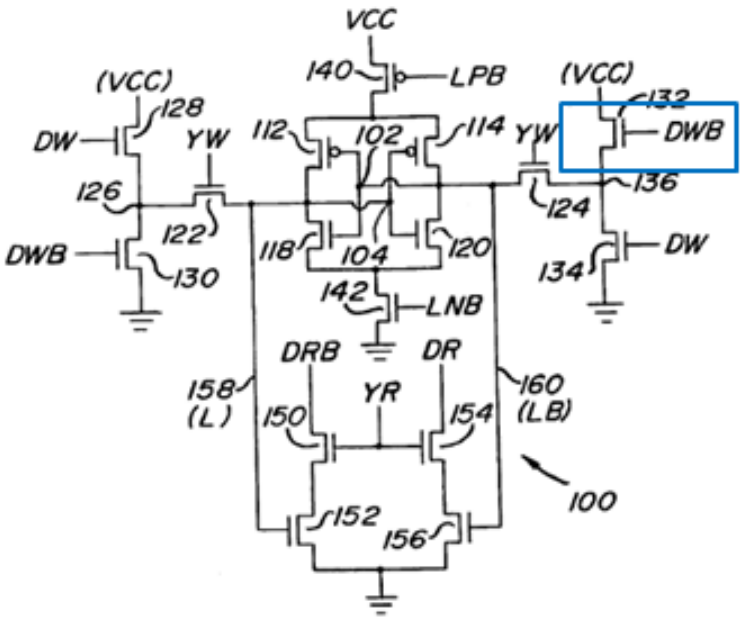

FIG. 5

(Ex. 1002, ¶107, citing Ex. 1001, FIG. 5 (annotated).)

h) "said second transistor of said second local data write driver circuit having a control electrode connected to receive said first data write signal."

Inoue discloses this feature. (Ex. 1002, ¶¶108-109.) *Inoue* discloses that Q_{N9} ("said second transistor") of Q_{N7} /Q_{N9} ("said second local data write driver circuit") having a gate ("control electrode") connected to receive a signal at write data input terminal D ("said first data write signal"). (Ex. 1005, FIG. 6.)

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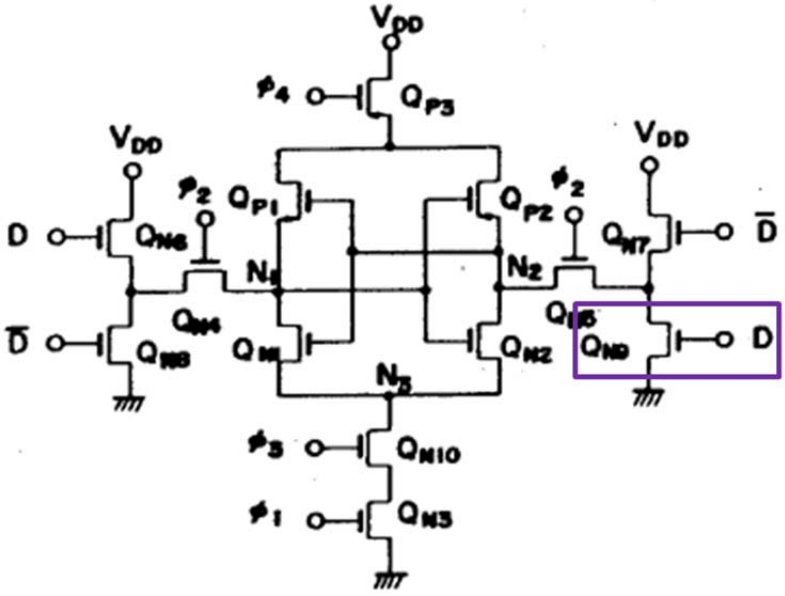


(Ex. 1002, ¶107, citing Ex. 1005, FIG. 6 (annotated to show the first transistor Q_{N6} receiving a first data write signal D at its gate terminal).)

The ’270 patent discloses the same configuration:

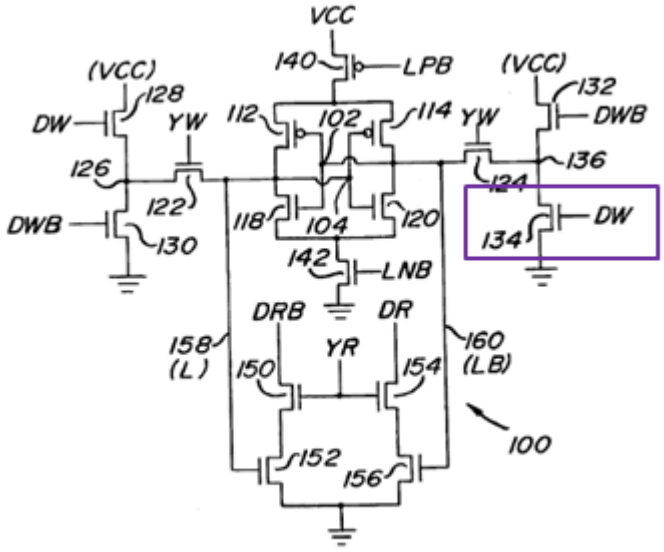


FIG. 5

(Ex. 1002, ¶109, citing Ex. 1001, FIG. 5 (annotated).)

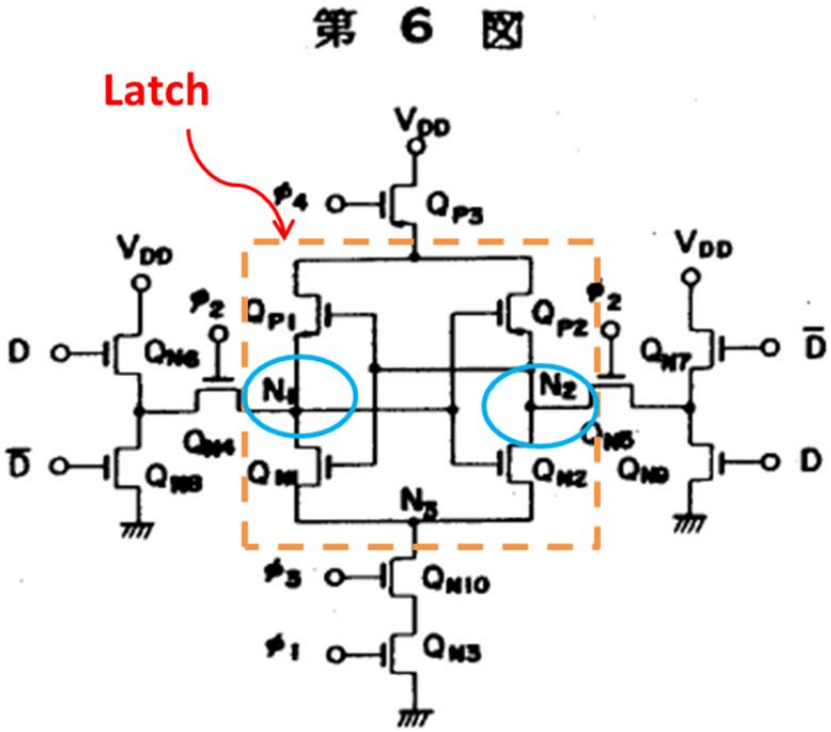
8. Claim 30

a) "A sense amplifier arrangement for an integrated circuit memory comprising:"

To the extent the preamble is limiting, *Inoue* discloses this feature for reasons discussed above for claim element 1(a). (Ex. 1002, ¶110; Section IX.A.1(a).)

b) "a sense amplifier latch circuit having internal nodes coupled directly or selectively to at least one pair of bit lines of the memory;"

Inoue discloses this feature. (Ex. 1002, ¶¶111-112.) As discussed above for claim element 1(b), transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} constitute a "latch circuit" having internal nodes $N_1$and N_2 that couple to a respective bit line pair of a memory. (Section IX.A.1(b).) *Inoue* discloses that in the figure 6 configuration "nodes N_1 and N_2" may correspond to bit lines of "memory" and that the latch circuit of figure 6 is a "sense amplifier latch circuit" because the circuit in figure 6 is disclosed as being applicable to a sense amplifier in dynamic memory. (Ex. 1005, 4, FIG. 6.)



(Ex. 1002, ¶111, citing Ex. 1005, FIG. 6 (annotated to show internal nodes (blue) of the latch circuit (orange).)

The ’270 patent discloses the same configuration:

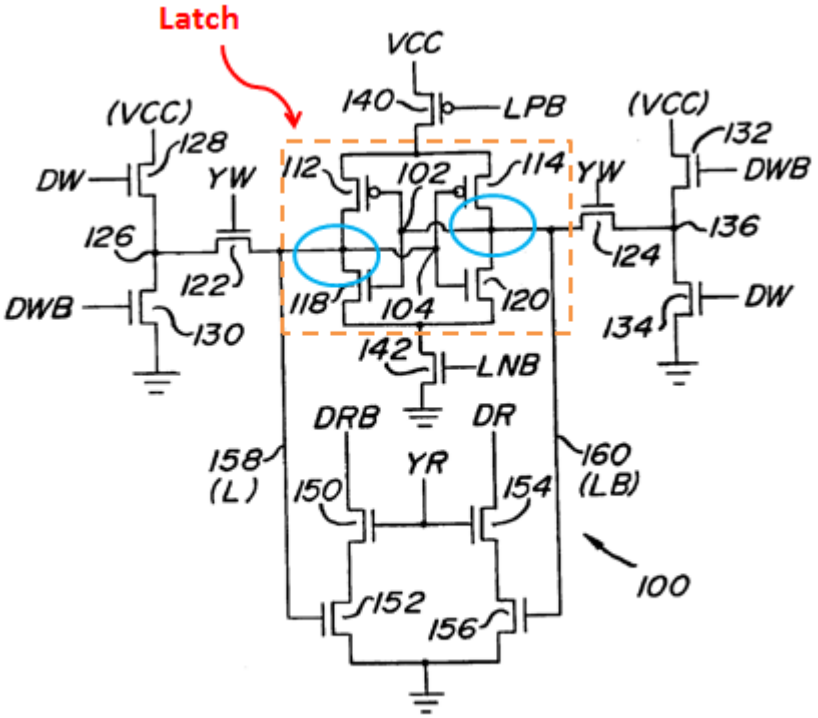


FIG. 5

(Ex. 1002, ¶112, citing Ex. 1001, FIG. 5 (annotated).)

c) "a local data write driver circuit coupled to said latch circuit, said driver circuit including a plurality of transistors coupled together;"

Inoue discloses this feature. (Ex. 1002, ¶¶113-114.) As discussed above for claim element 1(d), *Inoue* discloses that Q_{N6} /Q_{N8} and Q_{N7}/Q_{N9} constitute "local data write driver circuits." (Ex. 1005, 3, 4; FIG. 6; Section IX.A.1(d).) Therefore, *Inoue* discloses that each of Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} is a "local data write driver circuit." Moreover, as discussed above for claim element 1(e), when Q_{N4} or Q_{N5} are conductive, the output of Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} is coupled to N_1 or N_2 (the nodes of the latch circuit Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}). (Ex. 1005, 3, 4; FIG. 6; Section IX.A.1(e).)

Therefore, *Inoue* discloses "a local data write driver circuit coupled to said latch circuit." As shown below, *Inoue* discloses that driver circuit Q_{N6}/Q_{N8} includes Q_{N6} and Q_{N8} ("a plurality of transistors") and driver circuit Q_{N7}/Q_{N9} includes Q_{N7} and Q_{N9} ("a plurality of transistors") that are coupled together. (Section IX.A.2, explaining that the two transistors in each write driver circuit are connected in series.)

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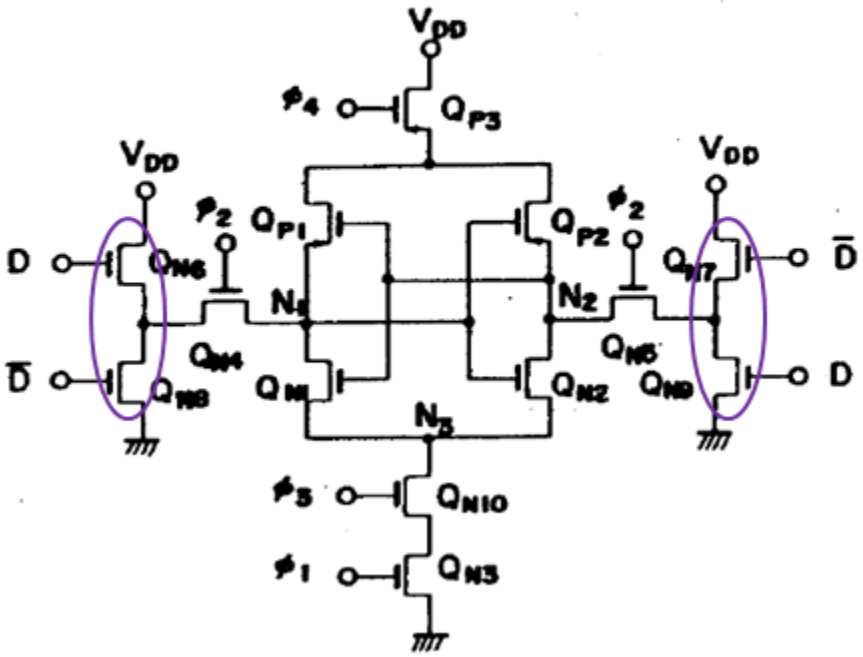

(Ex. 1002, ¶113, citing Ex. 1005, FIG. 6 (annotated to show local data write driver circuits (purple).)

The '270 patent discloses the same configuration:

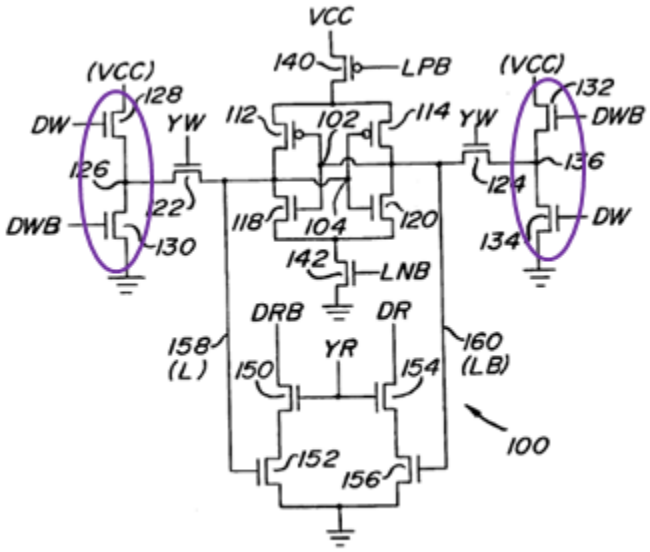

FIG. 5

(Ex. 1002, ¶114, citing Ex. 1001, FIG. 5 (annotated).)

d) "said local data write driver circuit being responsively coupled to a data write control signal so that a power supply voltage may be selectively coupled via said local data write driver circuit to an internal node of said latch circuit and thus to a corresponding bit line, in accordance with said data write control signal."

Inoue discloses this feature. (Ex. 1002, ¶¶115-117.) *Inoue* discloses that each of Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("said local data write driver circuit") is responsively coupled to signals on write data input terminals D or $\overline{D}$ ("a data write control signal") so that V_{DD} ("a power supply voltage") may be selectively coupled via Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("said local data write driver circuit") to N_1 or N_2 ("an internal node of said latch circuit") and thus to a corresponding bit line, in accordance with the data write control signal. (Ex. 1005, 3, 4, FIG. 6.)

For instance, *Inoue* discloses that "D, $\overline{D}$ [are] write data input terminals used to write data to F/F." (Ex. 1005, 3.) Each of the signals at terminals D and $\overline{D}$ is a "data write control signal." Terminal D is the gate terminal of Q_{N6}, and terminal $\overline{D}$ is the gate terminal Q_{N7}. (*Id.*) Therefore, each of Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("said local data write driver circuit") is "responsively" coupled to D ("a data write control signal") and $\overline{D}$ ("a data write control signal") because these signals are applied to the gates of one of the transistors in each of these data write driver circuits, and the gate of a transistor controls the transistor's conductivity. (Ex. 1002, ¶116.) *Inoue* gives an example of this fundamental circuit concept when it explains that a high voltage (V_{DD}) at terminal D (which provides the gate voltage for Q_{N6}) results in current flow through Q_{N6}. (Ex. 1005, 3.)

Inoue also discloses that because of the above configuration "a power supply voltage may be selectively coupled . . ." like that recited in this claim element. (Ex. 1002, ¶117.) *Inoue* discloses that when "the terminal D is at 'H' and the terminal $\overline{D}$ at 'L', the node N_1 is charged through the path $V_{DD} \rightarrow Q_{N6} \rightarrow Q_{N4} \rightarrow N_1$ and assumes a level 'H.'" (Ex. 1005, 3.) A POSITA would have understood that when the terminal $\overline{D}$ at 'H' and the terminal D is at 'L,' the node N_2 would be charged through the path $V_{DD} \rightarrow Q_{N7} \rightarrow Q_{N5} \rightarrow N_2$ and assume a level 'H.' (Ex. 1002, ¶117.) V_{DD} ("a power supply voltage") may be selectively coupled via Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("said local data write driver circuit") to N_1 or N_2 ("an

internal node of said latch circuit") and thus to a corresponding bit line (because N1 and N2 are connected to bit lines), in accordance with control signal D and $\overline{D}$ ("data write control signals"). The coupling is "selective" because this current flow occurs when "the terminal D is at 'H' and the terminal $\overline{D}$ at 'L'." (*Id.*)

9. Claim 31

a) "The sense amplifier arrangement according to claim 30 wherein said data write control signal includes first and second data write control signals;"

Inoue discloses this feature. (Ex. 1002, ¶118.) *Inoue* discloses a signal at write data input terminal D ("first data write control signal") and a signal at write data input terminal $\overline{D}$ ("second data write control signal"). (*See* discussion in Section IX.A.1(d).)

b) "wherein said local data write driver circuit includes a first transistor responsively coupled to said first data write control signal and coupled to a first power supply voltage, and a second transistor responsively coupled to said second data write control signal and coupled to a second power supply voltage."

Inoue discloses this feature. (Ex. 1002, ¶¶119-120.) For example, *Inoue* discloses that said local data write driver circuit Q_{N6}/Q_{N8} includes Q_{N6} ("a first transistor") responsively coupled to signal at terminal D ("said first data write control signal") and coupled to V_{DD} ("a first power supply voltage"), and Q_{N8} ("a second transistor") responsively coupled to signal at terminal $\overline{D}$ ("second data write

control signal") and coupled to GND ("a second power supply voltage"). (Ex. 1005, FIG. 6.) Transistors Q_{N6} and Q_{N8} are "responsively" coupled to D ("first data write control signal") and $\overline{D}$ ("a second write control signal"), respectively, because these signals are applied to the gate terminals of these transistors and the gate of a transistor controls the transistor's conductivity. (*See* Section IX.A.1(d).)

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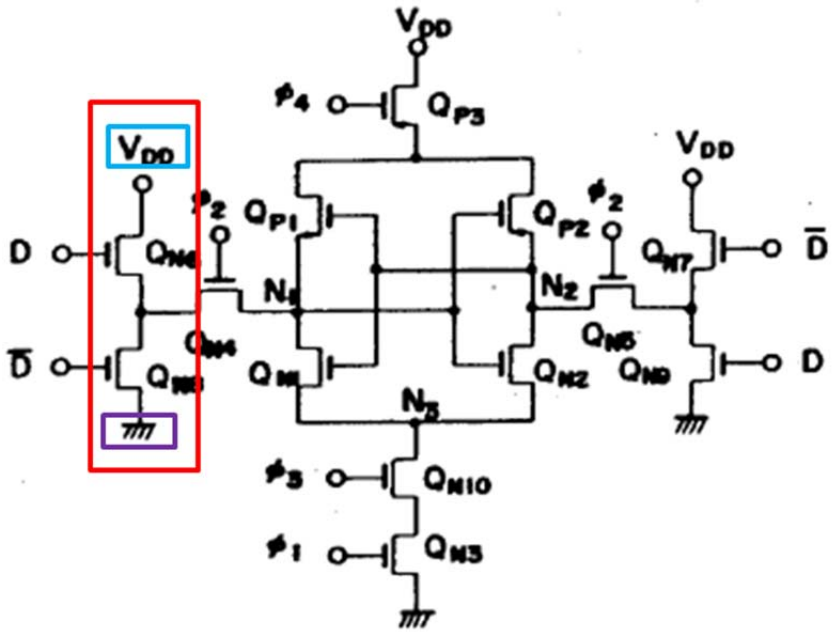


(Ex. 1002, ¶119, citing Ex. 1005, FIG. 6 (annotated with claimed features in red, including first power supply voltage (blue) and second power supply voltage (purple)).)

The '270 patent discloses the same configuration:

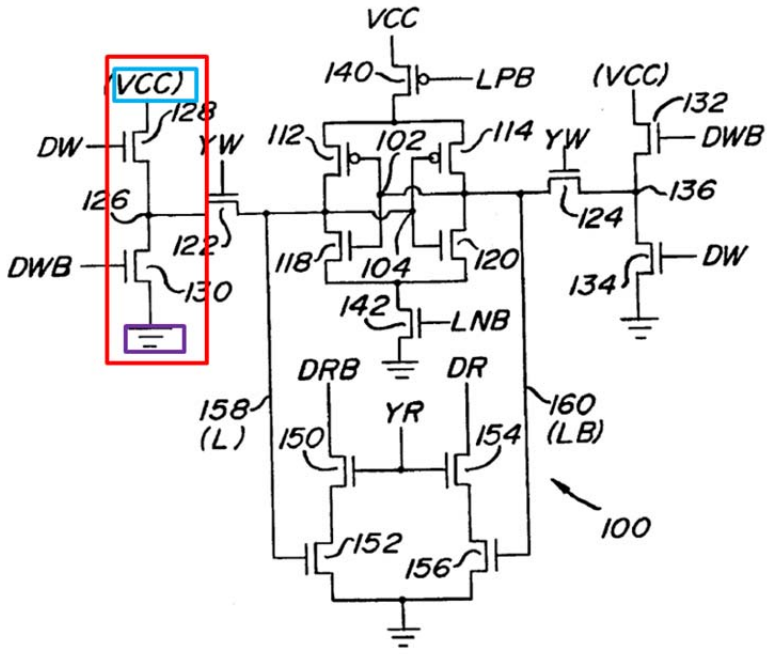


FIG. 5

(Ex. 1002, ¶120, citing Ex. 1001, FIG. 5 (annotated).)

10. Claim 32

a) "The sense amplifier arrangement according to claim 30 wherein said data write control signal includes first and second data write control signals;"

Inoue discloses this feature for reasons discussed above for claim element 31(a). (Ex. 1002, ¶121; Section IX.A.9(a).)

b) "wherein said local data write driver circuit comprises first and second local data write driver circuits, each including respective first and second transistors responsively coupled to said first and second data write control signals, each said transistor also being coupled to a corresponding power supply voltage."

Inoue discloses this feature. (Ex. 1002, ¶122.) *Inoue* discloses a "first local data write driver circuit" Q_{N6}/Q_{N8} and a "second local data write driver circuit"

Q_{N7}/Q_{N9}. Each of the local data write driver circuits includes Q_{N6} or Q_{N9} ("a first transistor") responsively coupled to signal at terminal D ("said first data write control signal"), and Q_{N7} or Q_{N8} ("a second transistor") responsively coupled to signal at terminal $\overline{D}$ ("second data write control signal"). (Ex. 1005, FIG. 6 (annotated below).) Each of transistors Q_{N6}, Q_{N8}, Q_{N7}, Q_{N9} is "responsively" coupled to one of D ("first data write control signal") and $\overline{D}$ ("a second write control signal") because these signals are applied to the gate terminals of these transistors and the gate of a transistor controls the transistor's conductivity. (Ex. 1002, ¶122; Section IX.A.1(d).) Transistors QN6 and QN7 are coupled to VDD ("a [first] corresponding power supply voltage"), and transistors QN8 and QN9 are coupled to GND ("a [second] corresponding power supply voltage"). (Ex. 1005, FIG. 6; Ex. 1002, ¶122.)

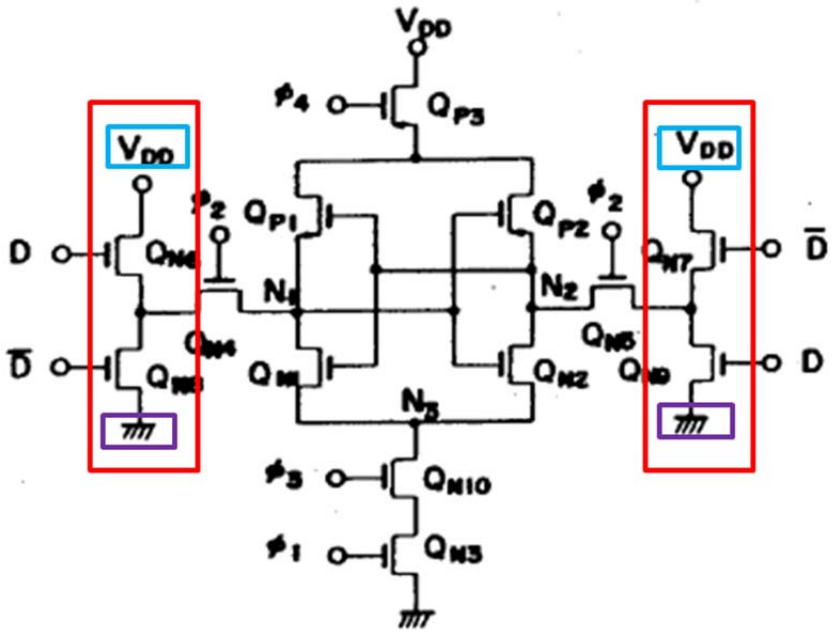
11. Claim 34

a) "The sense amplifier arrangement according to claim 30 wherein said local data write driver circuit comprises a pair of transistors having source-drain paths connected in series between first and second power supply voltages;"

Inoue discloses this feature. (Ex. 1002, ¶¶123-124.) *Inoue* discloses that each of Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("said local data write driver circuit") comprises a pair of transistors having source-drain paths connected in series between V_{DD} ("first

power supply voltage") and GND ("second power supply voltage"). (Ex. 1005, FIG. 6; Section IX.A(2).)

第 6 図



(Ex. 1002, ¶123, citing Ex. 1005, FIG. 6 (annotated with claimed features in red, including first power supply voltage (blue) and second power supply voltage (purple)).)

The '270 patent discloses the same configuration:

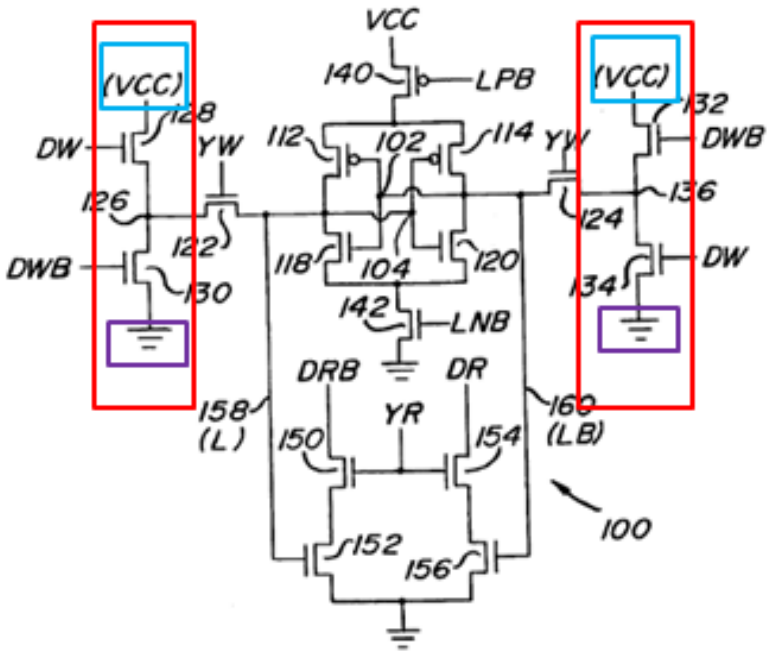


FIG. 5

(Ex. 1002, ¶124, citing Ex. 1001, FIG. 5 (annotated).)

b) "at least one of said local data write driver circuit transistors having a gate electrode connected to receive said data write control signal."

Inoue discloses this feature. (Ex. 1002, ¶125.) *Inoue* discloses that all four of the transistors in the transistor pairs Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("at least one of said local data write driver circuit transistors") have a gate electrode connected to receive a signal at write data input terminals D or $\overline{D}$ ("said data write control signal"). (Ex. 1005, FIG. 6.)

12. Claim 35

a) **"**The sense amplifier arrangement according to claim 34 wherein one of said power supply voltages is provided by said data write control signal."

Inoue discloses this feature. (Ex. 1002, ¶¶126-127.) *Inoue* discloses that the input voltage at terminals D and $\overline{D}$ is an "H" or "L" which according to *Inoue* correspond to V_{DD} and GND ("power supply voltages"), respectively. (Ex. 1005, 3, "the terminal D is at 'H' and the terminal $\overline{D}$ at 'L', the node N_1 is charged through the path $V_{DD} \rightarrow Q_{N6} \rightarrow Q_{N4} \rightarrow N_1$ and assumes a level 'H.'") A POSITA would have understood that 'H' in *Inoue* corresponds to V_{DD} because the statement that "node N_1 is charged through the path $V_{DD} \rightarrow Q_{N6} \rightarrow Q_{N4} \rightarrow N_1$" shows that node N_1 will be charged to V_{DD}, and *Inoue* states that the result of this charging is that node N_1 is at 'H.' (Ex. 1002, ¶126.) Thus, terminal D has a value of V_{DD} because it is at 'H' at the time of the writing. Accordingly, terminal D provides the power supply voltage V_{DD} to gate Q_{N6} and therefore *Inoue* teaches "wherein one of said power supply voltages is provided by said data write control signal." Similarly, *Inoue* indicates that 'L' corresponds to ground. (Ex. 1005, 3, "the node N_2 is discharged through the path $N_2 \rightarrow Q_{N5} \rightarrow Q_{N9} \rightarrow$ GND and assumes a level "L.") Therefore, $\overline{D}$ similarly provides ground ("power supply voltage") to the gate of Q_{N8}.

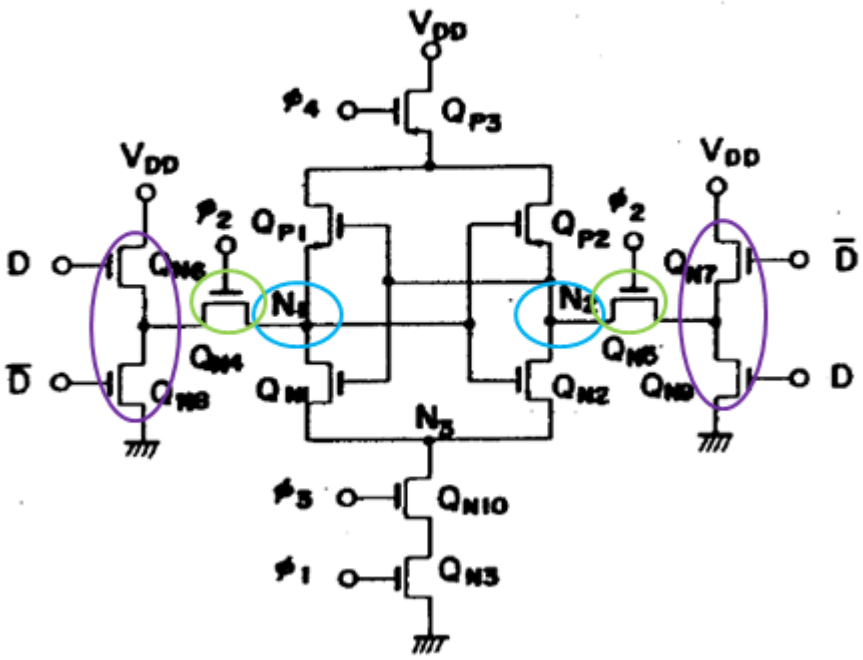
Inoue discloses these features for another reason. Terminal D ("data write control signal") also provides power supply voltage V_{DD} to node N1 because when D is "at 'H' and the terminal $\overline{D}$ at 'L', the node N_1 is charged through the path $V_{DD} \rightarrow Q_{N6} \rightarrow Q_{N4} \rightarrow N_1$ and assumes a level 'H.'" (*Id*.) At the same time, "the node N2 is discharged through the path N2 → QN5 → QN9 → GND and [] assumes a level 'L'." (*Id*.) That is, terminal D ("data write control signal") also provides power supply voltage GND to node N2. In both the above instances, *Inoue* teaches "wherein one of said power supply voltages is provided by said data write control signal." (Ex. 1002, ¶127.)

13. Claim 36

a) **"**The sense amplifier arrangement according to claim 34 further comprising a coupling transistor coupling said local data write driver circuit to a corresponding one of said internal nodes."

Inoue discloses this feature. (Ex. 1002, ¶¶128-129.) *Inoue* discloses Q_{N4} or Q_{N5} ("a coupling transistor") coupling Q_{N6}/Q_{N8} or $Q_{N7}/Q_{N9,}$ respectively ("said local data write driver circuit"), to N_1 or N_2 ("a corresponding one of said internal nodes"), respectively. For instance, in *Inoue* "clock ϕ_2 is allowed to rise, thereby causing Q_{N4} and Q_{N5} to be conducting" (Ex. 1005, 3, FIGS. 4 and 6) and "when clock ϕ_2 rises, Q_{N4} becomes conducting, and the current flows from V_{DD} to the node N_1 through Q_{N6} and Q_{N4}, while the current flows out from N_2 to GND through Q_{N5} and Q_{N9}." (Ex. 1005, 3, FIG. 6.)

第 6 図



(Ex. 1002, ¶128, citing Ex. 1005, FIG. 6 (annotated with local write driver circuits (purple), coupling transistors (green) and internal nodes (blue).)

The ’270 patent discloses the same configuration:

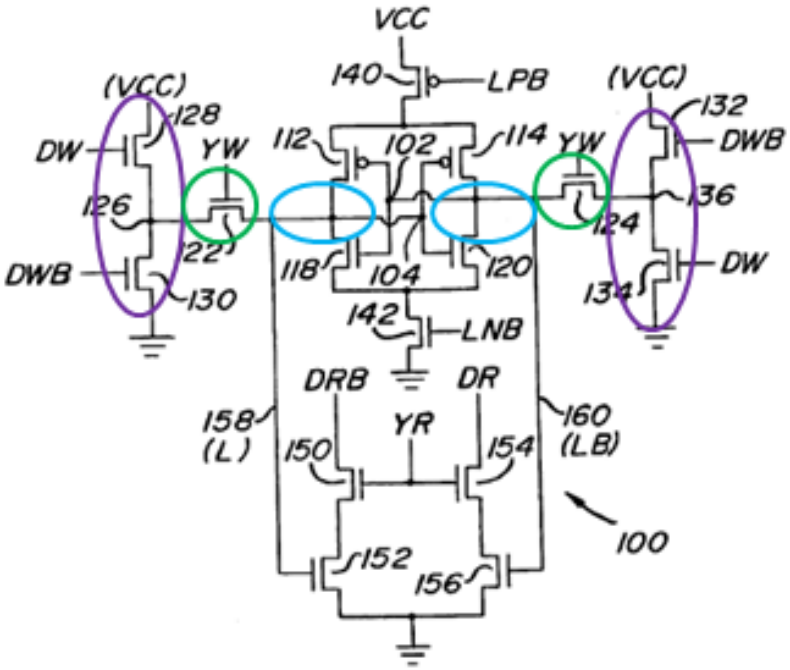


FIG. 5

(Ex. 1002, ¶129, citing Ex. 1001, FIG. 5 (annotated).)

14. Claim 38

a) "The sense amplifier arrangement according to claim 35 further comprising a coupling transistor coupling said local data write driver circuit to a corresponding one of said internal nodes."

Inoue discloses this feature for the reasons discussed above for claim 36.

(Ex. 1002, ¶130; Section IX.A.13.)

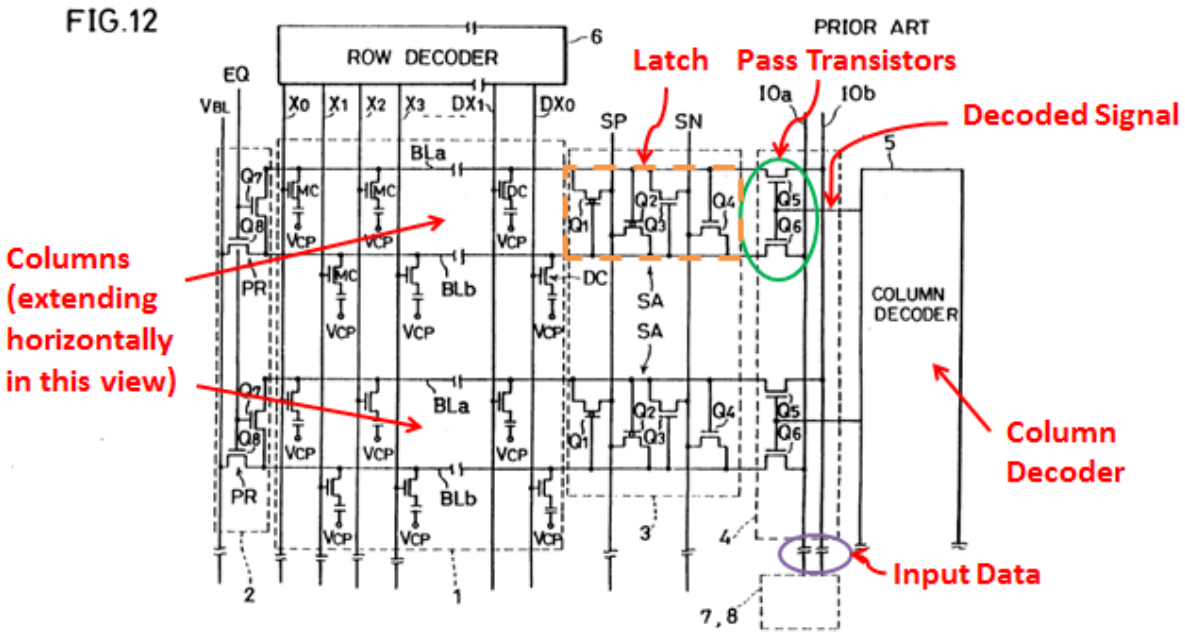
B. Ground 2: *Inoue* and *Ogawa* Render Obvious Claims 4-6, 12-14, 17, 19, 37, and 39

1. Claim 4

a) "The sense amplifier arrangement according to claim 3 wherein said write control signal is a column write signal."

Inoue in combination with *Ogawa* discloses this feature. (Ex. 1002, ¶¶131-139.) While *Inoue* discloses that ϕ_2 is a write control clock ("a write control signal") that is received by the pass transistors Q_{N4} and Q_{N5} (*see* claim element 3(a)), it does not expressly disclose that ϕ_2 is a column write signal. As discussed below, *Ogawa* discloses this feature, and it would have been obvious to a POSITA to utilize a column write signal as the write control signal in *Inoue* in light of *Ogawa*. (Ex. 1002, ¶132.)

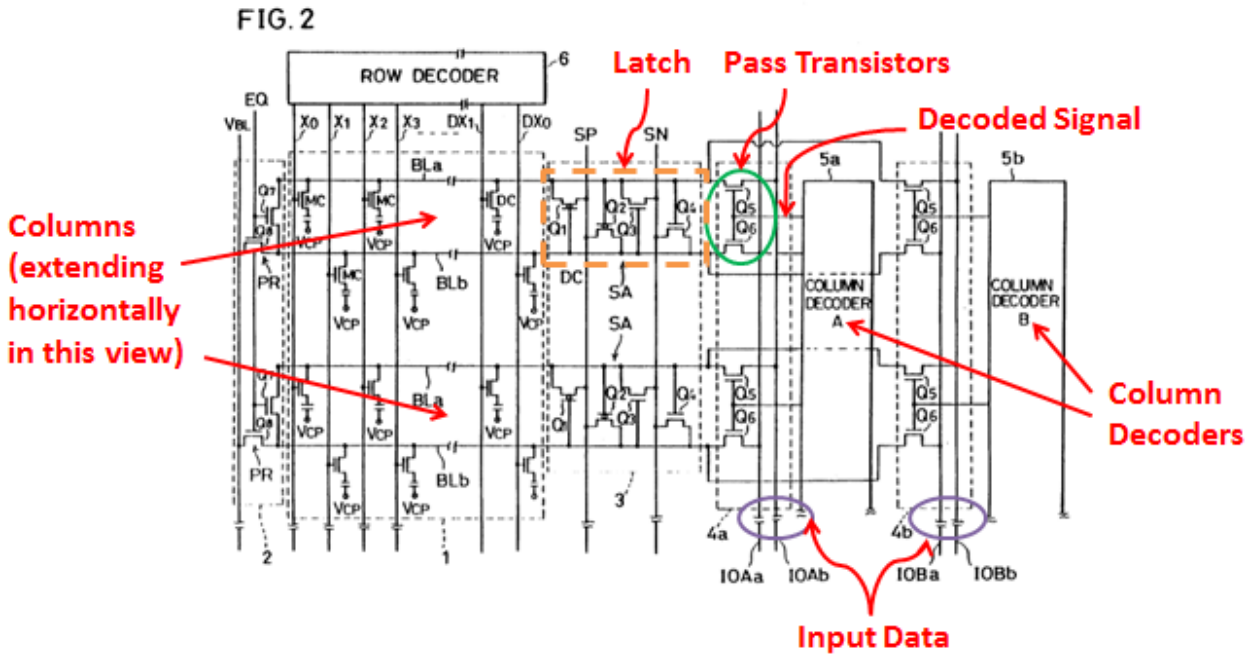
Ogawa discloses a variation of the conventional dynamic memory system in which "a plurality of memory cells [are] arranged in a matrix of rows and columns." (*See, e.g.*, Ex. 1006, 1:18-19, FIGS. 2, 12; *see also supra* Section VII.A, citing Ex. 1008, FIG. 2.) *Ogawa* explains that in the conventional memory writing technique a "column decoder 5" is provided a column address, which decodes the address, and selects "a desired bit line pair." (Ex. 1006, 1:24-27, FIGS. 2, 12, 3:1-13.) To select a bit line pair (column) for writing data (which is provided on data buses IOa and IOb), the column decoder turns on transistors Q5 and Q6 corresponding to that bit line pair. (Ex. 1006, 2:17-26, FIG. 12.)



(Ex. 1002, ¶133-134, citing Ex. 1006, FIG. 12 (annotated).)

Annotated figure 12 above and below also shows the correspondence between *Inoue*'s FIG. 6 and *Ogawa*'s circuitry. As shown, Q_5 and Q_6 are the corresponding "pass transistors" in *Ogawa*'s circuit because like *Inoue*'s transistors Q_{N4} and Q_{N5}, these transistors must be turned ON to access the latch circuit. (*Id.*; Ex. 1006, 2:7-12; Ex. 1005, 3, 4; Section IX.A.1(c).)

Ogawa's embodiments (*e.g.*, figure 12) retain the above basic functionality during a write operation but modify the conventional arrangement by providing two column decoders (*e.g.*, decoders 5A and 5B in figure 2) instead of one (decoder 5 in figure 12). (Ex. 1002, ¶135; Ex. 1006, 8:16-36; *compare id.*, FIG. 12, *with* FIG. 2.)



(Ex. 1002, ¶135, citing Ex. 1006, FIG. 2 (annotated).)

Based on the foregoing disclosures, a POSITA would have understood that *Ogawa*'s signal provided from any of column decoders 5/5a/5b to pass transistors Q5 and Q6 is a "column write signal" as in claim 4 of the '270 patent when the decoder(s) select a column (bit line pair) for writing. (Ex. 1002, ¶136.) Indeed, at the time of writing to a given column, the decoded signal output from decoders 5A/5B/5 turns ON transistors Q5 and Q6 "connected to the select bit line pair" to allow data on the data buses to be written to each bit line. (Ex. 1006, 2:17-33, 8:16-36.)

In view of *Ogawa*, it would have been obvious to a POSITA to implement *Inoue*'s write control clock ϕ_2 as a "column write signal" that is provided by a decoder as disclosed in *Ogawa*. (Ex. 1002, ¶137.) A POSITA would have looked

to *Ogawa* to refine or improve the *Inoue* system, because *Inoue* discloses that its figure 6 circuit configuration may be applied to a sense amplifier in dynamic memory and *Ogawa* teaches how to operate a dynamic memory with multiple rows and columns of memory cells. (*Id.*)

A POSITA would have been motivated to use *Ogawa*'s teachings to enable *Inoue*'s system to work with a memory array containing rows and columns of memory cells, particularly in light of the fact that at the time of the alleged invention of the '270 patent a typical way to arrange memory cells in dynamic memory was by columns and rows, as explained by *Ogawa*. (*Id.*, ¶138; Section VII.A.) Modifying the write control clock ϕ_2 in *Inoue* to be a "column write signal" that is provided by a decoder as disclosed in *Ogawa* would have allowed a column of memory cells to be selected and would have been a necessary feature to enable *Inoue*'s configuration to be implemented in a dynamic memory, which would have included many memory cells. (Ex. 1002, ¶138.) *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007).

The above modification would have been the result of combining prior art elements (*e.g.*, *Inoue*'s sense amplifier and pass transistors (Ex. 1005, FIG. 6), and *Ogawa*'s column decoder that drives pass transistors (Ex. 1006, FIGS. 2 and 12) according to known methods (*e.g.*, driving a pass transistor with the column write signal as in *Ogawa*) to yield predictable results (*e.g.*, turn on pass transistors using

the column write signal to select a column in memory). (Ex. 1002, ¶139.) *See KSR*, 550 U.S. at 416.

2. Claim 5

a) "The sense amplifier arrangement according to claim 4 wherein said column write signal is a decoded column write signal."

As discussed above for claim 4 the *Inoue-Ogawa* combination discloses a column write signal that is provided by a decoder, which decodes a column address. (Ex. 1002, ¶140; Section IX.B.1.) Therefore, the column write signal in the *Inoue-Ogawa* combination is a "decoded" column write signal.

3. Claim 6

a) "The sense amplifier arrangement according to claim 5 wherein said integrated circuit memory has a plurality of columns and wherein said decoded column write control signal is decoded for a subset of said plurality of columns."

Inoue in combination with *Ogawa* discloses or suggests this feature. (Ex. 1002, ¶¶141-142.) As discussed above for claims 4 and 5, the *Inoue-Ogawa* combination discloses a DRAM architecture having a plurality of columns and a decoded column write signal that is used to select among these plurality of columns for reading and writing. (*See* Sections IX.B.1. and IX.B.2.) A POSITA would have understood that a DRAM is an "integrated circuit memory." (Ex.

1002, ¶141.) Therefore, the combined *Inoue-Ogawa* system discloses "said integrated circuit memory has a plurality of columns."

Moreover, as discussed for claim 4, *Ogawa*'s decoded column select signal selects "a desired bit line pair," *i.e.*, it selects one column from the plurality of columns. (Ex. 1006, 1:24-27, FIGS. 2, 12, 3:1-13.) A single column is a "subset" of a plurality of columns. (Ex. 1002, ¶142.) Therefore, the *Inoue-Ogawa* system discloses "said decoded column write control signal is decoded for a subset of said plurality of columns."

4. Claim 12

a) "The sense amplifier arrangement according to claim 11 wherein said pass transistors are connected to receive a column write signal."

Inoue in combination with *Ogawa* discloses or suggests this feature. (Ex. 1002, ¶143.) As discussed above for claim 11, *Inoue* discloses Q_{N4} ("first") and Q_{N5} ("second") pass transistors. (Ex. 1005, 3, 4, FIG. 6; Section IX.A.7.c.) *Inoue* further discloses that Q_{N4} and Q_{N5} receive a write control clock ϕ_2, but it does not expressly disclose that ϕ_2 is a column write signal. However, as discussed above for claim 4, the combined *Inoue-Ogawa* system discloses how a POSITA would have been motivated to modify ϕ_2 to be "a column write signal." (*Id.*) Therefore, in the combined *Inoue-Ogawa* system, Q_{N4} ("first") and Q_{N5} ("second") pass transistors "are connected to receive a column write signal."

5. Claim 13

a) "The sense amplifier arrangement according to claim 12 wherein said column write signal is a decoded column write signal."

Inoue in combination with *Ogawa* discloses or suggests this feature for the reasons discussed above for claim 5. (Ex. 1002, ¶144; *supra* Section IX.B.2.)

6. Claim 14

a) "The sense amplifier arrangement according to claim 13 wherein said integrated circuit memory has a plurality of columns and wherein said decoded column write control signal is decoded for a subset of said plurality of columns."

Inoue in combination with *Ogawa* discloses or suggests this feature for the reasons discussed above for claim 6. (Ex. 1002, ¶145; *supra* Section IX.B.3.)

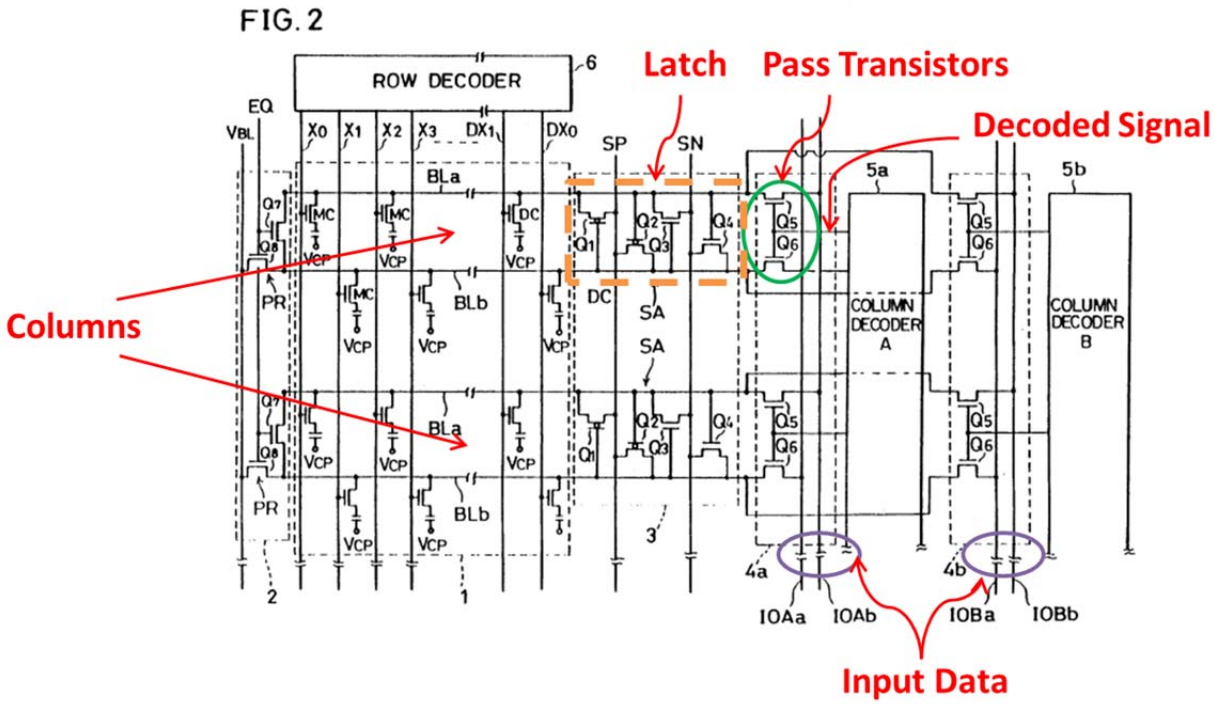
7. Claim 17

a) The sense amplifier arrangement of claim 16 wherein said first and second data write signals are controlled to have a same value when no write is to occur to a memory cell for the sense amplifier.

Inoue in combination with *Ogawa* discloses or suggests this feature. (Ex. 1002, ¶¶146-153.) In Section IX.D.6 below, *Inoue* discloses or suggests the limitations of claim 16. (*Id*.) *Inoue* further discloses that D and $\overline{D}$ (the data write terminals) control writing of data into the sense amplifier latch. (*See* Sections IX.A.7(e), IX.A.7(f).) But *Inoue* does not disclose how input data (*e.g.*, from an I/O line) is presented to D and $\overline{D}$. (Ex. 1002, ¶146.) For instance, if a '1' has to be

written to the latch, *Inoue* does not disclose how D and $\overline{D}$ are driven by the input data. (*Id.*) *Ogawa* discloses this feature as discussed below.

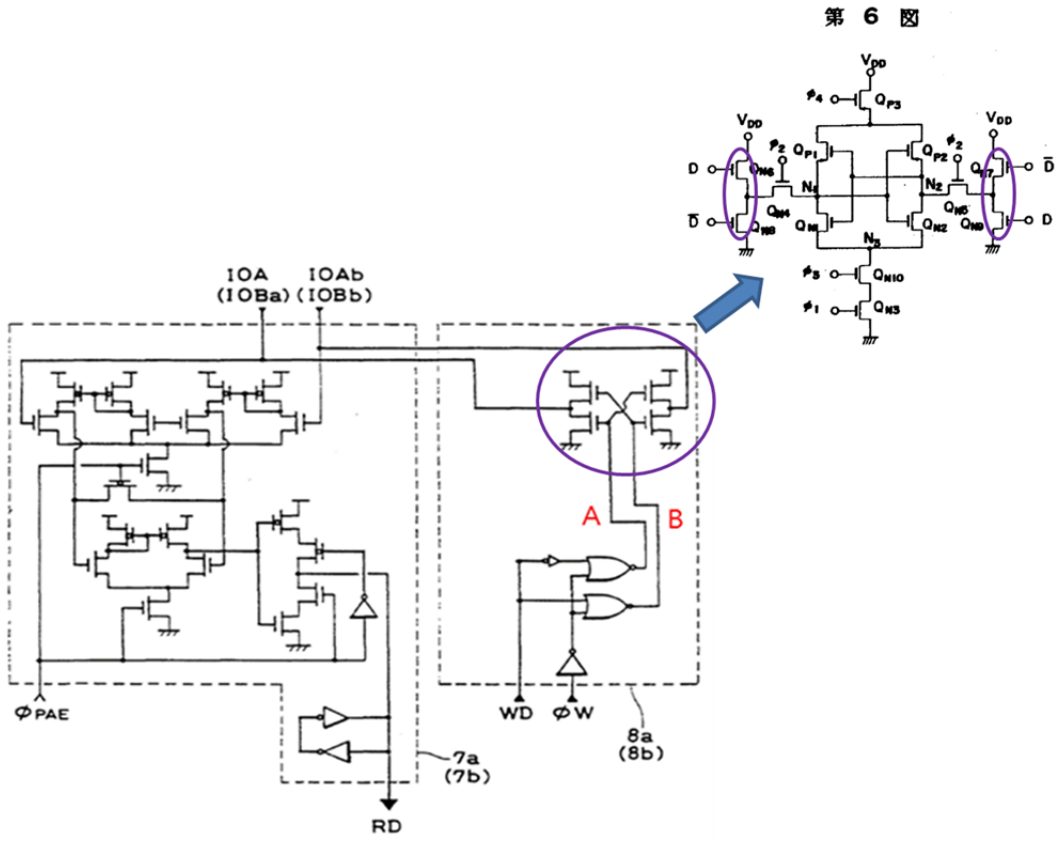
Ogawa discloses that the input data for writing to the latch is provided along I/O buses IOA or IOB. (Ex. 1006, 8:1-4, FIG. 2.)



(Ex. 1002, ¶147, citing Ex. 1006, FIG. 2 (annotated).)

The data on I/O buses IOA and IOB is generated by a write driver 8a (8b). (Ex. 1006, 7:66-8:4, FIG. 5.) The circuitry in the lower half (*i.e.*, the two NOR gates and inverter) of write driver 8a and 8b provides the inputs (annotated as "A" and "B" below) to the data write circuits (the 4 NMOS transistors in the top half of 8a) based on input data. (Ex. 1006, FIG. 5, 8:59-62.) The correspondence between

Inoue's data input buffer transistors Q_{N6}-Q_{N9} (Ex. 1005, 4) and *Ogawa*'s data write circuits (the 4 NMOS transistors in the top half of 8a) is illustrated in figure 5 below that includes *Inoue*'s figure 6. (Ex. 1002, ¶148.) A POSITA would have understood that "A" and "B" (as shown below) would correspond to D and $\overline{D}$ in figure 6 of *Inoue* when combined.



(Ex. 1002, ¶148, citing Ex. 1006, FIG. 5 (annotated) with superimposed Ex. 1005, FIG. 6 (annotated).)

Based on the figure 5 configuration of *Ogawa*, the signals indicated by "A" and "B" would have the following values based on the values of write data WD and ϕW:

WD	ϕW	A	B
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

(Ex. 1002, ¶149; Ex. 1006, 8:59-62.)

As seen from the table, when ϕW is low, which a POSITA would have understood means that no write is to occur, A and B (*i.e.*, the signals corresponding to D and $\overline{D}$ in Inoue) have the same value ('0'). (Ex. 1002, ¶150.)

In view of *Ogawa*, a POSITA would have been motivated to modify *Inoue* to include first and second signals that are controlled to have a same value when no write is to occur to a memory cell for the sense amplifier. (*Id.*, ¶151.) Both *Inoue* and *Ogawa* relate to semiconductor memory devices including sense amplifiers for memory cells. (*Id.*) Accordingly, a POSITA would have looked to *Ogawa* to refine the teachings of *Inoue*, *e.g.*, regarding setting values for signals in *Inoue*. (*Id.*) Having looked to *Ogawa*, a POSITA would have found the above modification obvious for at least the following reasons.

First, combining the teachings of *Inoue* and *Ogawa* constitutes no more than a combination of familiar elements by known methods where the combined

elements continue to perform the same function they did separately. (Ex. 1002, ¶152.) *KSR*, 550 U.S. at 416. *Inoue* discloses that D and $\overline{D}$ (the data write terminals) control writing of data into the sense amplifier latch. But *Inoue* does not disclose how input data (*e.g.*, from an I/O line) is presented to D and $\overline{D}$. Accordingly, the addition of circuitry from *Ogawa*, which performs the same function of generating data write signals, to *Inoue*'s circuit constitutes a combination of known elements where the known elements perform the same functions they did prior to their combination. (Ex. 1002, ¶152.) In the combined system, the data write signals have the same value ('0') when no write is to occur. (*Id.*)

Second, the combination of *Ogawa* with *Inoue* would have reduced erroneous data writes into the latch. (*Id.*) For instance, in *Inoue*, data can only be written to the latch when clock ϕ_2 goes high. (Ex. 1005, 3.) But if the metal line that carries ϕ_2 in the DRAM is shared between many sense amplifiers or if ϕ_2 becomes high due to transients on neighboring metal lines, data can be written out of turn into the latch based on the voltages at D and $\overline{D}$. (Ex. 1002, ¶153.) For example, if D is high and $\overline{D}$ is low, and ϕ_2 goes high out of turn or otherwise, the latch (specifically, node N1) will change state to store a 1 if it previously stored a 0. (*Id.*) Such problems can be avoided by shutting off Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} when the latch does not have to be written to, which is exactly what *Ogawa* does by

controlling ϕW to be a 0 when no writing is to occur. (*Id.*) A POSITA would have recognized this benefit associated with modifying *Inoue* in view of the teachings of *Ogawa*, and therefore would have been motivated to make the modification. (*Id.*) *KSR*, 550 U.S. at 401.

8. Claim 19

a) "The sense amplifier arrangement of claim 18 wherein said first and second data write signals are controlled to have a same value when no write is to occur to a memory cell for the sense amplifier."

Inoue in combination with *Ogawa* discloses or suggests this feature for the reasons discussed above for claim 17. (Ex. 1002, ¶154.) (*See supra* Section IX.B.7.)

9. Claim 37

a) "The sense amplifier arrangement according to claim 36 wherein said coupling transistor is responsively coupled to a column control signal."

Inoue in combination with *Ogawa* discloses or suggests this feature. (Ex. 1002, ¶155.) As discussed above regarding claim 36, *Inoue* discloses transistors Q_{N4} and Q_{N5}, each of which is a "coupling transistor." (Section IX.A.13.) As further discussed above for claim 4, in the combined *Inoue*-*Ogawa* system, the write control clock ϕ_2 provided to transistors Q_{N4} and Q_{N5} controls writing of a particular column of the memory cell array. (*See* Section IX.B.1.) Therefore, the modified write control clock ϕ_2 is a "column control signal." (Ex. 1002, ¶155.)

Moreover, Q_{N4} and Q_{N5} are "responsively coupled" to write control clock ϕ_2 ("column control signal") because clock ϕ_2 turns transistors Q_{N4} and Q_{N5} ON or OFF. (Ex. 1005, 3, "clock ϕ_2 is allowed to rise, thereby causing Q_{N4} and Q_{N5} to be conducting"; *see also id.*, FIG. 6.)

10. Claim 39

a) "The sense amplifier arrangement according to claim 38 wherein said coupling transistor is responsively coupled to a column control signal."

Inoue in combination with *Ogawa* discloses or suggests this feature for the reasons discussed above for claim 37. (Ex. 1002, ¶156; *supra* Section IX.B.9.)

C. Ground 3: *Inoue, Ogawa,* and *Okamura* Render Obvious Claims 7 and 15

1. Claim 7

a) "The sense amplifier arrangement according to claim 6 wherein said decoded column write signal is decoded for four columns of said memory."

Inoue in combination with *Ogawa* and *Okamura* discloses or suggests this feature. (Ex. 1002, ¶¶157-163.) The *Inoue-Ogawa* combination discloses a DRAM with a plurality of columns and a decoded column write signal that is used to select one column among the plurality of columns. (*See* Sections IX.B.1, IX.B.3.) The *Inoue-Ogawa* combination does not, however, explicitly disclose that the decoded column write signal is decoded for "four columns of said memory." It

would have been obvious to a POSITA to modify the *Inoue-Ogawa* combination to include this feature in view of *Okamura*. (Ex. 1002, ¶157-158.)

Okamura discloses a sense amplifier design for a DRAM. (Ex. 1007, Abstract.) The architecture of *Okamura*'s design is illustrated in figure 3.

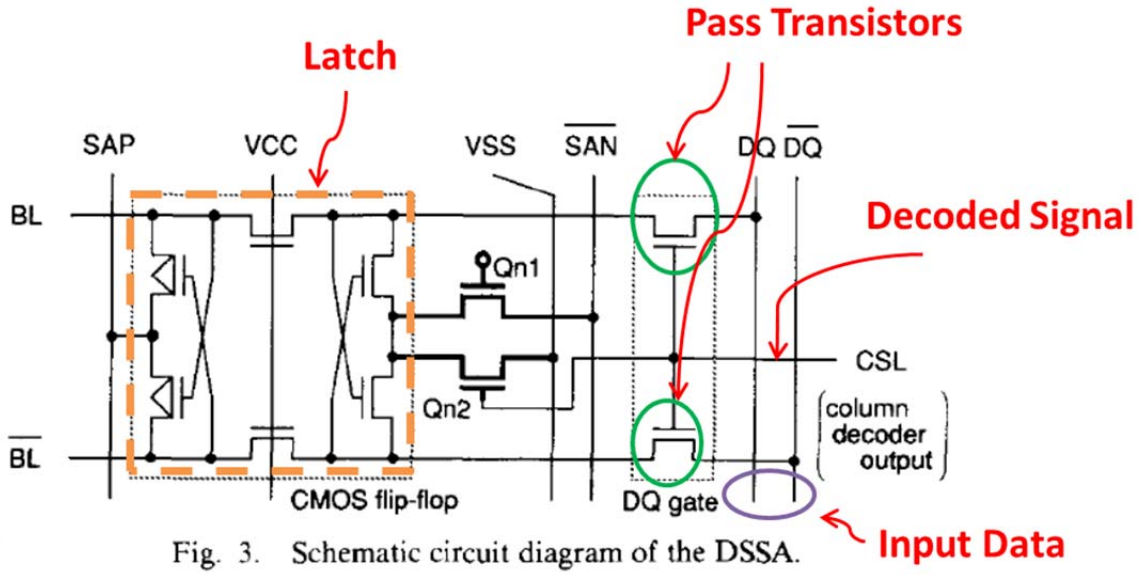


Fig. 3. Schematic circuit diagram of the DSSA.

(Ex. 1002, ¶159, citing Ex. 1007, FIG. 3 (annotated).)

A "DQ pair" (illustrated as DQ and $\overline{DQ}$) is connected to the sense amplifier and the bit lines of a column based on a column decoder output labelled "CSL" ("decoded column write control signal") provided to the two DQ gates, which a POSITA would have understood to correspond to the claimed "pass transistors." (Ex. 1002, ¶160; Ex. 1007, 20, "[The Decoded-Source Sense Amplifier], when accessed by CSL, drastically amplifies the bit-line signal and strongly drives the DQ pair.") *Okamura* further discloses that the CSL is decoded for four columns

("decoded for four columns of said memory") because it discloses "partial decoding" in which "four columns [are] selected by the same CSL." (Ex. 1007, 22.)

A POSITA would have looked to *Okamura* to refine the teachings of the *Inoue-Ogawa* combination because the references disclose sense amplifier configurations and related techniques. (Ex. 1002, ¶161.) Having looked to *Okamura*, a POSITA would have been motivated to modify the decoded column write signal in the *Inoue-Ogawa* combination such that the decoded signal selects four columns at a given time for several reasons. (*Id.*)

Using a single decoded signal to access more than one column was a well-known technique that was used to reduce the number of address pins while increasing the word size written to, or read from, the memory. (*Id.*, ¶¶162-163.) Without this technique, a single column address output by a decoder would correspond to 1-bit of memory. (*Id.*) As a result, accessing four bits of memory would require accessing the memory four times. (*Id.*) The modified system would have allowed the same decoded signal to access four columns at the same time, allowing four bits of data to be concurrently written to. (*Id.*) Moreover, using a single decoded address signal to access multiple columns would have resulted in fewer address pins on the decoder because more columns may be accessed with the

same number of address pins on the decoder. (*Id.*) Accordingly, a POSITA would have found the above modification obvious. *See KSR*, 550 U.S. at 401.

2. Claim 15

a) "The sense amplifier arrangement according to claim 14 wherein said decoded column write signal is decoded for four columns of said memory."

Inoue in combination with *Ogawa* and *Okamura* discloses or suggests this feature for the reasons discussed above for claim 7. (Ex. 1002, ¶164; *supra* Section IX.C.1.)

D. Ground 4: *Inoue* Renders Obvious Claims 16 and 18

Claim 16 depends from independent claim 11, and claim 18 depends from depends from claims 9, 8, 2, and independent clam 1. Thus, Petitioner demonstrates below how *Inoue* discloses the limitations of claims 1, 2, 8, 9, and 11 (Sections IX.D.1-D.5) before addressing the limitations of claims 16 and 18 (Sections IX.D.6-D.7). The analysis in this section is based on the disclosure of FIG. 3 of *Inoue* in combination with FIG. 6, in part because FIG. 3 of *Inoue* explicitly discloses the "active memory block" limitation of claims 16 and 18, as discussed below. Because the disclosure of FIG. 6 (as discussed above) builds on the circuits disclosed in FIGS. 1, 3, and 4 of *Inoue*, the analysis in this section overlaps with the analysis above in section IX.A. (Ex. 1002, ¶¶165-166.) When describing the operation and composition of FIG. 3, *Inoue* does not repeat the

details it previously discusses for common aspects between FIGS. 1 and 3. (*See* Ex. 1005, 3.) Therefore, in this section the common aspects of FIGS. 1, 2, and 3 of *Inoue* are referenced when describing the configuration of FIG. 3.

1. Claim 1[8]

a) Claim Element 1(a)

To the extent the preamble is limiting, *Inoue* discloses or suggests this feature. (Ex. 1002, ¶¶167-172.) Figure 3 of *Inoue* discloses a CMOS flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}. (Ex. 1005, 3, FIG. 3.) *Inoue* discloses in figure 1, N-channel transistors Q_{N1}, Q_{N2} that constitute a flip-flop and that "FIG. 3 illustrates an example of a CMOS F/F" similar to FIG. 1 except that the F/F also includes "P-channel transistors Q_{P1}, Q_{P2}" in addition to the N-channel transistors Q_{N1}, Q_{N2}. (*Id.*, 3, FIGS. 1, 3.) The flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2} would have been readily recognized by a skilled person as a "sense amplifier." (Ex. 1002, ¶67.) The '270 patent confirms this understanding because it shows the same configuration that was known for a "sense amplifier." (*Compare* Ex. 1005, FIG. 3 (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}), *with* Ex. 1001, 1:47-62, FIG. 1, illustrating "sense amplifier 10" that includes P-Channel transistors 12, 14 and N-Channel transistors 18, 20.)

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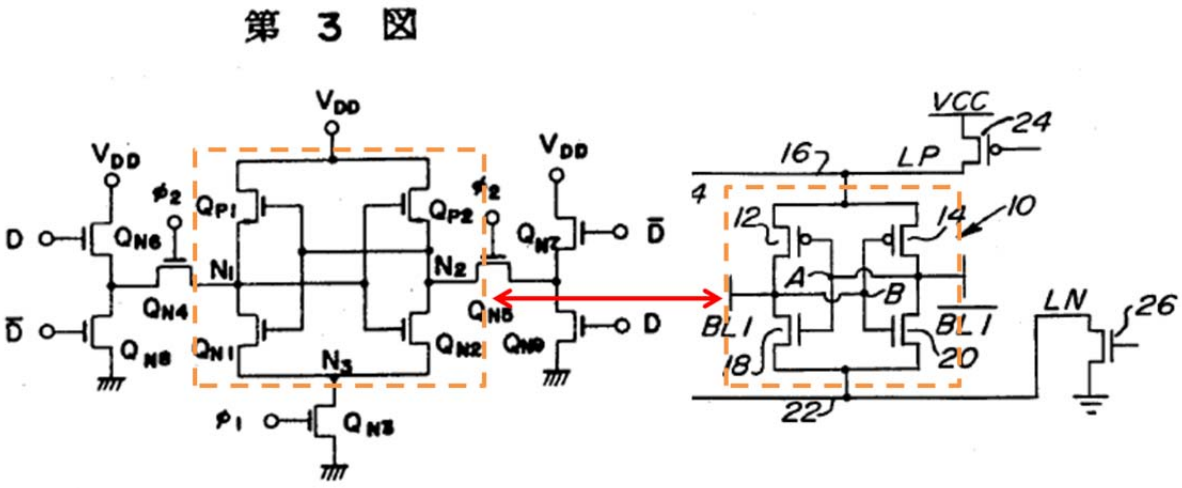
[8] The limitations of claims 1, 2, 8, 9, and 11 are provided above in ground 1 (Section IX.A) and are not repeated here.



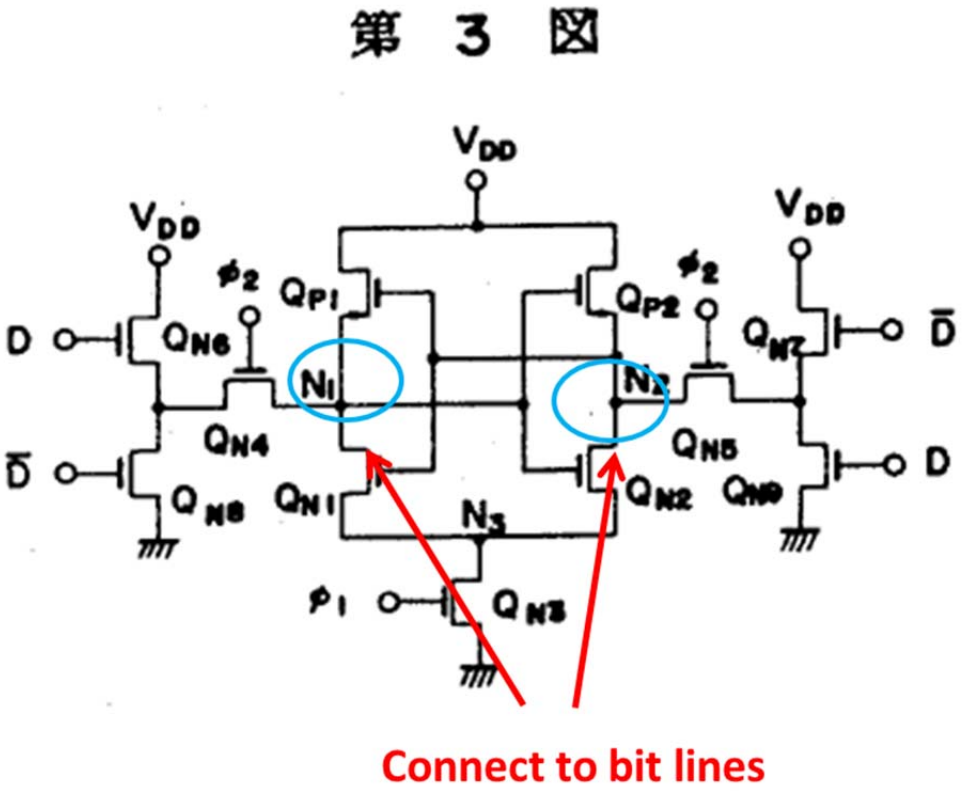
Inoue, FIG. 3 '270 Patent, FIG. 1 (excerpt)

(Ex. 1002, ¶167, citing Ex. 1005, FIG. 3 (annotated), Ex. 1001, FIG. 1 (annotated).) Accordingly, figure 3 of *Inoue* discloses a "sense amplifier arrangement" (e.g., flip-flop (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) that a POSITA would have recognized as a "sense amplifier.") (Ex. 1002, ¶168.)

Figure 3 of *Inoue*, however, does not explicitly disclose that the sense amplifier "is for an integrated circuit memory." But figure 6 of *Inoue* discloses that the same flip-flop configuration as figure 3 can be applied to "a sense amp in . . . dynamic memory." (Ex. 1005, 4, FIG. 6.) For instance, figure 6 discloses the same configuration as figure 3 except for the addition of transistors QP3 and QN10 above and below the flip-flop circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}). (*Compare id.*, FIG. 3, *with id.*, FIG. 6.) *Inoue* also discloses that the circuit of figure 6 can be "applied to a sense amp in the dynamic memory" where "for example, N_1 and N_2 correspond

to bit lines." (*Id.*, 4.) Therefore, figure 6 discloses a flip-flop circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) that is a "sense amplifier" for an "integrated circuit memory" because a POSITA would have understood that "dynamic memory" in *Inoue* refers to a DRAM, which is a type of integrated circuit memory. (Ex. 1002, ¶169; *see also* Section VII.A.)

In view of figure 6 in *Inoue*, a POSITA would have found it obvious to utilize the sense amplifier configuration disclosed in figure 3 in a DRAM, which is a type of "integrated circuit memory." (Ex. 1002, ¶170.) For instance, a POSITA would have been motivated to combine the teachings of figures 3 and 6 in *Inoue* such that nodes N1 and N2 in figure 3 also correspond to bit lines of a DRAM like nodes N1 and N2 in figure 6 in *Inoue*. (*Id.*; Ex. 1005, FIG. 3.)



(Ex. 1002, ¶170, citing Ex. 1005, FIG. 3 (annotated to show the modification of figure 3 based on figure 6).)

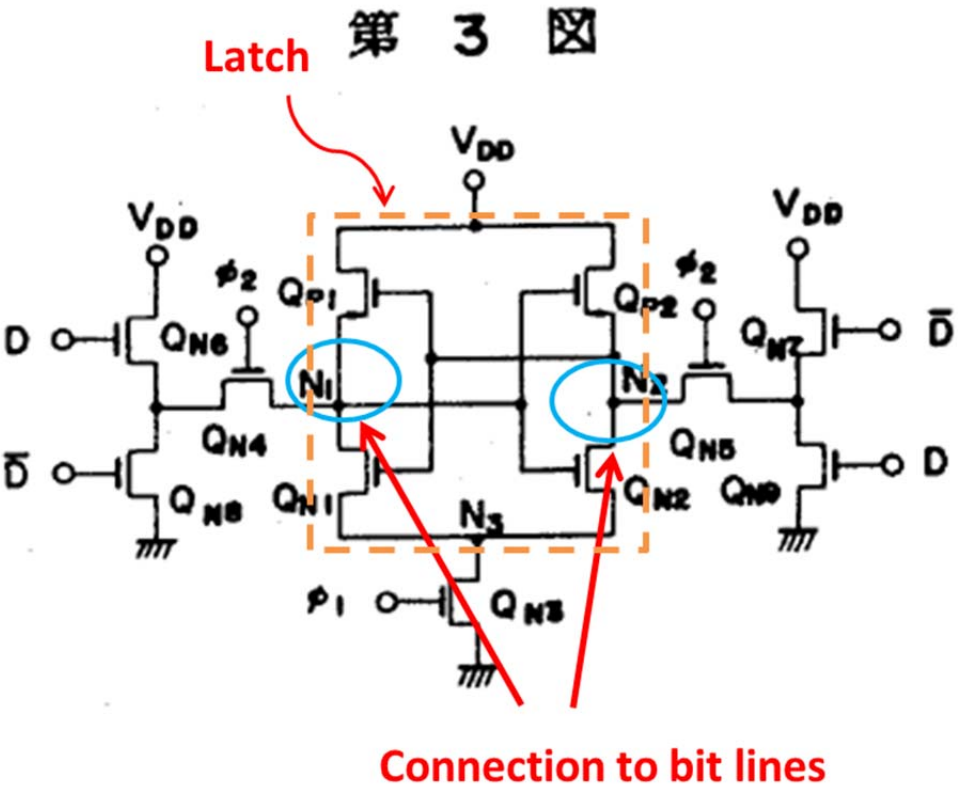
The above modification would have allowed the figure 3 circuit to be used for reading and writing data to memory cells of a DRAM, thereby enhancing the utility of the circuit of figure 3. (Ex. 1002, ¶171.) Indeed, this conventional function of a sense amplifier is recognized by the '270 patent as being well-known at the time of the alleged invention. (Ex. 1001, 1:37-46.)

Furthermore, a POSITA would have recognized that the above modification would have been merely the result of combining prior art elements (*e.g.*, *Inoue*'s

figure 3 circuit and bit lines coupled to N1, N2 in figure 3) according to known methods (*e.g.*, connecting N1, N2 in figure 3 to bit lines in a DRAM) to yield predictable results (*e.g.*, sensing and amplifying of data read and written to memory cell by the sense amplifier of figure 3). (Ex. 1002, ¶172.) *KSR*, 550 U.S. at 416.

b) Claim Element 1(b)

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶173-175.) For example, *Inoue* discloses a CMOS flip-flop comprising transistors Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}. (Ex. 1005, 3, FIG. 3; Section IX.D.1(a).) As discussed above, a flip-flop is a "latch circuit." (*Supra* Section IX.A.1(b).) Moreover, as discussed above, the flip-flop (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) ("latch circuit") of figure 3 modified based on figure 6 has internal nodes N1 and N2 that are coupled to bit lines. (Section IX.D.1(a).)

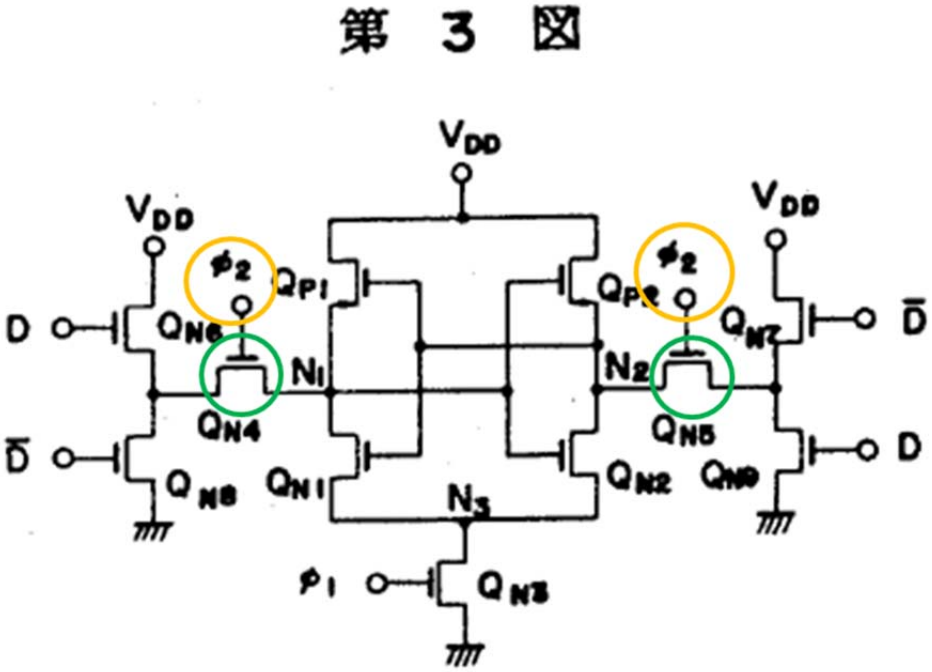


(Ex. 1002, ¶174, citing Ex. 1005, FIG. 3 (annotated to show internal nodes (blue) of the latch circuit (orange).)

c) Claim Element 1(c)

Inoue discloses or suggests this feature for reasons similar to those discussed above in Section IX.A.1(c) for claim element 1(c). (Ex. 1002, ¶¶176-178; Section IX.A.1(c).) *Inoue* discloses transistors Q_{N4} and Q_{N5} ("a pair of pass transistors") each coupled to respective one of N_1 or N_2 ("a respective one of said internal nodes"), Q_{N4} and Q_{N5} ("the pair of pass transistors") having a gate terminal ("a

control electrode") coupled to receive write control clock ϕ_2 ("a first control signal"). (Ex. 1005, 3, FIG. 3.)

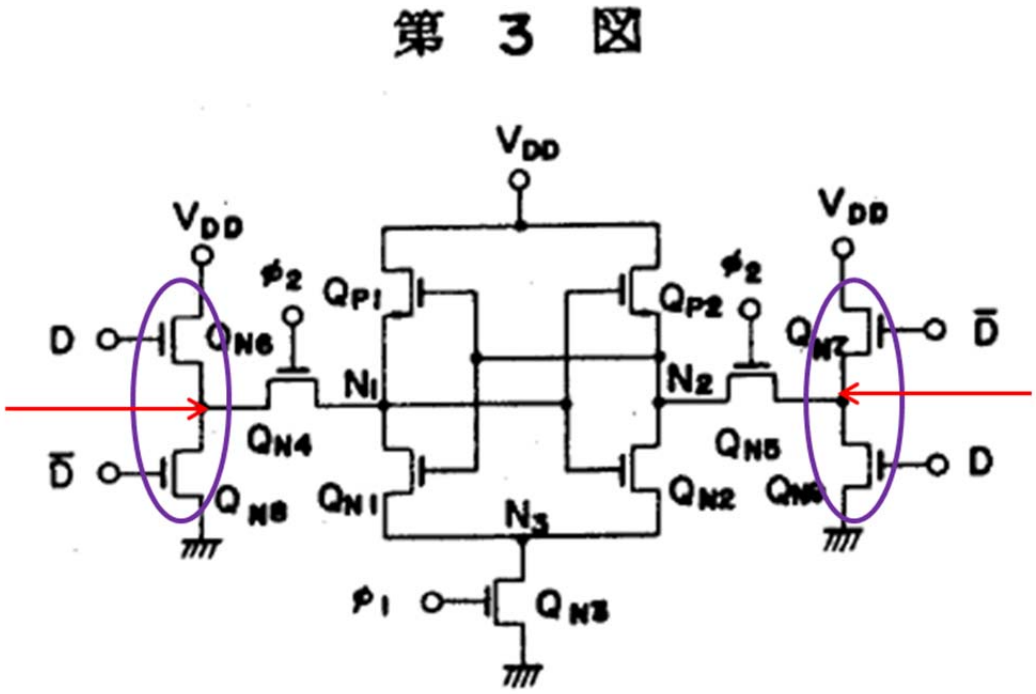


(Ex. 1002, ¶178, citing Ex. 1005, FIG. 3 (annotated to show a pair of pass transistors (green) with their control electrodes (orange).)

d) Claim Element 1(d)

Inoue discloses or suggests this feature for reasons similar to those discussed above for claim element 1(d). (Ex. 1002, ¶¶179-182; Section IX.A.1(d).) *Inoue* discloses two data write circuits: Q_{N6} and $Q_{N8,}$ and Q_{N7} and Q_{N9} ("a pair of local data write driver circuits") that are associated with only a single latch circuit (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}). (Ex. 1005, 3, FIG. 3.) The gates ("control electrodes") of Q_{N6} and

$Q_{N8,}$ and Q_{N7} and Q_{N9} are coupled to receive the signals at write data input terminals D and $\overline{D}$ ("second write control signals") that write to nodes N_1 and N_2 ("receive second write control signals for data write operations and to provide a pair of data write output signals"). (Ex. 1005, 3, FIG. 3.)

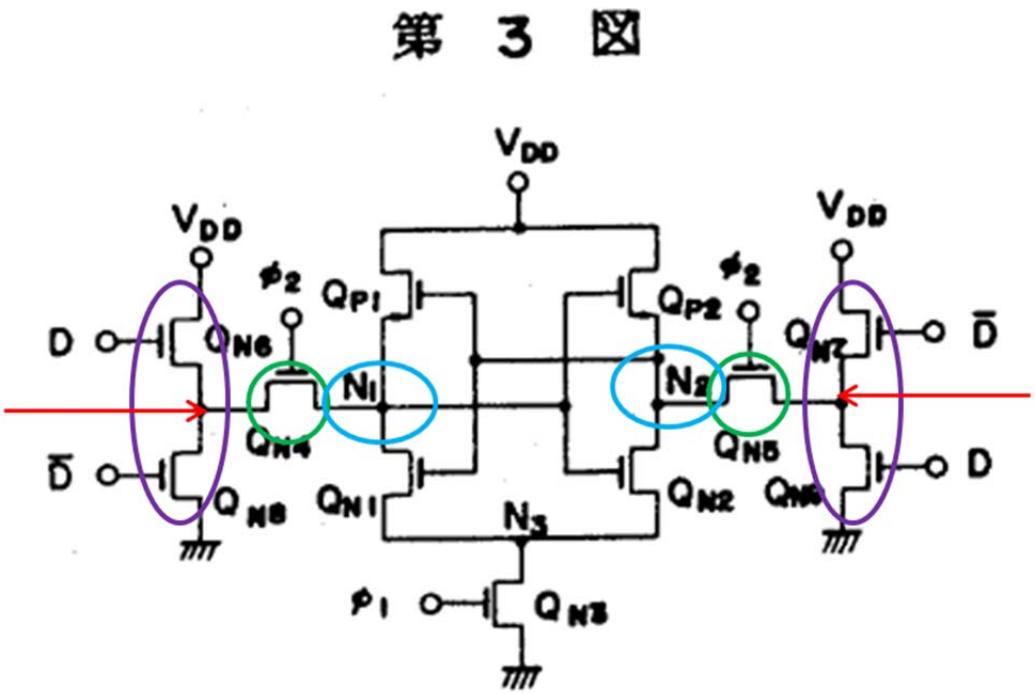


(Ex. 1002, ¶183, citing Ex. 1005, FIG. 3 (annotated to show local data write driver circuits (purple) and an output (red arrow).)

e) Claim Element 1(e)

Inoue discloses or suggests this feature for reasons similar to those discussed above for claim element 1(e). (Ex. 1002, ¶¶183-185; Section IX.A.1(e).) *Inoue*

discloses that Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("each local data write driver circuit") are coupled to Q_{N4} and $Q_{N5,}$ respectively ("its corresponding pass transistor"), so that Q_{N4} or Q_{N5} when conductive, couples the output signal from Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} to N_1 or N_2, which as discussed above are connected to bit lines in the modified figure 3 circuit ("the corresponding internal node of the latch circuit and to a corresponding bit line"). (Ex. 1005, 3, FIG. 3; Section IX.D.1(a).)

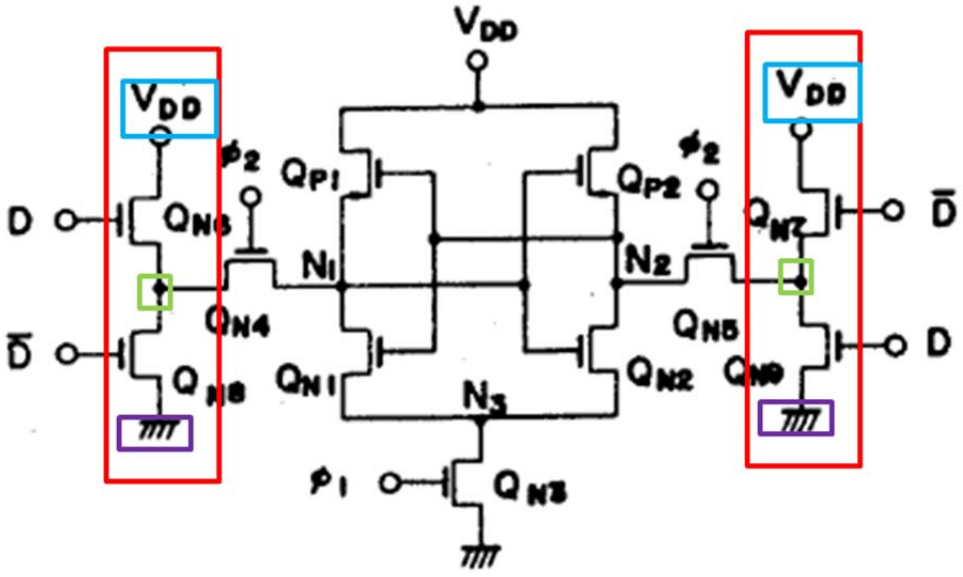


(Ex. 1002, ¶185, citing Ex. 1005, FIG. 3 (annotated to show that the output (red arrow) of local data write driver circuits (purple) are connected to respective nodes N1, N2 (blue) through corresponding pass transistors (green).)

2. Claim 2

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶186-188; Section IX.A.2.) *Inoue* discloses write circuits Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("each of said local data write driver circuits"), each of which is comprised by Q_{N6} or Q_{N7} ("a pull-up transistor") and Q_{N8} or Q_{N9} ("a pull-down transistor") having their source-drain paths coupled in series (red below) and forming an output node therebetween (green below), the output node being coupled to the corresponding pass transistor Q_{N4} or Q_{N5}, the source-drain paths being coupled between V_{DD} (blue below) and GND (purple below) ("first and second voltages"). (*See* Ex. 1005, 3, FIG. 3.)

第 3 図

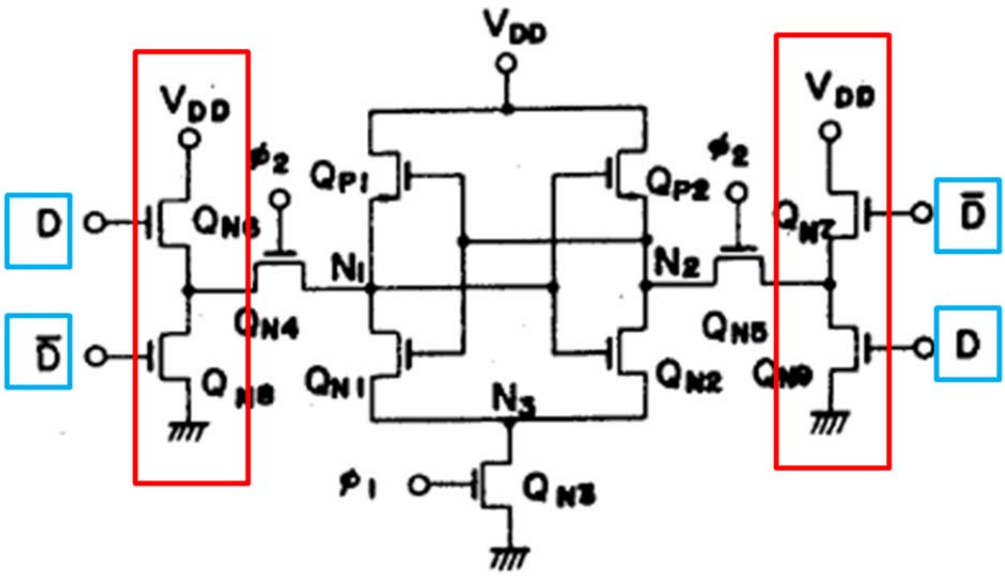


(Ex. 1002, ¶188, citing Ex. 1005, FIG. 3 (annotated).)

3. Claim 8

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶189-190; Section IX.A.4.) *Inoue* discloses that Q_{N6}/ Q_{N8} and Q_{N7}/Q_{N9} ("said local data write driver circuits") receive write signals D and $\overline{D}$ ("said second write control signals") at the gates ("control terminals") of Q_{N6} or Q_{N7} ("said pull-up transistors") and Q_{N8} or Q_{N9} ("said pull-down transistors"). (Ex. 1005, 3, FIG. 3.)

第 3 図



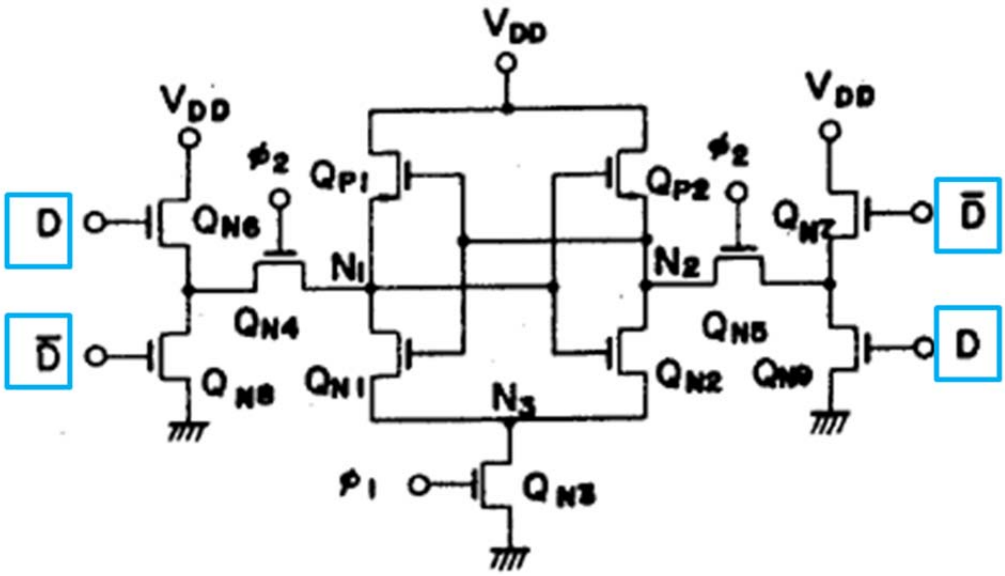
(Ex. 1001, ¶190, citing Ex. 1005, FIG. 3 (annotated).)

4. Claim 9

a) Claim Element 9(a)

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶191-192; Section IX.A.5(a).) *Inoue* discloses that signals D, $\overline{D}$ ("said second write control signals") comprise a signal at write data input terminal D ("first . . . data write signal[]") and a signal at write data input terminal $\overline{D}$ ("second data write signal[]"). (Ex. 1005, 3, FIG. 3.)

第 3 図



(Ex. 1002, ¶191, citing Ex. 1005, FIG. 3 (annotated to show that the second write control signals (blue) include first and second data write signals at D, $\overline{D}$, respectively).)

b) Claim Element 9(b)

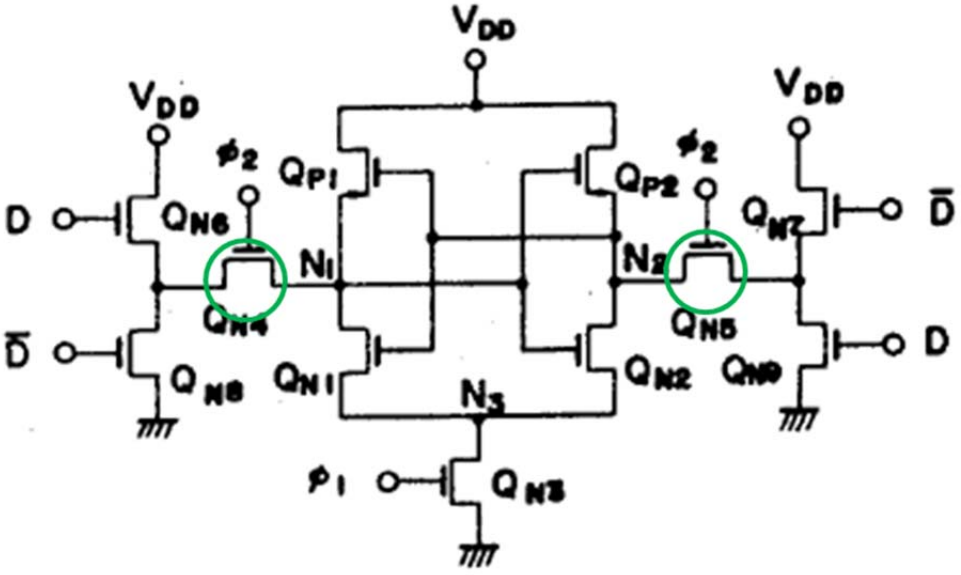
Inoue discloses or suggests this feature. (Ex. 1002, ¶193.) *Inoue* discloses that Q_{N6} ("one said pull-up transistor in the local data write driver circuits for the corresponding latch circuit") receives the signal at terminal D ("the first data write signal") and Q_{N7} ("the other said pull-up transistor") receives the signal at terminal $\overline{D}$ ("second data write signal"). (Ex. 1005, FIG. 3.)

5. Claim 11

a) Claim Elements 11(a), 11(b), 11(c)

Inoue discloses or suggests the features of these claim elements for reasons similar for claim elements 1(a), 1(b), 1(c), respectively. (Ex. 1002, ¶¶194-197; Sections IX.D.1(a)-D.1(c).) (*See also* Ex. 1005, FIG. 3 (Q_{N4} ("first") and Q_{N5} ("second") pass transistors (green below))

第 3 図

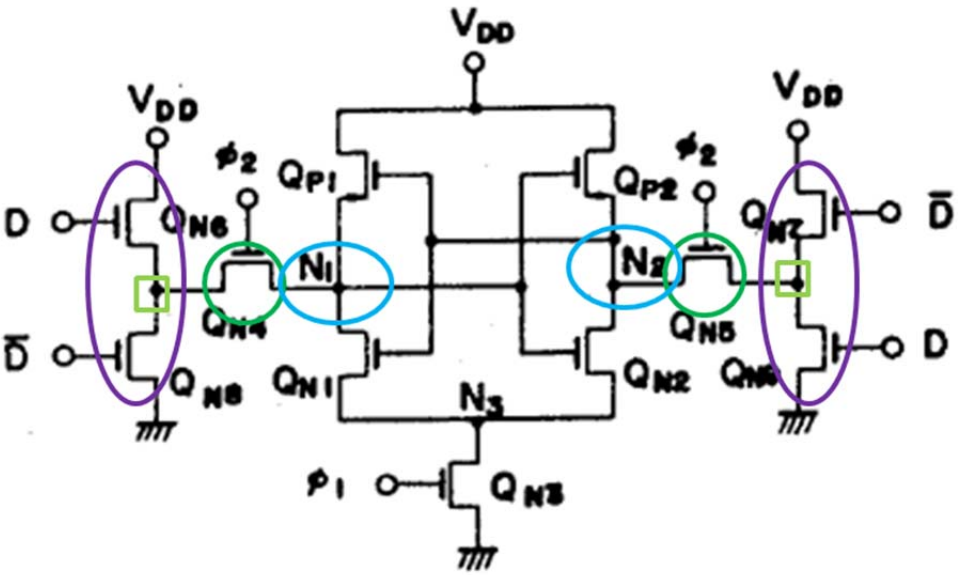


(Ex. 1002, ¶197, Ex. 1005, FIG. 3 (annotated)

b) Claim Element 11(d)

Inoue discloses or suggests this feature for reasons similar for claim element 1(d). (Ex. 1002, ¶¶199-201; Section IX.A.7(d); Ex. 1005, 3, FIG. 3.)

第 3 図

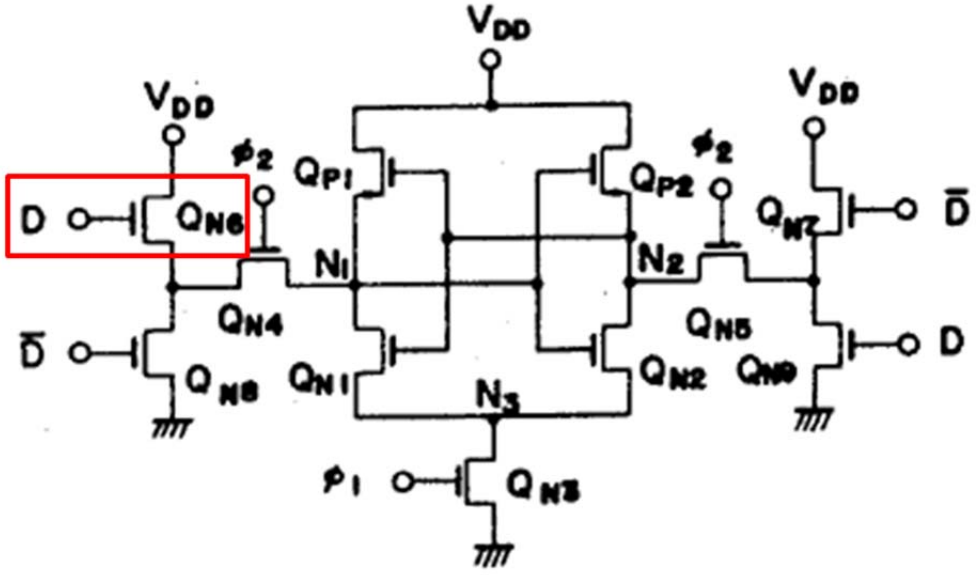


(Ex. 1002, ¶200, citing Ex. 1005, FIG. 3 (annotated to show that the output node (light green) of local data write driver circuits (purple) are selectively connected to respective nodes N1, N2 (blue) through corresponding pass transistors (dark green).)

c) Claim Element 11(e)

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶202-203.) As discussed above in Section IX.A.7(e), Q_{N6} ("said first transistor") of Q_{N6}/Q_{N8} ("said first local data write driver circuit") has a gate terminal ("control electrode") connected to receive a signal at terminal D ("a first data write signal").

第 3 図

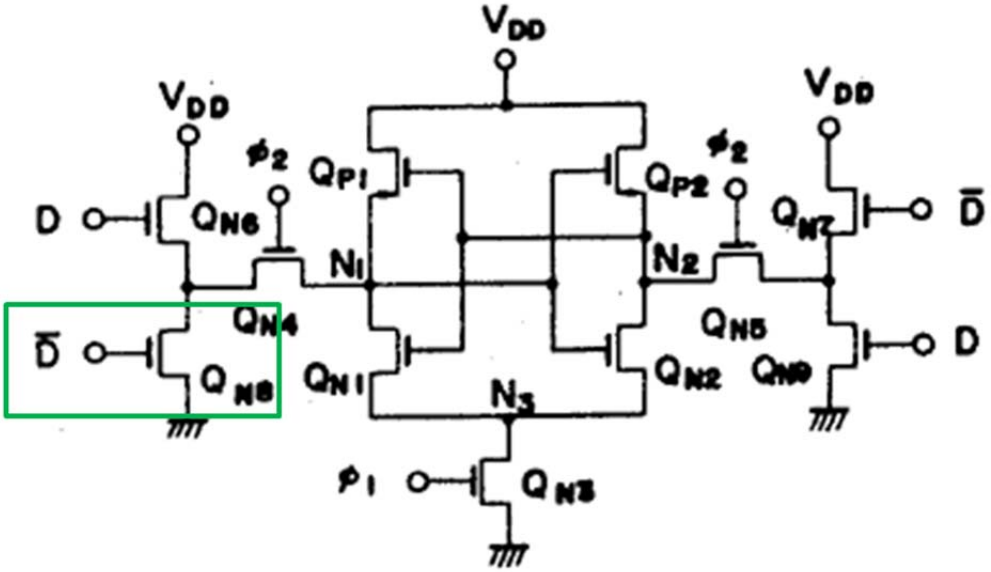


(Ex. 1002, ¶203, citing Ex. 1005, FIG. 3 (annotated).)

d) Claim Element 11(f)

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶204-206.) As discussed above in Section IX.A.7(f), *Inoue* discloses Q_{N8} ("said second transistor") of Q_{N6} /Q_{N8} ("said first local data write driver circuit") has a gate terminal ("control electrode") connected to receive a signal at write data input terminal $\overline{D}$ ("a second data write signal").

第 3 図

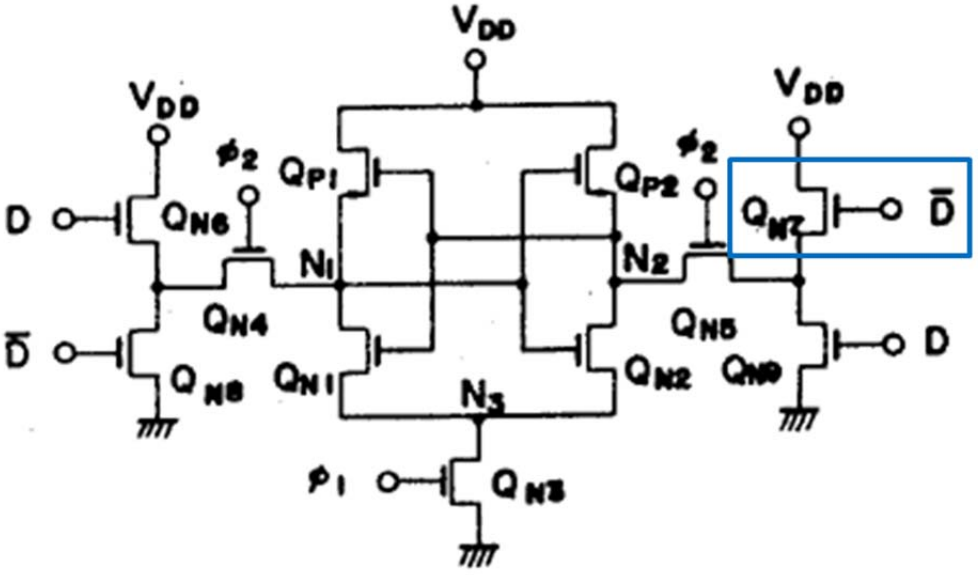


(Ex. 1002, ¶204, citing Ex. 1005, FIG. 3 (annotated).)

e) Claim Element 11(g)

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶206-207.) As discussed above in Section IX.A.7(g), Q_{N7} ("said first transistor") of Q_{N7}/Q_{N9} ("said second local data write driver circuit") has a gate terminal ("control electrode") connected to receive a signal at write data input terminal $\overline{D}$ ("second data write signal").

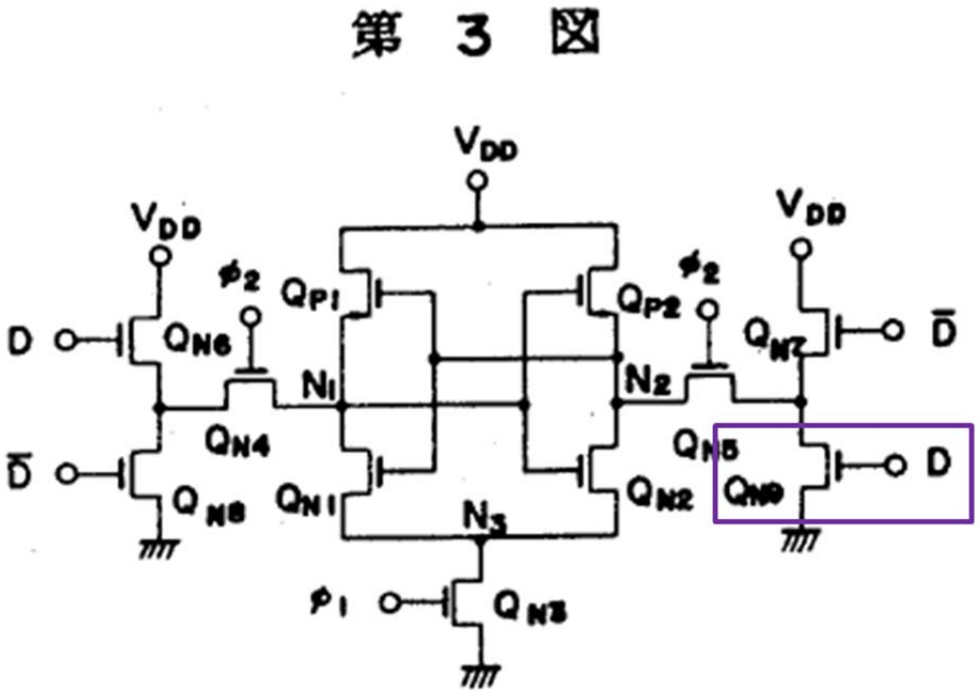
第 3 図



(Ex. 1002, ¶206, citing Ex. 1005, FIG. 3 (annotated).)

f) Claim Element 11(h)

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶208-209.) As discussed above in Section IX.A.7(h), Q_{N9} ("said second transistor") of Q_{N7} /Q_{N9} ("said second local data write driver circuit") has a gate ("control electrode") connected to receive a signal at write data input terminal D ("said first data write signal").



(Ex. 1002, ¶208, citing Ex. 1005, FIG. 3 (annotated).)

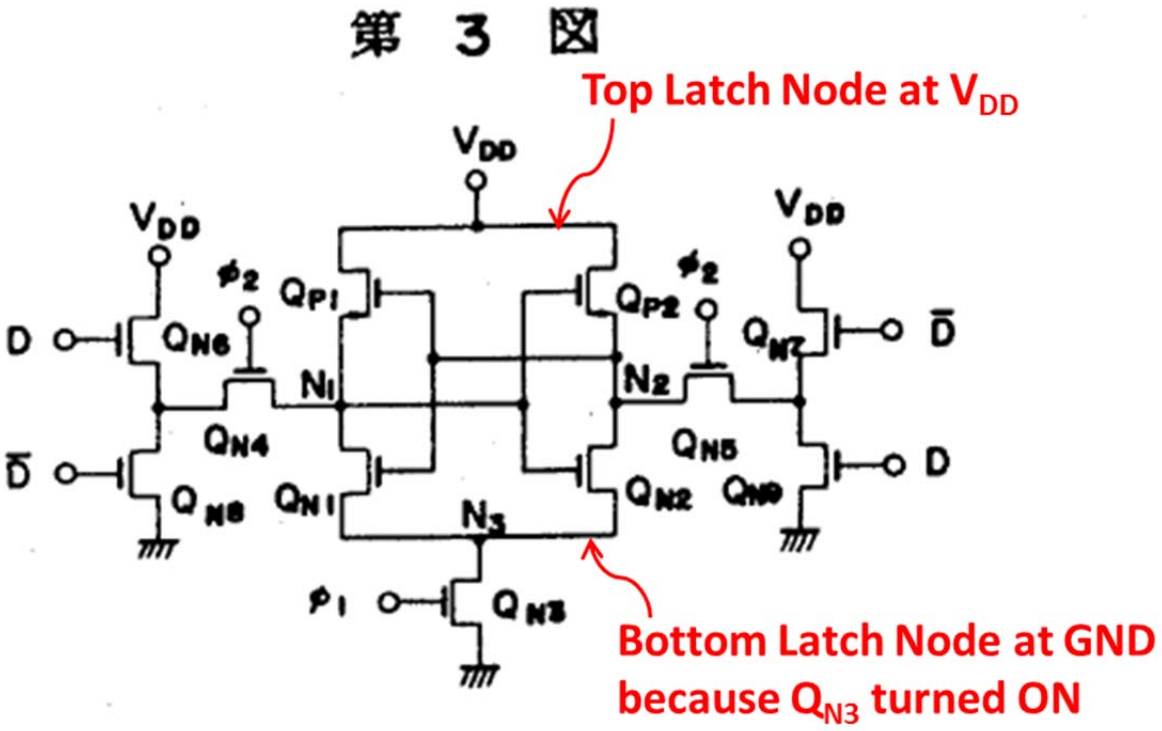
6. Claim 16

a) "The sense amplifier arrangement of claim 11 wherein said first and second data write signals are complementary signals for writing data into an active memory block."

Inoue discloses or suggests this feature. (Ex. 1002, ¶¶210-212.) *Inoue* discloses that the circuit of figure 3 operates in a manner similar to figure 1. (Ex. 1005, 3.) *Inoue* discloses with respect to figure 1, which also applies to figure 3, that the signals at write data input terminal D ("said first data write signal") and

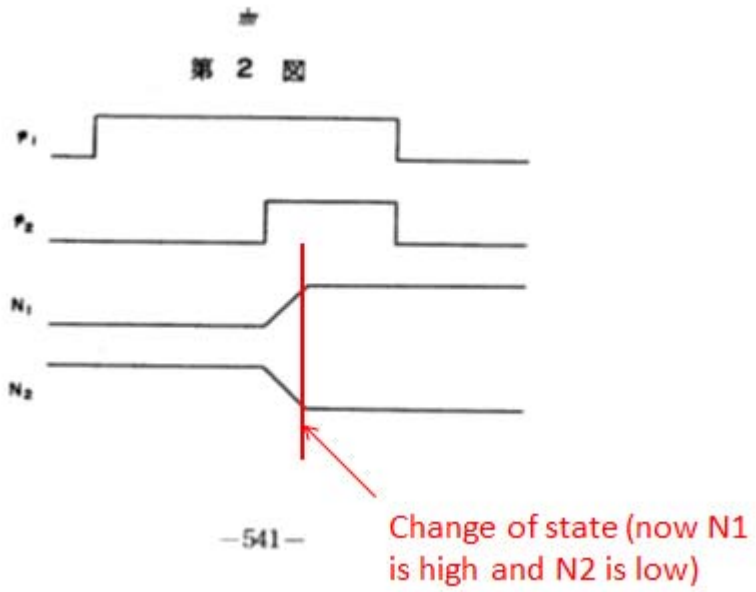
write data input terminal $\overline{D}$ ("second data write signal") are complementary signals at the time of writing because when D is a high, $\overline{D}$ is a low. (*Id.*)

Furthermore, *Inoue* discloses that when data is written to nodes N1 and N2, the latch (Q_{P1}, Q_{P2}, Q_{N1}, Q_{N2}) is active, *i.e.*, D and $\overline{D}$ are complementary signals for writing data "into an active memory block." (Ex. 1002, ¶211.) According to the '270 patent, an active memory block refers to a latch circuit whose top and bottom nodes are connected to Vcc and GND, respectively. (Ex. 1001, 4:32-34, 6:24-26, FIG. 4.) In *Inoue*, when node N1 transitions from state I ("L") to state II ("H"), *i.e.*, during writing, the top latch node (see below) and the bottom latch node (see below) are at VDD and GND, respectively. (Ex. 1005, 3, during "transition from state I to state II" N_3 is at GND, FIG. 3.)



(Ex. 1002, ¶211, citing Ex. 1005, FIG. 3 (annotated).)

Figure 2 confirms that when N1 and N2 change state, Q_{N3} is turned ON because ϕ_1 is high ("H"), which indicates that node N_3 is pulled down to ground. (Ex. 1002, ¶212; Ex. 1005, FIG. 2.)



(Ex. 1005, FIG. 2; Ex. 1002, ¶212)

7. Claim 18

a) "The sense amplifier arrangement of claim 9 wherein said first and second data write signals are complementary signals for writing data into an active memory block."

Inoue discloses this feature for the reasons discussed above for claim 16.

(Ex. 1002, ¶¶213; Section IX.D.6.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-19, 30-32, and 34-39 of the '270 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: October 7, 2016 By: /Naveen Modi/
Naveen Modi (Reg. No. 46224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,088,270 contains, as measured by the word-processing system used to prepare this paper, 13,806 words. This word count does not include the items excluded by 37 C.F.R. § 42.24(a).

Respectfully submitted,

Dated: October 7, 2016

By: /Naveen Modi/
Naveen Modi (Reg. No. 46224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on October 7, 2016, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,088,270 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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