UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

INNOVATIVE MEMORY SYSTEMS, INC.
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 7,085,159
Title: HIGHLY COMPACT NON-VOLATILE MEMORY AND METHOD THEREFOR WITH INTERNAL SERIAL BUSES

Petition For *Inter Partes* Review of U.S. Patent No. 7,085,159 Under 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

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Patent Trial and Appeal Board
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Micron Exhibit #	Description
MICRON-1001	U.S. Patent No. 7,085,159 ("159 Patent")
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MICRON-1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 6,288,936 ("Kawamura")
MICRON-1006	*IEEE Standard Dictionary of Electrical and Electronics Terms* (1984)

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1, 5, 11, and 12 of U.S. Patent No. 7,085,159, titled "Highly Compact Non-Volatile Memory and Method Therefor With Internal Serial Buses" (MICRON-1001, the "159 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR *INTER PARTES* REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 159 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 159 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Douglas W. McClellan Registration No. 41,183 (doug.mcclellan@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5313; F: 713-224-9511	Jeremy Jason Lang Registration No. 73,604 (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for Petitioner is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Innovative Memory Systems has asserted the 159 Patent and U.S. Patent Nos. 6,169,503 (the "503 Patent"), 6,324,537 (the "537 Patent"), 6,901,498 (the "498 Patent"), 7,000,063 (the "063 Patent"), 7,045,849 (the "849 Patent"), 7,495,953 (the "953 Patent") and 7,886,212 (the "212 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Innovative Memory Systems, Inc., v. Micron Tech., Inc.*, 14-cv-1480 (D. Del.) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 6,169,503, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 6,324,537, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 6,901,498, IPR2016-Unassigned;

Petition for *Inter Partes* Review of U.S. Patent No. 7,000,063, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,045,849, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,495,953, IPR2016-Unassigned; and Petition for *Inter Partes* Review of U.S. Patent No. 7,886,212, IPR2016-Unassigned.[1]

The 159 Patent claims priority to U.S. Patent Application No. 10/254,919, filed on September 24, 2002, which application resulted in U.S. Patent No. 6,891,753. U.S. Patent 7,447,070, resulting from Application No. 11/422,719, filed on June 7, 2006, claims priority to the 159 Patent Application.

2.5. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 159 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Ground #1: Claims 1, 5, 11 (with respect to claims 1 and 5), and 12 (with respect to claims 1 and 5) are invalid under 35 U.S.C. § 102(b) as anticipated by

[1] These petitions will be filed concurrently or within a few days.

U.S. Patent No. 6,288,936 ("Kawamura"), entitled "Nonvolatile Memory For Storing Multivalue Data," filed on December 12, 2000 and issued on September 11, 2001. Kawamura is attached as MICRON-1005. This ground is explained below and is supported by the Declaration of Dr. R. Jacob Baker (MICRON-1003, "Baker Decl.").

4. OVERVIEW OF THE 159 PATENT

The 159 Patent was filed on May 5, 2005 and claims priority to U.S. Patent Application No. 10/254,919, filed on September 24, 2002. The 159 Patent issued on August 1, 2006. The 159 Patent generally relates to non-volatile semiconductor memory wherein memory cells in an array are read and written in parallel. MICRON-1001, 159 Patent at 1:15-20, 9:12-17. Read/write circuits within the memory device are used to read or write (program) the memory states of addressed memory cells. *Id.* at 7:22-26. These circuits consist of a number of modules that are connected by bit lines to memory cells in an array. *Id.*

As the 159 Patent acknowledges, improving read/write operations in non-volatile memory by operating in a parallel manner was well known in the art. *Id.* at 8:15-17, 8:27. Indeed, the 159 Patent gives the example of a particular architecture where operations were conducted in parallel on all even or all odd bit lines at a time (an "interleaving page architecture"). *Id.* The 159 Patent states that this architecture is disadvantageous for three reasons: 1) it requires additional

multiplexing circuitry, 2) it is slow in performance, and 3) it is not optimum in addressing disturb effects such as field coupling between neighboring elements. *Id.* at 8:27-36.

The 159 Patent purports to solve these problems by utilizing an architecture that reduces redundancy in the read/write circuits. *Id.* at 9:9-11. This is accomplished by redistributing the modules in the read/write circuits into "core" portions that operate in parallel and a smaller set of "common" portions as illustrated below in Fig. 10. *Id.* at 9:11-17.

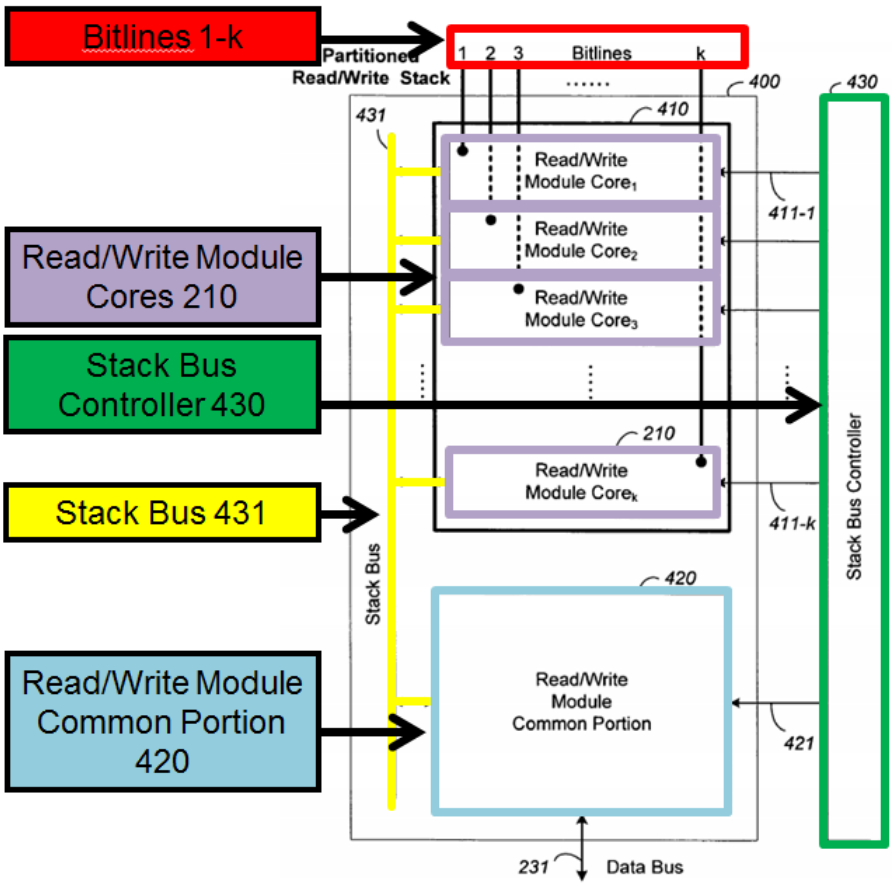


FIG. 10

MICRON-1001, 159 Patent at Figure 10 (with annotations).

As shown in Fig. 10, each of the "core" portions of the read/write circuits (Read/Wire Module Core 210) are connected to a bitline (1-k). Also as shown in Fig. 10, each of these "core" portions is connected to a smaller number of "common" portions (Read/Write Module Common Portion 420). The 159 Patent states that the "core" portions are all operated in parallel. *Id.* at 14:65-67. The 159 Patent also states that after the memory cells (connected to bitlines 1-k) are sensed in parallel, "the sensed results can be processed by the relatively fewer common portions in a serial manner." *Id.* at 14:67-15:3.

Communication between each of the "core" portions of the read/write circuits and the "common" portion is through the Stack Bus 431 under the control of the Stack Bus Controller 430. *Id.* at 15:4-8. Control lines (Control Lines 411-k and Control Lines 421) connect the controller 430 to the "core" and "common" portions. *Id.*

Memory cells in non-volatile memory can store one or more bits of information at a time. *Id.* at 6:10-13. As acknowledged by the 159 Patent, memory cells that store more than one bit of data ("multi-state or multi-level memory cells") were already known in the art. *Id.* at 6:10-17.

5. 159 PATENT PROSECUTION HISTORY

The application that led to the issuance of the 159 Patent was a continuation application originally filed with 20 claims. MICRON-1002, 5-5-2005 Preliminary Amendment at .070-.073. On October 18, 2005, in the first Office Action, the Examiner rejected all claims under the judicially created doctrine of obviousness-type double patenting. *Id.*, 10-18-2005 Office Action at .089-.090. The rejection was purportedly obviated by a terminal disclaimer filed by the patent owner. *Id.*, 2-23-2006 Terminal Disclaimer at .108-.109. On March 6, 2006, a notice of allowance issued in which all pending claims were allowed. *Id.*, 3-6-2006 Notice of Allowance at .119-.122.

6. CLAIM CONSTRUCTION[2]

6.1. Applicable Law

A claim subject to *inter partes* review is given the "broadest reasonable construction in light of the specification of the patent in which it appears."[3] 37

[2] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 159 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 159 Patent.

C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

(Pre-AIA) 35 U.S.C. § 112 ¶ 6 recites a mandatory procedure for interpreting the meaning of a means- or step-plus-function claim element. "These claim limitations 'shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.'" *Al-Site Corp. v. VSI Int'l, Inc.*, 174 F.3d 1308, 1320 (Fed. Cir. 1999). "Use of the word 'means' creates a presumption that § 112, ¶ 6 applies." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (en banc).

Means-plus-function limitations are construed by determining what the claimed function is and identifying the structure or materials disclosed in the

[3] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

specification that correspond to the means for performing that function. *Kemco Sales, Inc. v. Control Papers Co.*, 208 F.3d 1352, 1360 (Fed. Cir. 2000).

6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill in the art and consistent with the specification of the 159 Patent. Petitioner respectfully submits that the following terms should be construed for this IPR:

6.2.1. "bus" (claims 1, 5, 11, 12)

The term "bus" is a limitation of independent claims 1 and 5 of the 159 Patent, and accordingly also limitations of dependent claims 11 and 12. Specifically, claims 1 and 5 recite "a **bus** servicing each component group" and "a **bus** controller coupled to components among each component group to control **bus** operations therein." The 159 Patent describes several different buses that connect and allow communications between components. For example, the 159 Patent describes "a serial bus" that "allows communications between components in each stack." MICRON-1001, 159 Patent at Abstract. Specifically, the serial bus "provides communication between the read/write module core portions and the common portion in each stack" *Id.* at 9:22-24. The 159 Patent also describes a "data bus" that "is coupled to the processor 222 and the data latch stack 224 while

also coupled to the stack bus 431 via the processor 222." Thus, under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "bus" in the context of the 159 Patent to mean "**connection that allows communications between components**." MICRON-1003, Baker Decl. ¶¶ 32-33.

This construction is further confirmed by definitions in industry dictionaries. *See* for example, MICRON-1006, IEEE Standard Dictionary of Electrical and Electronic Terms (1984) at .004 ("bus . . . (3) (electronic computers). One or more conductors used for transmitting signals or power from one or more sources to one or more destinations."). MICRON-1003, Baker Decl. ¶ 33.

6.2.2. "means for controlling operations of components among each component group with its bus" (claim 5)

Claim 5 includes a claim element ("means for controlling operations of components among each component group with its bus") that begins with the words "means for" and invokes 35 U.S.C. § 112 ¶ 6. The sole recited **function** of the limitation is "**controlling operations of components among each component group with its bus.**" MICRON-1003, Baker Decl. ¶ 34.

Under the broadest reasonable interpretation standard, the structures disclosed in the 159 Patent that correspond to this function are the combination of Stack Bus Controller 430 and Control Lines 411-k. MICRON-1003, Baker Decl. ¶ 35; MICRON-1001, 159 Patent at 13:30-35 ("Communication among each

read/write stack 400 is effected by an interconnecting stack bus 431 and controlled by the stack bus controller 430. Control lines 411 provide control and clock signals from the stack bus controller 430 to each of the core portion of the read/write stacks 410.") (emphasis added).

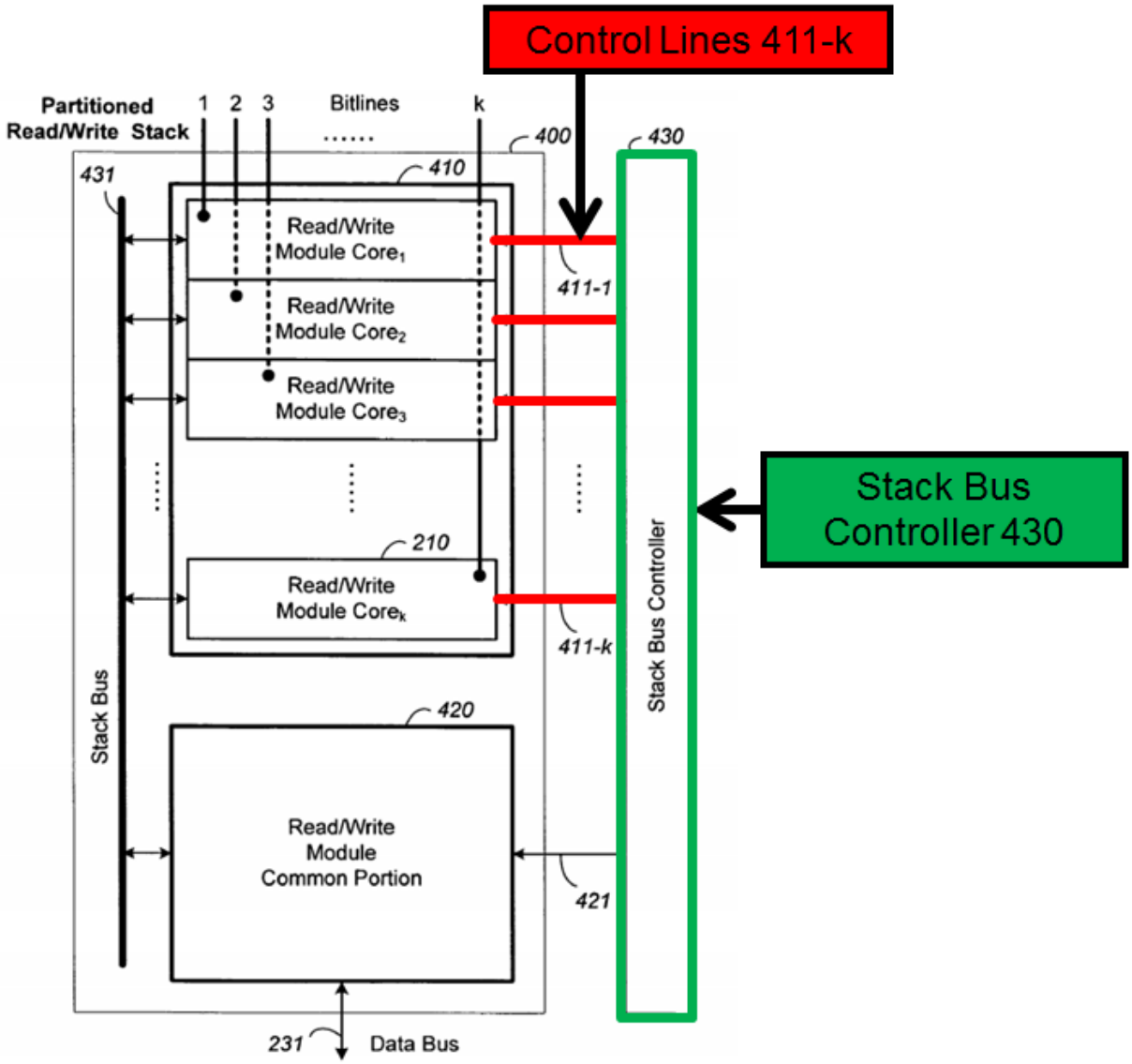


FIG. 10

MICRON-1001, 159 Patent at Figure 10 (with annotations).

As shown in Fig. 10, the "core" portions of the read/write circuits (Read/Write Module Core 210) are components within a larger component group, the core portion of the Read/Write Stack 410. MICRON-1003, Baker Decl. ¶ 35; MICRON-1001, 159 Patent at 13:26-29. As discussed above with regard to Fig. 10, the Stack Bus Controller 430 controls communications between each of the "core" portions of the read/write circuits (Read/Write Module Core 210). *Id*. This control is effected via control lines (Control Lines 411-k). *Id.*; MICRON-1001, 159 Patent at 13:30-35; *see also* MICRON-1003 Baker Decl. ¶ 36.

Thus, because the Stack Bus Controller 430 and Control Lines 411-k collectively perform the function of controlling operations of components (Read/Write Module Core 210) among each component group (the core portion of the Read/Write Stack 410) with its bus (Stack Bus 431), the **corresponding structure** of the claimed "means for controlling operations of components among each component group with its bus" is **Stack Bus Controller 430 and Control Lines 411-k, and equivalents thereof.** MICRON-1003, Baker Decl. ¶ 37.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 159 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design of memory device

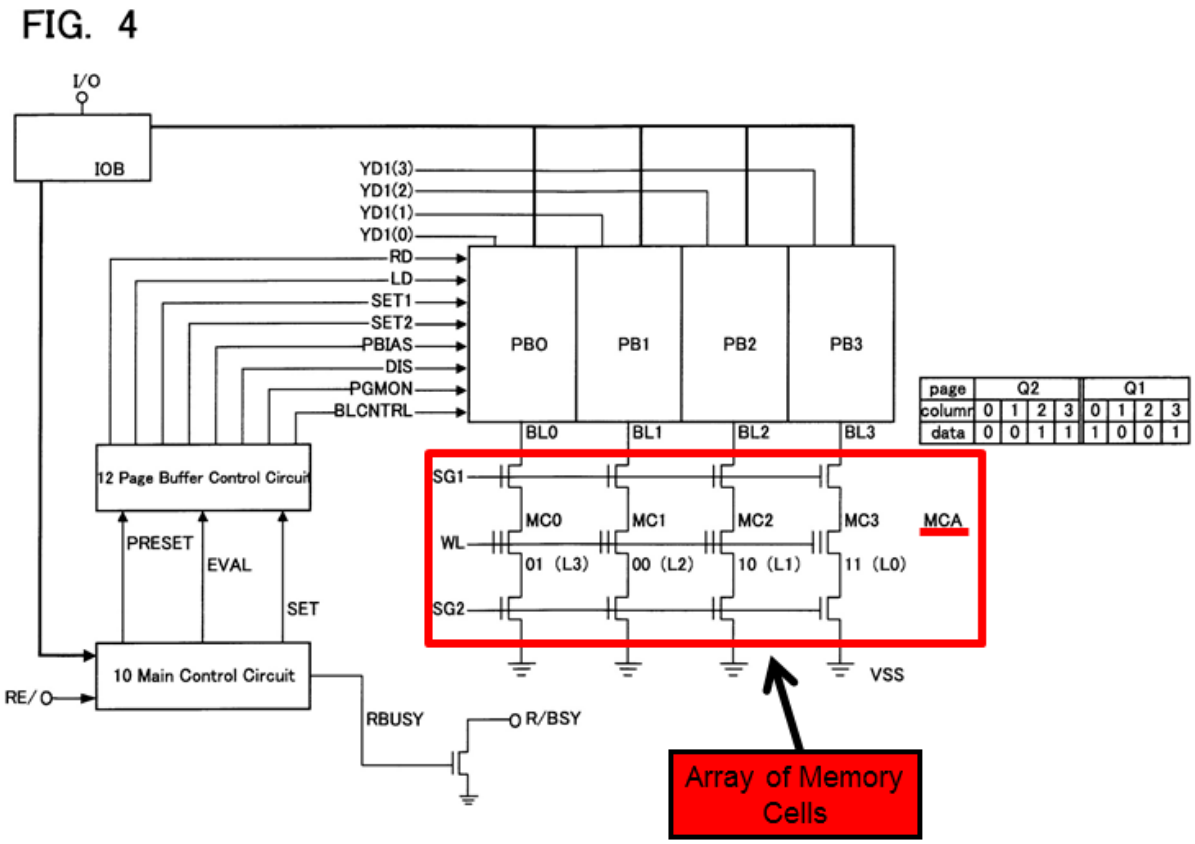
systems. An individual with an advanced degree in a relevant field would require less experience in the design of memory device systems. MICRON-1003, Baker Decl. ¶ 17.

8. DESCRIPTION OF THE PRIOR ART

8.1. U.S. Patent No. 6,288,936 ("Kawamura")

U.S. Patent No. 6,288,936 ("Kawamura") (MICRON-1005) was filed on December 12, 2000. Kawamura issued on September 11, 2001 to Shoichi Kawamura and is entitled "Nonvolatile Memory For Storing Multivalue Data." The original assignee was Fujitsu Limited. Kawamura is prior art to the 159 Patent under (pre-AIA) 35 U.S.C. § 102(b) because the patent issued more than one year before the application to which the 159 Patent claims priority was filed.

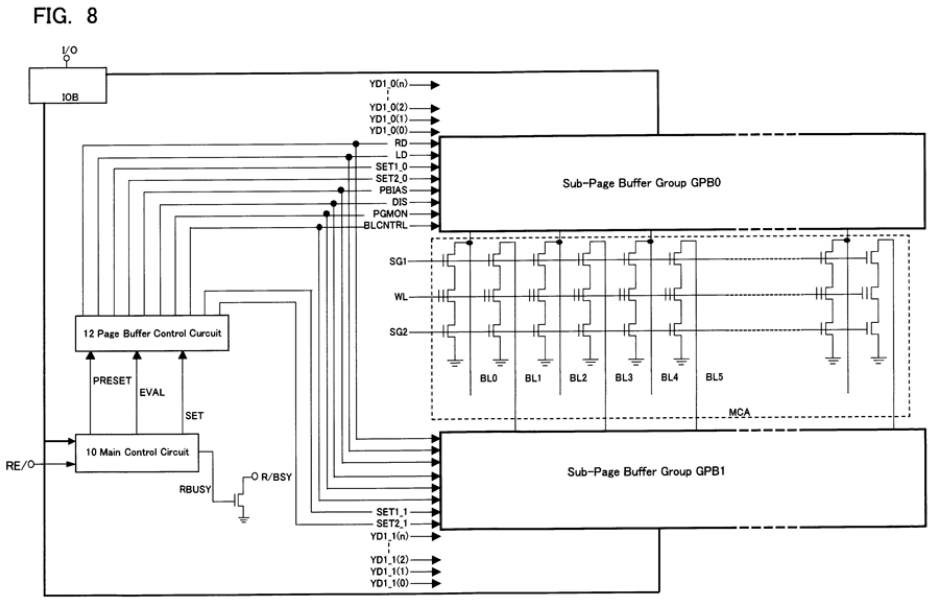
Kawamura discloses a non-volatile memory comprising memory cells that can store multivalue data. MICRON-1005, Kawamura at 1:6-9. Each of the memory cells is read and written to by circuity including a page buffer. *Id.* at 8:4-6, 12:24-25. These page buffers (like the "core" modules of the 159 Patent) are connected to memory cells in an array via bit lines. Each page buffer is connected to one bit line, as depicted in Fig. 4:



MICRON-1005, Kawamura at Figure 18 (with annotations).

Fig. 4, Fig. 10, and Fig. 18 depicts a memory cell array comprising 4 memory cells at the intersections of the bit lines BL0-BL3 and the word line (WL). A one row by four column configuration is used for the memory cell array to "simplify matters." *Id.* at 4:65-67. Each bit line BL0-BL3 is connected to a corresponding Page Buffer PB0-PB3. Each of the Page Buffers PB0-PB3 is then connected to the Input/Output Buffer IOB (or Program Input Circuit 20 in Fig. 10).

Kawamura also discloses an alternative arrangement of Page Buffers in an embodiment depicted in Fig 8:



MICRON-1005, Kawamura at Figure 8.

In Fig. 8, the Page Buffers are divided into Sub-Page Buffer Groups GPB0-GPB1.[4] "[P]age buffer group GPB0 [is] connected to even-number bit lines and page buffer group GPB1 [is] connected to odd-number bit lines." MICRON-1005, Kawamura at 8:21-24.

The Page Buffers read data from the memory cells in parallel. *Id.* at 8:15-18 ("That is, while all data in all columns can be read to the page buffer from the

[4] The Sub-Page Buffer Groups GPB0-GPB1 depicted in Fig. 8 are referred to as Page Buffer Groups in the specification of Kawamura. MICRON-1005, Kawamura at 8:21-31. For the purposes of consistency, the term "Sub-Page Buffer Group" will be used.

memory cell at once, data can only be sent to the input-output buffer IOB from each page buffer in a time series.") (emphasis added), *id.* at 8:34-36 ("During the period T0, the first data Q2 held by the memory cell is **read** by both [sub-]page buffer group GPB0 and [sub-]page buffer group GPB1 and stored in the latch circuit.") (emphasis added). After data is read in parallel, it is then sent serially via bus to the Input-Output Buffer IOB shown in Fig. 4, Fig. 8, Fig. 10 and Fig. 18. *Id.* at 8:15-18.

The Page Buffers (PB0-PB3 (Fig. 4, Fig. 10, Fig. 18), Sub-page Buffer Group GPB0-GPB1 (Fig. 8)) and the bus connecting the Page Buffers to the Input/Output Buffer IOB are controlled by set of signals. These signals cause the Page Buffers to perform operations such as reading and writing to memory cells. *See, for example, id.* at 5:65-67 ("Read data that has been read from a memory cell and latched to a latch circuit [in a Page Buffer] is output by moving the read signal RD to the H level."). Some of these control signals are from the Page Buffer Controller 12 and Main Controller 10. *Id.* at 5:9-13. Other signals to the Page Buffers include selection signals YD1(0)-YD1(3) that select which Page Buffer should be sending or receiving a signal from the Input/Output Buffer IOB at any given point in time. *Id.* at 7:26-29.

The Page Buffers also write data from the memory cells in parallel. MICRON-1005, Kawamura at 14:38-41 ("It is preferable that the common

program input circuit 20 can **store the data Q2 and Q1 for the columns that are simultaneously programmed** as shown in FIGS. 15A-C.") (emphasis added). Data is first sent to the Page Buffers serially, and then is written to the memory cells in parallel. *See, for example*, Kawamura at 11:17-12:5 (explaining how in the first stage, all memory cells to be programmed to the L3 state (1 of 4 possible states) are programmed simultaneously in parallel).

9. GROUND #1: CLAIMS 1, 5, 11, AND 12 OF THE 159 PATENT ARE UNPATENTABLE AS ANTICIPATED OVER KAWAMURA

As explained below, claims 1, 5, 11 (with respect to claims 1 and 5), and 12 (with respect to claims 1 and 5) of the 159 Patent are unpatentable as anticipated under 35 U.S.C. § 102(b).

9.1. Claim 1 is anticipated by Kawamura

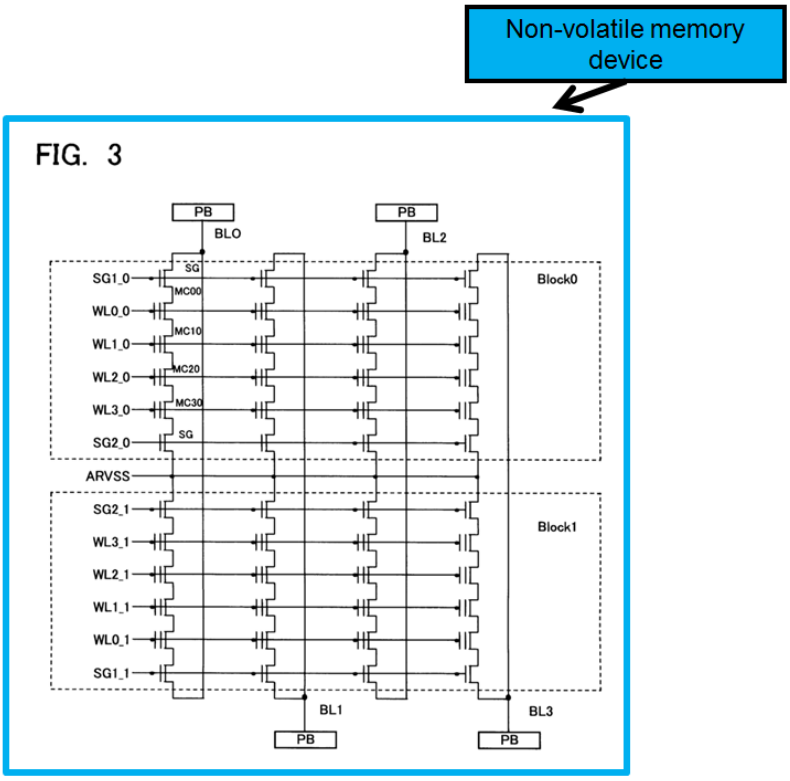
9.1.1. [1.P] "A non-volatile memory device, comprising:"

To the extent the preamble is limiting, Kawamura discloses a non-volatile memory device. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [1.P].

Namely, Kawamura discloses "**[a] nonvolatile memory** that has a plurality of floating gate type cell transistors comprises a read buffer circuit, connected to the bit line, that detects the threshold voltage states in the cell transistor." MICRON-1005, Kawamura at Abstract (emphasis added).

Kawamura discloses flash memory, a type of nonvolatile memory. *Id.* at 1:30-33 ("Because semiconductor **nonvolatile memory**, **such as flash memory**, is small and stores data even when the power is turned off, it is widely used as an image and audio recording medium in equipment such as digital cameras.") (emphasis added).

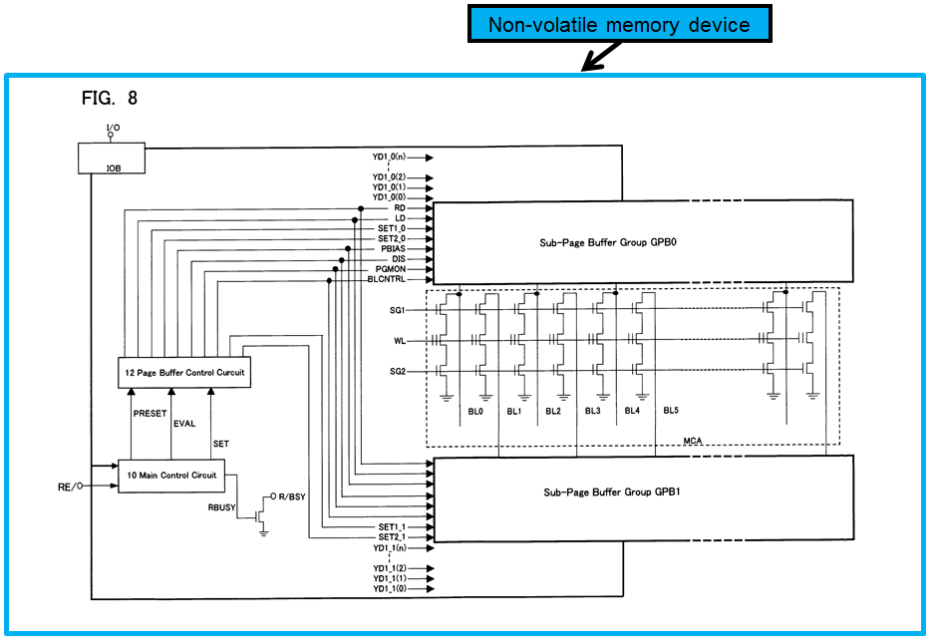
Figure 3 depicts NAND flash non-volatile memory cell arrays. MICRON-1005, Kawamura at 2:65-57 ("FIG. 3 is a diagram showing the configuration of **NAND flash memory** and page buffer in this aspect of the embodiment").



MICRON-1005, Kawamura at Figure 3 (with annotations).

Figure 4 depicts the non-volatile memory device in Fig. 3 with only one word line to simplify the depiction of the memory cell array (MCA), connection to page buffers, PB0-PB4, and bus controller consisting of controllers 12 and 14. As explained with respect to Fig. 4, "[to] simplify matters, a one row by four column configuration is used for the memory cell array MCA." MICRON-1005, Kawamura at 4:65-67 (emphasis added); *Id.* at 3:1-2 ("FIG. 4 is a schematic view of the entire **flash memory** in this aspect of the embodiment") (emphasis added).

Figure 8 also depicts a non-volatile memory device disclosed in Kawamura. *Id.* at 3:9-10 ("FIG. 8 is another schematic general view of the **flash memory**") (emphasis added).



MICRON-1005, Kawamura at Figure 8 (with annotations).

Figure 10 depicts still yet another view of the non-volatile memory device disclosed in Kawamura. MICRON-1005, Kawamura at 3:12-13 ("FIG. 10 is a schematic general view of the **flash memory** for explaining programming operations") (emphasis added).

Figure 18 depicts another schematic view of a non-volatile memory device, FM0, disclosed in Kawamura along with 3 block representations, FM1-FM3, of the non-volatile memory device. MICRON-1005, Kawamura at 3:29-31 ("FIG. 18 is a schematic view of a memory device that has a **plurality of flash memories**.") (emphasis added).

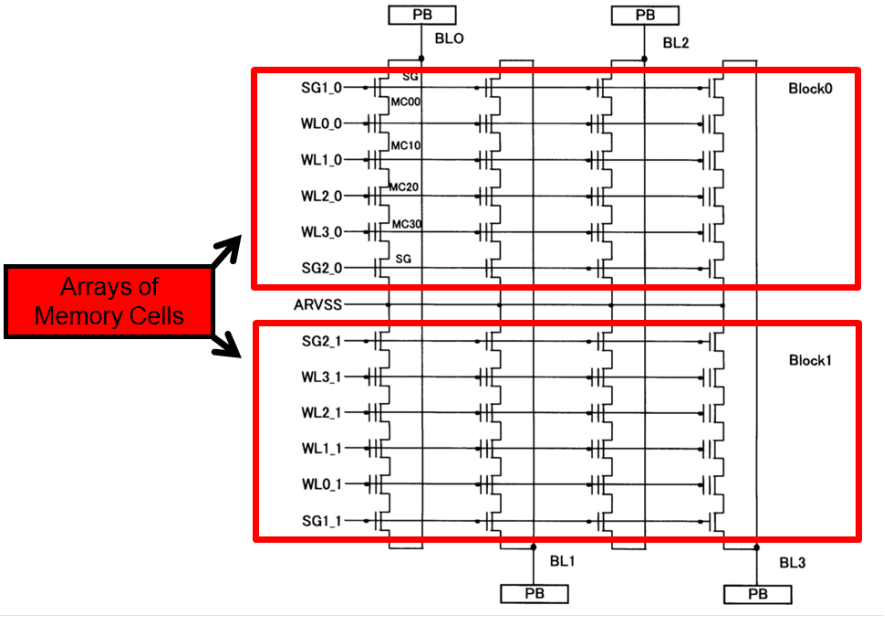
Thus, because Kawamura discloses non-volatile memory devices such as flash memories, it discloses a non-volatile memory device.

9.1.2. [1.1] "an array of memory cells;"

Kawamura discloses an array of memory cells. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [1.1].

For example, Kawamura discloses an array of memory cells with multiple rows. MICRON-1005, Kawamura at 4:43-45 ("FIG. 3 shows the configuration of the page buffer and the NAND-type **flash memory array** . . .") (emphasis added).

FIG. 3



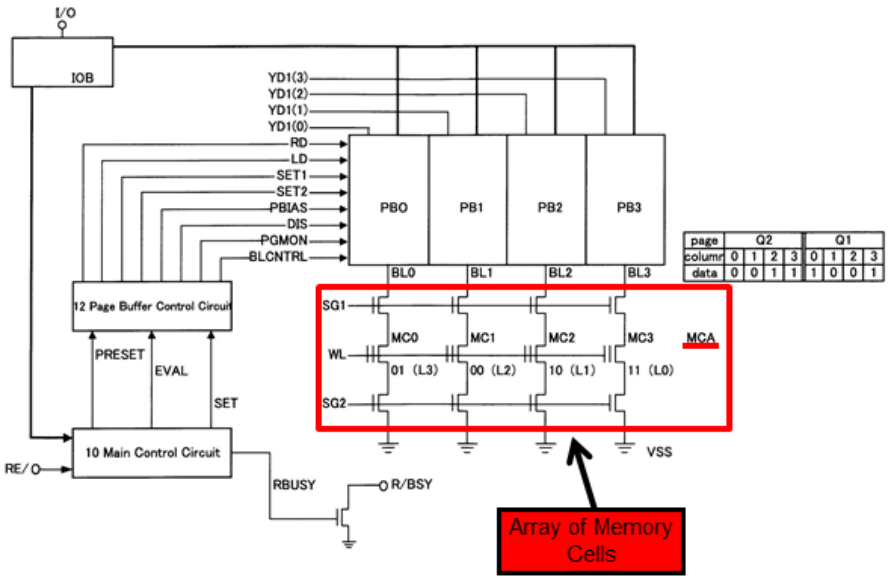
MICRON-1005, Kawamura at Figure 3 (with annotations).

Two arrays of memory cells are depicted in Fig. 3. The arrays are in a 4 row by 4 column configuration. There are 4 bit lines shown BL0-BL3 and each bit line is connected to four memory cells (MC00, MC10, MC20, MC30) within each block. MICRON-1005, Kawamura at 4:45-46 ("[Fig. 3] shows four bit lines BL0 through BL3 . . ."), *id.* at 4:49-51 ("In the example shown in FIG. 3, the four memory cells MC00 through MC30 are connected to the bit line BL0 . . .").

As explained with respect to Fig. 4, "[to] simplify matters, a one row by four column configuration is used for the memory cell array MCA." MICRON-1005, Kawamura at 4:65-67 (emphasis added). The same array is shown in Fig. 10. Though the label MCA does not appear, the identical array configuration (one row

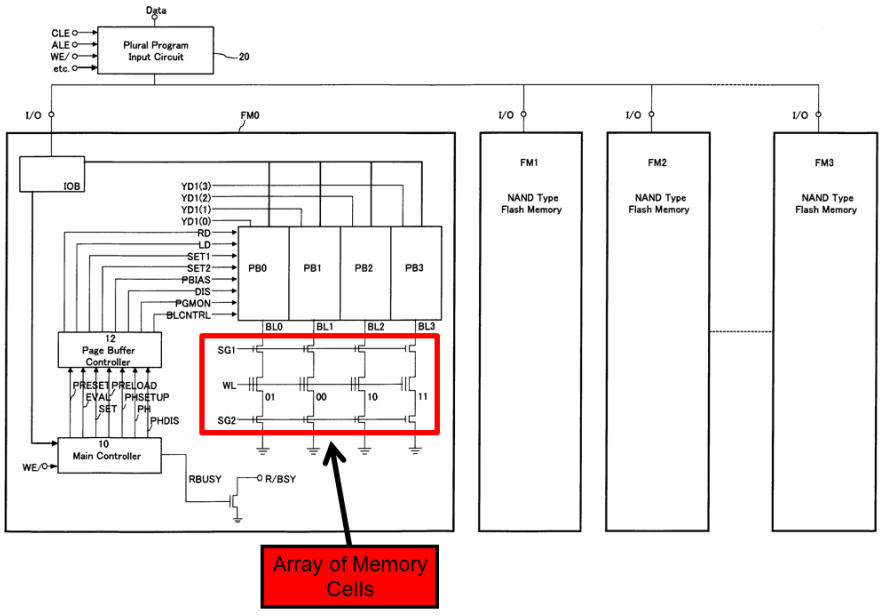
by four columns) also appears in Fig. 18. *Compare* MCA in Fig. 4 to the array in Fig. 18.

FIG. 4



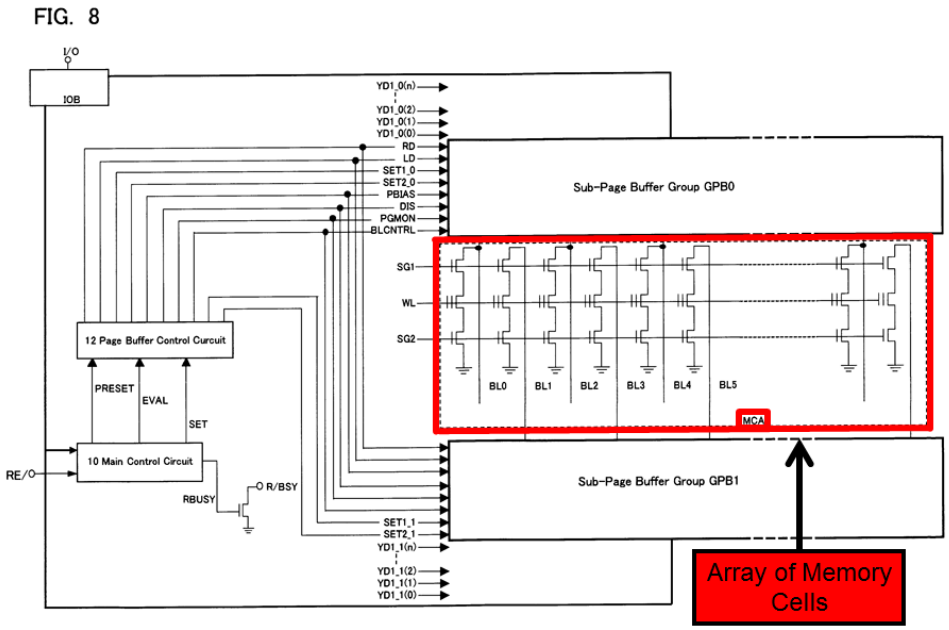
MICRON-1005, Kawamura at Figure 4 (with annotations).

FIG. 18



MICRON-1005, Kawamura at Figure 18 (with annotations).

Kawamura also discloses a "memory cell array" (labeled MCA) in Fig. 8:



MICRON-1005, Kawamura at Figure 8 (with annotations).

Thus, because Kawamura discloses a Memory Cell Array MCA, it discloses an "array of memory cells."

9.1.3. [1.2] "a set of read/write circuits for operating on a set of memory cells in parallel among said array;"

Kawamura discloses a set of read/write circuits for operating on a set of memory cells in parallel among said array. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [1.2].

Kawamura discloses Page Buffers, Input Output Buffers, and Program Input Circuits (set of read/write circuits).

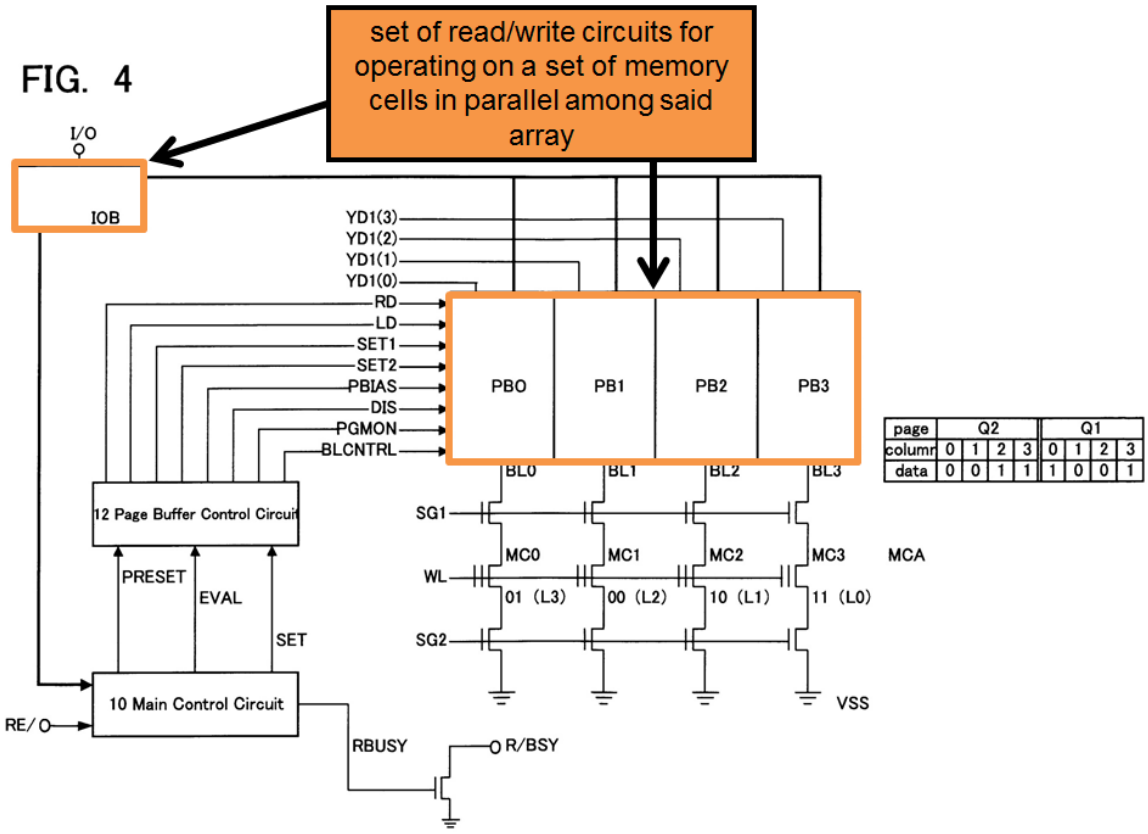
Page Buffers are buffers in the read / write path. When describing one aspect of the Page Buffers, the 159 Patent describes them as "read buffer circuits" that "comprise[] a circuit for detecting the bit line level and a latch circuit for holding read data." MICRON-1005, Kawamura at 4:60-63, Fig. 3. Despite being initially characterized as "read buffer circuits," Kawamura makes clear that the Page Buffers are also used to write (or program) data to cells. *See, e.g.*, *id.* at 2:44-46 ("During the programming, the read buffer circuit latches the above program data and sends the program data to the bit lines."), *id.* at 12:24-25 ("write enable data is stored in page buffer PB2 and then data is written to the corresponding memory cell."), *id.* at 14:2-6 ("the write data . . . will be automatically . . . transferred to the page buffer corresponding to the program data Pout, and data will be written . . ."). Indeed, this is further confirmed by a stated object of Kawamura which is to provide a circuit with a simple configuration that enables *programming* of multivalue data in nonvolatile memory, and the fact that the only circuits directly connected to the bit lines of the memory cells in Kawamura are the Page Buffers. *Id.* at 2:1-4, Fig. 4, Fig. 8, Fig. 10 and Fig. 18.

An Input-Output Buffer is also an intermediary buffer in the read / write path. It is connected to the Page Buffers either directly or through a Program Input Circuit. MICRON-1005, Kawamura at 5:4-8 ("An external input-output terminal I/O is **connected to all four page buffers PB0 through PB3 via an input-output**

buffer IOB. Through use of page buffer selection signals YD1 (0) through (3), one page buffer is connected to the input-output buffer IOB.") (emphasis added); *see also* Fig. 10.

A Program Input Circuit is also an intermediary in the read / write path. It is connected to the Page Buffers either directly or through an Input-Output Buffer. MICRON-1005, Kawamura at 9:34-39 ("In the flash memory shown in FIG. 10, the two bits of data to be programmed, Q2 and Q1, are input serially from the input-output terminal I/O and, **the program input circuit sends the program data Pout**, which shows whether or not a program exists, **to the page buffer PB** in accordance with the combination of two-bit data.") (emphasis added); *see also* Fig. 18.

Kawamura discloses that the Page Buffers (part of the set of read/write circuits) read ("operate") memory cells in the Memory Cell Array (array of memory cells) in parallel. Figure 4 depicts Page Buffers ("read/write circuits") that read ("operate") in parallel. MICRON-1005, Kawamura at 5:11-13 ("FIG. 4 is a schematic view that explains the read operation and that shows the control signals required for reading data.") Further, Fig. 4 depicts an Input-Output Buffer IOB to which data is transferred from the Page Buffers.



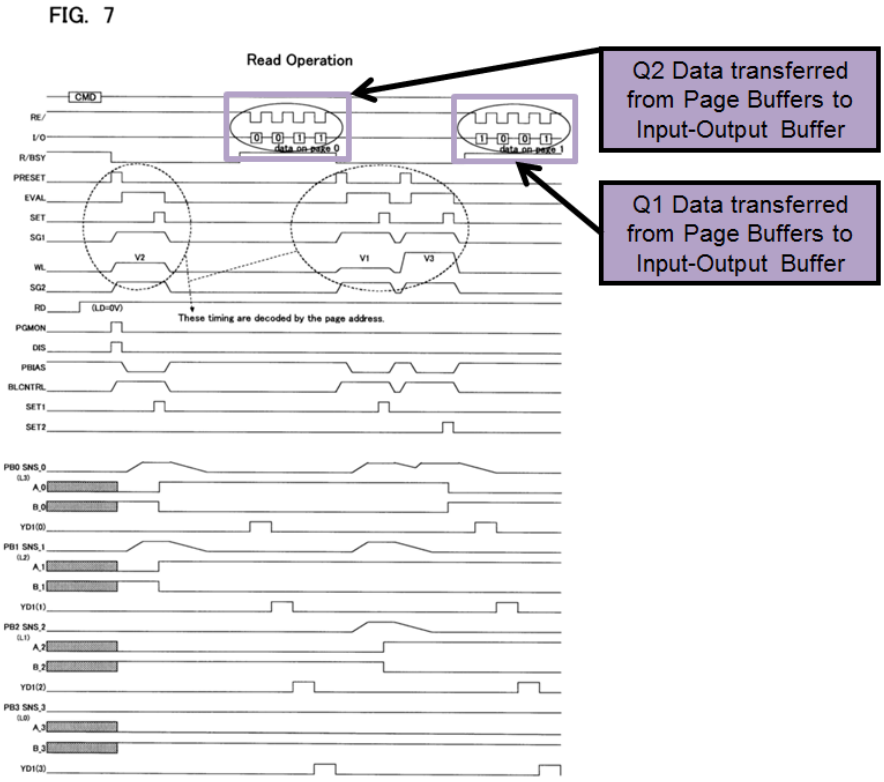
MICRON-1005, Kawamura at Figure 4 (with annotations).

Each of the memory cells MC0-MC3 in Fig. 4 holds two bits of data. MICRON-1005, Kawamura at 5:18-20 ("Because each memory cell holds two bits, the memory cell array MCA physically consists of one row and four columns but logically of two rows and four columns.") When performing a read operation, the Page Buffers PB0-PB3 first read the higher order bit Q2 from the memory cells MC0-MC3 in parallel. The data is stored in the Page Buffers PB0-PB3 in a latch circuit LATCH. The data is then sent serially from the Page Buffers PB0-PB3 to the Input-Output Buffer IOB. MICRON-1005, Kawamura at 7:29-31 ("**The states of the latch circuits in each page buffer are sent via the input-output buffer**

circuit IOB to the input-output terminal I/O. As shown in FIG. 7, "0011" is output to the terminal I/O as the first data Q2.") (emphasis added).

The Page Buffers PB0-PB3 then read the lower order bit Q1 from the memory cells MC0-MC3 in parallel. The data is stored in the Page Buffers PB0-PB3 in a latch circuit LATCH. MICRON-1005, Kawamura at 6:51-53 ("In both the first and second cycles, data in the latch circuit LATCH is sent from the page buffer PB to the input-output buffer IOB."), *see also* MICRON-1005, Kawamura at 7:62-67 (emphasis added).

Figure 7 depicts a timing chart for this read operation of Kawamura showing the Q2 and Q1 data being transferred serially from the Page Buffers PB0-PB3 to the Input-Output Buffer IOB after the data is read in parallel from the memory cells:

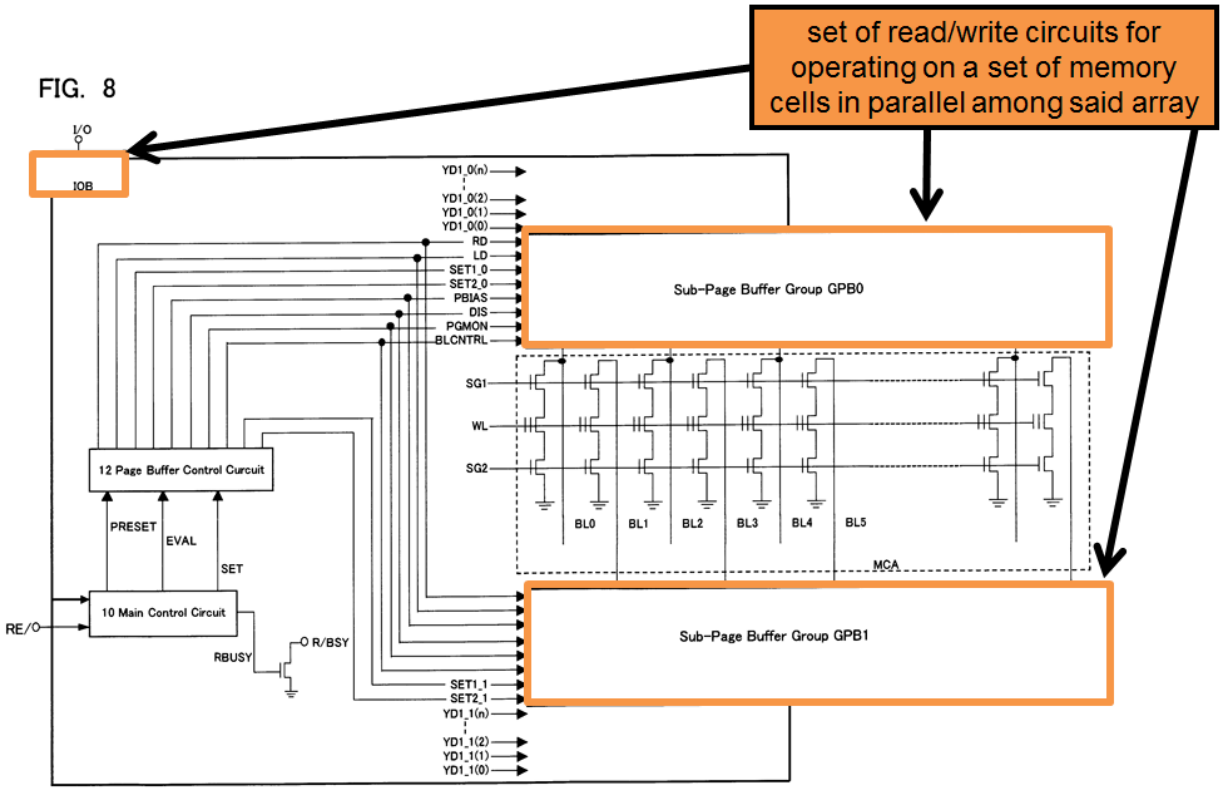


MICRON-1005, Kawamura at Figure 4 (with annotations).

See also MICRON-1005, Kawamura at 8:11-20 ("That is, **while all data in all columns can be read to the page buffer from the memory cell at once, data can only be sent to the input-output buffer IOB from each page buffer in a time series**.") (emphasis added).

Kawamura also discloses "a set of read/write circuits for operating on a set of memory cells in parallel among said array" in Fig. 8. In Fig. 8, the Page Buffers (part of the set of "read/write circuits") are arranged in an alternate configuration where the "plurality of page buffers [] divided into a [sub-]page buffer group

GPB0 connected to even-number bit lines and [sub-]page buffer group GPB1 connected to odd-number bit lines." *Id.* at 8:21-24 (emphasis added).



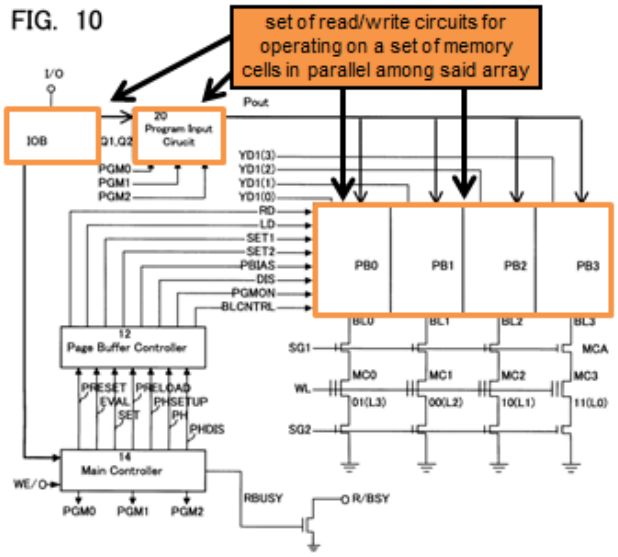
MICRON-1005, Kawamura at Figure 8 (with annotations).

The Sub-Page Buffer Groups GPB0 and GPB1, and Input-Output Buffer IOB are included in "a set of read/write circuits for operating on a set of memory cells in parallel among said array." Because the Page Buffers can read data from the memory cells in all of columns at the same time, they "operat[e] on a set of memory cells in parallel." *Id.* at 8:34-36 ("During the period T0, the first data Q2 held by the memory cell is **read** by both [sub-]page buffer group GPB0 and [sub-]page buffer group GPB1 and stored in the latch circuit.") (emphasis added). After

data is read in parallel, it is then sent serially to the input-output buffer IOB. *Id.* at 8:15-18.

Thus, Because the Page Buffers (Page Buffers PB0-PB3 in Fig. 4, Fig. 10, or Fig. 18, or the Page Buffers within sub-page buffer groups GPB0-GPB1 in Fig. 8) in combination with the Input-Output Buffer IOB read memory cells in parallel, they "operat[e] on a set of memory cells in parallel."

The "a set of read/write circuits for operating on a set of memory cells in parallels among said array" limitation is also disclosed because the Page Buffers *write* ("operate") to memory cells in parallel. Fig. 10 is a schematic "for explaining the program operation." MICRON-1005, Kawamura at 9:11-12.

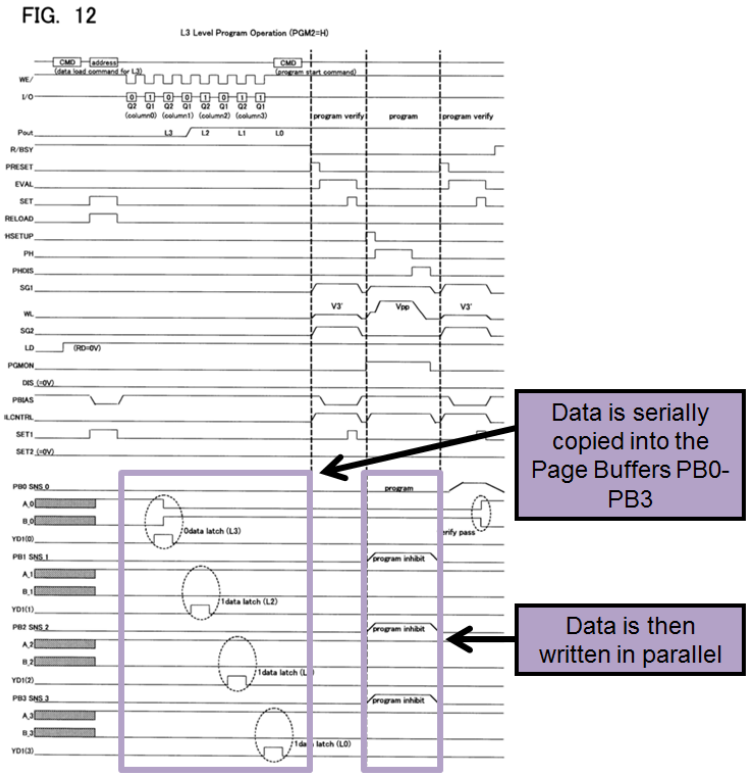


MICRON-1005, Kawamura at Figure 10 (with annotations).

The Memory Cells MC0-MC3 each hold two bits of data. Thus, they each have one of four possible states (L0-L3). MICRON-1005, Kawamura at 9:9-12;

9:18-20 ("[T]he memory cells hold two bits of data and so are programmed in four threshold voltage states, L0 through L3.") When writing (programming) to the memory cells, the data is first input serially though the Input-Output Buffer, then to the Program Input Circuit 20 (as shown in Fig. 10). Data is then serially sent to the four Page Buffers PB0-PB3. MICRON-1005, Kawamura at 9:34-49 ("Accordingly, in the example shown in FIG. 10, four sets of data Q2 and Q1 are serially input from the input-output terminal I/O and the corresponding program data Pout is sent serially to four page buffers PB.").

The programming operation then consists of stages. MICRON-1005, Kawamura at 9:26-33. First, all of the Memory Cells to be programed to L3 are programed simultaneously in parallel. This is depicted in Fig. 12 which shows a timing chart for this operation of programming to state L3. MICRON-1005, Kawamura at 10:59-11:16 ("The L3 level program operation will be explained using FIG. 12. Firstly, the data to be written is input into NAND-type flash memory. The write data load command that corresponds to state L3 is first input").

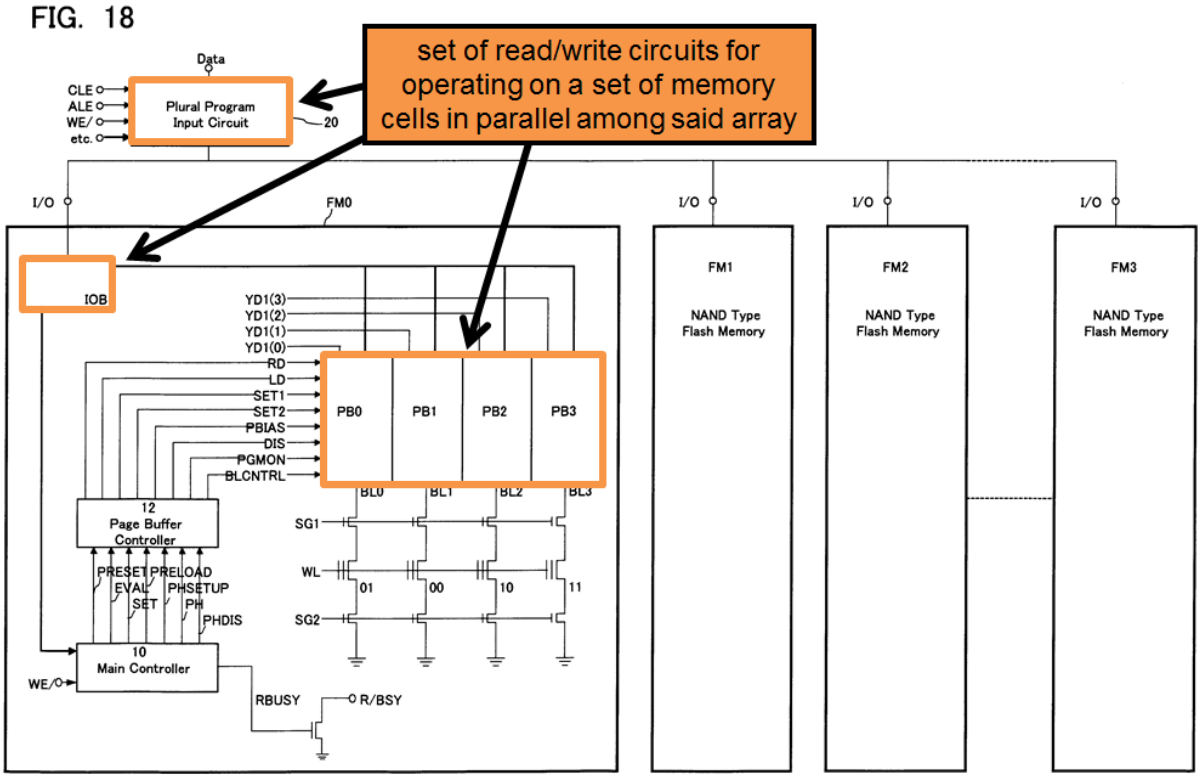


MICRON-1005, Kawamura at Figure 12 (with annotations).

Once the program data Pout is stored in the latch circuit of the Page Buffers, it is written to the memory cells in parallel. In the example provided in Fig. 12, only the data for the memory cell connected to PB0 corresponds to L3 (node A is low), so only that cell is written. However, if the data for the other memory cells corresponded to L3, then those cells would be written at the same time. MICRON-1005, Kawamura at 11:17-12:5.

Figure 13, and Fig. 14 depict the timing charts for the operations for programming to the other states L1 and L2, respectively. MICRON-1005, Kawamura at 3:17-22.

Kawamura also discloses "a set of read/write circuits for operating on a set of memory cells in parallel among said array" in Fig. 18. Fig. 18 discloses a set of Page Buffers PB0-PB3, Input-Output Buffer IOB, and a Program Input Circuit 20:



MICRON-1005, Kawamura at Figure 18 (with annotations).

In Fig. 18, "a program input circuit 20 is provided as an external circuit . . ." MICRON-1005, Kawamura at 14:32-33. The Program Input Circuit 20 is then connected to the Input-Output Buffer IOB which is then connected to the Page Buffers PB0-PB3 as shown in Fig. 18.

The Page Buffers PB0-PB3 are capable of operating on the memory cells in parallel. As shown in Fig. 18 above, the Page Buffers PB0-PB3 are the only

circuits connected to the bit lines of the memory cells. And, with respect to Fig. 18, Kawamura discloses writing to multiple portions of the memory simultaneously. *Id.* at 14:38-41 ("It is preferable that **the common program input circuit 20 can store the data Q2 and Q1 for the columns that are <u>simultaneously programmed</u>** as shown in FIGS. 15A-C.") (emphasis added). Because the Page Buffers PB0-PB3 are the only circuits connected to the bit lines, and portions of the memory are written simultaneously, the Page Buffers PB0-PB3 are capable of operating on memory cells in parallel.

Because the Page Buffers in combination with an Input-Output Buffer, and Program Input Circuit ("read/write circuits") write memory cells in parallel, they "operat[e] on a set of memory cells in parallel."

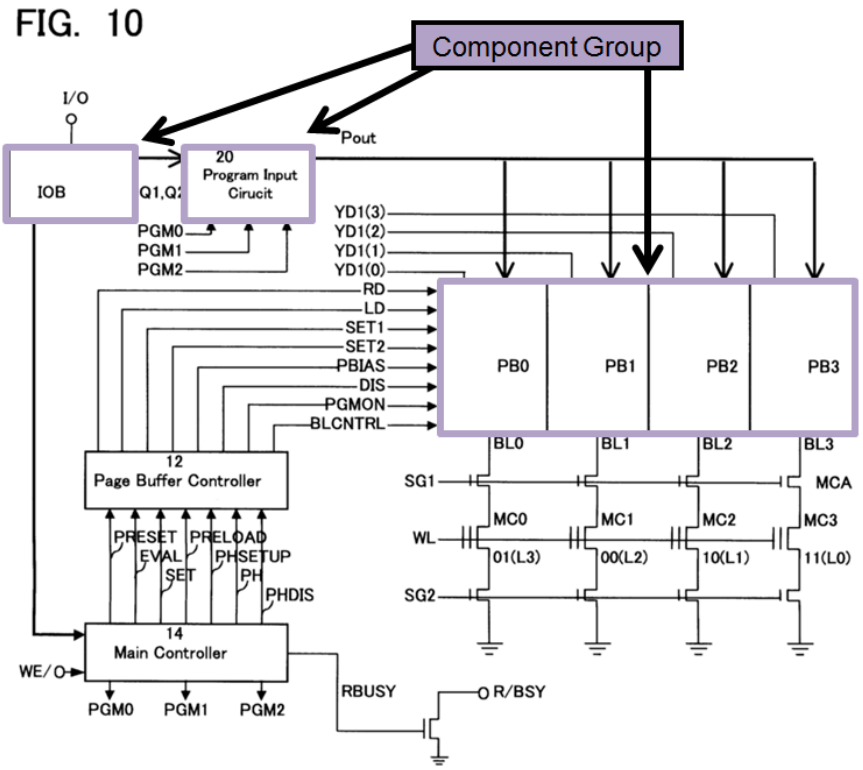
Thus, because Kawamura discloses Page Buffers, PB0-PB3 (Fig. 4, Fig. 10, and Fig. 18) or Sub-Page Buffer Groups GPB0-GPB1 (Fig. 8), Input-Output Buffer IOB, and Program Input Circuit 20 (collectively, read/write circuits) that read (operate) and write (operate) in parallel on a memory cell array (an array of memory cells), Kawamura discloses a set of read/write circuits for operating on a set of memory cells in parallel among said array.

9.1.4. [1.3] "said set of read/write circuits having a plurality of components forming one or more component groups;"

Kawamura discloses the set of read/write circuits having a plurality of components forming one or more component groups. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [1.3].

The set of read/write circuits (Page Buffers, Input-Output Buffer IOB, and Program Input Circuit 20, collectively, discussed above for claim limitation [1.2]) include a plurality of components. Namely, each of the Page Buffers, Input-Output Buffer IOB, and Program Input Circuit 20, is a component, and, collectively, they are a "component group."

Fig. 10 discloses a single group of Page Buffers, Input-Output Buffer IOB, and Program Input Circuit 20.

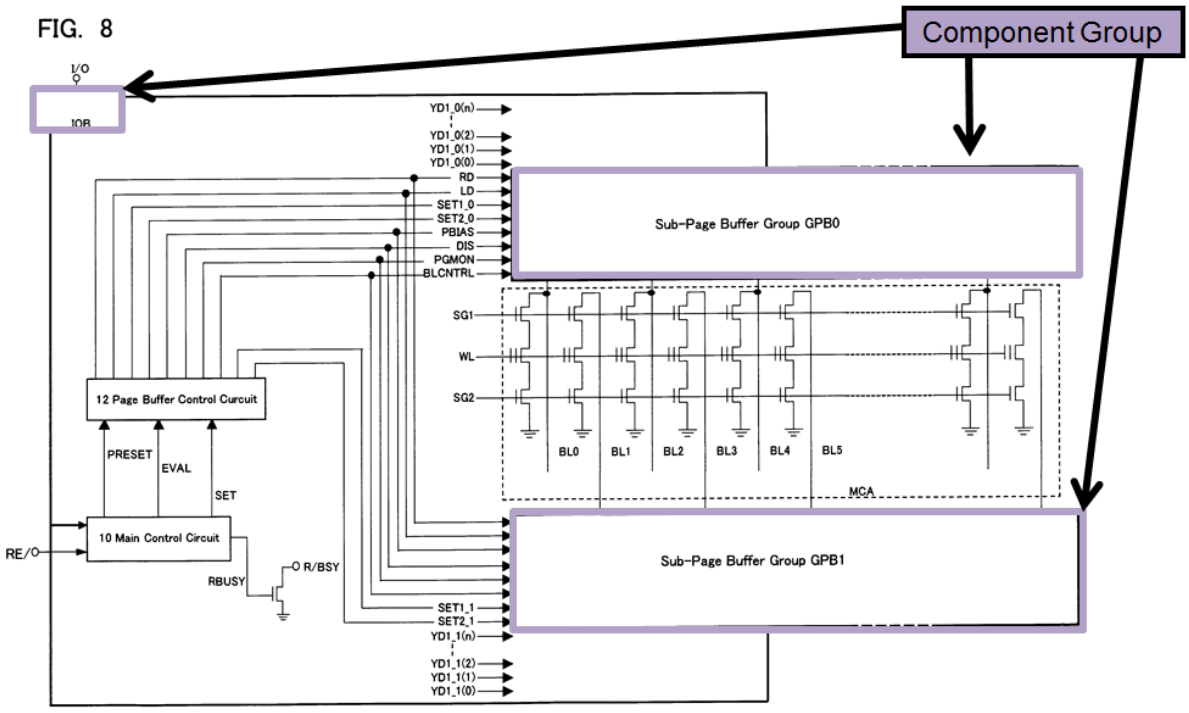


MICRON-1005, Kawamura at Figure 10 (with annotations).

Even though only a single group of Page Buffers PB0-PB3 ("component group") is depicted, Fig. 4 still discloses this limitation because only "**one** or more component groups" is required.

This group (Page Buffers PB0-PB3, Input-Output Buffer IOB, and Program Input Circuit 20) ("component group") is also depicted in Fig. 4 and Fig. 18. However, the Program Input Circuit 20 is not shown in Fig. 4 because Fig. 4 is a "a schematic view that explains the read operation" as opposed to Fig. 10 which explains the write (or program) operation. MICRON-1005, Kawamura at 5:11-13, 9:11-12.

Also, Fig. 8 depicts a configuration of Page Buffers identified as Sub-Page Buffer Group GPB0 and Sub-Page Buffer Group GPB1. *See* MICRON-1005, Kawamura at 8:21-24 ("In the flash memory of FIG. 8, the plurality of page buffers is divided into a [sub-]page buffer group GPB0 connected to even-number bit lines and [sub-]page buffer group GPB1 connected to odd-number bit lines.") (emphasis added). These Sub-Page Buffer Groups in combination with the Input-Output Buffer IOB form a single "component group."



MICRON-1005, Kawamura at Figure 8 (with annotations).

Thus, because Kawamura discloses a set of Page Buffers (Page Buffers PB0-PB3 in Fig. 4, Fig. 10 and Fig. 18, or Page Buffers in Sub-Page Buffer Groups GPB0-GPB1 in Fig. 8), Input-Output Buffer IOB, and Program Input Circuit 20

("set of read/write circuits") that each comprise multiple components (Page Buffers, Input-Output Buffers, and Program Input Circuits) that form a group, Kawamura discloses said set of read/write circuits having a plurality of components forming one or more component groups.

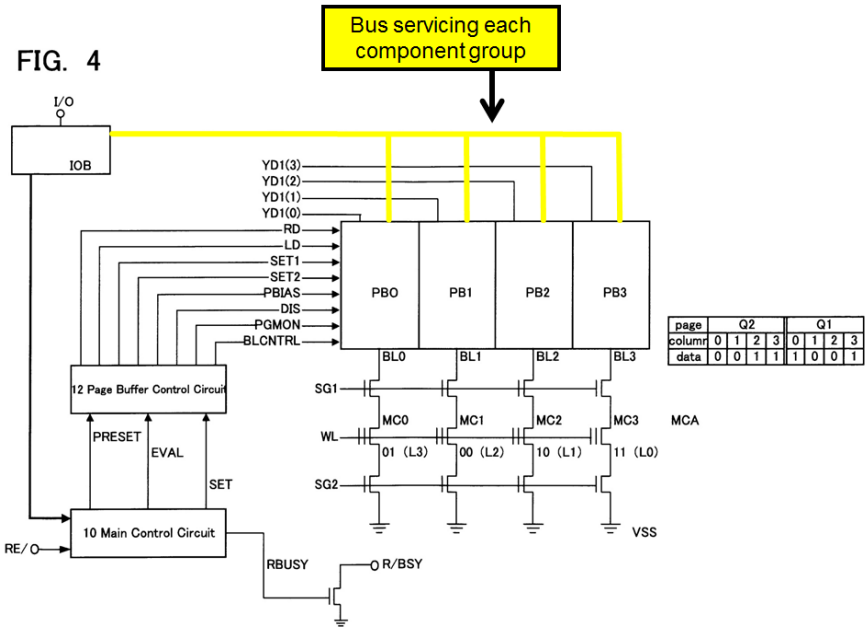
9.1.5. [1.4] "a bus servicing each component group; and"

Kawamura discloses a bus servicing each component group. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [1.4].

As explained above, under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "bus" in the context of the 159 Patent to mean a "connection that allows communications between components." Section 6.2.1, MICRON-1003, Baker Decl. ¶¶ 32-33.

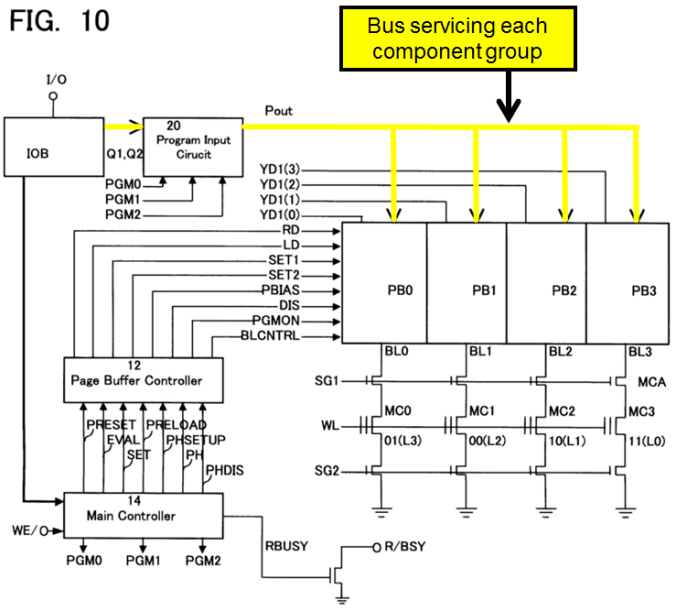
Kawamura discloses a connection that allows communications between Page Buffers, Input-Output Buffer IOB, and Program Input Circuit 20.

Namely, Figure 4 discloses a connection that allows communications between components ("bus") servicing Page Buffers PB0-PB3 and Input-Output Buffer IOB (part of "component group"). This connection is between the Input-Output Buffer and the Page Buffers PB0-PB3. MICRON-1005, Kawamura at 5:4-6 (explaining, with respect to Fig. 4, that an external terminal is connected to all four Page Buffers PB0-PB3 via the Input-Output Buffer IOB).

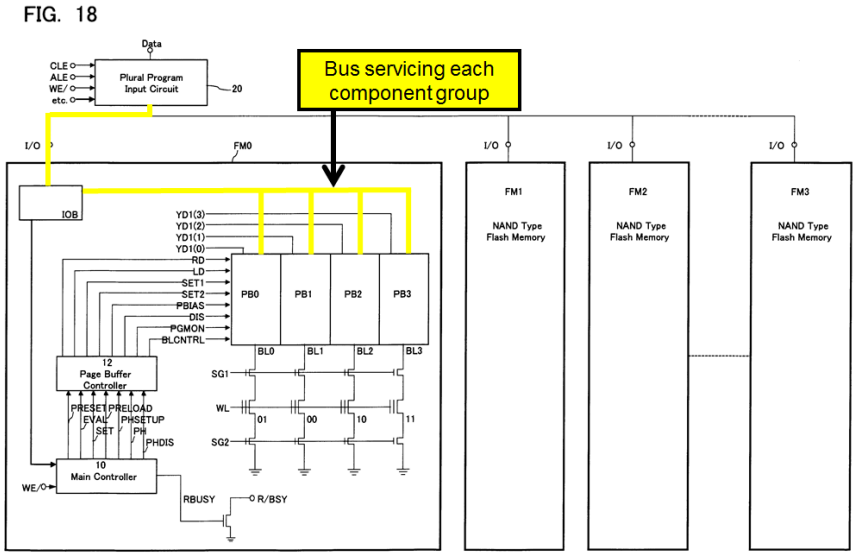


MICRON-1005, Kawamura at Figure 4 (with annotations).

Figure 10 and Fig. 18 disclose a similar connection that allows communications between components ("bus") servicing Page Buffers PB0-PB3, Input-Output Buffer IOB, and Program Input Circuit 20 ("component group").

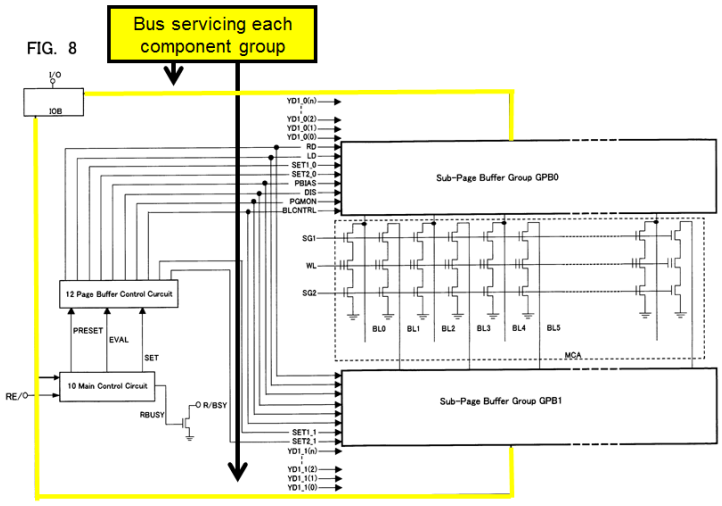


MICRON-1005, Kawamura at Figure 10 (with annotations).



MICRON-1005, Kawamura at Figure 18 (with annotations).

With respect to Fig. 8, Kawamura discloses a connection that allows communications between components ("bus") servicing the portion of the component group (Page Buffers in Sub-Page Buffer Groups GPB0-GPB1, and Input-Output Buffer IOB).



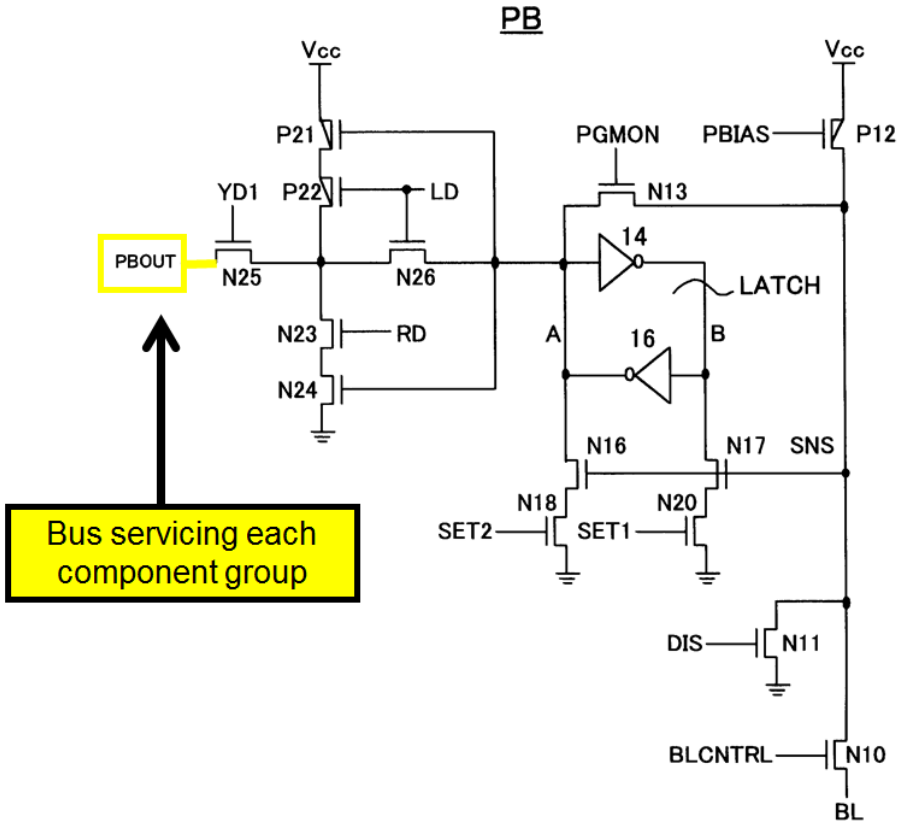
MICRON-1005, Kawamura at Figure 8 (with annotations).

As shown in the annotated Fig. 8 above, the Page Buffers in Sub-Page Buffer Group has a connection to the Input Output Buffer IOB.

Kawamura also discloses page buffer selection signals YD1 that are used to connect a specific page buffer to the input-output buffer IOB. MICRON-1005, Kawamura at 5:4-8 ("An external input-output terminal I/O is connected to all four page buffers PB0 through PB3 via an input-output buffer IOB. Through use of page buffer selection signals YD1 (0) through (3), one page buffer is connected to the input-output buffer IOB."). These buffer selection signals YD1 appear in Fig. 4, Fig. 8, Fig. 10, and Fig. 18.

Kawamura discloses that the bus identified for Fig. 4, Fig. 8, Fig. 10, and Fig. 18 is connected to the PBOUT terminal of the Page Buffers PB. This is depicted in Fig. 5:

FIG. 5



MICRON-1005, Kawamura at Figure 5 (with annotations).

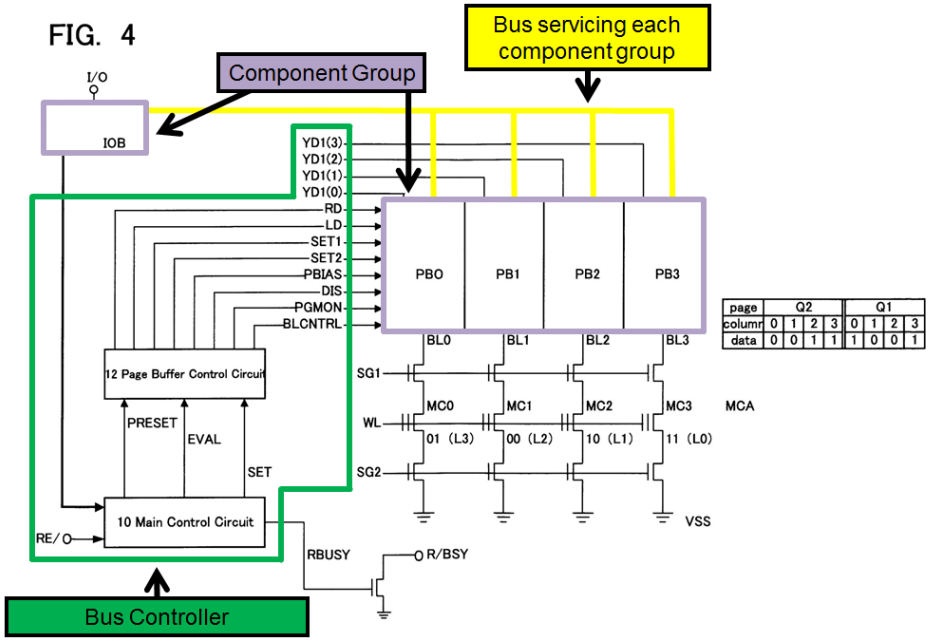
Thus, because Kawamura discloses a connection that allows communications between components servicing Page Buffers PB0-PB3 (or Sub-Page Buffer Groups GPB0-GPB1 in Fig. 8), Input/Output Buffer IOB, and Program Input Circuit 20, Kawamura discloses a bus servicing each component group.

9.1.6. [1.5] "a bus controller coupled to components among each component group to control bus operations therein."

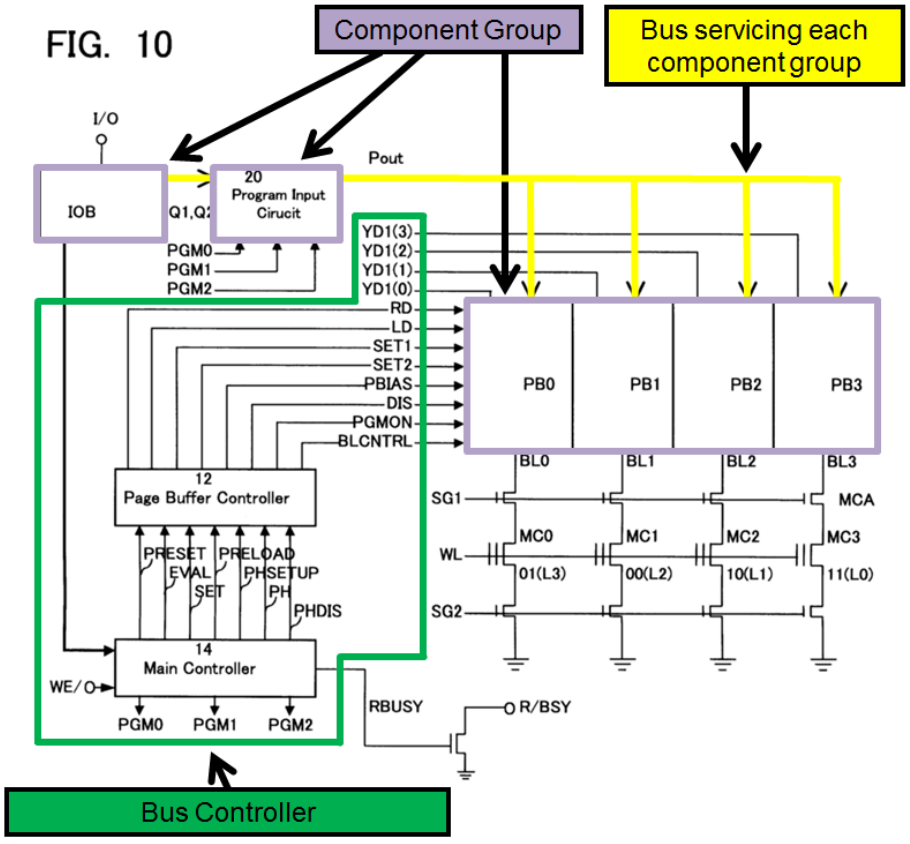
Kawamura discloses a bus controller coupled to components among each component group to control bus operations therein. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [1.5].

As explained above, under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "bus" in the context of the 159 Patent to mean "connection that allows communications between components." Section 6.2.1, MICRON-1003, Baker Decl. ¶¶ 32-33.

As shown in Fig. 4, Fig. 10, and Fig. 18 and discussed in the specification, Kawamura discloses that the YD1 signals, Page Buffer Controller 10, and Main Controller 10 are coupled to components (Page Buffers PB0-PB3, Input-Output Buffer IOB, and Program Input Circuit 20) within each of the component groups (collectively, Page Buffers PB0-PB3, Input-Output Buffer IOB, and Program Input Circuit 20) to control bus operations:

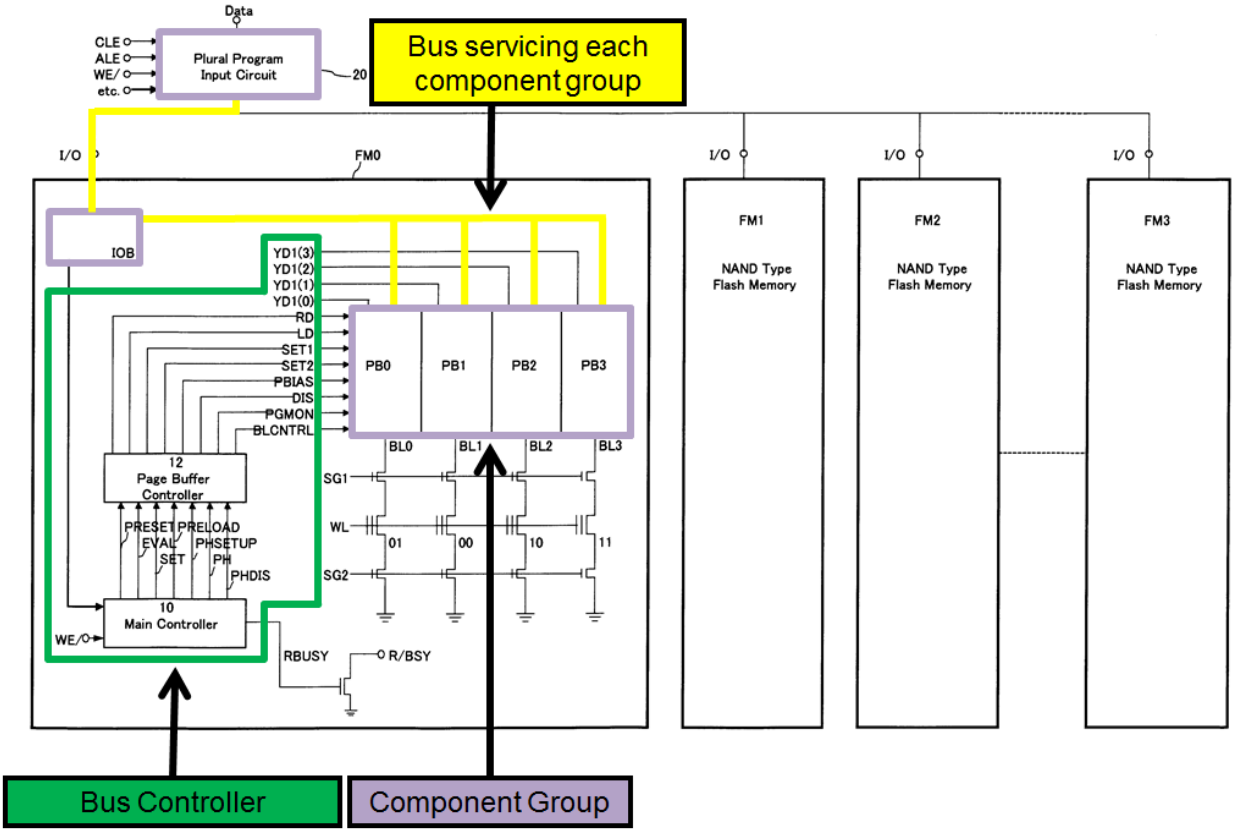


MICRON-1005, Kawamura at Figure 4 (with annotations).



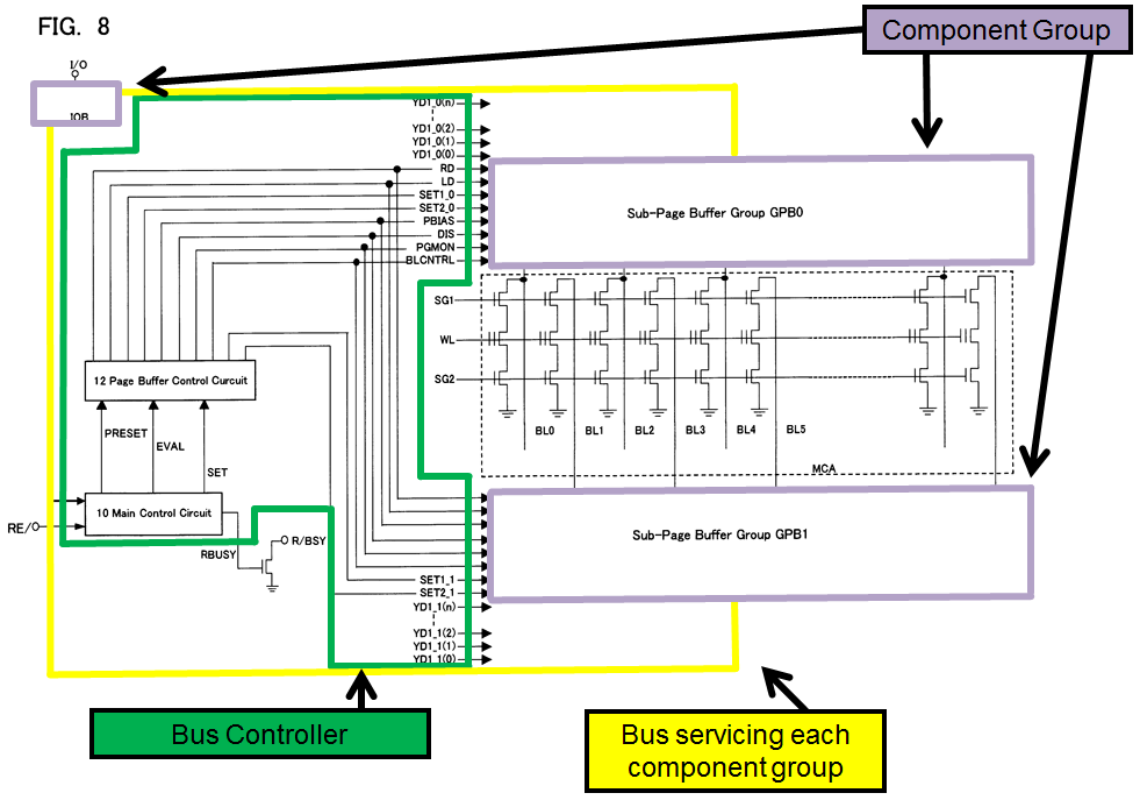
MICRON-1005, Kawamura at Figure 10 (with annotations).

FIG. 18



MICRON-1005, Kawamura at Figure 18 (with annotations).

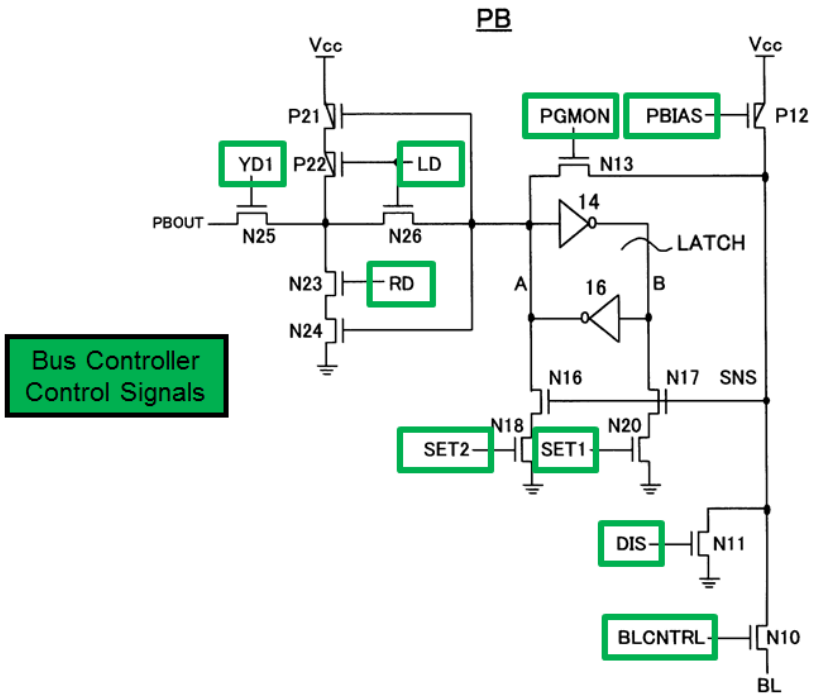
With respect to the embodiment depicted in Fig. 8, Kawamura discloses YD1 signals, Page Buffer Controller 12, and Main Controller 10 that are coupled to components (Page Buffers and Input-Output Buffer) within each of the component groups (collectively, Sub-Page Buffer Group GPB0-GPB1 and Input-Output Buffer) to control bus operations.



MICRON-1005, Kawamura at Figure 8 (with annotations).

While not directly shown in Fig. 4, Fig. 8, Fig. 10, and Fig. 18, each of signals to the page buffers (YD1, RD, LD, SET1, SET2, PBIAS, DIS, PGMON, and BLCNTRL) are connected to each of the Page Buffers and not just to the set of Page Buffers as a whole. This is shown by Fig. 5 which depicts the schematic of a single Page Buffer with inputs for each of the signals shown in Fig. 18. *Compare* the YD1, RD, LD, SET1, SET2, PBIAS, DIS, PGMON, and BLCNTRL signals in each of Fig. 4, Fig. 5, Fig. 8, Fig. 10, and Fig. 18.

FIG. 5



MICRON-1005, Kawamura at Figure 5 (with annotations).

The only other two inputs or outputs to a Page Buffer, as shown in Fig. 4, Fig. 5, Fig. 8, Fig. 10, and Fig. 18, are PBOUT which is connected to the Input Output Buffer IOB (or Program Input Circuit 20 in Fig. 10), and BL (Bit Line) which is connected to the memory cell below.

The YD1 signals and the signals from Page Buffer Controller 12 and Main Controller 10 control the bus operations within each Page Buffer. For example, assuming that the set of signals are properly configured, "[r]ead data that has been read from a memory cell and latched to a latch circuit [in a Page Buffer] is output by moving the read signal RD to the H level." MICRON-1005, Kawamura at 5:65-67. Also, for example, the YD1 signals control which Page Buffer is connected to

the Input-Output Buffer IOB at a time. *Id.* at 5:6-8 ("Through use of page buffer selection signals YD1 (0) through (3), one page buffer is connected to the input-output buffer IOB."); *Id.* at 7:26-29 ("Continuous changing of internal addresses in synchronized with the read-enable clock RE/ enables the selection signals YD1 (0) through YD1 (3) for each page buffer to move to the H level in a time series.")

Thus, because Kawamura discloses the YD1 signals, Page Buffer Controller 12, and Main Controller 10 coupled to Page Buffers ("components") among the group of Page Buffers PB0-PB3 (Fig. 4, Fig. 10, Fig. 18) or Sub-Page Buffer Group GPB0 and Sub-Page Buffer Group GPB1 (Fig. 8), Input-Output Buffer IOB, and Program Input Circuit 20 (collectively, "component group") to control bus operations with the Input-Output Buffer IOB (or Program Input Circuit 20 as shown in Fig. 10), Kawamura discloses a bus controller coupled to components among each component group to control bus operations therein.

9.2. Claim 5 is anticipated by Kawamura

9.2.1. [5.P] "A non-volatile memory device, comprising:"

To the extent the preamble is limiting, Kawamura discloses a non-volatile memory device. MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [5.P]. This limitation is identical to limitation [1.P] and is disclosed by Kawamura for the same reasons set forth above. *See* Section 9.1.1.

9.2.2. [5.1] "an array of memory cells;"

Kawamura discloses an array of memory cells. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [5.1]. This limitation is identical to limitation [1.1] and is disclosed by Kawamura for the same reasons set forth above. *See* Section 9.1.2.

9.2.3. [5.2] "a set of read/write circuits for operating on a set of memory cells in parallel among said array;"

Kawamura discloses a set of read/write circuits for operating on a set of memory cells in parallel among said array. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [5.2]. This limitation is identical to limitation [1.2] and is disclosed by Kawamura for the same reasons set forth above. *See* Section 9.1.3.

9.2.4. [5.3] "said set of read/write circuits having a plurality of components forming one or more component groups;"

Kawamura discloses the set of read/write circuits having a plurality of components forming one or more component groups. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [5.3]. This limitation is identical to limitation [1.3] and is disclosed by Kawamura for the same reasons set forth above. *See* Section 9.1.4.

9.2.5. [5.4] "a bus servicing each component group; and"

Kawamura discloses a bus servicing each component group. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [5.4]. This limitation is identical

to limitation [1.4] and is disclosed by Kawamura for the same reasons set forth above. *See* Section 9.1.5.

9.2.6. [5.5] "means for controlling operations of components among each component group with its bus."

Kawamura discloses a means for controlling operations of components among each component group with its bus. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [5.5].

As explained above, under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "bus" in the context of the 159 Patent to mean "connection that allows communications between components." Section 6.2.1; MICRON-1003, Baker Decl. ¶¶ 32-33.

As explained above, under the broadest reasonable interpretation standard, the recited function is "controlling operations of components among each component group with its bus" and the corresponding structure is Stack Bus Controller 430, and Control Lines 411, and equivalents thereof (collectively, the "159 Corresponding Structure"). Section 6.2.2; MICRON-1003, Baker Decl. ¶¶ 34-37.

The structure "for controlling operations of components among each component group with its bus" disclosed in Kawamura is the same as or at least

equivalent to the 159 Corresponding Structure. *Compare*, for example, Fig. 10 of 159 Patent to Fig. 4 of Kawamura:

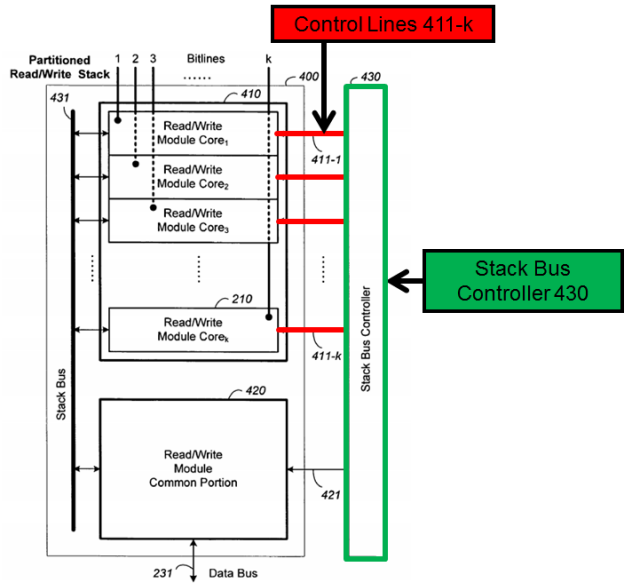
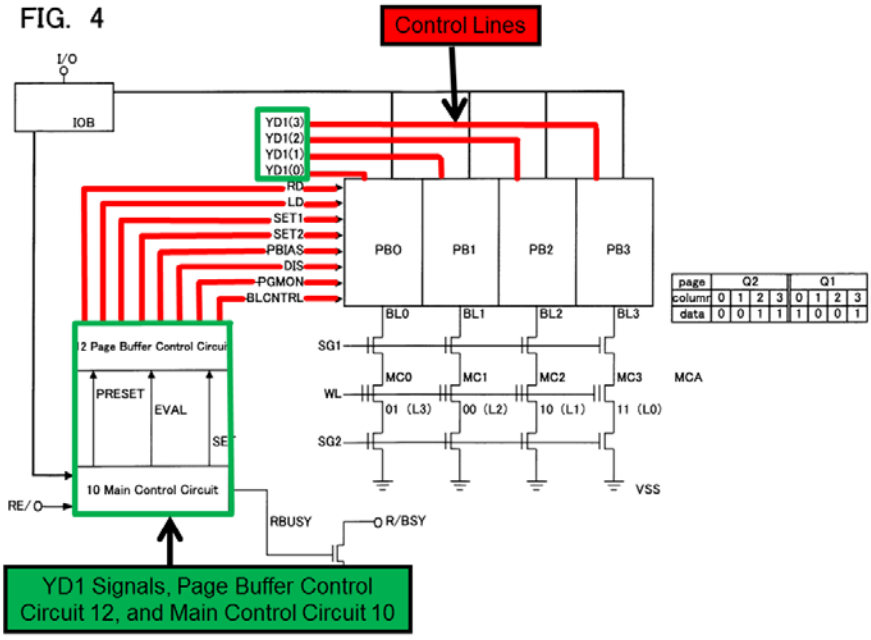


FIG. 10

MICRON-1001, 159 Patent at Figure 10 (with annotations).



MICRON-1005, Kawamura at Figure 4 (with annotations).

The YD1 Signals, Page Buffer Controller 10, Main Controller 10, and corresponding control lines (collectively, the "Kawamura Corresponding Structure") of Fig. 4, Fig. 8, Fig. 10 and Fig. 18 have an identical function to the corresponding structure. Namely, the function of the Kawamura Corresponding Structure is for controlling operations of components (Page Buffers) among each component group (collectively, the Page Buffers in Sub-Page Buffer Groups GPB0-GPB1 (Fig. 8) or Page Buffers PB0-PB3 (Fig. 4, Fig. 10, Fig. 18), Input-Output Buffer IOB, and Program Input Circuit 20) with its bus (the connection between the Input-Output Bus IOB (and Program Inputs Circuit 20 in Fig. 10) and the Page Buffers). For example, "[r]ead data that has been read from a memory cell and latched to a latch circuit [in a Page Buffer] is output by moving the read signal RD to the H level." MICRON-1005, Kawamura at 5:65-67. Also, for example, the YD1 signals control which Page Buffer is connected to the Input-Output Buffer IOB at a time. *Id.* at 5:6-8 ("Through use of page buffer selection signals YD1 (0) through (3), one page buffer is connected to the input-output buffer IOB."). While not directly shown in Fig. 4, Fig. 8, Fig. 10 and Fig. 18, each of signals to the page buffers (YD1, RD, LD, SET1, SET2, PBIAS, DIS, PGMON, and BLCNTRL) are connected to each of the Page Buffers and not just to the component groups as a whole. *See* Annotated Fig. 5 in Claim [1.5] above.

The 159 Corresponding Structure performs this function by sending signals from a controller, along control lines, to control the operations of components with its bus. MICRON-1001, 159 Patent at 9:26-28 ("A bus controller sends control and timing signals to control the operation of the components and their interactions through the serial bus."), *id.* at 13:33-35 ("Control lines 411 provide control and clock signals from the stack bus controller 430 to each of the core portion of the read/write stacks 410."). Likewise, the Kawamura Corresponding Structure performs this function in substantially the same way by sending YD1 signals and signals from the Page Buffer Controller 10 and Main Controller 10, along control lines, to control the operations of components (Page Buffers in Sub-Page Buffer Groups GPB0-GPB1 (Fig. 8) or Page Buffers PB0-PB3 (Fig. 4, Fig. 10, Fig. 18), Input-Output Buffer IOB, and Program Input Circuit 20) with the bus. For example, assuming that the set of signals are properly configured, "[r]ead data that has been read from a memory cell and latched to a latch circuit [in a Page Buffer] is output by moving the read signal RD to the H level." MICRON-1005, Kawamura at 5:65-67. Also, for example, the YD1 signals control which Page Buffer is connected to the Input-Output Buffer IOB at a time. *Id.* at 5:6-8 ("Through use of page buffer selection signals YD1 (0) through (3), one page buffer is connected to the input-output buffer IOB.").

The result of the 159 Corresponding Structure performing its function is that the flow of data along the bus servicing each component group is controlled by the 159 Corresponding Structure. MICRON-1001, 159 Patent at 15:42-45 ("Each of the bit line latches and sense amplifiers communicates with other components in the read/write stack 400 through the stack bus 431 (see FIG. 10) under the control of the stack bus controller via control lines 411."). Likewise, the result of the Kawamura Corresponding Structure performing its function is substantially the same in that the flow of data along the bus servicing each component group (collectively, Sub-Page Buffer Groups GPB0-GPB1 (Fig. 8) or Page Buffers PB0-PB3 (Fig. 4, Fig. 10, Fig. 18), Input-Output Buffer IOB, and Program Input Circuit 20) is controlled by the Kawamura Corresponding Structure (YD1 Signals, Page Buffer Controller 10, Main Controller 10, and corresponding control lines). MICRON-1005, Kawamura at 5:6-8, 5:65-67. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [5.5].

Because the 159 Corresponding Structure and the Kawamura Corresponding Structure have an identical function that is performed in substantially the same way to achieve substantially the same result, they are at least equivalent under 35. U.S.C. § 112 ¶ 6.

Thus, Kawamura discloses a "means for controlling operations of components among each component group with its bus."

9.3. Claim 11 is anticipated by Kawamura

9.3.1. [11.0] "A non-volatile memory device as in any one of claims 1-8, wherein each memory cell stores one bit of data."

Claim 11 is in multiple dependent form and is anticipated by Kawamura with respect to independent claims 1 and 5. Kawamura discloses a non-volatile memory device as in claims 1 and 5, wherein each memory cell stores one bit of data. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [11.0].

Kawamura discloses cell transistors that store only one bit. MICRON-1005, Kawamura at 1:33-36 ("Greater storage capacity is being demanded but, as described above, in a **conventional nonvolatile memory for normal use a cell transistor can only store one-bit (single value) data.**"), *see also id.* at 13:35-38.

Thus, because Kawamura discloses cell transistors that store only one bit and all the elements of claims 1 and 5, Kawamura discloses a non-volatile memory device as in claims 1 and 5, wherein each memory cell stores one bit of data. *See* Sections 9.1 and 9.2 above.

9.4. Claim 12 is anticipated by Kawamura

9.4.1. [12.0] "A non-volatile memory device as in any one of claims 1-8, wherein each memory cell stores more than one bit of data."

Claim 12 is in multiple dependent form and is anticipated by Kawamura with respect to independent claims 1 and 5. Kawamura discloses a non-volatile memory device as in claim 1 and claim 5, wherein each memory cell stores more

than one bit of data. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, Claim [12.0].

Kawamura discloses memory cells that can hold 2 bits of data. MICRON-1005, Kawamura at 1:37-42 ("**For this reason, the recording of multivalue data, such as 2 bits data, in cell transistors is being proposed.** By controlling the electrical charge injected into floating gates, a plurality of threshold voltage states is achieved and **multivalue data can be recorded**. For example, when **4 value data (2 bits) is stored four threshold voltage states will be stored.**"), *id.* at 2:9-14 ("Each cell transistor can hold 2^N threshold voltage states and accordingly, the read buffer circuit reads N bits of data. For this purpose, the read buffer circuit has a latch circuit that latches the read data in accordance with the detected threshold voltage state.") Memory cells that can hold 2 bits of data can be in one of four states.

Thus, because Kawamura discloses memory cells that hold 2 bits of data and Kawamura discloses all of the elements of claims 1 and 5, Kawamura discloses a non-volatile memory device as in claims 1 and 5, wherein each memory cell stores more than one bit of data. *See* Sections 9.1 and 9.2 above.

10. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1, 5, 11 and 12 of the 159 Patent is requested.

Respectfully submitted,

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By: _____

Douglas W. McClellan
Lead Counsel for Petitioner
Registration No. 41,183
Weil, Gotshal & Manges LLP
700 Louisiana, Suite 1700
Houston, TX 77002
Telephone: 713-546-5313

CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	December 14, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 7,085,159 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1006
Persons served	Patent Owner's Address of Record: Davis Wright Tremaine LLP IP Docketing Dept. 1201 Third Avenue, Suite 2200 Seattle, WA 98101 Additional Addresses Known as Likely to Effect Service: Brian E. Farnan Farnan LLP 919 North Market Street, 12th Floor Wilmington, DE 19801 bfarnan@farnanlaw.com Edward C. Flynn Cohen & Grace, LLC 105 Braunlich Drive, Suite 300 Pittsburgh, PA 15237 eflynn@cohengrace.com

/ Jeremy Jason Lang /
Jeremy Jason Lang
Back-Up Counsel for Petitioner
Registration No. 73,604