UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

INNOVATIVE MEMORY SYSTEMS, INC.
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 7,000,063
Title: WRITE-MANY MEMORY DEVICE AND METHOD FOR LIMITING A NUMBER OF WRITES TO THE WRITE-MANY MEMORY DEVICE

Petition For *Inter Partes* Review of U.S. Patent No. 7,000,063 Under 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

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MICRON-1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 6,662,262 ("Kasa")
MICRON-1006	B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994) ("Dipert")
MICRON-1007	U.S. Patent No. 5,999,447 ("Naura")
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MICRON-1011	D. Kahng and S.M. Sze, *A Floating Gate and Its Application to Memory Devices*, Bell Syst. Tech. J., (46) (1967) ("Kahng")

Micron Exhibit #	**Description**
MICRON-1012	United States Copyright Office public record search result for B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994)
MICRON-1013	Declaration of Lisa Browar regarding B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994) ("Browar Declaration")
MICRON-1014	Declaration of Sharon Wiles-Young regarding B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994) ("Wiles-Young Declaration")

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 42, 43 and 44 of U.S. Patent No. 7,000,063, titled "Write-Many Memory Device and Method for Limiting a Number of Writes to the Write-Many Memory Device" (MICRON-1001, the "063 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 063 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 063 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Douglas W. McClellan Registration No. 41,183 (doug.mcclellan@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5313; F: 713-224-9511	Jeremy Jason Lang Registration No. 73,604 (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for the Petitioner is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Innovative Memory Systems has asserted the 063 Patent and U.S. Patent Nos. 6,169,503 (the "503 Patent"), 6,324,537 (the "537 Patent"), 6,901,498 (the "498 Patent"), 7,045,849 (the "849 Patent"), 7,085,159 (the "159 Patent"), 7,495,953 (the "953 Patent") and 7,886,212 (the "212 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Innovative Memory Systems, Inc., v. Micron Tech. Inc.*, 14-cv-1480 (D. Del.) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 6,169,503, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 6,324,537, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 6,901,498, IPR2016-Unassigned;

Petition for *Inter Partes* Review of U.S. Patent No. 7,045,849, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,085,159, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,495,953, IPR2016-Unassigned; and Petition for *Inter Partes* Review of U.S. Patent No. 7,886,212, IPR2016-Unassigned.[1]

The 063 Patent does not claim priority to any foreign or U.S. patent application.

2.5. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 063 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Ground #1: Claims 42 and 44 of the 063 Patent are invalid under (pre-AIA) 35 U.S.C. § 102(e) on the ground that they are anticipated by U.S. Patent No. 6,662,262, to Kasa et al. ("Kasa"), entitled "OTP Sector Double Protection for a Simultaneous Operation Flash Memory," filed on October 19, 1999 and issued on

[1] These petitions will be filed concurrently or within a few days.

December 9, 2003. Kasa is attached as MICRON-1005. This ground is explained below and is supported by the Declaration of Dr. R. Jacob Baker (MICRON-1003, "Baker Decl.").

Ground #2: Claim 43 of the 063 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Kasa in view of Brian Dipert and Markus Levy, *Designing with Flash Memory* (1994) ("Dipert"). The excerpts attached as MICRON-1006 are from a copy of the Dipert textbook that was published in 1994.[2] This ground is explained below and is supported by the Baker Decl.

Ground #3: Claim 42 of the 063 Patent is invalid under (pre-AIA) 35 U.S.C. § 102(b) on the ground that is anticipated by U.S. Patent No. 5,999,447, to Naura, et al. ("Naura"), entitled "Non-Volatile Electrically Erasable and

[2] Dipert has an imprint with a copyright date of 1993 and 1994. The United States Copyright Office discloses a publication date of November 1, 1993 in the official registration of copyright. *See* MICRON-1012 (Retrieved Dec. 7, 2015 from the United States Copyright Office public record search). In addition to the copyright and publication date of the reference, *see* MICRON-1013 (Browar Declaration) and MICRON-1014 (Wiles-Young Declaration) which provide additional evidence of its availability to the public.

Programmable Memory," issued on December 7, 1999. Naura is attached as MICRON-1007. This ground is explained below and is supported by the Baker Decl.

Ground #4: Claim 43 of the 063 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Naura in view Dipert. This ground is explained below and is supported by the Baker Decl.

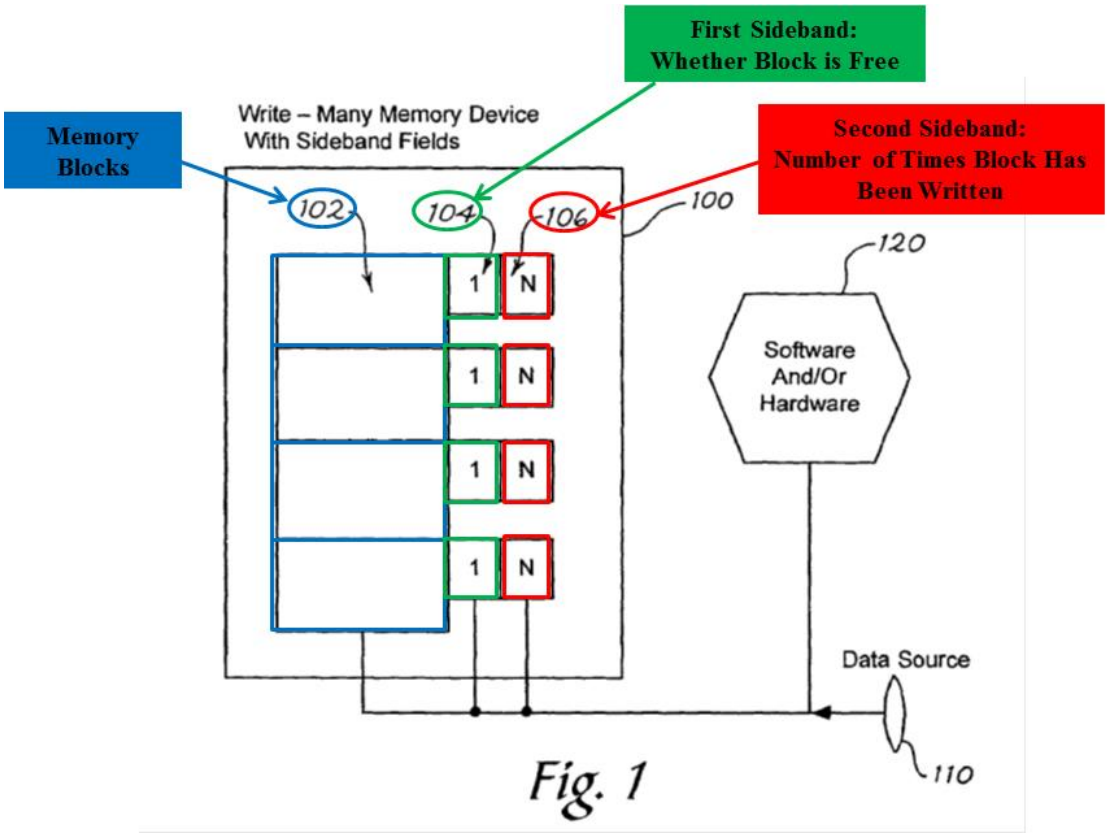
Ground #5: Claim 44 of the 063 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Naura. This ground is explained below and is supported by the Baker Declaration.

4. OVERVIEW OF THE 063 PATENT

The 063 Patent was filed on October 5, 2001 and issued on February 14, 2006. The 063 Patent relates generally to limiting the number of writes to a write-many memory device, such as flash memory. MICRON-1001, 063 Patent at 1:19-21, 1:48-51. More particularly, the 063 Patent provides a mechanism where a user can limit the number of writes to between 1 and the maximum number of writes allowed to a write-many memory device. *Id*. at 3:56-61. The 063 Patent alleges that there were no memory devices that controlled the number of writes to a memory device (*e.g.*, 2 re-writes or 10 re-writes). *Id*. at 1:12-14.

The 063 Patent purportedly provides a solution to this problem by providing a system that includes a write-many memory device containing a plurality of

blocks, where each block is limited to N number of writes. *Id*. at 1:51-55. This write-many memory device could be, for example, flash memory. 2:29-32. In the preferred embodiment, each block of memory includes two sideband fields. *Id*. at 3:12-15. The first sideband field can store data indicating whether the memory block is free, and the second sideband field can store a count of how many times the block had been written to. *Id*. at 3:33-45. Each time the block is written to, the count in the second sideband field increases. *Id*. Data is stored in the memory block only if there have been fewer than N number of writes to the block. This embodiment is illustrated below in Fig. 1:



MICRON-1001, 063 Patent at Figure 1 (annotated).

The 063 Patent describes that this solution would allow a user to not merely choose between a "write-once" memory device and a "write-many" memory device, but to be able to choose between "write-5" and "write-10" memory devices. *Id*. at 6:5-9. The "write-5" and "write-10" memory devices could be priced between the "write-once" and "write-many" memory devices. *Id*. at 6:9-12.

The 063 Patent also describes that the memory device could be preset so that N is limited to 1, resulting in the write-many device operating as a write only device. *Id*. at 3:56-59. It also describes that the write-many memory device can comprise a plurality of blocks of memory that are limited to the maximum number of writes and an additional block that can be limited to a different number of writes. *Id*. at 7:6-11.

The 063 Patent further explains that the manufacturer of the memory device could limit the write-many memory device to a specific number of writes. *Id*. at 3:51-67. For example, the manufacturer could pre-set the write-many memory device so that it can be written to once or as many times as allowed. *Id*.

In addition, the 063 Patent describes that the write-many memory device can be a device that can be removed from a host device. *Id*. at 2:56-67. For example, the write-many memory device could be a card or stick that can be removed from a host device, such as a computer, personal digital assistant, or cellular telephone. *Id*. at 2:67-3:11.

The claims at issue in this petition, claims 42-44, all relate to an embodiment of the alleged invention where a portion of a write-many memory device, such as a flash memory device, is prevented from being written to more than once. *Id*. at 1:18-21, 10:23-32.

5. 063 PATENT PROSECUTION HISTORY

The application that led to the issuance of the 063 Patent was originally filed with 50 claims. MICRON-1002, 10-5-2001 Application at .013-.018, *id.*, 5-13-2002 Preliminary Amendment at .063-.065. The Examiner issued a non-final rejection of all 50 claims finding they were anticipated or obvious by the disclosure in prior art reference U.S. Patent No. 6,058,047 ("Kikuchi") (MICRON-1008). *Id.*, 6-3-2003 Non-Final Rejection at .077-.081. The claims at issue in this Petition, claims 42, 43, and 44 (original claims 47, 48, and 49) were rejected as being obvious over Kikuchi. *Id.* The Examiner contended that Kikuchi disclosed that the number of writes could be limited to 100,000 or 1,000,000 times and it would have been obvious to limit the number of writes to 1. *Id.* at .080. In response, the Applicant argued that Kikuchi taught away from limiting the number of writes to 1 because Kikuchi explained that the blocks may still be writeable even after reaching the predetermined number of writes, *e.g.*, 100,000 or 1,000,000 times. *Id.*, 2003-9-11 Applicant Remarks at .102-.103. The Examiner subsequently allowed claims 42, 43, and 44. *Id.*, 12-17-2003 Non-Final Rejection at .111-.115.

6. CLAIM CONSTRUCTION[3]

6.1. Applicable Law

A claim subject to *inter partes* review is given the "broadest reasonable construction in light of the specification of the patent in which it appears."[4] 37 C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

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[3] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 063 Patent for failure to satisfy the requirements of 35 U.S.C. § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 063 Patent.

[4] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill in the art and consistent with the specification of the 063 Patent. Petitioner respectfully submits that the following terms should be construed for this IPR:

6.2.1. "write-many memory device"/"write-many memory cell" (claims 42, 43, 44)

The terms "write-many memory device" and "write-many memory cell" are limitations of independent claim 42 of the 063 Patent, and accordingly also limitations of dependent claims 43 and 44. Specifically, claim 42 recites "[a] method for creating a write-once memory device from a write-many memory device" and "providing a memory device comprising a memory array comprising a plurality of write-many memory cell [sic]." MICRON-1001, 063 Patent at Claim 42. The 063 Patent describes that the write-many memory device can be written to many times. *Id*. at 2:19-23, 3:56-61. Indeed, the 063 Patent asserts that there were "no write-many memory devices that control the number of allowable writes (or re-writes) to the memory device." *Id*. at 1:12-14. The 063 Patent also describes that "memory device" and "storage device" are used interchangeably. *Id*. at 2:18-19. Thus, under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of

"write-many memory device" in the context of the 063 Patent to mean "**an electronic storage device to which data can be written more than once**." MICRON-1003, Baker Decl. ¶¶ 52-53.

Likewise, the 063 Patent discusses that the write-many memory device, such as flash memory, has memory cells that can be written to many times. MICRON-1001, 063 Patent at 5:43-57. Thus, under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "write-many memory cell" to mean "**a memory cell to which data can be written more than once**." MICRON-1003, Baker Decl. ¶¶ 54-55.

6.2.2. "manufacturer" (claim 44)

The term "manufacturer" is a limitation of dependent claim 44 of the 063 Patent. Specifically, claim 44 recites that "at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device." MICRON-1001, 063 Patent at Claim 44. The patentee acted as his own lexicographer with respect to the term "manufacturer." The 063 Patent defines a "manufacturer" as follows:

> As used herein, a "manufacturer" of a memory device refers to any party who handles the memory device before it is sold or distributed to an end user (e.g., a consumer). A "manufacturer" can include a party involved in the manufacturing, assembly, packaging, sale, or distribution of the memory device.

Id. at 3:61-67. Thus, under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "manufacturer" to mean "**any party who handles the memory device before it is sold or distributed to an end user, including a party involved in the manufacturing, assembly, packaging, sale or distribution of the memory device**." MICRON-1003, Baker Decl. ¶ 57.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 063 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design of memory devices. An individual with an advanced degree in a relevant field would require less experience in the design of memory devices. MICRON-1003, Baker Decl. ¶ 19.

8. DESCRIPTION OF THE PRIOR ART

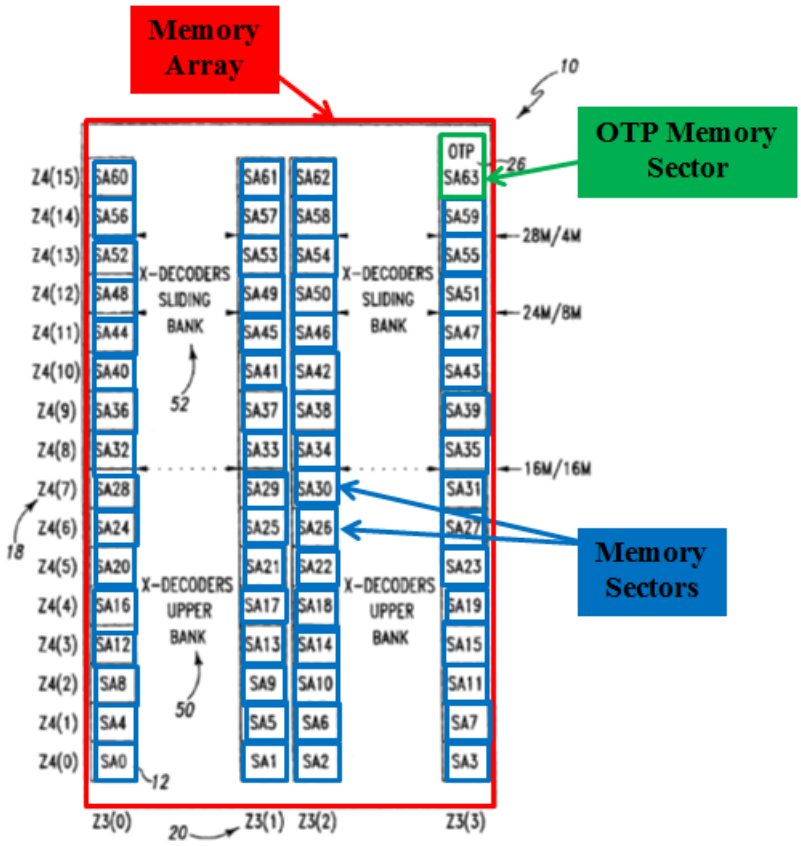
8.1. U.S. Patent No. 6,662,262 ("Kasa")

U.S. Patent No. 6,662,262 ("Kasa") (MICRON-1005) was filed on October 19, 1999 and issued on December 9, 2003 to Yasushi Kasa, Johnny Chung-Lee Chen, Guowei Wang, and Tiao-Hua Kuo. It is entitled "OTP Sector Double Protection for a Simultaneous Operation Flash Memory." The original assignee of Kasa was Advanced Micro Devices, Inc. and Fujitsu Limited. Kasa is prior art to

the 063 Patent under 35 U.S.C. § 102(e) because Kasa was filed almost two years before the 063 Patent Application was filed.

Like the 063 Patent, Kasa is directed to flash memory. MICRON-1005, Kasa at 3:47-48. In addition, like the 063 Patent, Kasa describes a method of preventing more than a single write to a portion of the flash memory device. *Id*. at 1:47-48. Specifically, Kasa describes creating a one-time programmable ("OTP") sector of memory in the flash memory device. *Id*.

Kasa describes that the flash memory device includes an array of storage sectors that include memory cells. *Id.* at 2:60-65, 5:3-5, 5:35-45, Fig. 1. One of those storage sectors is an OTP sector. *Id.* at 3:61-4:4. The OTP sector can be programmed during fabrication to include code data and then locked so that a user cannot alter the data. *Id*. at 3:19-44, 3:61-4:4, 4:33-62. The flash memory device is illustrated below in Fig. 1:



MICRON-1005, Kasa at Figure 1 (with annotations).

The OTP sector of the flash memory device has dual write protection. *Id*. at 1:14-18, 3:3:47-48, 4:18-32, 10:60-11:9, 11:10-32. This is done using two content addressable memories ("CAM") that can be used to store data. *Id*. at 4:8-10. There is an OTP sector write-protect CAM and an OTP sector lock CAM. *Id*. at 4:50-62. After the code data is programmed during fabrication, the OTP sector write-protect CAM is programmed. *Id*. at 4:41-44. This prevents the data in the OTP sector from being changed while the data is being tested. *Id*. After in-house testing occurs, the OTP sector lock CAM is programmed, preventing the OTP

sector write-protect CAM from being altered. *Id*. at 4:44-49. This provides for dual write protection for the OTP sector.

Like the 063 Patent, the flash memory device in Kasa can be used in computers, personal digital assistants, cellular telephones and other electronic systems. *Id*. at 1:21-23.

8.2. U.S. Patent No. 5,999,447 ("Naura")

U.S. Patent No. 5,999,447 ("Naura") (MICRON-1007) was filed on November 25, 1998 and it claims priority to an application filed in France on November 28, 1997. Naura issued on December 7, 1999 to David Naura and Sebastien Zink. It is entitled "Non-volatile Electrically Erasable and Programmable Memory." The original assignee of Naura was STMicroelectronics S.A. Naura is prior art to the 063 Patent under 35 U.S.C. § 102(b) because the patent issued more than one year before the application for the 063 Patent was filed. Naura accordingly is not redundant of Kasa because the patent owner cannot swear behind it, as Naura is 35 U.S.C. § 102(b) prior art. In addition, Naura is not redundant because it teaches a state bit. The state bit (*i.e.*, the "OTP bit") indicates whether the OTP portion of the memory has been programmed. MICRON-1007, Naura at 1:31-35. The state bit has one value if the OTP portion is programmed and the complimentary value if it has not been programmed *Id*.

Like the 063 Patent, Naura describes a write-many memory device, specifically an "[e]lectrically erasable and programmable non-volatile memory device[]." MICRON-1007, Naura at 1:11-13. The memory device "comprises a memory array having a plurality of memory cells each for storing an information bit." *Id*. at 2:51-52. The "cells of the memory array" can be subjected to "repeated write and erase cycles." *Id*. at 3:1-3.

This device can include a row of memory cells in the memory array that can only be programmed once. *Id*. at 1:15-16, 1:25-27. This row of memory cells is called an "OTP row" because it is one-time programmable. *Id*. at 1:25-27, 5:19-28. There is also an OTP bit which is programmed once data has been written into the OTP row. *Id*. at 1:34-37. If the OTP bit is programmed, then the memory will not allow another write operation to the OTP row. *Id*. at 1:32-50. The memory has means to permit writing into the row, depending on the value of the OTP bit. *Id*. at 1:36-38. The OTP bit can be a special bit in the OTP row in the memory array or alternatively can be a supplementary cell outside the memory array. *Id*. at 1:35-50, 2:66-3:3, 5:19-23, 5:34-43. The invention in Naura is to transfer the OTP bit from the memory array, where it was subject to deterioration caused by high voltages needed to program and erase the cells of the memory array, to a supplementary cell that is not part of the memory array. *Id*. at 1:41-45, 2:66-67. Naura implements

this change because it is important for the OTP bit to maintain its value so that the OTP row is not wiped out by a new write operation. *Id*. at 5:40-43.

Like the 063 Patent, Naura describes that this memory device can be used in electronic systems. *Id*. at 1:11-21. Moreover, manufacturing references registered by the manufacturer of an electronic system, such as date of manufacture, can be programmed into this OTP row. *Id*.

8.3. Brian Dipert and Markus Levy, *Designing With Flash Memory* (2d ed. 1994)

Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards ("Dipert") (MICRON-1006) was authored by Brian Dipert and Markus Levy. It was published in April 1994. Dipert is prior art to the 063 Patent under 35 U.S.C. § 102(b) because the textbook was published more than one year before the application for the 063 Patent was filed.

Dipert is a textbook that describes the basic features of flash memory and how flash memory is used with other electronic devices. Particular disclosures of Dipert relevant to the challenged claims are discussed below.

9. GROUND #1: CLAIMS 42 AND 44 OF THE 063 PATENT IS UNPATENTABLE AS ANTICIPATED BY KASA

As explained below, claims 42 and 44 of the 063 Patent are unpatentable as anticipated by Kasa under 35 U.S.C. § 102(e). Kasa discloses all of the limitations of claims 42 and 44 of the 063 Patent, and therefore anticipates these claims.

9.1. Claim 42 is anticipated by Kasa

9.1.1. [42.P] "A method for creating a write-once memory device from a write-many memory device, the method comprising:"

To the extent the preamble is limiting, Kasa discloses a method for creating a write-once memory device from a write-many memory device. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, claim [42.P]. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "write-many memory device" in the context of the 063 Patent to mean "an electronic storage device to which data can be written more than once." *Id.* ¶¶ 52, 53.

Specifically, Kasa describes a flash memory device that can be written to many times. MICRON-1005, Kasa at 1:35-38, 3:18-30, 3:47-48, 5:24-27, 5:35-38. A flash memory device is one example of a write-many memory device in the 063 Patent. MICRON-1001, 063 Patent at 1:19-21. Accordingly, the flash memory device described in Kasa, like the flash memory device described in the 063 Patent, is a write-many memory device.

Kasa also describes that the flash memory device includes a one-time programmable ("OTP") sector. MICRON-1005, Kasa at 3:34-36, Fig. 1. The OTP sector has the same structure as the other sectors in the flash memory device and can be erased and re-programmed unless a write-protect content addressable memory ("CAM") is programmed. *Id*. at 3:54-60, 4:5-17. If the write-protect CAM is programmed, the OTP sector cannot be written to again. *Id*. at 3:61-4:4, 4:35-49, 4:59-62, 6:46-54, Fig. 1. Kasa describes that the OTP sector is programmed during fabrication with code and then write protected before being distributed to the user. *Id*. Accordingly, the OTP sector is a write-once memory device that is included in the write-many memory device. MICRON-1003, Baker Decl., Appx. A at Ground 1, claim [42.P]. Further details regarding the structure and operation of creating an OTP sector within the flash memory device are discussed below in claim limitations [42.1] and [42.2].

Thus, by disclosing an OTP sector (*i.e.,* the "write-once memory device") within the flash memory device (*i.e.,* the "write-many memory device"), Kasa discloses a method for creating a write-once memory device from a write-many memory device.

9.1.2. [42.1] "(a) providing a memory device comprising a memory array comprising a plurality of write-many memory cell [sic]; and"

Kasa discloses providing a memory device comprising a memory array comprising a plurality of write-many memory cells. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, claim [42.1]. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "write-many memory cell" in the context of the 063 Patent to mean a "memory cell to which data can be written more than once." *Id.* ¶¶ 54, 55.

Kasa describes a flash memory device. MICRON-1005, Kasa at 1:35-38, 3:47-48, 5:24-27, 5:35-38. The flash memory device includes an array of sectors. *Id*. at 5:3-5 ("FIG.1 illustrates a block diagram of an array of sectors in a flash memory…"); 5:35-45, Fig. 1. Furthermore, Kasa describes that the flash memory device includes an array of sectors that includes memory cells. *Id*. at 2:60-65 ("[E]ach sector includes a set of memory cells"); 2:38-40, 5:48-59. Accordingly, Kasa describes a flash memory device comprising a memory array comprising a plurality of memory cells. This is further confirmed by U.S. Patent No. 5,847,998 ("Van Buskirk") (MICRON-1009) which is incorporated by reference into Kasa (MICRON-1005, Kasa at 2:60-3:17), which further explains that a flash memory

device includes a memory array with memory cells. MICRON-1009, Van Buskirk at Abstract, 2:67-3:4, 3:13-23, 3:64-4:3.

Furthermore, Kasa explains that the memory cells in the flash memory device can be written more than once. MICRON-1005, Kasa at 1:46-52, 3:18-33, 4:1-4. Indeed, the 063 Patent specifically identifies a flash memory device as including memory cells that can be written more than once. MICRON-1001, 063 Patent at 5:51-53 ("However, with other write-many technologies, such as Flash memory, the cells of a block must be returned to their un-programmed digital state before new data can be written into the block."). Accordingly, just like the memory cells in the flash memory device in the 063 Patent are write-many memory cells, the memory cells in the flash memory device in Kasa are write-many memory cells.

9.1.3. [42.2] "(b) rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to said at least some of the write-many memory cells."

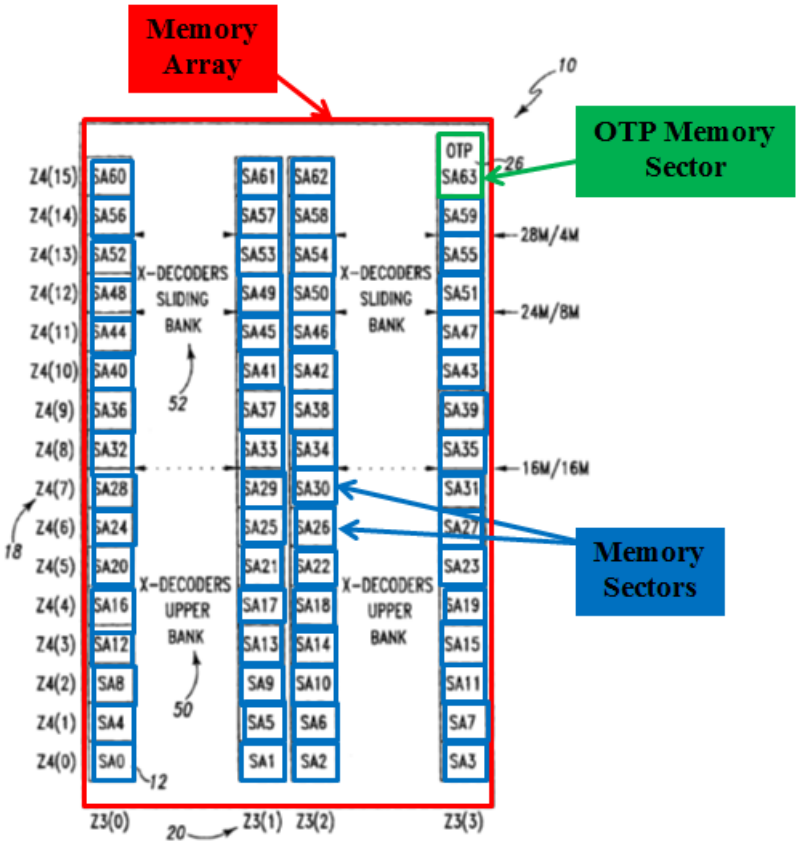
Kasa discloses rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to at least some of the write-many memory cells. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, claim [42.2]. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "write-many memory cell" in the context of the

063 Patent to mean a "memory cell to which data can be written more than once." *Id.* ¶¶ 54, 55.

Kasa explains that it is necessary to write protect portions of the flash memory (*i.e.*, the "write-many memory device") to protect, for example, program code that is used to execute various operations that the flash memory is capable of performing. MICRON-1005, Kasa at 3:18-30. Accordingly, it is necessary to include an OTP sector in the memory device, which cannot be erased or reprogrammed. *Id*. at 3:31-37.

Kasa describes a method for preventing more than one write to one of the memory sectors, which includes memory cells, in the flash memory device. *Id*. at 3:61-4:4 ("The flash memory cells in the OTP sector are programmed during fabrication and then locked out after testing so that the user cannot change the data content in the OTP sector.") Kasa describes that this is done using content addressable memory ("CAM"). *Id*. at 4:8-10. Specifically, the OTP sector is protected by programming an OTP write-protect CAM and an OTP sector lock CAM. *Id*. at 4:17-32. The OTP write-protect CAM prevents the OTP sector from being changed, while the OTP sector lock CAM prevents the OTP write-protect CAM from being changed. *Id*. at 4:50-62, 11:10-32. The OTP sector, like any other sector in the flash memory, can be erased and re-programmed unless the OTP

write-protect CAM is programmed. *Id*. at 4:5-17. The OTP sector is illustrated in Fig. 1, below. *Id*. at 7:21-28.



MICRON-1005, Kasa at Figure 1 (with annotations).

The OTP sector is programmed during fabrication, locked during in-house testing by programming the OTP write-protect CAM, and then after testing is completed the OTP sector is permanently locked by programming the OTP sector lock CAM. *Id*. at 4:35-49.

Thus, Kasa discloses preventing more than one write to memory cells in the OTP sector of the flash memory device (*i.e.*, creating "write-once memory cells"

from the "write-many memory cells") by programming the OTP write-protect CAM and OTP sector lock CAM. MICRON-1005, Kasa at 4:1-4, 4:59-62, 4:35-49, 6:46-54.

9.2. Claim 44 is anticipated by Kasa

9.2.1. [44.P] "The invention of claim 42, wherein"

See analysis for claim 42 in Section 9.1 above.

9.2.2. [44.1] "said at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device."

See analysis for claim 42 in Section 9.1 above.

Kasa discloses that at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, claim [44.1]. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "manufacturer" in the context of the 063 Patent to mean "any party who handles the memory device before it is sold or distributed to an end user, including a party involved in the manufacturing, assembly, packaging, sale or distribution of the memory device." *Id.* ¶ 57. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary

meaning of "write-many memory cell" in the context of the 063 Patent to mean a "memory cell to which data can be written more than once." *Id.* ¶¶ 54, 55.

Kasa explicitly states that the "memory manufacturer" includes the OTP sector in the flash memory device. MICRON-1005, Kasa at 3:61-4:4 ("As set forth above, some peripheral devices that use flash memory have generated a need for memory manufacturers to include at least one sector that is designated as an OTP sector.") Moreover, Kasa explains that the OTP sector is programmed during fabrication and then locked so that a user cannot alter the code that has been programmed in the OTP sector. MICRON-1005, Kasa at 3:21-30, 3:61-4:4, 4:21-24, 4:35-49, 6:50-54, 11:10-32. One of ordinary skill in the art would have understood that a manufacturer of the memory device would be involved during the fabrication of the memory device and certainly before it is distributed to the end user. *See* MICRON-1003, Baker Decl., Appx. A at Ground 1, claim [44.1].

10. GROUND #2: CLAIM 43 OF THE 063 PATENT IS UNPATENTABLE OVER KASA IN VIEW OF DIPERT

10.1. Claim 43 is obvious over Kasa in view of Dipert

As explained below, claim 43 of the 063 Patent is unpatentable over Kasa in view of Dipert under 35 U.S.C. § 103(a). Kasa in view of Dipert renders obvious all of the limitations of claim 43 of the 063 Patent, and therefore renders the claim obvious. In particular, Kasa discloses that the flash memory device can be used with a host device, such as a computer or personal digital assistant. Dipert, a

textbook, supplements the teachings of Kasa and explains that that memory, including flash memory, has long been used in memory cards.

One of ordinary skill in the art would have been motivated to combine Kasa and Dipert. MICRON-1003, Baker Decl. ¶¶ 79-80. First, Dipert was a well-known textbook about flash memories in the 1990s. *Id*. ¶ 81. Those of ordinary skill in the art would have understood that Dipert was a good resource to consider when considering design options for flash memory. *Id*. Given that Kasa also describes a flash memory device (MICRON-1005, Kasa at 3:47-48), one of ordinary skill in the art would have been motivated to consider the teachings of Dipert when implementing improvements in the field. *Id.*; *see also* MICRON-1006, Dipert at Title (.001), .033, .040. Second, one of ordinary skill in the art would have understood that combining Kasa and Dipert amounts to combining known methods to yield predictable results. MICRON-1003, Baker Decl. ¶ 82. Both Kasa and Dipert discuss flash memory devices. MICRON-1005, Kasa at 3:47-48; MICRON-1006, Dipert at .030, .037, .078. Placing flash memory on a memory card was a design choice with respect to utilization of flash memory and was textbook material well before the 063 Patent was filed. MICRON-1003, Baker Decl. ¶ 82. It was understood to yield predictable results because it was so well known. *Id*. For example, it allowed a user to transfer data between a portable computer and a desktop workstation. MICRON-1006, Dipert at .037.

10.1.1. [43.P] "The invention of claim 42, wherein"

See analysis for claim 42 in Section 9.1 above.

10.1.2. [43.1] "the memory device comprises a modular memory device that is removably couplable [sic] with a host device."

See analysis for claim 42 in Section 9.1 above.

Kasa in view of Dipert renders obvious that the memory device comprises a modular memory device that is removably couplable with a host device. *See* MICRON-1003, Baker Decl., Appx. A at Ground 2, claim [43.1].

The 063 Patent describes that the memory device could be on a "modular device," such as a "card," and be removable from a host device such as "a personal digital assistant, a cellular telephone, or a general purpose computer." MICRON-1001, 063 Patent 2:60-3:10. Kasa, like the 063 Patent, describes that the flash memory device can be used with computers, personal digital assistants, cellular telephones and other electronic systems and devices. MICRON-1005, Kasa at 1:21-34. Kasa does not explicitly disclose that the flash memory device could be on a memory card. However, it would have been obvious to one of ordinary skill in the art that the flash memory could have been included on a removable memory card. MICRON-1003, Baker Decl., Appx. A at Ground 2, claim [43.1]. It was merely a design choice for one of skill in the art. *Id*.

Indeed, Dipert describes that memory cards had been around for many years. MICRON-1006, Dipert at .078. One example of a memory card is a flash memory card. *Id*. at .037, .060, .163, .174, Table 4.1 (at .082). Flash memory devices can be placed on flash memory cards. *Id*. The dominant memory interface for flash memory cards was the PCMICIA memory card. *Id*. at .175-.176. Dipert further describes that a memory card was a removable device that could be used to exchange information between, for example, a portable computer and a desktop computer. *Id*. at .030, .037, .078, .161, Fig. 2.3 (at .038). It would have been obvious to include the flash memory in Kasa on a memory card so that it could be used with, for example, a desktop computer or a portable computer. MICRON-1003, Baker Decl., Appx. A at Ground 2, claim [43.1].

Thus, Kasa in view of Dipert discloses that a flash memory device could be included on a memory card and thus be "removably couplable [sic]" with a host device, such as a computer or personal digital assistant.

11. GROUND #3: CLAIM 42 OF THE 063 PATENT IS UNPATENTABLE AS ANTICIPATED BY NAURA

As explained below, claim 42 of the 063 Patent is unpatentable as anticipated by Naura under 35 U.S.C. § 102(b). Naura discloses all of the limitations of claim 42 of the 063 Patent, and therefore anticipates this claim.

11.1. Claim 42 is anticipated by Naura

11.1.1. [42.P] "A method for creating a write-once memory device from a write-many memory device, the method comprising:"

To the extent the preamble is limiting, Naura discloses a method for creating a write-once memory device from a write-many memory device. *See* MICRON-1003, Baker Decl., Appx. A at Ground 3, claim [42.P]. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "write-many memory device" in the context of the 063 Patent to mean "an electronic storage device to which data can be written more than once." *Id.* ¶¶ 52, 53.

Specifically, Naura describes an electrically erasable and programmable non-volatile memory device. MICRON-1007, Naura at 1:11-21, 2:40-44. The memory device in Naura can be written to many times. *Id*. at 1:41-50, 2:66-3:3, 5:15-17, 5:34-43. Accordingly, the memory device described in Naura is a write-many memory device.

Naura also describes that a row of the memory array in the memory device can be turned into a one-time programmable ("OTP") row. *Id*. at 3:61-4:4, 4:59-62, 6:46-54. The memory cells in the OTP row have the same structure as the rest of the memory cells in the memory device. *Id*. at 1:28-31 ("Since the memory cells of the OTP row have the same structure as those of the rest of the memory

array…"). In addition, Naura discloses a state bit, called the "OTP bit." *Id*. at 1:31-33; 2:66-3:3. The OTP bit indicates whether the OTP row has been programmed or not. *Id*. at 1:31-35 ("[A]n OTP bit contains either a logic 0 value or a logic 1 value when the OTP row is blank. … If the OTP row is programmed it has the complementary logic value.") The OTP row can only be written to once because it is protected by the OTP bit. *Id*. at 1:13-28, 1:31-40, 1:41-48, 2:40-44, 5:19-28. Accordingly, the OTP row is a write-once memory device that is included in the write-many memory device. *Id*. Further details regarding the structure and operation of creating an OTP row within the memory device are discussed below in claim limitations [42.1] and [42.2].

Thus, by disclosing an OTP row (*i.e.*, the "write-once memory device") within the memory device (*i.e.*, the "write-many memory device"), Naura discloses a method for creating a write-once memory device from a write-many memory device.

11.1.2. [42.1] "(a) providing a memory device comprising a memory array comprising a plurality of write-many memory cell [sic]; and"

Naura discloses providing a memory device comprising a memory array comprising a plurality of write-many memory cells. *See* MICRON-1003, Baker Decl., Appx. A at Ground 3, claim [42.1]. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood

the plain and ordinary meaning of "write-many memory cell" in the context of the 063 Patent to mean a "memory cell to which data can be written more than once." *Id.* ¶¶ 54, 55.

Naura describes an electrically erasable and programmable non-volatile memory device. MICRON-1007, Naura at 1:11-21, 2:40-44. The memory device includes an array of memory cells. *Id*. at 2:40-56 ("The memory comprises a memory array having a plurality of memory cells each for storing an information bit…"), 1:11-15, 1:22-24, 3:19-20, 3:40-47, 4:34-38, Fig. 1. These memory cells in the memory array can be written more than once. *Id*. at 2:66-3:3 ("[T]he cells of the memory array are subjected to through [sic] repeated write and erase cycles…"), 1:43-50, 5:15-17, 5:34-43. Accordingly, the memory cells in the array in the memory device in Naura are "write-many memory cells." Accordingly, Naura describes a write-many memory device that includes a memory array of write-many memory cells.

11.1.3. [42.2] "(b) rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to said at least some of the write-many memory cells."

Naura discloses rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to at least some of the write-many memory cells. *See* MICRON-1003, Baker Decl., Appx. A at Ground 3, claim [42.2]. Under the broadest reasonable

interpretation, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "write-many memory cell" in the context of the 063 Patent to mean a "memory cell to which data can be written more than once." *Id.* ¶¶ 54, 55.

Naura explains that it is necessary to make a portion of the write-many memory device one-time programmable to contain, for example, manufacturing data. MICRON-1007, Naura at 1:13-21. These one-time programmable cells in the memory device can be a row of the memory array known as the "OTP row." *Id*. at 1:11-16, 1:21-31, 1:25-27, 5:19-30. These memory cells in the OTP row are protected by a state bit called the OTP bit. *Id.* at 1:25-39, 1:46-51, 2:66-67, 5:19-30. The OTP bit can be in the OTP row in the memory array or alternatively in a supplementary cell outside the memory array. *Id*. at 1:35-39, 1:40-50, 2:66-3:3, 5:19-23, 5:34-45, Fig. 1. The OTP bit indicates whether the OTP row has been programmed or not. *Id*. at 1:31-35 ("[A]n OTP bit contains either a logic 0 value or a logic 1 value when the OTP row is blank. … If the OTP row is programmed it has the complementary logic value."). Whether the memory permits writing to the OTP row depends on the value of the OTP bit. *Id*. at 1:37-40 ("The memory has means to permit or not permit writing in the OTP row, depending on the value of this bit."), 1:46-48 ("It is important that the OTP bit keep its programmed value once it has been programmed to indicate that the OTP row is no longer blank."),

5:21-23 ("This bit relates to the blank or non-blank state of a group of memory cells designed to be programmed only once..."). Thus, Naura discloses preventing more than one write to memory cells in the OTP row of the memory device by setting the value of the OTP bit (*i.e.*, creating "write-once memory cells" from the "write-many memory cells").

12. GROUND #4: CLAIM 43 OF THE 063 PATENT IS UNPATENTABLE OVER NAURA IN VIEW OF DIPERT

12.1. Claim 43 is obvious over Naura in view of Dipert

As explained below, claim 43 of the 063 Patent is unpatentable over Naura in view of Dipert under 35 U.S.C. § 103(a). Naura in view of Dipert renders obvious all of the limitations of claim 43 of the 063 Patent, and therefore renders the claim obvious. In particular, Naura discloses that the electrically erasable and programmable non-volatile memory device can be used with an electronic system. MICRON-1007, Naura at 1:11-21. Naura also discloses, on the face of the patent, the prior art reference "Intelligent Memory Chips for Smart Cards." *Id*. at [56] References Cited. Dipert, a textbook, supplements the teachings of Naura and explains that that memory, including electrically erasable and programmable non-volatile memory, has long been used in memory cards, including smart cards.

One of ordinary skill in the art would have been motivated to combine Naura and Dipert. MICRON-1003, Baker Decl. ¶¶ 85-86. First, Dipert was a well-known textbook about electrically erasable and programmable non-volatile

memory, specifically flash memory, in the 1990s. *Id*. ¶ 87. Those of skill in the art would have understood that Dipert was a good resource to consider when considering design options for nonvolatile memory. *Id.*; *see also* MICRON-1006, Dipert at Title (at .001), .033, .040, Table 1.2 (at .024); MICRON-1006, Naura at 2:40-41. Given that Naura also describes an electrically erasable and programmable non-volatile memory device (MICRON-1007, Naura at 1:11-13, 2:40-41), one of ordinary skill in the art would have been motivated to consider the teachings of Dipert when implementing improvements in the field. MICRON-1003, Baker Decl. ¶ 87. Second, one of ordinary skill in the art would have understood that combining Naura and Dipert amounts to combining known methods to yield predictable results. MICRON-1003, Baker Decl. ¶ 88. Both Naura and Dipert discuss electrically erasable and programmable non-volatile memory devices. MICRON-1007, Naura at 1:11-13, 2:40-41; MICRON-1006, Dipert at .024, .025, .040, .089. Placing electrically erasable and programmable non-volatile memory, such as flash memory, on a memory card was a design choice with respect to utilization of flash memory and was textbook material well before the 063 Patent was filed. MICRON-1003, Baker Decl. ¶ 88; *see also* MICRON-1006, Dipert at .037, .078. It was understood to yield predictable results because it was so well known. MICRON-1003, Baker Decl. ¶ 88. For example, it

allowed a user to transfer data between a portable computer and a desktop workstation. MICRON-1006, Dipert at .037; *see also id*. at .030.

12.1.1. [43.P] "The invention of claim 42, wherein"

See analysis for claim 42 in Section 1.11 above.

12.1.2. [43.1] "the memory device comprises a modular memory device that is removably couplable [sic] with a host device."

See analysis for claim 42 in Section 11.1 above.

Naura in view of Dibert renders obvious that the memory device comprises a modular memory device that is removably couplable with a host device. *See* MICRON-1003, Baker Decl., Appx. A at Ground 4, claim [43.1].

The 063 Patent describes that the memory device could be on a "modular device," such as a "card," and be removable from a host device such as "a personal digital assistant, a cellular telephone, or a general purpose computer." MICRON-1001, 063 Patent 3:1-8. Naura, like the 063 Patent, describes that the memory device can be used with an "electronic system." MICRON-1007, Naura at 1:11-19. Moreover, on the face of Naura, one of the prior art references mentioned is entitled "Intelligent Memory Chips for Smart Cards." *Id.* at [56] References Cited. As the prior art reference illustrates, one of ordinary skill in the art would have understood that it would have been obvious to include the memory device in Naura on a memory card, such as a smart card—even though Naura does not explicitly

disclose this. *See* MICRON-1003, Baker Decl., Appx. A at Ground 4, claim [43.1]. This was merely a design choice for one of skill in the art. *Id*.

Indeed, Dipert describes that memory device in Naura could be flash memory and that including flash memory devices on memory cards had been well known for years. MICRON-1006, Dipert at .024, .025, .037, .040, .060, .078, .089, .163, .174-.176, Table 4.1 (at .082). Dipert further describes that a memory card was a removable device that could be used to exchange information between, for example, a portable computer and a desktop computer. *Id*. at .030, .037, .078, .161, Fig. 2.3 (at .038). Given the disclosure in Naura and Dipert, it would have been obvious to include the memory in Naura on a memory card to be used with a host device, such as a computer. MICRON-1003, Baker Decl., Appx. A at Ground 4, claim [43.1].

Thus, Naura in view of Dipert discloses that a flash memory device could be included on a memory card and thus be "removably couplable [sic]" with a host device, such as a computer or personal digital assistant.

13. GROUND #5: CLAIM 44 OF THE 063 PATENT IS UNPATENTABLE OVER NAURA

As explained below, claim 44 of the 063 Patent is unpatentable over Naura under 35 U.S.C. § 103(a). Naura renders obvious all of the limitations of claim 44 of the 063 Patent, and therefore renders the claim obvious.

13.1. Claim 44 is obvious over Naura

13.1.1. [44.P] "The invention of claim 42, wherein"

See analysis for claim 42 in Section 11.1 above.

13.1.2. [44.1] "said at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device."

See analysis for claim 42 in Section 11.1 above.

Naura renders obvious that at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device. *See* MICRON-1003, Baker Decl., Appx. A at Ground 5, claim [44.1]. Under the broadest reasonable interpretation, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "manufacturer" in the context of the 063 Patent to mean "any party who handles the memory device before it is sold or distributed to an end user, including a party involved in the manufacturing, assembly, packaging, sale or distribution of the memory device." *Id.* ¶ 57. Under the broadest reasonable interpretation, a person of ordinary skill in the art would have understood the plain and ordinary meaning of "write-many memory cell" in the context of the 063 Patent to mean a "memory cell to which data can be written more than once." *Id.* ¶¶ 54-55.

Naura explains that the memory device is protected by an OTP bit in the OTP row or in a supplementary memory cell. MICRON-1007, Naura at 1:35-39,

1:40-50, 2:66-3:3, 5:19-23, 5:34-43. Naura does not explicitly disclose that the OTP bit was created by the memory device manufacturer. However, one of ordinary skill in the art would have understood that the manufacturer of the memory device could be the entity that would include the OTP bit in the device and thereby render some of the write-many memory cells as one time programmable cells. *See* MICRON-1003, Baker Decl., Appx. A at Ground 5, claim [44.1].

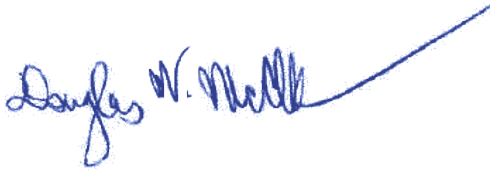
Moreover, Naura explains that the OTP row can be used to include manufacturing references registered by the manufacturer of an electronic system. MICRON-1007, Naura at 1:16-21. Naura also explains that the OTP row is designed to be programmed once by the "user" where the user is a "designer of an electronic system containing the memory." *Id*. at 5:21-25. Although Naura does not explicitly state that the manufacturer of the memory device would be the entity that would program those manufacturing references into the memory device, one of ordinary skill in the art would have understood that a manufacturer could actually program that OTP data (*i.e.,* the manufacturing references) into the memory device before it was distributed to a user. *See* MICRON-1003, Baker Decl., Appx. A at Ground 5, claim [44.1].

Accordingly, it would have been obvious to one of ordinary skill in the art that the manufacturer could render some of the write-many memory cells in the memory array as write-once memory cells. *Id.*

14. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 42, 43 and 44 of the 063 Patent is requested.

Respectfully submitted,



Dated: December 14, 2015

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	December 14, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 7,000,063 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1014
Persons served	Patent Owner's Address of Record: Martin A. Farber 866 United Nations Plaza New York, NY 10017-1872 Additional Addresses Known as Likely to Effect Service: Brian E. Farnan Farnan LLP 919 North Market Street, 12th Floor Wilmington, DE 19801 bfarnan@farnanlaw.com Edward C. Flynn Cohen & Grace, LLC 105 Braunlich Drive, Suite 300 Pittsburgh, PA 15237 eflynn@cohengrace.com

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