UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

INNOVATIVE MEMORY SYSTEMS, INC.
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 7,045,849
Title: USE OF VOIDS BETWEEN ELEMENTS IN SEMICONDUCTOR STRUCTURES FOR ISOLATION

Petition For *Inter Partes* Review of U.S. Patent No. 7,045,849 Under 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

***Mail Stop* "PATENT BOARD"**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

Page

Exhibit List

Micron Exhibit #	Description
MICRON-1001	U.S. Patent No. 7,045,849 ("849 Patent")
MICRON-1002	File History for U.S. Patent No. 7,045,849
MICRON-1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 6,720,612 ("Takeuchi")
MICRON-1006	Lee, Jae-Duk et al., *Effects of Floating Gate Interference on NAND Flash Memory Cell Operation* (2002) ("Lee")
MICRON-1007	JP Patent Application Publication No. 2000-100976 ("Sato")
MICRON-1008	Cappelletti, Paulo et al., *Flash Memories* (1999) ("Cappelletti")
MICRON-1009	U.S. Patent No. 5,867,429 ("Chen")
MICRON-1010	D. Kahng and S.M. Sze, *A Floating Gate and Its Application to Memory Devices* (May 16, 1967) ("Kahng")
MICRON-1011	B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994) ("Dipert")
MICRON-1012	Matsuoka , Fujio et. al., *New Ultra High Density EPROM and Flash EEPROM with NAND Structure Cell* (1987) ("Matsuoka")
MICRON-1013	U.S. Patent No. 6,888,755 ("Harari")
MICRON-1014	United States Copyright Office public record search result for B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994)
MICRON-1015	Declaration of Lisa Rowlison de Ortiz regarding Lee, Jae-Duk et al., *Effects of Floating Gate Interference on NAND Flash Memory Cell Operation* ("Rowlinson de Oritz Declaration")

Micron Exhibit #	**Description**
MICRON-1016	Declaration of Lisa Browar regarding B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994) ("Browar Declaration")
MICRON-1017	Declaration of Sharon Wiles-Young regarding B. Dipert and M. Levy, *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* (1994) ("Wiles-Young Declaration")
MICRON-1018	U.S. Patent No. 6,376,330 (Fulford)

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-6 of U.S. Patent No. 7,045,849, titled "Use of Voids Between Elements in Semiconductor Structures for Isolation" (MICRON-1001, the "849 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR *INTER PARTES* REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 849 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 849 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang Registration No. 73,604 (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Douglas W. McClellan Registration No. 41,183 (doug.mcclellan@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5313; F: 713-224-9511

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for Petitioner is

attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Innovative Memory Systems has asserted the 849 Patent and U.S. Patent Nos. 6,169,503 (the "503 Patent"), 6,324,537 (the "537 Patent"), 6,901,498 (the "498 Patent"), 7,000,063 (the "063 Patent"), 7,085,159 (the "159 Patent"), 7,495,953 (the "953 Patent) and 7,886,212 (the "212 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Innovative Memory Systems, Inc., v. Micron Tech., Inc.*, 14-cv-1480 (D. Del.) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 6,169,503, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 6,324,537, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 6,901,498, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,000,063, IPR2016-

Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,085,159, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,495,953, IPR2016-Unassigned; and Petition for *Inter Partes* Review of U.S. Patent No. 7,886,212, IPR2016-Unassigned.[1]

The 849 Patent does not claim priority to any prior U.S. patent applications. According to USPTO records, and to the best of Petitioner's knowledge, the following U.S. applications and patents claim priority to the application that led to the issuance of the 849 Patent: U.S. Patent App. No. 11/210,218 filed on August 22, 2005, now U.S. Patent No. 7,569,465. To the best of Petitioner's knowledge, the U.S. patent that claims priority to the 849 Patent has not been asserted in litigation and is not the subject of any co-pending USPTO proceedings.

2.5. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 849 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

[1] These petitions will be filed concurrently or within a few days.

Ground #1: Claims 1-6 of the 849 Patent are invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that they are obvious over U.S. Patent No. 6,720,612 ("Takeuchi"), entitled "Semiconductor Device," filed on March 15, 2002 and issued on April 13, 2004, in view of Lee, Jae-Duk et al., *Effects of Floating-Gate Interference on NAND Flash Memory Cell Operation* ("Lee"), which was published and publically known at least as early as May 15, 2002. Takeuchi is attached as MICRON-1005, and Lee is attached as MICRON-1006.

Ground #2: Claims 1-6 of the 849 Patent are invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that they are obvious over Japanese Patent Application Publication No. 2000-100976 ("Sato"), entitled "Semiconductor Memory Device and Manufacture Thereof," filed on September 21, 1998 and published April 7, 2000, in view of Lee. A certified English translation of Sato, as well as a certificate of translation by Magdalena Kawalkowski and original Japanese application, is attached as MICRON-1007.

These grounds are explained below and are supported by the Declaration of Dr. R. Jacob Baker (MICRON-1003, "Baker Decl.").

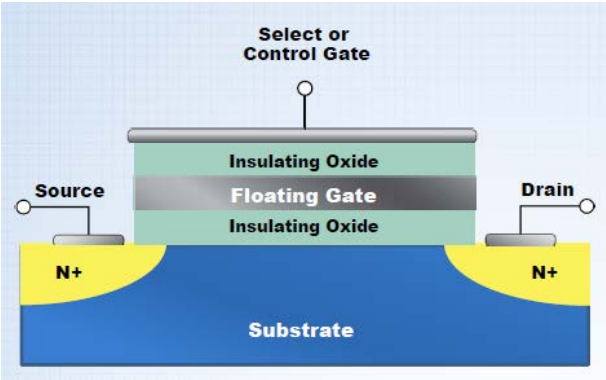
The Proposed Grounds Are Not Redundant: Petitioner's grounds for institution are not redundant because both Sato and Lee, in Ground #2, are prior art under 35 U.S.C. § 102(b) and cannot be sworn behind as a defense to invalidity, whereas, in Ground #1, Takeuchi is not prior art under § 102(b).

4. OVERVIEW OF THE 849 PATENT

The 849 Patent was filed on May 21, 2003 and issued on May 16, 2006. The 849 Patent "relates generally to the isolation of tightly packed elements in semiconductor structures, and, more specifically, to the electric field isolation of neighboring charge storage elements of non-volatile flash electrically erasable and programmable read-only memory (flash EEPROM) cell arrays." MICRON-1001, 849 Patent at 1:7-12.

4.1. Technology Background

As was well known in the art, the building block of a non-volatile flash memory array is a single flash memory cell. MICRON-1003, Baker Decl. ¶ 27. As a general matter, individual memory cells within a non-volatile flash memory array use a field-effect transistor ("FET") which includes a source, a drain, and a floating gate which can store electrical charge. *Id.* ¶ 29; *see also* MICRON-1001, 849 Patent at 2:54-61.



MICRON-1003, Baker Decl. ¶ 30.

Shown above is a cross-section of an exemplary flash memory cell in a

conventional stack configuration.[2] Each memory cell includes a first insulating oxide formed on a semiconductor substrate, also commonly referred to as a tunneling oxide, a floating gate formed on the tunneling oxide, followed by a second insulating oxide and a select or control gate formed on the second insulating oxide. MICRON-1003, Baker Decl. ¶ 30; *see generally* MICRON-1001, 849 Patent at 5:56-6:39 (describing formation of flash memory structure). By applying appropriate bias voltages across the FET, sense amplifier circuitry can determine whether current is flowing across the source to drain, and therefore determine whether charge is stored in the floating gate of an individual memory cell. MICRON-1003, Baker Decl. ¶ 31. This is the mechanism by which information or data bits can be represented by the amount of stored charge in a memory cell. *Id.*

Real-world memory systems required large arrays of these floating-gate memory cells in order to store information. However, as the 849 Patent acknowledges in the background section of the patent, there were significant market pressures to both increase the amount of digital data that could be stored on

[2] A flash memory cell in a conventional stack configuration is one wherein the control gate is formed upon and aligned with the floating gate such that the control gate is stacked on the floating gate. MICRON-1003, Baker Decl. ¶ 30.

a given area of a silicon substrate and to shrink the overall size of the device. MICRON-1001, 849 Patent at 2:8-16.

One way the data storage density of non-volatile memory arrays was increasing was the shrinking of the horizontal dimensions of individual memory cells as a result of improvements in integrated circuit manufacturing techniques. S*ee id.* at 3:50-53 (describing the spacing between memory cells was decreasing "as the result of improvements of integrated circuit manufacturing techniques"); MICRON-1003, Baker Decl. ¶¶ 37-39. Indeed, on average there had been a factor of two reduction in cell dimensions every four years from 1967 until the early 2000's. *Id.* (citing MICRON-1008, Cappelletti at .051). This naturally allowed for increased storage density on a given area of silicon substrate.

A second way of increasing the data storage density was to store more than one bit of data per cell. MICRON-1001, 849 Patent at 2:16-24. Namely, the use of higher precision circuitry allows "levels" of charge to be detected and distinguished in a floating gate, thus allowing more bits (*i.e.* a multi-bit memory cell) to be represented by the stored charge level on the floating gate. MICRON-1003, Baker Decl. ¶¶ 32, 38; s*ee* MICRON-1001, 849 Patent at 2:18-30 (describing multi-bit memory cells).

However, as the number of states stored in each memory cell increases, the tolerance for any shifts in the programmed charge level on the floating gate

decreases. *Id.* at 3:33-35. One cause of apparent shifts in the programmed charge level is field coupling, also referred to as parasitic capacitance, between adjacent memory cells, which "necessarily increases as the spaces between memory cell storage elements are decreased." *Id.* at 3:48-52; MICRON-1003, Baker Decl. ¶¶ 40-41. Field coupling is not unique to non-volatile flash memory devices, and refers to the unavoidable interference between parts of an electronic circuit because of the proximity of their electrical fields to one another. *Id.*

There were several known techniques for reducing the parasitic capacitance/electric field coupling between adjacent memory cells. One such technique was to add elements to the structure of the array that significantly reduce the amount of electric field coupling between floating gates of adjacent cells. MICRON-1001, 849 Patent at 4:1-4. For example, it was well known that control gate lines, which run across rows of floating gates, could be extended downward between the floating gates. *Id.* at 4:1-8. In this way, the control gate serves to shield a floating gate from adjacent floating gates on opposite sides along a row. *Id.*; MICRON-1003, Baker Decl. ¶ 42.

An alternative to providing a conductive shield is to use a dielectric material between adjacent conductors. *Id.*; MICRON-1009, Chen at 6:33-36[3]. However,

[3] U.S. Patent No. 5,867,429 ("Chen") is cited within the 849 Patent as a prior art

the degree of electric coupling between adjacent conductors is increased as the dielectric constant "k" of the insulator between them increases. *Id*. at 6:41-43. The dielectric constant of silicon dioxide, the dielectric material most typically employed between adjacent memory cells, has a dielectric constant of about 4. *Id*. at 6:36-38. Silicon nitride, also used for some dielectrics along with or in place of silicon dioxide, has a dielectric constant of about 7.5. *Id*. at 6:39-41.

4.2. The 849 Patent

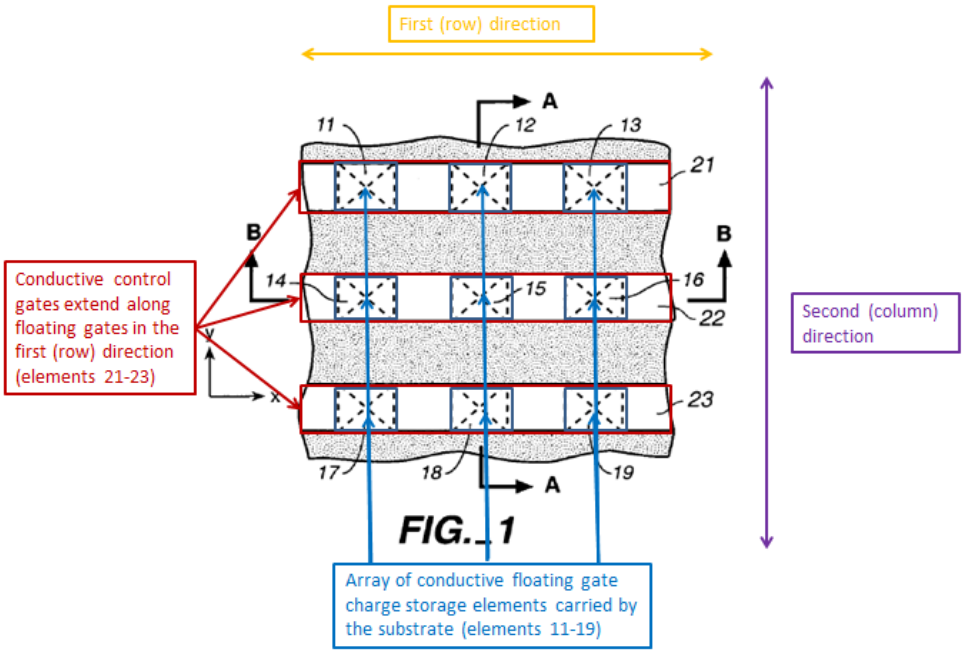
The alleged invention of the 849 Patent is the further reduction of field coupling between adjacent memory cells by providing a "dielectric between them that contains a void extending a major part of the distance between the elements instead of the usual technique of making the dielectric solid throughout the entire space between charge storage elements." MICRON-1001, 849 Patent at 4:20-24. This void reduces the capacitive coupling as compared to a solid dielectric because air has a dielectric constant of 1.0 (or a small amount above 1.0), which is significantly lower than the dielectric constant of silicon dioxide or silicon nitride. *Id*. at 4:24-34.

Challenged independent claims 1 and 2 are identical other than their final

---

description of the field coupling problem. *See* MICRON-1001, 849 Patent at 3:48-64. Chen issued on February 2, 1999 and is prior art under 35. U.S.C. § 102(b).

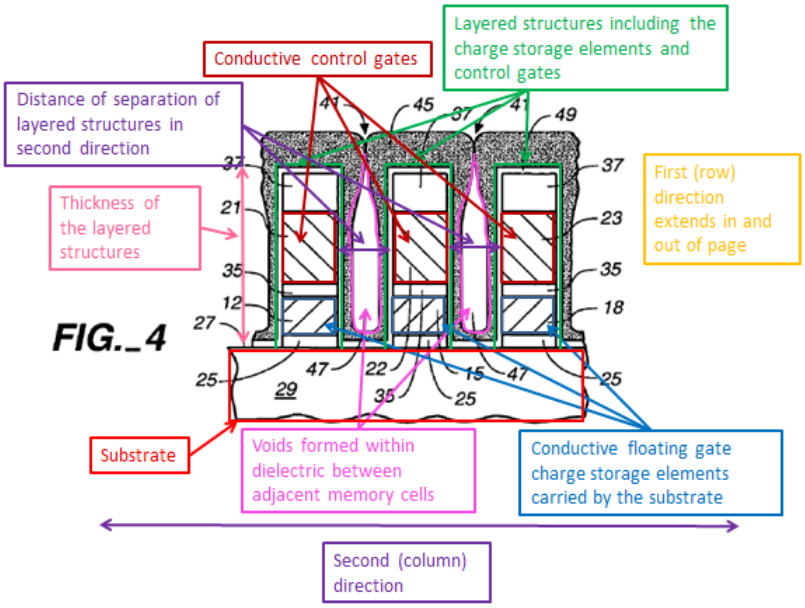
limitations. MICRON-1003, Baker Decl. ¶ 44. The common limitations are described with reference to annotated Figs. 1 and 4 below. Fig. 1 is a plan view representation of an array of floating gate memory cells regularly spaced in a first row direction and second column direction on a semiconductor substrate. MICRON-1001, 849 Patent at 5:37-41, 5:45-48. Control gates extend across and are commonly connected to memory cells in a row, and spaced apart in the column direction such that they are aligned with the floating gates. *Id.* at 5:41-45.



MICRON-1001, 849 Patent at Figure 1 (with annotations).

The structure of the individual memory cells is depicted in annotated Fig. 4 below, which is a cross section taken at section A-A of Fig. 1. *Id.* at 5:19-21. Each memory cell is formed as a "self-aligned stack" of, for example, a gate dielectric (25), floating gate charge storage elements (12, 15, 18), inter-polysilicon

layer (35), control gate (21, 22, 23), a dielectric (37), and an optional layer of dielectric 49. *Id.* at 6:34-39, 7:17-20. The claims refers to "layered structures" which "includ[e] at least the charge storage elements and the control gates." *Id.* at claims 1, 2. A dielectric material is formed between adjacent stacks while leaving a void. *Id.* at 7:7-11.



MICRON-1001, 849 Patent at Figure 4 (with annotations).

The claims are specifically directed to embodiments wherein the spacing between memory cells (annotated in purple above) is less than one fifth (or one eighth as required by claim 5) of the height of the memory cells (annotated in pink above)[4]. However, the 849 Patent notes that the aspect ratio is

[4] This is also referred to as the "cross-sectional aspect ratio of the spaces between the stacks" or "aspect ratio" in the 849 Patent, and is referred to as the "aspect

> a result of process improvements allowing the shrinking of horizontal dimensions across the substrate causing the widths of the spaces 41 to be reduced without the height of the stacks forming the spaces necessarily being changed. The aspect ratio is also controlled, independent of the process resolution element size, by controlling the heights of the stacks without affecting operation of the resulting array, particularly by controlling the thickness of the top dielectric layer 37 or another dielectric layer that may be added on top of it.

Id. at 6:49-58.[5]

In other words, the aspect ratio is merely a design choice that is in part dictated by the available integrated circuit manufacturing processes. MICRON-1003, Baker Decl. ¶¶ 47-48. The 849 Patent does not disclose any methods for reducing the horizontal spacing between adjacent memory cells, or novel techniques for increasing the height of the layered structures. *Id.* The alleged purpose of these 5:1 and 8:1 aspect ratios is to allow a dielectric to be formed between the memory cells which contains voids. *See* MICRON-1001, 849 Patent at 4:40-47.

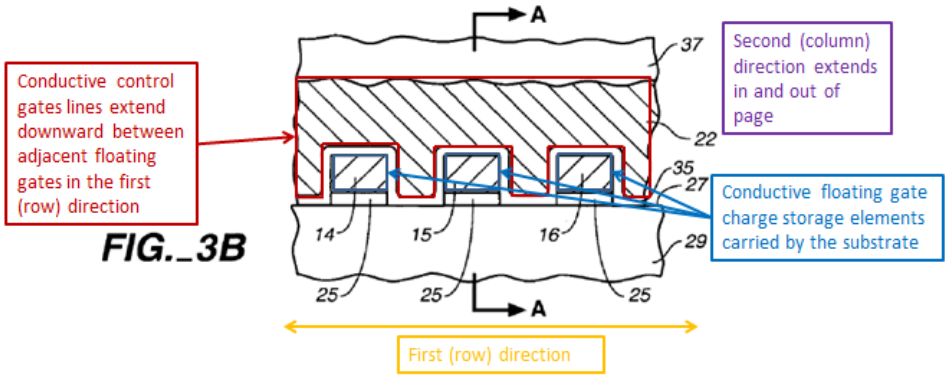
The final limitations of challenged independent claims 1 and 2 are directed

---

ratio" throughout this Petition. *See, e.g.*, MICRON-1001, 849 Patent at 4:40-44; MICRON-1003, Baker Decl. ¶ 47.

[5] Emphasis added throughout unless otherwise stated.

to admittedly known prior art concepts. Specifically, the final limitation of claim 1 is directed to providing shielding between adjacent floating gates in the row direction by extending the control gate lines downward between adjacent floating gates as shown in annotated Fig. 3B below.



MICRON-1001, 849 Patent at Figure 3B (with annotations).

The final limitation of claim 2 is merely directed to connecting the individual memory cells in a typical NAND array wherein "the control gate lines include word lines extending in the first direction along rows of charge storage elements and the charge storage elements form, along columns in the second direction, series strings of a plurality of charge storage transistors." MICRON-1001, 849 Patent at 10:15-19; MICRON-1003, Baker Decl. ¶ 50; *see also* MICRON-1001, 849 Patent at 1:61-2:6 (describing that NAND arrays containing series strings of memory cells were well known in the art), 8:32-36 ("In the case of a NAND array, the control gate lines 21-23 are word lines of the array, each extending in the x-direction across a row of one memory cell in each of a large number of such NAND columnar series strings of memory cells."). This limitation

is met by any non-volatile EEPROM array arranged in a NAND configuration. *See id.*; MICRON-1003, Baker Decl. ¶ 50.

5. 849 PATENT PROSECUTION HISTORY

The application that led to the issuance of the 849 Patent was originally filed with 17 claims. MICRON-1002, 5-21-2003 Claims at .016-.019. On February 17, 2004, the Examiner found that claims 1-8 were drawn to a semiconductor device and claims 9-17 to a method of making semiconductor devices and issued a restriction requirement. *See id.*, 2-17-2004 Non-Final Rejection at .057. The Examiner also issued a non-final rejection finding claims 1-3, 5 and 8 anticipated by Sugimae et al. (US 2003/0151069 A1). The Examiner stated that claims 4, 6 and 7 would be allowable if rewritten in independent form. *Id.*, at .058-.060.

In a June 18, 2004 Amendment, the Applicant withdrew claims 9-17 pursuant to the requirement for restriction, and amended claims 4, 6 and 7 so as to be written in independent form. *Id.*, 6-18-2004 Amendment at .080. The Applicant also requested reconsideration of the rejection of claims 1-3, 5 and 8, stating that the claims call for "dielectric material having '…voids between adjacent charge storage elements…' (claim 1, last paragraph)" and arguing that in Sugimae et al., the "air gaps 26 are positioned higher than floating gates 6, between the control gates 10 (layers 8 and 9) and the dielectric mask 11." *Id.*

On September 9, 2004, the Examiner again rejected claims 1-3, 5 and 8 as

being anticipated by Sugimae et al. in a Final Rejection. *Id.*, 9-9-2004 Final Rejection at .093-.094. The Examiner found Applicant's arguments regarding the location of the air gaps unavailing because no language in the claims required the air gaps to extend to the bottom of the stacks. *Id.* at .094. The Examiner explained that the "claims do not mention the placement of the voids at the bottom of the stacks. The fact that the voids (26) are positioned higher than the charge storage elements (6) does not preclude the voids from being between the charge storage elements when the three layers in question are seen to lie on three different planes." *Id.* Claims 4, 6 and 7 were allowed.

On February 8, 2005, the Applicant filed several amendments to claim 1 specifying that the void was at bottom portions of the spaces between layered structures and requested continued examination of claims 1-3, 5 and 8. *Id.*, 2-8-2005 Amendment at .101-.103. The Applicant added claim 18 for consideration.

On May 18, 2005, the Examiner rejected claims 1-3, 5, 6[6], 8 and 18 as anticipated by Onakodo et al. (U.S. Patent No. 6,469,339 B1). *Id.*, 5-18-2005 Non-Final Rejection at .118-119.

On August 19, 2005, the Applicant canceled claims 1 and 5 and amended

[6] Although the Examiner had previously stated claims 4, 6, and 7 were allowable, the Examiner reconsidered those claims during the continued examination.

claims 2, 3, 8 and 18 to depend from claim 6. *Id.*, 8-19-2005 Amendment at .127-.130. The Applicant argued that claim 6 was not disclosed in Onakodo et al. because the memory cell transistors in that patent are connected in parallel rather than in series as required by claim 6. *Id.* at .130.

A Notice of Allowance was issued on December 19, 2005. *Id.*, 12-19-2005 Notice of Allowance at .134-.137. The following is a table listing the original claim numbers and issued claim numbers:

Original Claim	**Issued Claim**
2	3
3	4
4	1
6	2
7	7
8	5
18	6

6. CLAIM CONSTRUCTION[7]

6.1. Applicable Law

[7] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 849 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 849 Patent.

A claim subject to *inter partes* review is given the "broadest reasonable construction in light of the specification of the patent in which it appears."[8] 37 C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill in the art and consistent with the specification of the 849 Patent. Petitioner respectfully submits that the following should be construed for this IPR:

6.3. "thickness" (claims 1-6)

The claim term "thickness" is found in challenged independent claim 1 and independent claim 2, and thus is also a limitation of claims 3-6 which depend on

[8] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

independent claim 2. The term "thickness" is also found in dependent claim 6.

The term "thickness" and "height" are used interchangeably within the specification of the 849 Patent and both terms are used to describe the vertical dimension of a material as measured in the direction away from the substrate. *See, generally, e.g.*, MICRON-1001, 849 Patent at 5:54-6:19 (describing the "thickness" of deposited elements with reference to Figs. 3A and 3B), *id.* at 6:43-45 (stating that the sum of the "thicknesses of the individual layers given in the specific example above" is the "height of the self-aligned stacks").

Thus, under the broadest reasonable interpretation standard, one of ordinary skill in the art would understand "thickness" to mean the "height as measured from the substrate." MICRON-1003, Baker Decl. at Section VII.B.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 849 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design and fabrication of memory devices. An individual with an advanced degree in a relevant field, such as materials science or electrical engineering, would require less experience in the design or fabrication of memory devices. *Id.* at Section IV.

8. DESCRIPTION OF THE PRIOR ART

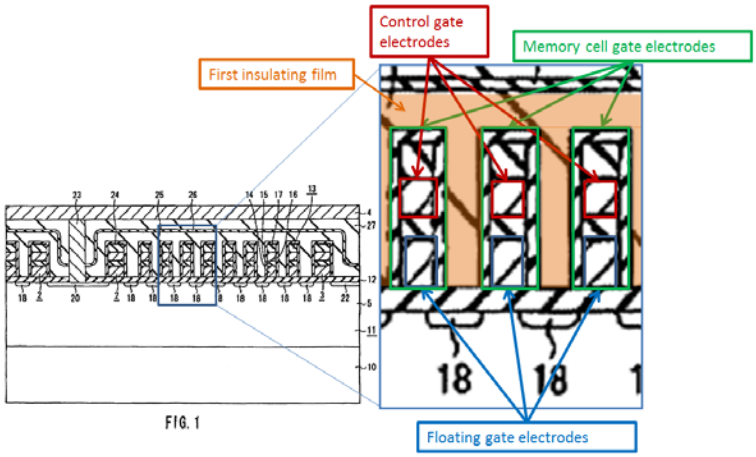
8.1. U.S. Patent No. 6,720,612 ("Takeuchi")

U.S. Patent No. 6,720,612 ("Takeuchi," MICRON-1005) is entitled "Semiconductor Device," issued to Yuji Takeuchi et al., and was originally assigned to Kabushiki Kaisha Toshiba. Takeuchi was filed with the USPTO on March 15, 2002 and issued on April 13, 2004. Takeuchi is prior art to the 849 Patent under at least (pre-AIA) 35 U.S.C. § 102(e) because the U.S. Patent Application which issued as Takeuchi was filed before the earliest application to which the 849 Patent claims priority.

Like the 849 Patent, Takeuchi is also directed to a non-volatile flash EEPROM array of memory cells. MICRON-1005, Takeuchi at 3:20-35, 7:57-64; MICRON-1003, Baker Decl. ¶ 67. The memory cells of Takeuchi are arranged as a NAND flash array, wherein "word lines 1 are arranged in parallel with each other and extend in the row direction" over a plurality of floating gate type memory cells. MICRON-1005, Takeuchi at 7:58-66 ("The present embodiment is applied to a NAND flash memory…"), 8:31-34. And, in the column direction, the memory cells form series strings of transistors. MICRON-1005, Takeuchi at 8:16-21, 8:35-39; *see also id.* at Fig. 3; MICRON-1003, Baker Decl. ¶ 67.

Each memory cell in Takeuchi is referred to as a "memory cell gate electrode 13," and, like the memory cells in the 849 Patent, each memory cell gate electrode 13 is formed in a stack upon a semiconductor substrate and has "a

floating gate electrode 14 which becomes a charge accumulation layer" and a "control gate electrode 16." MICRON-1005, Takeuchi at 8:26-31. A first insulating film 25 is then formed so as to embed between the gate electrodes of the memory cell transistors. *Id.* at 9:19-26.



MICRON-1005, Takeuchi at Figure 1 (with annotations).

Takeuchi is directed to the same problem as the 849 Patent: capacitive coupling between adjacent memory cells and the effect on the threshold voltage of a memory cell as a function of the dielectric material between adjacent cells. *Id.* at 5:5-9 (indicating a particular deterioration of the electrical characteristics of the transistors when gate length is small), 18:8-17 (reducing interference caused by parasitic capacitance from adjacent memory cells); MICRON-1003, Baker Decl. ¶ 70. As one solution, Takeuchi discloses that "first insulating material 25" can also "embed" between the memory cell gate electrodes such that, like the alleged invention of the 849 Patent, voids are formed within the first insulating material between adjacent memory cell gates. MICRON-1005, Takeuchi at 9:42-45 ("Now,

the phrase 'to embed' means not only to completely embed, but also to embed but include a cavity or cavities"); *see also id.* at 16:64-17:1 (describing cavities between all adjacent cells as shown in Fig. 16).

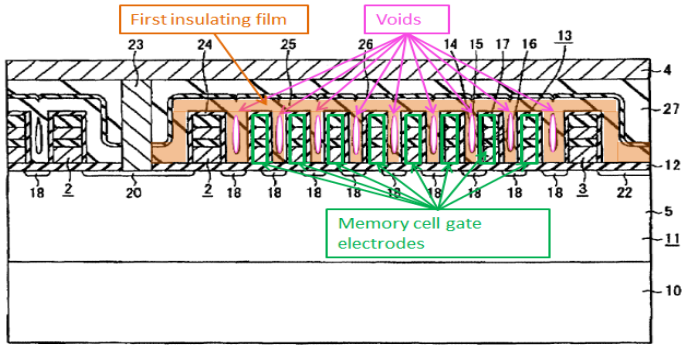


FIG. 16

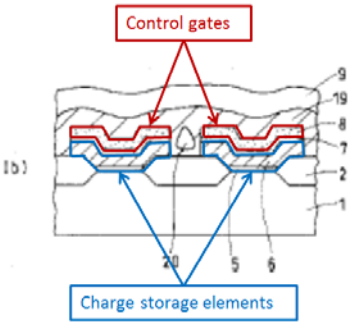
MICRON-1005, Takeuchi at Figure 16 (with annotations).

Moreover, just like the 849 Patent, Takeuchi discloses that "when the gate electrode is formed in a significant height comparing to the distance between the gate electrodes," the voids are easily formed. *Id.* at 16:21-24. In other words, Takeuchi discloses that cavities are easily generated when using a high aspect ratio. *See id.*; MICRON-1003, Baker Decl. ¶ 71.

8.2. JP Patent Application Publication No. 2000-100976 ("Sato")

Japanese Patent Application Publication No. 2000-100976 ("Sato," MICRON-1007) entitled "Semiconductor Memory Device and Manufacture Thereof," applied for by Matsushita Electronic Industries Corp. on behalf of Kazuo Sato. Sato was filed on September 21, 1998 and published on April 7, 2000. Sato is prior art to the 849 Patent under at least (pre-AIA) 35 U.S.C. § 102(b) because it was published more than one year before the filing date of the 849 Patent.

Sato is directed to "semiconductor memory array devices having floating gate structures with a size of less than a half micron." MICRON-1007, Sato at [0009]. Like the EEPROM memory cell arrays formed as "layered structures" in the 849 Patent, the semiconductor array devices in Sato are "configured from EEPROM with the typical conventional stack type floating gate structure." *Id*. at [0003]; MICRON-1003, Baker Decl. ¶ 74. For example, the memory cells are formed in an array of four cells, and each memory cell has a "floating gate electrode 6" and a "control gate electrode 8" which are formed on a "semiconductor substrate 1." MICRON-1007, Sato at [0004]; *see also id.* at [0043]-[0044] (describing embodiments shown in Fig. 9(b)).



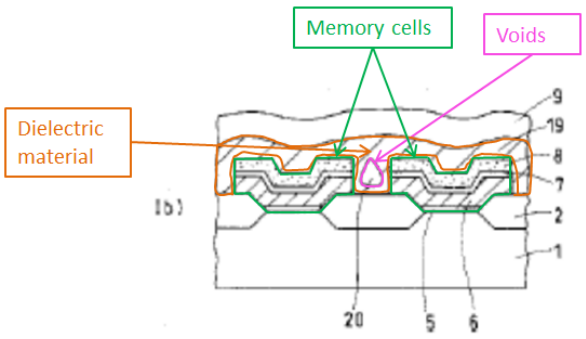
MICRON-1007, Sato at Figure 9(b) (with annotations).

The control gate electrodes are common to and extend across and downward between a plurality (*e.g.* two) of floating gate electrodes in the row direction. *See id.* at Figs. 6, 9(a); MICRON-1003, Baker Decl. ¶ 75.

Sato is also directed to the same problem as the 849 Patent. MICRON-1003, Baker Decl. ¶ 76. Namely, as spacing between adjacent floating gates and control

gate electrodes becomes small, there is unwanted capacitive coupling between the dielectric deposited between adjacent memory cells. MICRON-1007, Sato at [0009]. Sato states that this problem is particularly significant when the gap between adjacent memory cells is less than 0.3 μm and, just like the 849 Patent, explains that this coupling makes it difficult to utilize multi-bit memory cells. *Id.* at [0011]; MICRON-1003, Baker Decl. ¶ 77.

Sato also describes the same means for solving the capacitive coupling problem. *Id.* ¶¶ 78-80. Namely, the invention is "characterized by providing a cavity between each of said floating gate electrodes and between each of said control gate electrodes." MICRON-1007, Sato at [0019]. Specifically, the cavity is formed, for example, within a silicon oxide insulating film 19 that does not entirely fill the trench between adjacent memory cells. *Id*. at [0043].



MICRON-1007, Sato at Figure 9(b) (with annotations).

8.3. Lee, Jae-Duk et al., *Effects of Floating Gate Interference on NAND Flash Memory Cell Operation* ("Lee")

Lee, Jae-Duk et al., *Effects of Floating Gate Interference on NAND Flash*

Memory Cell Operation ("Lee," MICRON-1006) [9] was published in IEEE Electron Device Letters, vol. 23, No. 5, in May, 2002. Lee was received by the UC Berkeley Library in Berkeley, California, on May 13, 2002, and was published according to normal library policies within 1-2 days of that date.[10] Accordingly, Lee is prior art under at least (pre-AIA) 35 U.S.C. § 102(b) because Lee was publically available more than one year prior to the filing date of the 849 Patent.

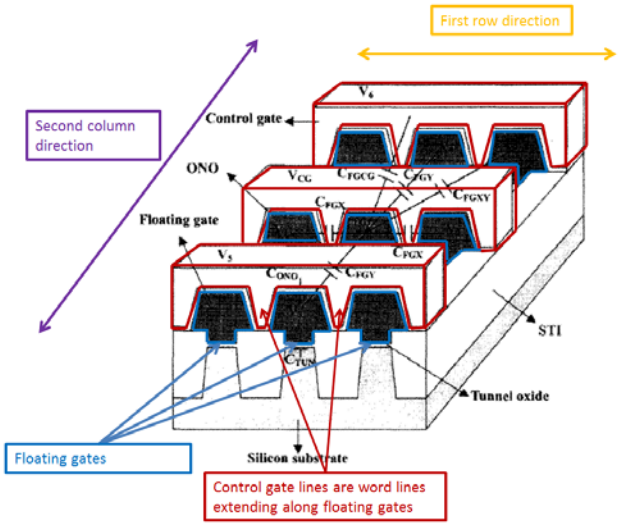
Lee claims to introduce "the concept of floating-gate interference in flash memory cells for the first time." MICRON-1006, Lee at .002 (Abstract). Specifically, Lee is directed to measuring the secondary effects on NAND flash memory cells from capacitive coupling between adjacent floating gates in the column direction. *Id.* Like the 849 Patent, Takeuchi, and Sato described above, Lee concludes that as gate-to-gate spacing is decreased, NAND flash memory cells suffer from increased parasitic capacitance with adjacent cells. *Id.* at .002

[9] Lee is cited on the face of the 849 Patent. However, it was not discussed by the Examiner during prosecution, and of course was not considered in combination with Takeuchi, or with Sato, neither of which are cited.

[10] In addition to the copyright and publication date of the reference, *see* MICRON-1015 (Rowlison de Ortiz Declaration) which provides additional evidence of its availability to the public.

(Introduction), .004 (Conclusion); MICRON-1003, Baker Decl. ¶ 83.

The memory cell array in Lee is a conventional NAND memory array as shown in Fig. 1 below. Each memory cell is formed in a stack structure on a silicon substrate and includes a floating gate and a control gate. MICRON-1006, Lee at .002. The control gates are common to the floating gates along a row forming word lines, and extend downward between adjacent floating gates. *Id;* MICRON-1003, Baker Decl. ¶ 84.



MICRON-1006, Lee at Figure 1 (with annotations).

Using the basic structure of a NAND memory array, Lee reports experimental and simulated results of the parasitic capacitance between adjacent floating gates in the column direction with variable gate-to-gate spacing. MICRON-1003, Baker Decl. ¶ 86-87; MICRON-1006, Lee at .003-.004 (Experiments, Results and Discussion, Fig. 4). The experimental results include NAND memory arrays with gate-to-gate spacing of 0.12 μm and simulated results

for arrays with spacing as small as 0.010 μm (10 nm). *See id.*; MICRON-1003, Baker Decl. ¶ 86. Like the 849 Patent, Takeuchi, and Sato, Lee concludes that a possible solution for minimizing the interference between floating gates is to develop a new cell structure that includes "vacuum isolation of the gate-to-gate spacing," *i.e.*, forming air gaps between the floating gates. MICRON-1006, Lee at .004; MICRON-1003, Baker Decl. ¶ 88.

9. GROUND #1: CLAIMS 1-6 OF THE 849 PATENT ARE UNPATENTABLE AS OBVIOUS OVER TAKEUCHI IN VIEW OF LEE

As explained below, claims 1-6 of the 849 Patent are unpatentable as obvious over Takeuchi in view of Lee under 35 U.S.C. § 103(a). Takeuchi discloses all of the elements of claims 1-6 except for an embodiment wherein the gate-to-gate spacing is less than one fifth (or one eighth as required by claim 5) of the height of the memory cells. However, such embodiments would have been obvious by Takeuchi in view of Lee. Additionally, Takeuchi is silent with regards to whether the control gates extend downward between adjacent floating gates as required by claim 1, which Lee discloses. A person of ordinary skill in the art therefore would have found claims 1-6 of the 849 Patent obvious over Takeuchi in view of Lee. MICRON-1003, Baker Decl. at Section IX.A.

It would have been obvious to combine the teachings of Takeuchi and Lee as Dr. Baker explains. *Id.* As discussed above, Takeuchi and Lee are both directed to

NAND flash non-volatile memory arrays formed in stack configurations. *See* MICRON-1005, Takeuchi at Fig. 1, 7:58-59; MICRON-1006, Lee at Fig. 1, .003. Both references are also directed to the same problem of coupling and interference between adjacent memory cells in a NAND memory cell array, and propose similar solutions to the problem. *See* Sections 8.1 and 8.3 above; MICRON-1003, Baker Decl. ¶ 97; *see also* MICRON-1005, Takeuchi at 5:5-11, 16:64-17:3, 17:65-18:17; MICRON-1006, Lee at .002, .004. A person of ordinary skill therefore would have understood that the teachings of Takeuchi and Lee are interrelated and compatible with one another, and would have been motivated to combine the references for that reason. MICRON-1003, Baker Decl. ¶¶ 93-97 (describing similarities between Takeuchi and Lee, and citing portions of each reference in support).

Second, Takeuchi states that the distance between memory cell gates can be "less than 0.2 μm," and that the problems that Takeuchi is directed to are "particularly significant when the gate length is smaller than about 0.2 μm." MICRON-1005, Takeuchi at 5:10-15; *see also id*. at 10:17-19. Those of ordinary skill in the art would have therefore understood to look at known techniques for fabricating memory cell arrays with reduced gate-to-gate spacing to apply to Takeuchi. Lee discloses well-known reductions in the gate-to-gate spacing. MICRON-1003, Baker Decl. ¶ 94. Persons of ordinary skill in the art understood that there were significant market pressures to maximize memory cell density on a

given amount of silicon, and would have been motivated to combine the references for that reason. *Id.*

Third, Takeuchi's NAND memory cell array would be particularly applicable to the reduced gate-to-gate spacing disclosed in Lee because, as discussed above, Lee concludes that it would be beneficial to use vacuum isolation between adjacent memory cells, which Takeuchi discloses. *See* Sections 8.1 and 8.3 above. A person of ordinary skill would have thus been motivated to combine Lee and Takeuchi because it would amount to using known techniques to improve similar devices to yield predictable results. MICRON-1003, Baker Decl. ¶ 95.

Fourth, persons of ordinary skill in the art understood that voids between adjacent memory cells were more easily formed, and could be formed larger, when the aspect ratio between the height of the memory cell and the width between the memory cell is high. *See* MICRON-1005, Takeuchi at 16:21-27; MICRON-1003, Baker Decl. ¶ 96 (citing MICRON-1018, Fulford at 3:46-54, 4:58-67 in support). A person of ordinary skill in the art would therefore have been motivated to increase the aspect ratio of the memory cells in Takeuchi and Lee in order to provide for better isolation of the floating gate electrodes, which would be a design choice. *Id.*; *see also* MICRON-1001, 849 Patent at 6:48-59.

Fifth, Takeuchi is silent with regards to the deposition of the word lines in the row direction. MICRON-1003, Baker Decl. ¶ 98. Those of ordinary skill in

the art would have understood to look at known techniques to apply to Takeuchi. Lee discloses one well-known way to form control gates, namely, they extend downward between adjacent floating gates in the row direction. *Id.; see* MICRON-1006, Lee at Fig. 1. A person of ordinary skill in the art would have been motivated to use the control gate structure disclosed in Lee because Lee shows a significant reduction in parasitic capacitance along floating gates in the row direction. MICRON-1003, Baker Decl. ¶ 98 (citing MICRON-1013, Harari at 3:55-59 in support); *see also* MICRON-1006, Lee at .002-.003 (Model). Indeed, such a structure was well known to provide capacitive shielding, as admitted in the background section of the 849 Patent. MICRON-1001, 849 Patent at 4:1-8.

9.1. Claim 1 obvious over Takeuchi in view of Lee

9.1.1. [1.P] "A non-volatile memory cell array formed on a semiconductor substrate, comprising:"

Takeuchi discloses this limitation. Namely, Takeuchi is directed to a conventional non-volatile semiconductor memory device in a NAND configuration with series-connected memory cell gate electrodes 13 formed on a semiconductor substrate 10. MICRON-1005, Takeuchi at 4:35-42 ("Here, in a non-volatile semiconductor memory device"), 7:57-62 ("The present embodiment is applied to a NAND flash memory…"); 8:35-39 ("A NAND cell (memory cell unit), which is one memory cell array, is formed of the series-connected memory cells"), 8:22-25 ("8 memory cells in one memory cell array each have a memory cell gate 13…

formed on the semiconductor substrate 10.").

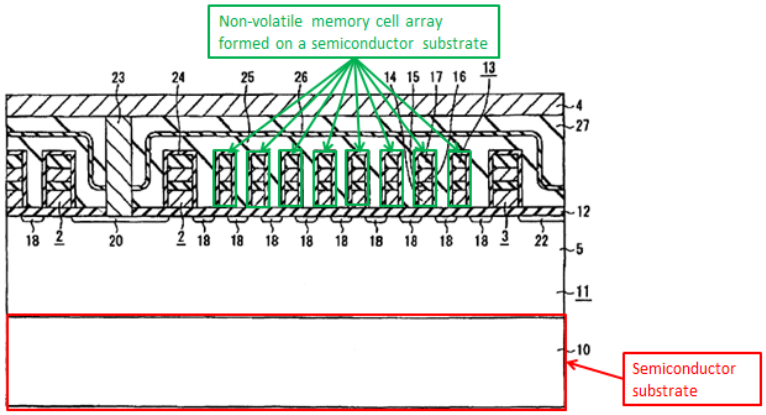


FIG. 1

MICRON-1005, Takeuchi at Figure 1 (with annotations).

9.1.2. [1.1] "an array of charge storage elements carried by the substrate,"

Takeuchi discloses this limitation. Specifically, Takeuchi discloses that each memory cell gate electrode in the array of memory cell gate electrodes described in the previous limitation has a conductive "floating gate electrode 14 which becomes the charge accumulation layer." *Id.* at 8:22-34; *see also id.* at Fig. 3, 8:16-21 (describing arrangement of memory cell array with reference to Fig. 3).

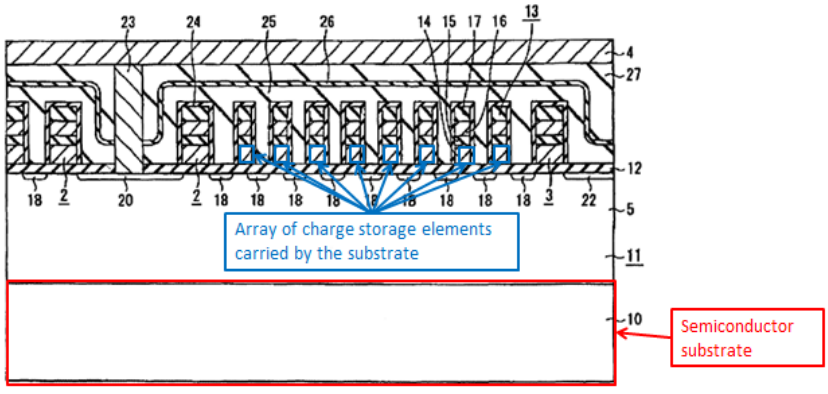


FIG. 1

MICRON-1005, Takeuchi at Figure 1 (with annotations).

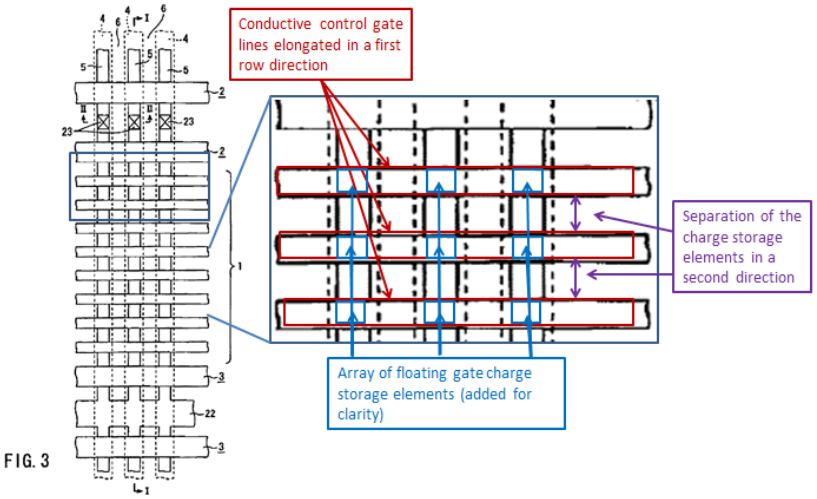
Specifically, the floating gates "formed on a gate insulating film 12 on the element region 5 in the well 11 are formed on the semiconductor substrate 10." *Id.* at 8:24-25. The floating gate electrodes are the claimed "charge storage elements carried by the substrate." MICRON-1003, Baker Decl. Appx. A at claim [1.1].

9.1.3. [1.2] "conductive control gate lines elongated in a first direction across the charge storage elements and being separated in a second direction by a distance of separation of the charge storage elements in the second direction, the first and second directions being orthogonal with each other,

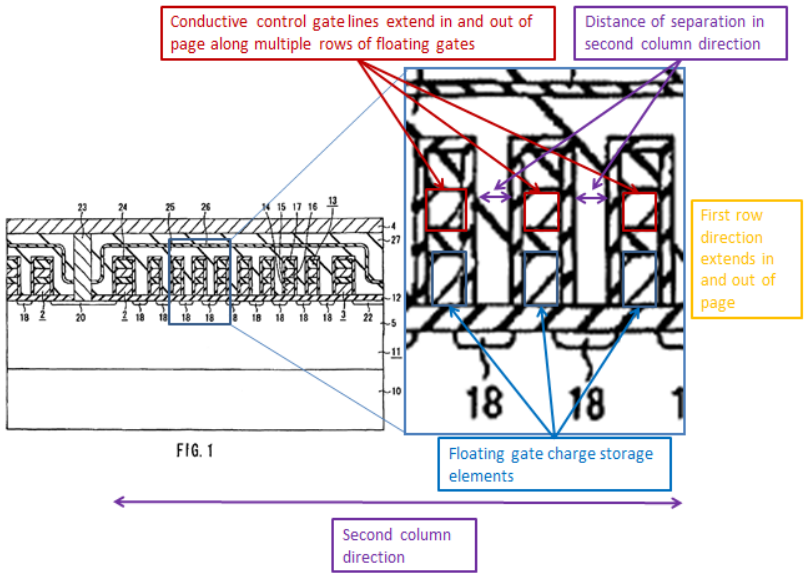
Takeuchi discloses this limitation. Takeuchi describes that each memory cell gate electrode 13 has a "control gate electrode 16" that is common to all of the memory cell gate electrodes along a row in order to form a word line 1. MICRON-1005, Takeuchi at 8:22-34 ("Each memory cell gate electrode 13 has…a control gate electrode 16 formed on the inter-gate insulating film 15…The control gate electrode 16 of one memory cell gate 13 in a row is common to the control gate electrode of another memory cell gate 13 in the row and forms the word line 1."); *see also id.* at 7:65-8:2 (explaining that word lines are arranged in parallel and extend in the row direction), 9:46-48 (disclosing exemplary spacing between gate electrodes).

As illustrated in Figs. 1 and 3 below, the control gate electrodes are formed on and aligned with the floating gates in rows, such that they are separated by a distance of separation of the floating gates in the column direction. *Id., see*

MICRON-1003, Baker Decl., Appx. A at claim [1.2]. As noted in the above figures, the row direction is the claimed "first direction" and the column direction is the claimed "second direction," which are orthogonal with each other. *Id*.



MICRON-1005, Takeuchi at Figure 3 (with annotations).



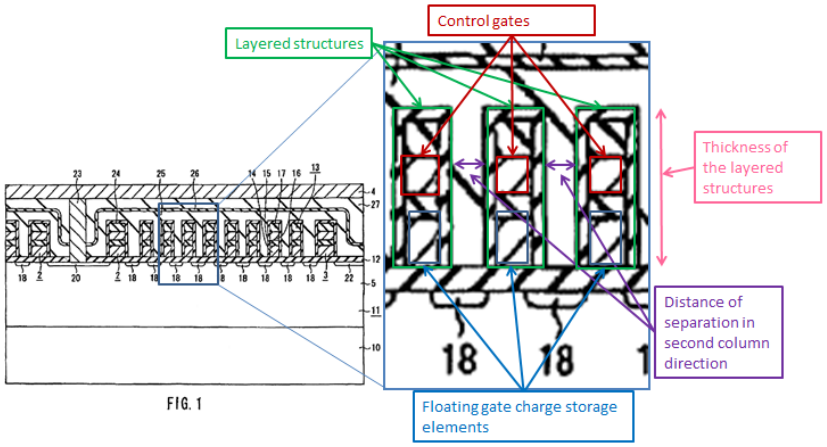
MICRON-1005, Takeuchi at Figure 1 (with annotations).

9.1.4. [1.3] "wherein layered structures including at least the charge storage elements and the control gates are separated in the second direction by distances that are

less than one-fifth of a thickness of the layered structures,"

Takeuchi in view of Lee renders this limitation obvious, wherein the term "thickness" means "the height as measured from the substrate" under the broadest reasonable interpretation standard. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.3]; *see also* Section 6.3 above.

First, Takeuchi discloses memory cell gate electrodes 13 which are formed in a conventional stack formation wherein "[e]ach memory cell gate electrode 13 has a floating gate electrode 14 which becomes a charge accumulation layer, an inter-gate insulating film 15 formed on the floating gate electrode 14, a control gate electrode 16 formed on the inter-gate insulating film 15, and a gate mask film 17 formed on the control gate electrode 16." MICRON-1005, Takeuchi at 8:22-34, Fig. 1. The memory cell gate electrodes 13 are the claimed "layered structures including at least the charge storage elements and the control gates." MICRON-1003, Baker Decl., Appx. A at claim [1.3].



MICRON-1005, Takeuchi at Figure 1 (with annotations).

What Takeuchi does not expressly disclose is an embodiment wherein the gate-to-gate spacing (i.e. the spacing between memory cell gate electrodes 13) is less than one fifth of the height of the memory cell gate electrodes as required by this limitation. However, a person of ordinary skill in the art would have found such an aspect ratio obvious by Takeuchi in view of Lee.

First, Takeuchi discloses an embodiment wherein the height of the memory cells (the thickness of the layered structures) is "about 0.6 μm" and the gate-to-gate spacing (the distance of separation in the second direction) is "about 0.2 μm." MICRON-1005, Takeuchi at 9:46-48. Takeuchi also discloses that the spacing can be less than 0.2 μm. *Id.* at 10:17-19; MICRON-1003, Baker Decl. at claim [1.3].

Based on the disclosed height in Takeuchi, the gate-to-gate spacing between adjacent memory cells would need to be reduced to less than about 0.12 μm to meet this limitation, which is disclosed in Lee. *See* MICRON-1006, Lee at .002 ("This letter…shows experimental results of the floating-gate interference using 0.12- μm [6] design-rule cell and predicts the interference in future cells based on simulation results." "In a 0.12- μm design rule cell (gate length = gate space = floating gate height = channel width = 120 nm"), .003 ("NAND flash cell arrays have been fabricated based on 0.12-μm [6] design-rule…"). A person of ordinary skill would have found this limitation obvious because 0.12 μm can be less than

one fifth of "about 0.6 μm." MICRON-1003, Baker Decl. Appx. A at claim [1.3]. Lee also discloses simulations of memory cells wherein the gate-to-gate spacing between adjacent cells is less than 0.12 μm which would also render obvious this limitation. These simulations were done for memory cell arrays with gate-to-gate spacing as small as 0.010 μm (10 nm). *See* MICRON-1006, Lee at Fig. 4; MICRON-1003, Baker Decl. Appx. A at claim [1.3]. Persons of ordinary skill in the art would have been motivated by the simulations in Lee to vary the gate-to-gate spacing in Takeuchi because the simulations show that variations in height and gate-to-gate spacing were design choices which yielded predictable results. *Id.*

Furthermore, persons of ordinary skill in the art would have found it obvious that the height of the memory cell structures in Takeuchi could be increased, and would have been motivated to do so when designing a NAND array with reduced floating gate coupling as discussed in Section 9 above. For example, a person of ordinary skill in the art would have understood that it would be a simple design choice to increase the height of the gate mask film 17 in order to more easily form, or to form larger, voids between adjacent memory cell gate electrodes without otherwise affecting operation of the memory array. *See* MICRON-1005, Takeuchi at 16:21-28; MICRON-1001, 849 Patent at 6:53-59 (implying it is a design choice to increase the aspect ratio by increasing the top dielectric layer of the stacks); MICRON-1003, Baker Decl., Appx. A at claim [1.3] (citing portions of MICRON-

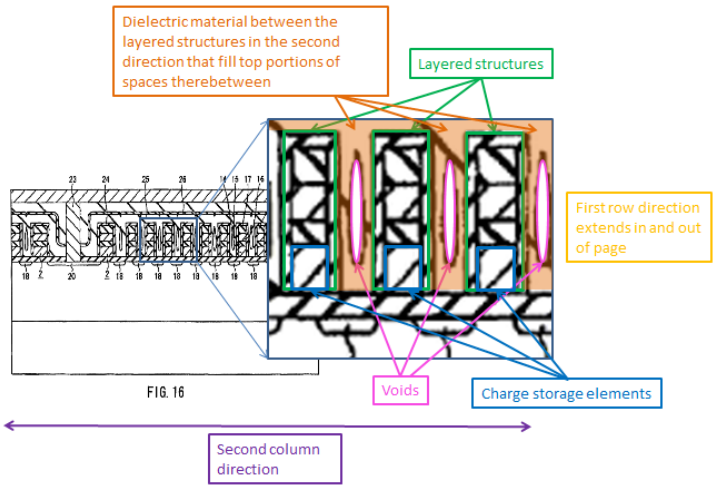
1018, Fulford in support). Similarly, a person of ordinary skill in the art would have understood that the height of the other components in the memory cell gate electrodes, including the height of the floating gate electrodes and control gate electrodes could be increased according to known techniques. *Id.*

9.1.5. [1.4] "dielectric material between the layered structures in the second direction that fill top portions of spaces there between while leaving voids between adjacent charge storage elements of the layered structures, and"

Takeuchi discloses this limitation. Namely, Takeuchi discloses that a "first insulating film 25" (the claimed "dielectric material") is formed so as to "embed between the gate electrodes 13 of the memory cell transistors." *Id.* at 9:24-30 ("The first insulating film 25 is formed so as to embed between the gate electrodes 13 of the memory cell transistor."); *see also id.* at 18:7-17 (describing the effects of different materials on parasitic capacitance for first insulation layer 25). As discussed in the previous limitation, the memory cell gate electrodes 13 are the claimed "layered structures." *See* Section 9.1.4 above.

Furthermore, Takeuchi specifies that the phrase "to embed" includes depositing the first insulating film such that it includes cavities or "voids" between the adjacent memory cell gate electrodes. MICRON-1005, Takeuchi at 9:42-45 ("Now, the phrase 'to embed' means not only to completely embed, but also to embed but include a cavity or cavities..."); *see also id.* at 18:26-38 (describing that in each embodiment "a cavity may exist in the first insulating film 25" between

memory cell gate electrodes). These voids are depicted, for example, in Fig. 16 below as being formed within the first insulating film 25 in all of the distances between the memory cell gate electrodes 13 in the second column direction. *Id.* at 16:61-17:3 ("FIG. 16 …is different from the first embodiment in that all of the distance portions between the memory cell gates contain voids."); *see also id.* at claims 19-22 (claiming "voids" between "memory cell gates").



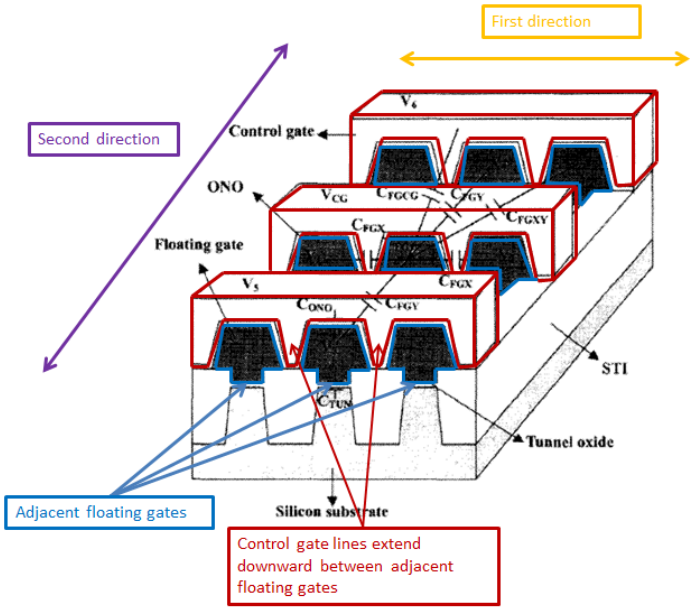
MICRON-1005, Takeuchi at Figure 16 (with annotations).

9.1.6. [1.5] "wherein the charge storage elements are conductive floating gates and the elongated control gate lines extend downward between adjacent floating gates in the first direction."

Takeuchi in view of Lee teaches this limitation. As discussed in claims [1.1] and [1.2] above, Takeuchi discloses elongated control gate lines which extend across conductive floating gates. *See* Sections 9.1.2 and 9.1.3 above. It would have been obvious to extend the control gate lines between adjacent floating gates in the first direction in view of the disclosures in Lee. MICRON-1003, Baker

Decl., Appx. A at claim [1.5].

As shown in annotated Fig. 1 below, Lee discloses a view of a NAND array wherein the control gate lines extend downward between adjacent floating gates.



MICRON-1006, Lee at Figure 1 (with annotations).

As Dr. Baker confirms, and as discussed above, a person of ordinary skill in the art would have been motivated to extend the control gates lines between adjacent floating gates in Takeuchi to reduce the parasitic capacitance between floating gates in a given row of memory cells. MICRON-1003, Baker Decl., Appx. A at claim [1.5]; *see also* Section 9 above.

9.2. Claim 2 is obvious over Takeuchi in view of Lee

The limitations of claim 2 are identical to claim 1 except for the final limitation. Accordingly, the discussion in Sections 9.1.1, 9.1.2, 9.1.3, 9.1.4 and 9.1.5 are hereby incorporated by reference for the identical limitations in claim 2.

The final limitation of claim 2 is addressed below.

9.2.1. [2.5] "wherein the control gate lines include word lines extending in the first direction along rows of charge storage elements and the charge storage elements form, along columns in the second direction, series strings of a plurality of charge storage transistors."

Takeuchi discloses this limitation, which simply requires that the claimed non-volatile memory cell array is formed in a NAND configuration. MICRON-1003, Baker Decl., Appx. A at claim [2.5].

As discussed above with respect to claim [1.2] above, Takeuchi discloses that "[t]he control gate electrode 16 of one memory cell gate 13 in a row is common to the control gate electrode of another memory cell gate 13 in the row and forms the word line 1." MICRON-1005, Takeuchi at 8:31-34; *see* annotated Fig. 3 in Section 9.1.3 above.

Furthermore, each memory cell gate electrode forms a memory cell transistor comprising the memory cell gate electrode and adjacent source/drain diffusion regions 18. MICRON-1005, Takeuchi at 8:35-39. Each memory cell transistor is connected in the second column direction to form "series strings of a plurality of charge storage transistors" between a source and drain side selecting gate. *Id.* at 8:35-39; *see also id.* at 9:5-6 ("The memory cell transistors are connected to each other in series."), 8:40-54 (describing drain and source side selecting gates), 9:12-15 (function of selecting transistors), Fig. 3, Figs. 1 and 16

(showing exemplary series strings of charge storage transistors in second column direction); MICRON-1003, Baker Decl., Appx. A at claim [2.5].

9.3. Claim 3 is obvious over Takeuchi in view of Lee

9.3.1. [3.0] "The array according to claim 2, wherein the dielectric material includes at least one of silicon dioxide and silicon nitride."

Takeuchi discloses this limitation. Specifically, Takeuchi discloses that the the first insulating film 25 (the claimed "dielectric material," s*ee* Section 9.1.5 above) can include, for example, a silicon oxide film, an oxinitride film, or an oxidized silicon nitride film. MICRON-1005, Takeuchi at 9:19-30; *see also id.* at 18:7-19 ("when the first insulating layer 25 embedded between the gates is made of silicon oxide…"), claim 5. Silicon dioxide was commonly referred to as "silicon oxide" by those of ordinary skill in the art, including as used in the 849 Patent. MICRON-1003, Baker Decl., Appx. A at [3.0]; *compare, e.g.*, MICRON-1001, 849 Patent at 2:64-66 (describing "[a] triple layer dielectric formed of silicon oxide, silicon nitride and silicon oxide ('ONO')"), *with id.* at 6:8-10 (describing that "ONO" is commonly known as a "composite layer of silicon dioxide, silicon nitride and silicon dioxide").

9.4. Claim 4 is obvious over Takeuchi in view of Lee

9.4.1. [4.0] "The array according to claim 2, wherein the charge storage elements are conductive floating gates."

Takeuchi discloses this limitation. As discussed above in Section 9.1.2,

Takeuchi discloses that "each memory cell gate electrode 13" in the NAND memory array of claim 2 comprises a conductive "floating gate electrode 14 which becomes a charge accumulation layer." MICRON-1005, Takeuchi at 8:26-29; *see* Sections 9.1.2, 9.1.6 and 9.2 above.

9.5. Claim 5 is obvious over Takeuchi in view of Lee

9.5.1. [5.0] "The array according to claim 2, wherein the layered structures are separated in the second direction by distances that are less than one-eighth of a thickness of the layered structures."

Takeuchi in view of Lee renders this limitation obvious, wherein the term "thickness" means "the height as measured from the substrate" under the broadest reasonable interpretation standard. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.3]; *see also* Sections 6.3, 9.1.4 above.

As discussed above in Sections 9 and 9.1.4, increasing the aspect ratio in Takeuchi was a simple design choice that could be accomplished by decreasing the gate-to-gate spacing of the memory cells as disclosed in Lee and/or increasing the height of the memory cell structures in Takeuchi. *See* Sections 9 and 9.1.4 above. A person of ordinary skill in the art would have understood that, for the same reasons discussed above, it would have been obvious to increase the aspect ratio of the memory cell gate electrodes in Takeuchi to greater than 8:1 as required by this limitation. MICRON-1003, Baker Decl., Appx. A at claim [5.0].

As discussed above Takeuchi discloses an exemplary height of the memory

cell gate electrodes 13 (the claimed "thickness of the layered structures") is about 0.6 μm. *See* Section 9.1.4 above. Thus, the gate-to-gate spacing between memory cell gate electrodes in Takeuchi would need to be fabricated at a distance of less than 0.075 μm to satisfy this limitation. Lee discloses such gate-to-gate spacing as discussed above. *See* Section 9.1.4 above; *see also* MICRON-1006, Lee at Fig. 4 (disclosing the parasitic capacitance of memory cell arrays with gate-to-gate spacing as small as 15 nm); MICRON-1003, Baker Decl. Appx. A at claim [5.0].

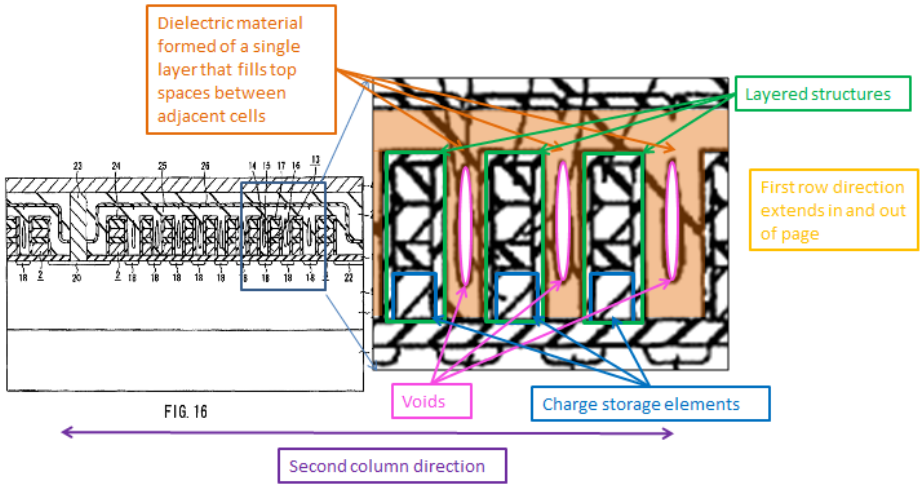
Additionally, the aspect ratio could be increased by, for example, increasing the height of the gate mask film 17, or other components, of the memory cell gate electrodes in Takeuchi, which was a simple design choice. *See* Section 9.1.4 above; *see also* Baker Decl. Appx. A at claim [5.0].

9.6. Claim 6 is obvious over Takeuchi in view of Lee

9.6.1. [6.0] "The array according to claim 2, wherein the dielectric material between the layered structures in the second direction are formed of a single layer of dielectric that fills top portions of spaces therebetween while leaving voids underneath the sealed top portions in between adjacent charge storage elements of the layered structures."

Takeuchi discloses this limitation. As discussed above, Takeuchi discloses a first insulating film 25 ("dielectric material") that is formed between the memory cell gate electrodes 13 ("layered structures") so as to embed the memory cell gate electrodes while also leaving voids between the adjacent memory cell gate

electrodes. *See* Section 9.1.5 above.



MICRON-1005, Takeuchi at Figure 16 (with annotations).

Furthermore, Takeuchi describes that, as shown in Fig. 16 above, the first insulating film is formed of a single layer that fills the top portion between adjacent memory cells such that the "upper surface of the first insulating film 25 is closed." MICRON-1005, Takeuchi at 18:26-38 ("In each embodiment, a cavity may exist in the first insulating film 25 embedding between the memory cell gate electrodes 13… Even if the cavity exists, as long as the upper surface of the first insulating film 25 is closed, the second insulating film 26 is not embedded in the portion between the gate electrodes of the memory cell transistor, therefore, the effects of the present invention will not be changed.").

10. GROUND #2: CLAIMS 1-6 OF THE 849 PATENT ARE UNPATENTABLE AS OBVIOUS OVER SATO IN VIEW OF LEE

As explained below, claims 1-6 of the 849 Patent are unpatentable as obvious over Sato in view of Lee under 35 U.S.C. § 103(a). Sato discloses all of

the elements of claims 1-6 except for an embodiment wherein the gate-to-gate spacing is less than one fifth (or one eighth as required by claim 5) of the height of the memory cells. However, such embodiments would have been obvious by Sato in view of Lee. Additionally, Sato does not expressly disclose an arrangement of the non-volatile memory cells in a standard NAND configuration as required by claim 2, which Lee discloses. A person of ordinary skill in the art therefore would have found claims 1-6 of the 849 Patent obvious over Sato in view of Lee. MICRON-1003, Baker Decl. at Section IX.B.

It would have been obvious to combine the teachings of Sato and Lee as Dr. Baker explains. MICRON-1003, Baker Decl. at Section IX.B. First, Sato states the technical field of the invention is "floating gate type semiconductor memory array devices" and Lee is directed to a floating-gate type memory array in a NAND configuration. MICRON-1007, Sato at [0001]; MICRON-1006, Lee at .002 (Abstract). Additionally, the memory cells in both Lee and Sato are formed in a conventional stack configuration comprising a floating gate and a control gate. *See* MICRON-1007, Sato at [0003], [0042]-[0043], Figs. 9(b), 22(b); MICRON-1006, Lee at Fig. 1. Both references are also directed to the same problem of parasitic capacitance between adjacent floating gates as gate-to-gate spacing is reduced. MICRON-1007, Sato at [0011]; MICRON-1006, Lee at .002 (Introduction). A person of ordinary skill would have recognized these similarities in structure and

function and the problem to be solved and been motivated to combine the teachings of one reference to the other. MICRON-1003, Baker Decl. ¶¶ 104-105.

Second, Sato's EEPROM memory cells would be particularly applicable to the NAND array with reduced gate-to-gate spacing disclosed in Lee. *Id.* ¶ 106. As discussed above, Lee concludes that it would be beneficial to use vacuum isolation between adjacent memory cells, which Sato discloses. *Id.*; *see also* MICRON-1006, Lee at .004 (Conclusion); MICRON-1007, Sato at [0043]-[0044] (method of forming cavities), [0045] ("the interior of the cavity 20 to be in a vacuum state").

Third, Sato describes that the spacing 10 between adjacent floating gates and the spacing 11 between adjacent control gates in the disclosed embodiments can be "less than 0.3 μm" or "less than 0.5 μm." *See, e.g.*, MICRON-1007, Sato at [0008], [0011]. Sato also specifies that by using the disclosed invention, microminiaturization of the spacing between floating gates and control gates can be "taken further than in the related art" while still suppressing "the influence of the charge states of adjacent EEPROM cells during readout." *See, e.g., id.* at [0041], [0042] (describing second embodiment as disclosed in Figs. 9(a) and 9(b)). A person of ordinary skill in the art thus would have been motivated to utilize the memory cell structures of Sato with memory arrays that have reduced gate-to-gate spacing, as disclosed in Lee. MICRON-1003, Baker Decl. ¶ 107.

Fourth, as discussed above in Section 9, a person of ordinary skill in the art

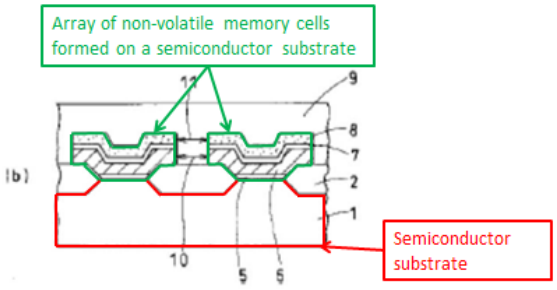
would have been motivated by market pressures and common sense to minimize the gate-to-gate spacing of a non-volatile memory array. *See* Section 9 above. These market pressures would have motivated a person of ordinary skill in the art to combine the memory cells in Sato with the reduced gate to gate spacing disclosed in Lee. MICRON-1003, Baker Decl. ¶ 108. Such a modification would have been an obvious design choice with predictable results (*e.g.*, a memory array with increased storage density). *Id.*

Fifth, NAND arrays of EEPROM memory cells were well known to those of ordinary skill, and it would have been a design choice to arrange the floating-gate type EEPROM cells in Sato as a NAND array such as disclosed in Lee. *Id.* ¶ 109. For example, a NAND configuration is preferable for mass storage devices. MICRON-1006, Lee at .002 ("NAND flash memory has given promise of high-density cell integration, thus it gets much attention as a mass-storage device"). A person of ordinary skill in the art would have understood that such a modification would be a simple substitution of one configuration of a floating-gate type memory cell array for a different type of floating-gate type memory cell array according to known techniques. MICRON-1003, Baker Decl. ¶ 109. Such a combination would have predictable results and would have been obvious to try depending on the application for which the memory cell array was being used. *Id.*

10.1. Claim 1 obvious over Sato in view of Lee

10.1.1. [1.P] "A non-volatile memory cell array formed on a semiconductor substrate, comprising:"

To the extent the preamble is limiting, Sato discloses this limitation. Specifically, Sato relates to "floating gate type semiconductor memory array devices and to manufacture methods thereof." MICRON-1007, Sato at [0001]; *see also id.* at [0002] ("Conventionally, as non-volatile electrically writable and erasable memory, electrically erasable and programmable read only memory (EEPROM) with the floating gate structure were well known"), [0003]-[0004] (describing memory cells), [0042]-[0043] (describing same with reference to Figs. 6 and 9), Figs. 6, 9.



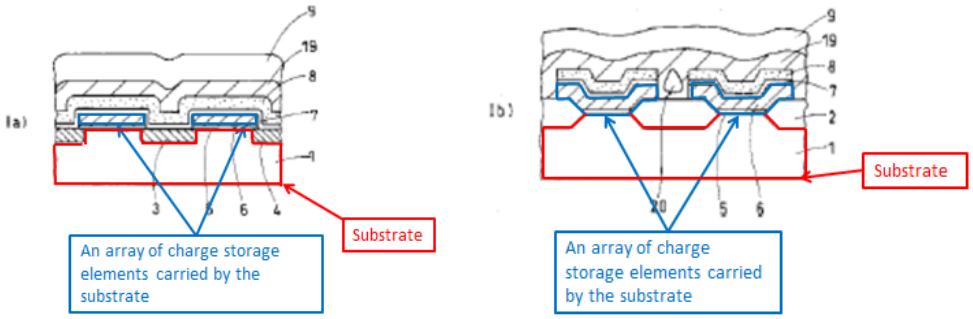
MICRON-1007, Sato at Figure 22(b) (with annotations).

The non-volatile memory arrays are configured from, for example, four EEPROM cells. *Id.* at [0003]. Each EEPROM cell in the array is formed "on a semiconductor substrate 1." *Id.* at [0042].

10.1.2. [1.1] "an array of charge storage elements carried by the substrate,"

Sato discloses this limitation. Each memory cell in Sato includes a "floating gate electrode 6" formed on a gate oxide 5 which in turn is formed on substrate 1.

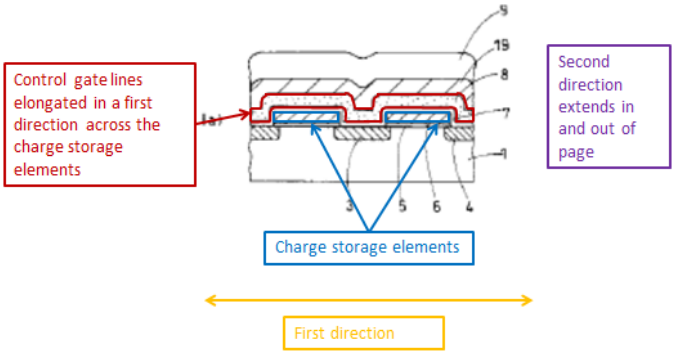
MICRON-1007, Sato at [0042]-[0043]; *see also id.* at [0003] (describing same with reference to Figs. 21 and 22), Figs 21, 22. The floating gate electrode 6 is the claimed "charge storage element." *See id* at [0004] ("…the potential of the floating gate electrode 6 is increased…"); MICRON-1003, Baker Decl. Appx. B at claim [1.1]. As discussed in the previous limitation, the exemplary embodiments in Sato include, for example, four EEPROM cells in an array. *See* Section 10.1.1.



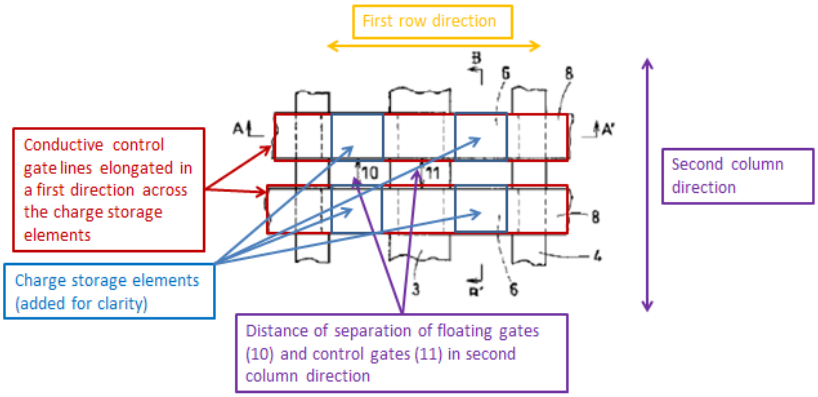
MICRON-1007, Sato at Figures 9(a) and (b) (with annotations).

10.1.3. [1.2] "conductive control gate lines elongated in a first direction across the charge storage elements and being separated in a second direction by a distance of separation of the charge storage elements in the second direction, the first and second directions being orthogonal with each other,

Sato discloses this limitation. Sato states that each memory cell has a "control gate electrode 8" which is deposited over the floating gate electrode 6. *See, e.g.*, MICRON-1007, Sato at [0042]-[0043] (describing Fig. 9), [0003] (describing Figs 21 and 22); *see also id.* at Figs. 21, 22. The control gates are elongated in the first direction across the floating gates as shown in Figs. 6, 9(a) below.



MICRON-1007, Sato at Figure 9(a) (with annotations).



MICRON-1007, Sato at Figure 6 (with annotations).

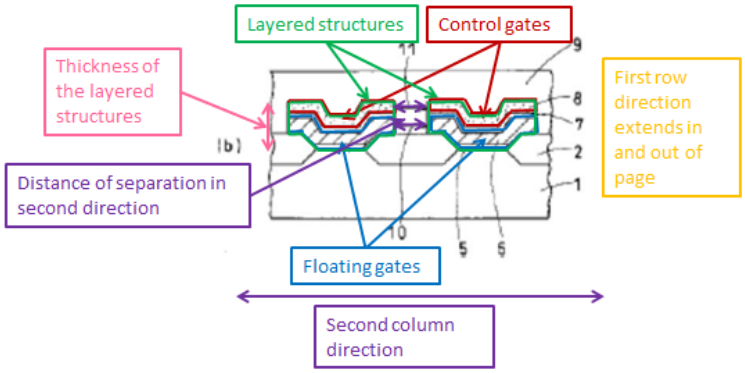
The control gates are separated by a "distance of separation," labeled 11, in the second column direction. MICRON-1007, Sato at [0041] ("…the spacing 11 between adjacent control gate electrodes 8…"); *see also* [0042] (discussing formation of control gates), [0043] (same), *see also id.* at [0008], Figs. 21, 22; MICRON-1003, Baker Decl. Appx. B at claim [1.2].

Furthermore, the control gates are formed upon and aligned with the floating gates, such that the control gates are separated in a second direction by a distance of separation of the charge storage elements in the second direction. MICRON-1007, Sato at [0041] ("…the spacing 10 between adjacent floating gate electrodes

6 and the spacing 11 between adjacent control gate electrodes 8…"); *see also* [0042] (discussing formation of control gates), [0043] (same), *see also id.* at [0008], Figs. 21, 22; MICRON-1003, Baker Decl. Appx. B at claim [1.2]. As noted in the figures, the "first direction" is the row direction and the "second direction" is the column direction, and the first and second directions are orthogonal to one another. *Id.*

10.1.4. [1.3] "wherein layered structures including at least the charge storage elements and the control gates are separated in the second direction by distances that are less than one-fifth of a thickness of the layered structures,"

Sato in view of Lee renders this limitation obvious, wherein the term "thickness" means "the height as measured from the substrate" under the broadest reasonable interpretation standard. *See* MICRON-1003, Baker Decl., Appx. B at claim [1.3]; *see also* Section 6.3 above. First, Sato discloses that the semiconductor memory array devices "are configured from EEPROM with the typical conventional stack type floating gate structure." MICRON-1007, Sato at [0003]. Each stacked memory cell in Sato is a claimed "layered structure" and includes a "floating gate electrode 6" and a "control gate electrode 8." *Id.* at [0003], [0042]-[0043], Figs 21, 22; *see* Sections 10.1.2 and 10.1.3 above. These "layered structures" are shown in, for example, annotated Fig. 22(b) below.



MICRON-1007, Sato at Figure 22(b) (with annotations).

Adjacent floating gate electrodes 6 are separated by a gap 10, and control gate electrodes by a gap 11 in the second column direction. *Id.* at [0008] ("gap 10 between adjacent floating gate electrodes 6, and the gap 11 between adjacent control gate electrodes 8"); *see also* [0041] (describing same with reference to Figs. 6, 9); *see also id.* at Fig. 9(b); annotated Fig. 6 in Section 10.1.3 above.

What Sato does not expressly disclose is an embodiment wherein the gate-to-gate spacing in the second column direction (the spacing 10 and 11) is less than one fifth of the height of the conventional stack structures as required by this limitation. However, a person of ordinary skill in the art would have found it obvious to do so in view of Lee. Specifically, Lee discloses an exemplary non-volatile EEPROM NAND memory array with gate-to-gate spacing of 0.12 μm and Sato discloses exemplary height dimensions for the components of the memory cell structures which, when summed, have a total height from the substrate of

between 790 and 1290 nm[11]. *See* MICRON-1007, Sato at [0042]; MICRON-1006, Lee at .002 ("… experimental results of the floating-gate interference using 0.12 μm [6] design-rule cell…"), Fig. 1 ("In a 0.12 μm design rule cell (gate length=gate space=floating gate height= channel width =120 nm); *see also id.* at .003 (Experiments); MICRON-1003, Baker Decl. Appx. B at claim [1.3]. Thus, the height of the memory cell structures in Sato in view of the reduced gate-to-gate spacing of the memory cell array in Lee disclose aspect ratios of between 6.58:1 to 10.75:1 and render this limitation obvious. *Id.*

As discussed above in Section 10, a person of ordinary skill in the art would have been motivated to make such a combination for several reasons including based on market pressures to increase the storage density of a memory cell array and to more easily form the cavities between memory cells. Additionally, as discussed in Dr. Baker's Declaration, a person of ordinary skill in the art would have understood that increasing the integration density of the memory arrays disclosed in Sato with the gate-to-gate spacing disclosed in Lee could have been accomplished in addition to or without otherwise changing the height of the layered structures. MICRON-1003, Baker Decl., Appx. B at claim [1.3]. Indeed,

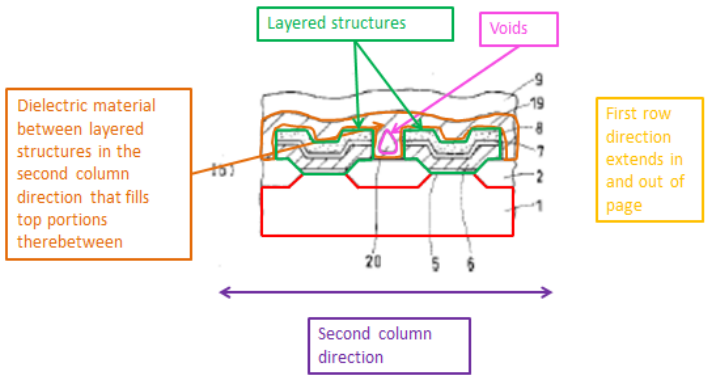
[11] As Dr. Baker explains, the height of the layered structures disclosed in Sato may be as tall as 1290 nm. MICRON-1003, Baker Decl. Appx. B at claim [1.3].

it would have been a simple design choice to design a memory cell array with the gate-to-gate spacing disclosed in Lee to the memory cell stacks with a height of 790 nm to 1290 nm disclosed in Sato. *Id.*

Additionally, nothing in Sato limits the height of the memory cell structures to the disclosed exemplary heights. It would have been a simple design choice to a person of ordinary skill in the art to modify the heights of the memory cells in order to increase the aspect ratio. MICRON-1003, Baker Decl. Appx. B at claim [1.3]. Lee also discloses simulations of memory cells wherein the gate-to-gate spacing between adjacent cells is less than 0.12 μm which could also be used to increase the aspect ratio. *See* MICRON-1006, Lee at Fig. 4 (parasitic capacitance results for gate-to-gate spacing as small as approximately 10 nm); MICRON-1003, Baker Decl. Appx. B at claim [1.3]. As discussed above in Section 10, a person of ordinary skill in the art understood that it was easier to form larger voids when the aspect ratio is high, and thus would have been motivated to increase the aspect ratio of the memory cells in Sato and Lee by decreasing the gate to gate spacing and/or increasing the height of the memory cell structures, depending on the level of shielding between adjacent cells that was needed. *See* Section 10 above; MICRON-1003, Baker Decl. Appx. B at claim [1.3].

10.1.5. [1.4] "dielectric material between the layered structures in the second direction that fill top portions of spaces therebetween while leaving voids between adjacent charge storage elements of the layered structures, and"

Sato discloses this limitation. As discussed in the previous limitation, Sato discloses memory cells in a conventional stack formation which are the claimed "layered structures." *See* Section 10.1.4 above. Sato also states that a silicon oxide insulating film 19 ("dielectric material") is formed over and between the memory cells (the claimed "layered structures"). MICRON-1007, Sato at [0043] ("…a silicon oxide insulating film 19 is deposited over the whole surface."). The dielectric film 19 does not entirely fill between adjacent memory cells in the second column direction thus forming a cavity 20 between the floating gate and control gate electrodes of adjacent memory cells. *Id.*; *see also id.* at [0044] ("a cavity is provided both between adjacent floating gate electrodes 6 and between adjacent control gate electrodes 8"), [0045] (further describing cavities).

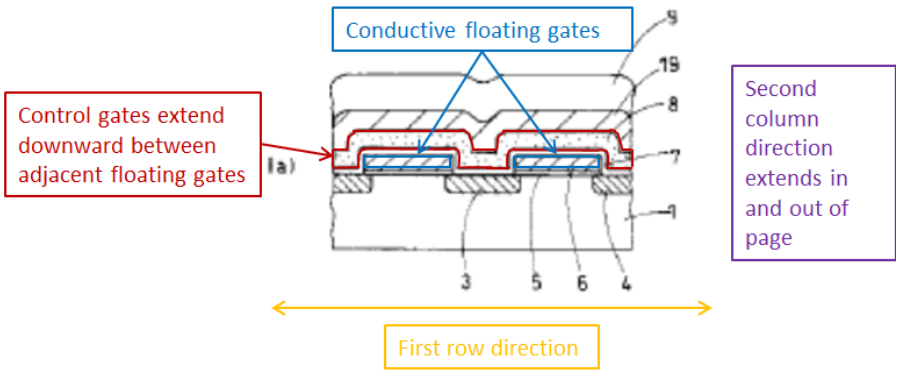


MICRON-1007, Sato at Figure 9(b) (with annotations).

The cavity is a "void" between adjacent "layered structures" in the second column direction as shown in annotated Fig. 9(b) above. MICRON-1003, Baker Decl., Appx. B at claim [1.4].

10.1.6. [1.5] "wherein the charge storage elements are conductive floating gates and the elongated control gate lines extend downward between adjacent floating gates in the first direction."

Sato discloses this limitation. As discussed above with respect to claims [1.1] and [1.2], the "charge storage elements" in Sato are floating gate electrodes 6, which have control gate electrodes 8 that extend across a plurality (two in the exemplary embodiment) of floating gate electrodes 6 in a row. *See* Sections 10.1.2 and 10.1.3 above. The floating gates are made of polysilicon and are therefore conductive. MICRON-1007, Sato at [0042]-[0043]. Furthermore, the control gates extend across and downward between adjacent floating gates in the first row direction. *See id.* at [0042]-[0043] (describing formation of control gate electrodes); MICRON-1003, Baker Decl. Appx. B at claim [1.5].



MICRON-1007, Sato at Figure 9(a) (with annotations).

10.2. Claim 2 is obvious over Sato in view of Lee

The limitations of claim 2 are identical to claim 1 except for the final limitation. Accordingly, the discussion in Sections 10.1.1, 10.1.2, 10.1.3, 10.1.4 and 10.1.5 are hereby incorporated by reference for the identical limitations in

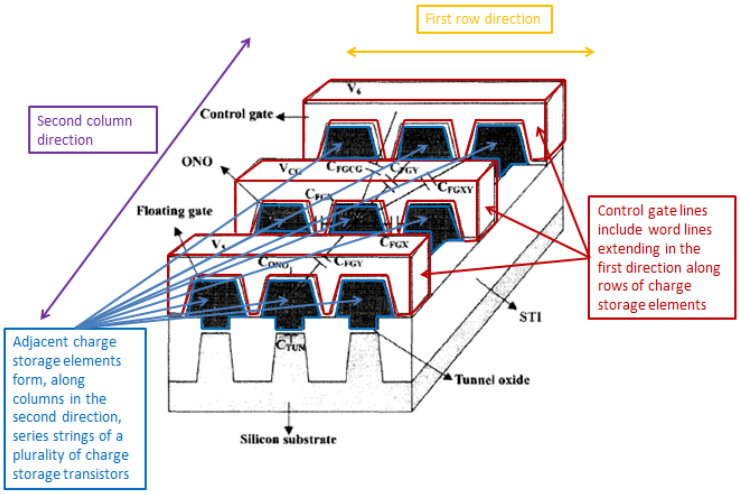
claim 2. The final limitation of Claim 2 is addressed below.

10.2.1. [2.5] "wherein the control gate lines include word lines extending in the first direction along rows of charge storage elements and the charge storage elements form, along columns in the second direction, series strings of a plurality of charge storage transistors."

Sato in view of Lee discloses this limitation, which simply requires that the claimed non-volatile memory cell array is formed in a NAND configuration. MICRON-1003, Baker Decl., Appx. B at claim [2.5]. As discussed above in Section 10.1.3, Sato discloses elongated control gates which extend across a plurality of floating gate electrodes in the first row direction. *See* Section 10.1.3 above. What Sato does not expressly disclose is a NAND configuration wherein the floating gates are arranged as a "series strings of a plurality of charge storage transistors" in the second direction, and that the control gates are "word lines." MICRON-1003, Baker Decl. Appx. B at claim [2.5]. Such a configuration is disclosed in Lee.

Specifically, Lee discloses a NAND array with 16-cell NAND memory transistor strings in the bit line (*i.e.* column) direction, and the control gates are word lines extending along floating gates in the first row direction. MICRON-1006, Lee at .002 ("In a 0.12-μm design-rule NAND flash cell, the floating-gate interference corresponds to about 0.2 V shift in multilevel cell operation. Furthermore, the adjacent word-line voltages affect the programming speed via

parasitic capacitors."), .003 ("It is measured in a 16-cell NAND string, in which each cell is sequentially named from the common ground to the bit-line direction as 'WL0 cell' to 'WL15 cell'.").



MICRON-1006, Lee at Figure 1 (with annotations).

As discussed above, NAND arrays of EEPROM memory cells were well known to those of ordinary skill, and it would have been a design choice to arrange the floating-gate type EEPROM cells in Sato as a NAND array and would have been motivated to do so, for example, for use as a mass storage device. *See* Section 10 above; MICRON-1003, Baker Decl. Appx. B at claim [2.5].

10.3. Claim 3 is obvious over Sato in view of Lee

10.3.1. [3.0] "The array according to claim 2, wherein the dielectric material includes at least one of silicon dioxide and silicon nitride."

Sato in view of Lee discloses this limitation. As discussed in Section 10.1.5 above, Sato discloses that a silicon oxide dielectric film 19 is formed between adjacent memory cells in the second column direction. *See* Section 10.1.5 above.

Specifically, the silicon oxide film 19 is formed using "silane gas and oxygen." MICRON-1007, Sato at [0043]. Silicon dioxide was commonly referred to as silicon oxide by those of ordinary skill in the art, including as used in the 849 Patent. MICRON-1003, Baker Decl. Appx. B at claim [3.0]; *see also* Section 9.3.1 above. Similarly, Lee discloses that the dielectric material that fills the gate-to-gate spacing can be either silicon oxide or silicon nitride. *See, e.g.*, MICRON-1006, Lee at .003.

10.4. Claim 4 is obvious over Sato in view of Lee

10.4.1. [4.0] "The array according to claim 2, wherein the charge storage elements are conductive floating gates."

Sato discloses this limitation. As discussed above, the memory cells in Sato are floating-gate type memory cells wherein the charge storage element is a conductive polysilicon floating gate electrode 6 that stores electrical potential. *See* Sections 10.1.1, 10.1.2, 10.1.3 and 10.1.6 above.

10.5. Claim 5 is obvious over Takeuchi in view of Lee

10.5.1. [5.0] "The array according to claim 2, wherein the layered structures are separated in the second direction by distances that are less than one-eighth of a thickness of the layered structures."

Sato in view of Lee renders this limitation obvious, wherein the term "thickness" means "the height as measured from the substrate" under the broadest reasonable interpretation standard. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.3]; *see also* Sections 6.3, 10.1.4 above.

As discussed above with respect to claim [1.3], Sato in view of Lee discloses aspect ratios of between 6.58:1 to 10.75:1. In other words, Sato in view of Lee discloses wherein the height of the memory cell "layered structures" is 6.58 to 10.75 times larger than the width between adjacent memory cells in the second direction. *See* Section 10.1.4 above.

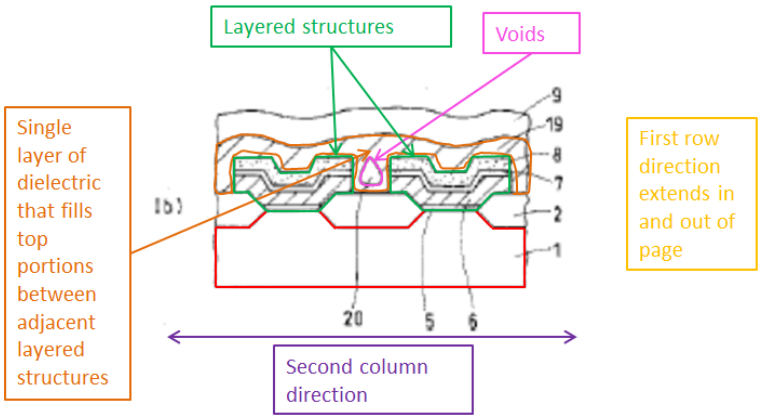
Additionally, further increasing the aspect ratio by decreasing the gate-to-gate spacing, as disclosed in Lee, or increasing the height of the memory cell "layered structures" in Sato would have been a simple design choice that was obvious to a person of ordinary skill in the art, and would have predictable results (*i.e.* larger voids between adjacent memory cells with increased shielding). *Id.;* MICRON-1003, Baker Decl., Appx. B at claim [5.0].

10.6. Claim 6 is obvious over Takeuchi in view of Lee

10.6.1. [6.0] "The array according to claim 2, wherein the dielectric material between the layered structures in the second direction are formed of a single layer of dielectric that fills top portions of spaces therebetween while leaving voids underneath the sealed top portions in between adjacent charge storage elements of the layered structures."

Sato discloses this limitation. As discussed in claim [1.4], Sato discloses a silicon oxide film 19 that is deposited so as to form a cavity between adjacent floating gate electrodes and control gate electrodes in the second column direction. *See* Section 10.1.5 above. Sato also discloses and depicts that the silicon oxide

film is deposited in a single layer such that it "overhangs" and fills the top portions of the spacing between memory cells, thus forming the cavity 20. MICRON-1007, Sato at [0043].



MICRON-1007, Sato at Figure 9(b) (with annotations).

11. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1-6 of the 849 Patent is requested.

Respectfully submitted,

Dated: December 14, 2015

By: _____

Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73,604
Weil, Gotshal & Manges LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: 650-802-3237

CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	December 14, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 7,045,849 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1018
Persons served	Patent Owner's Address of Record: Hill, Van Santen, Steadman & Simpson P.C. 85th Fl. Sears Tower 233 South Wacker Dr. Chicago, IL 60606 Additional Addresses Known as Likely to Effect Service: Brian E. Farnan Farnan LLP 919 North Market Street, 12th Floor Wilmington, DE 19801 bfarnan@farnanlaw.com Edward C. Flynn Cohen & Grace, LLC 105 Braunlich Drive, Suite 300 Pittsburgh, PA 15237 eflynn@cohengrace.com

/ Jeremy Jason Lang /
Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73,604