UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

INNOVATIVE MEMORY SYSTEMS, INC.
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 6,169,503
Title: PROGRAMMABLE ARRAYS FOR DATA CONVERSIONS BETWEEN ANALOG AND DIGITAL

Petition For *Inter Partes* Review of U.S. Patent No. 6,169,503 Under 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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TABLE OF CONTENTS

Page

Exhibit List

Micron Exhibit #	Description
MICRON-1001	U.S. Patent No. 6,169,503 ("503 Patent")
MICRON-1002	File History for U.S. Patent No. 6,169,503
MICRON-1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 5,376,935 ("Seligson")
MICRON-1006	U.S. Patent No. 5,187,483 ("Yonemaru")
MICRON-1007	U.S. Patent No. 4,591,825 ("Bucklen")
MICRON-1008	R. J. Baker et al., *CMOS Circuit Design, Layout, and Simulations* (1998) ("Baker CMOS Circuit Design")
MICRON-1009	EP Patent Specification No. 0 221 238 ("Knierim 238")
MICRON-1010	U.S. Patent No. 5,019,820 ("Matsuzawa")
MICRON-1011	U.S. Patent No. 5,382,955 ("Knierim 955")
MICRON-1012	U.S. Patent No. 4,533,903 ("Yamada")

Micron Exhibit #	**Description**
MICRON-1013	U.S. Patent No. 4,183,016 ("Sawagata")
MICRON-1014	U.S. Patent No. 5,029,136 ("Tran")
MICRON-1015	United States Copyright Office public record search result for R. J. Baker et al., *CMOS Circuit Design, Layout, and Simulations* (1998).
MICRON-1016	Declaration of Mariellen F. Calter regarding R. J. Baker et al., *CMOS Circuit Design, Layout, and Simulations* (1998) ("Calter Decl.")

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1, 8, 9, and 10 of U.S. Patent No. 6,169,503, titled "Programmable Arrays for Data Conversions Between Analog and Digital" (MICRON-1001, the "503 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 503 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 503 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang Registration No. 73,604 (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Douglas W. McClellan Registration No. 41,183 (doug.mcclellan@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5313; F: 713-224-9511

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for Petitioner is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this Petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Innovative Memory Systems has asserted the 503 Patent and U.S. Patent Nos. 6,324,537 (the "537 Patent"), 6,901,498 (the "498 Patent"), 7,000,063 (the "063 Patent"), 7,045,849 (the "849 Patent"), 7,085,159 (the "159 Patent"), 7,495,953 (the "953 Patent") and 7,886,212 (the "212 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Innovative Memory Systems, Inc., v. Micron Tech., Inc.*, 14-cv-1480 (D. Del.) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 6,324,537, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 6,901,498, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,000,063, IPR2016-Unassigned;

Petition for *Inter Partes* Review of U.S. Patent No. 7,045,849, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,085,159, IPR2016-Unassigned; Petition for *Inter Partes* Review of U.S. Patent No. 7,495,953, IPR2016-Unassigned; and Petition for *Inter Partes* Review of U.S. Patent No. 7,886,212, IPR2016-Unassigned.[1]

The 503 Patent does not claim priority to any foreign or U.S. patent application.

2.5. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

2.6. Proof of Service

Proof of service of this Petition on the patent owner at the correspondence address of record for the 503 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

Ground #1: Claim 1 of the 503 Patent is invalid under (pre-AIA) 35 U.S.C. § 102(b) on the ground that it is anticipated by U.S. Pat. No. 5,376,935, to Seligson, entitled "Digital-To-Analog And Analog-To-Digital Converters Using Electrically Programmable Floating Gate Transistors," filed on March 30, 1993 and issued on December 27, 1994. MICRON-1005 ("Seligson").

[1] These petitions will be filed concurrently or within a few days.

Ground #2: Claim 1 of the 503 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Seligson in view of U.S. Pat. No. 5,187,483, to Yonemaru, entitled "Serial-To-Parallel Type Analog-Digital Converting Apparatus And Operating Method Thereof," filed on November 26, 1991 and issued on February 16, 1993. MICRON-1006 ("Yonemaru").

Ground #3: Claim 8 of the 503 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Seligson in view of U.S. Pat. No. 4,591,825, to Bucklen, entitled "Analog-To-Digital-Converter And Related Encoding Technique," filed on August 22, 1983 and issued on May 27, 1986. MICRON-1007 ("Bucklen").

Ground #4: Claim 8 of the 503 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Seligson in view of Yonemaru and Bucklen.

Ground #5: Claims 9-10 of the 503 Patent are invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that they are obvious over Seligson in view of Yonemaru.

These grounds are explained below and are supported by the Declaration of Dr. R. Jacob Baker (MICRON-1003, "Baker Decl.").

4. BACKGROUND OF TECHNOLOGY AND OVERVIEW OF THE 503 PATENT

The 503 Patent was filed on September 23, 1998 and issued on January 2, 2001. The 503 Patent relates generally to analog-to-digital converters and digital-to-analog converters. The claims at issue (1 and 8-10) in this Petition relate to analog-to-digital converters ("A/D converters").

An A/D converter converts an analog signal, such as a voltage, to a digital value. This may be necessary to, for example, store an analog signal in digital form (*e.g.*, an audio signal). *See* MICRON-1001, 503 Patent at 1:13-20. The 503 Patent allegedly builds on the basic A/D converter by using a special type of comparator to reduce the footprint of traditional A/D converters, namely, using reference cells (*e.g.*, flash memory cells) as the comparators. The below summarizes the basic building blocks of an A/D converter to put the alleged invention of the 503 Patent in context. The relevant claims of the 503 Patent include these basic building blocks but substitute a specific type of comparator.

Generally speaking, converting an analog signal to a digital value requires using (1) quantization levels (also known as reference values), (2) comparators, and (3) an encoder. *See id.* at 1:35-52. Quantization levels are discrete digital values with corresponding analog signals or voltages that serve as reference values to compare against an analog signal. Comparators perform comparisons of the analog signal to the reference values. And an encoder generates a digital value

from the results of the comparisons, *e.g.*, a digital value in binary or decimal form. *See id.*

As an example of a basic A/D conversion using these components, let us assume that an analog voltage represents temperature, and the temperature will be any value within 0-50 degrees. Let us further assume that we have 25 quantization levels, each of which represents a 2 degree band, *i.e.*, 0, 2, 4, 6, etc., degrees (each of which has a corresponding reference voltage). With this, comparators can perform 25 comparisons using the analog temperature voltage and the reference voltages: is the temperature (1) greater than 0 degrees, (2) greater than 2 degrees, (3) greater than 4 degrees, etc. The comparators simply compare the analog signal (which represents the temperature) to each of the reference voltages. At some point, the comparators will indicate the approximate analog value in digital form because the comparisons will transition from returning a positive result (the analog signal is greater than the respective reference voltages) to negative result (the analog signal is not greater than the respective reference voltages). For example, if the first two comparators return a positive result, but the third returns a negative result, we know the temperature is between 2-4 degrees. Using the results of these comparisons, encoders generate a digital value that represents this range. For example, the encoder may encode this result into a binary number 3 (*i.e.*, 11) to

represent the temperature is between 2-4 degrees. *See* MICRON-1003, Baker Decl. ¶ 34.

The above describes a flash[2] or parallel converter, which along with serial-to-parallel converters, is at issue in this Petition. These converters use a comparator for each level of quantization.[3] The result of each comparison produces what is known as thermometer code, *i.e.*, a logical 0 or 1 value that represents the result of the respective comparison. *See* MICRON-1001, 503 Patent at 5:14-37; *see also* MICRON-1003, Baker Decl. ¶¶ 36-39 (describing thermometer code and citing MICRON-1008, Baker CMOS Circuit Design[4] at

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[2] "Flash" in this context does not refer to flash memory.

[3] A serial-to-parallel converter uses a 2-phase approach: one for the upper bits and one for the lower bits (*see* discussion of Yonemaru *infra*). These converters use a comparator for each level of quantization for the upper and lower bits separately, but by using a two phase approach, it reduces the total number of comparators relative to a pure parallel converter. *See* MICRON-1003, Baker Decl. ¶¶ 91-92.

[4] R. J. Baker et al., *CMOS Circuit Design, Layout, and Simulations* (1998) ("Baker CMOS Circuit Design"). Baker CMOS Circuit Design has an imprint with a copyright date of 1998. The United States Copyright Office discloses a publication date of August 8, 1997 in the official registration of copyright. *See* MICRON-

.054-.055, .076-.077 and MICRON-1009, Knierim 238 at 2:33-35). For example, if the comparison is true (greater than the quantization level), the comparator may produce a logical 1. In this way, the comparators will produce logical 1s until what is known as the transition or boundary. At that point, the comparators will produce logical 0s because the analog value is less than all quantization levels above that point. The encoder uses this thermometer code to encode the digital result. *See id.*

An encoder typically encodes the thermometer code to a more useful form. Below is an example of 8 quantization levels and their corresponding decimal, thermometer, and binary code.

Decimal Value	Binary Number			Thermometer Code							
	B2	B1	B0	T7	T6	T5	T4	T3	T2	T1	T0
0	000			0000000							
1	001			0000001							
2	010			0000011							
3	011			0000111							
4	100			0001111							
5	101			0011111							

1015 (Retrieved Dec. 7, 2015 from the United States Copyright Office public record search). In addition to the copyright and publication date of the reference, *see* MICRON-1016 ("Calter Declaration") which provides additional evidence of its availability to the public.

Decimal Value	Binary Number	Thermometer Code
6	110	0111111
7	111	1111111

As can be seen from above, the binary number (which represents the decimal form in a useable computer version) is much more compact than the thermometer code. Therefore, encoders often convert the result to a binary number. *See* MICRON-1003, Baker Decl. ¶¶ 36-39 (describing thermometer code and citing MICRON-1008, Baker CMOS Circuit Design at .054-.055, .076-.077 and MICRON-1009, Knierim 238 at 2:33-35).

Notably, as was well known in the prior art and as is evident from the above table, the conversion of thermometer to binary code requires only counting or adding the number of logical 1s (or logical 0s if logical 0 represents a true comparison result) in the thermometer code. *See* MICRON-1003, Baker Decl. ¶ 39; *see also* MICRON-1009, Knierim 238 at 2:33-34 ("It should be noted that the technique of counting the logical-true bits also correctly encodes an in-sequence thermometer code input."). With this approach, an encoder can comprise a simple adder to count the values of the thermometer code until the transition point, thereby converting the thermometer code into binary code. *See, e.g.*, MICRON-1007, Bucklen at 1:6-40.

The 503 Patent alleges that prior art converters require a large circuit area and consume a large amount of power primarily due to the comparators, which

may comprise, for example, reference resistors. MICRON-1001, 503 Patent at 1:35-2:11. In simple terms, the 503 Patent teaches that rather than using a row of resistor-type comparators, a row of reference cells such as programmable threshold transistors (programmable flash cells)[5] can instead perform the comparisons. *See id.* at 2:34-59, 3:6-24. The threshold voltages of the reference cells serve as the reference values. These reference cells produce the exact same thermometer code as the conventional prior art resistor-type comparators in serial-to-parallel and parallel converters. *See id.* Therefore, prior art encoding techniques are equally applicable.

An embodiment of the 503 Patent is shown below:

[5] A programmable threshold transistor is simply a transistor wherein its threshold voltage is programmable to different values. A transistor "turns on," that is, becomes conductive across its channel, if the voltage applied to its control gate is greater than its threshold voltage. *See* MICRON-1003, Baker Decl ¶¶ 28, 32.

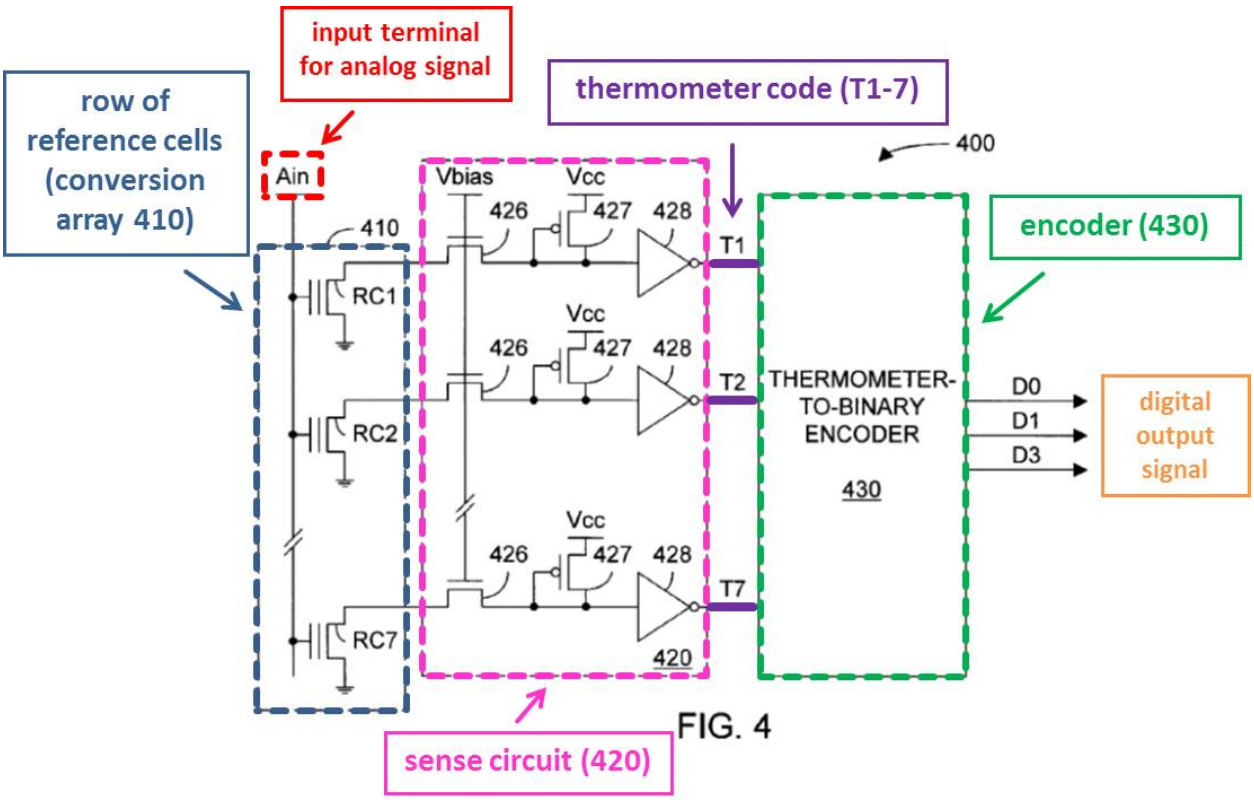

FIG. 4

MICRON-1001, 503 Patent at Figure 4 (with annotations).

Fig. 4 depicts the conversion array in the column direction, but the 503 Patent also depicts the same array as a row, such as in Fig. 3 (claims 9-10 require a conversion array with multiple rows). The reference array 410 and sense circuit 420 function together as comparators, and the rest of the A/D converter functions as a conventional flash or parallel converter.

The reference array 410 includes reference cells RC1-7. *See id.* at 4:55-64. The reference cells may be programmable floating gate transistors (*i.e.*, flash type memory cells). *See id.* at 3:13-16. Each of the reference cells has a different threshold voltage that, for example, corresponds to a digital value (the threshold

voltages are the quantization levels). *See id.* at 4:57-63. The sense circuit biases the lines to the encoder. The analog signal A_{in} is applied to the control gates of each reference cell. When the reference cells are conductive, the cells pull down the voltage to ground, whereas if the cells are not conductive, the sense circuit pulls up the lines to logical high voltage. The reference cells become conductive if the analog signal applied to their gate is greater than their respective threshold voltage. *See id.* at 5:6-13. Thus, if the reference cell is conductive, this means that the comparison is a true: the analog signal is greater than that reference value (a quantization level). In this way, the reference cells perform the comparison step. *See id.* at 4:65-5:13. These comparisons generate thermometer code at the input side of the encoder in the same manner as prior art parallel and serial-to-parallel converters using resistor-type comparators. *See id.* at 5:14-37.

Indeed, the 503 Patent notes that the encoding methods to encode thermometer code are "well known," *see id.* at 5:36-37, and provides a similar thermometer to binary encoding table as above. *Id.* at 5:20-35. Accordingly, the 503 Patent allegedly simply builds on the traditional flash converter by replacing the resistor-type comparators with, for example, floating gate transistors.

The 503 Patent also describes an embodiment in which there are multiple rows and a select circuit that, via a row decoder, can select a specific row to which to apply the analog signal. *See id.* at 7:9-20. This simply amounts to stacking

multiple rows of the reference cells from Figs. 3-5 of the 503 Patent on top of one another and selecting only a single row for the conversion. A row decoder simply selects the appropriate row to apply the analog signal. *See id.* at 7:14-17. The 503 Patent notes that this may allow for different types of conversions. *See id.* at 9:18-31.

5. 503 PATENT PROSECUTION HISTORY

The application that led to the issuance of the 503 Patent was originally filed with 21 claims. MICRON-1002, 9-23-1998 Application at .024-.028. The below provides a table that correlates the original claims to the issued claims:

Original	Issued Claim
4	1
15	8
16	9
17	10

This summary focuses on the claims at issue in this Petition.[6] On March 24, 2000, original claim 4 was rejected as anticipated based on U.S. Pat. No. 5,376,935

[6] As to the whole of the file history, there was a single Office Action. *See* MICRON-1002, 3-24-2000 Office Action at .048-.051. Claim 19 was rejected under 35 U.S.C. ¶ 112. *Id.* at .049. Claims 1-5 and 8-12 were rejected as anticipated by U.S. Pat. No. 5,376,935 (Seligson). *Id.* at .050. Claims 6, 7, 13, 14, 16, and 20 were rejected under 35 U.S.C. ¶ 103(a) over Seligson in view of EP 0

(Seligson). Original claim 16 was rejected as being unpatentable over Seligson in view of EP 0 798 739 (Dunlap et al.). The Examiner found that while Seligson did not disclose a matrix (multiple rows), Dunlap taught multiple rows of a conventional memory system. Original claim 17 was rejected as being unpatentable over Seligson, Dunlap, and further in view of U.S. Pat. No. 5,694,356 (Wong). The Examiner found that while Seligson and Dunlap did not disclose a counter that provides address information, Wong provides a counter for sequential addressing. Original claims 15 and 21 were objected to because they were dependent on a rejected claim, but would be allowable if rewritten. *See* MICRON-1002, 3-24-2000 Office Action at .051.

On July 3, 2000, Applicant argued that original claim 4 is patentable because it recites "an array of memory cells that contains the plurality of transistors."

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798 739 (Dunlap et al.). *See id.* Claims 17-19 were rejected under 35 U.S.C. ¶ 103(a) over Seligson, Dunlap, and further in view of U.S. Pat. No. 5,694,356 (Wong). *Id.* at .051. Claims 15 and 21 were only objected to as being dependent on a rejected base claim. *See id.* Applicant rewrote claims 15 and 21 into independent form and cancelled claims 1-3, 8, 10, 13, and 14. *See Id.*, 7-3-2000 Amendment at .062. Examiner then allowed the claims. *See id.*, 8-28-2000 Notice of Allowability at .068-.069.

Applicant argued that Seligson provides no disclosure that the plurality of transistors of Seligson form part of a memory array. *See id.*, 7-3-2000 Amendment at .062-.063. Applicant argued that original claim 16 was not obvious in view of Seligson and Dunlap because Dunlap simply provides a traditional array of memory cells and it would not have been obvious in light of Dunlap to select a single row and provide the analog signal to that row. *See id.* at .064-.065. Applicant argued that original claim 17 was not obvious in view of Seligson, Dunlap, and Wong because it recited "a terminal for a conversion select signal … coupled to provide at least a portion of an address." *See id.* at .065. Claims 15 and 21 were rewritten into independent form. *See id.* at .062.

On August 28, 2000, the Examiner allowed original claims 4-7, 9, 11, 12, and 15-21. The Examiner noted that: "[t]he art of record does not show the array of cells as used by applicant, *i.e.* multi-row, or the read circuit. Additionally, the combined analog-to-digital converter and digital-to-analog converter is not disclosed as the art of record only shows these in separate embodiments." *Id.*, 8-28-2000 Notice of Allowability at .069.

Notably, the Examiner did not cite to the section of Seligson that discloses an "array" of reference transistors: "[a]nother prior method of constructing the voltage ladder is to **use an array of metal-oxide-semiconductor (MOS) transistors**, **each transistor of the array** having a different threshold voltage

corresponding to one of the desired voltages of the voltage ladder." MICRON-1005, Seligson at 1:33-37.[7] Accordingly, it does not appear that the Examiner appreciated that Seligson discloses an "array" of reference transistors. Also, the Examiner did not cite to the second row of programmable floating gate transistors (memory cells) in Fig. 4 of Seligson (63a-h), suggesting that the Examiner may not have appreciated that transistors 62a-h of Seligson reside in a larger matrix. *See id.* at Fig. 4.

6. CLAIM CONSTRUCTION[8]

6.1. Applicable Law

A claim subject to *inter partes* review is given the "broadest reasonable

[7] Emphasis is added throughout unless otherwise noted.

[8] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 503 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 503 Patent.

construction in light of the specification of the patent in which it appears."[9] 37 C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill in the art and consistent with the specification of the 503 Patent. Petitioner respectfully submits that the following terms shall be construed for this IPR:

6.2.1. "array" (claims 1 and 8-10)

The term "array" is a limitation of claims 1, 8, and 9 of the 503 Patent, and thus is also a limitation of dependent claim 10.

[9] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

Under the broadest reasonable construction standard, this term in light of the specification would have been understood to mean "two or more elements that form at least one of a row or column." *See* MICRON-1003, Baker Decl. ¶¶ 61-65. This Petition, however, includes alternative Grounds 2 and 4 which assume that "array" means at least 2 rows or columns of elements.

First, the specification of the 503 Patent supports this construction. Specifically, it uses "array" to refer to two or more elements in either the row or column direction—including when these elements comprise only one row or only one column. Thus, a construction requiring "array" to require multiple rows or columns would be inconsistent with the 503 Patent's own usage of the term "array." For example, the 503 Patent states: "ADC 300 includes a conversion array 310 containing reference cells RC0 to RCx with respective threshold voltages VT0 to VTx." *See* MICRON-1001, 503 Patent at 4:23-25. Here, as shown in Fig. 3, the 503 Patent uses "array" to refer to a single row of reference cells because array 310 includes only a single row. Likewise, the 503 Patent states: "[a]rray 410 includes seven reference cells RC1 to RC7." *Id.* at 4:57-58. Here, as shown in Fig. 4, the 503 Patent uses "array" to refer to a single column of reference cells because array 410 includes only a single column.

The claim language itself also makes clear that an array can be a single row or column. Claim 8 recites "an array of reference cells." *See id.* at Claim 8.

Claim 9 recites "an array of reference cells … wherein the array contains a plurality of rows." *See id.* at Claim 9. Thus, claim 9 recognizes that an "array" could include only a single row, because the "wherein the array contains a plurality of rows" would otherwise be redundant.

Further, this is the common usage of an "array" for a person of ordinary skill in the art in semiconductor design and in science, engineering, computer science, and mathematics. *See, e.g.*, MICRON-1003, Baker Decl. ¶ 65 (citing U.S. Pat. No. 5,029,136 at 4:43-50 as exemplary support).

6.2.2. "a counter coupled to count pulses from the sense circuit" (claim 8)

The term "a counter coupled to count pulses from the sense circuit" is a limitation of claim 8.

Under the broadest reasonable construction standard, this term in light of the specification would have been understood to mean "a counter that counts changes in current or voltage from a circuit that indicates whether a given reference cell is conducting." *See* MICRON-1003, Baker Decl. ¶¶ 67-68. The 503 Patent describes this "counter" as counting the thermometer code to create the digital output. *See* MICRON-1001, 503 Patent at 6:11-20. The thermometer code reflects the logical states that the reference cells and sense circuit generate and output to the encoder. *See id.* at 5:15-37. Thus, the counter is counting changes in current or voltage (the

logical states that the reference cells and sense circuit generate), and these changes are a result of whether the reference cells are conducting.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 503 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design of memory devices. An individual with an advanced degree in a relevant field would require less experience in the design of memory devices. *See* MICRON-1003, Baker Decl. ¶ 19.

8. DESCRIPTION OF THE PRIOR ART

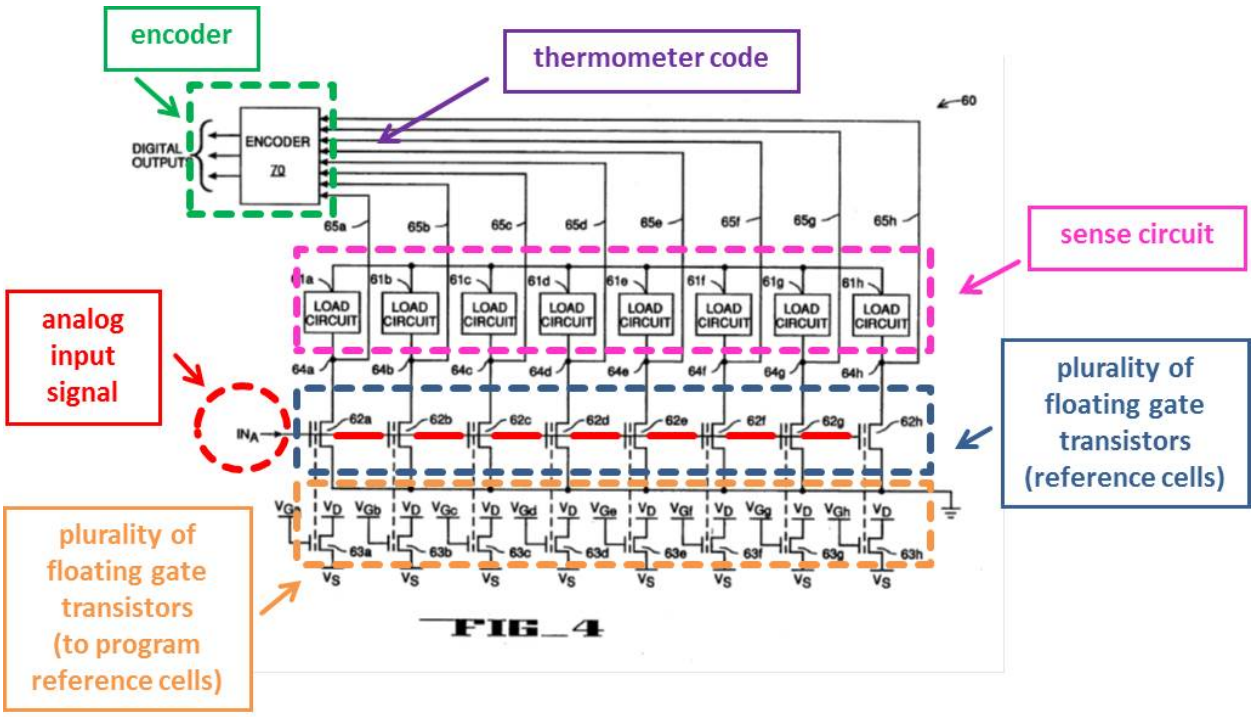
8.1. U.S. Patent No. 5,376,935 ("Seligson")[10]

Seligson describes the same prior art problem with A/D converters as the 503 Patent, *i.e.*, that prior art approaches using resistor-type comparators require a relatively large amount of space. *See* MICRON-1005, Seligson at 1:15-24. Seligson recognizes, however, that even prior art A/D converters solved this

[10] Seligson issued on December 27, 1994 and is prior art under 102(b). *See* MICRON-1005, Seligson. Seligson was cited as prior art during the prosecution of the 503 Patent. As explained above, the Examiner did not cite the portions of Seligson disclosing an array of reference transistors. *See* Section 5, above.

problem by using an "array" of MOS transistors with different threshold voltages, just like the 503 Patent. *See id.* at 1:33-53. Seligson criticizes this prior art as expensive because the MOS transistors were expensive to fabricate with different threshold voltages. *See id.* at 1:33-2:15. Accordingly, Seligson extends this concept of using MOS transistors with different threshold voltages to using floating gate transistors specifically, just like an embodiment of the 503 Patent, because it was possible to program these transistors to different threshold voltages (which reduces cost). *See, e.g., id.* at 1:33-2:7.

The below is an exemplary embodiment shown in Fig. 4 of Seligson that uses floating gate transistors. Seligson shows only an exemplary row of floating gate reference transistors in Fig. 4. To the extent "array" is read to mean multiple rows or columns, it would have been obvious to include additional rows of floating gate reference cells in Fig. 4 because Seligson itself recognizes prior art "array[s]" of reference transistors (*see id.* at 1:33-53). *See infra* at Section 4; *see also* MICRON-1003, Baker Decl. ¶ 73.



MICRON-1005, Seligson at Figure 4 (with annotations).

The embodiment above operates precisely as does the 503 Patent. The IN_A analog signal (analog voltage) enters the above circuit via a terminal (as shown with the arrow), which in turn, is applied to the gates of each of 8 reference floating gate transisters 62a-h. The reference floating gate transisters 62a-h each has a different threshold voltage, *e.g.*, increasing respectively by 1 volt from 1-8 volts (thus 62a has a threshold voltage of 1 volt, 62b of 2 volts, etc.). MICRON-1005, Seligson at 7:35-65. Transistors 62a-h and the Load Circuits 61a-h serve as comparators. Specifically, after application of the analog signal IN_A, certain transistors 62a-h will become conductive, namely, each transistor with a threshold voltage that is less than the analog signal voltage. For example, if IN_A is 3.5 volts, the first 3 transistors turn on. The Load Circuits sense whether the transistors

become conductive by biasing lines 65a-h and allowing transistors 62a-h to pull down the lines to a logical low if the transistors do conduct and by maintaining lines 65a-h at logically high if the transistors do not conduct. Thus, a logical low value indicates that a respective analog signal has a voltage that is greater than that transistor's respective threshold voltage because the IN_A analog signal was able to turn on that transistor. Just like the 503 Patent, Seligson uses floating gate transistors (flash memory cells) and a sense circuit to perform the comparison step.

The comparison step generates thermometer code on lines 65a-h. *See id.* at 7:66-8:14. Following the example of IN_A being 3.5 volts, lines 65a-c will be at a logical zero, and lines 65e-h will be at a logical high. The thermometer code sent to the decoder therefore is 00011111. The encoder converts this to a 3-bit binary number, namely, 011, which is simply a count of the logical 0s. *See id.* at 8:15-21.

Note that transistors 63a-h are also floating gate transistors, *i.e.*, flash memory cells. *See id.* at 8:22-25. Thus, Seligson discloses a row of reference transistors within a larger array of memory cells (the reference transistors within the array of 62a-h and 63a-h).

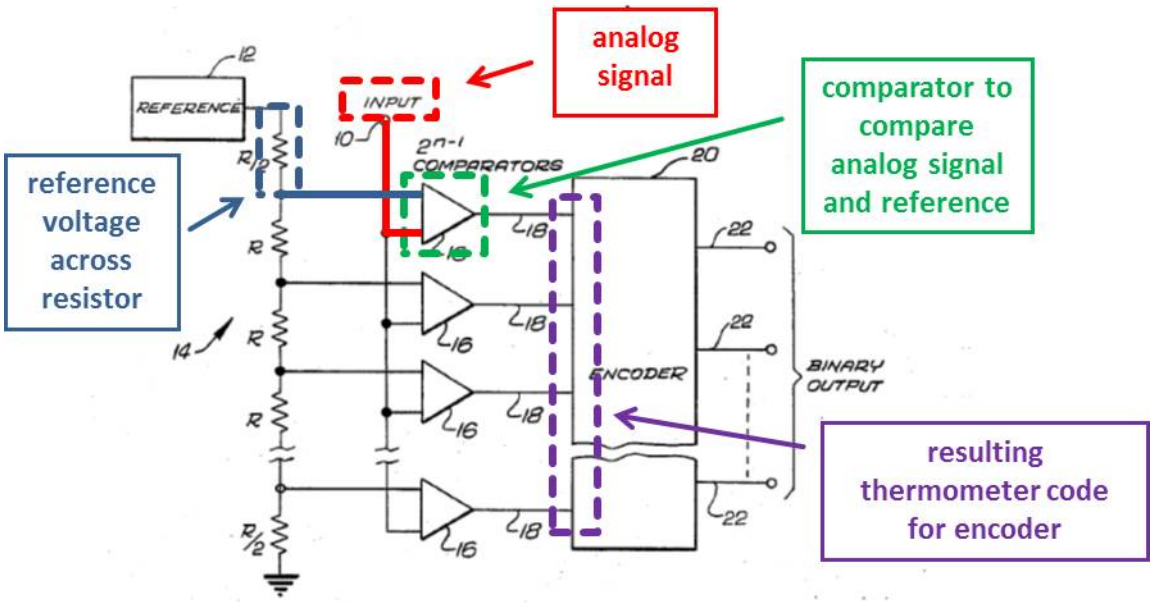
Seligson does not describe decoder 70 in detail. However, given that it encodes thermometer code, it would have been obvious to use the encoding of Bucklen (*see* below), which is relevant to claim 8. Seligson also only describes an exemplary row of reference transistors in Fig. 4. However, it would have been

obvious to extend the concept of using reference transistors for the exemplary row to conventional multi-row arrangements, as in Yonemaru (*see* below), which is relevant to claims 9-10.

8.2. U.S. Patent No. 4,591,825 ("Bucklen")[11]

The relevant portions of Bucklen for the purposes of this Petition relate to its encoding disclosures. Specifically, it discloses the conventional encoding scheme of counting 1s (indicating true comparisons) of the thermometer code until the transition point to encode the result into a binary number. *See* MICRON-1007, Bucklen at 1:7-40. Bucklen discloses an analog-to-digital converter that uses conventional comparators instead of floating gate transistors. *Id.* Nonetheless, the conventional comparators, just like the floating gate transistors, produce a logical value for each level comparison and thus generate thermometer code. This arrangement is shown below:

[11] Bucklen issued on May 27, 1986 and is prior art under 102(b). *See* MICRON-1007, Bucklen.



MICRON-1007, Bucklen at Figure 1 (with annotations).

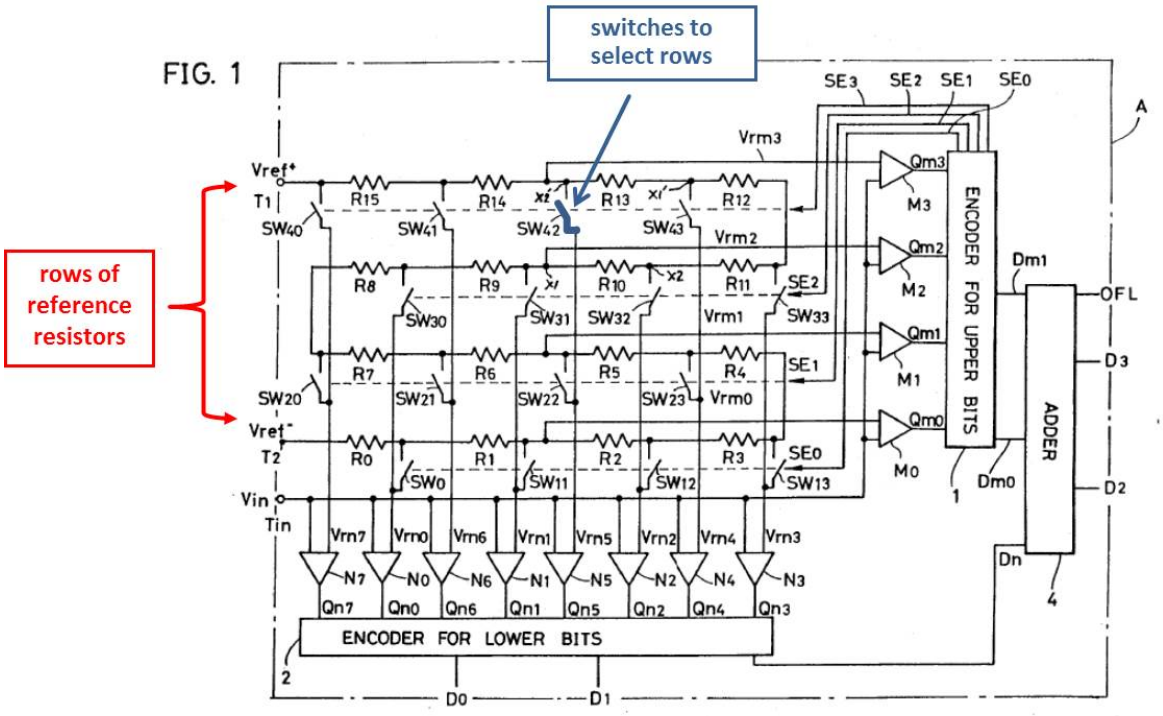
Specifically, Bucklen discloses encoding circuitry that generates a specific value at the transition point of the thermometer code. *See id.* at Fig. 2a; *see also id.* at 3:50-4:30. The encoding circuitry counts the logical outputs until it reaches this transition point and converts this count to binary form via an adder. *See id.* at 1:33-40 (noting implementation of an "adder" to effectuate the "count[ing]" encoding technique); *see also* Fig. 3; 5:17-6:5. In sum, Bucklen discloses an encoder that converts thermometer code to a binary number by counting until the transition point.

8.3. U.S. Patent No. 5,187,483 ("Yonemaru")[12]

The relevant portions of Yonemaru for the purposes of this Petition relate to its disclosure of a multi-row serial-to-parallel converter. This arrangement enables the A/D converter to selectively use different rows of reference components depending on the value of the analog signal. Specifically, this type of A/D converter first determines the higher order digital bits of the analog signal (by generating thermometer code) and then using those bits, it selects particular rows of reference elements (resistors) to decode the lower order digital bits of the analog signal (again by generating thermometer code).[13] This reduces the footprint of the encoder. This arrangement is shown below:

[12] Yonemaru issued on February 16, 1993 and is prior art under 102(b). *See* MICRON-1006, Yonemaru.

[13] It is well known that these encoders generate thermometer code respectively for the lower and upper bit encoders. *See, e.g.*, MICRON-1010, U.S. Pat. No. 5,019,820 ("Matsuzawa") at 3:7-52.



MICRON-1006, Yonemaru at Figure 1 (with annotations).

As shown above, this embodiment first generates thermometer code Qm0-3 (a thermometer value for each comparison) using comparators M0-3. Using these values, the upper bit decoder generates SE0-SE3 signals, which select particular reference rows via the SW switches (and is thus a row decoder). *See id.* at 5:52-6:19. This selects the rows of reference resistors for the lower bit encoder. *See id.* This scheme selects from among rows of reference values (akin to rows of floating gate transistors with different threshold values) to use in the comparing step to generate the thermometer code for the lower order bits.

8.4. Motivations To Combine: Seligson in Combination with Bucklen

A person of ordinary skill in the art would have been motivated to combine Seligson with the encoder teachings of Bucklen for several reasons. *See* MICRON-1003, Baker Decl. ¶¶ 93-96.

First, both are squarely in the same field of A/D converters. *Compare* MICRON-1005, Seligson at Title *with* MICRON-1007, Bucklen at Title; *see also* MICRON-1003, Baker Decl. ¶ 94. Second, the combination of Seligson with the encoder of Bucklen would simply be applying a known technique (the counting thermometer code technique of Bucklen) to yield predictable results. MICRON-1003, Baker Decl. ¶ 95 (citing MICRON-1009, Knierim 238 at 2:33-34; MICRON-1007, Knierim 955 at 1:43-2:22). Third, the encoding teaching of Bucklen was an obvious technique to apply and the combination was common sense because of its simplicity. MICRON-1003, Baker Decl. ¶ 96.

8.5. Motivations To Combine: Seligson in Combination with Yonemaru

A person of ordinary skill in the art would have been motivated to combine Seligson with the multiple row and column arrangement of Yonemaru for several reasons. *See* MICRON-1003, Baker Decl. ¶¶ 97-101.

First, both are squarely in the same field of A/D converters. *Compare* MICRON-1005, Seligson at Title *with* MICRON-1006, Yonemaru at Title; *see also* MICRON-1003, Baker Decl. ¶ 98. Second, one of ordinary skill in the art

would have been motivated to consider well-known architectures such as Yonemaru in combination with Seligson, e.g., to decrease the size of the converter. MICRON-1003, Baker Decl. ¶ 99. Third, the combination is simply arranging the Seligson elements according to a known technique, that is, arranging the reference cells of Seligson into a serial-to-parallel arrangement as in Yonemaru, and the results would have been understood as predictable. MICRON-1003, Baker Decl. ¶ 100. Fourth, for the same reasons as directly above, the combination would have been obvious to try. MICRON-1003, Baker Decl. ¶ 101.

8.6. Motivations To Combine: Seligson in Combination with Bucklen and Yonemaru

A person of ordinary skill in the art would have been motivated to combine Seligson with both Bucklen and Yonemaru for several reasons. *See* MICRON-1003, Baker Decl. ¶¶ 102-03.

The reasons for combining Seligson with both Bucklen and Yonemaru individually are equally applicable to the three-way combination. MICRON-1003, Baker Decl. ¶ 102. Additionally, a person of ordinary skill in the art would have been motivated to combine Yonemaru and Bucklen to apply the known technique of encoding thermometer code with predictable results (i.e., encoding thermometer code of Yonemaru with Bucklen's encoder). MICRON-1003, Baker Decl. ¶ 103.

9. GROUND #1: CLAIM 1 THE 503 PATENT IS UNPATENTABLE AS ANTICIPATED BY SELIGSON

9.1. Claim 1 anticipated by Seligson

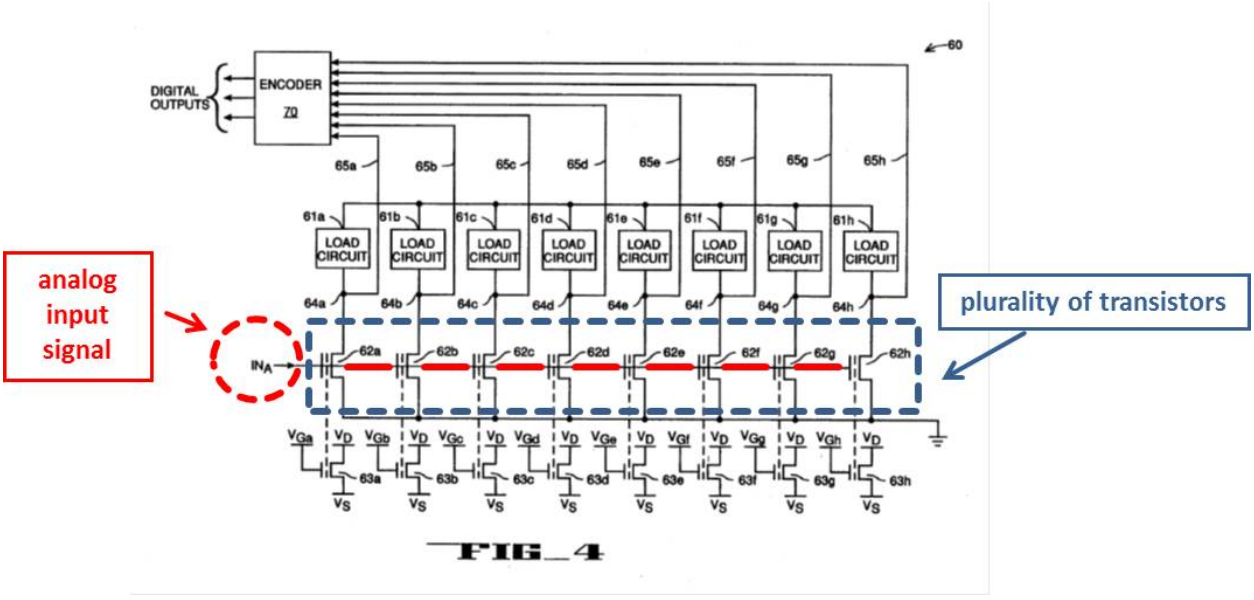
9.1.1. [1.P] "A converter comprising:"

Seligson discloses this limitation. Specifically, Seligson discloses an A/D converter. MICRON-1005, Seligson at Title ("Digital-To-Analog And Analog-To-Digital Converters Using Electrically Programmable Floating Gate Transistors"); *see also id.* at Fig. 4, 3:59-63, 7:16-17 ("an A/D converter 60" of Fig. 4).

Thus, by disclosing A/D converter 60, Seligson discloses a "converter."

9.1.2. [1.1] "a plurality of transistors having a plurality of different threshold voltages;"

Seligson discloses this limitation. First, as shown below, Seligson discloses programmable floating gate transistors 62a through 62h (a plurality of transistors):



MICRON-1005, Seligson at Figure 4 (with annotations).

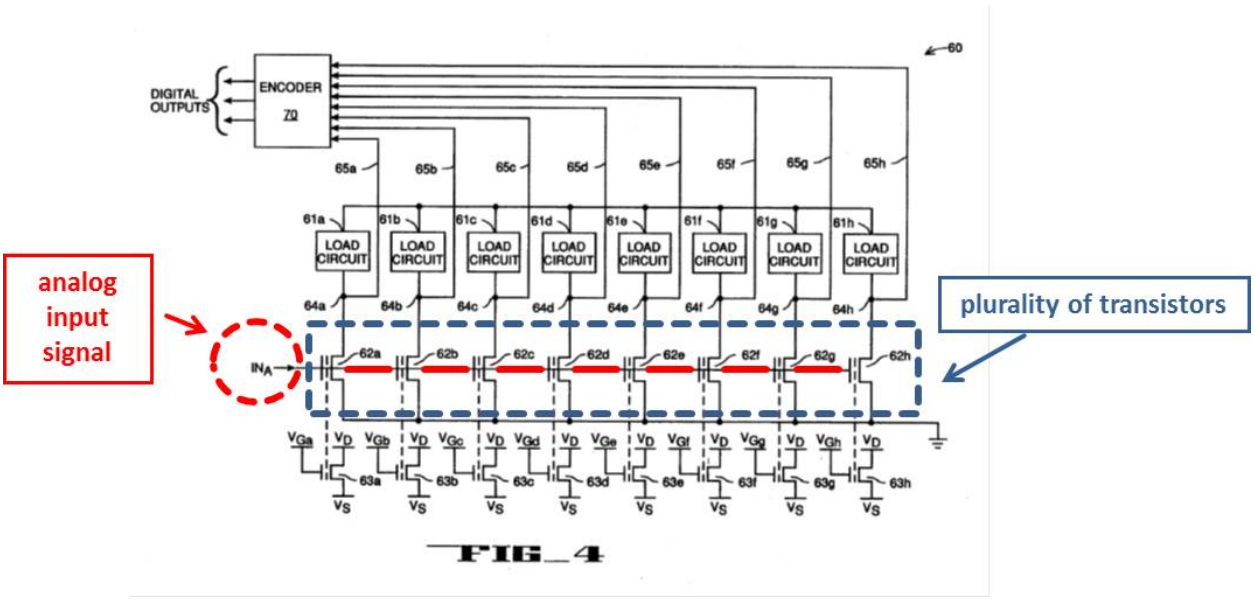
See also id. 7:16-31 (noting that "A/D converter 60 includes **eight electrically erasable and electrically programmable floating gate transistors 62a through 62h, each for one of the eight conversion levels"**).

Second, the pluarity of transistors each has a different threshold voltage that corresponds to a conversion level (a different quantization level that corresponds to a different digital value). *See id.* at 7:48-65 ("Like floating gate transistors 33a-33h of FIG. 3, **each of floating gate transistors 62a-62h has a programmable threshold voltage**. The threshold voltage of each of transistors 62a-62h can be electrically programmed to various voltages and can be electrically erased. … **The threshold voltage of each of transistors 62a-62h differs from that of its adjacent one of transistors 62a-62h by an amount corresponding to the least significant binary bit."**).

Thus, by disclosing transistors 62a-h, each of which has a different threshold voltage that corresponds to a different quantization level and digital value, Seligson discloses a plurality of transistors having a plurality of different threshold voltages.

9.1.3. [1.2] "an input terminal coupled to apply an analog input signal to the gates of the transistors; and"

Seligson discloses this limitation. Specifically, as shown below, the signal IN_A is an analog signal, and it directly connects to the gates of the transistors 62a-h through an input terminal to the A/D converter shown in Fig. 4:



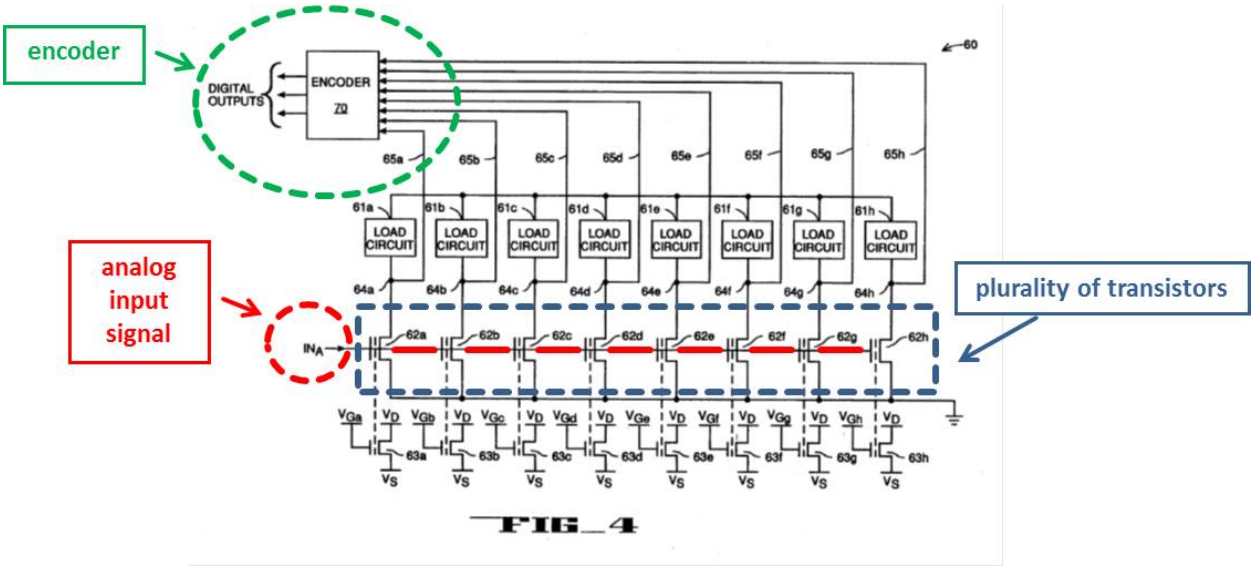
MICRON-1005, Seligson at Figure 4 (with annotations).

As shown above, the analog signal either renders the transistors conductive or not by its coupling to the control gates of transistors 62a-h. *See id.* at 7:66-8:14 (noting that "**[d]uring operation, the input analog voltage IN_A is applied to the control gate of each of transistors 62a-62h**. Depending on the voltage level of the analog voltage IN_A, one or more than one of transistors 62a-62h can be conducting.").

Thus, by disclosing analog signal IN_A, which is fed to the transistors via a terminal that connects to the gates of the plurality of transistors that have different threshold voltages, Seligson discloses an input terminal coupled to apply an analog input signal to the gates of the transistors.

9.1.4. [1.3] "an encoder coupled to the transistors, wherein the encoder generates a multi-bit output signal that represents a value that depends on which of the transistors conduct when the analog signal is applied; and"

Seligson discloses this limitation. First, Seligson discloses an encoder (70) as shown below that is coupled to the transistors via lines 65a-h:



MICRON-1005, Seligson at Figure 4 (with annotations).

See also id. at 7:35-47 (describing that drains of transistors 62a-h connect to the encoder via lines 65a-h).

Second, the encoder (70) (an 8-3 encoder) generates a multi-bit output signal (3 bits) that represents a value that depends on which of the transistors (62a-h) conduct when the analog signal (IN_A) is applied. *See id.* at 7:66-8:21 ("During operation, the input analog voltage IN_A is applied to the control gate of each of transistors 62a-62h. **Depending on the voltage level of the analog voltage IN_A,**

one or more than one of transistors 62a-62h can be conducting. The conducting ones of transistors 62a-62h each then causes the voltage at its output node to be pulled down to ground. … **Encoder 70 encodes the logical signals received from lines 65a-65h into an output binary digital signal.**"). Specifically, this is a three bit binary number, which the encoder generates from the thermometer code. *See id.*; *see also* MICRON-1001, 503 Patent at 5:14-37 (Table 1 Thermometer-to-Binary Encoding).

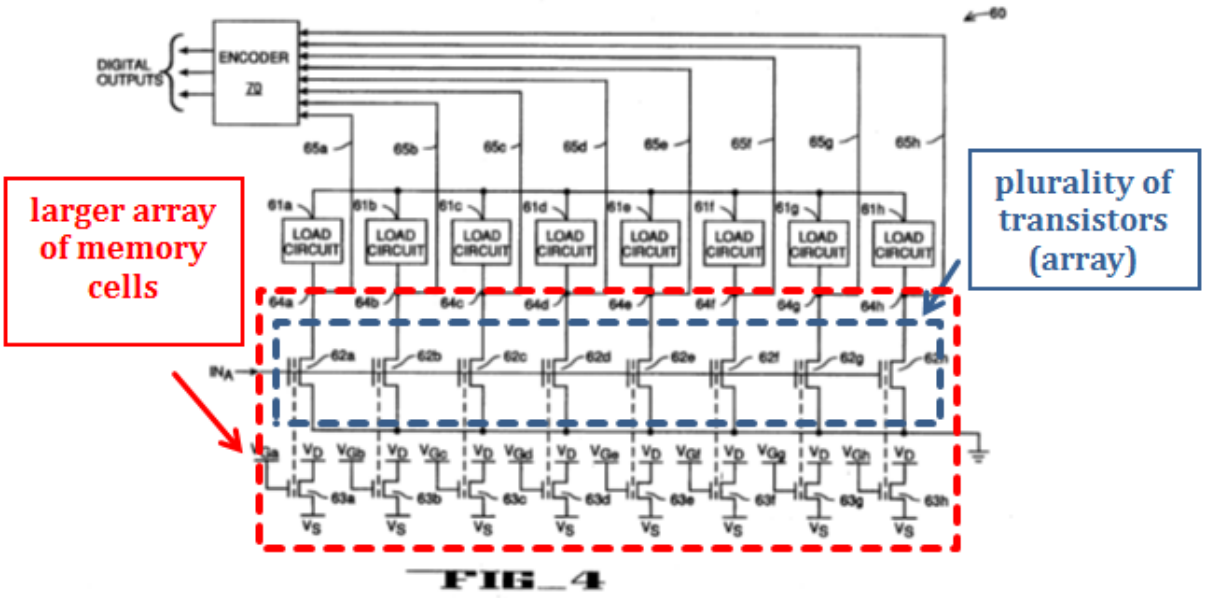
Thus, by disclosing encoder (70), to which the transistors 62a-h connect via lines 65a-h, and which generates a 3-bit binary number from thermometer code via three output signal lines that depend on which of transistors 62a-h the analog signal IN_A renders conductive, Seligson discloses an encoder coupled to the transistors, wherein the encoder generates a multi-bit output signal that represents a value that depends on which of the transistors conduct when the analog signal is applied.

9.1.5. [1.4] "an array of memory cells that contain the plurality of transistors."

Seligson discloses this limitation.

Under the broadest reasonable construction standard, "array" means "two or more elements that form at least one of a row or column." *See* Section 6.2.1 (claim construction section).

As shown below, transistors 62a-h are both an array of memory cells within their own array and within the larger array of memory cells 62a-h and 63a-h:



MICRON-1005, Seligson at Figure 4 (with annotations).

The transistors 62a-h and 63a-h are memory cells, specifically, electrically erasable and electrically programmable cells. *See id.* at 6:57-7:7, 7:22-44, 8:22-25; *see also id.* at 4:19-32, 4:33-59 (programming and erasing with standard hot electron injection flash programming); *see also id.* MICRON-1003, Baker Decl. ¶¶ 74-77. Further, Seligson discloses an "array" of reference "(MOS) transistors" in its background section, and thus transistors 62a-h could likewise be within this "array." *See id.* at 1:33-53.

Thus, by disclosing programmable transistors 62a-h (flash memory cells) (as well as an "array" of reference cells), and in addition that these are within the larger matrix of 62a-h and 63a-h, Seligson discloses an array of memory cells that contain the plurality of transistors.

10. GROUND #2: CLAIM 1 THE 503 PATENT IS UNPATENTABLE AS BEING OBVIOUS OVER SELIGSON IN VIEW OF YONEMARU

10.1. Claim 1 is obvious over Seligson in view of Yonemaru

10.1.1. [1.P] "A converter comprising:"

Seligson discloses this limitation. *See* analysis for Claim [1.P], Ground 1, Section 9.1.1.[14]

10.1.2. [1.1] "a plurality of transistors having a plurality of different threshold voltages;"

Seligson discloses this limitation. *See* analysis for Claim [1.1], Ground 1, Section 9.1.2.

10.1.3. [1.2] "an input terminal coupled to apply an analog input signal to the gates of the transistors; and"

Seligson discloses this limitation. *See* analysis for Claim [1.2], Ground 1, Section 9.1.3.

10.1.4. [1.3] "an encoder coupled to the transistors, wherein the encoder generates a multi-bit output signal that represents a value that depends on which of the transistors conduct when the analog signal is applied; and"

Seligson discloses this limitation. *See* analysis for Claim [1.3], Ground 1, Section 9.1.4.

[14] The Petition will note <u>if</u> there are any differences in claim language when referring back to earlier analysis.

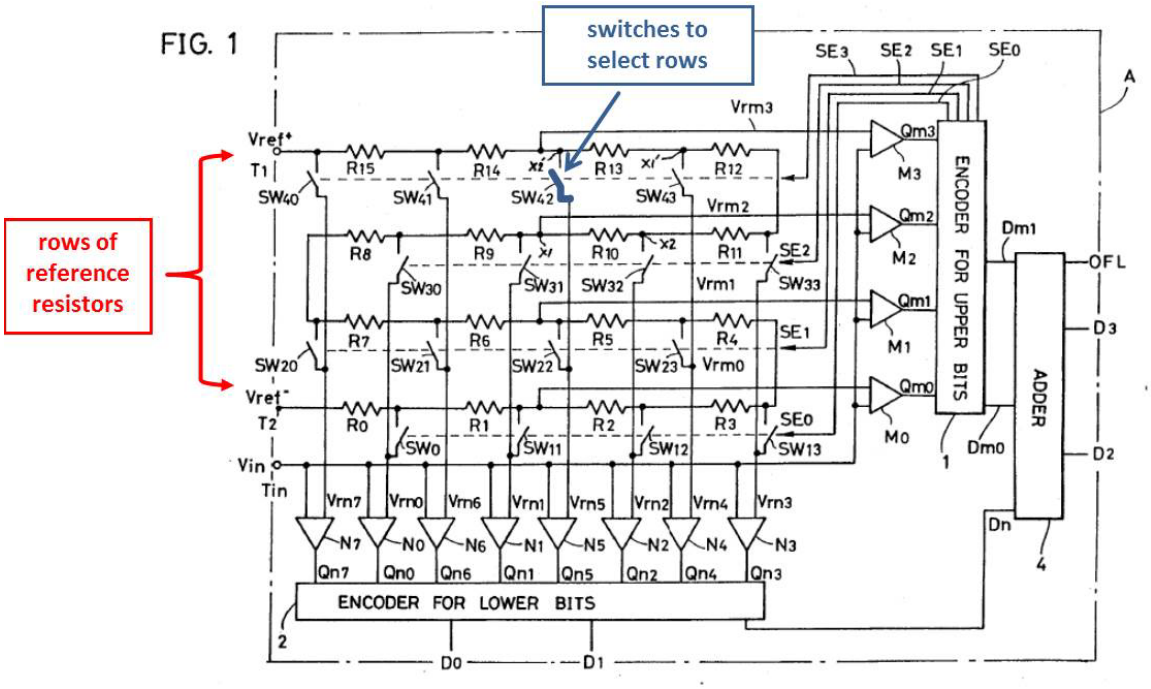
10.1.5. [1.4] "an array of memory cells that contain the plurality of transistors."

Seligson in view of Yonemaru discloses this limitation.

Under the broadest reasonable construction standard, the plain and ordinary meaning of "array" means "two or more elements that form at least one of a row or column." *See* Section 6.2.1 (claim construction section). The below analysis, however, assumes that "array" means at least two of either rows or columns.

Note that Seligson discloses only an exemplary row of reference cells in its array as shown in Fig. 4. *See* MICRON-1005, Seligson at Fig. 4, 7:16-31, 7:48-65; *see also* Claim [1.4], Ground 1, Section 9.1.5. However, Seligson discloses an "array" of reference "(MOS) transistors" in its background section, and thus it would have been obvious to include multiple rows within Fig. 4. *See id.* at 1:33-53. Further, in view of Yonemaru it would have been obvious to include multiple rows of reference cells in Seligson to convert different ranges of analog values.

Yonemaru discloses multiple rows of reference cells in an array:



MICRON-1006, Yonemaru at Figure 1 (with annotations).

Yonemaru discloses an analog-to-digital converter with two stages (one for the lower and one for the upper bits). MICRON-1006, Yonemaru at 5:52-57. The "matrix" of reference resistors provide a reference for comparing the analog signal Vin to selected rows of reference cells (which then have a voltage across them). The SW switches select rows within the resistor array depending on the value of the upper bits, *i.e.*, depending on the range of the analog signal. *See id.* at 5:52-6:37 (noting "[r]esistors R0-R15 are provided in a matrix on a semiconductor substrate A. **Resistors R0-R3 form a row of resistance, R4-R7 forms another row, R8-R11 forms still another row, and R12-R15 form a further row.** …

Encoder 1 … generates signals SE0-SE3 for selecting resistances for generating reference voltages for the lower bits.").

Yonemaru teaches that the purpose of multiple rows is to provide for conversion of different ranges of analog values (which the upper bit decoding identifies). *See id.* at 6:20-37. It would have been obvious in light of Yonemaru to add additional rows to the exemplary row within the Seligson array to likewise sense different ranges of analog values. *See* Section 8.5 (obviousness discussion of Seligson in view of Yonemaru). This would result in a multi-row arrangement of the floating gate transistors, *i.e.*, memory cells, and hence an array of memory cells that contain the first plurality of transistors (a row within that array). *See* Claims [1.1] and [1.4], Ground 1, Section 9.1.2, 9.1.5. ("first plurality of transistors" of Seligson that are memory cells).

Thus, by Yonemaru disclosing multiple rows within a reference array and teaching each row corresponds to a different sensing range, and by Seligson disclosing an exemplary row of reference memory cells (transistors 62a-h) each of which has a different threshold voltage, Seligson in view of Yonemaru discloses an array of memory cells that contain the plurality of transistors.

11. GROUND #3: CLAIM 8 THE 503 PATENT IS UNPATENTABLE AS BEING OBVIOUS OVER SELIGSON IN VIEW OF BUCKLEN

11.1. Claim 8 is obvious over Seligson in view of Bucklen

11.1.1. [8.P] "A converter comprising"

Seligson discloses this limitation. *See* analysis for Claim [1.P], Ground 1, Section 9.1.1.

11.1.2. [8.1] "an array of reference cells, the reference cells having a plurality of threshold voltages;"

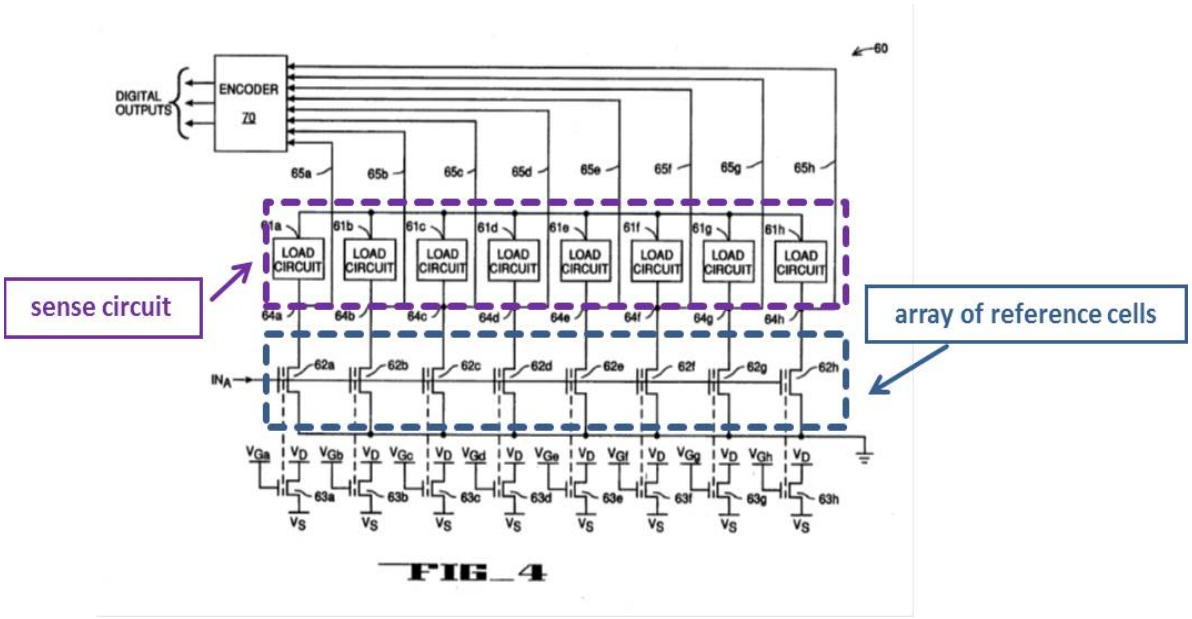
Under the broadest reasonable construction standard, "array" means "two or more elements that form at least one of a row or column." *See* Section 6.2.1 (claim construction section).

Seligson discloses this limitation. *See* analysis for Claim [1.1], Section 9.1.2, Ground 1. This element differs with respect to claim element [1.1] only in that it refers to "array of reference cells" instead of "plurality of transistors." The 503 Patent uses "reference cells" to include the subset of floating gate transistors that are references for the analog signal. *See, e.g.*, MICRON-1001, 503 Patent at Fig. 3, 4:20-31 (using "reference cells RC0 to RCx with respective threshold voltages VT0 to VTx" to include embodiment with "floating gate transistor[s]"); *see also id.*at 4:14-19 (noting that reference cells and memory cells can be the same structure). And under the above construction of "array," a plurality of transistors satisfies "array." *See id.* at Fig. 4. Thus, by disclosing floating gate

transistors 62a-h that have different threshold voltages, Seligson discloses an array of reference cells, the reference cells having a plurality of threshold voltages.

11.1.3. [8.2] "a sense circuit coupled to the array; and"

Seligson discloses this limitation. Specifically, Seligson discloses Load Circuits 61a-h (the sense circuit) that directly connect to the array:



MICRON-1005, Seligson at Figure 4 (with annotations).

The sense circuit of Seligson enables the encoder to determine and sense whether the transistors 62a-h are conductive during application of the analog voltage (IN_A). The Load Circuits include a resistor or constant-on load transistor to bias lines 65a-h, thereby enabling transistors 62a-h to either pull down the voltage or leave it high depending on their conducive states. *See* MICRON-1005, Seligson at 7:44-47 ("For one embodiment, each of **load circuits 61a-61h includes a resister**. For another embodiment, each of **load circuits 61a-61h**

includes a constant-on load transistor."); *see also id. at* 7:66-8:14 (describing pull-up or pull-down sensing mechanism).

Thus, by Seligson disclosing Load Circuits to pull-up or pull-down lines 65a-h according to whether transistors 62a-h are conductive or not, which in turn the encoder uses for encoding, Seligson discloses a sense circuit coupled to the array.

11.1.4. [8.3A] "an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct when an analog input signal is applied to a set of reference cells,"

Seligson discloses this limitation. *See* analysis for Claim [1.3], Ground 1, Section 9.1.4. Note that the only difference relative to claim element [1.3] is that this element states that (a) the encoder is coupled to the sense circuit instead of the floating gate transistors, (b) the encoder generates a digital output signal, and (c) the encoder uses "reference cells" instead of "transistors." First, as shown in Fig. 4 of Seligson, the sense circuit of Seligson (Load Circuits 61a-h) directly couples to the encoder (70) via lines 65a-h. *See* MICRON-1005, Seligson at Fig. 4. Second, the multi-bit output signal in Seligson is a digital signal. *See id.* at 7:66-8:21 ("Encoder 70 encodes the logical signals received from lines 65a-65h into **an output binary digital signal**."). Finally, as described above (Claim [8.1]), the

floating gates transistors 62a-h of Seligson are both the first plurality of transistors (Claim 1) and reference cells (Claim 8).

11.1.5. [8.3B] "wherein the encoder comprises a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference cells that conduct."

Seligson in view of Bucklen discloses this limitation.

Under the broadest reasonable construction standard, "a counter coupled to count pulses from the sense circuit" means "a counter that counts changes in current or voltage from a circuit that indicates if a given reference cell is conducting." *See* Section 6.2.2 (claim construction section).

Note that Seligson discloses that encoder 70 is an eight-to-three encoder for encoding the 8-bit thermometer code signals from the reference cells into a binary number. *See id.* at 7:35-47. Seligson, however, does not expressly disclose the specific manner of encoding the thermometer code to the binary number. It would have been obvious to one of ordinary skill in the art, however, to use traditional encoding techniques for thermometer code such as the conventional encoding in Bucklen. *See* Section 8.4 (obvious section on combining Seligson and Bucklen).

Specifically, Bucklen discloses using an "adder" to "count" the number of conductive comparators (pulses from the sense circuit that are the thermometer code) and convert the code to the binary digital number for output. *See* MICRON-1007, Bucklen at 1:7-40. ("For this reason, the output code is sometimes referred

to as a **thermometer code**. The desired **digital output can be obtained as the sum of the individual comparator outputs**. … **Implementation of an adder to count** the number of 'one' comparator outputs is not a simple matter, however, and virtually all higher-resolution parallel analog-to-digital converters built today rely on the detection of a single one-to-zero transition in the array of comparator outputs. Once the transition is located, it is converted to a desired digital code in a read-only memory circuit.").[15]

Bucklen discloses circuits in detail that detect the transition point between conductive and non-conductive cells, that count the pulses until the transition point, and then that generate the multi-bit digital output via an adder from this count. *See id.* at 1:7-40 (describing "counter" and "adder"), *id.* at Fig. 2a, 3:50-4:56 (circuitry to detect boundary), *id.* at 5:17-6:5 and Fig. 3 (adder to count and latch the multi-digital output count).

[15] Note that Bucklen refers to the adding as not a simple matter because certain errors can result from faulty transitions (e.g., if there is transition because of faulty comparison), and therefore teaches techniques to improve this issue. *See id.* at 1:40-55; 5:6-16. This was, therefore, not a difficult technique to implement to a person of ordinary skill in the art. *See* MICRON-1003, Baker Decl. ¶¶ 84-88.

As Seligson produces this same thermometer code (comparator or reference outputs), it would have been obvious to apply Bucklen's encoding technique to Seligson, wherein the count would be of reference cells that are conductive, and the count would stop when the cells become non-conductive (the boundary or transition point in the thermometer code). *See id.* at 5:17-6:5; *see also* Section 8.4 (motivations to combine).

Thus, by Bucklen disclosing an encoder that counts pulses from the sense circuit (outputs from AND gates 26) to generate a multibit digital output signal which is thermometer code, and Seligson disclosing an encoder that also accepts thermometer code based on whether reference cells conduct (pulses), Seligson in view of Bucklen discloses wherein the encoder comprises a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference cells that conduct.

12. GROUND #4: CLAIM 8 THE 503 PATENT IS UNPATENTABLE AS BEING OBVIOUS OVER SELIGSON IN VIEW OF BUCKLEN AND YONEMARU

12.1. Claim 8 is obvious over Seligson in view of Bucklen and Yonemaru

12.1.1. [8.P] "A converter comprising"

Seligson discloses this limitation. *See* analysis for Claim [1.P], Ground 1, Section 9.1.1.

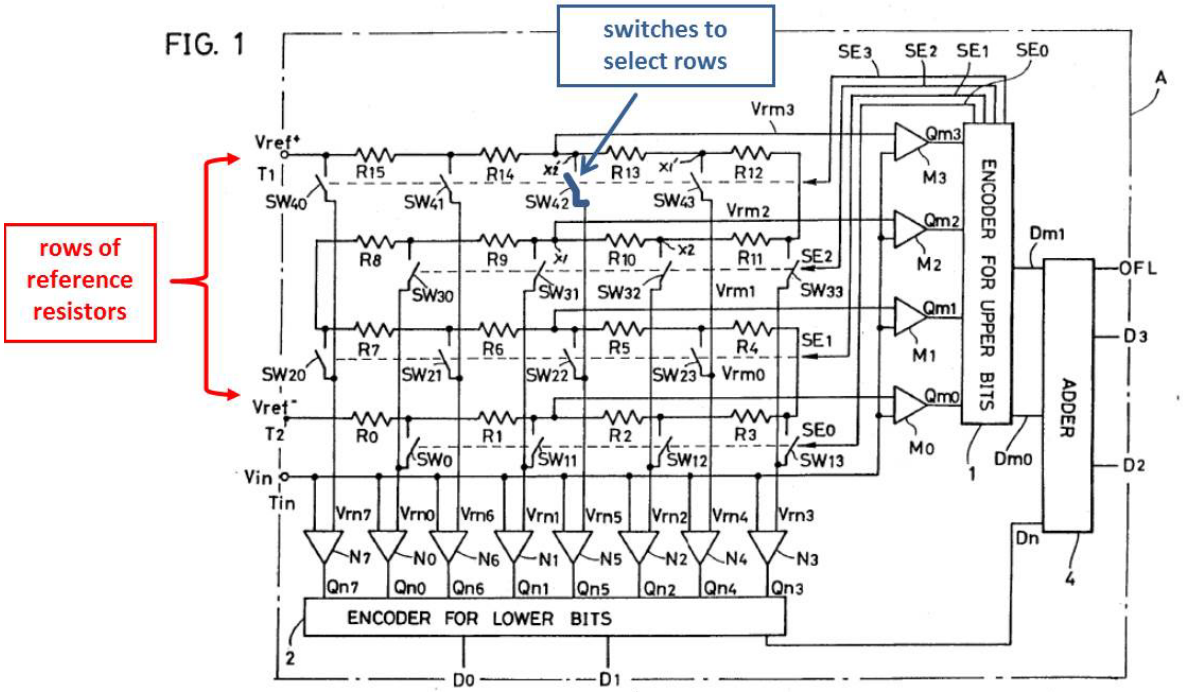
12.1.2. [8.1] "an array of reference cells, the reference cells having a plurality of threshold voltages;"

Under the broadest reasonable construction standard, "array" means "two or more elements that form at least one of a row or column." *See* Section 6.2.1 (claim construction section). The below analysis, however, assumes that "array" means at least two of either rows or columns.

Note that the only difference between this limitation in Ground 4 with respect to Ground 3 is the alternative construction of "array." Thus, the analysis is otherwise the same, *see* Claim [8.1], Ground 3, Section 11.1.2, except for whether Seligson discloses at least two of either rows or columns of reference cells.

Note that Seligson discloses only an exemplary row of references cells in its array as shown in Fig. 4. *See* MICRON-1005, Seligson at Fig. 4, 7:16-31, 7:48-65; *see also* Claim [1.4], Ground 2, Section 10.1.5. However, Seligson discloses an "array" of reference "(MOS) transistors" in its background section, and thus it would have been obvious to include multiple rows within Fig. 4. *See id.* at 1:33-53.

Further, in view of Yonemaru it would have been obvious to include multiple rows of reference cells in Seligson to convert different ranges of analog values. Yonemaru discloses multiple rows of reference cells in an array:



MICRON-1006, Yonemaru at Figure 1 (with annotations).

Yonemaru discloses an analog-to-digital converter with two stages (one for the lower and one for the upper bits). *See* MICRON-1006, Yonemaru at 5:52-57. The "matrix" of reference resistors provide a reference for comparing the analog signal Vin to selective rows of reference (which then have a voltage across them). The SW switches select rows within the resistor array depending on the value of the upper bits, *i.e.*, depending on the range of the analog signal. *See id.* at 5:52-6:37 (noting "[r]esistors R0-R15 are provided in a matrix on a semiconductor substrate A. **Resistors R0-R3 form a row of resistance, R4-R7 forms another row, R8-R11 forms still another row, and R12-R15 form a further row.** … Encoder 1 … generates signals SE0-SE3 for selecting resistances for generating reference voltages for the lower bits.").

Yonemaru teaches that the purpose of multiple rows is to provide for conversion of different ranges of analog values (which the upper bit decoding identifies). *See id.* at 6:20-37. It would have been obvious in light of Yonemaru to add additional rows of the exemplary row within the Seligson array to likewise sense different ranges of analog values. *See* Section 8.5 (motivations to combine Seligson with Yonemaru). This would result in a multi-row arrangement of the floating gate transistors, *i.e.*, memory cells, and hence an array of memory cells that contain the first plurality of memory cells (a row within that array). *See* Claim [1.1] and [1.4], Ground 1, Sections 9.1.2 and 9.1.5. ("first plurality of transistors" of Seligson that are memory cells).

Thus, by Yonemaru disclosing multiple rows within a reference array and teaching each row corresponds to a different sensing range, and by Seligson disclosing an exemplary row of reference cells (transistors 62a-h) each of which has a different threshold voltage, Seligson in view of Yonemaru discloses an array of reference cells, the reference cells having a plurality of threshold voltages.

12.1.3. [8.2] "a sense circuit coupled to the array; and"

Seligson discloses this limitation. *See* analysis for Claim [8.2], Ground 3, Section 11.1.3.

12.1.4. [8.3A] "an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct when an analog input signal is applied to a set of reference cells,"

Seligson discloses this limitation. *See* analysis for Claim [8.3A], Ground 3, Section 11.1.4.

12.1.5. [8.3B] "wherein the encoder comprises a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference calls that conduct."

Seligson in view of Bucklen discloses this limitation. *See* analysis for Claim [8.3B], Ground 3, Section 11.1.5.

13. GROUND #5: CLAIMS 9-10 OF THE 503 PATENT ARE UNPATENTABLE AS BEING OBVIOUS OVER SELIGSON IN VIEW OF YONEMARU

13.1. Claim 9 is obvious over Seligson in view of Yonemaru

13.1.1. [9.P] "A converter comprising:"

Seligson discloses a converter. *See* analysis for Claim [1.P], Ground 1, Section 9.1.1.

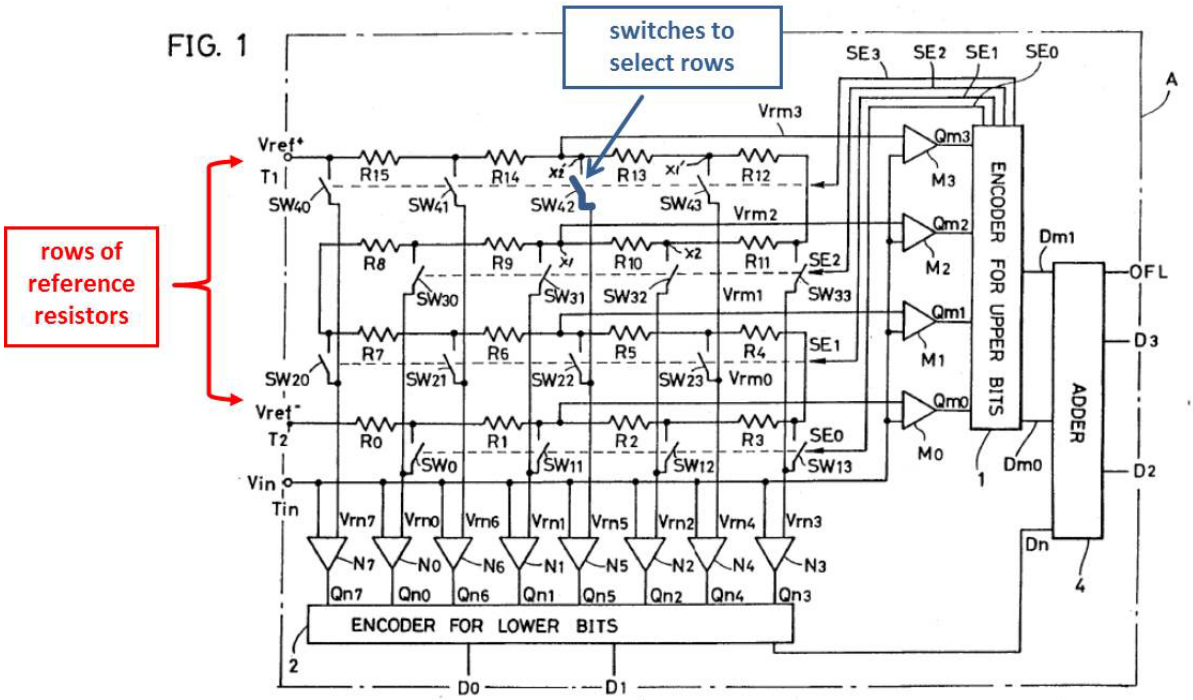
13.1.2. [9.1] "an array of reference cells, the reference cells having a plurality of threshold voltages, wherein the array contains a plurality of rows;"

Seligson in view of Yonemaru discloses this limitation. *See* analysis for Claim [8.1], Ground 3, Section 11.1.2. This element only differs with respect to claim element [8.1] in that it also recites a "wherein the array contains a plurality

of rows." Recall that Seligson discloses an exemplary row of reference cells that have different threshold voltages as shown in Fig. 4. *See* MICRON-1005, Seligson at Fig. 4, 7:16-31, 7:48-65; *see also* Claim [1.4], Ground 2, Section 10.1.5. However, Seligson discloses an "array" of reference "(MOS) transistors" in its background section, and thus it would have been obvious to include multiple rows within Fig. 4. *See id.* at 1:33-53.

Further, in view of Yonemaru it would have been obvious to include multiple rows of reference cells in Seligson to convert different ranges of analog values.

Yonemaru discloses multiple rows of reference cells in an array:



MICRON-1006, Yonemaru at Figure 1 (with annotations).

Yonemaru discloses an analog-to-digital converter with two stages (one for the lower and one for the upper bits). MICRON-1006, Yonemaru at 5:52-57. The "matrix" of reference resistors provide a reference for comparing the analog signal Vin to selective rows of reference (which then have a voltage across them). The SW switches select rows within the resistor array depending on the value of the upper bits, *i.e.*, depending on the range of the analog signal. *See id.* at 5:52-6:37 (noting "[r]esistors R0-R15 are provided in a matrix on a semiconductor substrate A. **Resistors R0-R3 form a row of resistance, R4-R7 forms another row, R8-R11 forms still another row, and R12-R15 form a further row.** … Encoder 1 … generates signals SE0-SE3 for selecting resistances for generating reference voltages for the lower bits.").

Yonemaru teaches that the purpose of multiple rows is to provide for conversion of different ranges of analog values (which the upper bit decoding identifies). *See id.* at 6:20-37. It would have been obvious in light of Yonemaru to add additional rows of the exemplary row within the Seligson array to likewise sense different ranges of analog values. *See* Section 8.5 (motivations to combine Seligson with Yonemaru). This would result in a multi-row arrangement of the floating gate transistors, *i.e.*, memory cells, and hence an array of memory cells that contain the first plurality of memory cells (a row within that array). *See* Claim

[1.1] and [1.4], Ground 1, Sections 9.1.2 and 9.1.5. ("first plurality of transistors" of Seligson that are memory cells).

Thus, by Yonemaru disclosing multiple rows within a reference array and teaching each row corresponds to a different sensing range, and by Seligson disclosing an exemplary row of reference cells (transistors 62a-h) each of which has a different threshold voltage, Seligson in view of Yonemaru discloses an array of reference cells, the reference cells having a plurality of threshold voltages.

13.1.3. [9.2] "a sense circuit coupled to the array; and"

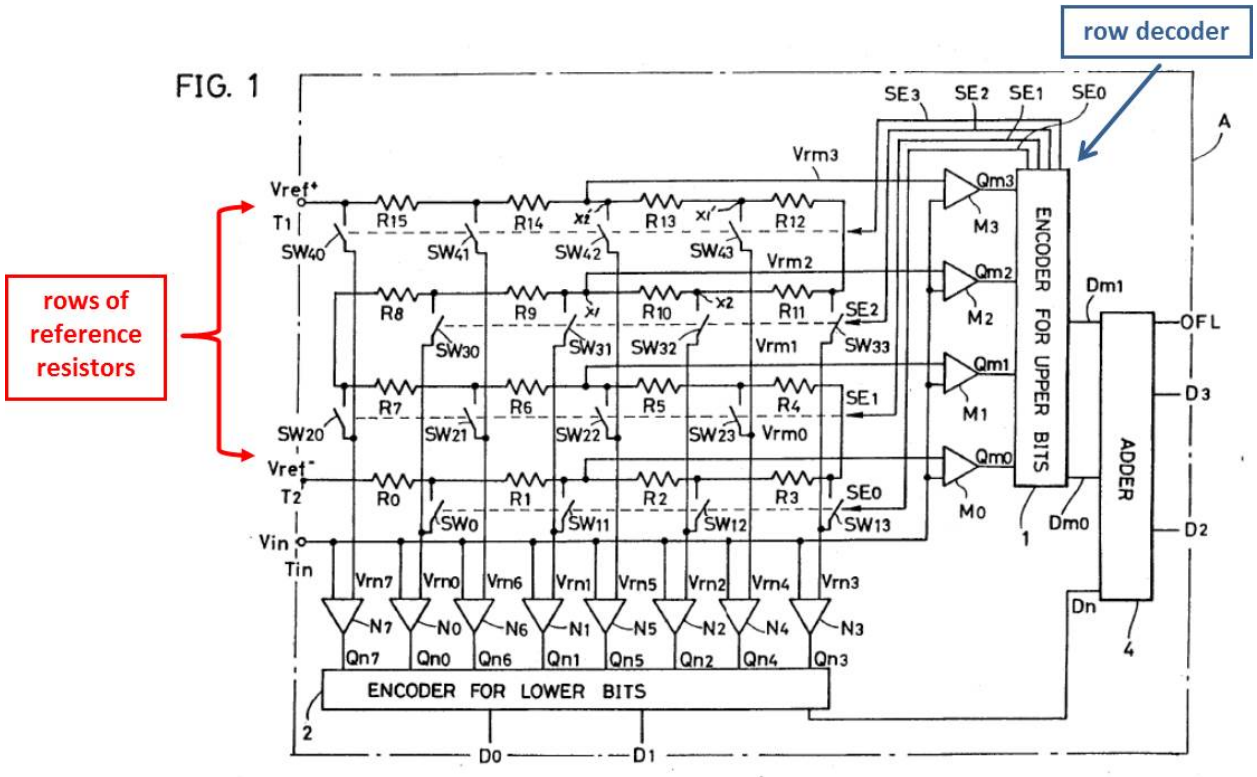
Seligson discloses this limitation. *See* analysis for Claim [8.2.], Ground 3, Section 11.1.3. Note that the only difference with respect to claim element 1.3 is that this element recites "reference cells" instead of "transistors." As described above in Claim [8.1], Ground 3, Section 11.1.2, the floating gates transistors 62a-h of Seligson are both the first plurality of transistors (Claim 1) and reference cells (Claim 9). Therefore, the analysis for Claim [8.2.], Ground 3, Section 11.1.3 is equally applicable here.

13.1.4. [9.3] "an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct when an analog input signal is applied to a set of reference cells; and"

Seligson discloses this limitation. *See* analysis for Claim [8.3A], Ground 3, Section 11.1.4.

13.1.5. [9.4] "a row decoder coupled to the array, the row decoder selecting a row of reference cells to which the analog signal is applied."

Seligson in view of Yonemaru discloses this limitation. Specifically, as shown below, Yonemaru discloses multiple rows of reference cells in an array and a row decoder to select the appropriate row:



MICRON-1006, Yonemaru at Figure 1 (with annotations).

The encoder for the upper bits is a row decoder, *i.e.*, the encoder generates address signals SE0-3, which via the SW switches, select rows within the resistor array depending on the value of the upper bits. In other words, the encoder decodes the appropriate row(s) to activate via the upper bits, and activates it with

the SW switches. *See* MICRON-1006, Yonemaru at 5:52-6:37 (noting "**[e]ncoder 1** … **generates signals SE0-SE3 for selecting resistances for generating reference voltages for the lower bits**. The signals SE0-SE3 are supplied to switches SW10-SW13, SW20-SW23, SW30-SW33 and SW40-SW43, respectively. … The encoder 1 for the upper bits determines based on the results of comparison Qm0-Qm3 of voltage comparators M0-M3, to which range of LSB of the upper bits the level of the analog input signal belongs. **The encoder 1 generates selecting signals SE0-SE3 to select two rows of resistances in the range of the aforementioned range +-1/2 LSB, and provides digital outputs Dm0 and Dm1**.").

Applying this teaching to Seligson, Seligson would include multiple rows of the exemplary row of reference cells shown in Fig. 4 of Seligson, and the encoder and switches of Yonemaru would connect the respective row to the analog signal (the gates of the transistors in that row to the analog signal) depending on the range of the analog signal. It would have been obvious to combine Seligson and Yonemaru so that Seligson could sense multiple analog ranges. *See* Section 8.5 (motivations to combine).

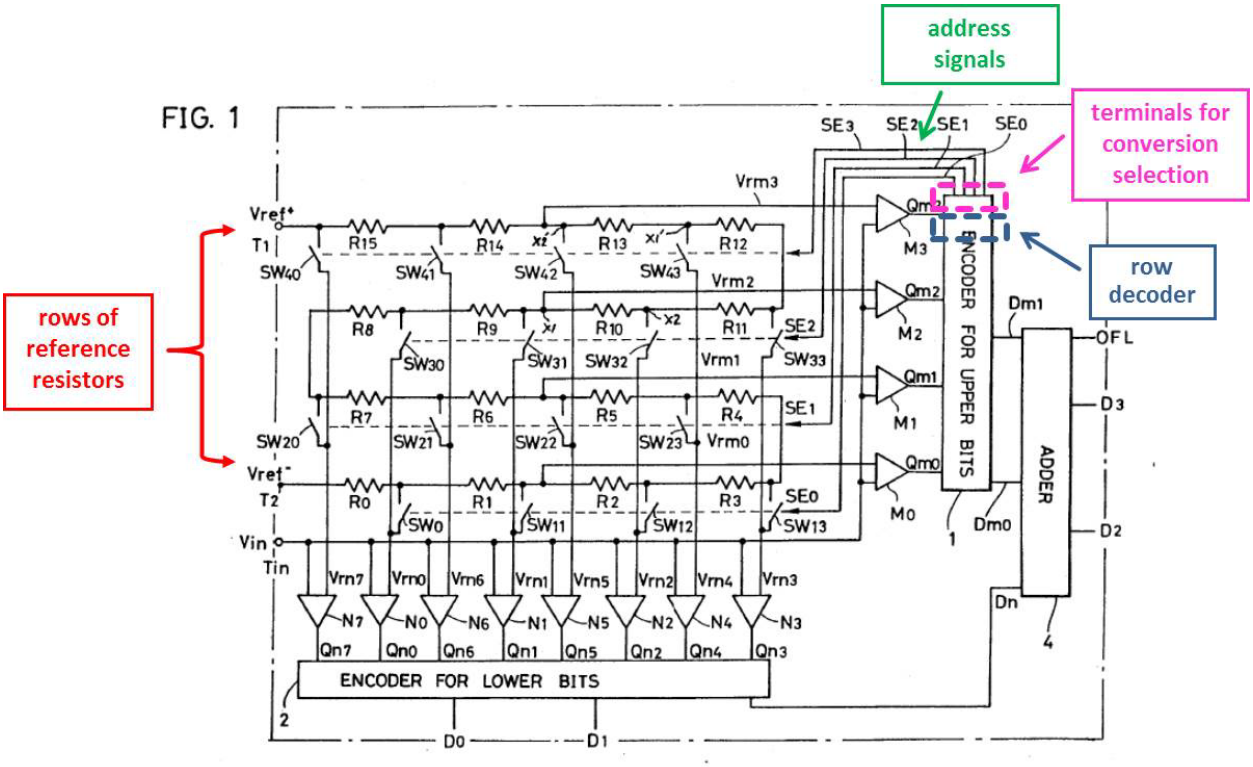
Thus, by Yonemaru disclosing row decoder (the encoder that generates the SE signals for the SW switches), which connects a respective row to the analog-to-digital path, and by Seligson disclosing a row of reference cells that accept the

analog signal on their gates, Seligson in view of Yonemaru discloses a row decoder coupled to the array, the row decoder selecting a row of reference cells to which the analog signal is applied.

13.2. Claim 10 is obvious over Seligson in view of Yonemaru

13.2.1. [10.0] "The converter of claim 9, further comprising a terminal for a conversion select signal that selects from among a plurality of conversions that the converter implements, the terminal being coupled to provide at least a portion of an address signal to the row decoder."

Seligson in view of Yonemaru discloses this limitation. First, as shown below, the terminals of Yonemaru for a conversion select signal are the output terminals of the encoder for the most significant bits:



MICRON-1006, Yonemaru at Figure 1 (with annotations).

S*ee also* MICRON-1006, Yonemaru at 5:53-6:37.

Second, the terminals in Yonemaru include a binary addressing system, wherein the SE0-3 signals (addresses) directly connect to the row decoder switches to connect the appropriate row(s) depending on their logical state. *See id.* at 6:20-37 (noting that "[t]he encoder 1 generates selecting signals SE0-SE3 to select two rows of resistances in the range of the aforementioned range +- 1/2 LSB ….").

Third, the terminals select from the range of LSB conversions (a plurality of conversions) that the converter implements. *See id.*

Thus, by Yonemaru disclosing terminals on the first encoder (for upper bits) for outputting the address signals SE0-3 to select a conversion for the LSB bits, Yonemaru discloses a terminal for a conversion select signal that selects from among a plurality of conversions that the converter implements, the terminal being coupled to provide at least a portion of an address signal to the row decoder.

14. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1, 8, 9, and 10 of the 503 Patent is requested.

Respectfully submitted

Dated: December 14, 2015

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	December 14, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 6,169,503 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1016
Persons served	Patent Owner's Address of Record: Davis Wright Tremaine LLP IP Docketing Dept. 1201 Third Avenue, Suite 2200 Seattle WA 98101 Additional Addresses Known as Likely to Effect Service: Brian E. Farnan Farnan LLP 919 North Market Street, 12th Floor Wilmington, DE 19801 bfarnan@farnanlaw.com Edward C. Flynn Cohen & Grace, LLC 105 Braunlich Drive, Suite 300 Pittsburgh, PA 15237 eflynn@cohengrace.com

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