UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

_____

Case IPR. No. **Unassigned**
U.S. Patent No. 6,697,296
Title: CLOCK SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE

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Petition For *Inter Partes* Review of U.S. Patent No. 6,697,296 Under 35 U.S.C §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

***Mail Stop* "PATENT BOARD"**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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Micron Exhibit #	*Description*
MICRON-1001	U.S. Patent No. 6,697,296 (“the 296 Patent”)
MICRON-1002	File History for U.S. Patent No. 6,697,296
MICRON-1003	Declaration of Dr. R. Jacob Baker (“Baker Decl.”)
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 6,023,175 (“Nunomiya”)
MICRON-1006	U.S. Patent No. 6,339,344 (“Sakata”)
MICRON-1007	U.S. Patent No. 5,848,014 (“Yukshing”)

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1, 11, 12, and 17-20 of United States Patent No. 6,697,296 titled "Clock Synchronous Semiconductor Memory Device" (MICRON-1001, "the 296 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 296 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 296 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang (Reg. No. 73604) (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Justin L. Constant (Reg. No. 66883) (justin.constant@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5217; F: 713-224-9511

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for the Petitioner is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Limestone has asserted the 296 Patent and U.S. Patent Nos. 5,805,504 ("the 504 Patent"), 5,894,441 ("the 441 Patent"), 5,943,260 ("the 260 Patent"), and 6,233,181 ("the 181 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Limestone Memory Sys. LLC v. Micron Tech. Inc.*, 8:15-cv-00278 (C.D. Cal.) ("Co-Pending Litigation"). Limestone has also asserted one or more of the asserted patents in the following actions: *Limestone Memory Sys. LLC v. OCZ Storage Solutions, Inc.*, 8:15-cv-00658 (C.D. Cal.) (the 504, 441, 181 and 296 Patents); *Limestone Memory Sys. LLC v. PNY Techs., Inc.*, 8:15-cv-00656 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Lenovo (US) Inc.*, 8:15-cv-00650 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Kingston Tech. Co. Inc.*, 8:15-cv-00654 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Transcend Info.*,

Inc. (California), 8:15-cv-00657 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Acer America Corp.*, 8:15-cv-00653 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Dell Inc.*, 8:15-cv-00648 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Hewlett-Packard Co.*, 8:15-cv-00652 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); and *Limestone Memory Sys. LLC v. Apple Inc.*, 8:15-cv-01274 (C.D. Cal.) (the 504, 441, 181, and 296 Patents).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 5,805,504, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 5,894,441, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 5,943,260, IPR2015-Unassigned (to be filed concurrently); and Petition for *Inter Partes* Review of U.S. Patent No. 6,233,181, IPR2015-Unassigned (to be filed concurrently).

The 296 Patent claims priority to foreign patent application JP-2001-178286 filed on June 13, 2001. The 296 Patent also claims priority to Provisional U.S. Pat. No. 2002/0191480 A1 filed on December 19, 2002.

2.5. Fee for Inter Partes Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. No. 506499.

2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 296 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Ground #1: Claims 1 and 11 of the 296 Patent are invalid under (pre-AIA) 35 U.S.C. § 102 (b) on the ground that they are anticipated by United States Patent No. 6,023,175, to Nunomiya et al., entitled "Level Interface Circuit," filed with the USPTO on January 30, 1998, issued February 8, 2000. ("Nunomiya," MICRON-1005). Nunomiya is prior art under at least 35 U.S.C. § 102(b).

Ground #2: Claim 12 is invalid under (pre-AIA) 35 U.S.C. § 103 on the ground that it is rendered obvious by Nunomiya in view of U.S. Patent No. 5,848,014 ("Yukshing," MICRON-1007). Yukshing was filed with the USPTO on June 12, 1997 and issued on December 8, 1998. Yukshing is prior art under at least 35 U.S.C. § 102(b).

Ground #3: Claims 17-20 are invalid under (pre-AIA) 35 U.S.C. § 103 on the ground that they are rendered obvious by U.S. Patent No. 6,339,344 ("Sakata," MICRON-1006) in view of Yukshing. Sakata was filed with the USPTO on Feb.

2, 2000 and issued on Jan 15, 2002. Sakata is prior art under at least 35 U.S.C. § 102(e).

These grounds are explained below and are supported by the Declaration of Dr. R. Jacob Baker ("Baker Decl.," attached as MICRON-1003).

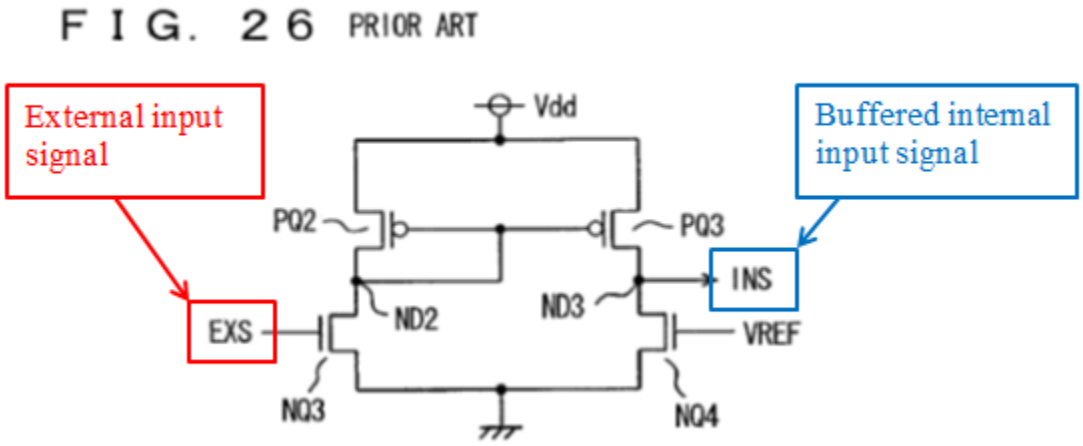
4. OVERVIEW OF THE 296 PATENT

The 296 Patent was filed on May 9, 2002 and claims priority to a Japanese patent application which was filed on June 13, 2001. The 296 Patent issued on February 24, 2004. The 296 Patent generally purports to address inefficiencies in prior art input circuits which are designed to produce an internal buffered signal from an external signal. MICRON-1001, 296 Patent at 1:7-13, 4:5-15. Specifically, the challenged claims of the 296 Patent are directed to two different allegedly novel inventions: (1) challenged claim 1 and dependent claims 11 and 12 are directed to reducing the number of fabrication steps and product costs of an input circuit which can accommodate for a plurality of different types of external interface signals, and (2) challenged claim 17 and dependent claims 18-20 are directed to reducing current consumption in a clock synchronous memory device comprising a first buffer circuit and second clock buffer circuit.

4.1. Input Circuit For Multiple External Interface Specifications (Claims 1, 11, and 12)

Input circuits were well known circuits to those of ordinary skill in the art when the 296 Patent was filed. Input circuits were used, at least in part, to "buffer"

external signals, or, in other words, to form an internal signal with a signal amplitude suitable for internal circuitry from an external signal.[1] *Id.* at 1:16-26. This is necessary in many circuits because an incoming external signal may have an amplitude which is too large or too small for the internal circuitry. *Id.* An exemplary prior art current mirror input buffer discussed in the 296 Patent is reproduced below:



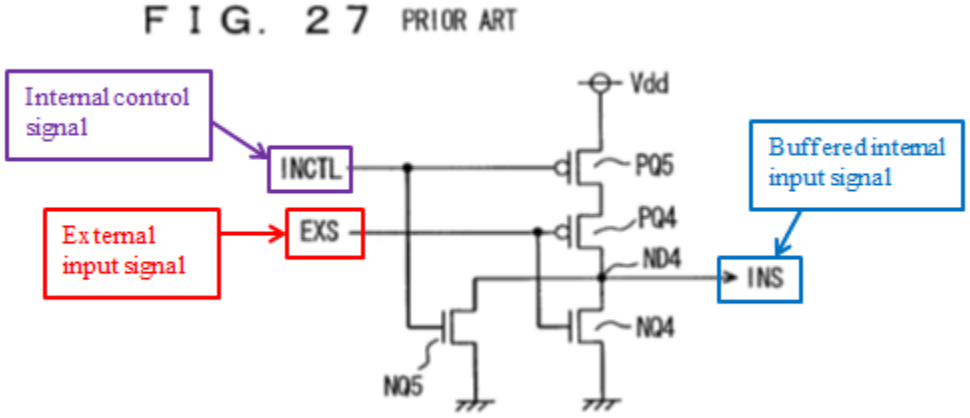
MICRON-1001, 296 Patent at Figure 26 (annotated).[2]

Another conventional input circuit described by the 296 Patent receives two signals, a first external input signal, and a second internal control signal. *Id.* at

[1] The terms "input circuit" and "input buffer" are used interchangeably in the 296 Patent and both refer to a circuit which produces a buffered signal from an external signal. MICRON-1003, Baker Decl. at p. 7 n.1.

[2] All emphases are added unless otherwise stated.

2:36-45. In this configuration, shown below with reference to Figure 27, the input circuit operates dynamically according to internal control signal INCTL such that the external input signal EXS is buffered only when INCTL is at a low level. MICRON-1001, 296 Patent at 2:52-57.



MICRON-1001, 296 Patent at Figure 27 (annotated).

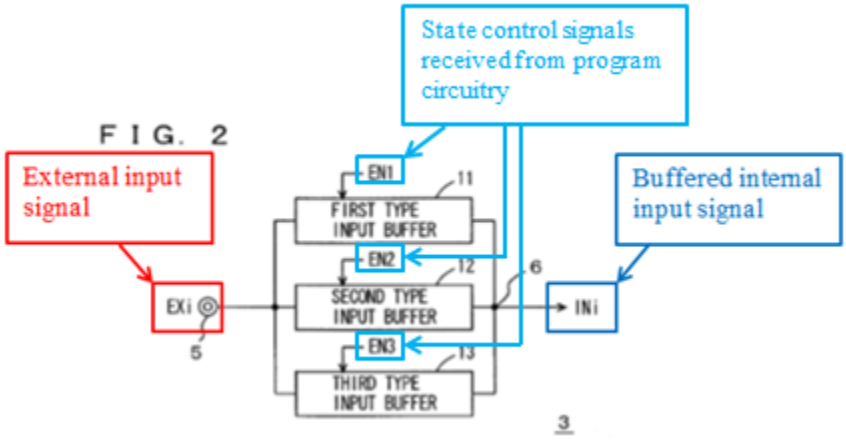
However, the prior art input buffers shown above and discussed in the 296 Patent are each designed to buffer a single type of external signal, i.e., an external signal of a specific amplitude or voltage level. *Id.* at 1:24-26. Thus, in order for an internal circuit to operate in accordance with multiple external signals of different signal amplitudes, a plurality of input circuits of different types or configurations would need to be formed. *Id.* at 3:13-19.

According to the 296 Patent, the plurality of input circuits would conventionally be formed using a master/slice process. *Id.* at 3:20-25. In a master/slice process, a plurality of input circuits corresponding to a plurality of

external interface signals would be formed in parallel on a partially fabricated semiconductor die in a master fabrication process. *Id.* Then, in a subsequent processing step, a patterned interconnect layer "slice" would be formed on top of the semiconductor die. MICRON-1003, Baker Decl. ¶ 27. The interconnect layer would connect the externally received signal to the internal circuitry via the input circuit configured for that type of received signal. *Id*. Thus, as the 296 Patent notes, the master process helps to simplify the manufacturing process because the same partially fabricated die can be used for all applications, but the formation of a separate interconnect layer for each type of input circuit increased fabrication turnaround time (TAT) and the overall product cost of the semiconductor device. MICRON-1001, 296 Patent at 3:35-40. Preparing the separate masks for each input circuit also resulted in further cost increases. *Id.* at 3:42-44.

Acknowledging these problems, the 296 Patent purports to reduce the turnaround time and product cost of an input circuit capable of buffering a plurality of different types of external signals without the need for a separate mask step. Specifically, the 296 Patent describes that a plurality of input buffers formed on the same semiconductor die can be selectively activated using program circuitry, such that only the input buffer designed to receive the external signal currently being applied is operable.

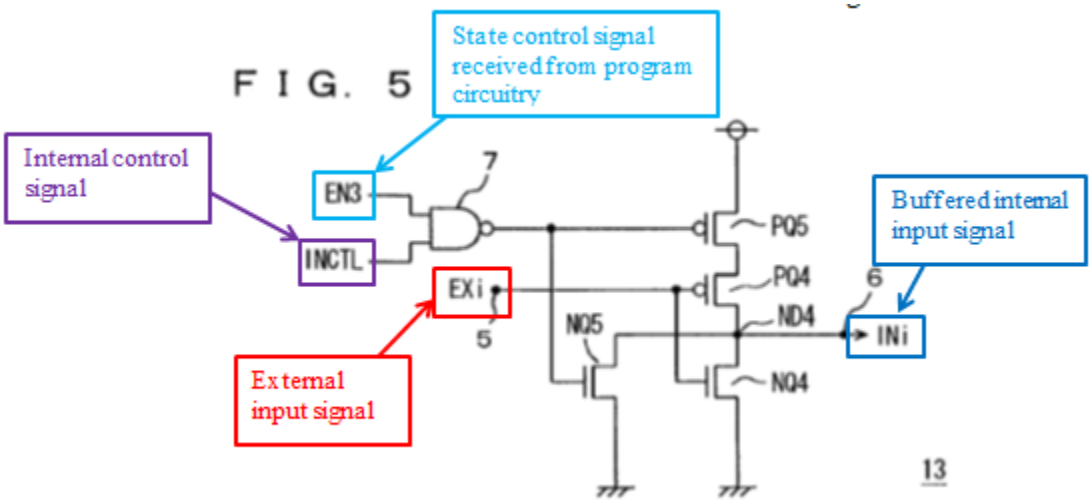
The alleged invention, which is the subject of claims 1, 11, and 12 of the 296 Patent, is to form a plurality of input buffers corresponding to different interface specifications in parallel between an external input signal and a common internal node. *Id.* at 8:27-35. Because each input buffer is designed for a different external interface, only one buffer needs to be activated in response to an incoming internal signal. The activation and deactivation of the input buffers is accomplished using common program circuitry which outputs a selection signal to the input buffers. *Id.* at 6:63-7:2. The selection signals are shown in Figure 2 as EN1, EN2, and EN3 for activating the first type, second type, and third type input buffer respectively. *Id.* This is shown in Figure 2 below.



MICRON-1001, 296 Patent at Figure 2 (annotated).

Only the input buffer selected by the program circuitry, i.e., only the input buffer which corresponds to the output signal EN1, EN2 or EN3 from the program circuitry, is activated and conducts current. *Id.* at 7:2-6.

Additionally, like the conventional input buffer described above, the 296 Patent describes that the operation of the plurality of input buffers can be further controlled in accordance with an internal control signal in addition to the selection signal output from said program circuitry. *Id.* at 8:5-19. Specifically, the selection signal and internal control signal can be received by a logic circuit, and the output of the logic circuit can control the current of the input buffer via a transistor connected between the buffer and its power source. *Id.* This configuration is shown below with reference to Figure 5.



MICRON-1001, 296 Patent at Figure 5 (annotated).

4.2. Low Power Mode For Clock Synchronous Memory Device (Claims 17-20)

The 296 Patent also purports to address the problem of unnecessary current consumption of input buffers used in a clock synchronous memory device. *Id.* at 4:13-15. Clock synchronous memory devices were well known in the art.

MICRON-1003, Baker Decl. ¶ 34. A clock synchronous memory device differs from a non-synchronous device in that a clock synchronous memory operates in accordance with a clock signal and a clock enable signal. *See* MICRON-1001, 296 Patent at 4:46-47; MICRON-1003, Baker Decl. ¶ 34. As the name implies, a clock enable signal can be used to enable or disable the use of the clock. *Id.* In order to do so, it was well known to those of ordinary skill in the art that clock synchronous memory devices could use a clock buffer that receives an external clock and a clock enable signal as inputs. *Id.*; *see* MICRON-1001, 296 Patent at 4:46-48. When the external clock enable signal is active, an internal clock can be generated from an external clock, and the internal clock can be used for timing of the clock synchronous memory device and its input circuit. *See id.*

It was also well known that input circuits are one of the most current consuming parts of a semiconductor device. MICRON-1003, Baker Decl. ¶ 35. However, the need to generate a signal at a high speed in order to drive the internal signal at a faster timing requires that an input buffer operate at all times in accordance with an external signal. MICRON-1001, 296 Patent at 3:45-48. Thus, because clock synchronous memory devices utilize input buffers as well as a clock buffer, the 296 Patent acknowledges that clock synchronous memory devices have power consumption problems that could be minimized when the clock synchronous memory device is not being accessed. For example, the 296 Patent

describes that data access to a clock synchronous memory device is made when a chip select signal is activated, while no access is necessary when a chip select signal is deactivated. *Id.* at 3:50-55. Thus, buffer circuits draw unnecessary power when the device is not being accessed by a chip select signal.

The solution, which is the subject of claims 17-20, is to detect when an external clock enable signal has been held inactive for a predetermined period of time, for example, two clock cycles. *Id.* at 22:37-41. When the external clock enable signal is held inactive for a predetermined amount of time, that signifies that the memory device should enter a low-power mode. *Id.* at 22:61-66. While in the low power mode, the flow of current to the clock buffer and input buffer cease and the buffers are rendered inactive. *Id.* at 22:66-23:4.

5. PROSECUTION HISTORY

The application that led to the issuance of the 296 Patent was originally filed with 18 claims. MICRON-1002, 5-9-2002 Claims at .085-89.

The Examiner subsequently issued a non-final rejection finding claim 1 indefinite under 35. U.S.C. § 112. *Id.,* 4-10-2003 Non-Final Rejection at .202. The Examiner determined that the phrase "according to a received signal when made active" rendered claim 1 indefinite. The Applicant overcame this challenge by amending the claims and stating that when an input buffer is set in an operable state, the input buffer drives the internal node in accordance with the received

signal when the input buffer is activated. *Id.*, 6-16-2003 Amendment at .218. The Applicant also specified that Claim 1 is exemplified by the arrangements of Figs. 3, 4, and 5, and specified that the claimed external signal could comprise an external signal solely in one arrangement and an external control signal for activating the input buffers in another arrangement. *Id.* The Applicant added claims 19 and 20 (which issued as claims 11 and 12) as being directed to specifying of the external signal. *Id.*

Pending claim 1 was also rejected during prosecution under 35 U.S.C. § 102 (b) on the basis that it was anticipated by U.S. Patent No. 5,450,341 ("Sawada"). *Id.*, 4-10-2003 Non-Final Rejection at .203-04. The Applicant overcame this challenge by stating that in the prior art, the input buffers were not of different types and were not capable of accommodating a plurality of interfaces. *Id.*, 6-16-2003 Amendment at .220. The Applicant also specified that in the prior art, the plurality of input buffers were not coupled to the same internal node wherein one of said plurality of input buffers was set to an operable state. *Id.*

6. CLAIM CONSTRUCTION[3]

6.1. Applicable Law

A claim subject to *inter partes* review is given the "broadest reasonable construction in light of the specification of the patent in which it appears."[4] 37 C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

[3] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 296 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35. U.S.C. § 112 are met for any claim of the 296 Patent.

[4] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a POSITA and consistent with the specification of the 296 Patent. Petitioner respectfully submits that the following terms should be construed for this IPR:

6.2.1. "plurality of input buffers of different types or configurations" (claims 1, 11 and 12)

The claim term "plurality of input buffers of different types or configurations" is a limitation of claim 1 of the 296 Patent, and thus is also a limitation of dependent claims 11 and 12. Under the applicable standard, this term means "two or more buffers each of which corresponds to a different interface or is of a different configuration."

The specification of the 296 Patent clarifies that the "input buffers of different types or configurations" in claim 1 are directed to input buffers corresponding to different interfaces, "regardless of whether or not a circuit configuration of the input buffer circuit is the same." MICRON-1001, 296 Patent at 10:29-32; *see also id.* at 10:12-17 ("Two kinds of the NOR input buffers shown in Fig. 5 are utilized as input buffers with the ratio of the circuits changed. There are prepared the circuits the same in circuit configuration but different in ratio, or different in input logic threshold voltage, as input buffers that are different in type and correspond to different interfaces"); MICRON-1003, Baker Decl. ¶ 45.

The prosecution history also supports Petitioner's construction. In order to overcome a prior art rejection of claim 1, the Applicant emphasized that the "plurality of input buffers" can accommodate a plurality of interfaces. MICRON-1002, 6-16-2003 Amendment at .220 ("According to the arrangement of the claim 1 invention, the semiconductor device can accommodate for a plurality of interfaces with the common buffer arrangement.").

Thus, a person of ordinary skill in the art would have understood that the claim term "plurality of input buffers of different types or configurations" means "two or more buffers each of which corresponds to a different interface or is of a different configuration." MICRON-1003, Baker Decl. ¶¶ 44-46.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 296 Patent would be a person with a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least 2-3 years of experience in the design of memory devices. An individual with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the design of memory devices. *Id.* ¶ 47.

8. DESCRIPTION OF THE PRIOR ART

8.1. U.S. PATENT NO. 6,023,175 ("NUNOMIYA")

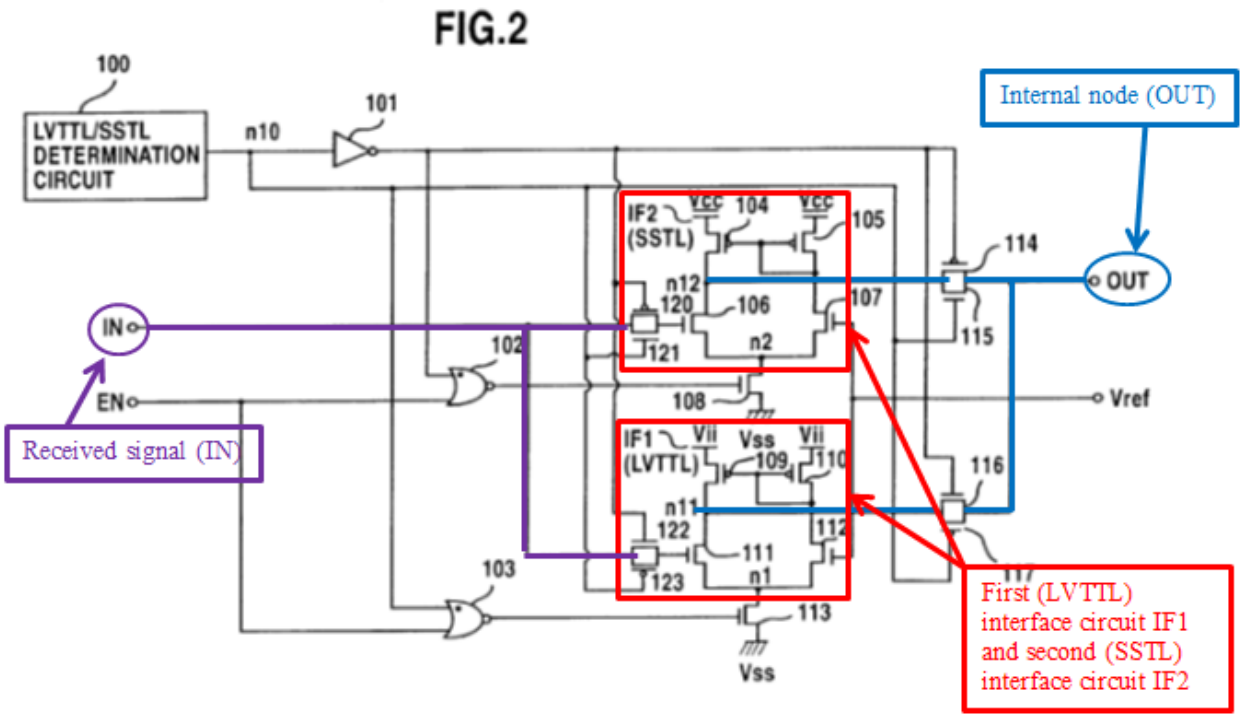
U.S. Patent No. 6,023,175 ("Nunomiya") (MICRON-1005), was filed on January 30, 1998, and claims priority to a Japanese patent application filed September 4, 1997. Nunomiya issued on February 8, 2000, to Kazuhiro Nunomiya, et al. and is entitled "Level Interface Circuit." The original assignee of Nunomiya was Fujitsu Limited. Nunomiya is prior art to the 296 Patent under at least (pre-AIA) 35 U.S.C. § 102(b) because the patent issued more than one year before the earliest application to which the 296 Patent claims priority was filed.

Nunomiya is directed to the same problem as that being addressed by Claims 1, 11 and 12 of the 296 Patent. Specifically, Nunomiya discloses that it is difficult to utilize the same input circuit for multiple different external interface signals having different amplitudes. MICRON-1005, Nunomiya at 1:5-7, 2:28-32. To address this problem, Nunomiya describes an input circuit which is compatible with different interface signals and can generate a common internal signal regardless of which type of external signal is being applied. *Id.* at 2:35-37.

In particular, Nunomiya describes forming two level interface circuits. The first interface circuit is optimized for a first external "LVTTL" interface level, and a second interface circuit is optimized for a second external "SSTL" interface level. *Id.* at 4:36-49. The "level interface circuits" described in Nunomiya are

"input buffers" as described and claimed in the 296 Patent. MICRON-1003, Baker Decl. ¶ 52.

The level interface circuits (input buffers) in Nunomiya are formed in parallel such that each circuit shares the same external input IN and are coupled to the same external output OUT as shown in Figure 2 below.



MICRON-1005, Nunomiya at Figure 2 (annotated).

Nunomiya also describes that the interface circuits (input buffers) are controlled in accordance with the output n10 of a LVTTL/SSTL determination circuit 100. MICRON-1005, Nunomiya at 4:36-49. Specifically, the output n10 of the LVTTL/SSTL determination circuit is provided to NOR gates 102 and 103, which selectively render either the first interface circuit or second interface circuit

operable. *Id.* at 4:45-48. Additional control over the operability of the interface circuits (input buffers) is provided by an enable control signal EN to the NOR gates 102 and 103. *Id.* at 4:48-49.

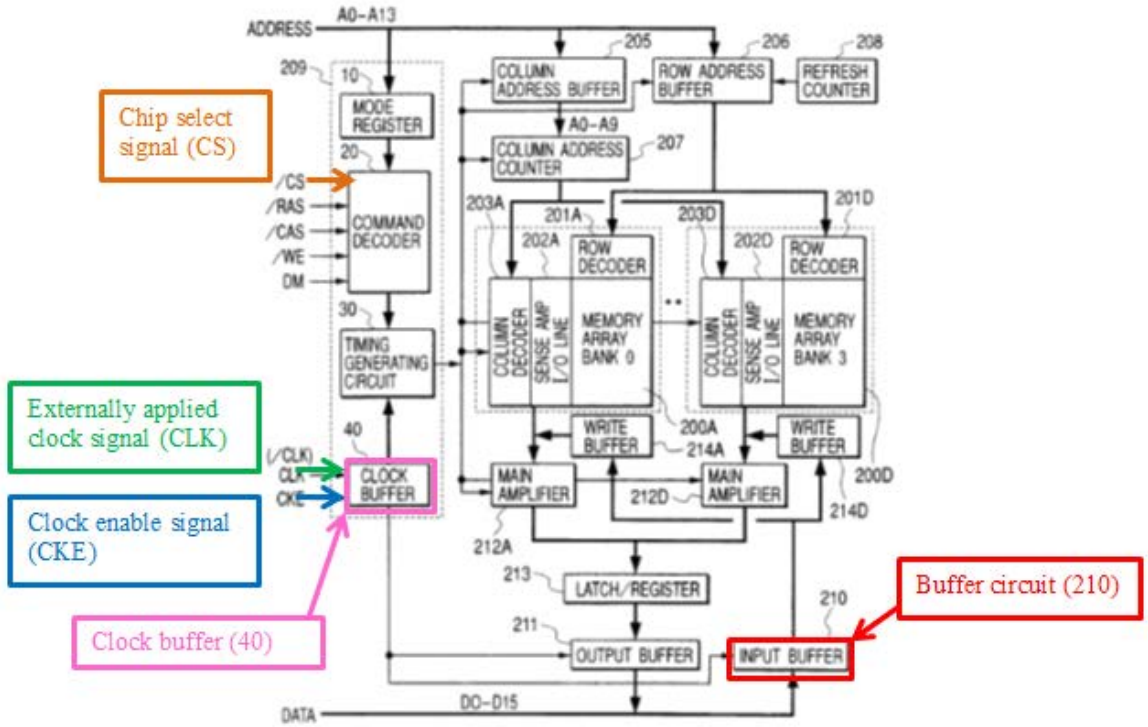
What Nunomiya is silent about, which is required by claim 12 of the 296 Patent, is whether the received enable control signal EN for activating the input buffers is an internal or external control signal. However, as discussed below, it would have been obvious to one of ordinary skill in the art to modify and/or supplement the teachings of Nunomiya with the internal control signal for activating and deactivating the input buffers disclosed in Yukshing.

8.2. U.S. PATENT NO. 6,339,344 ("SAKATA")

U.S. Patent No. 6,339,344 ("Sakata") (MICRON-1006) was filed on February 2, 2000, and claims priority to two Japanese patent applications, the earliest of which was filed on February 17, 1999. Sakata issued on January 15, 2002, to Takeshi Sakata, et al. and is entitled "Semiconductor integrated circuit device." The original assignees of Sakata were Hitachi, Ltd., and Hitachi ULSI Systems Co., Ltd. Sakata is prior art to the 296 Patent under at least (pre-AIA) 35 U.S.C. § 102(e) because the U.S. Patent Application which issued as Sakata was filed before the earliest application to which the 296 Patent claims priority.

Sakata is directed to the same problem of reducing power consumption of buffer circuits when a clock synchronous memory device is not in use that is being

addressed by claims 17-20 of the 296 patent. MICRON-1006, Sakata at 10:54-61. In particular, Sakata teaches an input circuit for a clock synchronous memory device which includes a clock buffer for generating an internal clock signal, and a buffer circuit for generating an internal signal from an externally applied data signal. *Id.* at 26:24-26, 26:59-61. Sakata also teaches an external clock enable signal CKE which controls the validity of the clock signal, and a chip select signal CS which controls the start of the command input cycle. *Id.* at 27:2-6, 27:12-16. These elements are depicted in Fig. 25 below.



MICRON-1006, Sakata at Figure 25 (annotated).

In order to address the problem of unnecessary power consumption, Sakata teaches an internal circuit which detects whether the clock enable signal has been

determined to be at a logic low level for more than a prescribed period of time, at which point a power down signal is generated. *Id.* at 11:30-34. In response to the power down signal, the input circuit can decrease current consumption and inactivate the input buffer. *Id.* at 11:34-41.

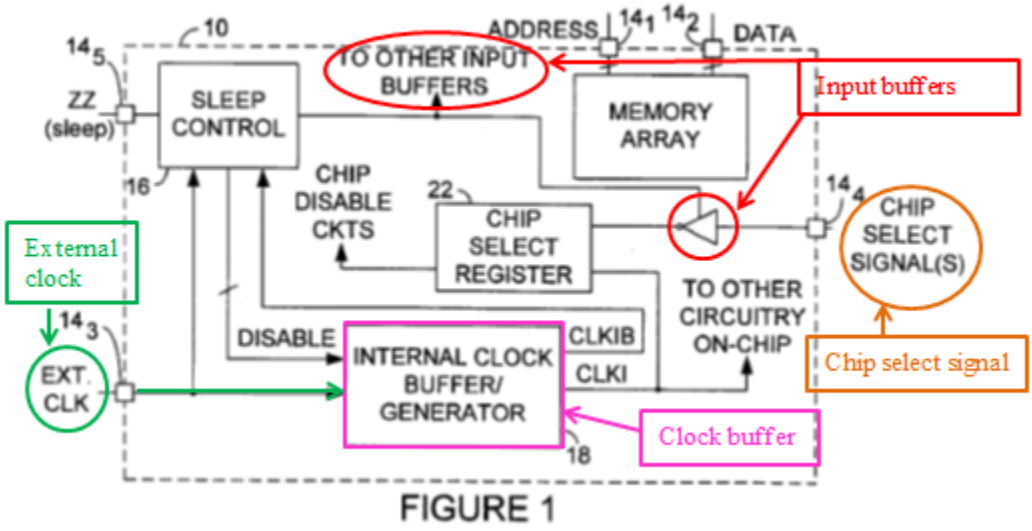
What Sakata does not describe expressly, which is required by independent claim 17 of the 296 Patent and therefore claims 18-20 by incorporation, is the deactivation of the clock buffer in response to the low power mode signal. Additionally, Sakata is silent as to whether its chip select signal (the claimed "activation control signal") is also deactivated, i.e., rendered inoperable, in response to the low power down mode, which is required by claim 19. However, as discussed in detail below, it would have been obvious to modify and/or supplement the teachings of Sakata with the clock buffer disable circuitry and chip select deactivation which is disclosed in Yukshing.

8.3. U.S. PATENT NO. 5,848,014 ("YUKSHING")

U.S. Patent No. 5,848,014 ("Yukshing") (MICRON-1007) was filed on June 12, 1997. Yukshing issued on December 8, 1998, to Antony Yukshing and is entitled "Semiconductor Device Such As A Static Random Access Memory (SRAM) Having A Low Power Mode Using A Clock Disable Circuit." The original assignee of Yukshing was Cypress Semciondcutor Corp. Yukshing is prior art to the 296 Patent under at least (pre-AIA) 35 U.S.C. § 102(b) because the patent

issued more than one year before the earliest application to which the 296 Patent claims priority was filed.

Yukshing discloses a clock synchronous memory device which can be placed into a reduced power mode of operation. MICRON-1007, Yukshing at 2:7-10. The semiconductor memory device includes an internal clock buffer for generating an internal clock, and other input buffers for generating internal signals from external signals, including input buffers which buffer control signals such as chip select or chip enable signals. *Id.* at 4:2-9, 4:15-19. These elements are shown in Figure 1 which is reproduced below.



MICRON-1007, Yukshing at Figure 1 (annotated).

Yukshing also discloses a reduced power mode which is commanded by the assertion of a reduced power command signal, such as the a Jedec-standard "ZZ" signal. *Id.* at Abstract. Specifically, when the ZZ sleep signal is inactive, the

memory device works in a normal operation mode wherein the clock buffer and input buffers are maintained in an operable state. *Id.* at 4:33-36. However, in response to the ZZ sleep signal being active, the internal clock buffer is disabled. *Id.* at 3:62-65. Additionally, Yukshing discloses that an internal control signal, CONTROL, is generated in the low power mode which disables the input buffers. *Id.* at 4:36-4:45. By disabling the input buffers, which as discussed above includes a chip select buffer, Yukshing discloses that the chip select signal is deactivated when the ZZ sleep signal is applied. *Id*.

9. GROUND #1: CLAIMS 1 AND 11 OF THE 296 PATENT ARE UNPATENTABLE AS ANTICIPATED BY NUNOMIYA

Claims 1 and 11 of the 296 Patent are unpatentable as anticipated under 35 U.S.C. § 102 by Nunomiya. Petitioner's arguments are supported by Dr. Baker's Declaration. In particular, Dr. Baker's Declaration includes a claim chart in Appendix A which demonstrates that the limitations of claims 1 and 11 are found in Nunomiya. Petitioner addresses those limitations below.

9.1. Claim 1 is anticipated by Nunomiya

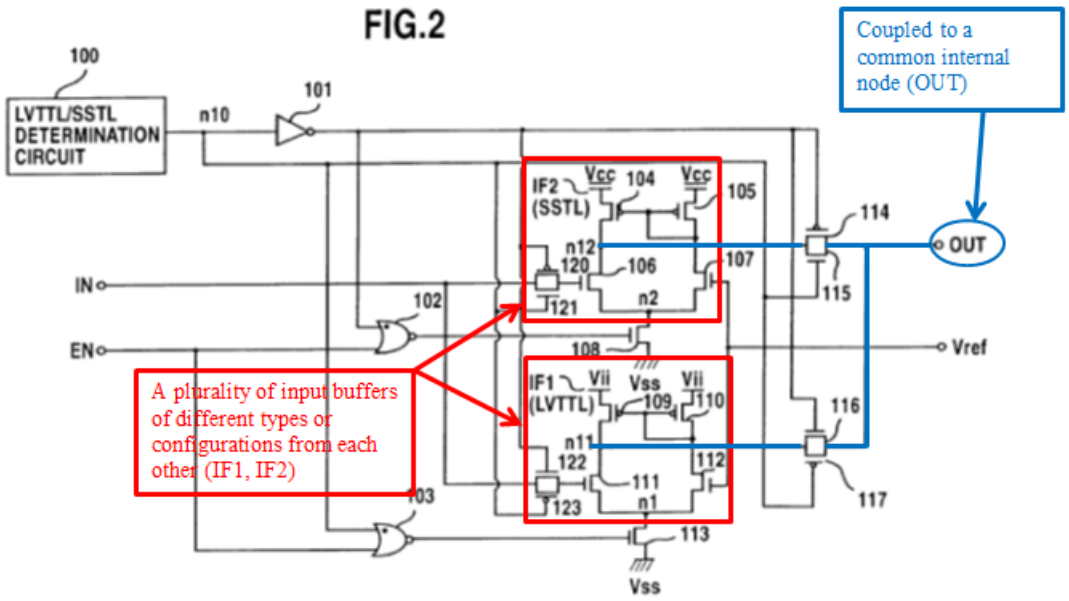
9.1.1. [1.P] "A semiconductor device comprising:…"

Nunomiya discloses a semiconductor device. Specifically, Nunomiya discloses a level interface circuit which includes transistors that would be found on

a semiconductor device such as a dynamic RAM. MICRON-1005, Nunomiya at 1:5-7, 1:8-10, Fig. 2.

9.1.2. [1.1] "a plurality of input buffers of different types or configurations from each other and coupled to a common internal node; and"

Nunomiya discloses a plurality of input buffers of different types or configurations from each other and coupled to a common internal node, wherein "a plurality of input buffers of different types or configurations from each other" means "two or more buffers each of which corresponds to a different interface or is of a different configuration." *Id.* at Fig. 2; *see* Section 6.2.1 *supra*.



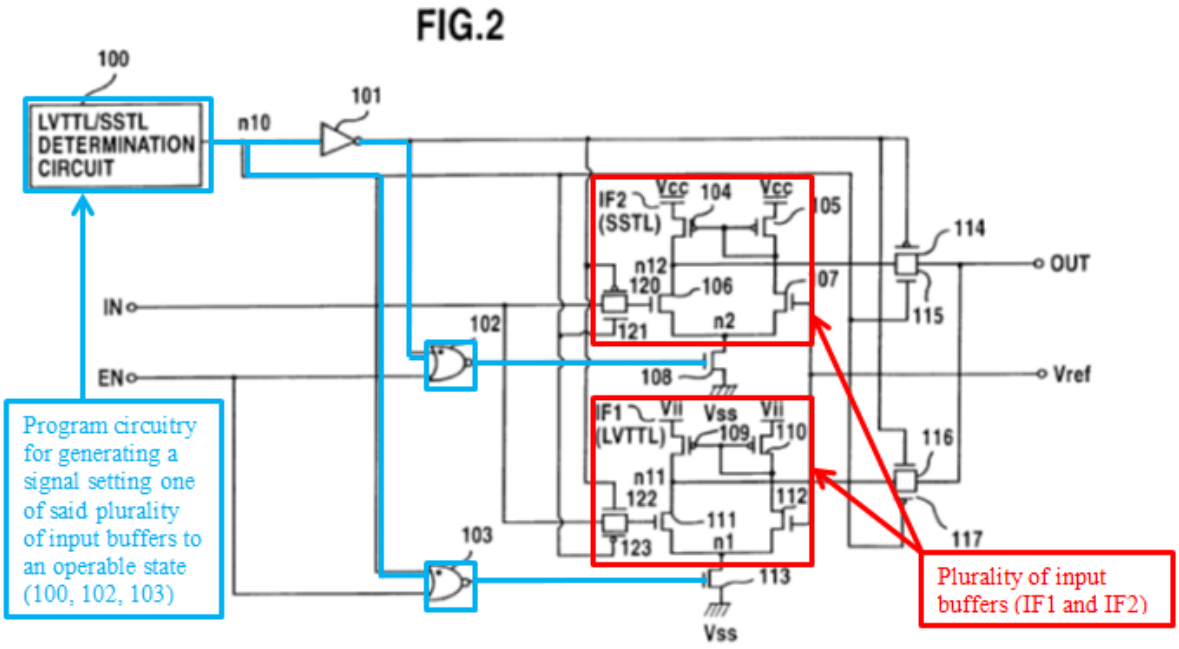
MICRON-1005, Nunomiya at Figure 2 (annotated).

Specifically, Nunomiya discloses "a first interface circuit IF1, to handle LVTTL circuit input signal IN" and "a second interface circuit IF2, to handle an SSTL circuit input signal IN." MICRON-1005, Nunomiya at 4:37-41. Interface

circuit IF1 and interface circuit IF2 are input buffers, and both are coupled to the same common internal node OUT. *Id.* at 6:42-44 ("the drain node n1l of the transistor 111 is connected to the output terminal OUT"), 6:52-54 ("the drain node n12 of the transistor 106 is connected to the output terminal OUT"). The 296 Patent confirms that the level interface circuits described in Nunomiya are input buffers of "different types" because they each correspond to a different interface. MICRON-1001, 296 Patent at 10:29-32 ("Therefore, an input buffer of a different type has only to be a circuit corresponding to a different interface, regardless of whether or not a circuit configuration of the input buffer is the same."); MICRON-1003, Baker Decl., Appx. A at claim [1.1].

9.1.3. [1.2] "program circuitry for generating a signal setting one of said plurality of input buffers to an operable state, said plurality of input buffers driving the internal node according to a received signal when an input buffer is set to the operable state."

Nunomiya discloses program circuitry for generating a signal setting one of said plurality of input buffers to an operable state, said plurality of input buffers driving the internal node according to a received signal when an input buffer is set to the operable state. MICRON-1005, Nunomiya at Fig. 2.

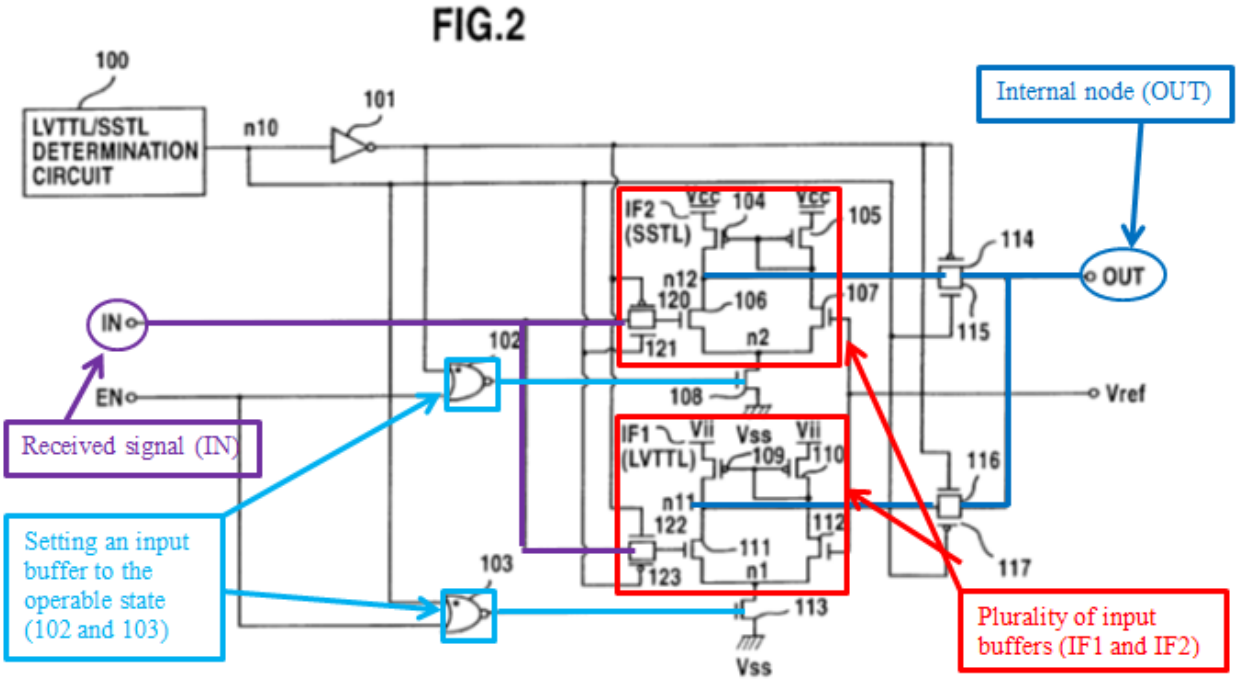


MICRON-1005, Nunomiya at Figure 2 (annotated).

Specifically, Nunomiya teaches a LVTTL/SSTL determination circuit which generates a signal n10 to set either the first interface circuit IF1 or second interface circuit IF2 to an operable state. *Id.* at 5:10-13 ("The LVTTL/SSTL determination circuit 100 examines the externally received reference level voltage Vref, and generates output signal n10 at level L for VTTL and output signal n10 at level H for SSTL"), 4:42-45 ("a determination circuit 100 for detecting an externally received reference level voltage Vref and determining whether or not it is an LVTTL circuit signal or an [sic] STTL circuit signal"). The LVTTL/SSTL determination circuit is the claimed "program circuitry." When an LVTTL signal is detected by the detection circuit, the LVTTL interface circuit IF1 is activated, and when an SSTL signal is detected, the SSTL interface circuit IF2 is activated.

Id. at 5:11-22. The interface circuits are set to an operable state by controlling via NOR gates 102 and 103 whether transistor 108 or transistor 113 is conductive. *Id.* If transistor 108 is conductive, the LVTTL circuit is made operable, and if transistor 113 is conductive, the SSTL circuit is made operable. *Id.*

Nunomiya also discloses that the OUT pin is connected in common to the outputs of the first and second level interface circuit, n11 and n12 respectively. According to a received signal IN, the OUT pin is selectively driven by either the first interface circuit or second interface circuit depending on which interface circuit is rendered operable by the determination circuit. *Id.* at Fig. 2, 6:28-44, 6:45-54.



MICRON-1005, Nunomiya at Figure 2 (annotated).

9.2 Claim 11 is anticipated by Nunomiya

9.2.1 [11.0] "The semiconductor device according to claim 1, wherein said received signal comprises an externally applied signal."

Nunomiya discloses the semiconductor device according to claim 1, wherein said received signal comprises an externally applied signal. Specifically, Nunomiya discloses that the received signal IN is "externally input." *Id.* at 1:61-67 ("The level interface circuit compares externally input signal IN with the reference level voltage Vref, and in accordance with level H and level L of the input IN, generates at the output terminal OUT a signal whose level is adjusted to the level of a CMOS circuit at the following stage."), 4:43 ("[A]n externally received reference level voltage Vref"); *see* Section 8.1 *supra*.

10. GROUND #2: CLAIM 12 OF THE 296 PATENT IS UNPATENTABLE AS OBVIOUS OVER NUNOMIYA IN VIEW OF YUKSHING

Claim 12 of the 296 Patent is unpatentable as obvious under 35 U.S.C. § 103 by Nunomiya in view of Yukshing. Nunomiya discloses all of the elements of Claim 12 except whether the control signal for activating the input buffers, EN, is an internal signal. Yukshing discloses such an internal control signal. A person of ordinary skill in the art therefore would have found claim 12 obvious over Nunomiya in view of Yukshing.

10.1. It would have been obvious to a person of ordinary skill in the art to combine Nunomiya with Yukshing

It would have been obvious to a person of ordinary skill in the art to combine Nunomiya with Yukshing as Dr. Baker explains. MICRON-1003, Baker Decl. Section X.B. Nunomiya and Yukshing both teach techniques useful in creating an input circuit for converting an external signal into an internal signal. Yukshing, for example, teaches an exemplary input circuit for a static RAM semiconductor device. MICRON-1007, Yukshing at 3:37-42. Nunomiya on the other hand teaches an input circuitry which can be generally applied for integrated circuit devices receiving LVTTL and SSTL interface signals. MICRON-1005, Nunomiya at 1:9-11. A person of ordinary skill in the art understood that one such integrated circuit device for receiving LVTTL and SSTL interface signals is a static RAM. MICRON-1003, Baker Decl. ¶ 69. Accordingly, a person of ordinary skill in the art would have found it obvious that the teachings of Nunomiya could be applied to Yukshing, and vice versa, and that such a combination would have been obvious to try. *Id.*

A person of ordinary skill in the art would have found the combination of Nunomiya with Yukshing to be merely a combination of prior art elements according to known methods that would yield predictable results. Specifically, the enable signal EN disclosed in Nunomiya and the internal signal, CONTROL, described in Yukshing both serve the same function of controlling the operability

of the input buffers. MICRON-1005, Nunomiya at 5:13-22 ("When LVTTL is detected, the output signal at the NOR gate 103 goes to level H because of …the active level L of the input enable signal EN … and the LVTTL interface circuit IF1 is activated. When SSTL is detected, the output signal at the NOR gate 102 goes to level H because … the active level L of the input enable signal EN … and the SSTL interface circuit IF2 is activated."); MICRON-1007, Yukshing at 4:2-9 ("In addition to the disable signal, sleep control circuit 16 further generates a control signal, designated CONTROL…The control signal disables the input buffers in the manner described below."). Thus, it would have been obvious to a person of ordinary skill in the art that the EN signal disclosed in Nunomiya could be substituted with the internal CONTROL signal disclosed in Yukshing. MICRON-1003, Baker Decl. ¶ 70.

Furthermore, persons of ordinary skill in the art would have been motivated to combine the teachings of Nunomiya with the teachings of Yukshing because both patents are directed to the same function of enabling and disabling different input buffers, and would have been motivated to combine the references for that reason. MICRON-1005, Nunomiya at 5:14-22; MICRON-1007, Yukshing at 4:2-15. In particular, a person of ordinary skill in the art would have found it obvious that the control system described in Yukshing would have been equally applicable to Nunomiya, and would have found it obvious to utilize such a system based on

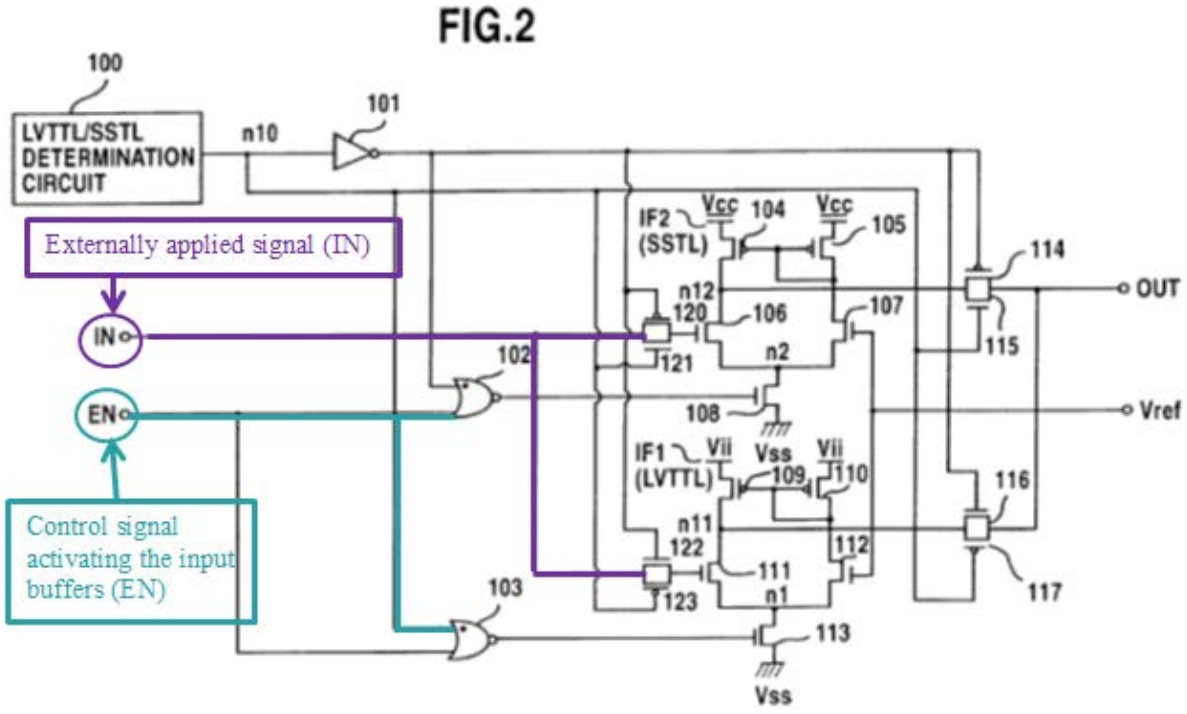
design pressures and market incentives to, for example, reduce the power consumption of the input circuit described in Nunomiya. *See* MICRON-1007, Yukshing at 1:16-21 ("In an effort to continually improve [present day electrical products], a desired goal has been to reduce the amount of power consumed during the operation of such products. Towards this end, it is desirable to reduce the power consumption of a product's component parts, including any semiconductor devices."); MICRON-1003, Baker Decl. ¶ 71.

Additionally, a person of ordinary skill in the art would have understood that substituting the internal control signal (CONTROL) disclosed in Yukshing for the enable signal (EN) disclosed in Nunomiya would have merely been a simple substitution of one known element for another to obtain predictable results. Indeed, as the 296 Patent admits, employing an internal control signal to control the operability of input buffers was a conventional design choice. *See* MICRON-1001, 296 Patent at 2:36-45 (describing conventional prior art input buffer using "internal control signal INCTL" to control operability of input buffers.); MICRON-1003, Baker Decl. ¶ 72.

10.2. Claim 12 is obvious over Nunomiya in view of Yukshing

10.2.1. [12.0] "The semiconductor device according to claim 1, wherein said received signal comprises an externally applied signal and an internal control signal activating the input buffers."

One of ordinary skill in the art would have found it obvious to modify Nunomiya using the teachings of Yukshing such that the received signal comprises an externally applied signal and an internal control signal activating the input buffers. MICRON-1005, Nunomiya at Fig. 2; MICRON-1003, Baker Decl. at claim [12.0]



MICRON-1005, Nunomiya at Figure 2 (annotated).

First, as discussed with respect to claim 11, Nunomiya discloses "wherein said received signal comprises an externally applied signal." *See* Section 9.2.1

claim [11.0] *supra*. Second, Nunomiya teaches an enable signal EN which activates the input buffers IF1 and IF2 through NOR gates 102 and 103. MICRON-1005, Nunomiya at 4:48-49. The input signal EN is the claimed "control signal for activating the input buffers." Specifically, the input buffers are activated only when the input enable signal EN is at the active level L. *Id.* at 5:13-22 ("When LVTTL is detected, the output signal at the NOR gate 103 goes to level H because of the level L of the output signal n10 and the active level L of the input enable signal EN; the transistor 113 is rendered conductive; and the LVTTL interface circuit IF1 is activated. When SSTL is detected, the output signal at the NOR gate 102 goes to level H because of the level H of the output signal n10 and the active level L of the input enable signal EN; the transistor 108 is rendered conductive; and the SSTL interface circuit IF2 is activated.").

There is no disclosure in Nunomiya which indicates whether the control signal EN is an internal or external input signal. However, it would have been obvious to a person of ordinary skill in the art to modify the enable signal EN disclosed in Nunomiya to be an internal control signal in view of the teachings of Yukshing. Specifically, Yukshing discloses an internal control signal "CONTROL" generated by sleep control circuit 16 which controls the operability of the input buffers. MICRON-1007, Yukshing at 4:2-9 ("In addition to the disable signal, sleep control circuit 16 further generates a control signal, designated

CONTROL, which is provided to preselected other circuits of SRAM 10, including input buffer 20, as well as, in a preferred embodiment, all other input buffers (except the ZZ buffer and the small clock monitor) such as the address and data input buffers. The control signal disables the input buffers in the manner described below.").

Yukshing describes that, like the enable signal EN in Nunomiya, internal signal CONTROL asynchronously controls the input buffers to be either ON, in which each input buffer passes the signal on its input to its output, or OFF, wherein the input buffers do not operate. *Id.* at 4:33-43 ("In the preferred embodiment, input buffer 20 (as well as other input buffers) is controlled asynchronously to be ON or OFF. When the buffers are 'ON' they merely pass the signal on their input to their output, as is conventional. When the input buffers are OFF, however, such as when the ZZ 'sleep' signal is applied to SRAM 10 to generate an active control signal, the respective output signals of the plurality of input buffers (especially the input buffers which buffer control signals like the chip enable signals) appear as though a nonactive signal is being externally applied to the respective input pin.").

Thus, in view of Yukshing, it would be obvious to modify Nunomiya to include internal control circuitry (e.g. sleep control circuit 16) to generate an internal signal EN). MICRON-1003, Baker Decl., Appx. A at claim [12.0].

11. GROUND #3: CLAIMS 17-20 OF THE 296 PATENT ARE UNPATENTABLE AS OBVIOUS OVER SAKATA IN VIEW OF YUKSHING

Claims 17-20 of the 296 Patent are unpatentable as obvious under 35 U.S.C. § 103 by Sakata in view of Yukshing. Sakata discloses all of the limitations of claims 17-20 except for deactivation of a clock buffer in response to a low-power mode signal and deactivation of an operation control signal in response to a low-power mode signal. Yukshing discloses such deactivation. A person of ordinary skill in the art therefore would have found claims 17-20 obvious over Sakata in view of Yukshing.

11.1. It would have been obvious to a person of ordinary skill in the art to combine Sakata with Yukshing

It would have been obvious to a person of ordinary skill in the art to combine Sakata with Yukshing as Dr. Baker explains. MICRON-1003, Baker Decl. Section X.C. Sakata and Yukshing both address the same technical problem – decreasing current consumption in a synchronous memory device by disabling input circuitry. *Id.* ¶ 78. Sakata, for example, discloses that it is an object of the invention to "provide a semiconductor device having an input circuit capable of reducing consumed current without delaying a timing of generating an internal signal." MICRON-1006, Sakata at 1:65-2:2. Similarly, Yukshing discloses that "[o]ne advantage of the invention is the substantial reduction in power

consumption due to disabling the external clock." MICRON-1007, Yukshing at 7:36-38.

Both Sakata and Yukshing adopt similar solutions to the problem. Both Sakata and Yukshing describe disabling buffer circuits when the memory device is put into a low power mode. More specifically, Sakata enters into a low power mode when a clock enable signal is held inactive for a prescribed period of time. MICRON-1006, Sakata at 11:31-41. In the low power mode, an internal circuit generates a power down signal PWD which disables the input buffer circuits. *Id.; see id.* at 16:7-19. Yukshing similarly enters into a low power mode when a low power sleep mode signal is input to the circuit. MICRON-1007, Yukshing at 6:47-61. Also like Sakata, Yukshing describes that input buffers are disabled in response to the low power sleep mode signal. *Id.* at 6:62-65. Yukshing also describes that the clock buffer and buffers for internal control signals such as a chip select signal are disabled such that the only current being drawn is leakage current. *Id.* at 7:37-40.

It would have been obvious to one of ordinary skill in the art for several reasons to combine the disclosures of Sakata with the teachings of Yukshing. First, as discussed above, the clock disable circuitry of Yukshing solves the same problem of current consumption that Sakata is directed to. Thus a person of ordinary skill in the art would have been motivated based on the nature of the

problem to be solved to adapt Sakata to include Yukshing. MICRON-1003, Baker Decl. ¶¶ 78-79.

Second, a person of ordinary skill in the art would have found the combination of Sakata and Yukshing to be merely a combination of prior art elements according to known methods that would yield predictable results. *Id.* ¶ 79. In both Sakata and Yukshing, the clock buffers serve the same function of buffering an external clock signal to form an internal clock signal, and the internal clock signal serves the same function of controlling other circuits in the memory device. MICRON-1006, Sakata at 26:59-61; MICRON-1007, Yukshing at 6:35-38. Similarly, the power down signal disclosed in Sakata serves the same function as the ZZ sleep mode signal in Yukshing, i.e., disabling internal circuitry when the memory device is not in use. MICRON-1006, Sakata at 11:30-40; MICRON-1007, Yukshing at 6:62-65. Further, the chip select signals in both Sakata and Yukshing serve the well-known function of selecting and deselecting a memory chip. MICRON-1006, Sakata at 27:2-6; MICRON-1007, Yukshing at 4:25-30. A person of ordinary skill in the art would thus have recognized that it was possible to operate the clock buffer in Sakata using the circuitry for enabling and disabling the clock buffer and rendering the chip select signal inactive as described in Yukshing. Thus, a person of ordinary skill in the art would have recognized that

Yukshing represents a solution to Sakata's problem that would have been obvious to try. MICRON-1003, Baker Decl. ¶ 80.

Additionally, while the embodiment described in Sakata is directed to a dynamic random access memory (DRAM) and Yukshing is directed to a static random access memory (SRAM), persons of ordinary skill in the art were familiar with both technologies and understood that the teachings in one type of memory could be applied to the other. *Id.* ¶ 81. For example, persons of skill in the art understood that the same types of input buffers were used in both DRAM and SRAM. *Id.* Additionally, Sakata explicitly describes that "the semiconductor integrated device may be a static RAM" and can be "widely utilized for a variety of semiconductor integrated circuit devices connected together through such an interface such a s LVTTL, LVCMOS or SSTL." MICRON-1006, Sakata at 35:6-12. Accordingly, persons of skill in the art would have found it obvious to combine the teachings of Yukshing with the teachings of Sakata because Sakata was known to be applicable to both types of random access memory devices.

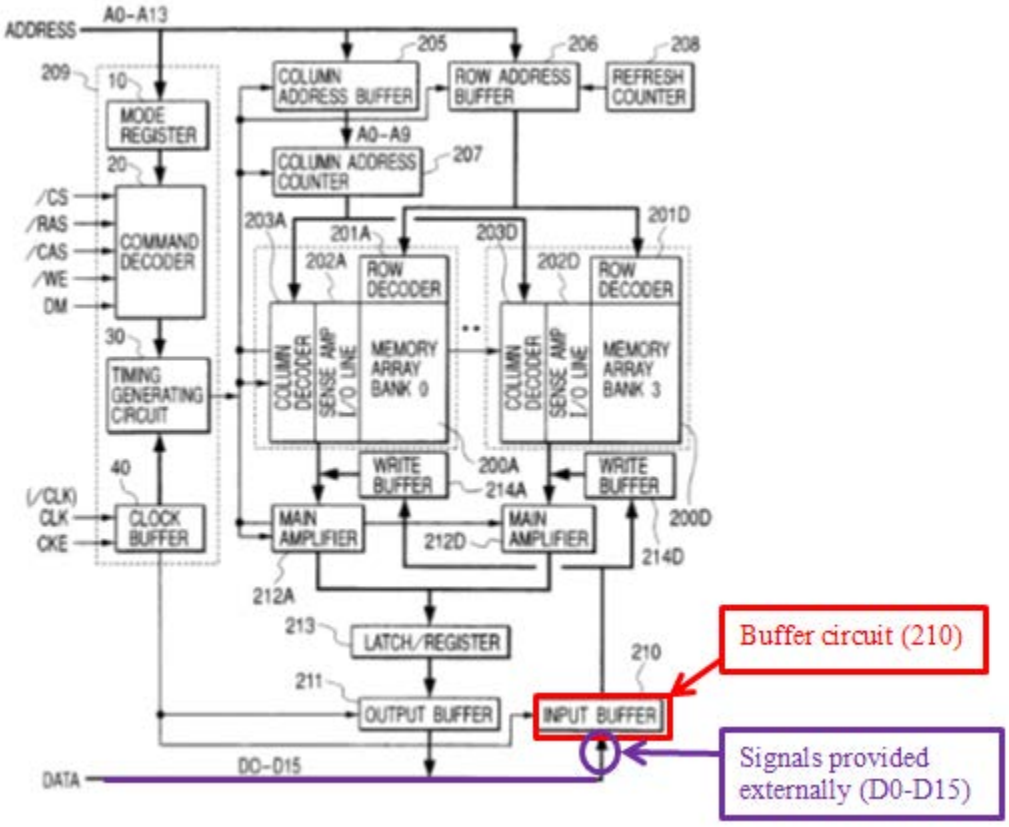
11.2. Claim 17 is obvious over Sakata in view of Yukshing

11.2.1. [17.P] "A semiconductor device comprising:…"

Sakata discloses a semiconductor device. Specifically, Sakata discloses a "semiconductor integrated circuit device." MICRON-1006, Sakata at Title.

11.2.2. [17.1] "a buffer circuit for buffering a signal provided externally when active"

Sakata discloses a buffer circuit for buffering a signal provided externally when active. *Id.* at Fig. 25.



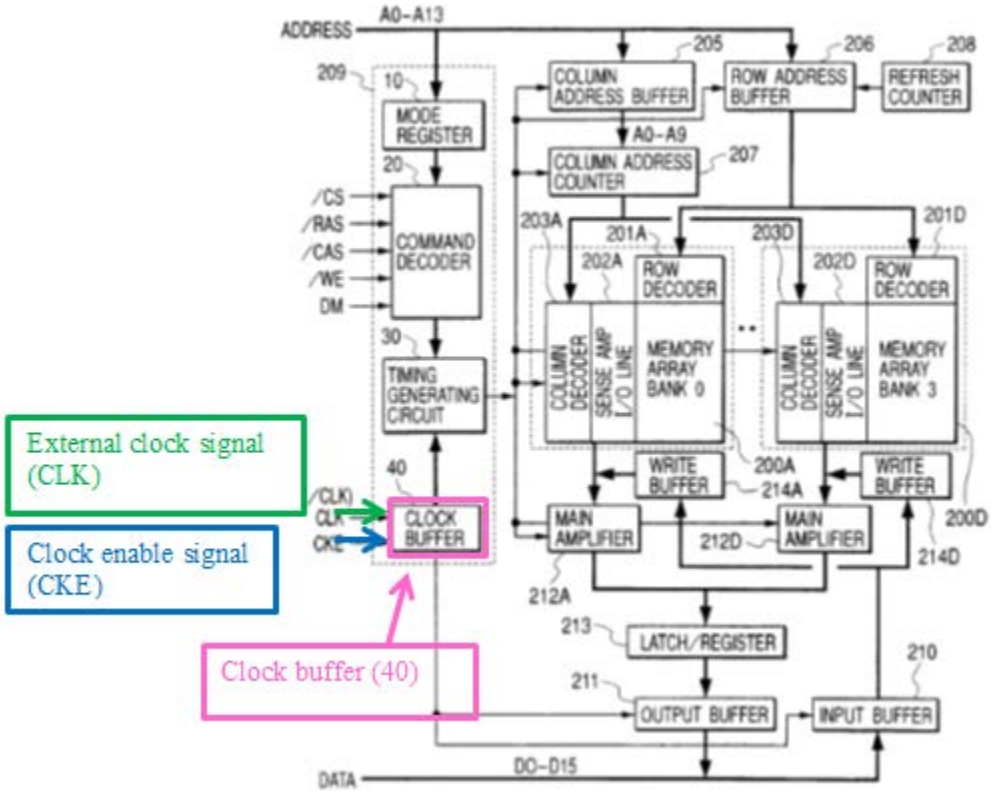
MICRON-1006, Sakata at Figure 25.

Specifically, Sakata teaches an input buffer 210 which buffers external data signals D0-D15. *Id.* at 26:24-28. The input buffer 210 is active in accordance with an internal clock signal. *Id.* at 26:62-64 ("[T]he internal clock is used as a timing signal for activating the output buffer 211 and the input buffer 210, and is fed to the timing-generating circuit 30."). The input buffer 210 is of the differential

amplifier circuit type. *Id.* at 5:34-40 ("As described above, the input buffer of the present invention uses the input circuit of the differential amplifier circuit type yet exhibiting characteristics equal to those of the input circuit such as the CMOS inverter circuit, and can be used in common for all interfaces such as the SSTL, LVTTL and LVCMOS.").

11.2.3. [17.2] "a clock buffer for generating an internal clock signal according to an external clock signal when a clock enable signal is active"

Sakata discloses a clock buffer for generating an internal clock signal according to an external clock signal when a clock enable signal is active. *Id.* at Figure 25.



MICRON-1006, Sakata at Figure 25.

Specifically, Sakata discloses a clock buffer 40 which buffers an external clock signal CLK to generate an internal clock. *Id.* at 26:45-58 ("In FIG. 25, though there is no particular limitation, a controller 209 represented by a dotted line **receives external control signals such as clock signal CLK**, clock enable signal CKE, chip select signal /CS, column address strobe signal /CAS (signals with a symbol / are row enable signals), row address strobe signal /RAS and write enable signal /WE, as well as control data through the address input terminals A0 to A11, **and forms internal timing signals for controlling the operation mode of the SDRAM** and the operation of the circuit blocks based on the changes in the levels of these signals and on the timings thereof. The controller 290 includes a mode register 10, a command decoder 20, a timing generating circuit 30 and **a clock buffer 40**."), 26:59-61 ("**The clock signal CLK** is input to the clock synchronizing circuit 50 described above via the **clock buffer 40 thereby to generate an internal clock**"). The clock buffer also has a clock enable signal CKE as an input which determines the validity of the internal clock signal when CKE is active at a high level. *Id.* at 27:12-15 ("The **clock enable signal CKE** is for instructing the validity of the next clock signal. When the signal CKE has the high level, the rising edge of the next clock signal CLK becomes effective.").

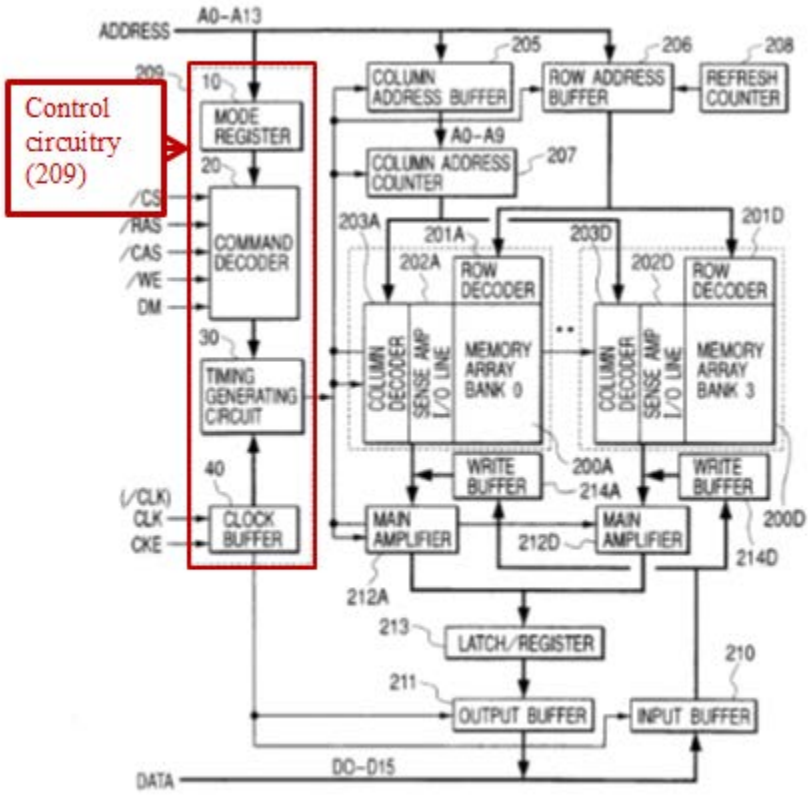
11.2.4. [17.3] "clock detection circuitry for detecting whether said clock enable signal is held inactive for a prescribed period of time in a low power operation mode; and"

Sakata discloses clock detection circuitry for detecting whether said clock enable signal is held inactive for a prescribed period of time in a low power operation mode. Specifically, Sakata discloses an internal circuit which forms a power-down signal PWD. *Id.* at 9:58-59 ("The internal circuit that is not shown forms a power-down signal PWD."). The internal circuit is the claimed "clock detection circuitry." The power-down signal is generated by the internal circuit when the clock enable signal CKE has been disabled for more than a predetermined period of time. *Id.* at 11:30-40 ("When it is judged that the signal CKE is of the low level for more than a predetermined period of time in the internal circuit, the power-down signal PWD is rendered to assume the high level."). Thus, the internal circuit detects "whether said clock enable signal is held inactive for a prescribed period of time in a low power operation mode" as claimed.

11.2.5. [17.4] "control circuitry for setting said buffer circuit and said clock buffer to an inactive state in response to a detection signal of said clock detection circuitry."

First, Sakata discloses control circuitry for setting said buffer circuit to an inactive state in response to a detection signal of said clock detection circuitry. Specifically, Sakata teaches that a controller 209 controls operation of the circuit

blocks in Figure 25, which circuit blocks include input buffer 210. *Id.* at 26:46-58 ("In FIG 25, though there is no particular limitation, a controller 209…forms internal timing signals for controlling the operation mode of the SDRAM and the operation of the circuit blocks…").



MICRON-1006, Sakata at Figure 25.

As discussed above with respect to the previous limitation, Sakata also discloses "clock detection circuitry" which generates a power-down signal PWD. *See* Section 11.2.5 claim [17.4] *supra*. Sakata describes that the power-down control signal PWD causes operation of the differential amplifier circuit to cease. MICRON-1006, Sakata at 11:21-29 ("As the power-down signal PWD changes

into the one of the high level…to cease the operation of the differential amplifier circuit…"). The differential amplifier circuit is the input buffer circuit disclosed in Sakata. *Id.* at 5:34-39 ("[T]he input buffer of the present invention uses the input circuit of the differential amplifier circuit type…"); *see* MICRON-1003, Baker Decl., Appx. A at claim [17.4].

Second, a person of ordinary skill in the art would have found that Sakata in view of Yukshing discloses and renders obvious control circuitry for setting said clock buffer to an inactive state in response to a detection signal of said clock detection circuitry. Sakata teaches generally that the consumption of current by the input circuit can be decreased in response to the PWD signal. *See* MICRON-1006, Sakata at 11:30-36. Although Sakata does not expressly disclose that the disclosed clock buffer is also set to an inactive state in response to the PWD signal, it would have been obvious to adapt Sakata to do so in do so in view of the teachings of Yukshing. Yukshing teaches that in order to save power in a synchronous memory device, both input buffers and clock buffers should be deactivated in response to a low power mode signal. MICRON-1007, Yukshing at 4:36-43 ("When the input buffers are OFF, however, such as when the ZZ 'sleep' signal is applied to SRAM 10 to generate an active control signal"), 4:15-24 ("Internal clock buffer/generator 18…is further arranged to discontinue generation of CLKI and CLKIB in response to the assertion of the disable signal by sleep control circuit 16…."), 7:36-48

("When in the low power mode, the only current being drawn by SRAM 10 is leakage current…"). It would have been obvious to disable the clock buffer in Sakata in view of the teachings in Yukshing at least for the reasons discussed above in Section 11.1.

Accordingly, a person of ordinary skill in the art would have found that Sakata in view of Yukshing discloses "control circuitry for setting said buffer circuit and said clock buffer to an inactive state in response to a detection signal of said clock detection circuitry." MICRON-1003, Baker Decl., Appx. A at claim [17.4].

11.3. Claim 18 is obvious over Sakata in view of Yukshing

11.3.1. [18.0] "The semiconductor device according to claim 17, wherein said semiconductor device is a clock synchronous semiconductor memory device operating in synchronization with said external clock signal, and"

Sakata discloses wherein said semiconductor device is a clock synchronous semiconductor memory device operating in synchronization with said external clock signal. Specifically, Sakata discloses a synchronous memory device which receives an external clock signal CLK. MICRON-1006, Sakata at 25:43-47 ("Fig. 25 is a block diagram illustrating the whole synchronous DRAM (hereinafter simply referred to as SDRAM) of about 64 megabits according to an embodiment of the present invention. Though there is no particular limitation on the SDRAM of this embodiment, there are shown a memory array 200A constituting a memory

bank 0 and a memory array 200D constituting a memory bank 3 among the four memory banks."), 26:46-48 ("[A] controller 209 represented by a dotted line receives external control signals such as clock signal CLK"). Sakata also discloses that an internal clock is generated from the external clock signal, and that the other external inputs to the memory device are synchronized in accordance with the rising edge of the internal clock. *Id.* at 26:59-67 ("The clock signal CLK is input to the clock synchronizing circuit 50 described above via the clock buffer 40 thereby to generate an internal clock. Though there is no particular limitation, the internal clock is used as a timing signal for activating the output buffer 211 and the input buffer 210, and is fed to the timing-generating circuit 30. Based on the clock signal, there is formed a timing signal fed to the column address buffer 205, row address buffer 206 and column address counter 207."), 27:1-2 ("The other external input signals are signified in synchronism with the rising edge of the internal clock signal."). Thus, because the external clock generates the internal clock, and the rest of the inputs of the memory device are synchronized with the internal clock, it follows that the memory device operates in synchronization with the external clock signal.

11.3.2. [18.1] "said low power operating mode is an operating mode in which access to said semiconductor memory device is ceased."

Sakata discloses said low power operating mode is an operating mode in which access to said semiconductor memory device is ceased. First, as discussed previously with respect to limitation [17.4], Sakata teaches generating a power-down signal which is a low power mode in which current consumption is decreased. *See* Section 11.2.5 claim [17.4] *supra*. Sakata also discloses that in the power-down mode, the operation of the input buffer is cut off and rendered inoperable. *Id.*; *see also* MICRON-1006, Sakata at 12:66-13:11, 13:12-31. In Sakata, the write signals are received through the input buffer, and accordingly, it would have been obvious to a person of ordinary skill in the art that, by deactivating the input buffer, write access to the memory device would cease. *Id.* at 25:14-15 ("A write signal input through the external terminal Din is received through the input buffer…"), 26:24-26 ("The write signal input through the external terminal is transmitted to the input terminals of the write buffers 214A, D through an input buffer 210."); MICRON-1003, Baker Decl., Appx. A at claim [18.1].

Similarly, regarding read access, Sakata teaches that the same input buffer circuit described for receiving write signals can be applied to the address input circuit. MICRON-1006, Sakata at 10:54-63 ("The above-mentioned input circuit

can be applied to an address input circuit that controls the operation in response to the operation mode, to the input circuit that receives control signals to the input circuit that receives the data. In the synchronous DRAM that will be described later, for example, the above-mentioned input circuit can be utilized except for the clock enable signals CKE that must be monitored concerning the state of input signals at all times."). Accordingly, it would have been obvious to one of ordinary skill in the art that read access to the memory device would also cease in the power-down mode disclosed in Sakata because read access is controlled by the address input circuit. MICRON-1003, Baker Decl., Appx. A at claim [18.1]. Thus, Sakata teaches "said low power operating mode is an operating mode in which access to said semiconductor memory device is ceased" as claimed.

11.4. Claim 19 is obvious over Sakata in view of Yukshing

11.4.1. [19.0] "The semiconductor device according to claim 17, wherein said clock detection circuitry comprises a circuit for deactivating said detection signal in response to activation of an external clock enable signal,"

One of ordinary skill in the art would have found it obvious that the internal clock detection circuit in Sakata would comprise, or could be modified to include, a circuit for deactivating the detection signal in response to an activation of an external clock enable signal. As explained by Dr. Baker, this limitation simply requires that when the device is no longer in a low power mode as signified by the clock enable signal being reactivated, the low power mode signal should be

deactivated. MICRON-1003, Baker Decl., Appx. A at claim [19.0]. Although Sakata does not discuss expressly that the PWD signal is deactivated in response to the CKE signal being reactivated, it would have been common sense to a person of ordinary skill in the art to do so.

In particular, as discussed previously with regards to limitations [17.3] and [17.4], Sakata discloses clock detection circuitry which forms a power-down signal PWD (the claimed "detection signal") when the clock enable signal is held inactive for a prescribed period of time. *See* Sections 11.2.4 claim [17.3] and 11.2.5 claim [17.4] *supra.* Sakata also discloses that the external clock enable signal determines the validity of the next clock cycle and is monitored at all times. MICRON-1006, Sakata at 27:12-13 ("The clock enable signal CKE is for instructing the validity of the next clock enable signal."), 10:58-63 ("In the synchronous DRAM…the clock enable signals CKE … must be monitored concerning the state of input signals at all times."). The activation of the CKE signal signifies that the clock signal is effective and when CKE is deactivated the clock signal is ineffective. *Id.* at 27:13-16 ("When the signal CKE has the high level, the rising edge of the next clock signal CLK becomes effective. When the signal CKE has the low level, the rising edge becomes ineffective."). A person of ordinary skill in the art would have thus understood and found it obvious that the reason that the CKE signal is still monitored during the low-power mode is to deactivate the PWD signal when the

device is no longer in the low power mode and to render the PWD signal inactive in response to a reactivation of the CKE signal. MICRON-1003, Baker Decl., Appx. A at claim [19.0].

Indeed, because the PWD signal (the claimed "detection signal") in Sakata controls the operability of the input buffers, the PWD signal must be deactivated for the input circuitry to function. *See* MICRON-1006, Sakata at 17:36-51 (discussing "returning from the power down in the input circuit"). Common sense would have thus dictated to a person of ordinary skill in the art that when the clock enable signal CKE is reactivated, the rising edge of the clock signal is rendered valid, and the internal circuitry must return to an operable state to receive external signals by disabling the PWD signal. MICRON-1003, Baker Decl., Appx. A at claim [19.0]. Thus, it would have been obvious to one of ordinary skill in the art that Sakata comprises, or could be modified to include, wherein said clock detection circuitry in response to activation of an external clock enable signal as claimed. *Id.*

11.4.2. [19.1] "said control circuitry deactivates an activation control signal in response to said detection signal and activates said activation control signal in response to said external clock enable signal [sic] said external clock signal, and"

Sakata in view of Yukshing discloses said control circuitry deactivates an activation control signal in response to said detection signal and activates said

activation control signal in response to said external clock enable signal. Specifically, Sakata discloses a chip select signal /CS which controls the start of the command input cycle. MICRON-1006, Sakata at 27:2-6. The chip select signal /CS is the claimed "activation control signal."

Sakata discloses that the chip select signal ("activation control signal") is activated,[5] i.e., rendered operable, in response to the external clock enable signal and external clock signal. Namely, Sakata discloses that external input signals such as the chip select signal operate on the rising edge of an internal clock signal. *Id.* at 26:59-61 ("The clock signal CLK is input to the clock synchronization circuit 50 described above via clock buffer 40 thereby to generate an internal clock."), 27:1-2 ("The other external input signals are signified in synchronism with the rising edge of the internal clock signal."), 26:46-56 ("a controller 209 represented by a dotted line receives external control signals such as clock signal CLK, clock enable signal CKE, chip select signal /CS…"). However, the edges of the internal clock signal are only operable when the clock enable signal is active at a high

[5] The 296 Patent describes, for example, that a chip select signal is "activated" or "deactivated" at an edge of the clock signal. MICRON-1001, 296 Patent at 14:44-47 ("This is because it is necessary to determine when said chip select signal CS is activated or deactivated at an edge of a clock signal…").

level. *Id.* at 27:12-15. Thus, the chip select signal ("activation control signal") is only activated, i.e. rendered operable, via the rising edge of the internal clock signal when the external clock enable signal is active.

Second, while Sakata does not expressly disclose that the chip select signal is deactivated, i.e., rendered inoperable, in response to the low power signal PWD (the claimed "detection signal" discussed above in Section 11.2.4 claim [17.3]), a person of ordinary skill in the art would have found it obvious to do so in view of Yukshing. Yukshing, like Sakata, discloses a chip select signal. MICRON-1007, Yukshing at 4:25-26 ("Input buffer 20 buffers a chip select signal, or as is also known, a chip enable signal, applied to interface pin 14_4."). Yukshing also discloses that in response to a low power signal, sleep mode signal ZZ, being asserted, control circuitry causes the chip select signal to be deactivated such that it appears that a non-active chip select signal is being applied to the internal circuitry. *Id.* at 6:62-7:2 ("[A]ssertion of the ZZ signal causes the input buffers of SRAM 10, particularly those associated with control signals, to produce a signal as if a nonactive signal was being applied externally. Of particular importance, the chip enable input signals…will be generated by the respective input buffers (e.g., buffer 20 in Fig. 1) as non-active signals."). When the low power mode is inactive, the memory device maintains a normal mode of operation. *Id.* at 6:21-38.

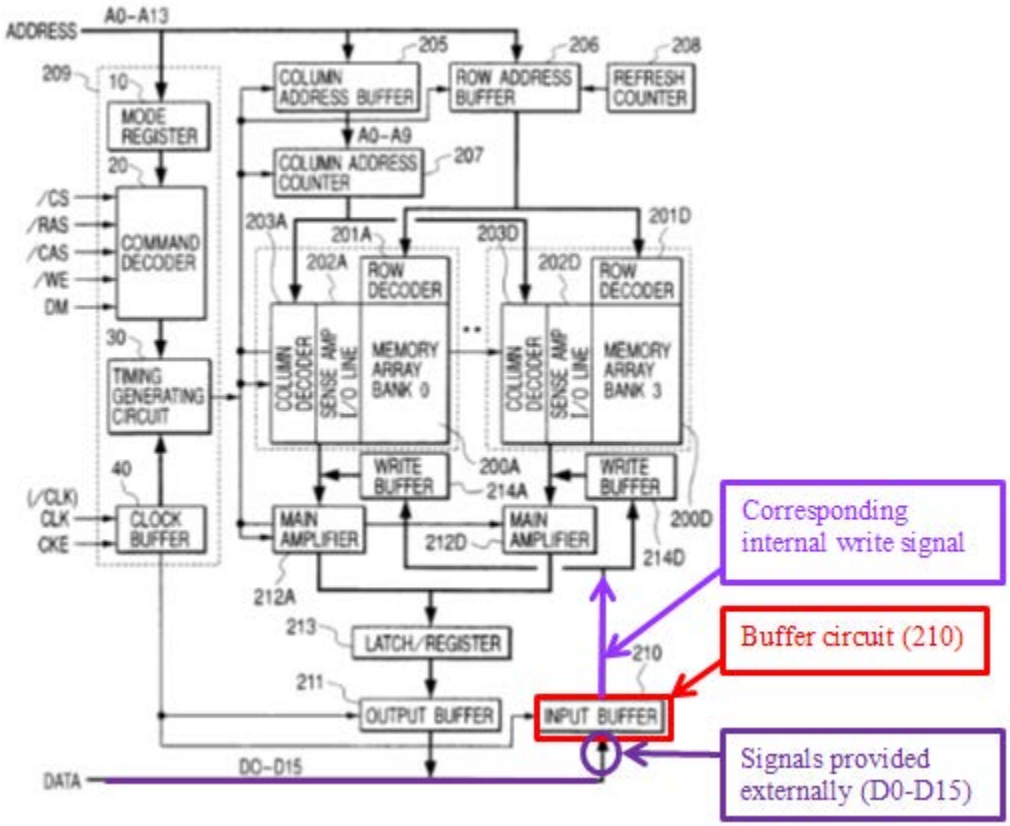
Thus, because Sakata discloses a chip select "activation control signal" which controls the command input cycle and is rendered operable in accordance with an external clock enable signal, and Yukshing discloses that a chip select signal can be deactivated in response to a low power signal such as the power down signal disclosed in Sakata, a person of ordinary skill in the art would have found it obvious based on Sakata in view of Yukshing, to use control circuitry to deactivate an activation control signal in response to said detection signal and activate said activation control signal in response to said external clock enable signal.

11.4.3. [19.2] "said buffer circuit and said clock buffer operate when said activation control signal is active and generate a corresponding internal signal according to a applied signal when active."

Sakata discloses said buffer circuit and said clock buffer operate when said activation control signal is active and generate a corresponding internal signal according to an applied signal when active. Specifically, Sakata discloses a chip select "activation control signal" (discussed in the previous limitation, *see* Section 11.4.2 claim [19.1]) which controls the command cycle of the memory device. A person of ordinary skill in the art would have understood and found it obvious that in order to operate a synchronous memory device for buffering a signal as disclosed in Sakata, the buffer circuit and the clock buffer would need to operate when the chip select signal was active. MICRON-1006, Sakata at 27:2-6 ("The

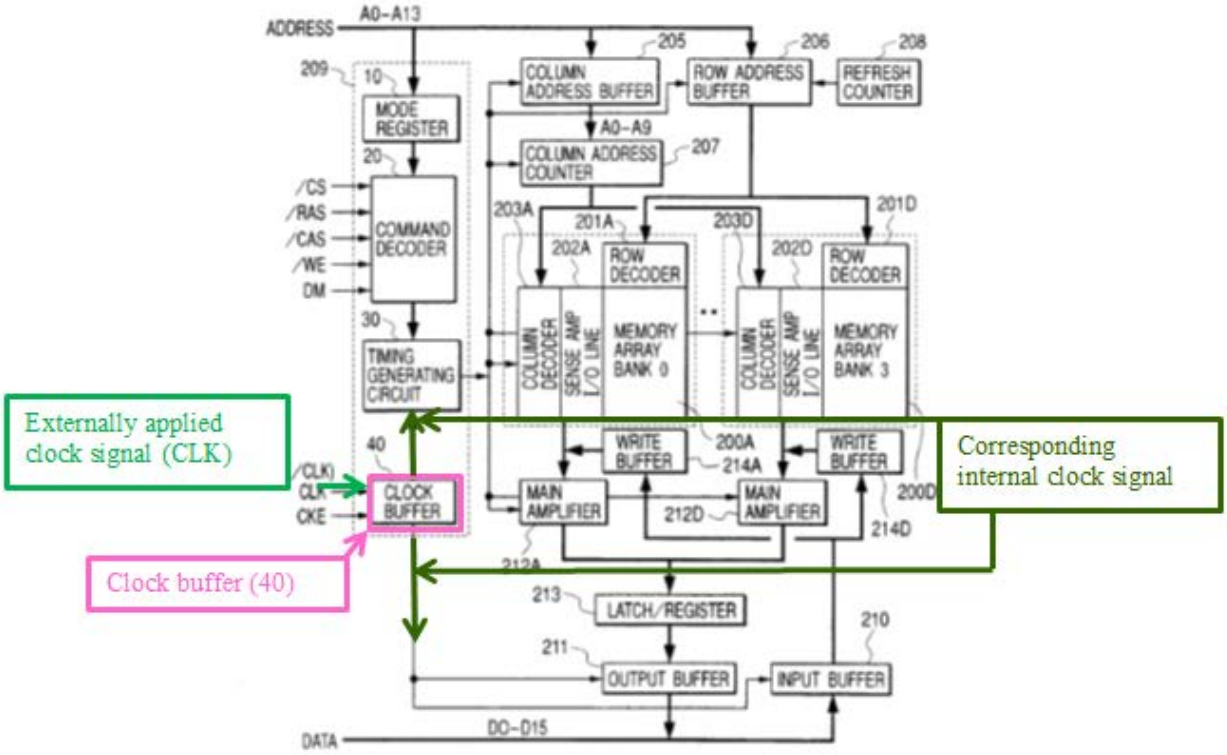
chip select signal /CS having the low level instructs the start of the command input cycle."); MICRON-1003, Baker Decl., Appx. A at claim [19.2]. The claimed buffer circuit and clock buffer are discussed above with respect to claim limitations [17.1] and [17.2]. *See* Sections 11.2.2 claim [17.1] and 11.2.3 claim [17.2] *supra*.

In addition, Sakata discloses that when the buffer circuit is active, it generates an internal write signal input according to externally applied data signals D0 to D15. MICRON-1006, Sakata at 26:24-28 ("The write signal input through the external terminal is transmitted to the input terminals of the write buffers 214A, D through an input buffer 210.").



MICRON-1006, Sakata at Figure 25 (annotated).

Similarly, when the clock buffer is active, it generates an internal clock signal according to external clock signal CLK. *Id.* at 26:59-61.



MICRON-1006, Sakata at Figure 25 (annotated).

11.5. Claim 20 is obvious over Sakata in view of Yukshing

11.5.1. [20.0] "The semiconductor device according to Claim 19, wherein said control circuitry deactivates said activation control signal according to said external clock enable signal when said external clock signal is at a first logical level."

Sakata discloses wherein said control circuitry deactivates said activation control signal according to said external clock enable signal when said external clock signal is at a first logical level. As discussed above with respect to claim limitation [17.4], Sakata discloses "control circuitry" 209 which receives external

control signals including a chip select "operation activation signal." *See* Section 11.2.5 claim [17.4] *supra*.

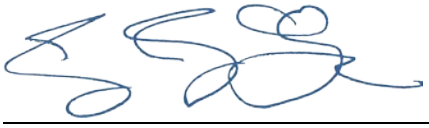
Additionally, Sakata discloses that the chip select signal is operated on the rising edge of an internal clock signal. MICRON 1006, Sakata at 27:1-6. Sakata also discloses that the validity of the rising edge of the internal clock signal is controlled by the external clock enable signal. *Id.* at 27:13-17. Accordingly, when the external clock enable signal is inactive, the operability of the chip select signal is deactivated because there is no valid rising edge of the internal clock signal. Furthermore, it would have been obvious to one of ordinary skill in the art that clock signals in synchronous memory devices as disclosed in Sakata would be a signal that oscillates between a logical high and a logical low level. MICRON-1003, Baker Decl., Appx. A at claim [20.0]. Thus, when the control circuitry deactivates the /CS signal, the external clock signal would inherently and obviously be at either a "high" or "low" logical level and thus at the claimed "first logical level." *Id.*

12. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1, 11, 12, and 17-20 of the 296 Patent is requested.

Respectfully submitted,

Dated: October 26, 2015

By: 

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	October 27, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 6,697,296 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1007
Persons served	Patent Owner's Address of Record: McDermott Will & Emery LLP The McDermott Building 500 North Capitol Street, N.W. Washington, DC 20001 Additional Address Known as Likely to Effect Service: Jon A. Birmingham Fitch Even Tabin & Flannery LLP 21700 Oxnard Street Suite 1740 Woodland Hills, CA 91367

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