UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

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Case IPR. No. Unassigned
U.S. Patent No. 6,233,181
Title: SEMICONDUCTOR MEMORY DEVICE
WITH IMPROVED FLEXIBLE REDUNDANCY SCHEME

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**Petition For *Inter Partes* Review of U.S. Patent No. 6,233,181 Under 35 U.S.C §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123**

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# 1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-7 of U.S Patent No. 6,233,181, titled "Semiconductor Memory Device With Improved Flexible Redundancy Scheme" (MICRON-1001, "the 181 Patent"), and cancel those claims as unpatentable.

# 2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

## 2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 181 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 181 Patent on the grounds identified herein.

## 2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

| **Lead Counsel** | **Back-Up Counsel** |
|---|---|
| Jeremy Jason Lang (Reg. No. 73604)<br>(jason.lang@weil.com)<br><br>Postal & Hand-Delivery Address:<br>Weil, Gotshal & Manges LLP<br>201 Redwood Shores Parkway<br>Redwood Shores, CA 94065<br>T: 650-802-3237; F: 650-802-3100 | Justin L. Constant (Reg. No. 66883)<br>(justin.constant@weil.com)<br><br>Postal & Hand-Delivery Address:<br>Weil, Gotshal & Manges LLP<br>700 Louisiana, Suite 1700<br>Houston, TX 77002<br>T: 713-546-5217; F: 713-224-9511 |

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for the Petitioner is attached.

### 2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

### 2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Limestone has asserted the 181 Patent and U.S. Patent Nos. 5,805,504 ("the 504 Patent"), 5,894,441 ("the 441 Patent"), 5,943,260 ("the 260 Patent"), and 6,697,296 ("the 296 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Limestone Memory Sys. LLC v. Micron Tech. Inc.*, 8:15-cv-00278 (C.D. Cal.) ("Co-Pending Litigation"). Limestone has also asserted one or more of the asserted patents in the following actions: *Limestone Memory Sys. LLC v. OCZ Storage Solutions, Inc.,* 8:15-cv-00658 (C.D. Cal.) (the 504, 441, 181 and 296 Patents); *Limestone Memory Sys. LLC v. PNY Techs., Inc.*, 8:15-cv-00656 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Lenovo (US) Inc.*, 8:15-cv-00650 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Kingston Tech. Co. Inc.*, 8:15-cv-00654 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Transcend Info., Inc. (California)*, 8:15-cv-00657 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Acer America Corp.*, 8:15-cv-00653 (C.D. Cal.) (the 504, 441, 260,

181, and 296 Patents); *Limestone Memory Sys. LLC v. Dell Inc.*, 8:15-cv-00648 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Hewlett-Packard Co.*, 8:15-cv-00652 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); and *Limestone Memory Sys. LLC v. Apple Inc.*, 8:15-cv-01274 (C.D. Cal.) (the 504, 441, 181, and 296 Patents).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 5,805,504, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 5,894,441, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 5,943,260, IPR2015-Unassigned (to be filed concurrently); and Petition for *Inter Partes* Review of U.S. Patent No. 6,697,296, IPR2015-Unassigned (to be filed concurrently).

The 181 Patent claims priority to foreign patent applications JP-10-160466 and JP-10-293421. The 181 Patent does not claim priority to any other U.S. patent applications. According to USPTO records, and to the best of Petitioner's knowledge, the following U.S applications and patents claim priority to the application that led to the issuance of the 181 Patent: U.S. Patent App. No. 09/798,944, filed on March 06, 2001, now U.S. Patent No. 6,449,199 (expired due to non-payment of maintenance fees); U.S. Patent App. No. 10/229,001, filed on

August 28, 2002, now U.S. Patent No. 6,545,931; and U.S. Patent App. No. 10/387,573, filed on March 14, 2003, now U.S. Patent No. 6,678,195. To the best of Petitioner's knowledge, the U.S. patents that claim priority to the 181 Patent have not been asserted in litigation and are not the subject of any co-pending USPTO proceedings.

### 2.5. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

### 2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 181 Patent is attached.

## 3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

**Ground #1:** Claims 1-2 and 6 of the 181 Patent are invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that they are obvious over U.S. Patent No. 5,487,040, to Sukegawa et al. ("Sukegawa"), entitled "Semiconductor Memory Device and Defective Memory Cell Repair Circuit," issued on January 23, 1996. Sukegawa is attached as MICRON-1005. This ground is explained below and is supported by the Declaration of Dr. R. Jacob Baker (MICRON-1007, "Baker Decl.").

**Ground #2:** Claim 3 of the 181 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Sukegawa in view of Betty Prince,

*Semiconductor Memories* (2d ed. 1992) ("Prince"). The excerpts produced at MICRON-1009 are from a copy of the Prince textbook that was stamped by the Library of Congress on March 26, 1992. This ground is explained below and is supported by the Baker Decl.

**Ground # 3**: Claim 4 of the 181 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Sukegawa in view of Prince. This ground is explained below and is supported by the Baker Decl.

**Ground # 4**: Claim 5 of the 181 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Sukegawa in view of U.S. Patent No. 4,967,397, to Walck ("Walck"), entitled "Dynamic RAM Controller," filed with the USPTO on May 15, 1989, issued October 30, 1990. Walck is attached as MICRON-1006. This ground is explained below and is supported by the Baker Decl.

**Ground #5**: Claim 7 of the 181 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Sukegawa in view of U.S. Patent No. 5,355,339, to Oh et al. ("Oh"), entitled "Row Redundancy Circuit of a Semiconductor Memory Device," filed with the USPTO on July 13, 1993, issued October 11, 1994. Oh is attached as MICRON-1010. This ground is explained below and is supported by the Baker Decl.

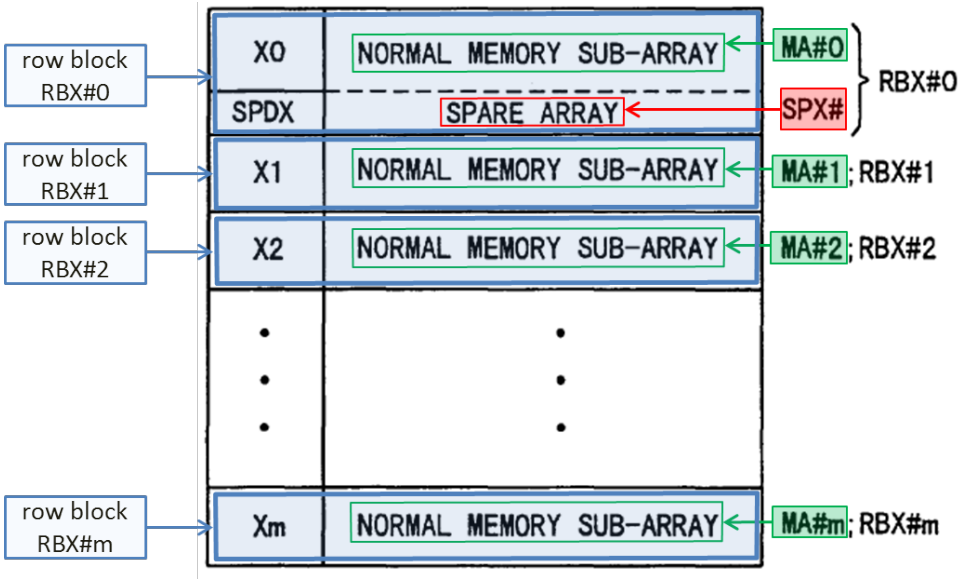
## 4. OVERVIEW OF THE 181 PATENT

The 181 Patent was filed on February 17, 1999, and claims priority to two Japanese patent applications, the earliest of which was filed on June 9, 1998. The 181 Patent issued on May 15, 2001. The 181 Patent relates generally to a semiconductor memory device having memory arrays that are further subdivided into a plurality of memory blocks, which themselves consist of a matrix of rows and columns of memory cells. MICRON-1001, 181 Patent at 1:7-9; MICRON-1007, Baker Decl. ¶¶ 33-41. More particularly, the 181 Patent concerns the replacement of defective memory cells in a memory block with spare memory cells. As was known in the art, when a memory cell becomes defective, the memory cell can be replaced with redundant—or spare—memory cells. *See*, *e.g.*, MICRON-1001, 181 Patent at 1:15-18 (describing the background of the art and stating that "a defective memory cell is replaced with a spare memory cell in order to equivalently repair the defective memory cell to raise the yield of the products").

The 181 Patent alleges, however, that prior art techniques provided spare word lines (extra rows of spare memory cells) or spare column/bit lines (extra columns of spare memory cells) in each memory block. MICRON-1001, 181 Patent at 1:28-38, 3:18-26; MICRON-1007, Baker Decl. ¶¶ 33-34. According to the 181 Patent, providing spare memory cells in each memory block resulted in inefficient use of the spare cells. MICRON-1001, 181 Patent at 3:58-67; *id.* at 4:1-

8. The 181 Patent purports to solve this alleged problem by disclosing a semiconductor device that has the ability to use spare memory cells in one memory block to replace defective memory cells in other blocks. MICRON-1001, 181 Patent at Abstract ("A spare memory array having spare memory cells common to a plurality of normal sub-arrays having a plurality of normal memory cells is provided. A spare line in the spare array can replace a defective line in the plurality of normal sub-array. The defective line is efficiently repaired by replacement in an array divided into blocks or sub-arrays."). *See also* MICRON-1007, Baker Decl. ¶ 35.

The claims are directed to an embodiment of the alleged invention that concerns repairing defective memory cells in a particular memory block within a group of memory blocks aligned in the column (vertical) direction. This is the third embodiment described in the 181 Patent, which is depicted in Figure 9 and described at 16:12-17:25. Figure 9 is reproduced below:




**MICRON-1001, 181 Patent at Figure 9 (annotated).**

The memory array in Figure 9 consists of row blocks RBX#0 to RBX#m, which are aligned in the column (vertical) direction. MICRON-1001, 181 Patent at 16:14-16. The row blocks RBX#1 to RBX#m are formed by "normal memory sub-arrays MA#1 to MA#m," which consist of normal memory cells arranged in a matrix of rows and columns. *Id.* at 16:16-19.

Row block RBX#0 includes a normal memory sub-array MA#0 with memory cells arranged in a matrix of columns and a spare array SPX# having spare memory cells arranged in a plurality of rows and sharing the columns with normal memory sub-array MA#0. *Id.* at 16:19-24. The "plurality of spare rows (spare word lines) included in spare array SPX# can replace defective normal word lines included in normal memory sub-arrays MA#0 to MA#m." *Id.* at 16:24-27; *see also id.* at 16:31-33 ("In the configuration shown in FIG. 9, spare array SPX#

is provided in common to normal memory sub-arrays MA#0 to MA#m."). The 181 Patent alleges that allowing the spare rows in SPX# to replace the memory cells in MA#0 to MA#m improves the efficiency with which the spare lines are used and simplifies the control operations when replacing defective memory cells. *See, e.g.*, *id.* at 16:33-39, 17:2-14.

**5. 181 PATENT PROSECUTION HISTORY**

The application that led to the issuance of the 181 Patent was originally filed with 20 claims. MICRON-1002, 181 Patent File History, 2-17-1999 Original Claims at .140-.147. Subsequently, following a restriction requirement, the Applicant elected the species of Figure 9, which corresponded to original claims 4-6. *Id.*, 2-10-2000 Response to Election Requirement at .452.

The Examiner subsequently issued a non-final rejection finding claims 1-3 anticipated by the disclosure of two prior art references: (1) Figures 3A and 3B of U.S. Patent No. 5,761,138 ("Lee") (MICRON-1003); and (2) Figure 3 of U.S. Patent No. 5,892,718 ("Yamada") (MICRON-1004). *Id.*, 4-12-2000 Non-Final Rejection at .456.

In a 10-11-2000 Amendment, the Applicant made several amendments to the claims. Notably, the Applicant amended claim 1 to require that the plurality of first memory blocks were aligned in the column direction. *See id.*, 10-11-2000 Amendment at .460-.461. The Applicant also added dependent claims 21-24. For

reference, the following is a table listing the original claim numbers and issued claim numbers:

| **Original Claim** | **Issued Claim** |
|---|---|
| 4 | 1 |
| 5 | 2 |
| 6 | 3 |
| 21 | 6 |
| 22 | 7 |
| 23 | 4 |
| 24 | 5 |

For ease of reference, this Petition refers to the claims by their issued claim number. In the remarks, the Applicant asserted that claim 1 "recites that (a) the first memory blocks are aligned in the column direction, and (b) each row of the plurality of first spare memory cells are [sic] capable of replacing a defective row including a defective normal memory cell in the plurality of first memory blocks." *Id.* at .464 (underline in original). The Applicant further stated that these features are shown in Figure 9. *Id.* With respect to Lee (MICRON-1003), the Applicant argued that Figures 3A and 3B disclosed a redundant memory cell array that could replace memory cells in a plurality of arrays aligned in the **row** direction, but did not disclose redundant memory cells that could replace memory cells in a plurality of arrays aligned in the **column** direction. *Id.* at .464-.465. With respect to Yamada (MICRON-1004), the Applicant argued that claim 1 requires "'a plurality of first spare memory cells arranged in a matrix of rows and columns in a

particular one of said plurality of first memory blocks,'" explaining that Figure 9 "shows spare array SPX# arranged in a particular one (normal memory sub-array MA#0) of the first memory blocks (MA#1-MA#m)." *Id.* at .465. The Applicant further argued that Yamada did not teach an array of spare memory cells within a particular one of the first memory blocks and further did not teach memory blocks aligned in the column direction. *Id.* at .465-.467. Subsequently, the Examiner allowed claims 1-7. *Id.*, 1-16-2011 Notice of Allowability at .473.

## 6. CLAIM CONSTRUCTION[1]

### 6.1. Applicable Law

A claim subject to *inter partes* review is given the "broadest reasonable construction in light of the specification of the patent in which it appears."[2] 37

[1] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 181 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 181 Patent.

[2] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the

C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

### 6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill in the art and consistent with the specification of the 181 Patent. Petitioner respectfully submits that the following terms shall be construed for this IPR:

#### 6.2.1. "word lines" (claims 1-7)

The term "word lines" is a limitation of claim 1 of the 181 Patent, and thus is also a limitation of dependent claims 2-7. Specifically, claim 1 requires "a plurality of first memory blocks each having a plurality of first normal memory cells arranged in a matrix of rows and columns, each of said plurality of first memory blocks including **word lines** provided corresponding to said rows."

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invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

MICRON-1001, 181 Patent at Claim 1. As Dr. Baker opines, in the semiconductor industry, the terms "row line" and "word line" were interchangeable and were well understood to refer to conductive materials that run horizontally through a memory device and connects multiple memory cells into a physical row. *See* MICRON-1007, Baker Decl. ¶ 55 (citing MICRON-1009, Prince[3] at .024, .029).

Thus, a person of ordinary skill in the art would have understood the plain and ordinary meaning of this term in the context of the 181 Patent to mean a "**conductive materials that run horizontally through a memory device that connect memory cells in a physical row**. *Id.* at ¶ 56.

**6.2.2. "spare memory cells" (claims 1-7)**

The term "spare memory cells" is a limitation of independent claim 1 of the 181 Patent, and thus is also a limitation of dependent claims 2-7. Specifically, claim 1 requires "a plurality of first **spare memory cells** arranged in a matrix of rows and columns in a particular one of said plurality of first memory blocks."

[3] As Dr. Baker explains, the Prince textbook was a well-known resource in the field of semiconductor memory devices. *See* MICRON-1007, Baker Decl. ¶ 23. The excerpts produced at MICRON-1009 are from a copy of the textbook that was stamped by the Library of Congress on March 26, 1992. *See* MICRON-1009, Prince at .005.

MICRON-1001, 181 Patent at Claim 1. The 181 Patent describes spare memory cells as memory cells that are capable of replacing defective normal memory cells:

> Row block RBX0 includes a normal memory sub-array MA#0 having normal memory cells arranged in a matrix of rows and columns, and a spare array SPX# having spare memory cells arranged in a plurality of rows and sharing the columns with normal memory sub-array MA#0. The plurality of spare rows (spare word lines) included in spare array SPX# can replace defective normal word lines included in normal memory sub-arrays MA#0 to MA#m.

MICRON-1001, 181 Patent at 16:19-27. Thus, a person of ordinary skill in the art would have understood the plain and ordinary meaning of this term in the context of the 181 Patent to mean "**memory cells capable of replacing defective memory cells.**" MICRON-1007, Baker Decl. ¶¶ 57-58.

**6.2.3. "sense amplifier bands" (claims 3 and 5)**

The term "sense amplifier band(s)" is a limitation of dependent claim 3 of the 181 Patent, and thus is also a limitation of dependent 5 (which depends from claim 3). Specifically, claim 3 requires "a plurality of **sense amplifier bands** provided between each of said plurality of first memory blocks and each of said second memory blocks, and shared by adjacent memory blocks in the column direction for sensing and amplifying data in each column of the adjacent memory block including a selected memory cell when activated." MICRON-1001, 181 Patent at Claim 3. When describing the embodiment of Figure 9 of the 181 Patent,

the 181 Patent specification discusses sense amplifiers but does not expressly define the term "sense amplifier band." *See id.* at 17:10-14.

The specification does make clear, however, that "band" refers to a plurality of sense amplifiers along the horizontal direction of a block (either on one end of the block, top or bottom, or in between two blocks). *See, e.g.*, MICRON-1001, 181 Patent at Figures 11, 14, 15, 20, 17:42-48. They are in the horizontal direction because they reside along the termination points of bit lines (which run orthogonal to the horizontal direction) to sense and restore contents of memory cells. *See* MICRON-1007, Baker Decl. ¶¶ 59-60.

As Dr. Baker opines, the term "sense amplifier" was understood to a person of ordinary skill in the art to mean an amplifier that senses the contents of memory cells and restores (amplifies) them to full levels. *See* MICRON-1007, Baker Decl. ¶ 60 (citing MICRON-1009, Prince at .037). Thus, a person of ordinary skill in the art would have understood the plain and ordinary meaning of this term in the context of the 181 Patent to mean "**amplifiers along the horizontal direction that sense the contents of memory cells and restore (amplify) them to full levels.**" *Id.* at ¶ 61.

## 7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 181 Patent would be a person with a Bachelor of Science degree in electrical

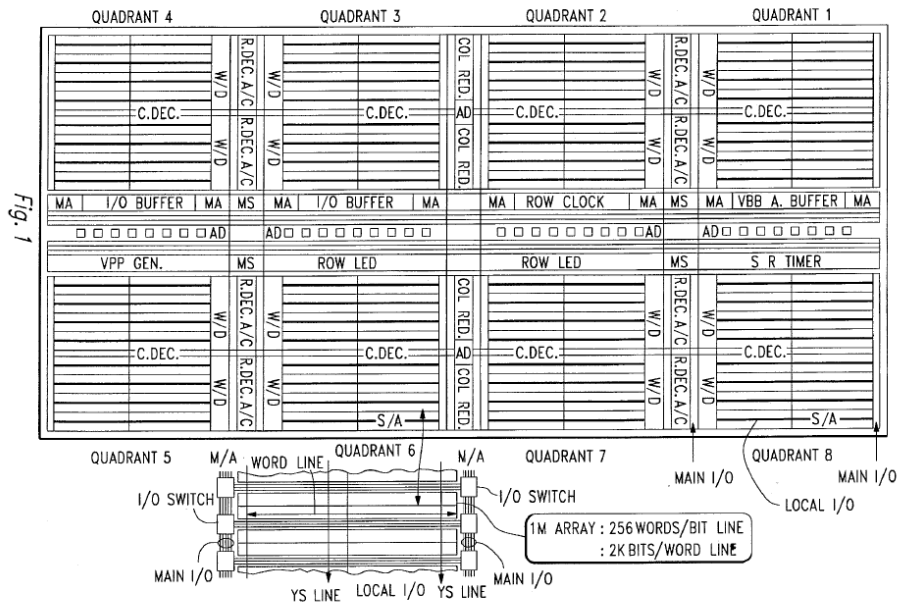
engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design of memory devices. An individual with an advanced degree in a relevant field would require less experience in the design of memory devices. MICRON-1003, Baker Decl. at ¶ 17.

## 8. DESCRIPTION OF THE PRIOR ART

### 8.1. U.S. Patent No. 5,487,040 ("Sukegawa")

U.S. Patent No. 5,487,040 ("Sukegawa") (MICRON-1005) was filed on July 12, 1993, and claims priority to a Japanese patent application filed on July 10, 1992. Sukegawa issued on January 23, 1996, to Shunichi Sukegawa and Tetsuya Saeki and is entitled "Semiconductor Memory Device and Defective Memory Cell Repair Circuit." The original assignees of Sukegawa were Texas Instruments Incorporated and Hitachi Ltd. Sukegawa is prior art to the 181 Patent under (pre-AIA) 35 U.S.C. § 102(b) because the patent issued more than one year before the earliest application to which the 181 Patent claims priority was filed.

Sukegawa discloses a semiconductor memory device having eight memory arrays, each of which is further subdivided into eight memory blocks aligned in the column direction. *See* MICRON-1005, Sukegawa at 1:38-54. The eight memory arrays are shown in the eight "Quadrants" of Figure 1 of Sukegawa.




**MICRON-1005, Sukegawa at Figure 1.**

Figure 8 of Sukegawa shows the structure of the memory array in each Quadrant, which includes eight memory blocks aligned vertically. *See* MICRON-1005, Sukegawa at 5:50-54.

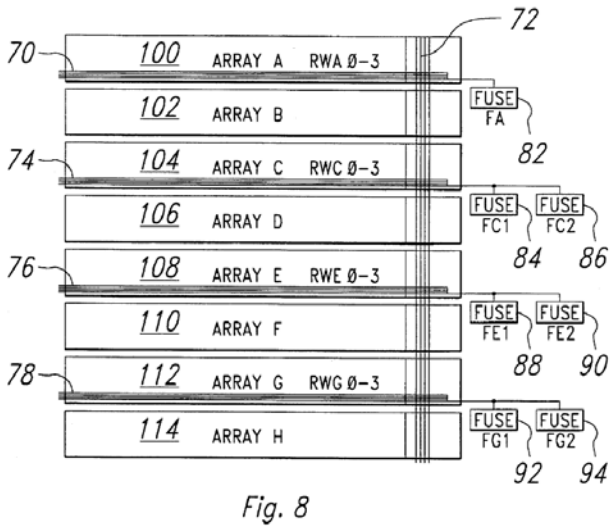



Fig. 8

**MICRON-1005, Sukegawa at Figure 8.**

In Figure 8, spare word line groups 70, 74, 76, and 78 run horizontally. As the spare word lines run horizontally in the figure, the column lines (which are not shown) run vertically. Thus, because the memory blocks are all aligned vertically, they are aligned in the column direction. Sukegawa discloses that (1) each memory block in a memory array may have row redundant (spare) memory, as described at 3:34-43 and 5:53-54; or (2) alternatively, as described in claim 1 and shown in Figure 8, "at least some" of the memory blocks in a memory array may have row redundant (spare) memory. As Dr. Baker opines, a person of ordinary skill in the art would have understood the terms "spare" and "redundant" to be synonymous. MICRON-1007, Baker Decl. ¶ 65. Thus, like the 181 Patent, Sukegawa discloses memory blocks aligned in the column direction, at least some of which contain spare memory cells.

Sukegawa further discloses an "any to any" redundancy scheme that allows any row of redundant memory cells in a particular memory block to be used to replace the defective memory in any other block, including blocks that are aligned in the column direction. MICRON-1005, Sukegawa at 3:34-43 (disclosing that the invention may include "multiple redundant word line groups placed in each memory block" and "a redundant mechanism which can be programmed to use the redundant memory to replace the defective memory in any other memory block");

*id.* at 2:21-59 (disclosing that all of the "redundant rows present in one quadrant can be allotted selectively to all quadrants, including the present quadrant").

Thus, just like the 181 Patent, Sukegawa discloses that spare memory in a particular memory block may be utilized to replace defective memory cells in other blocks aligned in the column direction. More details concerning the disclosures of Sukegawa, and how those disclosures teach the respective elements of the challenged claims, are provided below.

**8.2. U.S. Patent No. 4,967,397 ("Walck")**

U.S. Patent No. 4,967,397 ("Walck") (MICRON-1006) was filed on May 15, 1989. Walck issued on October 30, 1990, to Jeffrey A. Walck and is entitled "Dynamic RAM Controller." The original assignee of Walck was Unisys Corporation. Walck is prior art to the 181 Patent under (pre-AIA) 35 U.S.C. § 102(b) because the patent issued more than one year before the earliest application to which the 181 Patent claims priority was filed.

Walck discloses a semiconductor memory device, namely a DRAM device that includes a controller. MICRON-1006, Walck at Abstract. The DRAM of Walck includes multiple banks (arrays within the DRAM). *Id.* at 1:10-15, Figure 1. Walck discloses that in normal operation, it was conventional in such memories to access each bank independently (one at a time). *Id.* at 1:44-48. But in refresh mode, it was conventional to access all banks simultaneously. *Id.* Walck discloses

DRAM controller circuitry to either access each bank independently or to access all banks simultaneously. *Id.* at 1:56-67.

### 8.3. Betty Prince, *Semiconductor Memories* (2d ed. 1992)

As Dr. Baker explains, Betty Prince, *Semiconductor Memories* (2d ed. 1992) ("Prince") was a well-known resource in the field of semiconductor memory devices. *See* MICRON-1007, Baker Decl. ¶ 23. The excerpts produced at MICRON-1009 are from a copy of the textbook that was stamped by the Library of Congress on March 26, 1992. *See* MICRON-1009, Prince at .005. Thus, Prince is prior art to the 181 Patent under (pre-AIA) 35 U.S.C. § 102(b) because it was publicly available at least by the middle of 1992, which is more than one year before the earliest application to which the 181 Patent claims priority was filed. Particular disclosures of Prince relevant to the challenged claims are discussed below.

### 8.4. U.S. Patent No. 5,355,339 ("Oh")

U.S. Patent No. 5,355,339 ("Oh") (MICRON-1010) was filed on July 13, 1993. Oh issued on October 11, 1994, to Seung-Cheol Oh and Moon-Gone Kim and is entitled "Row Redundancy Circuit of a Semiconductor Memory Device." The original assignee of Oh was Samsung Electronics Co. Oh is prior art to the 181 Patent under (pre-AIA) 35 U.S.C. § 102(b) because the patent issued more

than one year before the earliest application to which the 181 Patent claims priority was filed.

Oh discloses a semiconductor memory device with a redundant mechanism that allows for replacement of defective memory cells with spare memory cells. MICRON-1010, Oh at Abstract. Oh discloses that the semiconductor memory device includes a plurality of normal submemory arrays. *Id.* The "submemory arrays" described in the abstract are also referred to as "memory cell arrays" in the specification. *See, e.g., id.* 4:64-5:1. Oh discloses that the redundancy technique allows any redundant address decoder to be utilized with any of the arrays, which "maximizes efficiency in redundant repairs as well as maximizes the use of the chip area." *Id.* at Abstract. An object of the disclosed mechanism is to "repair[]word line failures occurring in different normal memory cell arrays using spare word lines within one redundant memory cell array." *Id.* at 3:6-10. Further, Oh discloses that spare word lines are provided in a single memory cell array and that other memory cell arrays have no spare word lines. *Id.* at 3:15-18. Particular disclosures of Oh relevant to the challenged claims are discussed below.

## 9. GROUND #1: CLAIMS 1-2 AND 6 OF THE 181 PATENT ARE UNPATENTABLE AS OBVIOUS OVER SUKEGAWA

As explained below, claims 1-4 and 6 of the 181 Patent are unpatentable as obvious over Sukegawa under 35 U.S.C. § 103(a).

### 9.1. Claim 1 is obvious over Sukegawa

**9.1.1. [1.P] A semiconductor memory device, comprising:**

Sukegawa describes a semiconductor memory device with a decoder that is reduced in size, thereby reducing the chip size without reducing the chip's ability to replace defective memory cells. *See* MICRON-1005, Sukegawa at Abstract ("To provide a type of **semiconductor memory device**[4] characterized by the fact that the area occupied by the redundant memory address decoder on the chip is minimized without reducing the redundancy of the defective memory, and hence the cost of the semiconductor memory device can be cut."); *id.* at 7:47-57 (disclosing a "semiconductor IC"). The exemplary semiconductor memory device in Sukegawa is a "64M bits dynamic random access memory chip known as 64M DRAM" (*id.* at 1:39-40) shown in Figure 1.

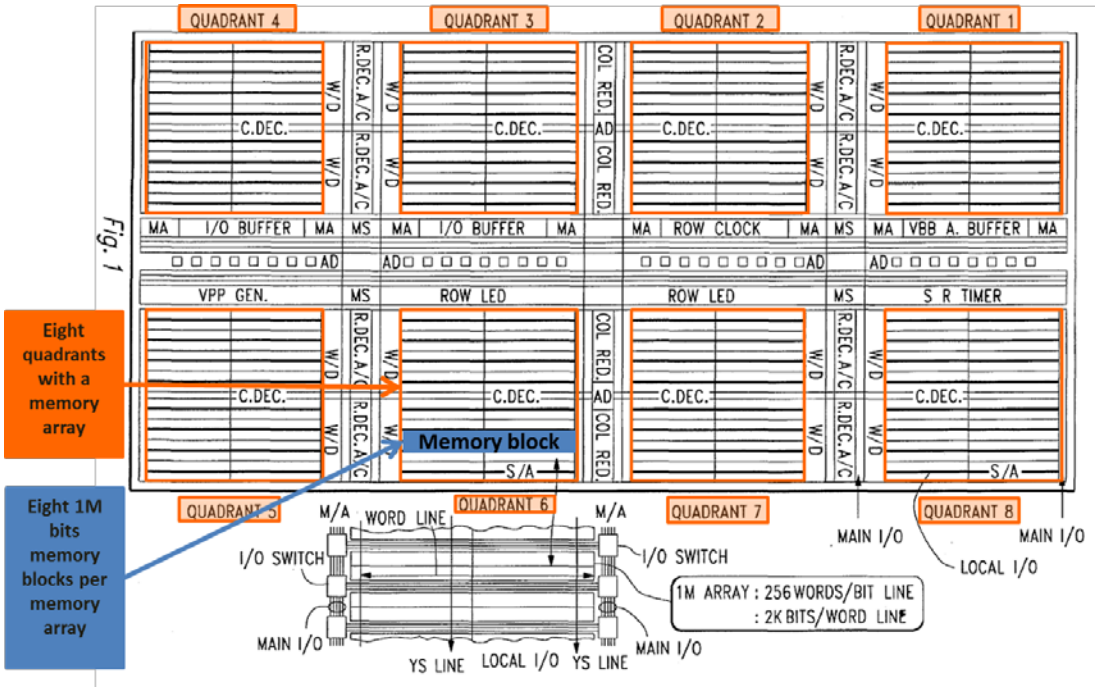
**Thus, Sukegawa discloses a semiconductor memory device (the semiconductor memory device shown in Figure 1).** *See also* MICRON-1007, Baker Decl. App'x A at claim element [1.P].

**9.1.2. [1.1a] a plurality of first memory blocks**

Figure 1 of Sukegawa depicts a 64M bits dynamic random access memory (DRAM) chip that is equally divided into eight quadrants of 1M bits. In Sukegawa, each quadrant has a memory array that is further subdivided into **eight**

[4] All emphases are added unless otherwise stated.

**1M bits memory blocks.** MICRON-1005, Sukegawa at 1:39-54 (disclosing that "[e]ach of the eight memory quadrants contains **eight 1M bits memory blocks**").




**MICRON-1005, Sukegawa at Figure 1 (annotated).**

The arrangement of the memory blocks in each quadrant is shown in Figure 8. *Id.* at 5:50-53 ("FIG. 8 shows the redundant mechanism. In the redundancy programming, the memory quadrant has **8 blocks of 1 M bits memory arrays**, each of which is divided into two 512K bits portions.").

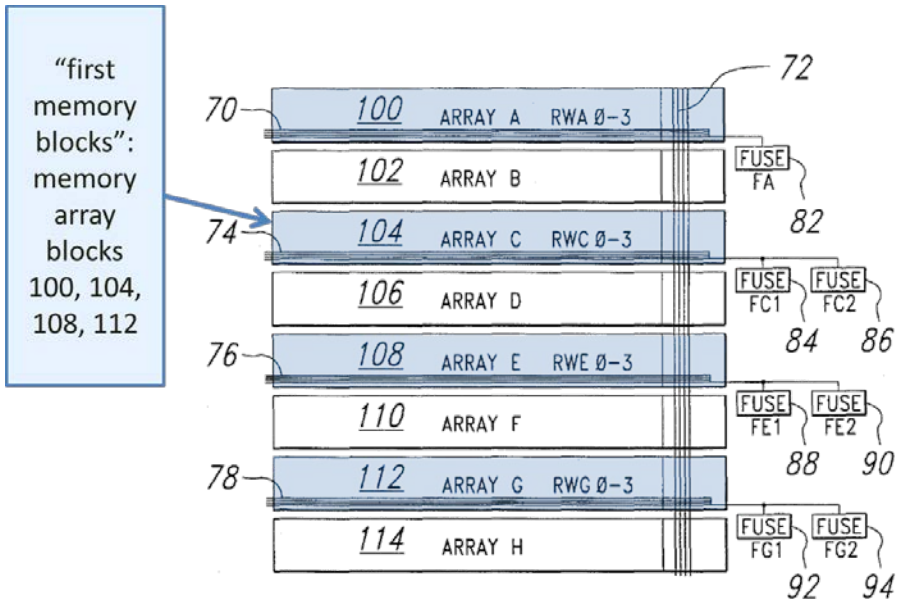


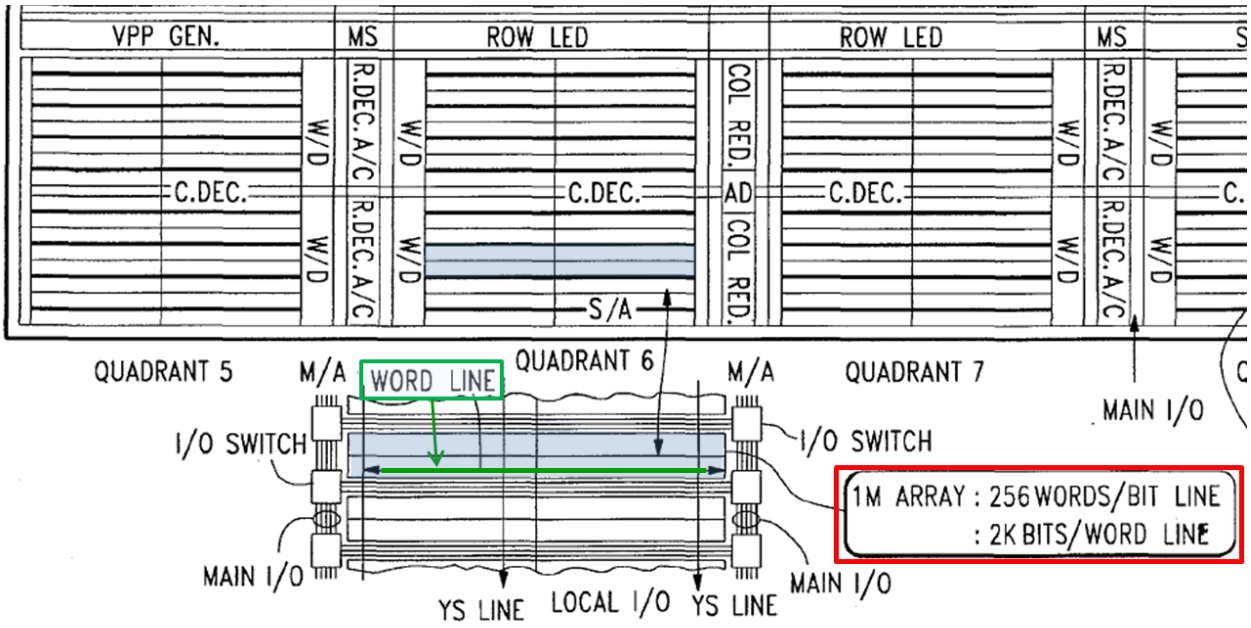

*Fig. 8*

**MICRON-1005, Sukegawa at Figure 8 (annotated).**

In Figure 8, the memory blocks are items 100, 102, 104, 106, 108, 110, 112, and 114, respectively. For the purposes of this claim element, the **plurality of first memory blocks in Figure 8 may be memory blocks 100, 104, 108, and 112.** *See also* MICRON-1007, Baker Decl. App'x A at claim element [1.1a]. It would have been obvious to one of ordinary skill in the art that the first plurality of memory blocks may include memory blocks 100, 104, 108, and 112. *See id.*

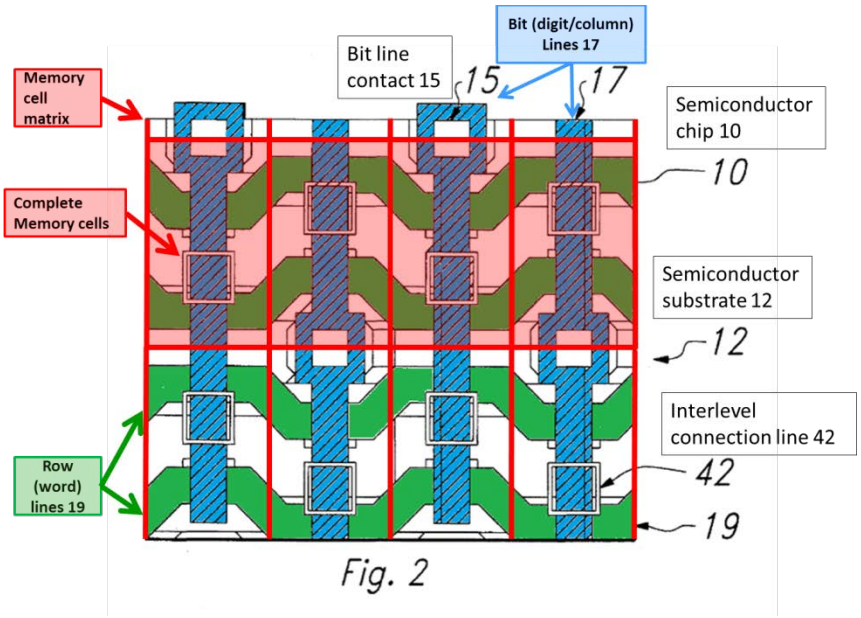
#### 9.1.3. [1.1b] each having a plurality of first normal memory cells arranged in a matrix of rows and columns,

In Figure 1, Sukegawa illustrates a "Word Line" of a particular memory block.




**MICRON-1005, Sukegawa at Figure 1 (annotated excerpt).**

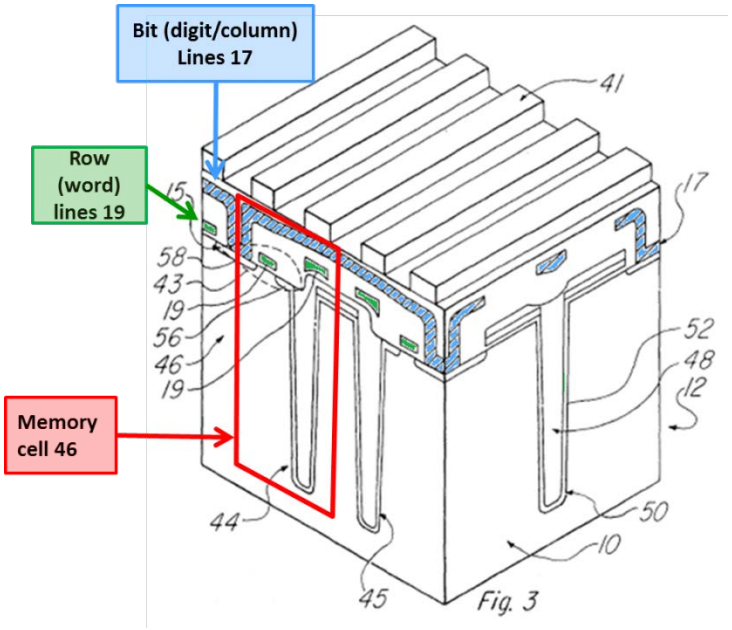
The bit lines are not shown in Figure 1, but would run parallel to the "YS LINES" and perpendicular to the Word Lines shown in the figure. The memory cells are roughly located at the intersection of every other intersection of a word line and bit line described in Figure 1. This forms a matrix of rows and columns of memory cells. *See* MICRON-1007, Baker Decl. App'x A at claim element [1.1b]. The structure of the matrix of memory cells is further illustrated in Figure 2, which shows a plane view of a portion of the memory array:




**MICRON-1005, Sukegawa at Figure 2 (annotated).**

> FIG. 2 is a plane view showing a portion of the memory array 12. Memory cells of memory array 12 are of the improved trench capacitor type made using submicron technology. The **memory cell has an area of about 4.8 μm$^2$, and is placed for every two word lines**. **Bit lines 17 are made of 3-layer polycide** for improving the tolerance with respect to noise. **Word lines 19 are made of polysilicon**, and a word line is connected for every 64 bits. In the prior art, redundant circuits were introduced for repairing the defective memory array.

MICRON-1005, Sukegawa at 1:55-64. The structure of the memory cell is further illustrated in Figure 3, which is an oblique view of a portion of the memory array:




**MICRON-1005, Sukegawa at Figure 3 (annotated).**

> FIG. 3 is an oblique view illustrating a portion of memory array 12. **Bit line 17 is connected to the each memory cells and is insulated from word line 19** by an interlayer insulating oxide layer. Word line 19 has a submicron width of about 0.6 μm. Word line 19 forms the gate of transfer gate 43. It is isolated from substrate 10 by means of a thin oxide layer. Other word lines 19, 19 pass through over upper trench capacitors 44, 45, and are connected to the other trench capacitors not shown in the figure. They are isolated from polysilicon field plate 48 by means of an oxide layer. **The gate portion of word line 19, source 56 and drain 58 form transfer gate 43** … **Transfer gate 43 and trench capacitor 44 form memory cell 46**.

*Id.* at 1:65-2:15. In addition, the specification discloses that each memory block comprises a plurality of first normal memory cells arranged in a matrix of rows and columns. *See id.* at 4:45-63 (disclosing that "the memory device consists of

multiple memory arrays which have memory cells arranged in a matrix configuration and have a redundant group for replacing the defective row groups …"). **Thus, Sukegawa discloses that each of the plurality of first memory blocks (memory blocks 100, 104, 108, and 112 in Figure 8) have a plurality of first normal memory cells arranged in a matrix of rows and columns**. *See also* MICRON-1007, Baker Decl. App'x A at claim element [1.1b].

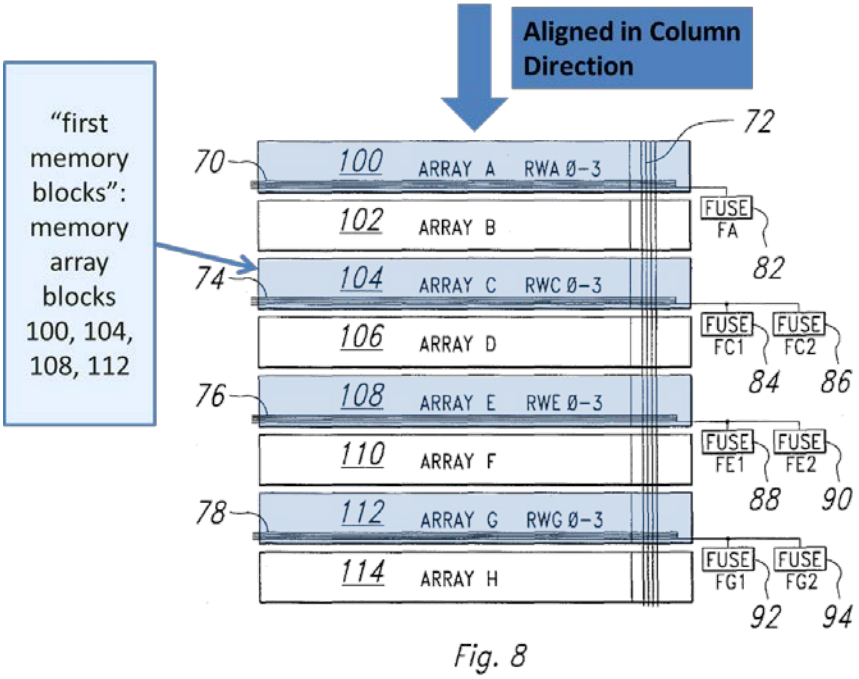
#### 9.1.4. [1.1c] each of said plurality of first memory blocks including word lines provided corresponding to said rows, respectively,

As discussed in Section 6 of this Petition, a person of ordinary skill in the art would have understood "word lines" to mean "conductive materials that run horizontally through a memory device that connect memory cells in a physical row." As described above with respect to Figures 1-3 of Sukegawa, each memory block includes word lines corresponding to the rows of memory cells. *See* Section 9.1.3, claim element [1.1b].

**Thus, Sukegawa discloses that each of said plurality of first memory blocks (memory blocks 100, 104, 108, and 112 in Figure 8) includes word lines provided corresponding to said rows of memory cells.** *See also* MICRON-1007, Baker Decl. App'x A at claim element [1.1c].

#### 9.1.5. [1.1d] and the first memory blocks aligned in the column direction; and

In Figure 8 of Sukegawa, the identified "first memory blocks"—i.e., blocks 100, 104, 108, and 112—are aligned vertically:




**MICRON-1005, Sukegawa at Figure 8 (annotated).**

In Figure 8, the bit/column lines corresponding to the memory cells in the memory blocks are not shown, but would run perpendicular to the redundant word line groups (70, 74, 76, and 78) that run horizontally in Figure 8. *See* Section 9.1.3, claim element [1.1b]. Thus, because the column lines run vertically, first memory blocks 100, 104, 108, and 112 are aligned in the column direction.

**Thus, Sukegawa discloses that the plurality of first memory blocks (memory blocks 100, 104, 108, and 112 in Figure 8) are aligned in the column direction**. *See also* MICRON-1007, Baker Decl. App'x A at claim element [1.1d].

### 9.1.6. [1.2a] a plurality of first spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of first memory blocks,

As discussed in Section 6 of this Petition, a person of ordinary skill in the art would have understood "spare memory cells" to mean "memory cells capable of replacing defective memory cells." As discussed in Section 8 of this Petition and Section VIII of Dr. Baker's declaration, the combined teachings of Sukegawa disclose to a person of ordinary skill in the art that (1) each memory block in a memory array may have row redundant (spare) memory, as described at 3:34-43 and 5:53-54; or (2) alternatively, as described in claim 1 and shown in Figure 8, "at least some" of the memory blocks in a memory array may have row redundant (spare) memory. In Figure 8, first memory blocks 100, 104, 108, and 112 include a redundant word (row) line groups 70, 74, 76, and 78, which are spare memory cells arranged in a matrix of rows and columns in each of the first memory blocks:

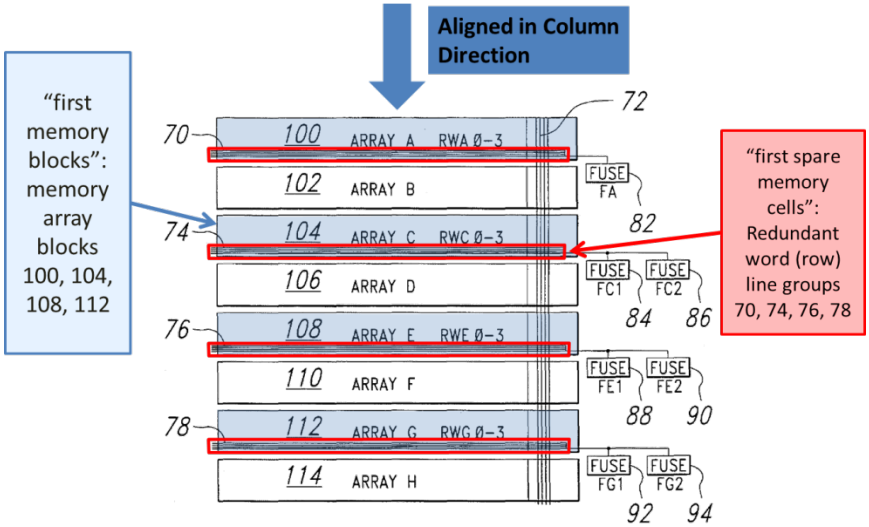



*Fig. 8*

**MICRON-1005, Sukegawa at Figure 8 (annotated).**

Thus, it would have been obvious in view of Sukegawa that a plurality of first spare memory cells (the memory cells formed by redundant word (row) line groups 70, 74, 76, and 78) are arranged in a matrix of rows and columns in each of the first memory blocks (memory blocks 100, 104, 108, and 112 in Figure 8). **For the purposes of this claim element, the "particular" first memory block may be block 100, and the plurality of first spare memory cells may be redundant word (row) line group 70**. *See also* MICRON-1007, Baker Decl. App'x A, at claim element [1.2a].

**9.1.7. [1.2b] each row of said plurality of first spare memory cells being capable of replacing a defective row including a defective first normal memory cell in said plurality of first memory blocks.**

As discussed in Section 6 of this Petition, a person of ordinary skill in the art would have understood "spare memory cells" to mean "memory cells capable of replacing defective memory cells." Sukegawa discloses an "any to any" redundancy scheme that allows any row of redundant memory cells in a particular memory block to be used to replace the defective memory in any other block, including blocks that are aligned in the column direction. *See* MICRON-1005, Sukegawa at 3:34-43 (disclosing that the invention may include "multiple redundant word line groups placed in each memory block" and "a redundant mechanism which can be programmed to use the redundant memory to replace the

defective memory in any other memory block"); *id.* at 2:21-59 (disclosing that all the "redundant rows present in one quadrant can be allotted selectively to all quadrants, including the present quadrant").

**Thus, Sukegawa discloses that each row of said plurality of first spare memory cells (redundant word (row) line group 70) in memory block 100 is capable of replacing a defective row including a defective first normal memory cell in any one of said plurality of first memory blocks (memory blocks 100, 104, 108, and 112 in Figure 8).** *See also* MICRON-1007, Baker Decl. App'x A at claim element [1.2b].

### 9.2. Claim 2 is obvious over Sukegawa

#### 9.2.1. [2.P] The semiconductor memory device as recited in claim 1, further comprising:

Sukegawa discloses the semiconductor memory device as recited in claim 1. *See* Section 9.1. *See also* MICRON-1007, Baker Decl. App'x A at claim element [2.P].

#### 9.2.2. [2.1a] a plurality of second memory blocks arranged alternatively with said plurality of first memory blocks along the column direction,

In Figure 8 of Sukegawa, memory blocks 102, 106, 110, and 114 are arranged alternatively with the plurality of first memory blocks 100, 104, 108, and 112 and are aligned with the first memory blocks vertically (i.e., the column direction). *See also* Section 9.1.3, claim element [1.1b]. In Figure 8, the

bit/column lines corresponding to the memory cells in the memory blocks are not shown, but would run perpendicular to the redundant word line groups (70, 74, 76, and 78) that run horizontally in Figure 8. *See also id.* Thus, because the column lines run vertically, the first memory blocks (100, 104, 108, and 112) and second memory blocks (102, 106, 110, and 114) are aligned in the column direction.

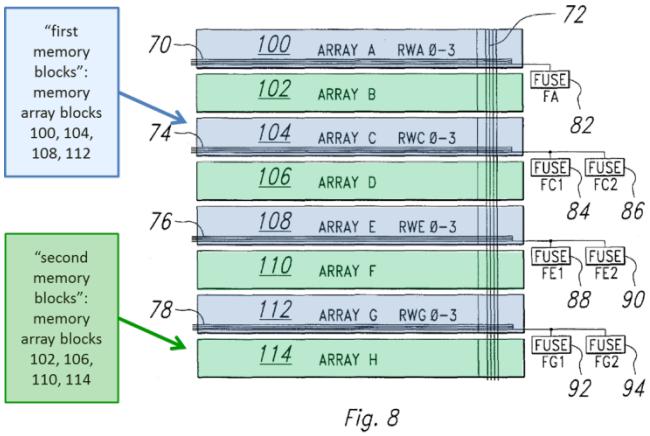



Fig. 8

**MICRON-1005, Sukegawa at Figure 8 (annotated).**

**Thus, Sukegawa discloses a plurality of second memory blocks (memory blocks 102, 106, 110, and 114) arranged alternatively with said plurality of first memory blocks (memory blocks 100, 104, 108, and 112) along the column direction.** *See also* MICRON-1007, Baker Decl. App'x A at claim element [2.1a].

#### 9.2.3. [2.1b] the second memory blocks each having a plurality of second normal memory cells arranged in a matrix of rows and columns; and

As described above with respect to claim element [1.1b], Sukegawa discloses that the memory blocks have a matrix of rows and columns of normal memory cells. *See* Section 9.1.3, claim element [1.1b]. **Thus, Sukegawa**

**discloses that the second memory blocks (memory blocks 102, 106, 110, and 114) each have a plurality of second normal memory cells arranged in a matrix of rows and columns**. *See also* MICRON-1007, Baker Decl. App'x A at claim element [2.1b].

#### 9.2.4. [2.2a] a plurality of second spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of second memory blocks,

As discussed in Section 6 of this Petition, a person of ordinary skill in the art would have understood "spare memory cells" to mean "memory cells capable of replacing defective memory cells." As discussed in Section 8 of the Petition and Section VIII of Dr. Baker's declaration, the combined teachings of Sukegawa disclose that (1) each memory block in a memory array may have row redundant (spare) memory, as described at 3:34-43 and 5:53-54; or (2) alternatively, as described in claim 1 and shown in Figure 8, "at least some" of the memory blocks in a memory array may have row redundant (spare) memory. In the first alternative, second memory blocks 102, 106, 110, and 114 would each have spare memory cells, even though they are not shown in Figure 8 to include spare memory cells. *See, e.g.*:

> FIG. 8 shows the redundant mechanism. In the redundancy programming, **the memory quadrant has 8 blocks of 1 M bits memory arrays**, each of which is divided into two 512K bits portions. **Each memory array block has 4 row redundant memories**.

MICRON-1005, Sukegawa at 5:50-54. **Thus, in this first alternative, the "particular" second memory block is block 102, and the plurality of second spare memory cells are the spare memory cells in block 102**. *See also* MICRON-1007, Baker Decl. App'x A at claim element [2.2a].

Likewise, it would have been obvious to a person of ordinary skill in the art to include spare memory cells in second plurality of memory blocks 102, 106, 110, and 114. In particular, in light of the above teachings of Sukegawa, as Dr. Baker opines, a person of ordinary skill in the art would have recognized that the placement of spare memory cells in any one of memory blocks 102, 106, 110, and 114 is a design choice, that the result of placing the spare memory cells in any of these memory blocks would have been predictable, and that motivations for including at least some redundancy in additional blocks include increasing access speed to redundant cells. MICRON-1007, Baker Decl. App'x A at claim element [2.2a].

**9.2.5. [2.2b] each row of said plurality of second spare memory cells being capable of replacing a defective row including a defective second normal memory cell in said plurality of second memory blocks.**

As discussed in Section 6 of this Petition, a person of ordinary skill in the art would have understood "spare memory cells" to mean "memory cells capable of replacing defective memory cells." Just as described with respect to Ground #1, claim element [1.2b], Sukegawa discloses an "any to any" redundant scheme in

which any row of redundant memory cells in a particular memory array block may be used to replace the defective memory in any other block in the same quadrant or in a different quadrant. **Thus, Sukegawa discloses that each row of said plurality of second spare memory cells (the spare memory cells in block 102) is capable of replacing a defective row including a defective second normal memory cell in any one of said plurality of second memory blocks (memory blocks 102, 106, 110, and 114 in Figure 8).** *See also* MICRON-1007, Baker Decl. App'x A, at claim element [2.2b].

### 9.3. Claim 6 is obvious over Sukegawa

#### 9.3.1. [6.P] The semiconductor memory device as recited in claim 1, wherein

Sukegawa discloses the semiconductor memory device as recited in claim 1. *See* Section 9.1. *See also* MICRON-1007, Baker Decl. App'x A at claim element [6.P].

#### 9.3.2. [6.1] the first normal memory cells and the first spare memory cells are arranged alignedly in the column direction.

As discussed in Section 6 of the Petition, a person of ordinary skill in the art would have understood "spare memory cells" to mean "memory cells capable of replacing defective memory cells." As discussed with respect to Ground #1 claim element [1.1d], the plurality of first memory blocks (100, 104, 108, and 112) in Figure 8 are aligned vertically:

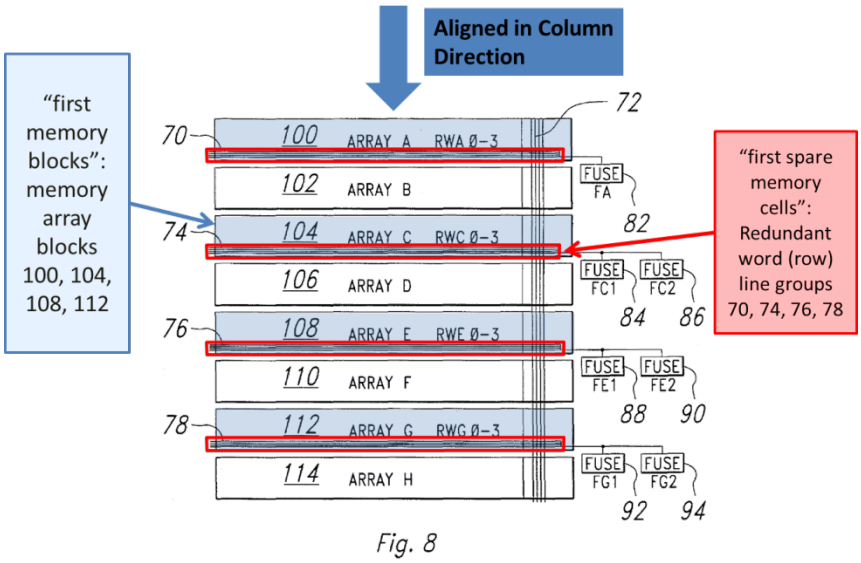
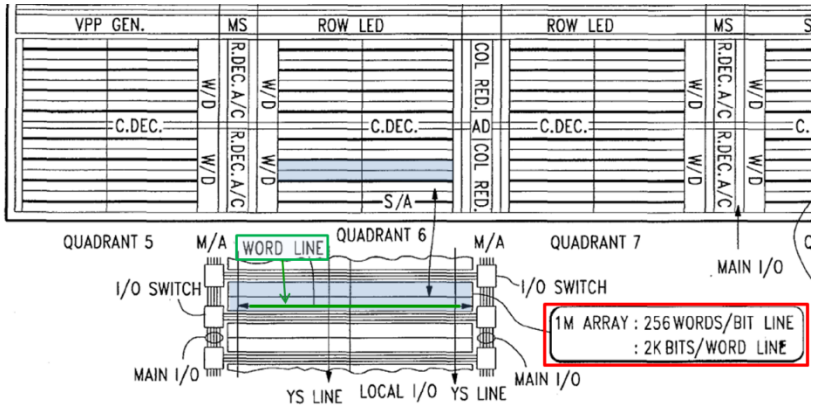



Fig. 8

**MICRON-1005, Sukegawa at Figure 8 (annotated).**

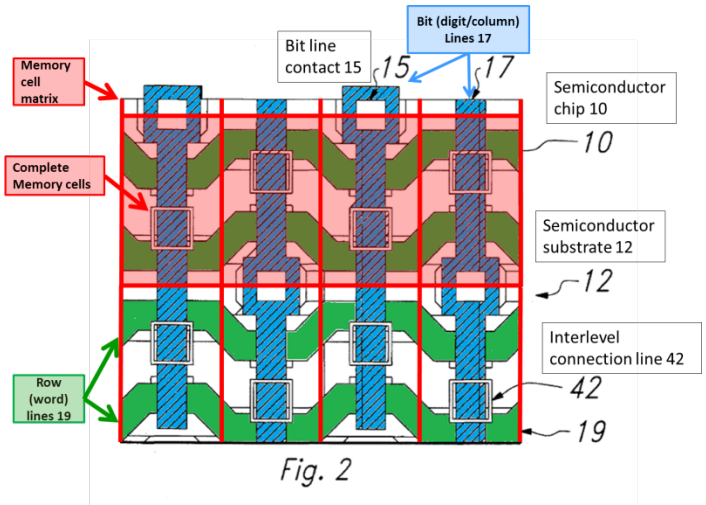
In Figure 1, Sukegawa illustrates a "Word Line" of a particular memory block.




**MICRON-1005, Sukegawa at Figure 1 (annotated excerpt).**

The column/bit lines are not shown in Figure 1, but would run parallel to the "YS LINES" and orthogonal to the Word Lines shown in the figure. The memory cells are roughly located at the intersection of every other intersection of a word line and bit line described in Figure 1. This forms a matrix of rows and columns of

memory cells. The structure of the matrix of memory cells is further illustrated in Figure 2, which shows a "plane" view of a portion of the memory array.




**MICRON-1005, Sukegawa at Figure 2 (annotated).**

Because the first normal memory cells in the first particular memory block 100 and the first spare memory cells in that memory block (redundant word (row) line group 70) would each share the same column/bit lines, this means that they would be aligned vertically *(i.e.*, in the column direction). **Thus, Sukegawa discloses that the first normal memory cells in block 100 and the first spare memory cells in block 100 (redundant word row line group (70)) are arranged alignedly in the column direction.** *See also* MICRON-1007, Baker Decl. App'x A at claim element [6.1].

However, to the extent Sukegawa does not explicitly disclose this claim element, this would have been obvious to a person of ordinary skill in the art. A central purpose of the claimed invention of Sukegawa is to minimize the size of the

redundant address decoder on the semiconductor device, and thus reduce the cost of the semiconductor device. *See* MICRON-1005, Sukegawa at Abstract. Thus, a person of ordinary skill in the art would have been motivated to make obvious modifications to Sukegawa to further this objective. In particular, as Dr. Baker opines, a person of ordinary skill in the art would have recognized that it would be necessary for the normal and spare memory cells to share the same column/bit lines (and thus be arranged alignedly in the column direction) to minimize the overall layout of the design. *See* MICRON-1007, Baker Decl. App'x A at claim element [6.1].

## 10. GROUND #2: CLAIM 3 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF PRINCE

Sukegawa renders claim 3 obvious in view of Prince.

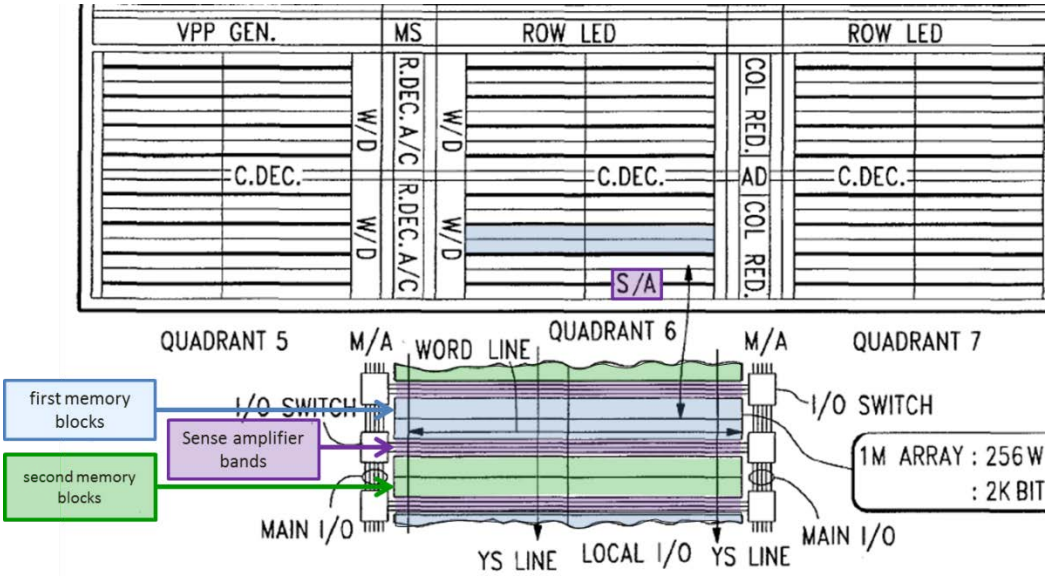
### 10.1. [3.P] The semiconductor memory device as recited in claim 2, further comprising

Sukegawa discloses the semiconductor memory device as recited in claim 2. *See* Section 9.2. *See also* MICRON-1007, Baker Decl. App'x A at claim element [3.P].

### 10.1. [3.1] a plurality of <u>sense amplifier bands</u> provided between each of said plurality of first memory blocks and each of said second memory blocks,

As discussed in Section 6 of this Petition, a person of ordinary skill in the art would have understood "sense amplifier bands" to mean "amplifiers along the horizontal direction that sense the contents of memory cells and restore (amplify)

them to full levels." Figure 1 of Sukegawa shows a cutout of the memory array in Quadrant 6. In the cutout, Sukegawa discloses that a sense amplifier band is located between each of the first and second plurality of memory blocks.




**MICRON-1005, Sukegawa at Figure 1 (annotated excerpt).**

Thus, although the sense amplifiers are not shown in Figure 8, it is clear that sense amplifier bands are located between each memory block in Figure 8:

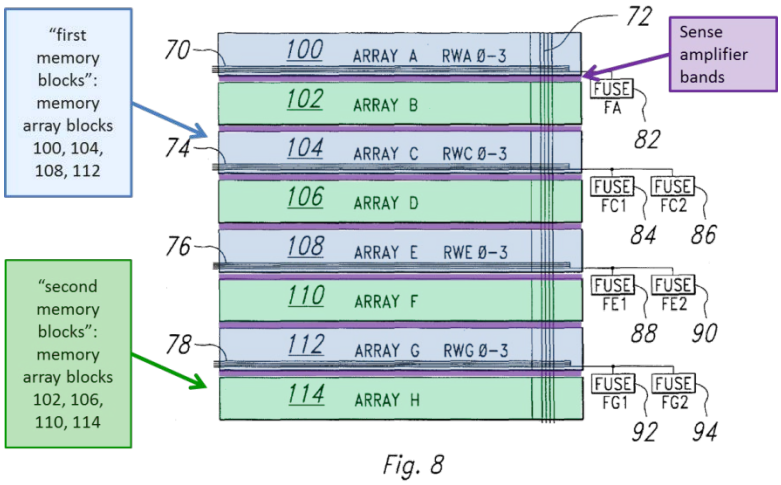



*Fig. 8*

**MICRON-1005, Sukegawa at Figure 8 (annotated).**

*See also* MICRON-1007, Baker Decl. App'x A at claim element [3.1].

Moreover, in view of Prince, it would have been obvious to a person of ordinary skill in the sense amplifier bands of Sukegawa would be between the blocks. Prince discloses that adjacent memory cells in an array may be divided into memory blocks. *See* MICRON-1009, Prince at .047 ("Mostek [40] dealt with the RC delay and capacitive coupling effects by using an innovative divided bit-line architecture which was evolved from a combination of the folded-bit line techniques and the shared sense amplifier concept as shown in Figure 6.25. This bit-line architecture divided the long columns into 16 polysilicon bit-line segments of 64 cells each with eight segments arranged end to end in a line on either side of a central column decoder. **Adjacent segments were grouped into pairs of open bit-lines to form eight memory blocks of 128k bits each**."). Prince further discloses that a sense amplifier can be shared between adjacent memory blocks.

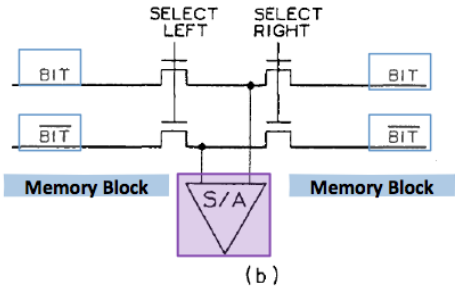



**Figure 6.25**
Evolution of multiplexed DRAM sense amps. (a) Folded bit-line. (b) Shared sense amplifier. (c) Divided bit-line. (From Taylor and Johnson [40], SGS-Thomson (Mostek) 1985, with permission of IEEE.)

**MICRON-1009, Prince at .048 (annotated).**

In Figure 6.25(b) above, the sense amplifier is shaded in purple and is shared between memory blocks (the bit lines each are part of a different memory block) on each side. Because the column/bit lines run horizontally in the figure, the figure shows the blocks in the horizontal direction, but they are aligned in the "column direction," *i.e.*, in line with the bit lines (Prince rotates the conventional arrangement, *e.g.*, of Sukegawa, horizontally in the figure). Thus, in view of Prince, it would have been obvious to place the sense amplifier bands of Sukegawa between the blocks.

**Thus, Sukegawa in view of Prince discloses a plurality of sense amplifier bands (shaded in purple above in the Sukegawa figures) provided between each of said plurality of first memory blocks (memory blocks 100, 104, 108, and 112) and each of said second memory blocks (memory blocks 102, 106, 110, and 114).**

**10.2. [3.2] and shared by adjacent memory blocks in the column direction for sensing and amplifying data in each column of the adjacent memory block including a selected memory cell when activated.**

Sukegawa in view of Prince discloses this limitation. Sukegawa does not explicitly disclose that blocks share the sense amplifier bands. However, Prince discloses this. Specifically, Prince discloses DRAM architectures with multiple memory blocks. *See* MICRON-1009, Prince at .047 ("**Adjacent segments were grouped into pairs of open bit-lines to form eight memory blocks of 128k bits**

**each**.”). As described above, Prince further discloses that a sense amplifier can be shared between adjacent memory blocks. *See* MICRON-1009, Prince at .048 ((Figure 6.25(b) (“shared”). And Prince discloses the well-known function of sense amplifiers, *i.e.*, sensing and amplifying data from memory cells during accesses. MICRON-1009, Prince at .037; *see also* MICRON-1007, Baker Decl. ¶ 27.

**Thus, Sukegawa in view of Prince discloses that the sense amplifier bands (shaded in purple in the Sukegawa figures) are shared by adjacent memory blocks (e.g., blocks 112 and 114) in the column direction for sensing and amplifying data in each column of the adjacent memory block including a selected memory cell when activated.** *See also* MICRON-1007, Baker Decl. App’x A at claim element [3.2].

### 10.3. Motivation to Combine Prince and Sukegawa

It would have been obvious to combine the teachings of Prince with Sukegawa, as Dr. Baker explains. *See* MICRON-1007, Baker Decl. Section VIII.E. As noted above, a central purpose of the claimed invention of Sukegawa is to minimize the size of the redundant address decoder on the semiconductor device, and thus reduce the cost of the semiconductor device. MICRON-1005, Sukegawa at Abstract. A person of ordinary skill in the art would have been motivated to make obvious modifications to Sukegawa to further this objective,

and in solving this problem would have been motivated to consult common resources in the semiconductor field. As Dr. Baker explains, Prince was a well-known resource in the field of semiconductor memory devices. *See* MICRON-1007, Baker Decl. ¶ 23. A person of ordinary skill in the art would have recognized that sharing sense amplifiers between adjacent memory blocks as disclosed in Prince would further this objective. Further, combining the teachings of Prince and Sukegawa would have predictable results (*i.e.*, a shared sense amplifier between adjacent memory blocks in the device disclosed in Sukegawa). *See id.* Shared sense amplifiers was a well-known design choices. *See id.*

## 11. GROUND #3: CLAIM 4 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF PRINCE

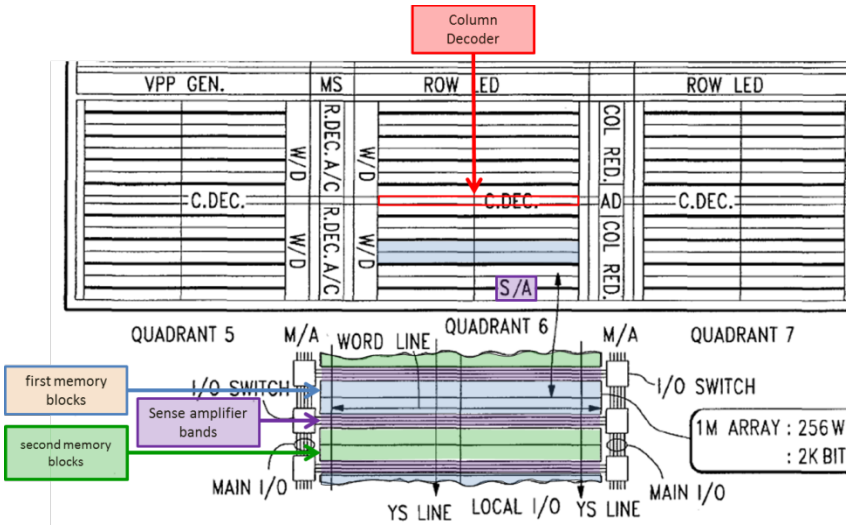
Sukegawa renders claim 4 obvious in view of Prince.

### 11.1. [4.P] The semiconductor memory device as recited in claim 2, wherein

Sukegawa discloses the semiconductor memory device as recited in claim 2. *See* Section 9.2. *See also* MICRON-1007, Baker Decl. App'x A at claim element [4.P].

### 11.2. [4.1] the first memory blocks and the second memory blocks share a circuit related to a memory cell selection operation.

The column decoders in Figure 1 of Sukegawa perform the function of selecting bit/column lines corresponding to the column address of a memory cell in the memory blocks:




**MICRON-1005, Sukegawa at Figure 1 (annotated excerpt).**

Sukegawa does not explicitly disclose that the blocks actually share the column decoder. However, a person of ordinary skill in the art would have found it obvious in view of Prince that the blocks of Sukegawa share the column decoders. First, because only one column decoder is provided for each memory array in Figure 1, the column decoder must be shared by the memory blocks in that array. If it was not shared by the memory blocks, the memory in the memory blocks in that array could not be selected. *See* MICRON-1007, Baker Decl. App'x A at claim element [4.1]. Second, consistent with this disclosure, Prince discloses that multiple memory blocks may share a column decoder. *See, e.g.*, MICRON-1009, Prince at .047 (describing a DRAM semiconductor device and stating that "[t]he column decoder and I/O bus lines are shared by eight 64k memory arrays."). Thus, a person of ordinary skill in the art would have it obvious for the blocks of Sukegawa to in fact share the column decoder.

**Thus, Sukegawa in view of Prince discloses that the first memory blocks and the second memory blocks share a circuit related to a memory cell selection operation (the column decoder).**

### 11.3. Motivation to Combine Prince and Sukegawa

It would have been obvious to combine the teachings of Prince with Sukegawa to render claim limitation [4.1] obvious. *See* MICRON-1007, Baker Decl. Section VIII.E, App'x A claim element [4.1]. As noted above, a central purpose of the claimed invention of Sukegawa is to minimize the size of the redundant address decoder on the semiconductor device, and thus reduce the cost of the semiconductor device. MICRON-1005, Sukegawa at Abstract. A person of ordinary skill in the art would have been motivated to make obvious modifications to Sukegawa to further this objective, and in solving this problem would have been motivated to consult common resources in the semiconductor field. As Dr. Baker explains, Prince was a well-known resource in the field of semiconductor memory devices. *See* MICRON-1007, Baker Decl. ¶ 23. A person of ordinary skill in the art would have recognized that sharing a circuit related to a memory cell selection operation as disclosed in Prince would further this objective. *See id.* Further, combining the teachings of Prince and Sukegawa (using the design choice of a shared decoder) would have predictable results (*i.e.*, a shared column decoder in

the device disclosed in Sukegawa). *See id.* Shared column decoders were a well-known design choice. *See id.*

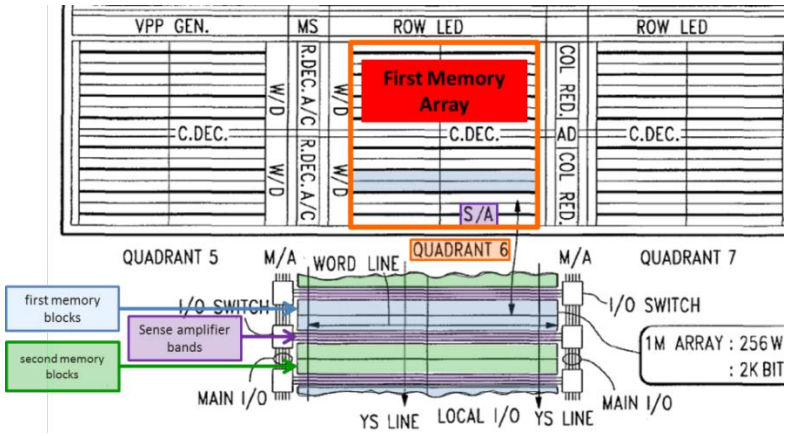
## 12. GROUND #4: CLAIM 5 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF WALCK

### 12.1. [5.P] The semiconductor memory device as recited in claim 3, wherein

Sukegawa discloses the semiconductor memory device as recited in claim 3. *See* Section 10. *See also* MICRON-1007, Baker Decl. App'x A at claim element [5.P].

### 12.2. [5.1] said plurality of first memory blocks, said plurality of second memory blocks and said plurality of sense amplifier bands form a first memory array, and

As discussed in Section 6 of this Petition, a person of ordinary skill in the art would have understood "sense amplifier bands" to mean "amplifiers along the horizontal direction that sense the contents of memory cells and restore (amplify) them to full levels." The first memory array may, for example, be the memory array in Quadrant 6 of Figure 1. Quadrant 6 contains a plurality of first and second memory blocks and a plurality of sense amplifier bands, which are shown below:

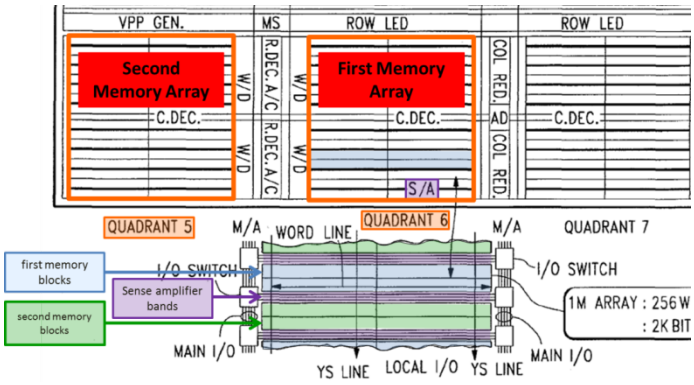



**MICRON-1005, Sukegawa at Figure 1 (annotated).**

**Thus, Sukegawa discloses that said plurality of first memory blocks, said plurality of second memory blocks and said plurality of sense amplifier bands form a first memory array (e.g., in quadrant 6)**. *See also* MICRON-1007, Baker Decl. App'x A at claim element [5.1].

### 12.3. [5.2] said semiconductor memory device further comprises: a second memory array having a same arrangement as the first memory array; and

As shown in Figure 1 of Sukegawa, each quadrant has the arrangement of memory blocks shown in Figure 1. Because Quadrant 6 was selected for the first memory array, the second memory array may be located in Quadrant 5 of Figure 1. Just like Quadrant 6, Quadrant 5 contains a plurality of first and second memory blocks and a plurality of sense amplifier bands:




**MICRON-1005, Sukegawa at Figure 1 (annotated).**

**Thus, Sukegawa discloses a second memory array having a same arrangement as the first memory array in a different quadrant than the first memory array (e.g., in Quadrant 5).** *See also* MICRON-1007, Baker Decl. App'x A at claim element [5.2].

### 12.4. [5.3a] control circuitry for driving one memory block from the first and second memory arrays into a selected state in a normal operation mode,

Sukegawa in view of Walck discloses this claim element. Walck discloses that in conventional memories, normal operation mode involves accessing a single bank (in Sukegawa, a quadrant) at a time. MICRON-1006, Walck at 1:44-46 ("Thus, it is appreciated that **for read/write memory access cycles, one of the plurality of RAS lines is enabled in order to access the appropriate bank**."). Applying this teaching to Sukegawa would involve accessing a single block within one quadrant at a time because a bank is equivalent to Sukegawa's quadrant and Sukegawa only teaches accessing one block within a quadrant at time (*e.g.*, because there is only a single decoder per quadrant). *See also* MICRON-1007,

Baker Decl. App'x A at claim element [5.3a]; MICRON-1005, Sukegawa at Fig. 1, 1:38-54. Memory access involves "driving" the memory block into a "selected state," that is, opening its row. *See id.*

Further, Walck discloses control circuitry to access a single bank at a time. *Id.* at 1:57-67 ("The **controller includes decoding and bank selection logic** that decodes the memory address into one of a plurality of bank selection lines which in turn provide the RAS signals, respectively. The bank selection lines are passed through refresh generating circuitry comprising logical OR functions responsive to the refresh request and RAS pulse usually derived from the microprocessor timing signals in order **to individually energize the RAS lines during read/write memory access cycles** and simultaneously energize the RAS lines during refresh cycles."). Accordingly, Sukegawa in view of Walck, discloses this element. *See also* MICRON-1007, Baker Decl. App'x A at claim element [5.3a].

**12.5. [5.3b] and for simultaneously driving a prescribed number of memory blocks from each of said first and second memory arrays into a selected state in a <u>particular operation mode</u>.**

Sukegawa in view of Walck discloses this claim element. Walck discloses that in conventional memories it was known to access all banks (in Sukegawa, quadrants) simultaneously to refresh the DRAM. MICRON-1006, Walck at 1:44-48 ("Thus, it is appreciated that for read/write memory access cycles, one of the plurality of RAS lines is enabled in order to access the appropriate bank. **<u>During</u>**

**memory refresh cycles, all of the RAS lines are simultaneously enabled**.”). The particular mode of Walck is “refresh” mode. *See id.*

Further, Walck discloses control circuitry to simultaneously access all banks. *Id.* at 1:57-67 (“The **controller includes decoding and bank selection logic** that decodes the memory address into one of a plurality of bank selection lines which in turn provide the RAS signals, respectively. The bank selection lines are passed through refresh generating circuitry comprising logical OR functions responsive to the refresh request and RAS pulse usually derived from the microprocessor timing signals in order to individually energize the RAS lines during read/write memory access cycles **and simultaneously energize the RAS lines during refresh cycles**.”). Accordingly, Sukegawa in view of Walck, discloses this element. *See also* MICRON-1007, Baker Decl. App’x A at claim element [5.3b].

### 12.6. Motivation to Combine Sukegawa and Walck

It would have been obvious to combine the teachings of Walck with Sukegawa as Dr. Baker explains. *See* MICRON-1007, Baker Decl. Section VIII.C.

First, both Sukegawa and Walck are within the DRAM memory space. *See, e.g.*, MICRON-1005, Sukegawa at 1:12-14; 2:21-22; MICRON-1006, Walck at Abstract. Second, both involve DRAM architectures with multiple arrays (quadrants in Sukegawa and banks in Walck). *See, e.g.*, MICRON-1005, Sukegawa at Figure 1; MICRON-1006, Walck at 1:11-32.

Third, those of ordinary skill the art understood that all DRAM require "refreshing." *See* MICRON-1007, Baker Decl. ¶ 80. Those of skill in the art would have understood to look at known refresh techniques to apply to Sukegawa. Walck discloses one well-known refresh scheme. *See id.* Moreover, Walck's refresh scheme would be particularly applicable because Sukegawa discloses a multi-quadrant architecture. *Id.*

Fourth, employing the refresh scheme of Walck is a design choice, and was known to yield predictable results given that it was a conventional refresh scheme. *Id.* at ¶ 81. And those of ordinary skill the art would have had motivation to apply the Walck refresh scheme to Sukegawa because it refreshes all rows more quickly because it uses a simultaneous access approach. *See id.*

## 13. GROUND #5: CLAIM 7 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF OH

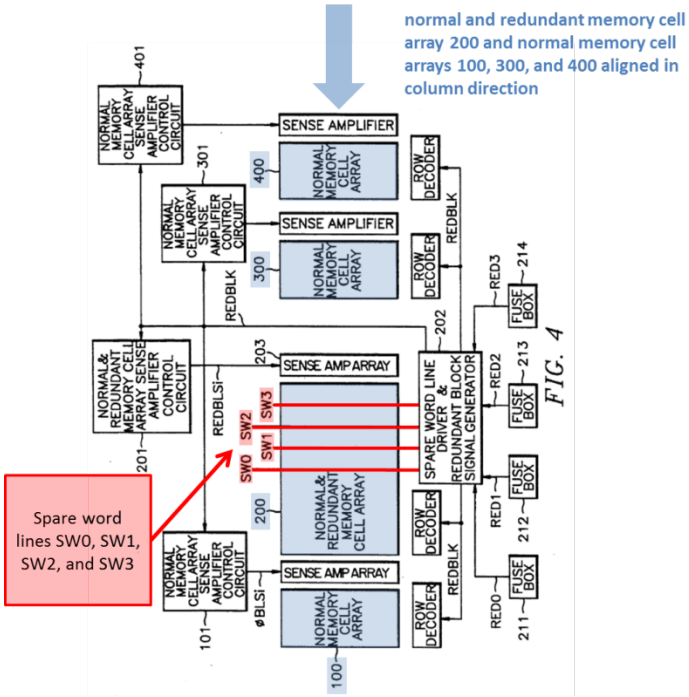
Sukegawa in view of Oh renders obvious claim 7, specifically, it renders obvious that one memory block in Sukegawa (the "particular" first memory block 100) would have spare memory cells while the remaining first memory blocks 104, 108, and 112 would not have spare memory cells.

**13.1. [7.P] The semiconductor memory device as recited in claim 1, wherein**

Sukegawa discloses the semiconductor memory device as recited in claim 1. *See* Section 9.1. *See also* MICRON-1007, Baker Decl. App'x A at claim element [7.P].

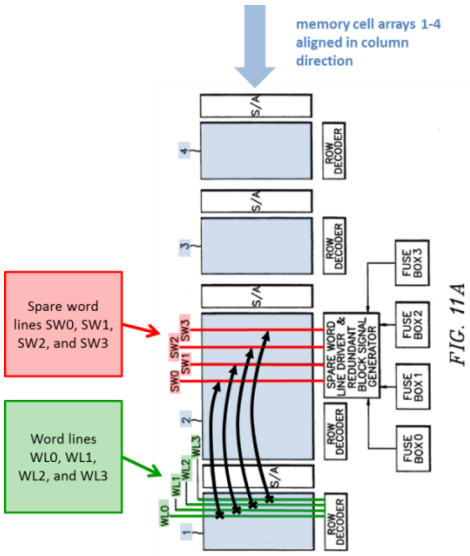
**13.2. [7.1] the first memory blocks other than said particular one has no first spare memory cells.**

Sukegawa in view of Oh discloses this limitation. Figure 4 of Oh is a block diagram showing the construction of the disclosed semiconductor device. MICRON-1010, Oh at 3:61-63. In Figure 4, array 200 is shown to include normal memory and redundant memory (spare word lines SW0-SW3) and arrays 100, 300, and 400 include normal memory only. Rotating Figure 4 by 90 degrees puts it in the same perspective as the 181 Patent. Specifically, the spare word lines run horizontally, and the column/bit lines would run vertically. The bit lines define the column and vertical direction. *See* analysis of claim limitation [1.1a]. Thus, because arrays 100, 200, 300, and 400 are all aligned in the bit lines direction, they are aligned in the vertical, column direction as shown below (rotated image to illustrate bit line direction as the vertical direction):

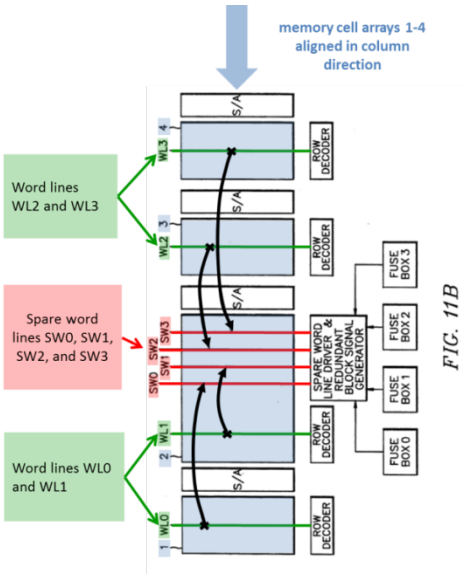



**MICRON-1010, Oh at Figure 4 (annotated and rotated).**

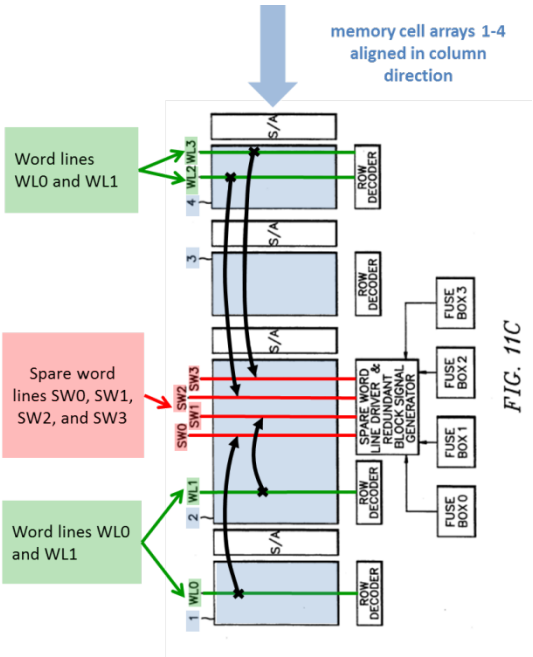
Figures 11A-C are simplified block diagrams that illustrate the operation of the redundancy mechanism. MICRON-1010, Oh at 6:19-22. Just like Figure 4, Figures 11A-C depict four memory arrays (arrays 1 through 4) aligned vertically (*i.e.*, aligned in the column direction), only one of which includes spare word lines (array 2). These figures further illustrate how the spare word lines in array 2 can replace defective memory in array 2 or any of the other arrays. Specifically, Figure 11A shows replacement of four word lines in array 1, Figure 11B shows replacement of one word line in each of arrays 1-4, and Figure 11C shows replacement of one word line in array 1, one word line in array 2, and two word lines in array 4. *See id.* at 6:22-33.




**MICRON-1010, Oh at Figure 11A (annotated).**




**MICRON-1010, Oh at Figure 11B (annotated).**




**MICRON-1010, Oh at Figure 11C (annotated).**

**Thus, Sukegawa in view of Oh discloses this element because Oh discloses one memory block ("particular" first memory block 2/200) that has spare memory cells while the remaining first memory blocks 1/100, 3/300, and**

**4/400 do not have spare memory cells**. *See also* MICRON-1007, Baker Decl. App'x A at claim element [7.1].

### 13.3. Motivation to Combine Sukegawa and Oh

It would have been obvious to combine the teachings of Oh with Sukegawa as Dr. Baker explains. *See* MICRON-1007, Baker Decl. Section VIII G. Both Sukegawa and Oh are directed to the goal of repairing defective memory while at the same time minimizing the amount of chip space that is required. *See, e.g.*, MICRON-1005, Sukegawa at Abstract**;** MICRON-1010, Oh at Abstract. Because both references address this same problem, a person of ordinary skill in the art would be motivated to combine their teachings. And in light of the teachings of Sukegawa and Oh, one of ordinary skill in the art would have been motivated to try different redundancy arrangements, the number of blocks having redundancy being a design choice. *See* MICRON-1007, Baker Decl. Section VIII G. Moreover, combining Sukegawa with Oh would have a predictable result (*i.e.*, placement of redundant memory in only one of the plurality of first memory blocks). *See id.*

## 14.CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1, 2, 3, 4, 5, 6 and 7 of the 181 Patent is requested.

Respectfully submitted,

Dated: October 26, 2015

By: 

Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73604
Weil, Gotshal & Manges LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: 650-802-3237

## CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

| | |
|---|---|
| *Date of service* | October 27, 2015 |
| *Manner of service* | EXPRESS MAIL |
| *Documents served* | Petition for *Inter Partes* Review of U.S. Pat. No. 6,233,181 with Micron's Exhibit List<br><br>Power of Attorney<br><br>Exhibits MICRON-1001 through MICRON-1010 |
| *Persons served* | Patent Owner's Address of Record:<br><br>McDermott Will & Emery LLP<br>The McDermott Building<br>500 North Capitol Street, N.W.<br>Washington, DC 20001<br><br>Additional Address Known as Likely to Effect Service:<br><br>Jon A. Birmingham<br>Fitch Even Tabin & Flannery LLP<br>21700 Oxnard Street Suite 1740<br>Woodland Hills, CA 91367 |

/Jeremy Jason Lang/

Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73604