`UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 5,943,260
Title: METHOD FOR HIGH-SPEED PROGRAMMING OF A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

Petition For *Inter Partes* Review of U.S. Patent No. 5,943,260 Under 35 U.S.C §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

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Patent Trial and Appeal Board
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P.O. Box 1450
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Exhibit List

Micron Exhibit #	*Description*
MICRON-1001	U.S. Patent No. 5,943,260 ("the 260 Patent")
MICRON-1002	File History for U.S. Patent No. 5,943,260
MICRON-1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 5,677,869 ("Fazio")
MICRON-1006	U.S. Patent No. 4,858,194 ("Terada")

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-5 of United States Patent No. 5,943,260, titled "Method for High-Speed Programming of a Nonvolatile Semiconductor Memory Device" (MICRON-1001, "the 260 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 260 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 260 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang (Reg. No. 73604) (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Justin L. Constant (Reg. No. 66883) (justin.constant@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5217; F: 713-224-9511

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for the Petitioner is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. (*See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.)

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Limestone has asserted the 260 Patent and U.S. Patent Nos. 5,805,504 ("the 504 Patent"), 6,233,181 ("the 181 Patent"), 5,894,441 ("the 441 Patent"), and 6,697,296 ("the 296 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Limestone Memory Sys. LLC v. Micron Tech. Inc.*, 8:15-cv-00278 (C.D. Cal.) ("Co-Pending Litigation"). Limestone has also asserted one or more of the asserted patents in the following actions: *Limestone Memory Sys. LLC v. OCZ Storage Solutions, Inc.*, 8:15-cv-00658 (C.D. Cal.) (the 504, 441, 181 and 296 Patents); *Limestone Memory Sys. LLC v. PNY Techs., Inc.*, 8:15-cv-00656 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Lenovo (US) Inc.*, 8:15-cv-00650 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Kingston Tech. Co. Inc.*, 8:15-cv-00654 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Transcend Info.*,

Inc., 8:15-cv-00657 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Acer America Corp.*, 8:15-cv-00653 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Dell Inc.*, 8:15-cv-00648 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Hewlett-Packard Co.*, 8:15-cv-00652 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); and *Limestone Memory Sys. LLC v. Apple Inc.*, 8:15-cv-01274 (C.D. Cal.) (the 504, 441, 181, and 296 Patents).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 5,805,504, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 6,233,181, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 5,894,441, IPR2015-Unassigned (to be filed concurrently); and Petition for *Inter Partes* Review of U.S. Patent No. 6,697,296, IPR2015-Unassigned (to be filed concurrently).

The 260 Patent claims priority to foreign patent application JP-09-054048. The 260 Patent does not claim priority to any other U.S. patent applications.

2.5. Fee for Inter Partes Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 260 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Ground #1: Claims 1, 2, 3, and 4 of the 260 Patent are invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that they are obvious over U.S. Patent No. 5,677,869, to Fazio et al. ("Fazio"), entitled "Programming Flash Memory Using Strict Ordering of States," filed with the USPTO on December 14, 1995, issued October 14, 1997. Fazio is attached as MICRON-1005.

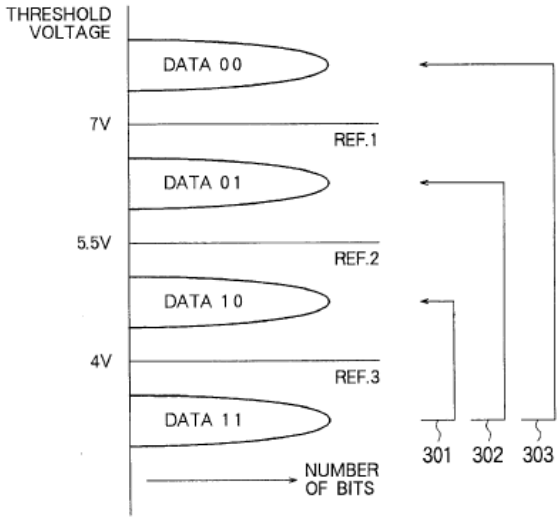
Ground #2: Claim 5 of the 260 Patent is invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that it is obvious over Fazio in view of U.S. Patent No. 4,858,194, to Terada et al. ("Terada"), entitled "Nonvolatile Semiconductor Memory Device Using Source Of A Single Supply Voltage," filed with the USPTO on February 10, 1988, issued August 15, 1989. Terada is attached as MICRON-1006.

These grounds (comprising claims 1-5, *i.e.*, the "challenged claims") are explained below and are supported by the Declaration of Dr. R. Jacob Baker (MICRON-1003, "Baker Decl.").

4. OVERVIEW OF THE 260 PATENT

The 260 Patent was filed with the USPTO on February 20, 1998, and claims priority to a Japanese patent application which was filed on February 21, 1997. The 260 Patent issued on August 24, 1999. The 260 Patent is directed to a method for programming nonvolatile memory devices having flash memory cells. *See* MICRON-1001, 260 Patent at Abstract; MICRON-1003, Baker Decl. ¶ 23. The specific type of flash memory cells mentioned in the 260 Patent are Flash EEPROM (Electronically Erasable and Programmable Read Only Memory), which were known in the art as nonvolatile memory devices containing memory cells that can be electronically programmed and erased. MICRON-1001, 260 Patent at 1:14-17. As was known in the art, EEPROM was developed in a way that allowed each memory cell to store more than one bit of data, and each one of those bits could have a different value. *Id.* at 1:52-55. To do this, each memory cell was allowed to have multiple threshold states with different assigned values. *Id.* A memory cell structure providing for more than two states is commonly known as multilevel cell memory. MICRON-1003, Baker Decl. ¶ 28. Figure 4 of the 260 Patent, which is admitted prior art, shows a graph of the different states of a multilevel memory cell (Data 00, Data 01, Data 10, and Data 11) as defined by different threshold voltages. *See also* MICRON-1001, 260 Patent at 2:65-3:10.

FIG. 4
PRIOR ART

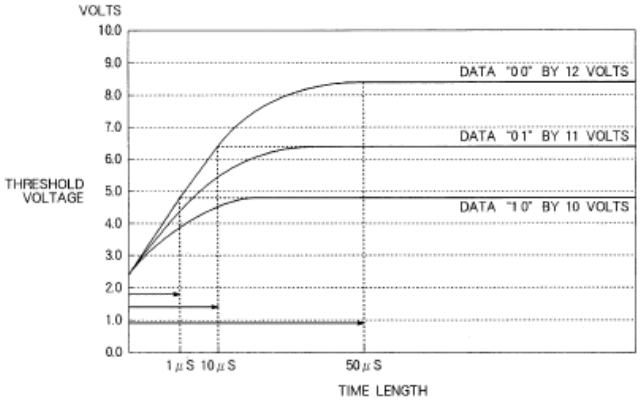


MICRON-1001, 260 Patent at Figure 4.

One of the conventional methods of programing a plurality of multilevel memory cells, which is admitted prior art, was to program groups of cells to the different threshold voltages sequentially. MICRON-1001, 260 Patent at 2:43-51; MICRON-1003, Baker Decl. ¶ 30. As shown in Figure 4 above and described in the specification, arrow 301 demonstrates the programming of cells by a 10 volt programming voltage to the threshold voltage, which is represented by Data 10 (between 4 and 5.5 volts). MICRON-1001, 260 Patent at 2:43-51 & Fig. 4. Arrow 302 demonstrates the programming of cells by an 11 volt programming voltage to the threshold voltage, which is represented by Data 01 (between 5.5 and 7 volts). Arrow 303 demonstrates the programming of cells by a 12 volt programming voltage to the threshold voltage represented by Data 00 (more than 7 volts). *Id.*

According to the 260 Patent, the length of time required to program each group of multilevel cells is generally large. *Id.* at 3:11-13. Figure 5 depicts the amount of time needed to program a memory cell to different threshold voltages, which represent the different states, using the prior art approach of Figure 4. *Id* at 3:19-31, 4:46-48.

FIG. 5
PRIOR ART



MICRON-1001, 260 Patent at Figure 5.

The alleged invention of the 260 Patent seeks to reduce the amount of time to program several groups of cells by programming them in parallel, when possible. *Id.* at 3:66-4:4, 4:23-30. Rather than programming each group of memory cells to different states with individualized programming routines, the 260 Patent teaches programming cells that will ultimately be in different states at the same time. MICRON-1003, Baker Decl. ¶ 33.

In particular, the method described by the patent is directed to programming nonvolatile memory devices (Flash EEPROM) that have a plurality of multi-level

cells grouped in blocks. MICRON-1001, 260 Patent at 4:5-8. The first steps analyze and detect a plurality of data to be programmed in memory cells located in a particular block. *Id.* at 4:9-11. Specifically, the first steps involve analyzing data and detecting two groups of cells within a block to be programmed to two different values: the first group to a first value and the second group to a second value. *Id.* at 4:11-14. In other words, these steps correlate the data to be programmed with respective memory cells. For example, if the block consists of 4 memory cells, and the data to be programmed in the block is 01, 01, 10, and 10, then the analyzing and detecting steps would determine that the first group consists of the first two memory cells (to be programmed to 01) and the second group consists of the last two memory cells (to be programmed to 10). MICRON-1003, Baker Decl. ¶ 34.

Then, the next steps are to consecutively apply increasing programming voltages to the detected groups of cells in parallel. MICRON-1001, 260 Patent at 4:14-15. This involves programming both groups of detected cells at the same time, even though ultimately these groups will be programmed to different states. *See id.* at 4:15-19. Specifically, a first programming voltage, corresponding to the first value, is applied to all of the cells in the first group **and the second group** in parallel. *Id.* at 4:15-17. This step will ultimately program the first group and second group, in parallel, to the first group's intended threshold voltage (a "first potential")—but the second group will need additional programming because the

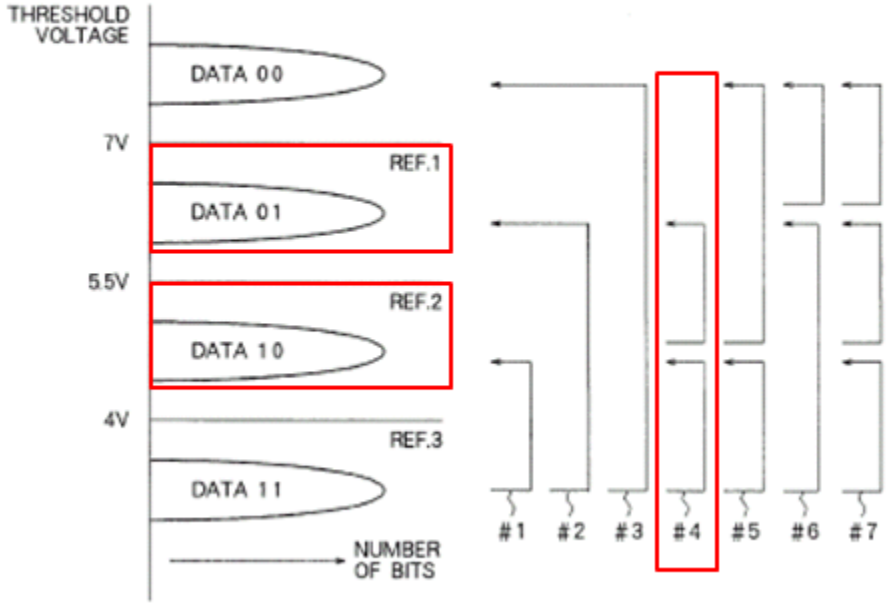
second group of cells must be programmed to reach a higher threshold voltage. Thus, a programming voltage corresponding to the second value is then applied only[1] to the cells in the second group to further program those cells to the second higher threshold voltage. *Id.* at 4:17-19. The 260 Patent teaches that this parallel approach saves time by programming group 1 and 2 cells together, rather than individually, which helps group 2 cells reach their threshold level more quickly. *See id.* at 4:23-31; MICRON-1003, Baker Decl. ¶ 39.

The 260 Patent also teaches that the programming voltage increases with each successive group, as the voltage corresponds to a different, higher value for the second group than the first group. *Id.* at 4:19-22. In simple terms, it is more time intensive to program cells to higher threshold voltages, and thus the 260 Patent teaches increasing the programming voltage when transitioning to the programming of higher-threshold groups. MICRON-1003, Baker Decl. ¶ 36.

[1] Effectively, the programming voltage is applied only to the second group. Technically, the programming voltage is applied to the entire row of cells, but because a voltage pulse is applied to the drains of only the second group, the programming voltage is effectively only applied to the second group. The drain voltage in a sense enables the programming voltage to actually program the cells. *See* MICRON-1003, Baker Decl. ¶ 35, fn. 2.

The programming process of the 260 Patent is depicted in Figures 8 and 9. In Figure 8, Arrow #4 indicates programming for a first group of data to "10" and a second group of data to "01." MICRON-1001, 260 Patent at 5:32-39.

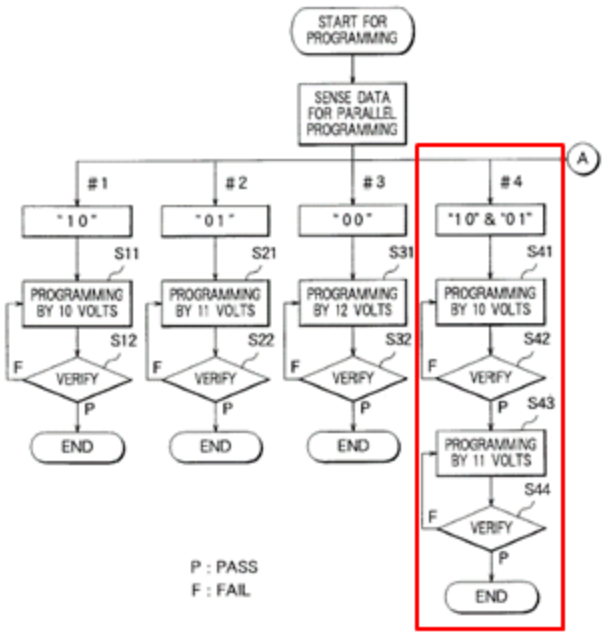
FIG. 8



MICRON-1001, 260 Patent at Figure 8 (annotated).

Path #4 in Figure 9 demonstrates the steps of the process by which these two groups are programmed.

FIG. 9



MICRON-1001, 260 Patent at Figure 9 (annotated).

At S41, both of groups of cells are programmed by 10 volts until the threshold voltage corresponding to "10" is reached. MICRON-1001, 260 Patent at 5:32-39. Then, at S43, only the second group is programmed by an additional 11 volts until the threshold voltage for "01" is reached. *Id.* As the cells in the second group were already partially programmed to a particular voltage in connection with the first group, the 260 Patent teaches faster programming that allows the second group of cells to reach their desired voltage more quickly. *Id.* at 4:23-31; MICRON-1003, Baker Decl. ¶ 39.

The method in the 260 Patent can also include the additional step of applying a third programming voltage to a third group of cells. MICRON-1001,

260 Patent at 8:47-55. Here, the third group would essentially be given two head starts (in connection with the programming of the first group and the programming of the second group). *Id.* This allegedly provides even greater program time savings. MICRON-1001, 260 Patent at 4:23-31.

Thus, the 260 Patent purports to be novel because, by programming all cells that need to achieve higher threshold voltages in parallel to lower threshold voltages initially, the total programming time is reduced. MICRON-1003, Baker Decl. ¶ 41.

5. PROSECUTION HISTORY

The examiner initially rejected all five pending claims in the application for the 260 Patent on the basis of anticipation under 35 U.S.C. §102(a) noting that there was no discernable difference between the claimed method and the prior art. MICRON-1002, 11-23-1998 Office Action at .162-163; MICRON-1003, Baker Decl. ¶ 43. In attempting to overcome this challenge with respect to claim 1, the alleged point of novelty identified by the Applicant was that "a first programming voltage is applied to ***both of*** the first group and the second group (please note that this feature is not disclosed in the prior art)." MICRON-1002, 2-16-1999 Amendment at .167 (emphasis and parenthetical in original). "Then, a second programming voltage is applied to the second group." *Id.*; MICRON-1003, Baker Decl. ¶ 43.

6. CLAIM CONSTRUCTION[2]

6.1. Applicable Law

A claim subject to *inter partes* review is given the "broadest reasonable construction in light of the specification of the patent in which it appears."[3] 37 C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

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[2] Petitioner expressly reserves the right to challenge one or more claims (and claim terms) of the 260 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 3.5. U.S.C. § 112 are met for any claim of the 260 Patent.

[3] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill in the art and consistent with the specification of the 260 Patent. Petitioner respectfully submits that the following terms shall be construed for this IPR:

6.2.1. "programming voltage" (claims 1-5)

The term "programming voltage" is a limitation of claims 1-5 of the 260 Patent. The 260 Patent does not provide an explicit definition of the term "programing voltage," but it does provide meaningful guidance as to the meaning of this term. Petitioner respectfully submits that the plain and ordinary meaning of this term is "a voltage applied to a control gate of a memory cell." Claim 5 of the 260 Patent supports this construction by making clear that the first and second programming voltages are applied to the control gates of the memory cells. MICRON-1001, 260 Patent at claim 5 (" . . . first and second programming voltages are applied to control gates of said first and second groups of memory cells . . .").

Additionally, the specification of the 260 Patent includes an example of the process used to program a memory cell in flash EEPROM. In the example, the process involves applying "about 12 volts" to the control gate of a memory cell.

Id. at 1:27-33 ("Programming of the memory cell in the flash EEPROM is effected, for example, by **applying about 12 volts to the control gate 107**, about 5 volts to the drain 101 and zero volts to the source 102, with the substrate 100 maintained at a ground potential, so as to raise the potential of the floating gate 105 by using capacitive coupling between the control gate 107 and the floating gate 105."). As explained later in the 260 Patent, "[t]he injected electrons stay in the floating gate 105 after programming, to **thereby raise the threshold of the MOSFET or memory cell**, because the floating gate 105 is surrounded by the insulator film." *Id.* at 1:41-44.

Further, the control gate of the memory cell is connected to "one of a plurality of word lines" in the memory device. *Id.* at 1:56-62 ("Referring to FIG. 2 showing a schematic configuration of a nonvolatile semiconductor memory device having multi-valued data, . . . **a plurality of word lines each connected to the control gates** of a row of memory cells in a memory cell array."). The specification also discloses applying the "programming voltage" to the word lines. *Id.* at 2:11-14 ("The program data sense block 205 controls the variable voltage generator 204 . . . to **provide a programming voltage to a selected word line** . . ."). Since the control gates of the memory cells are connected to the word lines of the device, the "programming voltage" is the voltage applied to the control gate of the memory device. MICRON-1003, Baker Decl. ¶ 22.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 260 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design of memory devices. MICRON-1003, Baker Decl. ¶ 15. An individual with an advanced degree in a relevant field would require less experience in the design of memory devices. *Id.*

8. DESCRIPTION OF THE PRIOR ART

8.1. U.S. PATENT NO. 5,677,869 ("FAZIO")

U.S. Patent No. 5,677,869 ("Fazio") (MICRON-1005) was filed on December 14, 1995. Fazio issued on October 14, 1997, to Albert Fazio et al., and is entitled "Programming Flash Memory Using Strict Ordering of States." The original assignee of Fazio was Intel Corporation. Fazio is prior art to the 260 Patent under at least (pre-AIA) 35 U.S.C. § 102(e) because Fazio was granted on an application that was filed before the earliest application that the 260 Patent claims priority was filed.

Like the 260 Patent, Fazio teaches a method of programming a nonvolatile flash memory device containing multilevel cells. MICRON-1005, Fazio at 2:32-34; MICRON-1003, Baker Decl. ¶ 45. Also like the 260 Patent, the object of the invention disclosed by Fazio is a method for programming multilevel cells at a

higher speed. MICRON-1005, Fazio at 2:32-34; MICRON-1003, Baker Decl. ¶ 45. Fazio discloses the same concept of parallel programing as the 260 Patent.

Specifically, the method in Fazio is directed to programming an array of memory cells, where each cell is able to store more than one bit of data in more than one state (*i.e.*, multilevel cells). MICRON-1005, Fazio at 2:35-37; MICRON-1003, Baker Decl. ¶ 46. The "state" refers to the value that can be programmed into the cell. MICRON-1005, Fazio at 1:29-36, 3:31-44; MICRON-1003, Baker Decl. ¶ 46. The "state," as used in Fazio, is identified by a range of charge and/or a corresponding range of threshold voltages or drain currents to represent the value stored in the cell. MICRON-1003, Baker Decl. ¶ 46; MICRON-1005, Fazio at 1:46-49 ("Therefore, each state to which a memory cell may be placed typically corresponds to a range of charge and/or a corresponding range of threshold voltages or drain currents.").

Figure 3A of Fazio "illustrate[s] possible state distributions for **digital** data storage applications."[4] MICRON-1005, Fazio at 5:4-5.

[4] Emphasis added unless otherwise noted.

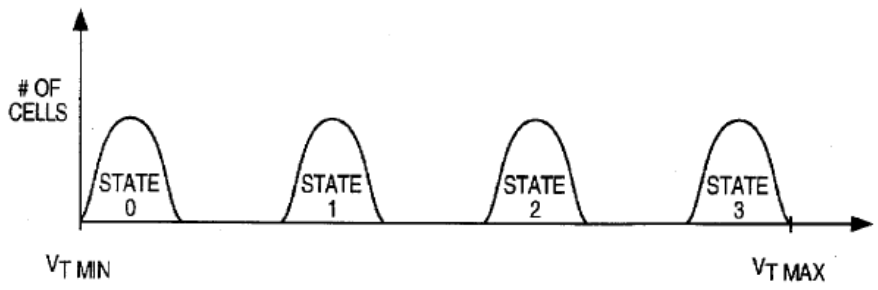


FIG. 3A

MICRON-1005, Fazio at Figure 3A.

The first step of the method disclosed in Fazio is to analyze the set of data to be programmed. *Id.* at 13:3-4, Figure 17. This is to detect which memory cells are to be programmed and to which "state" those cells will be programmed. MICRON-1005, Fazio at 13:3-19; MICRON-1003, Baker Decl. ¶ 48. Specifically, the first step correlates the data to be programmed with respective memory cells, thereby grouping the cells in "destination state[s]" (the destination states correspond to respective data values). *See* MICRON-1005, Fazio at 13:3-19.

The next step of the method is to employ parallel programming on multiple groups of cells. MICRON-1005, Fazio at 13:5-19. Specifically, in Figure 17, Fazio discloses programming multiple memory cells that have different destination states in parallel. *Id.* at 12:63-65; MICRON-1003, Baker Decl. ¶ 49.

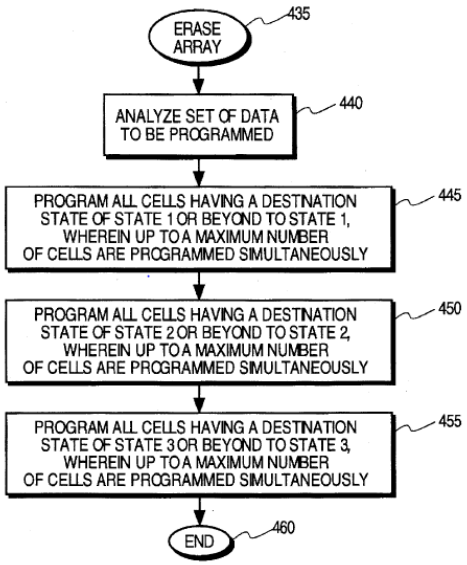


FIG. 17

MICRON-1005, Fazio at Figure 17.

First, all cells that are to be programmed to State 1 **or higher** are initially programmed to State 1. *See* MICRON-1005, Fazio at 12:65-13:1 ("The programming method of FIG. 17 recognizes that cells programmed to a destination state beyond a first program state must 'pass through' the first programmed state."). Next, any cells that are to be programmed to State 2 or higher are programmed to State 2. *See id.* at 13:9-12 ("Thus, some cells having a destination state of State 2, State 3, etc. are initially programmed to State 1. Process block 450 control engine programs all cells having a destination state of State 2 or beyond to State 2."). The cells that need to be programmed to State 2 can be programmed faster because they have been programmed initially to State 1, and do not have to begin their programming from a much lower threshold voltage. MICRON-1003,

Baker Decl. ¶ 50. Thus, like the 260 Patent, the method disclosed by Fazio teaches a quicker method of programming by giving groups of memory cells a "head start." *Id*.

In addition, Fazio teaches increasing the programming voltage for each successive programming of a group to a higher state. As explained in Fazio, "[p]rogramming in the saturated region occurs much more quickly if the gate voltage V_G is increased with each subsequent programming pulse." MICRON-1005, Fazio at 6:25-27. Figure 15 and associated text depicts this process, wherein the gate voltage ("V_G") progressively increases from V_{G1} to V_{G2} to V_{G3} for each successive programming step, wherein V_{G1}, $V_{G2,}$ and V_{G3} correspond to the desired threshold voltages for States 1, 2, and 3, respectively. *Id*. at 11:11-22; MICRON-1003, Baker Decl. ¶ 53.

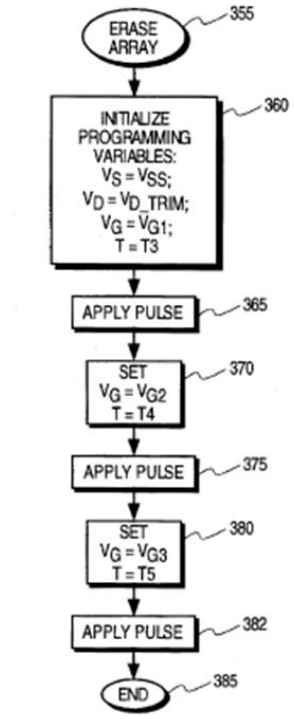


FIG. 15

MICRON-1005, Fazio at Figure 15.

Fazio does not describe in detail the structure and architecture of the conventional Flash memory cell. What Fazio is silent about, which is implicated by claim 5 of the 260 Patent, is how the bit lines are specifically connected to the memory cells. However, as discussed below, it would have been obvious to one of ordinary skill in the art to modify or supplement the teachings of Fazio with the conventional Flash memory structure and architecture disclosed in Terada.

8.2 U.S. PATENT NO. 4,858,194 ("TERADA")

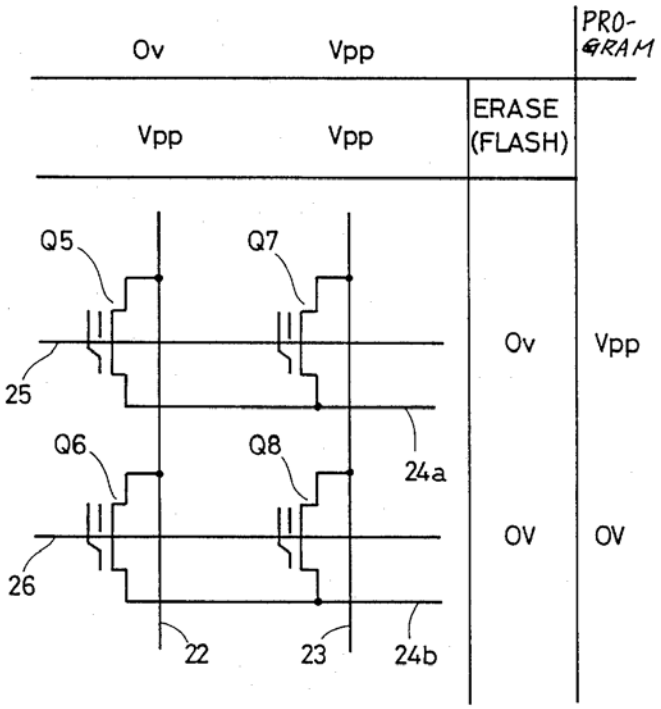
U.S. Patent No. 4,858,194 ("Terada") (MICRON-1006) was filed on February 10, 1988, and claims priority to a Japanese patent application filed on

July 21, 1987. Terada issued on August 15, 1989, to Yasushi Terada et al., and is entitled "Nonvolatile Semiconductor Memory Device Using Source Of A Single Supply Voltage." The original assignee of Terada was Mitsubishi Denki Kabushiki Kasisha. Terada is prior art to the 260 Patent under at least (pre-AIA) 35 U.S.C. § 102(b) because it issued more than one year before the earliest application to which the 260 Patent claims priority was filed.

Terada discloses the conventional Flash memory cell and its structure within a memory architecture. Fazio does not expressly describe the architecture of a Flash memory cell with respect to which part of the cells the bit lines connect. Specifically, Fazio does not explain that in conventional Flash memories, the bit lines connect to the drains of the Flash cells, and thus programming pulses are applied to the drains via bit lines. Terada, however, explains this well-known architecture in the context of background prior art.

Terada depicts Flash cells as known in the prior art shown below in Figure 1:

FIG. 1 PRIOR ART



MICRON-1006, Terada at Figure 1.

Terada explains that, as was conventional, the bit lines (22 and 23) connect to the drains of the transistors (Q5-Q8) of the respective memory cells. MICRON-1006, Terada at 1:24-41; MICRON-1003, Baker Decl. ¶ 56. Terada further explains that a program cycle, *i.e.*, programming the memory cells, involves applying a program high voltage to the drain (via the bit line), a program high voltage to the control gate (via the word line), and holding the source at ground. MICRON-1006, Terada at 2:18-41; MICRON-1003, Baker Decl. ¶ 56. This is

known as hot electron injection, and this injects elections onto the floating gate to modify the threshold voltage of the Flash memory cells. *See id.*

9. GROUND #1: CLAIMS 1-4 OF THE 260 PATENT ARE UNPATENTABLE AS OBVIOUS OVER FAZIO

As explained below, claims 1-4 of the 260 Patent are unpatentable as obvious over Fazio under 35 U.S.C. § 103(a). One of ordinary skill in the art would have understood Fazio in light of the basic knowledge of one of ordinary skill in the art to disclose all steps and limitations of the method in claims 1-4 of the 260 Patent.

9.1. Claim 1 is obvious over Fazio

9.1.1. [1.P] "A method for programming a nonvolatile memory device having a plurality of memory cells grouped in a plurality of blocks…"

Fazio discloses the claimed method of programming a nonvolatile memory device having a plurality of cells in a plurality of blocks. MICRON-1003, Baker Decl., Appx. A at claim [1.0]. Fazio describes a method of programming nonvolatile memory devices. *See* MICRON-1005, Fazio at 1:5-7 ("The present invention relates generally to memory devices and more particularly to methods for programming memory devices."); *id.* at 1:11-14 ("One type of prior **nonvolatile semiconductor memory** device is the flash electrically-erasable programmable read-only memory ('flash EEPROM')…"). The method of programming specifically occurs along blocks of memory cells. *See, e.g., id.* at 12:7-11

("Programming is often performed on a **'block' by block basis**, wherein a block of memory cells typically includes a single addressable byte or word of data. The programming of a block of memory cells occurs within a single 'programming cycle.'").

9.1.2. [1.1] "for storing multi-valued data represented as multi-valued threshold voltages,"

Fazio discloses storing multi-valued data represented as multi-valued threshold voltages. Fazio describes threshold voltages as "states." MICRON-1003, Baker Decl., Appx. A at claim [1.1]; MICRON-1005, Fazio at 2:32-34 ("[I]t is an object of the present invention to provide a method for more quickly placing a memory cell having **three or more analog states** to a desired state."). Figure 3A of Fazio depicts a programming distribution where the different states are represented as threshold voltages.

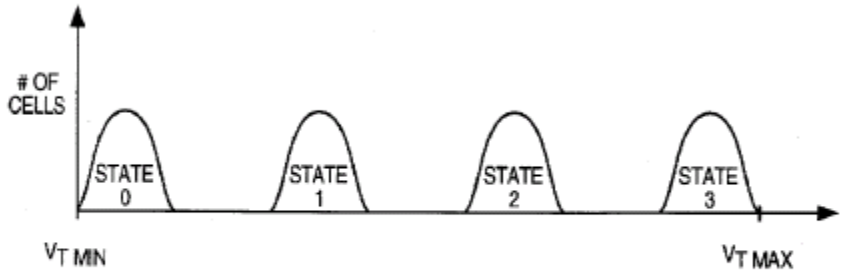


FIG. 3A

MICRON-1005, Fazio at Figure 3A.

Data may be of one of four values, represented as one of four states. MICRON-1005, Fazio at 4:38-42 ("FIG. 3A shows a programming distribution of the number of cells in a given state **versus the threshold voltage** of that state. As shown, **four states**, State 0, State 1, State 2, and State 3 **are defined within the programming window.**"); *see also id.* at 5:4-5 ("FIGS. 3A-3D illustrate possible state distributions for digital data storage applications).

9.1.3. [1.2] "said method comprising the step of detecting a plurality of program data to be programmed in said memory cells in one of said blocks,"

Fazio discloses the step of detecting a plurality of data to be programmed in memory cells within one block. MICRON-1003, Baker Decl., Appx. A at claim [1.2]; *see also, e.g.*, MICRON-1005, Fazio at 12:7-11 ("Programming is often performed on a **'block' by block basis**, wherein a block of memory cells typically includes a single addressable byte or word of data. The programming of a block of memory cells occurs within a single 'programming cycle.'").

Fazio teaches analyzing a set, or plurality, of data to be programmed within a block. In Figure 17, at process block 440, Fazio teaches the step of analyzing data to be programmed. *Id.* at 13:3-4 ("At process block 440, control engine 150 **analyzes the set of data to be programmed**."). By teaching the step of "analyz[ing]" the data to be programmed, Fazio teaches a method comprising

"detecting" the data to be programmed. MICRON-1003, Baker Decl., Appx. A at claim [1.2]; *see also, e.g.*, MICRON-1005, Fazio at Fig. 17 (step 440).

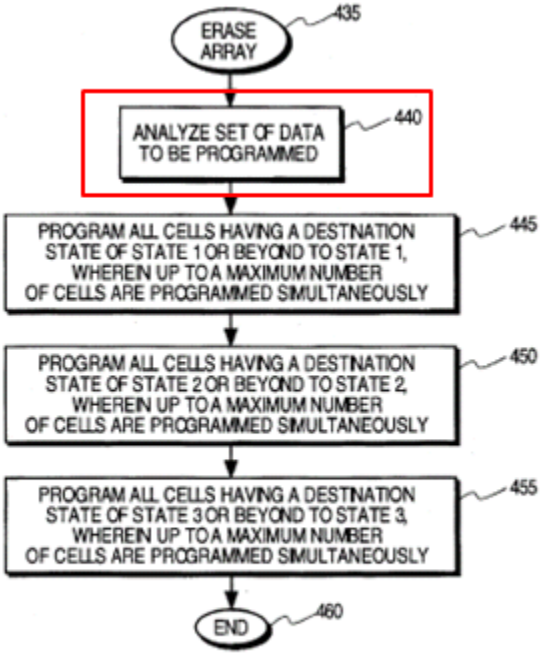


FIG. 17

MICRON-1005, Fazio at Figure 17 (annotated).

9.1.4. [1.3] "and further, upon detecting a first value to be programmed in a first group of said memory cells in said one of blocks and a second value to be programmed in a second group of said memory cells in said one of blocks,"

In Figure 17, Fazio teaches a method that includes the step of detecting data to be programmed ("analyze" in step 440), then programming data to different destination states (steps 445-455). *Id.* at 12:63-65 ("FIG. 17 shows an alternative data stream analysis method wherein memory cells having **differing destination**

states are programmed simultaneously."); *id.* at 13:9-10 ("some cells having a destination state of State 2, State 3, etc….").

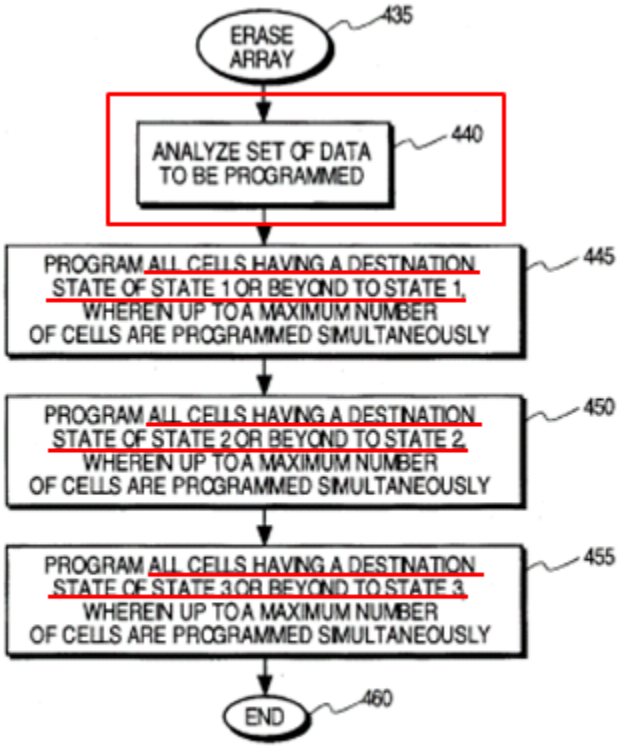


FIG. 17

MICRON-1005, Fazio at Figure 17 (annotated).

As explained above, Fazio describes "analyz[ing] the set of data to be programmed." *Id.* at 13:3-4. Fazio then describes programming groups of cells based on that analysis. *See id.* at 13:4-12 ("Control engine 150 ignores cells that are to remain in the erased state or State 0. At process block 445, control engine 150 programs all cells having a destination state of State 1 or beyond to State 1, wherein up to a maximum number of cells are programmed simultaneously. Thus,

some cells having a destination state of State 2, State 3, etc. are initially programmed to State 1. Process block 450 control engine programs all cells having a destination state of State 2 or beyond to State 2."). Thus, Fazio discloses correlating the data to be programmed with the memory cells.

Further, because the steps following step 440 require programming specific cells having a destination state of "State 1 or Beyond to State 1" and "State 2 or Beyond to State 2," one of ordinary skill in the art would appreciate that the step of analyzing the set of data to be programmed, which will be programmed to "different destination states," includes detecting which cells are to be programmed to which states. MICRON-1003, Baker Decl., Appx. A at claim [1.3]. In other words, to the extent that Fazio does not expressly disclose this limitation, it would have been obvious to a person of ordinary skill in the art because the data to be programmed must be correlated to the memory cells so that the cells having different destination states can be identified. A person of ordinary skill in the art would have understood with a given data set, the cells that the data will be written to must be identified so that, in fact, the data can be written to memory. Accordingly, it would have been obvious to one of ordinary skill in view of Fazio that a first value is detected to be programmed in a first group of said memory cells in said one of blocks and a second value is detected to be programmed in a second

group of said memory cells in said one of blocks. MICRON-1003, Baker Decl., Appx. A at claim [1.3].

9.1.5. [1.4] "the steps of consecutively applying a first programming voltage, which corresponds to said first value, to said first group and said second group maintained at a first potential,"

Fazio discloses the step of consecutively applying a first voltage, corresponding to a first value, to the first and second group of data to be programmed. MICRON-1003, Baker Decl., Appx. A at claim [1.4].

First, Fazio teaches applying a programming voltage, i.e., "a voltage applied to a control gate of a memory cell" (proposed construction). While Fazio uses the term "select gate," one of ordinary skill in the art would have understood that it is the same as a "control gate." MICRON-1003, Baker Decl., Appx. A at claim [1.4]; MICRON-1005, Fazio at 5:21-23 ("The select gate 30 of flash memory cell 25 is connected to a programming voltage V_G.").

Fazio also teaches the first consecutive step of applying a first programming voltage ("V_{G1}"), which corresponds to a first value, in Figure 15.

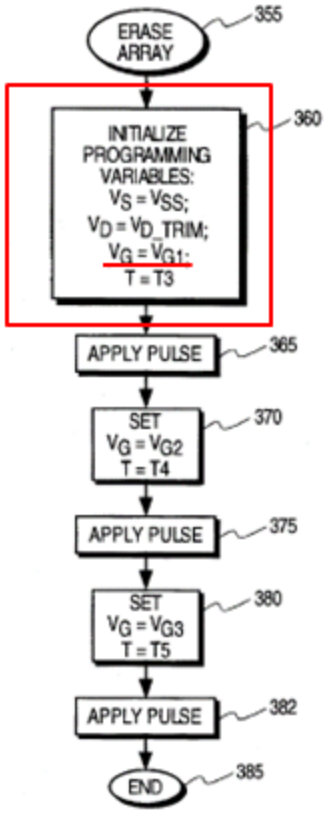


FIG. 15

MICRON-1005, Fazio at Figure 15 (annotated).

Fazio teaches setting the programming voltage to a first value, represented as V_{G1}. MICRON-1005, Fazio at 11:35-37 ("The programming variables are initialized at processing block 360, wherein the gate voltage is initialized to be V_{G1} . . .").

Fazio then teaches applying the first program voltage to a first and second group such that the threshold voltage of the cells reaches the level for State 1. Specifically, in Figure 17, the method includes the step of programming all cells that have a destination of State 1 or beyond to State 1. *Id.* at 13:4-7 ("Control engine 150 ignores cells that are to remain in the erased state or State 0. At

process block 445, control engine 150 **programs all cells having a destination state of State 1 or beyond to State 1**…").

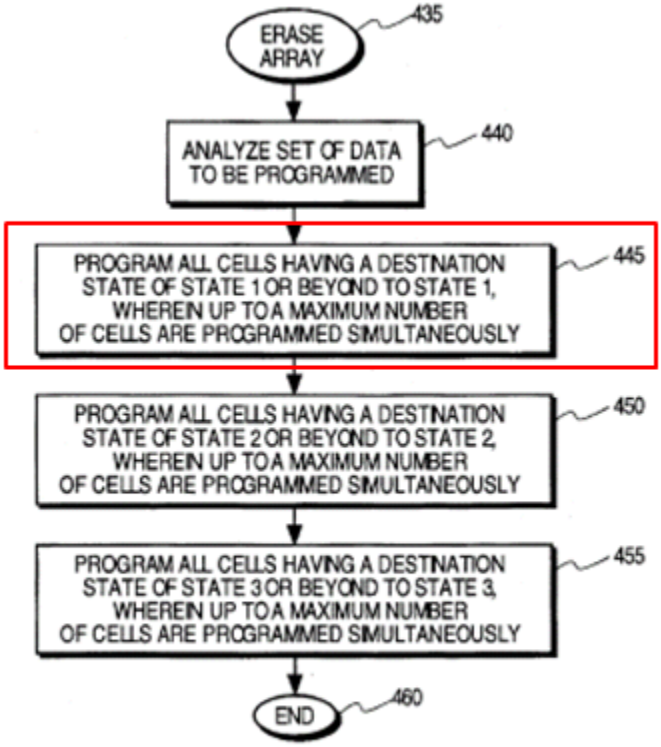


FIG. 17

MICRON-1005, Fazio at Figure 17 (annotated).

See also id. at Figure 3A (showing State 1 and State 2 represented by a range of threshold voltages (V_T)) and Figure 5 (showing how the threshold voltages are increased by application of different gate voltages (V_G) over a period of time.) Fazio also teaches applying the first programming voltage, V_{G1}, to a first group, which are any cells that are to be programmed to State 1, as well as a second group, which are the cells that are to be programmed to State 2. *Id.* at 13:9-10

("**some cells having a destination state of State 2, State 3, etc. are initially programmed to State 1**"). The first programming voltage is applied to these two groups simultaneously. *Id.* at 13:8-9 ("cells are programmed simultaneously").

Fazio also discloses that first group and the second group are maintained at a first potential. Specifically, the sources of the cells are held at ground and the drains are held at the programming drain voltage. MICRON-1005, Fazio at 5:34-48 ("As shown, **source 40 is coupled to system ground VSS, and drain 45 is coupled to a drain voltage V_D.** The difference in potential between the drain 45 and the source 40 creates a 'horizontal' electric field that accelerates electrons from the source 40 across the channel towards the drain 45. For one embodiment, it is sufficient for V_D to be 5-7 volts greater than the voltage at source 40. Electron flow in the horizontal electric field is shown as an arrow having its head at drain 45 and its tail at source 40. This substantially shows the direction of electron flow across the channel. The accelerated or 'hot' electrons collide with the lattice structure of the substrate 50, and some of the hot electrons are swept onto the floating gate by the vertical electric field. In this manner, the amount of charge stored on the floating gate may be increased."). In other words, Fazio discloses that when cells are being programmed (here, the first and second groups), their sources are held at ground and their drains are held at a drain voltage to enable the programming. *See also* MICRON-1003, Baker Decl., Appx. A at claim [1.4].

After this step, the threshold voltages for the first and second groups are at a first level (State 1), and the programming will continue with the next step below. MICRON-1005, Fazio at 13:9-10.

9.1.6. [1.5] "and applying a second programming voltage, which corresponds to said second value, to said second group."

Fazio discloses the second consecutive step of applying a second programming voltage, which corresponds to a second value, to the second group of cells.

First, Fazio teaches the step of applying a second programming voltage, which corresponds to a second value in Figure 15. MICRON-1003, Baker Decl., Appx. A at claim [1.5].

Fazio teaches applying a programming voltage, i.e., "a voltage applied to a control gate of a memory cell" (proposed construction). While Fazio uses the term "select gate," one of ordinary skill in the art would have understood that it is the same as a "control gate." MICRON-1003, Baker Decl., Appx. A at claim [1.5]; MICRON-1005, Fazio at 5:21-23 ("The select gate 30 of flash memory cell 25 is connected to a programming voltage V_G.")

Fazio teaches setting the programming voltage to a second value, represented as V_{G2}. MICRON-1005, Fazio at 11:41-45 ("At process block 370 control engine 150 **sets the programming voltage to V_{G2}** and the pulse width to

T4, wherein T4, is selected to result in saturation programming for a programming gate voltage of $V_{G2.}$").

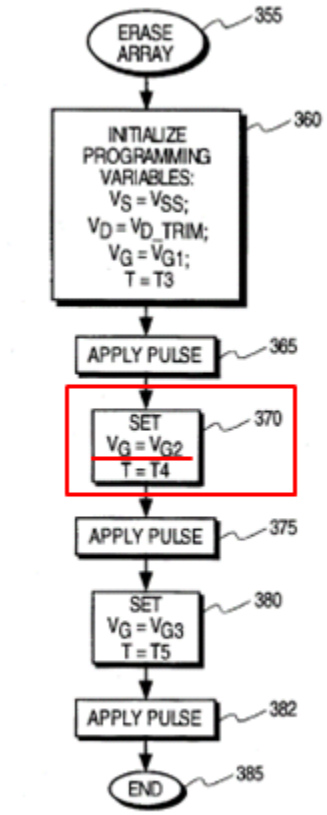


FIG. 15

MICRON-1005, Fazio at Figure 15 (annotated).

This second voltage is then applied to program cells to the second value, State 2. *Id.* at 11:45-46 ("At process block 375, control engine 150 applies a programming pulse to place selected cells in State 2.").

Second, Fazio teaches applying this voltage to the second group. MICRON-1003, Baker Decl., Appx. A at claim [1.5]. Specifically, in FIG. 17, the method includes the step of programming a second group, which includes the cells that

have the destination of State 2 or beyond, to State 2. MICRON-1005, Fazio at 13:11-14 ("Process block 450 control engine programs all cells having a destination state of State 2 or beyond to State 2. Again, up to a maximum number of cells are programmed simultaneously.").

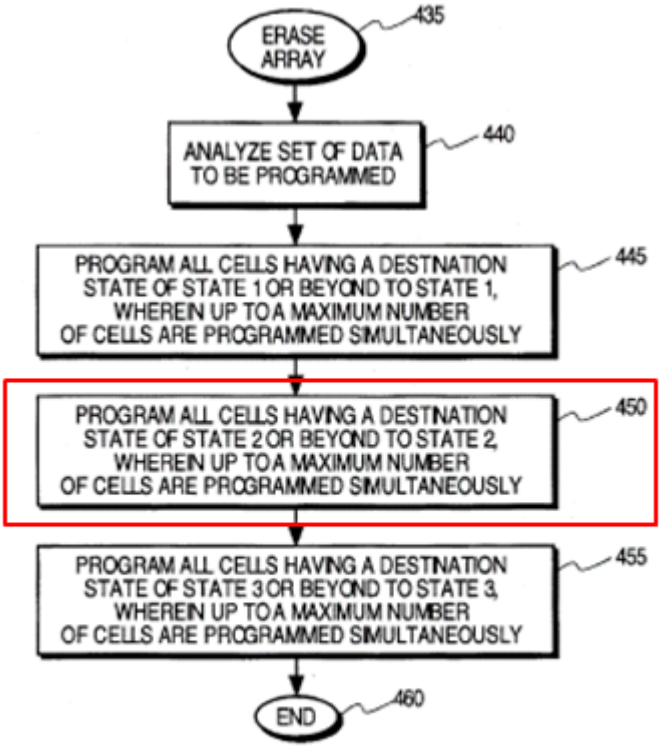


FIG. 17

MICRON-1005, Fazio at Figure 17 (annotated).

Fazio specifically teaches that these steps, applying a first programming voltage, then a second programming voltage, are consecutive. *Id.* at 11:54-64 ("The process shown in FIG. 15 may be formed in a 'carry along' manner wherein all cells of the array that are to be programmed receive all programming pulses

until they have received the programming pulse that places them to the desired state. For example, the first programming pulse is applied to all the cells of the array that are to be programmed. Those cells that are to be programmed only to the State 1 are deselected to prevent further programming, and all cells that are to be programmed to State 2 and subsequent states receive the second pulse. State 2 cells receive no further programming.").

9.2. Claim 2 is obvious over Fazio

9.2.1. [2.0] "A method as defined in claim 1, wherein said second programming voltage with respect to said first potential is larger than said first programming voltage with respect to said first potential."

Fazio discloses that, within the method described above, the second programming voltage is larger than the first programming voltage with respect to the said first potential. MICRON-1003, Baker Decl., Appx. A at claim [2]. Specifically, the programming gate voltage associated with each state increases with each of the four states. MICRON-1005, Fazio at 11:12-22 ("[G]iven a four state memory cell wherein the lowest state is State 0 and the highest state is State 3, it is sufficient that a gate voltage associated with each state follow the following order: $V_{G0}<V_{G1}<V_{G2}<V_{G3}$ wherein V_{G0} defines the threshold voltage level for a memory cell in state 0, V_{G1} defines the threshold voltage level for a memory cell in State 1, V_{G2} defines the threshold voltage level for a memory cell in State 2, and V_{G3} defines the threshold voltage level for a memory cell in State 3."); *see also*

MICRON-1003, Baker Decl., Appx. A at claim [2]. Because the second programming voltage is larger than the first programming voltage, the second programming voltage with respect to said first potential is larger than said first programming voltage with respect to said first potential. MICRON-1003, Baker Decl., Appx. A at claim [2]. In other words, the second programming voltage is larger whether the first potential is the drain, source, or difference between drain and source). *See id.*

Fazio also teaches, in Figure 15, that the gate voltages are to be set to V_{G1}, then V_{G2}, then V_{G3} sequentially. *See* MICRON-1005, Fazio at Figure 15. As explained in Fazio, "[p]rogramming in the saturated region occurs much more quickly if the gate voltage V_G is increased with each subsequent programming pulse." *Id.* at 6:25-27.

9.3. Claim 3 is obvious over Fazio

9.3.1. [3.0] "A method as defined in claim 1 wherein, upon detecting a third value to be programmed in a third group of said memory cells in said one of blocks in addition to said first and second groups,"

Fazio teaches a programming method that can also program a third group of cells. MICRON-1003, Baker Decl., Appx. A at claim [3.0]. Specifically, in Figure 17, Fazio shows a third value to be programmed in a third group of memory cells. MICRON-1005, Fazio at 12:63-65 ("FIG. 17 shows an alternative data stream analysis method wherein memory cells **having differing destination states** are

programmed simultaneously."), 13:9-10 ("some cells having a destination state of State 2, **State 3**, etc."); *see also* above analysis of claim [1.3].

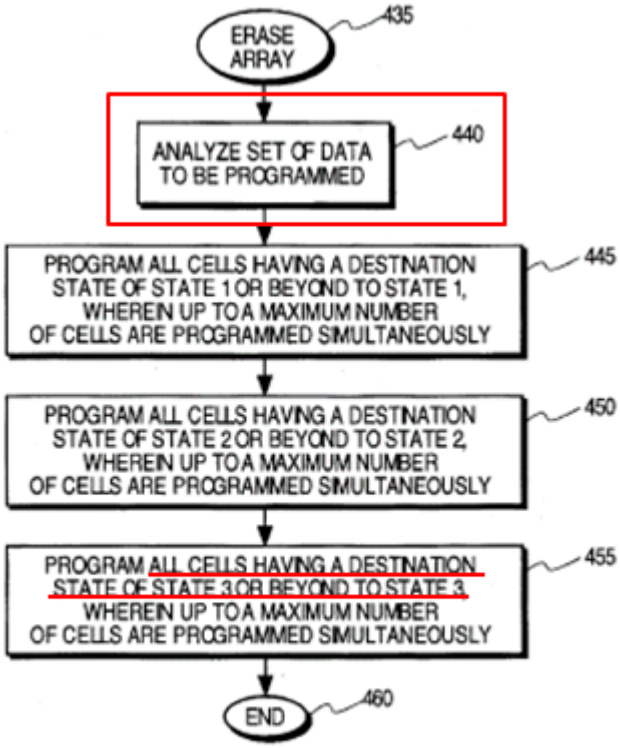


FIG. 17

MICRON-1005, Fazio at Figure 17 (annotated).

As explained in Section 9.1.4 (at claim [1.3]), Fazio describes "analyz[ing] the set of data to be programmed." MICRON-1005, Fazio at 13:3-4. Fazio then describes programming groups of cells based on that analysis. *See id.* at 13:4-12 ("Control engine 150 ignores cells that are to remain in the erased state or State 0. At process block 445, control engine 150 programs all cells having a destination state of State 1 or beyond to State 1, wherein up to a maximum number of cells are

programmed simultaneously. Thus, some cells having a destination state of State 2, State 3, etc. are initially programmed to State 1. Process block 450 control engine programs all cells having a destination state of State 2 or beyond to State 2."). Thus, Fazio discloses correlating the data to be programmed with the memory cells.

Further, because the steps following step 440 require programming specific cells having a destination state of "State 3," one of ordinary skill in the art would appreciate that the step of analyzing the set of data to be programmed, which will be programmed to "different destination states," includes detecting which cells are to be programmed to which states. MICRON-1003, Baker Decl., Appx. A at claim [3.0]. In other words, to the extent that Fazio does not expressly disclose this limitation, it would have been obvious to a person of ordinary skill in the art because the data to be programmed must be correlated to the memory cells so that the cells having different destination states can be programmed to those states as described. A person of ordinary skill in the art would have understood with a given data set, the cells that the data will be written to must be identified so that, in fact, the data can be written to memory. MICRON-1003, Baker Decl., Appx. A at claim [3.0]. Accordingly, it would have been obvious to one of ordinary skill in view of Fazio that a third value is detected to be programmed in a third group of

said memory cells in said one of blocks in addition to said first and second groups. *Id.*

9.3.2. [3.1] "first and second programming voltage applying steps apply said first programming voltage and said second programming voltage to said third group,"

Fazio discloses applying the first and second programming gate voltages to the third group of cells in Figure 17. MICRON-1003, Baker Decl., Appx. A at claim [3.1]. Specifically, Fazio teaches programming all cells having a destination state of State 1 or beyond to State 1 simultaneously, then programming all cells having a destination state of State 2 or beyond to State 2 simultaneously. MICRON-1005, Fazio at 13:6-14 ("At process block 445, control engine 150 programs all cells having a destination state of State 1 or beyond to State 1, wherein up to a maximum number of cells are programmed simultaneously. Thus, **some cells having a destination state of State 2, State 3**, etc. **are initially programmed to State 1**. Process block 450 control engine programs all cells **having a destination state of State 2 or beyond to State 2**. Again, up to a maximum number of cells are programmed simultaneously.").

Cells that are to be programmed to State 3 are those that are to be programmed "beyond" States 1 and 2.

9.3.3. [3.2] "and said method comprises the step of applying a third programming voltage, which corresponds to said third value, to said third group."

Fazio discloses that the method comprises the step of applying a third programming voltage, which corresponds to a third value, to a third group of cells. MICRON-1003, Baker Decl., Appx. A at claim [3.2]; *see also* above analysis in Section 9.1.4 and 9.1.5.

Fazio teaches applying a programming voltage, i.e., "a voltage applied to a control gate of a memory cell" (proposed construction). MICRON-1003, Baker Decl., Appx. A at claim [3.2]. While Fazio uses the term "select gate," one of ordinary skill in the art would have understood that it is the same as a "control gate." *Id.*; MICRON-1005, Fazio at 5:21-23 ("The select gate 30 of flash memory cell 25 is connected to a programming voltage V_G.").

Fazio teaches applying a third programming gate voltage, which corresponds to a third value in Figure 15. MICRON-1005, Fazio at 11:46-51 ("At process block 380, control engine 150 sets the programming gate voltage to V_{G3} and sets the pulse width to T5, wherein T5 is selected to result in saturation programming given the programming gate voltage V_{G3}. A pulse is applied at process block 382 to place selected cells in State 3….").

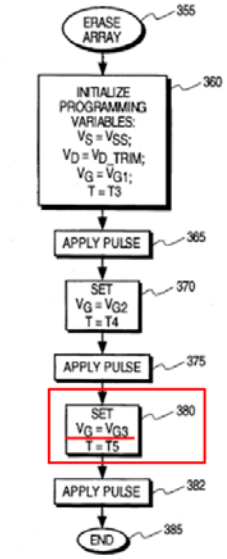


FIG. 15

MICRON-1005, Fazio at Figure 15 (annotated).

Fazio also teaches applying the third programming pulse to a third group of cells in Figure 17. *Id.* at 13:13-16 ("At process block 455, control engine 150 programs all cells having a destination state of State 3 or beyond to State 3. Again, up to a maximum number of cells are programmed simultaneously.").

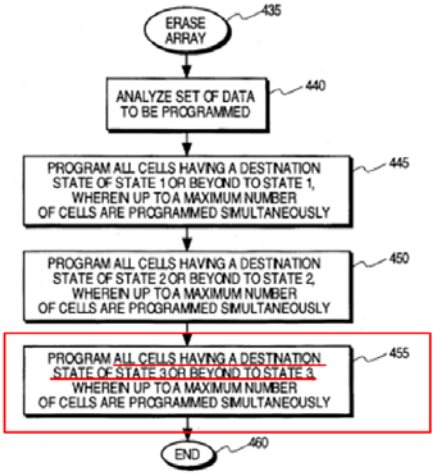


FIG. 17

MICRON-1005, Fazio at Figure 17 (annotated).

Because Fazio teaches applying a third programming gate voltage, which corresponds to a third value, to a third group of cells, it discloses this claim element. MICRON-1003, Baker Decl., Appx. A at claim [3.2].

9.4. Claim 4 is obvious over Fazio

9.4.1. [4.0] "A method as defined in claim 3, wherein said third programming voltage with respect to said first potential is larger than said second programming voltage with respect to said first potential."

Fazio discloses that the third programming gate voltage is larger than the first and second programming voltages. *See* above analysis of claim [2] wherein the third programming voltage (V_{G3}) is larger than the second programming voltage; MICRON-1005, Fazio at 11:12-16 ("[G]iven a four state memory cell wherein the lowest state is State 0 and the highest state is State 3, it is sufficient that a gate voltage associated with each state follow the following order: $V_{G0}<V_{G1}<V_{G2}<V_{G3}$. . ."). The first potential voltage is, for example, the drain voltage, source voltage, or difference between the source and drain voltage. In each case, the third programming voltage is larger than the second programming voltage with respect to said first potential because the third programming voltage is larger than said second programming voltage. MICRON-1003, Baker Decl., Appx. A at claim [4].

10. GROUND #2: CLAIM 5 OF THE 260 PATENT IS UNPATENTABLE AS OBVIOUS OVER FAZIO IN VIEW OF TERADA

As explained below, claim 5 of the 260 Patent is unpatentable as obvious over Fazio in view of Terada under 35 U.S.C. § 103(a).

10.1.1. It would have been obvious to a person of ordinary skill in the art to combine Fazio with Terada

It would have been obvious to a person of ordinary skill in the art to combine Fazio with Terada. MICRON-1003, Baker Decl. ¶ 60. Fazio and Terada both relate to Flash memories. *Id.* Fazio teaches a "head start" programming approach that would be applicable to a wide variety of memory architectures. MICRON-1003, Baker Decl. ¶¶ 50, 61; MICRON-1005, Fazio at 1:5-7 ("The present invention relates generally to memory devices and more particularly to methods for programming memory devices."). Terada describes the typical architecture for a Flash memory. MICRON-1003, Baker Decl. ¶¶ 55-56; MICRON-1006, Terada at 1:24-41, 2:18-41. Specifically, Terada describes the basic architecture as known in the art, in more detail, and specifies that addressable word lines and bit lines connect to the memory cells for programming and reading the memory cells. One of ordinary skill in the art would have understood that the teachings of Fazio are applicable to architectures as described in Terada. MICRON-1003, Baker Decl. ¶¶ 60-61. In fact, one of ordinary skill would have had to look to architectures, such as the one described in Terada, to apply Fazio's

programming method, as Fazio does not specifically address how the bit lines connect to the memory cells. *Id.* at ¶ 60.

It would have been obvious to one of ordinary skill in the art to adapt Fazio in light of Terada and specify that Fazio applies to memory cells in which the bit lines connect to the drains of the cells. *Id.* at ¶ 61. One of ordinary skill in the art would have been motivated to make this adaption for several reasons. First, as noted above, one of ordinary skill in the art would have been motivated to apply the Fazio programming teachings to a memory with addressable cells, as described in Terada. *Id.* Indeed, given that Terada discloses such an architecture as background prior art, those of ordinary skill in the art would have been motivated to incorporate Fazio's teachings into conventional, tested architectures such as the one set forth by Terada. *Id.* That is, the architecture described in Terada could be combined with the method in Fazio, and this combination would be understood by one of ordinary skill in the art as producing predictable results. *Id.*

The architecture described in Terada was a known architecture for Flash memory, and Fazio's teachings are applicable to Flash memory architectures and would improve their programming by providing the "head start" to certain memory cell groups. *Id.* The combination is merely applying the programming of Fazio to the well-known architecture of Terada.

Finally, applying the method taught in Fazio to the conventional architecture in Terada is nothing more than a design choice. MICRON-1003, Baker Decl. ¶ 62. Fazio teaches a general Flash programming approach that utilizes a voltage on the drains of Flash cells. However, Fazio does not specify that the bit lines connect to the drains of the cells, which are implicated in carrying out the programming method. Yet Terada describes the conventional Flash architecture, wherein bit lines connect to the drains of Flash cells. Thus, one of ordinary skill in the art would have understood that adopting the architecture of Terada in performing the method in Fazio was a design choice, which would yield predictable results given that the architecture in Terada was conventional and compatible with Fazio's teachings. *Id.* at ¶ 62.

For these reasons, it would have been obvious to one of ordinary skill in the art to combine Fazio with Terada.

10.2. Claim 5 is obvious over Fazio in view of Terada

10.2.1. [5.P] "A method as defined in claim 1, wherein…"

Fazio discloses this claim element, as explained in the above analysis of claim [1].

10.2.2. [5.1] "said first and second programming voltages are applied to control gates of said first and second groups of memory cells through a corresponding word line,"

Fazio discloses a method wherein memory cells are programmed by applying first and second programming voltages to control gates through

corresponding word lines. MICRON-1003, Baker Decl., Appx. A at claim [5.1]. First, Fazio discloses a memory cell with a "select gate" which one of ordinary skill in the art would have understood is the same as a "control gate." *Id.*; MICRON-1005, Fazio at 3:46-47 ("FIG. 2 shows a nonvolatile memory cell 25 having a select gate 30, a floating gate 35, a source 40, and a drain 45."). Second, Fazio teaches that the gates of the memory cells are connected to a word line. MICRON-1005, Fazio at 1:19-21 ("The flash memory cell is read by applying a select voltage via a wordline to the select gate."). By teaching a method of programming where voltages are applied to gates and where the gates are connected to a corresponding word line, Fazio discloses this claim element.

10.2.3. [5.2] "and select pulses are applied to drains of said first and second groups of memory cells through corresponding bit lines at timings of said first and second programming voltages."

Fazio teaches a method where select pulses are applied to the drains of the memory cells through corresponding bit lines at the times of the first and second programming gate voltages. MICRON-1003, Baker Decl., Appx. A at claim [5.2].

First, Fazio teaches applying a programming pulse to the drains of the select memory cells to be programmed. MICRON-1005, Fazio at 1:64-67 ("A **programming pulse**, which **comprises applying appropriate voltages to** the select gate, source, and **drain** of each selected flash memory cell for a predetermined amount of time, is applied to the selected flash memory cell…"),

2:12-15 ("If the selected flash memory cell is not in the programmed state, programming pulses are applied to the selected flash memory cell until it is successfully placed to the programmed state."), 5:38-40 ("For one embodiment, it is sufficient for V_D to be 5-7 volts greater than the voltage at source 40.").

Second, Fazio teaches programming different groups of cells with different programming voltages. *See* analysis above in Section 9.1. Fazio also teaches that each state has a corresponding threshold voltage or drain current. MICRON-1005, Fazio at 1:45-48 ("[E]ach state to which a memory cell may be placed typically corresponds to a range of charge and/or a corresponding range of threshold voltages or drain currents."). Fazio further teaches that the pulse width is the duration that the programming gate and drain voltages are applied to select memory cells. *Id.* at 5:49-56 ("The state to which a non-volatile memory is placed is determined by the gate voltage V_G, the drain voltage V_D, the effective channel length L_{eff} of the memory cell, temperature, and pulse width, wherein **the pulse width is the duration for which the programming gate voltage V_G and the programming drain voltage V_D are applied to the memory cell.** As will now be discussed, the programming gate voltage V_G is of primary significance."); MICRON-1003, Baker Decl., Appx. A at claim [5.2].

Third, Terada discloses that the voltage is applied to the drains of flash memory cells through their bit lines. MICRON-1006, Terada at 1:24-41;

MICRON-1003, Baker Decl. ¶ 55. Terada further explains that a program cycle, *i.e.*, programming the memory cells, involves applying a program high voltage to the drain (via the bit line), a program high voltage to the control gate (via the word line), and holding the source at ground. MICRON-1006, Terada at 2:18-41; MICRON-1003, Baker Decl. ¶ 56.

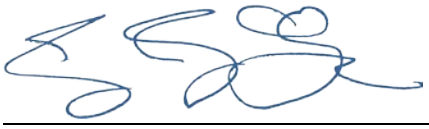
Accordingly, it would have been obvious to one of ordinary skill in the art, under Fazio in view of Terada, that select pulses are applied to drains of said first and second groups of memory cells through corresponding bit lines at timings of said first and second programming voltages.

11. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1-5 of the 260 Patent is requested.

Respectfully submitted,

Dated: October 26, 2015

By: 

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	October 27, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 5,943,260 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1006
Persons served	Patent Owner's Address of Record: Foley & Lardner LLP 3000 K Street NW Suite 500 P.O. Box 25696 Washington, DC 20007-8696 Additional Address Known as Likely to Effect Service: Jon A. Birmingham Fitch Even Tabin & Flannery LLP 21700 Oxnard Street Suite 1740 Woodland Hills, CA 91367

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