UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 5,894,441
Title: SEMICONDUCTOR MEMORY DEVICE
WITH REDUNDANCY CIRCUIT

Petition For *Inter Partes* Review of U.S. Patent No. 5,894,441 Under 35 U.S.C §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

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Exhibit List

Micron Exhibit #	*Description*
MICRON-1001	U.S. Patent No. 5,895,441 ("the 441 Patent")
MICRON-1002	File History for U.S. Patent No. 5,894,441
MICRON-1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 5,270,975 ("McAdams")
MICRON-1006	Japanese Patent Application No. H06-052696 ("Minami")
MICRON-1007	Excerpts from Betty Prince, *Semiconductor Memories* (2d ed. 1992) ("Prince")

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100, Micron Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-3 and 5-15 of U.S. Patent No. 5,894,441, titled "Semiconductor Memory Device With Redundancy Circuit" (MICRON-1001, "the 441 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 441 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 441 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang (Reg. No. 73604) (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Justin L. Constant (Reg. No. 66883) (justin.constant@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5217; F: 713-224-9511

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for the Petitioner is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. (*See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.)

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Limestone has asserted the 441 Patent and U.S. Patent Nos. 5,805,504 ("the 504 Patent"), 6,233,181 ("the 181 Patent"), 5,943,260 ("the 260 Patent"), and 6,697,296 ("the 296 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Limestone Memory Sys. LLC v. Micron Tech., Inc.*, 8:15-cv-00278 (C.D. Cal.) ("Co-Pending Litigation"). Limestone has also asserted one or more of the asserted patents in the following actions: *Limestone Memory Sys. LLC v. OCZ Storage Solutions, Inc.*, 8:15-cv-00658 (C.D. Cal.) (the 504, 441, 181 and 296 Patents); *Limestone Memory Sys. LLC v. PNY Techs., Inc.*, 8:15-cv-00656 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Lenovo (US) Inc.*, 8:15-cv-00650 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Kingston Tech. Co. Inc.*, 8:15-cv-00654 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Transcend Info., Inc. (California)*, 8:15-cv-00657 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Acer America Corp*., 8:15-cv-00653 (C.D. Cal.) (the 504, 441, 260,

181, and 296 Patents); *Limestone Memory Sys. LLC v. Dell Inc.*, 8:15-cv-00648 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Hewlett-Packard Co.*, 8:15-cv-00652 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); and *Limestone Memory Sys. LLC v. Apple Inc.*, 8:15-cv-01274 (C.D. Cal.) (the 504, 441, 181, and 296 Patents).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 5,805,504, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 6,233,181, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 5,943,260, IPR2015-Unassigned (to be filed concurrently); and Petition for *Inter Partes* Review of U.S. Patent No. 6,697,296, IPR2015-Unassigned (to be filed concurrently).

The 441 Patent claims priority to foreign patent application JP-09-081203. The 441 Patent does not claim priority to any other U.S. patent applications.

2.5. Fee for Inter Partes Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 441 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Ground #1: Claims 1-3, and 5 are invalid under (pre-AIA) 35 U.S.C. § 102(b) on the ground that they are anticipated by U.S. Patent No. 5,270,975, to McAdams ("McAdams"), entitled "Memory Device Having A Non-Uniform Redundancy Decoder Arrangement," filed with the USPTO on August 13, 1992, issued December 14, 1993. McAdams is attached as MICRON-1005.

Ground #2: Claims 3 and 6-15 are invalid under (pre-AIA) 35 U.S.C. § 103 on the ground that they are obvious over McAdams in view of Japanese Patent Application No. H06-052696 ("Minami"), which was filed on July 31, 1992 and was published on February 25, 1994. Minami is attached as MICRON-1006.

These grounds are explained below and are supported by the Declaration of Dr. R. Jacob Baker (MICRON-1003, "Baker Decl.").

4. OVERVIEW OF THE 441 PATENT

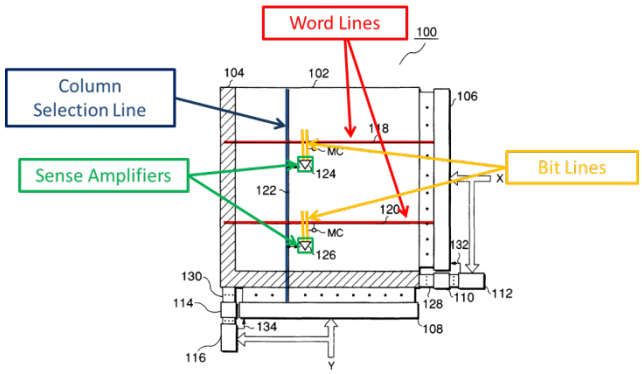
The 441 Patent was filed on March 31, 1998 and issued on April 13, 1999. The 441 Patent is directed to a semiconductor memory device that purportedly enhances the relief efficiency of defective bit lines by means of redundant bit lines. MICRON-1001, 441 Patent at Abstract.

In a semiconductor memory device, memory cells are located in a grid at the intersection of word lines and bit lines. MICRON-1001, 441 Patent at Figure 2; MICRON-1003, Baker Decl. at ¶ 27. As a general matter, word lines run in the row direction whereas bit lines run in the column direction. MICRON-1003, Baker Decl. at ¶¶ 27-28. Column selection lines are associated with the bit lines and also run in the column direction. MICRON-1001, 441 Patent at Figure 2; MICRON-1003, Baker Decl. ¶¶ 27-28.

Almost all semiconductor memory devices include defective components. MICRON-1001, 441 Patent at 1:14-17; MICRON-1003, Baker Decl. ¶ 29. So that the devices can operate with such defects, it has long been general practice to include redundancy circuits that allow the manufacturer to disable the use of a defective component and replace it with a redundant one. MICRON-1001, 441 Patent at 1:18-22; MICRON-1003, Baker Decl. ¶¶ 29, 30. To replace the maximum number of defective word lines or bit lines, it is desirable to include as many redundant components, *e.g.*, redundant word lines and/or bit lines, as practicable. MICRON-1001, 441 Patent at 1:34-37; MICRON-1003, Baker Decl. ¶ 29. However, these redundant word and/or bit lines, and the corresponding redundancy circuitry to activate and utilize those redundant components come at a cost since they require additional silicon space. MICRON-1001, 441 Patent at 1:37-42; MICRON-1003, Baker Decl. ¶ 30. The 441 Patent purports to increase

the relief efficiency of redundant bit lines so that fewer redundant lines are needed, thus reducing cost and space needed for redundancy circuitry. MICRON-1001, 441 Patent at 2:8-13; MICRON-1003, Baker Decl. ¶ 30.

The alleged invention is directed to a semiconductor device with a divided bit line architecture. MICRON-1001, 441 Patent at 3:1-2. This means that, "in the same column, a bit line is divided into plural parts . . . ." MICRON-1001, 441 Patent at 3:23-27. This structure is depicted in Figure 1.



MICRON-1001, 441 Patent at Figure 1 (annotated).

The above annotated Figure 1 depicts a single column selection line (122) that is connected to multiple sense amplifiers (124, 126). MICRON-1001, 441 Patent at 3:22-34; MICRON-1003, Baker Decl. ¶ 32. These sense amplifiers are each connected to different bit lines. *Id*. These bit lines, respectively, intersect two different word lines (118, 120). MICRON-1001, 441 Patent at 3:18-34; MICRON-1003, Baker Decl. ¶ 32. The memory cells (MC) are at the intersection of the word lines and the bit lines. *Id.* This is called a divided bit line architecture

because there are multiple bit lines along a single column that are selected by a single column selection line. MICRON-1003, Baker Decl. ¶¶ 31-32.

When a memory cell is written or read, a column and row address are provided that specify the particular memory cell. MICRON-1003, Baker Decl. ¶ 33; MICRON-1001, 441 Patent at 3:6-9. As shown in Figure 1, which shows a prior art architecture, the row address X is provided to the row decoder 106 which activates the appropriate word line, and the column address Y is provided to the column decoder 108 which activates the designated column select line. MICRON-1001, 441 Patent at 3:9-16. "[W]hen the column selection line 122 is activated in response to a Y address, [multiple] sense amplifiers are selected simultaneously." *Id.* at 3:28-31. "However, only the data corresponding to an activated word line is selected finally out of the [multiple] selected sense amplifiers, and is readout." *Id.* at 3:32-34.

As shown in Figure 1, the column address Y is also provided to a redundancy column decoder 116. MICRON-1003, Baker Decl. ¶ 34; MICRON-1001, 441 Patent at 3:6-9. If the column address corresponds to a column with a defective bit line, then the column redundancy decoder causes a redundant column selection line (with redundant bit lines) to be activated. MICRON-1003, Baker Decl. ¶ 35; MICRON-1001, 441 Patent at 3:53-60. The regular column decoder 108 is also inhibited from activating the column with a defective bit line. *Id.*

According to the 441 Patent, the problem with the approach depicted in Figure 1 is that all of the bit lines along a single column are replaced even if only one of the bit lines is defective. MICRON-1001, 441 Patent at 3:62-65. The 441 Patent purports to correct this inefficiency by enabling a single redundant column selection line to partially replace components from different columns. MICRON-1003, Baker Decl ¶ 37; *see also* MICRON-1001, 441 Patent at 7:25-29 ("In other words, half of the single redundant column selection line 230 replaces half of the column selection line 222, and the remaining half of the same redundant column selection line 230 replaces half of the column selection line 290."). This is accomplished by using a portion of the row address in addition to the column address when determining whether to activate a redundant column selection line. *See* MICRON-1001, 441 Patent at Figure 2 (showing XA0 and XA1, part of the row address X, being passed to the column redundancy decoder 216); MICRON-1003, Baker Decl. ¶ 38. If the portion of the row address **is** associated with a selection of rows connected to a defective bit line and the column address is associated with a defective bit line, then the redundant column selection line is activated. MICRON-1003, Baker Decl. ¶ 39. However, if the portion of the row address **is not** associated with a selection of rows connected to a defective bit line and the column address is associated with a defective bit line, then the regular column selection line is activated. *Id*. The effective result is that only the portion

of the column select line with the defective bit line is replaced with a portion of the redundant column selection line as opposed to replacement of the entire line. *Id.* ¶ 40. This allows the other portions of the redundant column selection line to be used to correct other defects in other lines, thus increasing efficiency. *Id.*

5. PROSECUTION HISTORY

The examiner allowed all 15 claims in the first office action without any rejections. The examiner noted in the Reasons for Allowance that "[t]he PRIOR ART fails to disclose or suggest such a column redundant circuit responsive to the row address as described above . . . ." MICRON-1002, 11-23-1998 Notice of Allowability at .090.

6. CLAIM CONSTRUCTION

6.1. Applicable Law

A claim subject to *inter partes* review is given the "broadest reasonable construction in light of the specification of the patent in which it appears."[1] 37 C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable

[1] The district court, in contrast, affords a claim term its "ordinary and customary meaning . . . to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Petitioner expressly reserves the right to argue different or additional claim construction positions under this standard in district court.

construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

6.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill and consistent with the specification of the 441 Patent. Petitioner respectfully submits that the following term shall be construed for this IPR:

6.2.1. "transfer gate" (claims 3 and 13)

The term "transfer gate" is a limitation of claims 3 and 13 of the 441 Patent. The 441 Patent does not provide an explicit definition of the term "transfer gate." Petitioner respectfully submits that the plain and ordinary meaning of this term is "logic that transfers the logic value of a signal."

The specification and claims describe the operation of the transfer gates disclosed in the patent as transferring a signal. For example, claim 13 requires that the "first transfer gate being activated **to transfer said first matching signal** to said redundant column selection line . . . ."[2] MICRON-1001, 441 Patent at claim 13. Further, the specification describes the functionality of transfer gate 310 as outputting "the matching signal 306 as the Y_{RED} when X_{AO} is at the high level" and

[2] Throughout this Petition, emphasis is added unless otherwise noted.

the functionality of the transfer gate 312 as outputting "the matching signal 308 as the Y_{RED} when XA1 is at the high level." MICRON-1001, 441 Patent at 5:55-61.

The pictorial representations of the transfer gates in the figures appear to be a pair of transistors which pass a signal (310 or 312) from the drain to the source of the transistors as controlled by part of a row address (XA0, XA1). MICRON-1003, Baker Decl. ¶ 47. However, there is nothing in the specification that limits them to that particular embodiment. *Id.* ¶ 48.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 441 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design of memory devices. An individual with an advanced degree in a relevant field would require less experience in the design of memory devices. MICRON-1003, Baker Decl. ¶ 49.

8. DESCRIPTION OF THE PRIOR ART

8.1. U.S. PATENT NO. 5,270,975 ("MCADAMS")

U.S. Patent No. 5,270,975 ("McAdams") (MICRON-1005) was filed on August 13, 1992 and claims priority to two abandoned U.S. Applications, the earliest of which was filed on March 29, 1990. McAdams issued on December 14, 1993, to Hugh McAdams, and is entitled "Memory Device Having A Non-Uniform Redundancy Decoder Arrangement." The original assignee was Texas Instruments

Incorporated. McAdams is prior art to the 441 Patent under at least (pre-AIA) 35 U.S.C. § 102(b) because the patent issued more than one year before the application that led to the 441 Patent was filed on March 31, 1998.

Like the 441 Patent, McAdams is directed to a semiconductor memory device with redundant column select lines and redundant bit lines. MICRON-1005, McAdams at 5:57-60, 6:43-48. McAdams refers to bit lines as "bitline segments." MICRON-1003, Baker Decl. ¶ 60. McAdams refers to column selection lines as column select lines. *Id.* ¶ 61. The semiconductor memory device has an array of memory cells arranged into addressable rows and columns along row lines and column lines. MICRON-1005, McAdams at 22:28-32; MICRON-1003, Baker Decl. ¶ 53. The array is broken up into 16 sub-blocks of a specified number of rows as shown in Figure 2.

MICRON-1005, McAdams at Figure 2.

Each one of the different sub-blocks has separate bit line segments. MICRON-1005, McAdams at Figure 3; MICRON-1003, Baker Decl. ¶ 54.

However, the column select lines Y_S and Y_{RS} run through each of the sub-blocks. *Id.* This is evidenced by the single column decoder at the bottom of Figure 2. MICRON-1003, Baker Decl. ¶ 56. Like the 441 Patent, this is a divided bit line architecture because there are multiple bit lines along a single column that are selected by a single column selection line. *Id.* As shown in Figure 3, McAdams discloses the use of redundant column selection lines ($Y_{RS1\text{-}RSN}$**)** and the associated redundant bit lines.[3] MICRON-1005, McAdams at Figure 3. Like the 441 Patent, McAdams discloses the use of row and column address information to determine whether to activate redundant column selection lines. MICRON-1005, McAdams at Abstract ("These column repair decoder circuits are programmable with column and row address information corresponding to a section of an array column containing a defective memory cell to replace the defective cell with a memory cell in one of the repair columns."). Also like the 441 Patent, the redundant column select lines "[are] capable of replacing multiple defective column portions with multiple redundant column portions which are enabled by the same redundant column select line." *Id.* at 3:12-16. Like the 441 Patent, this is possible because both the column address and part of the row address are used when determining

[3] Figure 3 depicts the word line running vertically and the column selection line running horizontally. That is, it is rotated 90 degrees relative to Figure 2.

whether to activate the redundant column selection lines. MICRON-1003, Baker Decl. ¶ 58; MICRON-1005, McAdams at Figure 4 (column address: CA_0 to CA_{n-x}; row address: RA_{m-y} to RA_m).

8.2. JAPANESE PATENT APPLICATION NO. H06-052696 ("MINAMI")

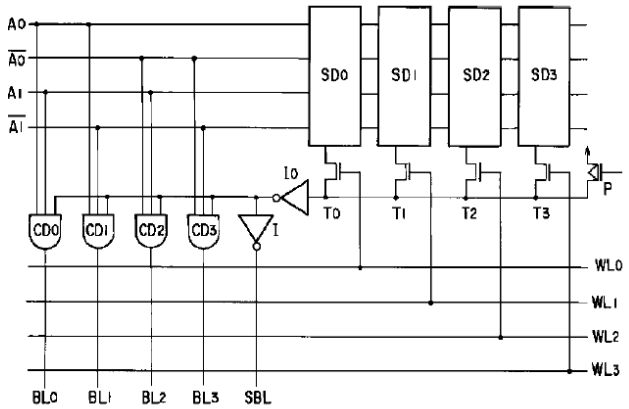
Japanese Patent Application No. H06-052696 ("Minami") (MICRON-1006) was filed on July 31, 1992 by Toshiba Corporation and lists Naoaki Minami and Shigeyoshi Watanabe as inventors. Minami was published on February 25, 1994 and is entitled "Semiconductor Memory Device." Minami is prior art under at least (pre-AIA) 35 U.S.C. § 102(b) because it was published more than one year before the application that led to the 441 Patent was filed on March 31, 1998.

Like the 441 Patent and McAdams, Minami discloses a semiconductor device with redundant cells and a redundant bit line, which Minami describes as a "spare bit line." MICRON-1006, Minami at Abstract, [0021]; MICRON-1003, Baker Decl. ¶ 64. Further, Minami describes a technique such that one spare bit line can be used to replace (or rescue) the defects along multiple bit lines, such that the number of redundant bit lines is decreased as compared to conventional approaches to redundancy circuits. MICRON-1006, Minami at [0017].

As shown below, in Figure 1, Minami discloses a redundancy circuit that uses address inputs (A_0/A_1) and the output from spare decoders (SD) to control column decoders (CD) and determine whether a redundant or "spare" bit line

(SBL) should be activated. MICRON-1003, Baker Decl. ¶ 65; MICRON-1006, Minami at [0022]. Within this circuit, Minami discloses that the spare decoders record the address of defective cells on each word line and use NMOS transistors (T_0-T_3) to transfer the signal from spare decoders, which indicate a defective bit, to an inverter I_0 to column decoders. *Id.* at [0023]; MICRON-1003, Baker Decl. ¶ 66. In particular, like the activation of a redundant column selection line in the 441 Patent, Minami describes that when a word and bit line corresponding to a defective cell is selected, the spare decoders transfer a signal to inverter I_0 and the output of inverter I_0 both (1) activates the spare bit line and (2) inactivates the regular bit lines by deactivating their corresponding column decoders. MICRON-1006, Minami at [0023], [0024]; MICRON-1003, Baker Decl. ¶ 67. Similarly, when a non-defective cell on a word and bit line is selected, the spare bit line is deactivated and the regular bit line selected by its respective column decoder is activated. *Id.*; MICRON-1006, Minami at [0024], [0026].

FIGURE 1



MICRON-1006, Minami at Figure 1.

Minami thus states that whereas conventional methods may have used three spare bit lines for four word lines, one spare bit line is sufficient in the redundancy system described in Minami. *Id.* at [0028]. Indeed, like the 441 Patent and McAdams, the redundancy system described in Minami has the effect reducing the chip surface area necessary for the redundancy circuitry. *Id.* at [0047].

9. GROUND #1: CLAIMS 1-3 AND 5 OF THE 441 PATENT ARE UNPATENTABLE AS ANTICIPATED BY MCADAMS

Claims 1-3 and 5 of the 441 Patent are unpatentable as anticipated under 35 U.S.C. § 102 by McAdams. McAdams discloses all of the limitations in claims 1-3 and 5 of the 441 Patent, and therefore anticipates these claims.

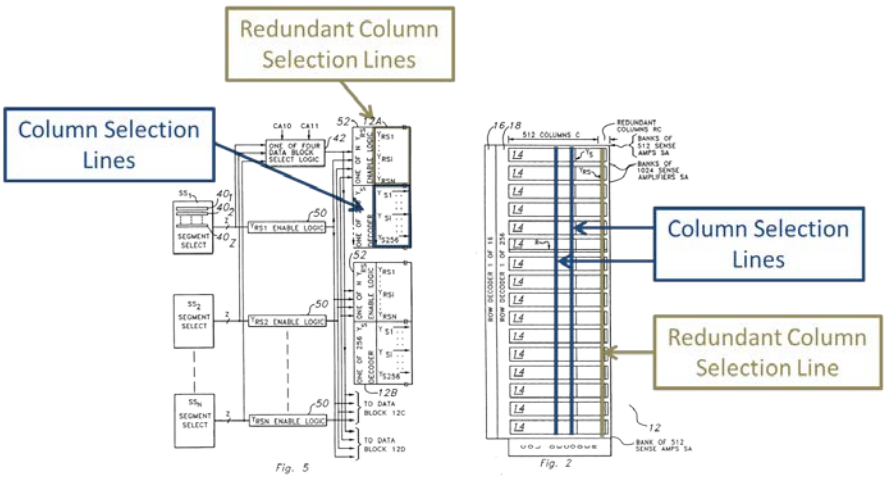
9.1. Claim 1 is anticipated by McAdams

9.1.1. [1.P] "A semiconductor memory device comprising, . . ."

McAdams discloses a semiconductor memory device. MICRON-1005, McAdams at 1:9-10 ("The present invention relates to semiconductor memory devices . . . ").

9.1.2. [1.1] "a plurality of column selection lines, at least one redundant column selection line,"

McAdams discloses a semiconductor memory device comprising a plurality of column selection lines, and at least one redundant column selection line. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.1]. As shown in annotated Figures 5 and 2 below, multiple column selection lines (Y_S) and multiple redundant column selection lines (Y_{RS}) are disclosed in McAdams.



MICRON-1005, McAdams at Figures 5 and 2 (combined, annotated).

In the annotated Figure 2, the column selection lines and redundant column selection line are drawn to connect through the various sub-blocks 14 to the column decoder. MICRON-1003, Baker Decl. ¶ 56 (describing that these lines connect through the blocks to the decoder).

McAdams generally refers to "selection lines" as "select lines," but these are understood as referencing the same component. MICRON-1003, Baker Decl. ¶ 61, Appx. A at claim [1.1]; MICRON-1005, McAdams at 5:39-47 ("Within each sub-block 14, there are 256 row or word lines R and 256 **column select lines Y_S**."); *see also* MICRON-1005, McAdams at 6:31-42 ("five **redundant select lines**").

Thus, by disclosing a memory device with column select lines (Y_S) and redundant column select lines (Y_{RS}), McAdams discloses a semiconductor memory device comprising a plurality of column selection lines, and at least one redundant column selection line.

9.1.3. [1.2] "a column decoder for activating one of said plurality of column selection lines in response to a column address,"

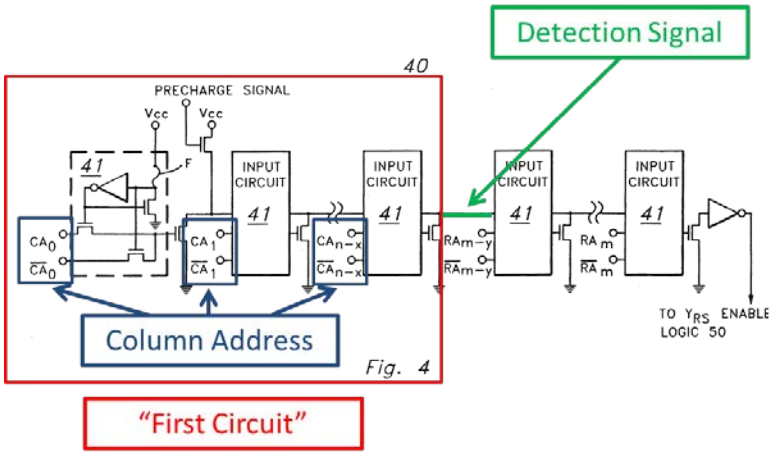
McAdams discloses a column decoder for activating one of said plurality of column selection lines in response to a column address. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.2]; MICRON-1005, McAdams at 6:21-24 ("The **decoder circuitry 20** receives eight bits of column address data, A0 through A7, **to provide a logic-high signal along one of the 256 select lines Y_S** in a data block 12."), Figures 1 and 2. These column decoders are identified as "COL DECODE" in Figure 1 and are also disclosed at the bottom of Figure 2 and in Figure 5. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.2].

Thus, by disclosing decoder circuitry 20 that activates the column selection lines (Y_S) in response to column address data (A0 – A7), McAdams discloses a column decoder for activating one of said plurality of column selection lines in response to a column address.

9.1.4. [1.3] "a first circuit generating a detection signal when the column address of a defective column selection line is supplied,"

McAdams discloses a first circuit generating a detection signal when the column address of a defective column selection line is supplied. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.3]. The column repair decoder circuity disclosed in McAdams includes a plurality of fusible comparator decoders 40 "[t]o effect substitution of redundant column cells for defective cells." MICRON-1005,

McAdams at 7:57-59, Figure 4. Each of the fusible comparator decoders 40 contains a number of input circuits 41 that receive part of a column address signal. The first portion of the input circuits 41 are a "first circuit" that generate a detection signal when the column address of a defective column selection line is supplied as shown below in the annotated Figure 4. *Id.* at 7:65-67 ("the decoder 40 includes n-x input circuits for receiving column address signals and m-y input circuits for receiving row address signals"); MICRON-1003, Baker Decl., Appx. A at claim [1.3].



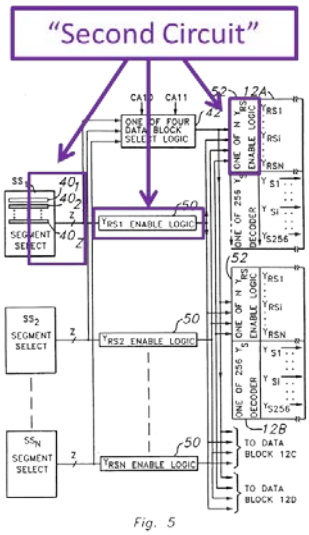
MICRON-1005, McAdams at Figure 4 (annotated).

Thus, by disclosing a first plurality of input circuits 41 that generate a signal when the address of a defective column selection line is supplied, McAdams discloses a first circuit generating a detection signal when the column address of a defective column selection line is supplied.

9.1.5. [1.4] "and a second circuit activating said redundant column selection line in response to said detection signal and at least a part of said row address."

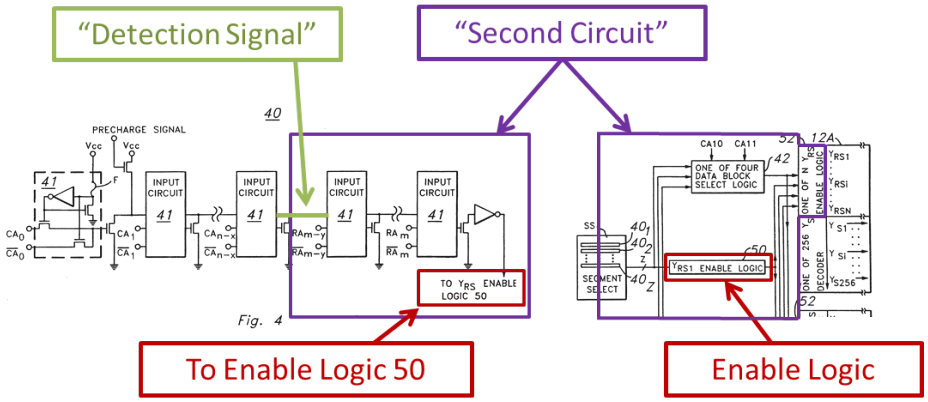
McAdams discloses a second circuit activating said redundant column selection line in response to said detection signal and at least a part of said row address. *See* MICRON-1003, Baker Decl., Appx. A at claim [1.4].

As shown in Figure 5, the output of the fusible comparator decoders 40 is provided to the Y_{RS} enable logic 50 that is then provided to the redundant column decoder (52) that activates the redundant column selection lines. MICRON-1005, McAdams at 8:48-61 ("**The outputs of all the decoders 40 in each segment select group SS_i are input to one of N select enable logic circuits 50.** When one decoder in a group SS_i outputs a logic high signal the select enable logic circuit 50 for that group outputs a logic high signal**, corresponding to the associated redundant select line** $Y_{RSi.}$ With appropriate addressing provided to the decoders 40 and 42, each select enable logic circuit 50 **provides a logic-high signal to one redundant select line Y_{RS} in each data block.**").



MICRON-1005, McAdams at Figure 5 (annotated).

Further, as shown in annotated Figures 4 and 5 below, the second set of input circuits 41 outputs a signal (the line labeled "To Y_{RS} Enable Logic 50") based on the detection signal and part of the row address. MICRON-1005, McAdams at 7:57-67 ("…the column repair decode circuitry includes a plurality of fusible comparator decoders 40 . . . the decoder 40 includes n-x input circuits for receiving column address signals and **m-y input circuits for receiving row address signals**.").



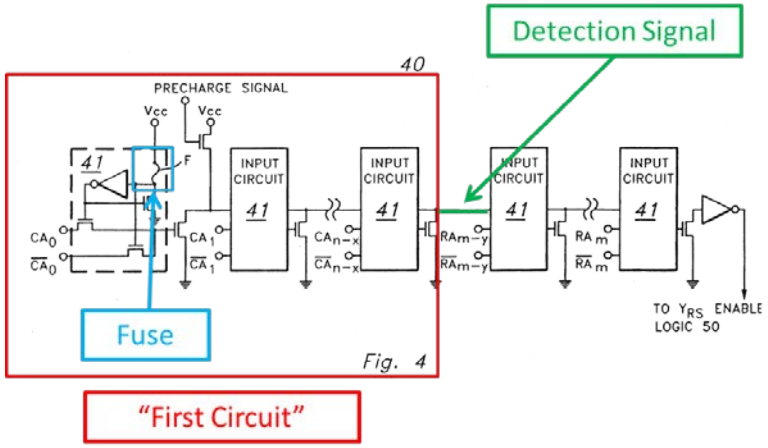
MICRON-1005, McAdams at Figures 4 and 5 (partial) (combined, annotated).

Thus, by disclosing a second plurality of input circuits 41 that accept the output of the first plurality of input circuits (the detection signal) and row address signals RA, and in response (and in combination with Y_{RS} Enable Logic 50 and combinatorial logic 52) activates the associated redundant select line Y_{RS1-N}, McAdams discloses a second circuit activating said redundant column selection line in response to said detection signal and at least a part of said row address.

9.2. Claim 2 is anticipated by McAdams

9.2.1. [2.0] "The semiconductor memory device as claimed in claim 1, wherein said first circuit includes a fuse block storing said column address of said defective column selection line to generate said detection signal."

McAdams discloses the semiconductor memory device as claimed in claim 1, wherein said first circuit includes a fuse block storing said column address of said defective column selection line to generate said detection signal. *See* MICRON-1003, Baker Decl., Appx. A at claim [2.0].



MICRON-1005, McAdams at Figure 4 (annotated).

Each of the input circuits 41 in the fusible comparator decoder discussed above that generates the detection signal includes a fuse. MICRON-1005, McAdams at 8:2-7 ("Each address input circuit 41 includes a **fuse** F for programming the decoder with the row or column address information . . . .").

Thus, by disclosing a plurality of fuses, each in the first plurality of input circuits 41 (including the "first circuit," discussed above for claim [1.3]) for programming the decoder 40, McAdams teaches wherein said first circuit includes

a fuse block storing said column address of said defective column selection line to generate said detection signal.

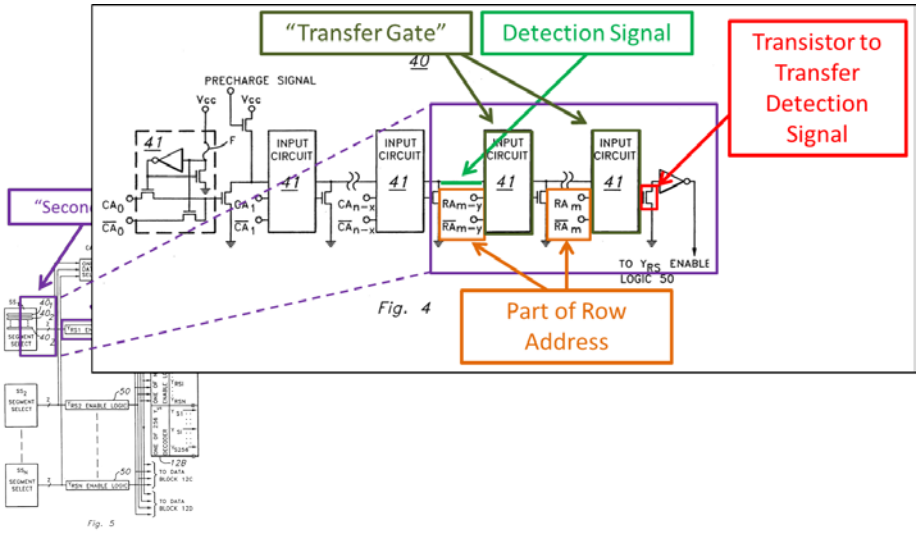
9.3. Claim 3 is anticipated by McAdams

9.3.1. [3.0] "The semiconductor memory device as claimed in claim 2, wherein said second circuit including a transfer gate controlled by said part of said row address to transfer said detection signal to activate said redundant column selection line."

McAdams discloses said second circuit including a transfer gate controlled by said part of said row address to transfer said detection signal to activate said redundant column selection line. *See* MICRON-1005, McAdams at 7:57-8:7, 8:44-61, Figure 4 (depicting structure of input circuits 41 wherein fuses and inputs control transferring input signal to subsequent enable circuit); MICRON-1003, Baker Decl., Appx. A at claim [3.0]. The following analysis applies the plain and ordinary meaning of transfer gate: "logic that transfers the logic value of a signal."

The "second circuit" described above for claim [1.4] comprises a plurality of input circuits 41. The input circuits contain logic that is controlled by part of the row address RA and the status of the fuses (blown or not blown) to transfer the detection signal to Y_{RS} Enable Logic 50 that activates the redundant column selection line. *See id.* Note that the second circuit further includes a transistor (following the last input circuit 41) that, according to the output of the final input

circuit, will also serve to transfer the detection signal to activate the redundant column selection line. *Id.*



MICRON-1005, McAdams at Figures 5 and 4 (combined, annotated).

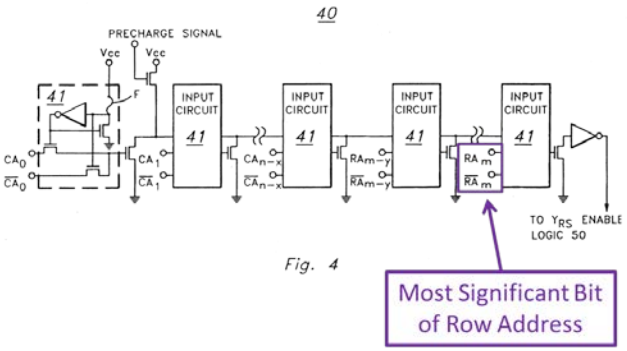
Thus, by disclosing a "second circuit" with input circuits 41 that are logic controlled by part of the row address, that transfers the detection signal to the Y_{RS} Enable Logic 50 and then combinatorial logic 52 to activate the associated redundant column selection line $Y_{RS,}$ McAdams discloses a circuit including a transfer gate controlled by said part of said row address to transfer said detection signal to activate said redundant column selection line.

9.4. Claim 5 is anticipated by McAdams

9.4.1. [5.0] "The semiconductor memory device as claimed in claim 1, wherein said part of said row address includes a most significant bit of said row address."

McAdams discloses the semiconductor memory device as claimed in claim 1, wherein said part of said row address includes a most significant bit of said row address. MICRON-1003, Baker Decl., Appx. A at claim [5.0].

McAdams discloses that the input circuits 41 receive inputs RA_m- RA_{m-y} which are the most significant digits of the row address. MICRON-1003, Baker Decl., Appx. A at claim [5.0]; MICRON-1005, McAdams at 7:62-8:7 ("Given n column address signals provided to the address buffers 24 and **m row address signals** provided to the address buffers 22, the decoder 40 includes n-x input circuits for receiving column address signals and **m-y input circuits for receiving row address signals.** The value of x corresponds to the number of columns C in a data block 12 and the **value of y will depend on the desired level of segmentation.**").



MICRON-1005, McAdams at Figure 4 (annotated).

Thus, by disclosing that the input circuits 41 in the "second circuit," discussed above in claim [1.4], use the highest order bits from the row address

signal, $RA_m - RA_{m-y}$, McAdams discloses the "second circuit" wherein part of said row address includes a most significant bit of said row address.

10. GROUND #2: CLAIMS 3 AND 6-15 OF THE 441 PATENT ARE UNPATENTABLE AS OBVIOUS OVER MCADAMS IN VIEW OF MINAMI

Claims 3 and 6-15 of the 441 Patent are unpatentable under 35 U.S.C. § 103 as obvious over McAdams in view of Minami. In particular, McAdams discloses all of the elements of claims 3 and 6-15 except whether the column line is accessed when the word line is activated as required by claim 6 and whether regular column decoders are deactivated when a redundant column line is selected as required by claims 8 and 10. Minami supplements the teachings of McAdams and teaches these limitations. Additionally, claims 3 and 13 of the 441 Patent require "transfer gates" in making a determination to use a redundant component. As discussed above with respect to claim 3, and below with respect to claim 13, McAdams discloses "transfer gates" if the term is construed to have its plain and ordinary meaning of "logic that transfers the logic value of a signal." *See* Section 9.3 claim 3 *supra*, Section 10.9 claim 13 *infra*; *see also* Section 6 Claim Construction *supra*. However, if "transfer gate" is construed more narrowly to specifically require a "transistor which transfers a signal from its source to its drain (or drain to its

source)" or something similar,[4] then McAdams discloses all of the elements of claims 3 and 13 except the use of transfer gates in making a determination to use a redundant component. Minami also discloses this element.

One of ordinary skill in the art would have been motivated to combine McAdams and Minami. MICRON-1003, Baker Decl. ¶¶ 71-79. First, both McAdams and Minami address the same problem, *i.e.*, increasing efficiency of redundancy schemes for semiconductor memory. *See, e.g.*, MICRON-1005, McAdams at 3:3-7; MICRON-1006, Minami at [0017]. Similarly, both McAdams and Minami explain that the purpose of the respective inventions is to reduce the necessary chip area for redundancy schemes. MICRON-1005, McAdams at 3:3-7; MICRON-1006, Minami at Abstract. And both McAdams and Minami adopt similar solutions to the problem. Both McAdams and Minami describe the use of redundant column lines in a memory which can be used to replace multiple defective column portions from a plurality of different rows, thus decreasing the number of required redundant column lines. MICRON-1005, McAdams at 3:12-16; MICRON-1006, Minami at [0028], [0029]; MICRON-1003, Baker Decl. ¶ 75.

[4] The fundamental difference with the more narrow construction being that it transfers the actual signal in addition to the logic value of the signal. MICRON-1003, Baker Decl. p. 36 n.3.

Second, a person of ordinary skill in the art would have understood that redundancy circuits were well known and components from one system were often interoperable with another. For example, McAdams expressly states that column address data can be applied in "any of several well known decoder circuit arrangements." MICRON-1005, McAdams at 6:27-30. Accordingly, a person of ordinary skill in the art would have found it obvious to combine the teachings of McAdams with the teachings of Minami because Minami discloses a well-known column decoder circuit arrangement for a redundancy circuit. *See* MICRON-1006, Minami at [0022], [0023]; MICRON-1003, Baker Decl. ¶ 76.

Third, one of ordinary skill in the art also would have found the combination of McAdams and Minami to be merely a simple substitution of prior art elements according to known methods that would yield predictable results. For example, a person of ordinary skill in the art would have understood that the Y_{RS} enable logic 50 described in McAdams could be substituted for or modified to include the NMOS transistors T_0-T_3 described in Minami because both types of components serve the same function of transferring a signal. MICRON-1003, Baker Decl ¶ 77. Specifically, McAdams teaches a Y_{RS} enable logic 50 that transfers a signal to a redundant column decoder that activates the redundant column selection lines. MICRON-1005, McAdams at 8:48-61. Similarly, the transfer gates disclosed in Minami are used to transfer signals indicating that the received address of a

memory cell is directed to a defective memory cell and that a spare bit line should be activated instead. MICRON-1006, Minami at [0023]. Accordingly, a person of ordinary skill in the art would have understood that modifying the redundancy circuit in McAdams with the transfer gates disclosed in Minami would have been obvious to try and would have yielded predictable results. MICRON-1003, Baker Decl. ¶ 77.

Additionally, one of ordinary skill in the art would have been motivated to combine the teachings of the redundancy system explicitly taught by McAdams with Minami's teachings based on market incentives and common sense. MICRON-1003, Baker Decl. ¶ 78. Indeed, one of ordinary skill in the art would have understood that (1) the use of transistors to pass a signal for activating a redundant column selection line, and (2) inhibiting of normal column selection lines when a redundant column selection line is activated, as both taught by Minami, would yield the predictable and desirable result of improving the redundancy system in McAdams. Specifically, a person of ordinary skill in the art would have understood that such a redundancy system would have and lower power consumption. *Id*. However, this would have been a mere design choice between greater logic complexity versus lower power consumption. *Id.*

A person of ordinary skill in the art therefore would have found claims 3 and 6-15 of the 441 Patent obvious over McAdams in view of Minami.

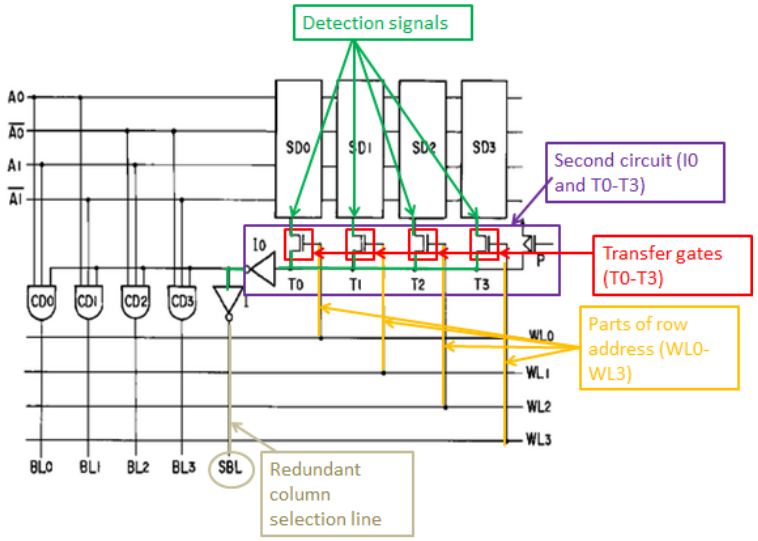
10.1. Claim 3 is obvious over McAdams in view of Minami

10.1.1. [3.0] "The semiconductor memory device as claimed in claim 2, wherein said second circuit including a transfer gate controlled by said part of said row address to transfer said detection signal to activate said redundant column selection line."

To the extent that transfer gate is construed to specifically require a "transistor which transfers a signal from its source to its drain (or drain to its source)," or something similar, claim 3 is rendered obvious by McAdams in view of Minami. *See* above analysis in Section 9.3 claim 3; MICRON-1003, Baker Decl., Appx. A at claim [3.0].

One of ordinary skill in the art would have found it obvious to modify McAdams in view of Minami such that the input circuits 41 would utilize a transistor which transfers a signal from its source to its drain (or drain to its source). *Id.* In particular, Minami discloses a "second circuit" which comprises NMOS transistors T_0-T_3 ("transfer gates") that are controlled by corresponding word line inputs WL_0-WL_3 ("part of said row address") and an inverter I_0. MICRON-1006, Minami at [0023] ("**The output of the spare decoders SD_i (SD_1, SD_2, SD_3 and SD_4) is supplied to the inverter I_0 via the NMOS transistors T_i (T_0, T_1, T_2, T_3) input by the word line WL_i to the gate.**"). This second circuit operates to transfer a signal from spare decoders SD_0-SD_3 to the column decoders and spare bit line via inverter I_0 when the word line of a defective cell is detected.

Id. ("For that reason, **when the input address corresponds to a defective line address, and when the word line of the defective cell is selected, the power source voltage V_{CC} is output respect to the inverter I_0**, and when there is no correspondence then 0V is output."), *id.* at [0024] ("**The inverter I_0** not only inactivates the regular bit lines by outputting 0V to each column decoder when V_{CC} is input, but **also activates the spare bit line SBL via the inverter I_1**."). The signal transferred from the spare decoders is a "detection signal" because the spare decoders record the address of defective regular cells on the word line. *Id.* at [0023]; *see* MICRON-1003, Baker Decl., Appx. A at claim [3.0]. These components are shown with reference to annotated Figure 1 of Minami below.



MICRON-1006, Minami at Figure 1 (annotated).

Thus, because McAdams discloses a "second circuit" with input circuits 41 that are controlled by part of the row address that transfers the detection signal to the Y_{RS} Enable Logic 50 and then combinatorial logic 52 to activate the associated

redundant column selection line Y_{RS} (as discussed in Section 9.3.1 claim [3.0] above), and Minami teaches transferring a signal from its source to its drain in this context, McAdams in view of Minami renders obvious claim 3 of the 441 Patent if "transfer gate" is construed narrowly.

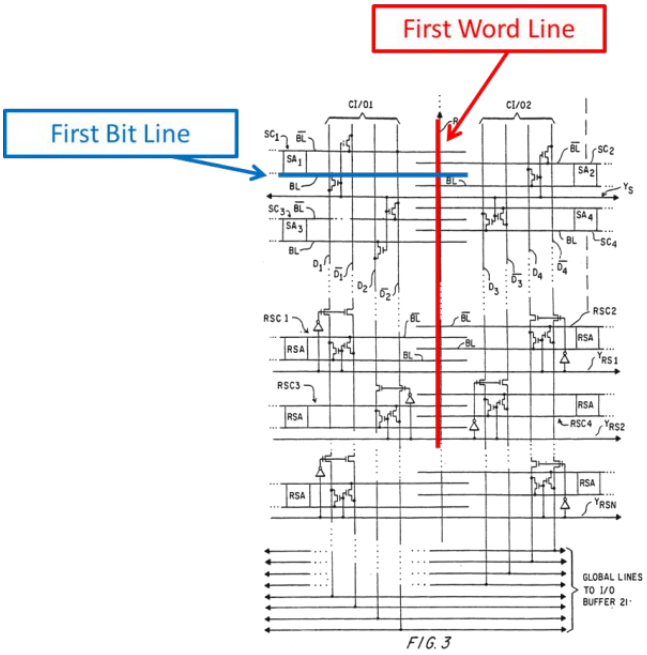
10.2. Claim 6 is obvious over McAdams in view of Minami

10.2.1. [6.0] "A semiconductor memory device comprising:"

McAdams discloses a semiconductor memory device. MICRON-1005, McAdams at 1:9-10 ("The present invention relates to **semiconductor memory devices**"). *See* MICRON-1003, Baker Decl., Appx. A at claim [6.0].

10.2.2. [6.1] "a plurality of word lines including at least first and second word lines; a plurality of bit lines including at least first and second bit lines;"

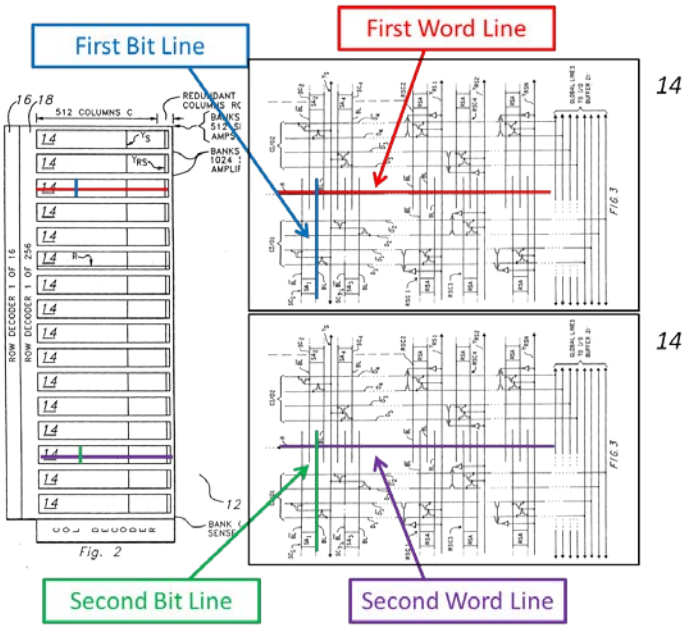
McAdams discloses a semiconductor memory device comprising a plurality of word lines including at least first and second word lines and a plurality of bit lines including at least first and second bit lines. *See* MICRON-1003, Baker Decl., Appx. A at claim [6.1]. The annotated Figure 3 below shows the row or word lines R running vertically, and the Column Select Lines Y_S and Y_{RSn} and bit lines BL run horizontally (contrary to convention). *Id*. This is a partial view of a sub-block with only one word line R, one column select line Y_S and two redundant select lines Y_{RSi}. MICRON-1005, McAdams at 4:31-32; MICRON-1003, Baker Decl., Appx. A at claim [6.1].



MICRON-1005, McAdams at Figure 3 (annotated).

"Within each sub-block 14, there are **256 row or word lines R** and 256 column select lines Y_S. For simplicity of illustration, only one row line R and one column select line Y_S are shown in Figure 3." MICRON-1005, McAdams at 5:39-42. McAdams generally uses the term "row lines," but as shown in the previous quote, "row lines" and "word lines" are interchangeable terms. MICRON-1003, Baker Decl., Appx. A at claim [6.1]. "The partial view of Figure 3 [shown above] illustrates two adjacent pairs of interdigitated subcolumns SC . . . Each of the pairs of subcolumns is associated with one of two adjacent columns in the sub-block . . . Thus, **each subcolumn SC comprises two bitline segments BL and BL[bar] with each containing memory cells** and connected to the same sense amplifier SA." MICRON-1005, McAdams at 5:19-29.

Shown below is Figure 2 interposed with two copies of Figure 3[5] to better depict different word lines from different sub-blocks 14. MICRON-1003, Baker Decl., Appx. A at claim [6.1]. The annotated figure shows multiple bit line segments BL and multiple word lines.



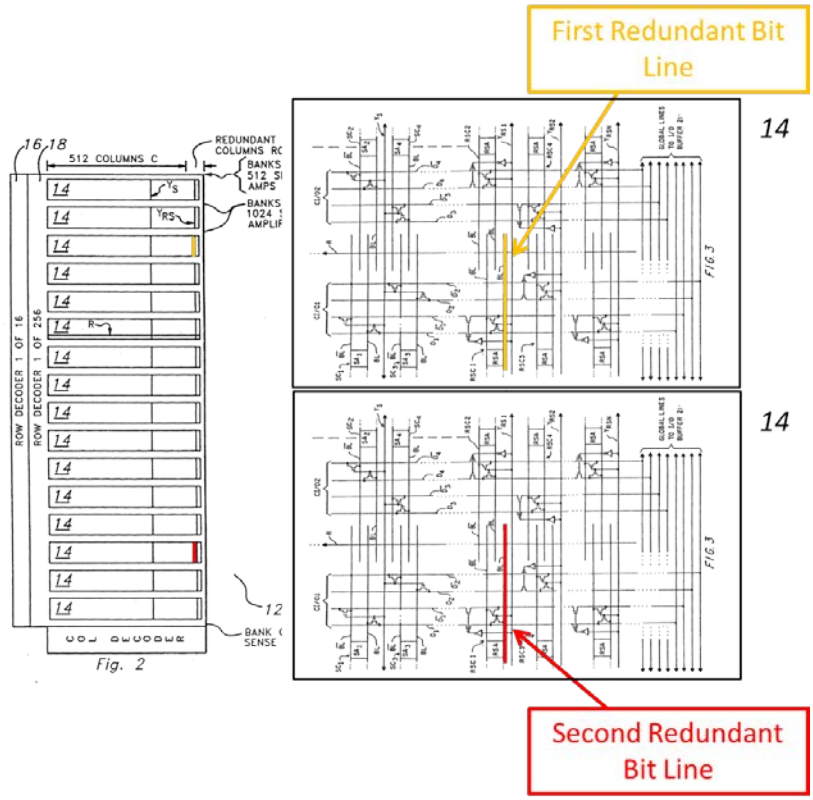
MICRON-1005, McAdams at Figures 2 and 3 (combined, annotated).

Thus, by disclosing multiple bit line segments and multiple row lines in different sub-blocks, McAdams discloses a plurality of word lines including at least first and second word lines; a plurality of bit lines including at least first and second bit lines.

[5] Figure 3 corresponds to a single sub-block 14. MICRON-1005, McAdams at 4:31-32.

10.2.3. [6.2] "a plurality of redundant bit lines including at least first and second redundant bit lines;"

McAdams discloses a plurality of redundant bit lines including at least first and second redundant bit lines (BL). *See* MICRON-1003, Baker Decl., Appx. A at claim [6.2]; MICRON-1005, McAdams at 6:43-48 (disclosing "redundant sub-columns RSC"). "[E]ach subcolumn SC comprises two bitline segments BL and BL[bar] with each containing memory cells and connected to the same sense amplifier SA." MICRON-1005, McAdams at 5:26-29.



MICRON-1005, McAdams at Figures 2 and 3 (combined, annotated).

Because Figure 3 only shows a single row line and a single column selection line (non-redundant), the above annotated image contains copies of Figure 3 to

expand the schematic such that two row lines are visible. The entirety of Figure 3 appears twice. MICRON-1003, Baker Decl., Appx. A at claim [6.2].

Thus**,** by disclosing multiple redundant columns RC that are formed as pairs of redundant subcolumns RSC, the subcolumns being comprised of two bitline segments within each sub-block 14, McAdams discloses a plurality of redundant bit lines including at least first and second redundant bit lines.

10.2.4. [6.3] "a plurality of memory cells each of which is disposed on intersections of said word lines and bit lines; a plurality of redundant memory cells each of which is disposed on intersections of said word lines and redundant bit lines;"

McAdams discloses a plurality of memory cells each of which is disposed on intersections of said word lines and bit lines and a plurality of redundant memory cells each of which is disposed on intersections of said word lines and redundant bit lines. MICRON-1003, Baker Decl., Appx. A at claim [6.3].

The partial view of Figure 3 illustrates subcolumns. "[E]ach subcolumn SC comprises **two bitline segments BL and BL[bar] with each containing memory cells** and connected to the same sense amplifier SA." MICRON-1005, McAdams at 5:26-29. As shown in Figure 3, the bitline segments BL and BL[bar] intersect row line R. As explained above for claim [6.1], the terms "word line" and "row line" are interchangeable in this context. Also, McAdams refers to bit lines generally as "bitline segments." MICRON-1003, Baker Decl., Appx. A at claim [6.3].

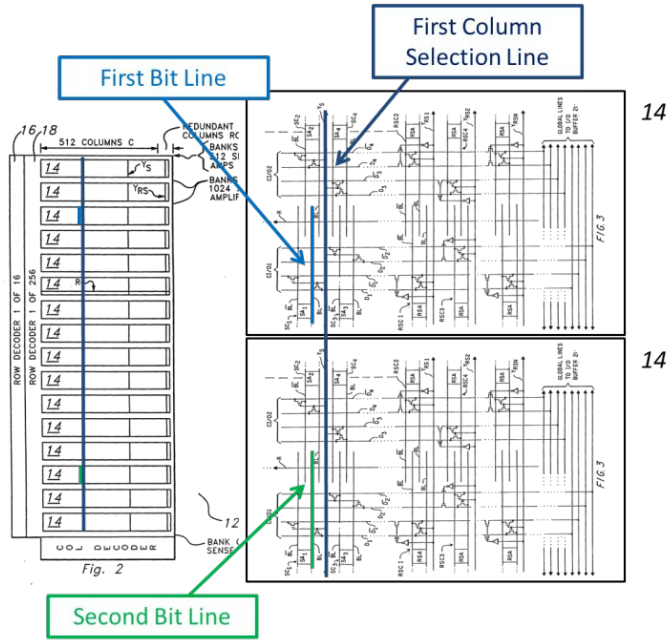
McAdams also discloses "a plurality of redundant memory cells arranged in a plurality of redundant columns, each redundant column including a redundant sub-column for each sub-block of memory cells in the respective memory block." MICRON-1005, McAdams at 20:23-28.

Thus, by disclosing the subcolumns (redundant and non-redundant) being comprised of two bit line segments containing memory cells, those bit line segments intersecting row lines R, McAdams discloses a plurality of memory cells each of which is disposed on intersections of said word lines and bit lines and a plurality of redundant memory cells each of which is disposed on intersections of said word lines and redundant bit lines.

10.2.5. [6.4] "a plurality of column selection lines including at least a first column selection line; said first and second bit lines being selected when said first column selection line is activated, a redundant column selection line; said first and second redundant bit lines being selected when said redundant column selection line is activated,"

This claim limitation essentially covers a divided bit line architecture, as described above, and McAdams discloses this limitation. MICRON-1005, McAdams at 20:23-28. *See* Sections 4 and 8.1; MICRON-1003, Baker Decl., Appx. A at claim [6.4].

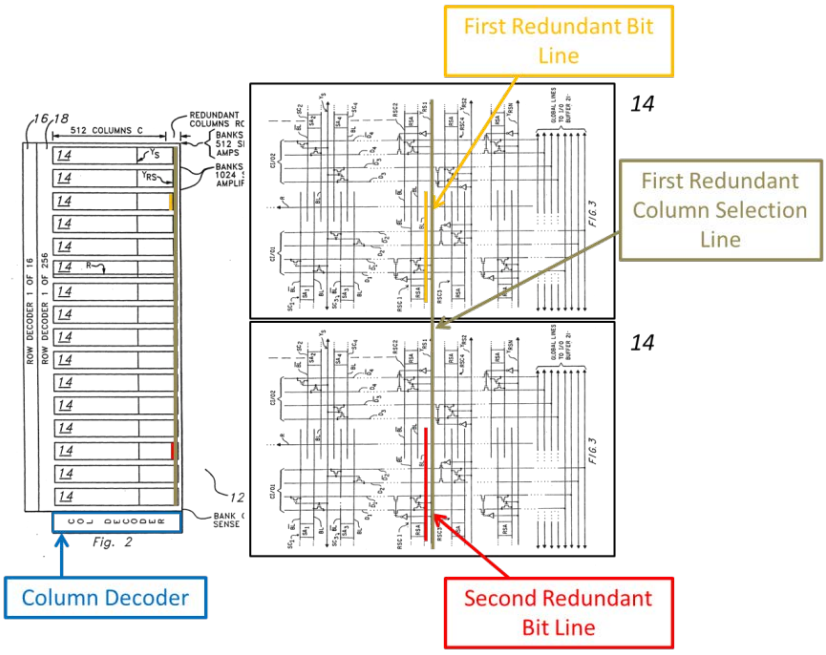
The following annotated image (with two copies of Figure 3 again) shows the first and second bit lines that are selected when the first column selection line is activated.



MICRON-1005, McAdams at Figures 2 and 3 (combined, annotated).

Also as shown in Figure 3, the bit lines are connected to data lines (which read data out of the block) by transistors, with the gates of those transistors connected to the column select lines. Thus, if the associated column select line is activated, the bit line is as well (as the respective bit line is then connected to the data line to output data from the respective sense amplifier via the bit line). MICRON-1005, McAdams at 5:39-6:2; MICRON-1003, Baker Decl., Appx. A at claim [6.4]. As explained above for claim [1.1], the column selection line is drawn in annotated Figure 2 and through the two Figure 3s to connect through the various sub-blocks 14. One of ordinary skill in the art would have understood that these lines would have been uninterrupted in order to function. MICRON-1003, Baker Decl. ¶ 56. Thus, if a single column select line is activated, multiple bit lines associated with that column are also activated. The same is also true for the

redundant column select lines and the redundant bit lines. *Id.* Appx A. at claim [6.4]. The following annotated image shows the first and second redundant bitlines that are selected when a redundant column selection line is activated. The same analysis applies from above.



MICRON-1005, McAdams at Figures 2 and 3 (combined, annotated).

Thus, by disclosing column select lines Ys and redundant column select lines Y_{RS}, each with a pair of subcolumns that are associated with adjacent columns comprising two bitline segments, McAdams discloses this limitation.

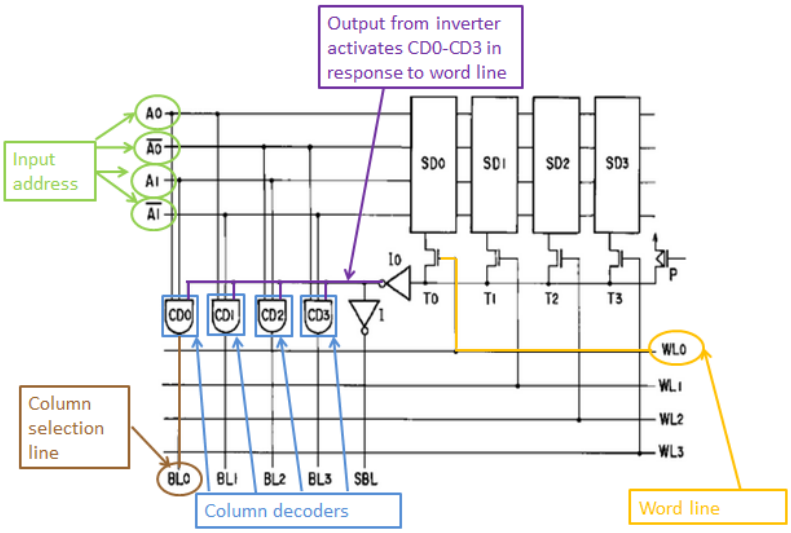
10.2.6. [6.5] "a column decoder activating said first column selection line in response to a first column address when said first word line is activated; and"

As disclosed in McAdams and as in a conventional semiconductor memory device during a data transfer operation, a row address is provided to a row decoder (16, 18) that is used to select a particular row line. MICRON-1005, McAdams at

5:39-47, 6:10-30, Figure 2. A column address is also provided to a column decoder 20 that is **then** used to activate a particular column selection line. MICRON-1005, McAdams at 6:21-24; MICRON-1003, Baker Decl., Appx. A at claim [6.5].

What McAdams does not expressly disclose is that the column decoder activates the first column selection line when the word line is activated. However, it would have been obvious to a person of ordinary skill in the art to activate the column decoder when the word line is activated because that was the conventional operation and would have nevertheless found it obvious in view of Minami. *Id.* Namely, Minami discloses that bit lines (columns) are selected by means of column decoders (CD_i) in correspondence with an input address and the output of an inverter I_0. MICRON-0005, Minami at [0022] ("The row address is input from the address lines A_0,/A_0, A_1,/A_1 and one of the regular **bit lines is selected by means of the column decoders CD_0, CD_1, CD_2 and CD_3 in correspondence with the input address**."), [0024] ("**The inverter I_0** not only inactivates the regular bit lines by **outputting 0V to each column decoder when V_{CC} is input**, but also activates the spare bit line SBL via the inverter I_1. **Moreover, when 0V is input, the spare bit line is deactivated, and the regular bit line selected by the column decoder is activated.**"), [0026]. As was conventional, Minami also discloses that the column selection occurs (via output of inverter I_0) when a word

line in activated ("selected"): "when the word line of the defective cell is selected, a power source voltage V_{CC} is output respect to the inverter I_0" (to the inverter) and when the word line corresponds to a cell which is not defective, then 0V is output to the inverter. *Id.* at [0023].[6] These components are identified in annotated Figure 1 of Minami below.



MICRON-1006, Minami at Figure 1 (annotated).

[6] As Dr. Baker confirms, a person of ordinary skill in the art would have understood that with respect to the word line disclosed in Figure 1 of Minami, the terms "selected" and "activated" have the same meaning, and that "when the word line is selected" also means "when the word line is activated." MICRON-1003, Baker Decl., Appx. A at claim [6.5].

Accordingly, Minami discloses that the regular column decoders CD_0-CD_3 are activated in accordance with an address signal (A_0, A_1) only when a word line is activated which corresponds to a non-defective cell. Thus one of ordinary skill in the art would have understood that McAdams in view of Minami discloses that the column decoder activates a column selection line (Y_S) in response to column address data when the word line is activated, as it would have been obvious that McAdams could have used the conventional row-then-column approach exemplified in Minami. MICRON-1003, Baker Decl., Appx. A at claim [6.5].

10.2.7. [6.6] "a column redundancy decoder activating said redundant column selection line in response to said first column address when said second word line is activated."

This limitation simply covers the concept of using a redundant bit line to replace only part of a column (a segment). Specifically, while the first column address and first word line activates the normal selection line, the same first column address and second word line activates the redundant column selection line. MICRON-1003, Baker Decl., Appx. A at claim [6.6].

As disclosed in McAdams and as in a conventional semiconductor memory device during a data transfer operation, a row address is provided to a decoder that is used to select a particular row line. MICRON-1005, McAdams at 5:39-47, 6:10-30. A column address is also provided to a column decoder 20 that is **then** used to activate a particular column selection line. *Id.* at 6:21-24.

McAdams discloses column repair decoder circuits that are "each connected to a repair column and each programmable **with column and row address information** corresponding to a section of an array column containing a defective memory cell. With this programming, **memory cells in a segment of a repair column can replace memory cells in a segment of an array column containing a defective memory cell**." *Id.* at 3:51-58. The redundant column select lines "[are] capable of replacing multiple defective column portions with multiple redundant column portions which are enabled by the same redundant column select line." *Id.* at 3:12-16. In other words, depending on the row address (first or second word line), activation of the redundant selection line will occur, *e.g.*, if the column and second word line address correspond to a defective cell.

As shown in Figure 5, the output of the fusible comparator decoders 40 (which detects a defective cell by using the row and column address) is provided to the Y_{RS} enable logic 50 that is then provided to the redundant column decoder that activates the redundant column selection lines if the address (*e.g.*, first column address and second word line) matches a defective cell. *Id.* at 7:57-8:7, 8:44-61 ("When one decoder in a group SS_i outputs a logic high signal the select enable logic circuit 50 for that group outputs a logic high signal**, corresponding to the associated redundant select line** Y_{RSi}**.** With appropriate addressing provided to

the decoders 40 and 42, each select enable logic circuit 50 **provides a logic-high signal to one redundant select line Y_{RS} in each data block."**).

What McAdams does not explicitly disclose is whether activating the column redundancy decoder occurs when a word line is activated. However, this would have been obvious to a person of ordinary skill in the art in view of the disclosures in Minami for the same reasons discussed above with reference to the previous limitation. *See* Section 10.2.6 claim [6.5] *supra*; MICRON-1003, Baker Decl., Appx. A at claim [6.6]. Thus, one of ordinary skill in the art would have found that McAdams in view of Minami discloses and renders obvious that the column redundancy decoder activates said redundant column selection line in response to said first column address when said second word line is activated.

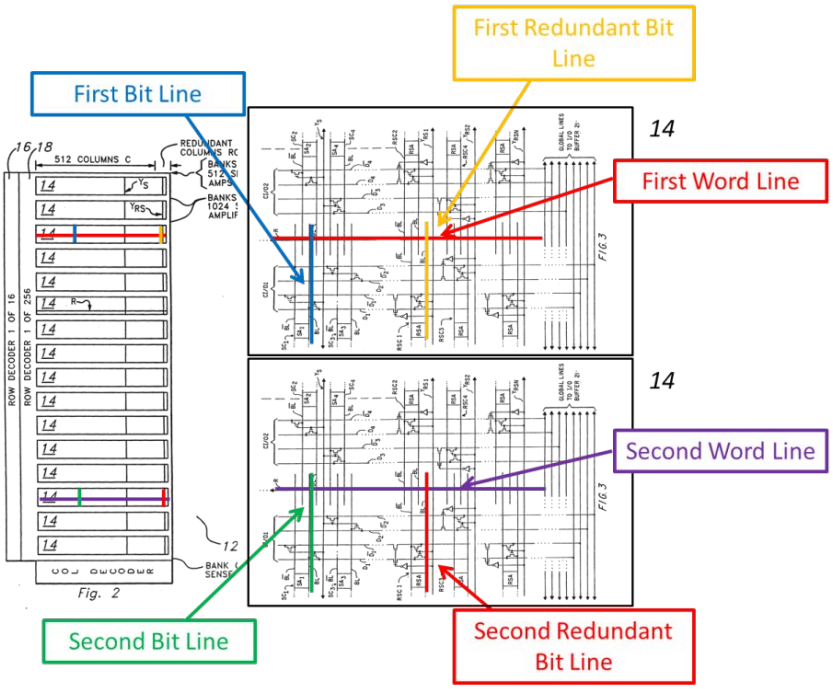
10.3. Claim 7 is obvious over McAdams in view of Minami

10.3.1. [7.0] "The semiconductor memory device as claimed in claim 6, wherein said first word line intersects said first bit line and said first redundant bit line without intersecting said second bit line and said second redundant bit line, said second word line intersecting said second bit line and said second redundant bit line without intersecting said first bit line and said first redundant bit line"

See analysis for claim 6 in Section 10.2 above.

McAdams discloses this limitation. *See* MICRON-1003, Baker Decl., Appx. A at claim [7.0]. Like claim [6.4], this claim limitation essentially covers a divided bit line architecture, as described above. *See* Sections 4 and 8.1. McAdams

teaches this architecture. MICRON-1005, McAdams at 5:39-47, Figs. 2, 3. As shown in the annotated figures below, each of the required structures is present. As before, Figure 3 has been copied, rotated, and interposed with Figure 2 to show where the bit lines and column selection lines are located with respect to the sub-blocks.



MICRON-1005, McAdams at Figures 2 and 3 (combined, annotated).

Thus, because McAdams discloses a plurality of row lines and intersecting bitline segments BL and BL[bar] from different sub-blocks 14, McAdams discloses the semiconductor memory device as claimed in claim 6, wherein said first word line intersects said first bit line and said first redundant bit line without intersecting said second bit line and said second redundant bit line.

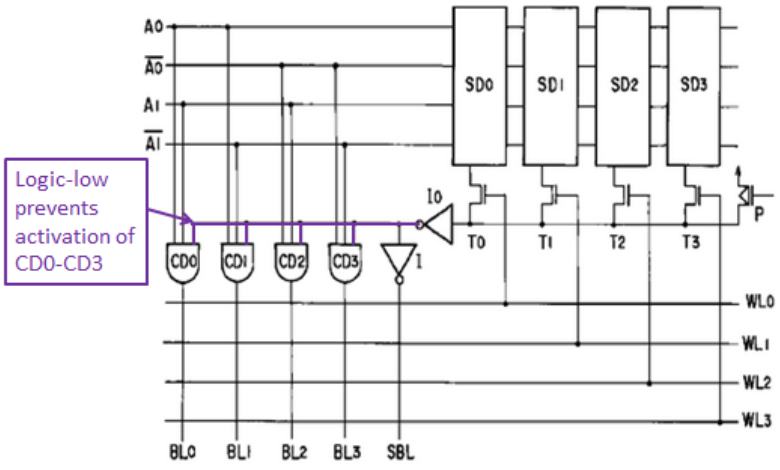
10.4. Claim 8 is obvious over McAdams in view of Minami

10.4.1. [8.0] "The semiconductor memory device as claimed in claim 7, wherein said column decoder is inhibited to activate said first column selection line in response to said first column address when said second word line is activated.

See analysis for claim 7 in Section 10.3 above.

This limitation essentially requires the common sense approach that when a redundant line is activated, regular column decoders connected to the defective line should be inhibited. One of ordinary skill in the art would have found it obvious to modify McAdams in view of Minami such that the column decoder identified above is inhibited to activate a non-redundant column selection line in response to a column and row address that is associated with a defective component.

Minami teaches inhibiting a column decoder (CD_i) and activating a redundant column selection line (SBL) in response to a column address and block information corresponding to defective components.



MICRON-1006, Minami at Figure 1 (annotated).

As shown in annotated Figure 1 above, a logic-low signal output from inverter I_0 renders column decoders CD_i deactivated and activates the spare bit line SBL via the inverter I_1. MICRON-1006, Minami at [0022], [0023], [0024] ("**The inverter I_0 not only inactivates the regular bit lines by outputting 0V to each column decoder when V_{CC} is input**, but also activates the spare bit line SBL via the inverter I_1. Moreover, when 0V is input, the spare bit line is deactivated, and the regular bit line selected by the column decoder is activated.").

One of ordinary skill in the art would have been motivated to make this modification in order to minimize power usage. *See* MICRON-1003, Baker Decl., Appx. A at claim [8.0]. Thus, by disclosing a column decoder that activates a column selection lines (Y_S) in response to column address data and a row line decoder that activates a row line when a row address is input (as discussed above in Section 10.2.6 claim [6.5]) further modified to be inhibited when the column and row address for a defective component is provided, McAdams in view of Minami renders obvious this claim.

10.5. Claim 9 is obvious over McAdams in view of Minami

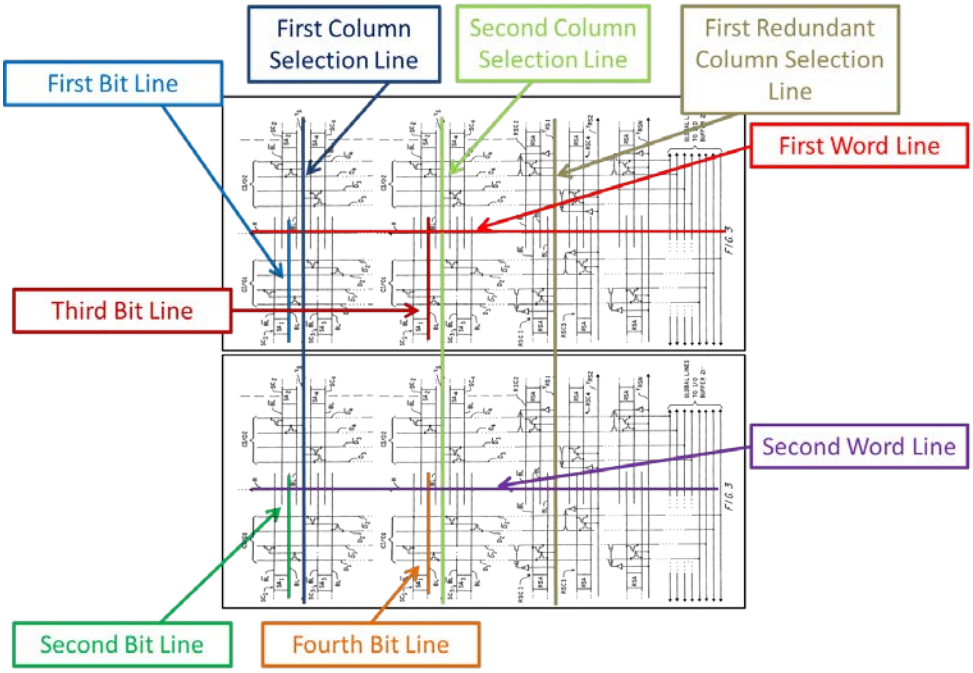
10.5.1. [9.0] "The semiconductor memory device as claimed in claim 7, wherein said plurality of bit lines further includes third and fourth bit lines, said plurality of column selection lines further including a second column selection line, said third and fourth bit lines being selected when said second column selection line is activated, said column decoder activating said second column selection line in response to a second column address when said second

> **word line is activated, said column redundancy decoder activating said redundant column selection line in response to said second column address when said first word line is activated."**

See analysis for claim 7 in Section 10.3 above.

McAdams teaches this limitation. *See* MICRON-1003, Baker Decl., Appx. A at claim [9.0]. Similar to limitation [6.6], this limitation again essentially covers the capability of using a single redundant column selection line to replace defective portions from two different columns. *See* MICRON-1003, Baker Decl., Appx. A at claim [9.0]. Building on claim 6, here, there is an additional column that has a defective bit line that corresponds to the first word line, but a non-defective bit that corresponds to the second word line, and the redundant column fixes the defective bit in both the first and second column depending on the word line address.

The relevant structures are identified in the following annotated figure.



MICRON-1005, McAdams at Figure 3 (annotated).

Because Figure 3 only shows a single word line and a single column selection line (non-redundant), the above annotated image contains copies of Figure 3 to expand the schematic such that two word lines and two column selection lines are visible. The entirety of Figure 3 appears twice in addition to 2 copies of the top portion (showing a column select line). *See* MICRON-1003, Baker Decl., Appx. A at claim [9.0]. As explained above, each of the sub-arrays have 256 rows and columns.

As explained in McAdams, "[w]ith this scheme, incorporating a level of row decoding in the repair column decoders, portions of redundant columns can be allocated to replace portions of array columns containing defective memory cells. Thus, with multiple decoders, a single redundant column can be utilized to replace

multiple defects occurring in different array columns." MICRON-1005, McAdams at 4:14-20; *see also id.* at 7:42-56. To the extent that McAdams does not expressly disclose the specific scenario of claim 9 (one redundant column replaces portions of two different columns depending on the word line address), it would have been obvious to one of ordinary skill in the art, as McAdams discloses an apparatus that is meant to, and can, provide for redundancy given this scenario. *See* MICRON-1003, Baker Decl., Appx. A at claim [9.0]. Thus, because McAdams discloses the relevant structures identified in annotated Figure 3 above and can utilize a single redundant select column to replace defective component from two different columns, one of ordinary skill in the art would have understood this limitation met and obvious in view of McAdams's teachings.

10.6. Claim 10 is obvious over McAdams in view of Minami

10.6.1. [10.0] "The semiconductor memory device as claimed in claim 9, wherein said column decoder is inhibited to activate said first column selection line in response to said first column address when said second word line is activated and inhibited to activate said second column selection line in response to said second column address when said first word line is activated.

See analysis for claim 9 in Section 10.5 above.

Claim 10 essentially requires that the regular column decoder be inhibited when a redundant column selection line is activated in the scenarios of claim 9. As described above (Section 10.5 claim 9), McAdams discloses that a defective

column selection line is activated either (1) when the second word line is activated and a first column address is provided, or (2) the first word line is activated and a second column address is provided. As discussed above (Section 10.4 claim 8), Minami discloses inhibiting the regular column decoders when activating redundant columns. MICRON-1006, Minami at [0022]-[0024]. And for the same reasons above with respect to claim 8, one of ordinary skill in the art would have found it obvious to modify McAdams in view of Minami such that the column decoder identified for claim [6.5] above is likewise inhibited to activate a non-redundant column selection line in response to these scenarios, i.e., when a column and row address that is associated with a defective component is provided. *See* analysis above for Section 10.4.1 claim [8.0]; MICRON-1003, Baker Decl., Appx. A at claim [10.0].

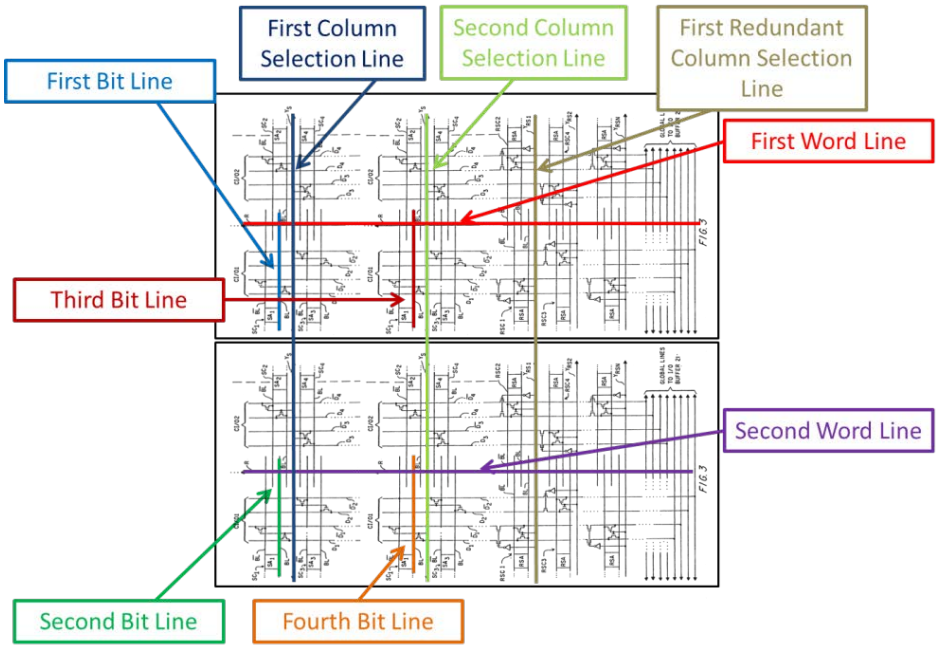
Thus, because McAdams in view of Minami discloses a column decoder that activates a column selection line (Y_S) in response to column address data and activation of a row (as discussed above in Section 10.2.6 claim [6.5]), and discloses that the column decoder is inhibited when the column and row address for a defective component is provided, McAdams in view of Minami renders obvious this claim.

10.7. Claim 11 is obvious over McAdams in view of Minami

10.7.1. [11.0] "The semiconductor memory device as claimed in claim 9, wherein said first word line further intersects

said third bit line without intersecting said fourth bit line, said second word line further intersecting said fourth bit line without intersecting said third bit line."

McAdams discloses this limitation. See analysis above for claims 7 and 9; MICRON-1003, Baker Decl., Appx. A at claim [11.0]. Like claim [6.4], this claim limitation essentially covers a divided bit line architecture, as described above for claim 7. *Id.* However, the concept has been extended for the third and fourth bit lines that were added by claim 9. *Id.* The below annotated figure, used to identify the relevant structures for claim 9, also shows that a divided bit line architecture extends to the third and fourth bit lines.



MICRON-1005, McAdams at Figure 3 (annotated).

The above annotated image contains two copies of Figure 3 to expand the schematic because Figure 3 shows a single word line and a single column selection line. *See* MICRON-1003, Baker Decl., Appx. A at claim [9.0]. As shown in the

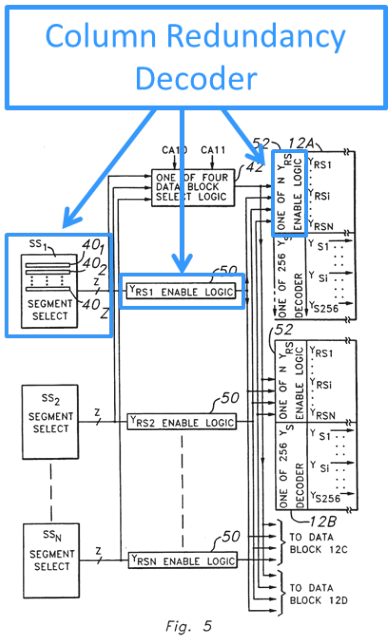
above image, the first word line in the above image intersects the third bit line but not the fourth. The second word line in the below image intersects the fourth bit line but not the third. Thus, McAdams discloses this limitation.

10.8. Claim 12 is obvious over McAdams in view of Minami

10.8.1. [12.0] "The semiconductor memory device as claimed in claim 9, wherein said column redundancy decoder includes first and second fuse blocks, said first fuse block activating a first matching signal in response to said first column address, and said second fuse block activating a second matching signal in response to said second column address."

McAdams discloses the semiconductor memory device as claimed in claim 9, wherein said column redundancy decoder includes first and second fuse blocks, said first fuse block activating a first matching signal in response to said first column address, and said second fuse block activating a second matching signal in response to said second column address. *See* analysis in Section 10.5 claim 9 above; MICRON-1003, Baker Decl., Appx. A at claim [12.0].

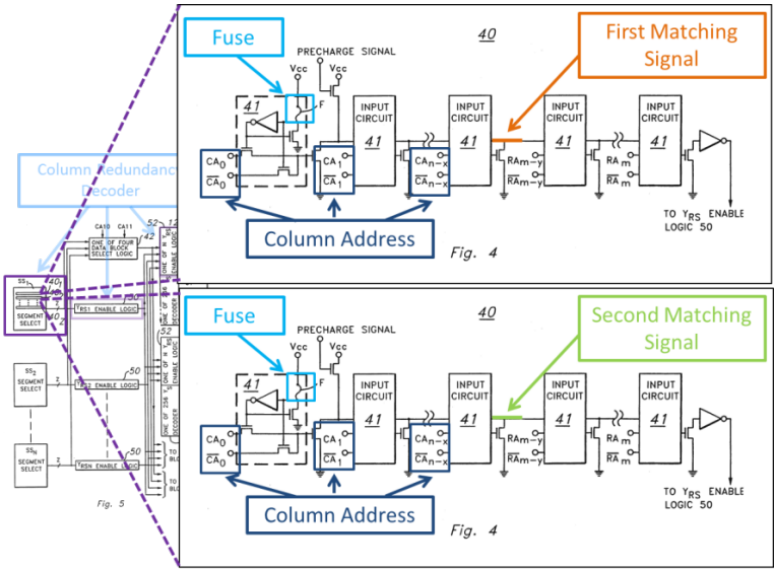
As shown in the below image, the "column redundancy decoder" identified above comprises a series of programming decoders 40.



MICRON-1005, McAdams at Figure 5 (annotated).

As discussed for claim 3, the programming decoders 40 comprise input circuits 41. Each input circuit 41 has a fuse that is used to program the decoder 40 so that a particular segment of redundant memory cells would replace a defective segment of memory cells in a column. MICRON-1005, McAdams at 8:2-7 ("Each address input circuit 41 includes a **fuse** F for programming the decoder with the row or column address information…"). As shown in the figure below, the first plurality of input circuits 41 in each of the programming decoders 40 input the column address. The "first matching signal" as identified in the figure below is generated by this first plurality of input circuits 41 and is only at a high-logic level if the corresponding column address (based on which fuses are blown) is provided. Because there is a plurality of programming decoders 40, there exists another

decoder with a second fuse block that generates a second matching signal in response to a second column address.



MICRON-1005, McAdams at Figure 4 (annotated).

Thus, by disclosing a plurality of fuses in the first plurality of input circuits 41 (discussed above in Section 9.1.4 claim [1.3]) for programming each of the plurality of decoders 40, McAdams teaches said column redundancy decoder includes first and second fuse blocks, said first fuse block activating a first matching signal in response to said first column address, and said second fuse block activating a second matching signal in response to said second column address.

10.9. Claim 13 is obvious over McAdams in view of Minami

10.9.1. [13.0] "The semiconductor memory device as claimed in claim 12, wherein said column redundancy decoder further includes first and second transfer gates said first transfer gate being activated to transfer said first matching signal to said redundant column selection line responsive to

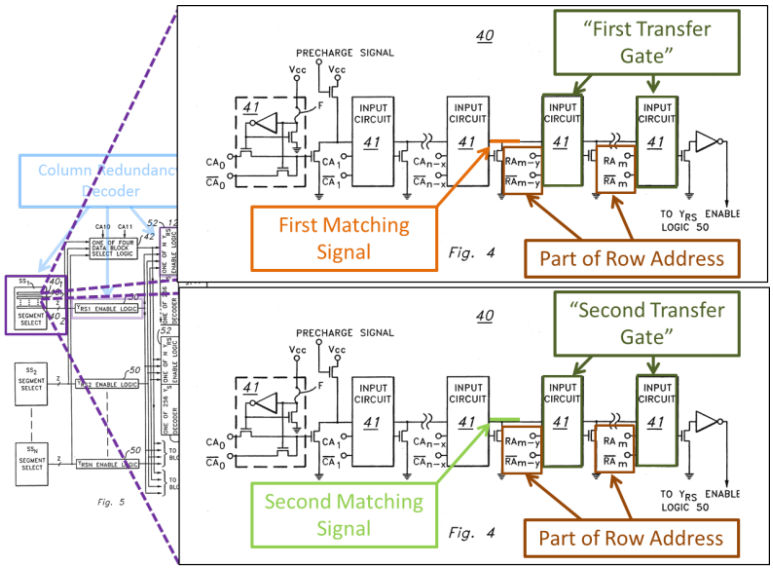
said second word line being activated said second transfer gate being activated to transfer said second matching signal to said redundant column selection line responsive to said first word line being activated."

See analysis for claim 12 in Section 10.8 above.

McAdams discloses the semiconductor memory device as claimed in claim 12, and further discloses this additional limitation. The following analysis assumes that transfer gate either has its plain and ordinary meaning, i.e., "logic that transfers the logic value of a signal," which McAdams discloses, or that transfer gate means something equivalent to a "transistor which transfers a signal from its input to its output," which Minami discloses and which would have been obvious to modify McAdams to include. This claim is essentially the same as claim 3 in that transfer gates are being used to transfer a signal.

10.9.1.1. McAdams discloses this limitation if "transfer gate" means "logic that transfers the logic value of a signal"

The "column redundancy decoder" identified above comprises a plurality of input circuits 41 (in Figure 5). The input circuits contain logic that is controlled by part of the row address RA (that is, responsive to the word line being activated) and the status of the fuses (blown or not blown) to transfer the matching signal to Y_{RS} Logic 50. *See* MICRON-1005, McAdams at Figs. 3, 4; MICRON-1003, Baker Decl., Appx. A at claim [13.0].



MICRON-1005, McAdams at Figures 4 and 5 (combined, annotated).

The above annotated image was created from Figure 4 and Figure 5. Figure 5 includes multiple decoders that are more thoroughly depicted in Figure 4.

Thus, by disclosing a plurality of input circuits that are logic that transfer said first and second matching signals in response to part of a specific row address (which also activates the relevant row) to the Y_{RS} enable logic that then activates the redundant column selection line $Y_{RS,}$ McAdams discloses this claim element.

10.9.1.1. McAdams in view of Minami discloses this limitation if "transfer gate" means "transistor which transfers a signal from its source to its drain (or drain to its source)"

Furthermore, to the extent that transfer gate is construed to mean a transistor which transfers a signal from its source to its drain (or drain to its source), claim 13 is also rendered obvious by McAdams in view of Minami for the same reasons as claim 3.

The "column redundancy decoder" identified above comprises a plurality of input circuits 41. *See* Section 10.2.7 claim [6.6]. One of ordinary skill would have found it obvious to modify McAdams in view of Minami such that the input circuits 41 would utilize transfer gates T_0-T_3 described in Minami to transfer matching signals to the column selection line in response to the relevant partial row address. *Id.* *See* analysis above for claim 3.

Thus, by disclosing a plurality of input circuits which could be modified to include transfer gates that transfer said first and second matching signals in response to part of a specific row address (which also activates the relevant row) to the Y_{RS} enable logic that then activates the redundant column selection line $Y_{RS,}$ McAdams in view of Minami renders obvious this claim element if "transfer gates" is construed narrowly.

10.10. Claim 14 is obvious over McAdams in view of Minami

10.10.1. [14.0] "The semiconductor memory device as claimed in claim 6, wherein said second bit line is defective.

See analysis in Section 10.2 claim 6; *see* MICRON-1003, Baker Decl., Appx. A at claim [14.0].

One of ordinary skill in the art would have understood that portions of redundant columns would only be used where there were defective components, such as a bit lines that cause short circuits, and it would have been obvious to one of ordinary skill in the art that a bit line could be a defective element of a column

in light of McAdams. MICRON-1005, McAdams at 1:15-23 ("short circuits"); *see* MICRON-1003, Baker Decl., Appx. A at claim [14.0]. In cases of defective bit lines, McAdams discloses a single redundant column can be used to replace the defective components in several different columns such as the second bit line. MICRON-1005, McAdams at 8:2-7; *id.* at 7:39-41 ("Generally, one redundant column RC can be used to eliminate defects occurring in multiple columns.").

Thus, as explained above, the columns comprise bit line segments and McAdams discloses such defects may include bit lines that cause short circuits. A person of ordinary skill in the art would have been motivated in view of McAdams that when the bit line segments are defective, as with any other types of defects, to program the column redundancy decoder to replace the corresponding bit line segments with redundant segments along the redundant column select line. *See* Baker Decl., Appx. A at claim [14.0].

10.11. Claim 15 is obvious over McAdams in view of Minami

10.11.1. [15.0] "The semiconductor memory device as claimed in claim 9, wherein said second and third bit lines are defective.

See analysis for claim 9 in Section 10.5 above; *see* MICRON-1003, Baker Decl., Appx. A at claim [15.0].

This limitation is similar to claim 14, but instead of a single bit line being defective, both the second and third bit lines are defective. For the same reasons as

set forth above, a person of ordinary skill in the art would have been motivated in view of McAdams that when the bit line segments are defective, as with any other types of defects, to program the column redundancy decoder to replace the corresponding bit line segments (here, the second and third bit lines) with redundant segments along the redundant column select line. *See* Baker Decl., Appx. A at claim [15.0].

11. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1-3, and 5-15 of the 441 Patent is requested.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	October 27, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 5,894,441 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1007
Persons served	Patent Owner's Address of Record: Sughrue Mion Zinn MacPeak & Seas PLLC 2100 Pennyslvania Avenue NW Washington, DC 20037 Additional Address Known as Likely to Effect Service: Jon A. Birmingham Fitch Even Tabin & Flannery LLP 21700 Oxnard Street Suite 1740 Woodland Hills, CA 91367

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