UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 5,805,504
Title: SYNCHRONOUS SEMICONDUCTOR MEMORY HAVING A BURST TRANSFER MODE WITH A PLURALITY OF SUBARRAYS ACCESSIBLE IN PARALLEL VIA AN INPUT BUFFER

Petition For *Inter Partes* Review of U.S. Patent No. 5,805,504 Under U.S.C §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

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Exhibit List

Micron Exhibit #	*Description*
MICRON-1001	U.S. Patent No. 5,805,504 ("the 504 Patent")
MICRON-1002	File History for U.S. Patent No. 5,805,504
MICRON-1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
MICRON-1004	*Curriculum Vitae* of Dr. R. Jacob Baker
MICRON-1005	U.S. Patent No. 5,581,746 ("Watanabe")
MICRON-1006	Japanese Unexamined Patent Application Publication, H4-326138 with Certified Translation ("Iwama")
MICRON-1007	U.S. Patent No. 5,337,050 ("Sugawara")

1. INTRODUCTION

Micron Technology, Inc. ("Petitioner"), in accordance with 35 U.S.C. § 311-319 and 37 C.F.R. § 42.100, hereby requests *inter partes* review of claims 1-2 of United States Patent No. 5,805,504, titled "Synchronous Semiconductor Memory Having A Burst Transfer Mode With A Plurality Of Subarrays Accessible In Parallel Via An Input Buffer" (MICRON-1001, "the 504 Patent"). According to USPTO records, the 504 Patent is assigned to Limestone Memory Systems LLC.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 504 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 504 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang (Reg. No. 73604) (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Justin L. Constant (Reg. No. 66883) (justin.constant@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 700 Louisiana, Suite 1700 Houston, TX 77002 T: 713-546-5217; F: 713-224-9511

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney for the Petitioner is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. (*See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.)

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

Limestone has asserted the 504 Patent and U.S. Patent Nos. 5,894,441 ("the 441 Patent"), 5,943,260 ("the 260 Patent"), 6,233,181 ("the 181 Patent") and 6,697,296 ("the 296 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *Limestone Memory Sys. LLC v. Micron Tech. Inc.*, 8:15-cv-00278 (C.D. Cal.) ("Co-Pending Litigation"). Limestone has also asserted one or more of the asserted patents in the following actions: *Limestone Memory Sys. LLC v. OCZ Storage Solutions, Inc.*, 8:15-cv-00658 (C.D. Cal.) (the 504, 441, 181 and 296 Patents); *Limestone Memory Sys. LLC v. PNY Techs., Inc.*, 8:15-cv-00656 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Lenovo (US) Inc.*, 8:15-cv-00650 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Kingston Tech. Co. Inc.*, 8:15-cv-00654 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Transcend Info.*,

Inc. (California), 8:15-cv-00657 (C.D. Cal.) (the 260 Patent); *Limestone Memory Sys. LLC v. Acer America Corp.*, 8:15-cv-00653 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Dell Inc.*, 8:15-cv-00648 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); *Limestone Memory Sys. LLC v. Hewlett-Packard Co.*, 8:15-cv-00652 (C.D. Cal.) (the 504, 441, 260, 181, and 296 Patents); and *Limestone Memory Sys. LLC v. Apple Inc.*, 8:15-cv-01274 (C.D. Cal.) (the 504, 441, 181, and 296 Patents).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 5,894,441, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 5,943,260, IPR2015-Unassigned (to be filed concurrently); Petition for *Inter Partes* Review of U.S. Patent No. 6,233,181, IPR2015-Unassigned (to be filed concurrently); and Petition for *Inter Partes* Review of U.S. Patent No. 6,697,296, IPR2015-Unassigned (to be filed concurrently).

The 504 Patent claims priority to foreign patent application JP-7-311238. The 504 Patent does not claim priority to any other U.S. patent applications.

2.5. Fee for Inter Partes Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 506499.

2.6. Proof of Service

Proof of service of this petition on the patent owner at the correspondence address of record for the 504 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

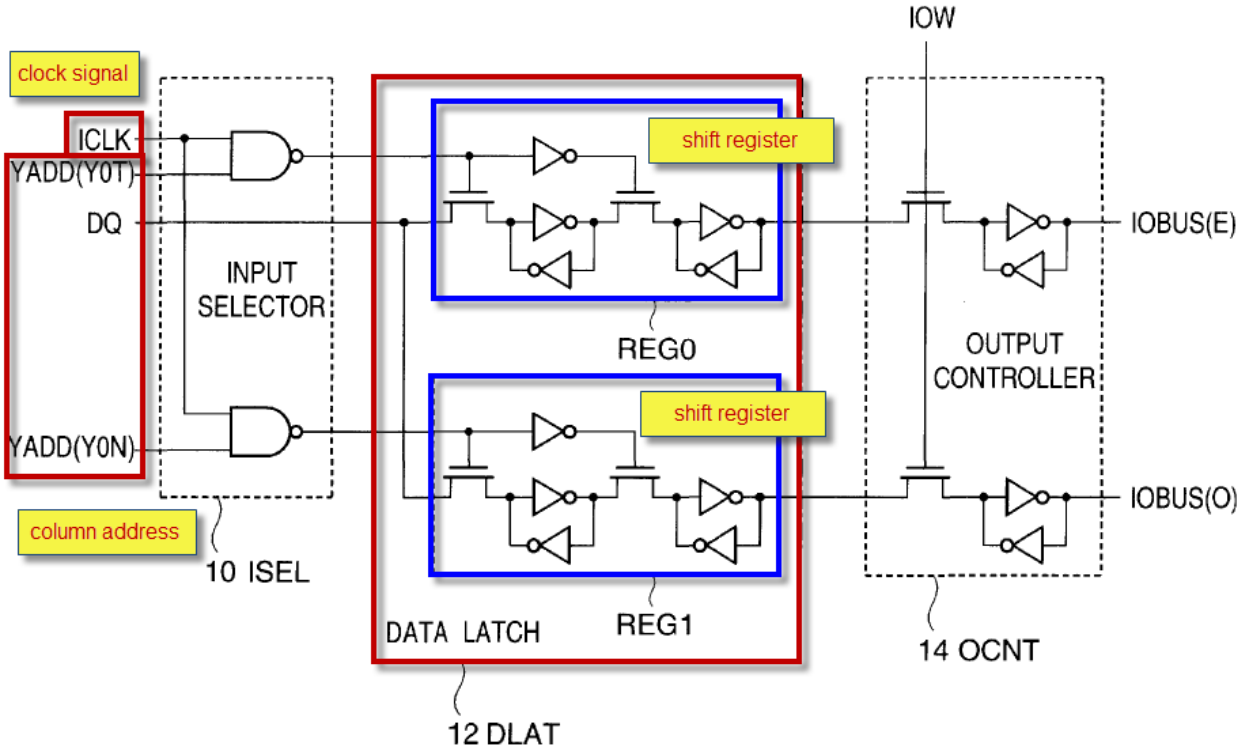
Ground #1: Claims 1 and 2 of the 504 Patent ("the challenged claims") are invalid under (pre-AIA) 35 U.S.C. § 103 on the ground that they are rendered obvious by U.S. Patent No. 5,581,746 ("Watanabe") in view of JP4-326138 ("Iwama"). Watanabe attached as MICRON-1005; Iwama attached as MICRON-1006. Watanabe was filed with the USPTO on December 28, 1993 and issued December 3, 1996. Watanabe is prior art under at least 35 U.S.C. § 102(a). Iwama was filed with the Japanese Patent Office on April 25, 1991 and was published November 16, 1992. Iwama is prior art under at least 35 U.S.C. § 102(a), (b).

This ground is explained below and is supported by the Declaration of Dr. R. Jacob Baker (MICRON-1003, "Baker Decl.").

4. OVERVIEW OF THE 504 PATENT

The 504 Patent was filed on November 29, 1996, and claims priority to a Japanese patent application which was filed on November 29, 1995. The 504 Patent purports to address inefficiencies in the prior art burst write operation (*see* MICRON-1003, Baker Decl. ¶¶ 28-29 discussing the "what" and "why" of burst write operations), which the 504 Patent depicts in Figure 3.

FIGURE 3 PRIOR ART

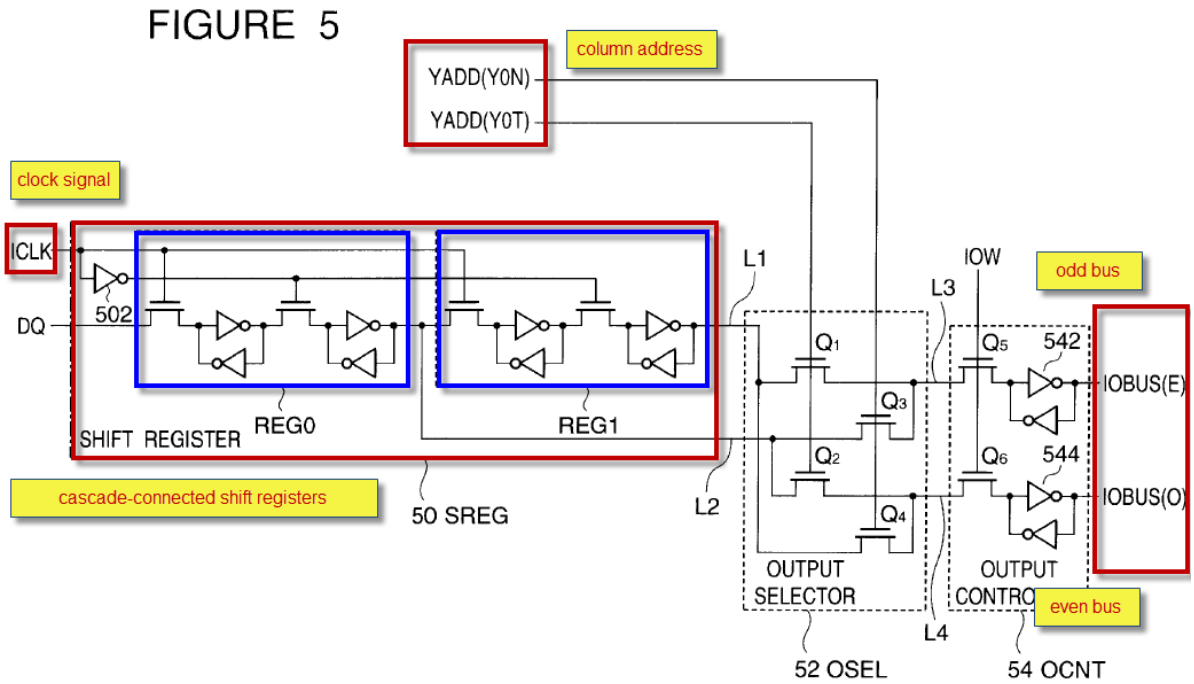


MICRON-1001, 504 Patent at Figure 3 (annotated).

In the admitted prior art burst write operation described in the 504 Patent, as data comes in from the left, input selector 10 distributes the data into registers REG0 and REG1 based on the column address of the data (YADD) and in synchronism with a reference clock ICLK. Once latched into registers REG0 and REG1, the data is then output simultaneously and in parallel to output controller 14. Following that, the data is distributed onto internal even and odd bus lines (IOBUS(E) and IOBUS(O)). This write operation is considered a burst write operation because two bits of information are written to the memory array in parallel over the internal buses in one write memory access.

The 504 Patent purports to address inefficiencies in Figure 3, above. Specifically, the 504 Patent states that the operation in Figure 3 is inefficient because it uses the column address signal (YADD) to steer data to REG0 and REG1. The 504 Patent states that because the input selector cannot distribute the data to registers REG0 and REG1 without first receiving the address, the process is slowed. The solution, which is the subject of claim 1, is to distribute the serial data without need for the column address (through shift registers that only use a clock and the input data). Only then, after the data is stored in the shift registers, does the 504 Patent use the column address to steer the data.

Figure 5 of the 504 Patent depicts the burst write process of the patent.



MICRON-1001, 504 Patent at Figure 5 (annotated).

Specifically, Figure 5 depicts an input buffer circuit (50 SREG) having cascade-connected registers, REG0 and REG1. Data is received on the left and shifted into the registers in synchronism with internal clock ICLK. The data is then steered into output selector 52 based on the column address and subsequently distributed to even and odd bus lines through output controller 54.

The difference between the 504 Patent and the admitted prior art described therein is the timing of the use of the column address. In the prior art, the column address is used to steer the data into the registers. In the 504 Patent, the column address is used to steer the data as the data leaves the registers. Otherwise, the prior art and the 504 Patent are substantially similar. In both cases, the prior art and the 504 Patent disclose (a) a plurality of memory cell sub-arrays which are accessible in parallel and simultaneously (*See e.g.*, MICRON-1001, 504 Patent at 4:40-45); (b) a plurality of internal data buses for inputting and outputting data to and from said plurality of memory cell sub-arrays, in parallel (*See e.g.*, *id.* at 4:30-45); and (c) an input buffer circuit receiving external data signals continuously and sequentially in time in synchronism with a reference clock signal, for converting said receiving serial data into a parallel data under control of an external command signal and an external address signal, so as to distribute said parallel data to said plurality of internal data buses (*id.*). MICRON-1003, Baker Decl. ¶ 32.

5. PATENT PROSECUTION HISTORY

The 504 Patent was issued in a first office action allowance on May 12, 1998. MICRON-1002, 5-12-1998 Notice of Allowance at .139. The Examiner stated that,

> The instant invention is directed at improving the speed of a synchronous memory device. More particularly, the instant invention divides the memory array into a plurality of memory subarrays, and operates the subarrays in parallel through the use of a plurality of internal buses and a input buffer. While the prior art includes examples of memory devices with a plurality of memory arrays, the prior art does not teach or suggest operating these arrays in parallel with the claimed input buffer. Thus, these features of the sole independent claim are not taught or suggested by the prior art of record:
>
> 1. A semiconductor memory having a burst mode transfer function comprising: ... an input buffer ..., the input buffer including a shift register composed of a plurality of cascade-connected registers and for latching and shifting said external data signals only in response to said reference clock signal, said cascade connected registers ..., and a register output selecting means receiving ..., for distributing said received parallel data signals, in parallel, to said plurality of internal data buses ...

MICRON-1002, 5-12-1998 Notice of Allowance at .143 (emphasis added).

The apparent distinguishing feature is the claimed input buffer, which includes a shift register composed of a plurality of cascade-connected registers that latch and shift data only in response to a clock signal.

6. CLAIM CONSTRUCTION[1]

6.1. Applicable Law

For a non-expired patent, a claim subject to *inter partes* review is interpreted in a manner that is consistent "broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). Any ambiguity regarding the "broadest reasonable construction" of a claim term is resolved in favor of the broader construction absent amendment by the patent owner. Final Rule, 77 Fed. Reg. 48680, 48699 (Aug. 14, 2012).

For expired patents, the claims are interpreted in accordance with the principles outlined in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See In re Rambus, Inc.*, 753 F.3d 1253, 1256 (Fed. Cir. 2014). The 504 Patent will expire on November 29, 2016, which may occur prior to the Board's institution decision. Accordingly, this petition proposes constructions below consistent with the standard for both non-expired and expired patents. These

[1] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 504 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 504 Patent.

constructions are proposed for the sole purpose of this petition and to comply with 37 C.F.R. §§ 42.100(b) and 42.104(b)(3). Likewise, this petition applies such interpretations, consistent with the *Phillips* standard, for terms not subject to construction.

6.2. Construction of Claim Terms

Petitioner respectfully submits that the following terms shall be construed for this IPR:

6.2.1. "register output selecting means . . . for distributing said received parallel data signals, in parallel, to said plurality of internal data buses in accordance with said external address signal" (claims 1-2)

The claim term, "register output selecting means . . . for distributing said received parallel data signals, in parallel, to said plurality of internal data buses in accordance with said external address signal" is a limitation of claim 1 of the 504 Patent, and thus is also a limitation of dependent claim 2. This claim term in independent claim 1 is governed by 35 U.S.C. §112 ¶ 6. For the reasons discussed below, the corresponding structure is a plurality of transfer gate transistors responsive to the column address to selectively distribute data in parallel to either the even or odd internal buses and equivalents thereof. MICRON-1003, Baker Decl. ¶ 23.

The Federal Circuit recently reaffirmed that the use of the word "means" creates a rebuttable presumption that a claim term is governed by 35 U.S.C. §112 ¶

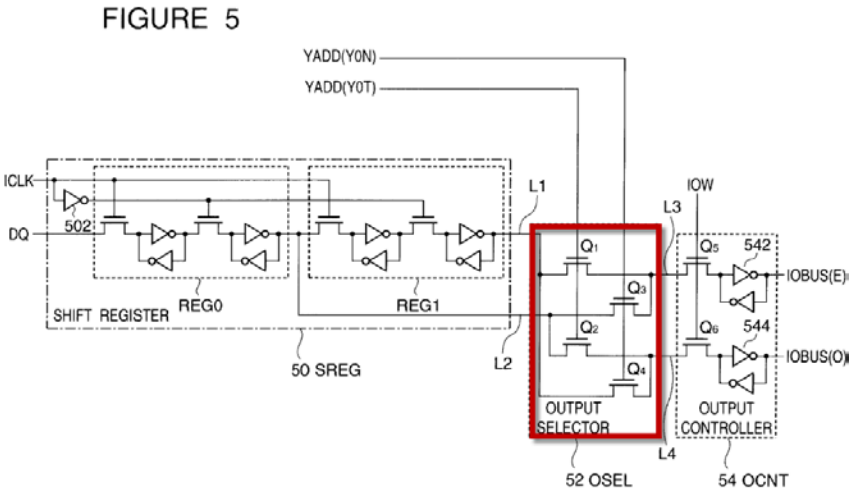
6. *Williamson v. Citrix Online, LLC,* 792 F.3d 1339, 1348 (Fed. Cir. 2015). The essential inquiry is "whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Id.* That is, "that the term, as the name for structure, has a reasonably well understood meaning in the art." *Id.* citing *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996).

In *Williamson,* the Court determined that the phrase "distributed learning control module for . . ." should be governed by 35 U.S.C. §112 ¶ 6 for four reasons. First, the Court noted that the phrase was drafted in a format consistent with traditional means-plus-function claim limitations. Second, the Court determined that the term "module" is a well-known nonce word that does not convey sufficiently definite structure. Third, the Court determined that the prefix language, "distributed learning control" did not impart any structural significance to the term "module." Finally, the Court was unable to find anything in the remaining claim language that described how the "distributed learning control module" interacted with other components such that a person of ordinary skill in the art would be informed of the structural character of the limitation. *Williamson,* 792 F.3d at 1352-60.

Applying the Court's reasoning to "register output selecting means" limitation leads to the same result – the term is governed by 35 U.S.C. §112 ¶ 6.

First, the claim term is drafted in traditional means-plus-function language – *i.e.*, "means . . . for" and the phrase "means for" creates a rebuttable presumption that the term is governed by 35 U.S.C. §112 ¶ 6. Second, the term "means" is a nonce word and does not convey sufficient structure. *Williamson*, 792 F.3d at 1360; MICRON-1003, Baker Decl. ¶ 21. Third, the prefix "register output selecting" does not add any structural significance to the term "means." *Id*. At best, the prefix implies that the means (*i.e.*, the structure) selectively outputs from the registers but it does not convey what structure is responsible for that output. Finally, the remainder of the claim language does nothing to inform a person of ordinary skill in the art as to the structure of the limitation. *Id*. Accordingly, in view of the foregoing, the term should be governed under 35 U.S.C. §112 ¶ 6.

Provided the limitation is governed by 35 U.S.C. §112 ¶ 6, the corresponding structure for performing the function, "distributing said received parallel data signals, in parallel, to said plurality of internal data buses in accordance with said external address signal" is depicted in the 504 Patent at Figure 5 as part of the output selector 52. MICRON-1003, Baker Decl. ¶ 22.



MICRON-1001, 504 Patent at Figure 5 (annotated).

As disclosed in the 504 Patent, "output selector 52 includes a first transfer gate transistor Q1 connected between the line L1 and the line L3, a second transfer gate transistor Q2 connected between the line L2 and the line L4, a third transfer gate transistor Q3 connected between the line L2 and the line L3, and a fourth transfer gate transistor Q4 connected between the line L1and the Line L4." MICRON-1001, 504 Patent at 9:54-60; MICRON-1003, Baker Decl. ¶ 23. These transfer gate transistors are responsive to column address YADD to distribute the data. MICRON-1001, 504 Patent at 9:60-10:2; MICRON-1003, Baker Decl. ¶ 23.

For example, "when the internal column address signal YADD indicates an even number . . . the data held in the first register REG0 is distributed to the even-numbered column address internal data bus IOBUS(E), and the data held in the second register REG1 is distributed to the odd-numbered column address internal data bus IOBUS(O)." MICRON-1001, 504 Patent at 10:3-11. Conversely, "if the

internal column address signal YADD indicates an odd number, the data held in the first register REG0 is distributed to the odd-numbered column address internal data bus IOBUS(O), and the data held in the second register REG1 is distributed to the even-numbered column address internal data bus IOBUS(E)." *Id.* at 10:11-17. Thus, the means "selectively" distributes the data, *i.e.*, in that data from either register may be distributed to either the even or odd buses.

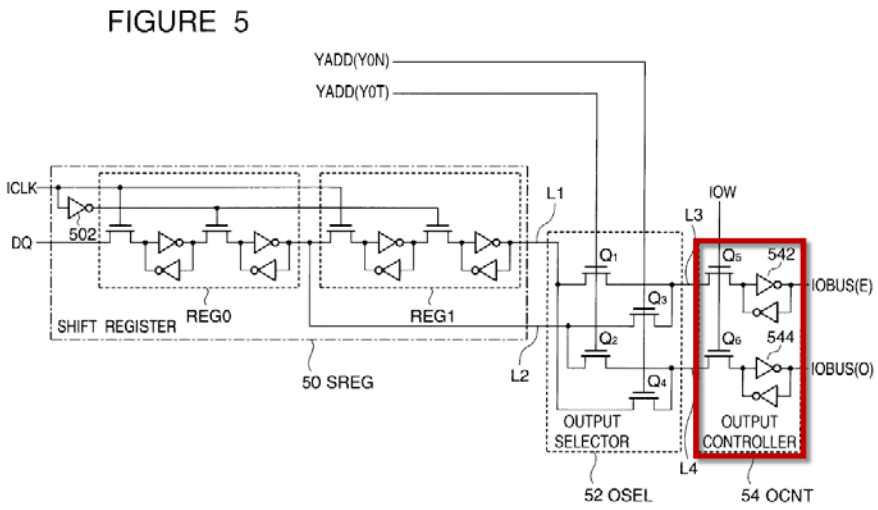
In view of the foregoing, the term is governed by 35 U.S.C. §112 ¶ 6 and the corresponding structure is a plurality of transfer gate transistors responsive to the column address to selectively distribute data in parallel to either the even or odd internal buses and equivalents thereof under both the broadest reasonable construction and under *Phillips*.

6.2.2. "buffer output control means for transferring said outputs of said register output selecting means, simultaneously and in parallel, to said plurality of internal data buses, in synchronism with an edge of said reference clock signal" (claim 2)

The claim term "buffer output control means for . . . " is a limitation of dependent claim 2 of the 504 Patent, and is governed by 35 U.S.C. §112 ¶ 6. For the reasons discussed below, the corresponding structure is a plurality of transfer gate transistors responsive to a buffer output control signal IOW. MICRON-1003, Baker Decl. ¶ 26.

First, the term includes the phrase "means for." Thus, there is a rebuttable presumption that the term is governed by 35 U.S.C. §112 ¶ 6. Second, the term "means" is a nonce word and fails to convey sufficiently definite structure to a person of ordinary skill in the art. MICRON-1003, Baker Decl. ¶ 25. Third, the prefix "buffer output control" does not impart any structural significance to the term "means." At best the prefix indicates that the unnamed structure controls what is output from the buffer. *Id.* Finally, none of the other limitations in the claim informs a person of ordinary skill in the art as to the structure of the limitation. *Id*. Accordingly, in view of the foregoing, the term should be governed by 35 U.S.C. §112 ¶ 6.

The corresponding structure for performing the function, "transferring said outputs of said register output selecting means, simultaneously and in parallel, to said plurality of internal data buses, in synchronism with an edge of said reference clock signal" is depicted in the 504 Patent at Figure 5 as part of the output controller 54. MICRON-1003, Baker Decl. ¶ 26. Note that the function only transfers data and thus the latches of output controller 54 are not part of the corresponding structure. *See id.*



MICRON-1001, 504 Patent at Figure 5 (annotated).

As disclosed in the 504 Patent, the "output controller 54 includes a transfer gate transistor Q5 having one end connected to the line L3, another transfer gate transistor Q6 having one end connected to the line L4, a latch 542 having an input connected to the other end of the transfer gate transistor Q5 and an output connected to the internal data bus IOBUS(E), and another latch 544 having an input connected to the other end of the transfer gate transistor Q6 and an output connected to the internal data bus IOBUS(O). The transfer gate transistors Q5 and Q6 are controlled in common by the data-in buffer output control signal IOW. Thus, under control of the data-in buffer output control signal IOW, the output controller 54 outputs the parallel two bits of data distributed and outputted from the register output selector 52, to the internal data bus IOBUS(E) and IOBUS(O), simultaneously and in parallel, respectively." MICRON-1001, 504 Patent at 10:18-34.

The plurality of transfer gate transistors is responsive to buffer output control signal IOW. MICRON-1001, 504 Patent at 10:26-28 ("The transfer gate transistors Q5 and Q6 are controlled in common by the data-in buffer output control signal IOW."); MICRON-1003, Baker Decl. ¶ 26. In view of the foregoing, the term is governed by 35 U.S.C. §112 ¶6 and the corresponding structure is a plurality of transfer gate transistors responsive to buffer output control signal (*e.g.*, IOW) or equivalents thereof under both the broadest reasonable construction and under *Phillips*.

7. PERSON HAVING ORDINARY SKILL IN THE ART

A person of ordinary skill in the art with respect to the technology described in the 504 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2-3 years of experience in the design of memory devices. An individual with an advanced degree in a relevant field would require less experience in the design of memory devices. MICRON-1003, Baker Decl. ¶ 17.

8. DESCRIPTION OF THE PRIOR ART

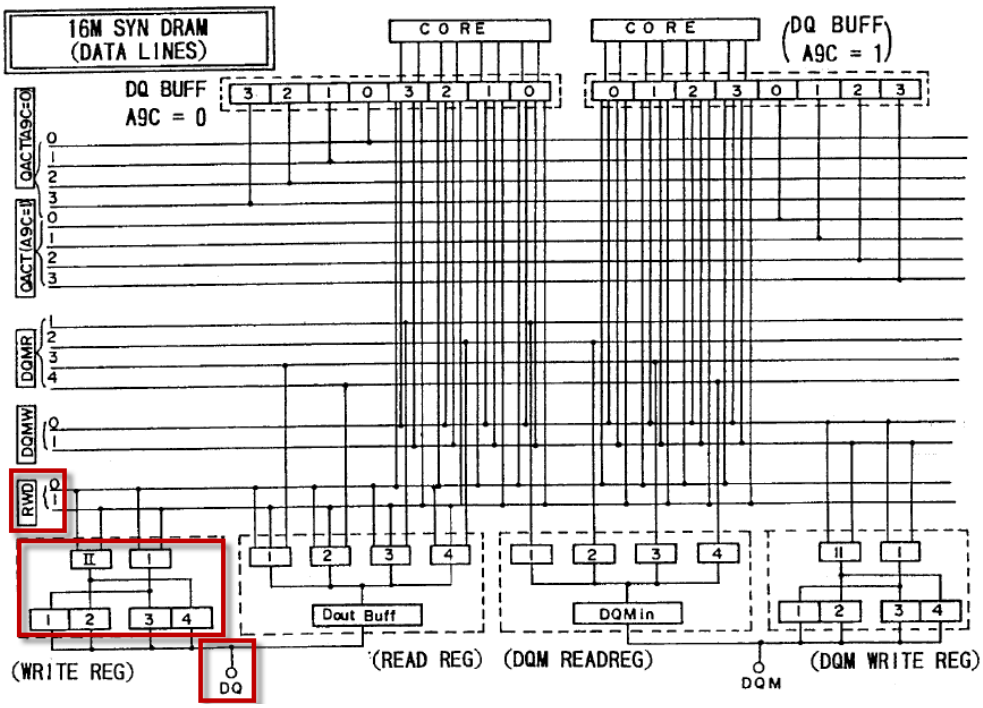
8.1. U.S. PATENT NO. 5,581,746 ("WATANABE")

U.S. Patent No. 5,581,746 ("Watanabe") (MICRON-1005) was filed on December 28, 1993, and claims priority to a Japanese patent application filed December 28, 1992. Watanabe issued on December 3, 1996, to Yuji Watanabe and is entitled "Synchronous LSI Memory Device." The originally assignee was

Kabushiki Kaisha Toshiba. Watanabe is prior art to the 504 Patent under at least 35 U.S.C. § 102(e) because the U.S. Patent Application which issued as Watanabe was filed before the earliest application to which the 504 Patent claims priority.

Watanabe is directed to the same technical field as that being addressed by the 504 Patent. Watanabe, like the 504 Patent, acknowledges that "the CPU has been improved to such an extent as to exceed that of the DRAM." MICRON-1005, Watanabe at 1:18-20. Watanabe notes that prior art solutions for addressing this problem have fallen short because the prior art solutions need overly complicated circuitry. *Id.* at 1:20-29. Watanabe's solution is to provide a circuit for a burst write operation, wherein two CPU cycles are used to input data but that data is then written to the memory array using a single memory access. *Id.* at Table 15, Figure 98; MICRON-1003, Baker Decl. ¶ 36.

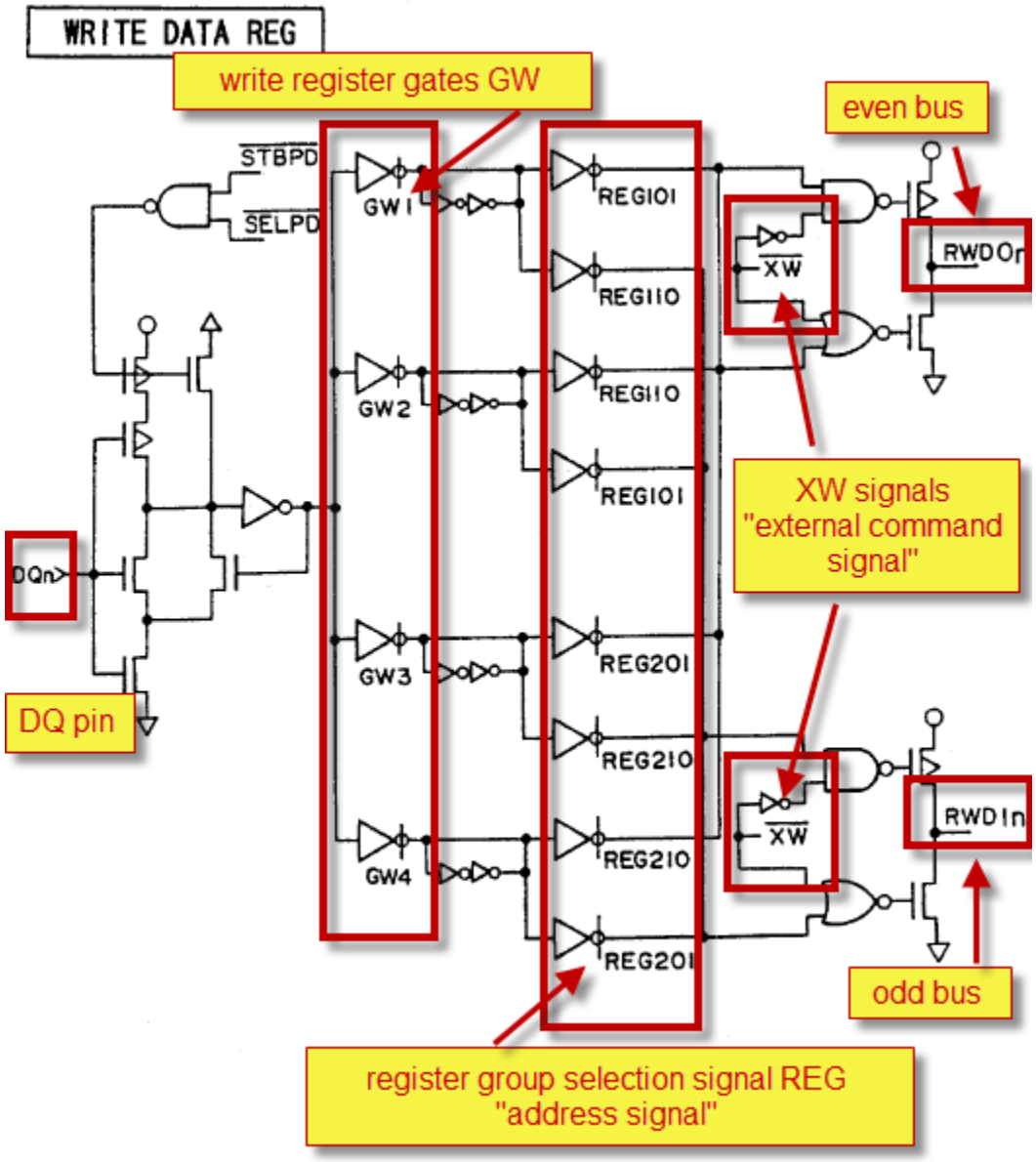
Relevant to this request, Watanabe discloses a write register circuit (WRITE REG). The WRITE REG circuit is depicted in Watanabe at Figure 2, which discloses a DRAM circuit. MICRON-1005, Watanabe at 7:24-27.



MICRON-1005, Watanabe at Figure 2 (annotated).

Data received by the WRITE REG circuit is distributed simultaneously and in parallel to internal buses RWD0 and RWD1 (even and odd buses). *See* MICRON-1003, Baker Decl. ¶ 36; MICRON-1005, Watanabe at Table 15. *See also id.* at Figure 98.

The WRITE REG circuit is seen in more detail in MICRON-1005, Watanabe at Figure 28.



MICRON-1005,Watanabe at Figure 28 (annotated).

The operation of the WRITE REG circuit is important to this Request and renders claims 1 and 2 obvious when considered in view of Iwama (discussed below). Watanabe discloses that data is received serially at pin DQn (note that there is a WRITE REG circuit for each DQ pin) and converted from serial to parallel data. MICRON-1003, Baker Decl. ¶ 37; MICRON-1005, Watanabe at 19:17-24. This is

achieved by using the write register gates GW above to shift the data into the registers (without use of the column address). MICRON-1003, Baker Decl. ¶ 38; MICRON-1005, Watanabe at Figure 28. Once the data is shifted into the registers, the data is distributed according to a register group selection signal REG, which is based on the column address. MICRON-1003, Baker Decl. ¶¶ 39-40; MICRON-1005, Watanabe at Figure 30(C)). From there, the data is finally distributed to even and odd bus lines in response to write enable signal ($\overline{XW}$) (also depicted in Figure 28, above). This signal, the write enable signal ($\overline{XW}$), is in synchronism with the clock signal. MICRON-1003, Baker Decl. ¶ 41.

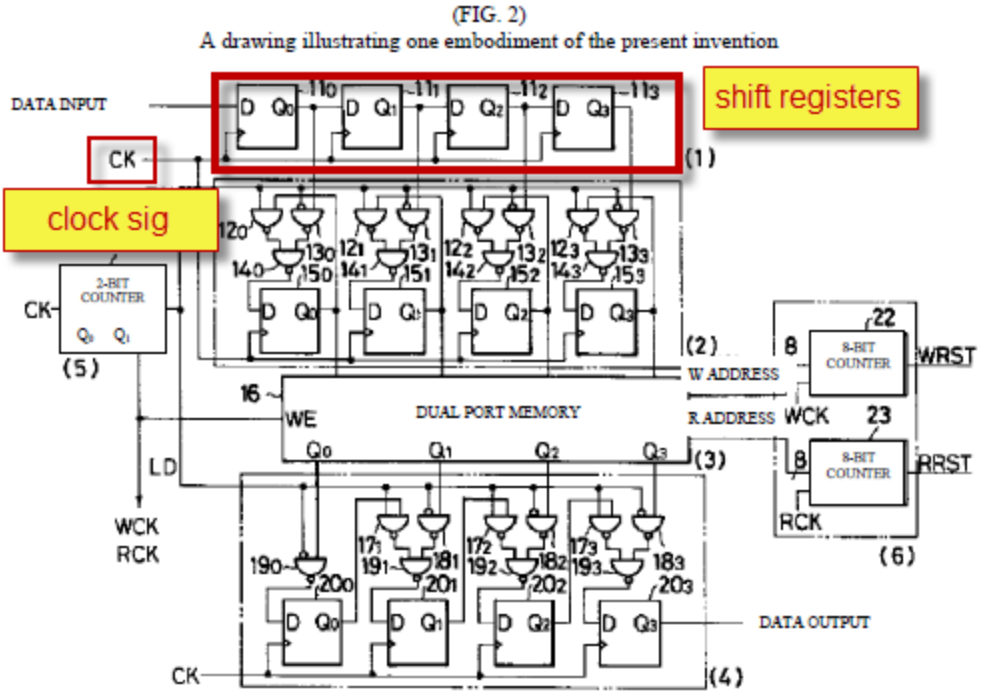
In short, Watanabe describes a system for taking in serial data, converting that data to parallel data using a series of gates, and distributing that data in synchronism to a plurality of internal buses based on an address and clock signal after receiving a write enable signal.

What Watanabe does not describe, which is required by claims 1 and 2 of the 504 Patent, is the use of cascade-connected registers to convert the serial data to plural data. Instead, Watanabe uses a series of write register gates (GW). However, as discussed in detail below, it would have been obvious to replace Watanabe's write register gates with the cascade-connected registers disclosed in Iwama.

8.2. Japanese Patent Application H4-326138 ("IWAMA")

Japanese Patent Application H4-326138 ("Iwama") (MICRON-1006) was filed April 25, 1991 and was published November 16, 1992. Iwama is entitled "HIGH-SPEED MEMORY IC" and issued to Fujistu, LTD. Iwama is prior art under at least 35 U.S.C. § 102(b) because it was published more than one year before the earliest application to which the 504 Patent claims priority was filed.

Iwama discloses a high-speed memory IC having a serial-parallel conversion shift register. MICRON-1006, Iwama at claim 1. Iwama addresses the same technical area addressed by both Watanabe and the 504 Patent – improving the access speed of conventional memory. The circuit architecture developed by Iwama, like that disclosed by the 504 Patent and Watanabe, includes a burst write operation. Iwama accomplishes the burst write operation using a series of cascade-connected registers for converting serial data to parallel data. MICRON-1003, Baker Decl. ¶¶ 43-44. This circuit is depicted in Iwama at Figure 2.



MICRON-1006, Iwama at Figure 2 (annotated).

Figure 2 discloses an input buffer comprising cascade-connected registers (labeled 11_0-11_3), which shift the data across the registers in response to clock signal CK. *See* MICRON-1006, Iwama at (0010); MICRON-1003, Baker Decl. ¶ 44.

9. GROUND #1: CLAIMS 1 AND 2 OF THE 504 PATENT ARE UNPATENTABLE AS OBVIOUS OVER WATANABE IN VIEW OF IWAMA

As explained below, claims 1 and 2 of the 504 Patent are unpatentable as obvious under 35 U.S.C. § 103 over Watanabe in view of Iwama. Watanabe discloses all the features of claims 1 and 2 except for an input buffer comprising a plurality of cascade-connected registers. Iwama discloses such an input buffer.

9.1. It would have been obvious to a person of ordinary skill in the art to combine Watanabe with Iwama

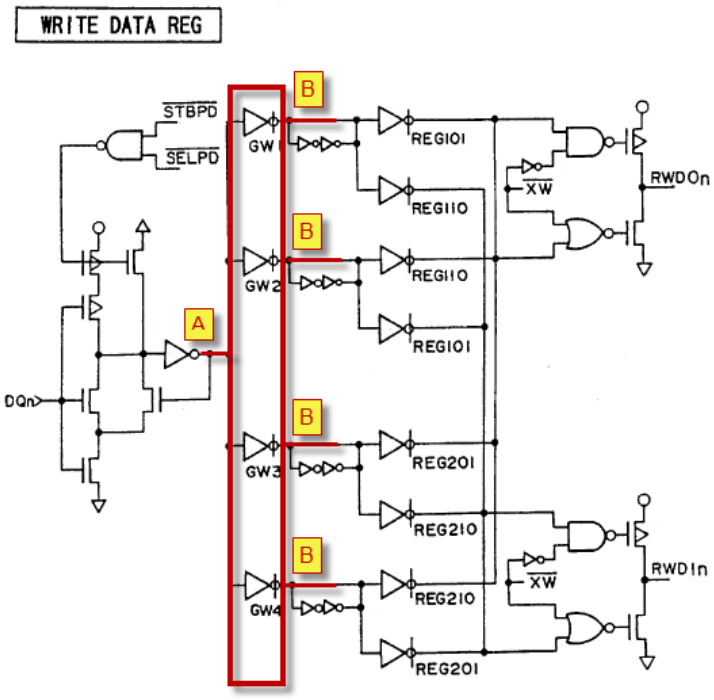
It would have been obvious to a person of ordinary skill in the art to combine Watanabe with Iwama. MICRON-1003, Baker Decl. ¶ 46. Watanabe and Iwama both address the same technical problem – increasing memory access speeds. *Id.* ¶ 47. Watanabe, for example, discloses that "the CPU has been improved to such an extent as to exceed that of the DRAM" and "there exists so far a strong need of memory structure and/or the memory control system which can match the operating speed of the CPU with that of the memory device." MICRON-1005, Watanabe at 1:18-20, 1:50-55. That is to say, CPU speeds have outstripped DRAM speeds. Watanabe proposes a burst write operation to increase memory access speed. More specifically, Watanabe takes serial data, steers the data into different registers using clock pulses, and then releases the data in a burst onto even and odd internal data buses using a write enable signal. *Id.* at Figure 28, 19:17-24.

Like Watanabe, Iwama recognizes that memory speed cannot match processor speed. *See* MICRON-1006, Iwama at (0004) ("[i]n conventional memory ICs, there has been limitation in reading and writing data at high speed due to problems on the process.") Iwama discloses a similar solution to that proposed by Watanabe – a burst write operation. *Id.* at (0007). In the case of

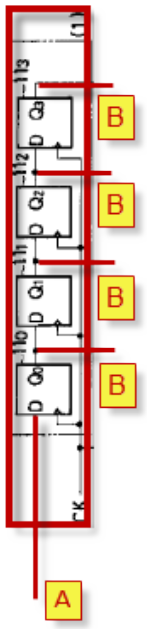
Iwama, however, the serial data is shifted through a plurality of cascade-connected registers to make parallel data. *Id.* at Figure 2, (0010)-(0013).

It would have been obvious to one of ordinary skill in the art for several reasons to adapt Watanabe to include the cascade shift registers disclosed by Iwama. First, as stated above, Iwama's cascade shift registers achieve the same function and result sought by Watanabe – *i.e.*, converting serial data to parallel data. Thus, a person of ordinary skill in the art would have been motivated based on the nature of the problem to be solved to adapt Watanabe to include Iwama's cascade shift registers to achieve the desired function and result. Indeed, both references are directed to solving the same problem. MICRON-1003, Baker Decl. ¶ 48. A person of ordinary skill in the art would have recognized the benefits provided by Iwama. *See, e.g.*, MICRON-1006, Iwama at (0005), (0006), (0018); MICRON-1003, Baker Decl. ¶ 48.

Second, it would have been a simple substitution of two components that would have had a predictable result – *i.e.*, a circuit that would convert serial data to parallel data. Such a simple substitution is reflected in the figures below:



MICRON-1005,
Watanabe at Fig. 28 (annotated).



MICRON-1006,
Iwama at Fig. 2 (annotated).

The figure on the left is Watanabe. The figure on the right is Iwama (rotated 90°). It was well within the skill of a person of ordinary skill in the art to substitute in Iwama's cascade registers for Watanabe's write register gates (GW). The combination of Watanabe and Iwama represent a combination of known elements according to their established functions to achieve predictable results. MICRON-1003, Baker Decl. ¶ 49. It would have been well within the skill of a person of ordinary skill in the art to make such a substitution. The data being treated is the same and the operation is discrete from other operations occurring in the circuit – *i.e.*, the substitution would not interfere with other operations. *Id*. Indeed, the

substitution takes the write register gates, which shift incoming data, and replace those with cascade shift registers.

Third, as mentioned above, to a person of ordinary skill in the art, the decision to use the circuit proposed by Watanabe or the circuit proposed by Iwama is nothing more than a design choice. *Id*. ¶¶ 50-52. Both circuits address the same problem and provide the same result – parallel data for a burst operation. *Id*. *See* MICRON-1005, Watanabe at Figure 28, 19:17-24, *cf.* MICRON-1006, Iwama at Figure 2, (0010)-(0013). Indeed, it was well known to a person of ordinary skill in the art that cascade registers could be used to convert serial data to parallel data—it was the "conventional" circuit for this function. MICRON-1003, Baker Decl. ¶¶ 50-52; *see also* MICRON-1007, U.S. Patent No. 5,337,050 at 1:12-22 ("Sugawara") ("**As a conventional serial-to-parallel converter circuit, these has been known a shift register as shown in FIG. 1 in which digital signals are received in a serial format and are then converted into parallel signals....**") (emphasis added).

9.2. Claim 1 is obvious over Watanabe in view of Iwama

9.2.1. Claim 1: [1.P] A semiconductor memory having a burst mode transfer function, comprising:

Watanabe discloses a semiconductor memory having a burst mode transfer function. Specifically, Watanabe discloses "[a] synchronous LSI memory device, [that] comprises memory cell array sections (BK1, BK2) each having a plurality of

memory cells." MICRON-1005, Watanabe at Abstract. "LSI" is an acronym for "large scale integration." An LSI memory device is a semiconductor memory.

Watanabe further discloses that the LSI memory device includes a burst mode transfer. *See id.* at 19:21-24 ("the column systems of the two-band cell arrays are pipeline-operated via DQ buffers and registers so that an access can be made once between the core sections for each two clocks."); *id.* at 16:32-34 ("In the burst cycle, the counter begins to operate between the fifth cycle and the eighth cycle after the column access cycle."); *see also id*. at 3:13-19, 15:40-45, Figure 98.

9.2.2. [1.1] a plurality of memory cell sub-arrays which are accessible in parallel and simultaneously

Watanabe discloses a semiconductor memory comprising a plurality of memory cell sub-arrays that are accessible in parallel and simultaneously. MICRON-1005, Watanabe at Figure 1 depicts the memory device of Watanabe:

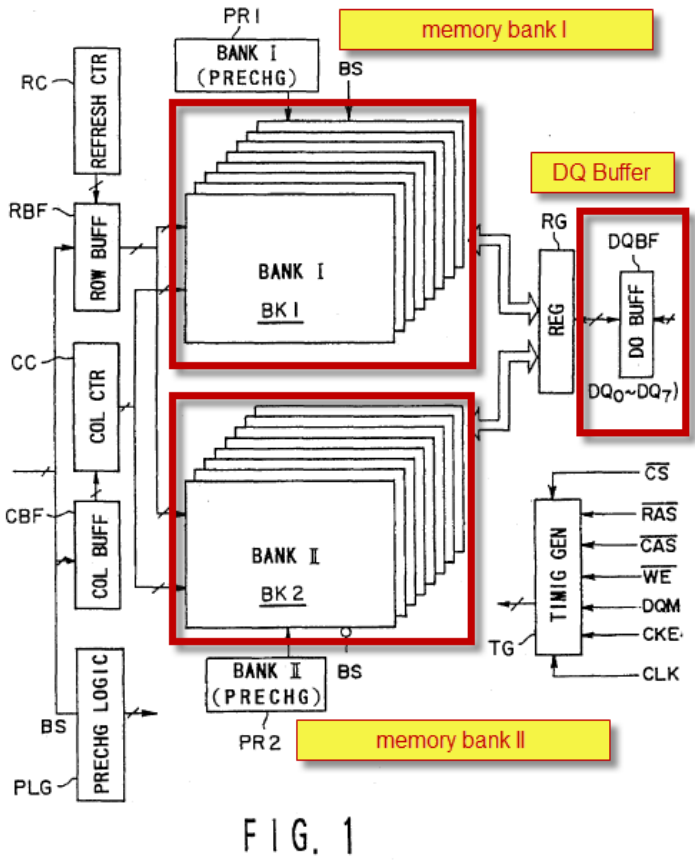


FIG. 1

MICRON-1005, Watanabe at Figure 1 (annotated).

The memory device includes several memory areas arranged in two memory banks – memory banks I and II. Data stored in the DQ buffer (note that there is one buffer for each DQ pin) is written in parallel to subarrays within these banks. Watanabe at Figure 1, above, depicts an 8-bit DRAM (DQ pins 0-7). MICRON-1005, Watanabe at Figure 2 depicts the circuit for diagram for writing to a 4-bit DRAM.

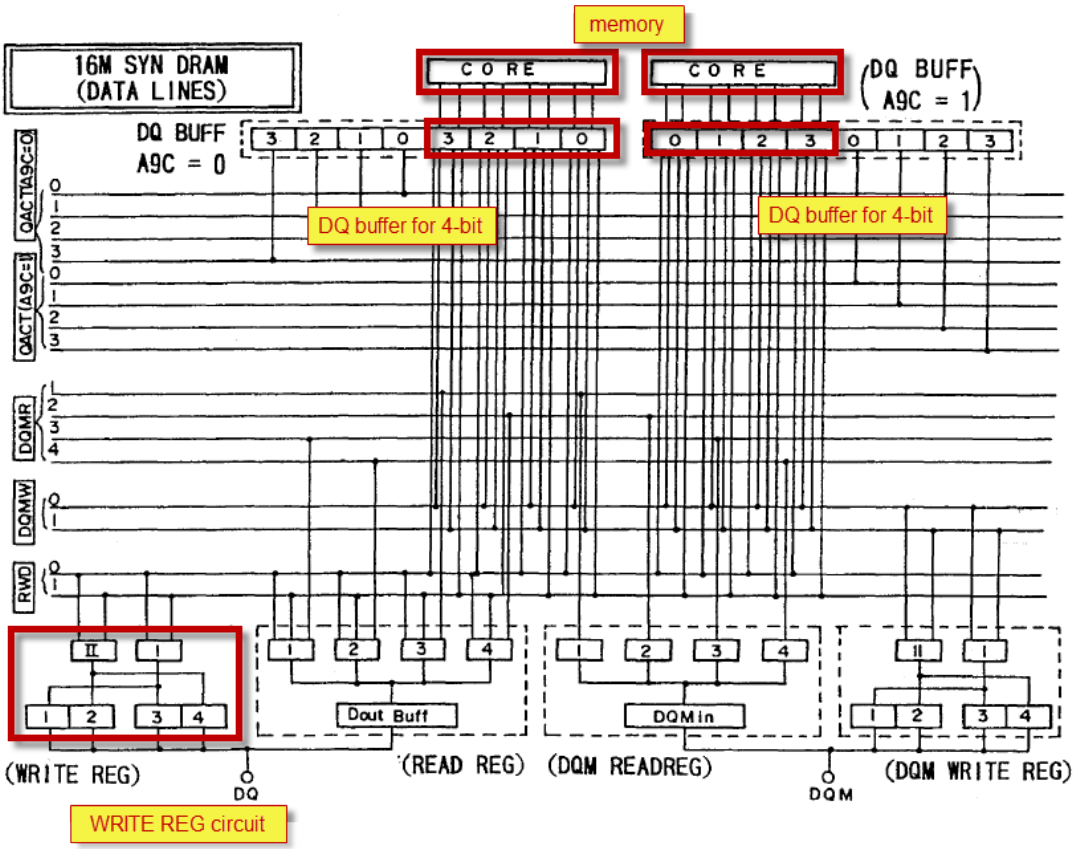


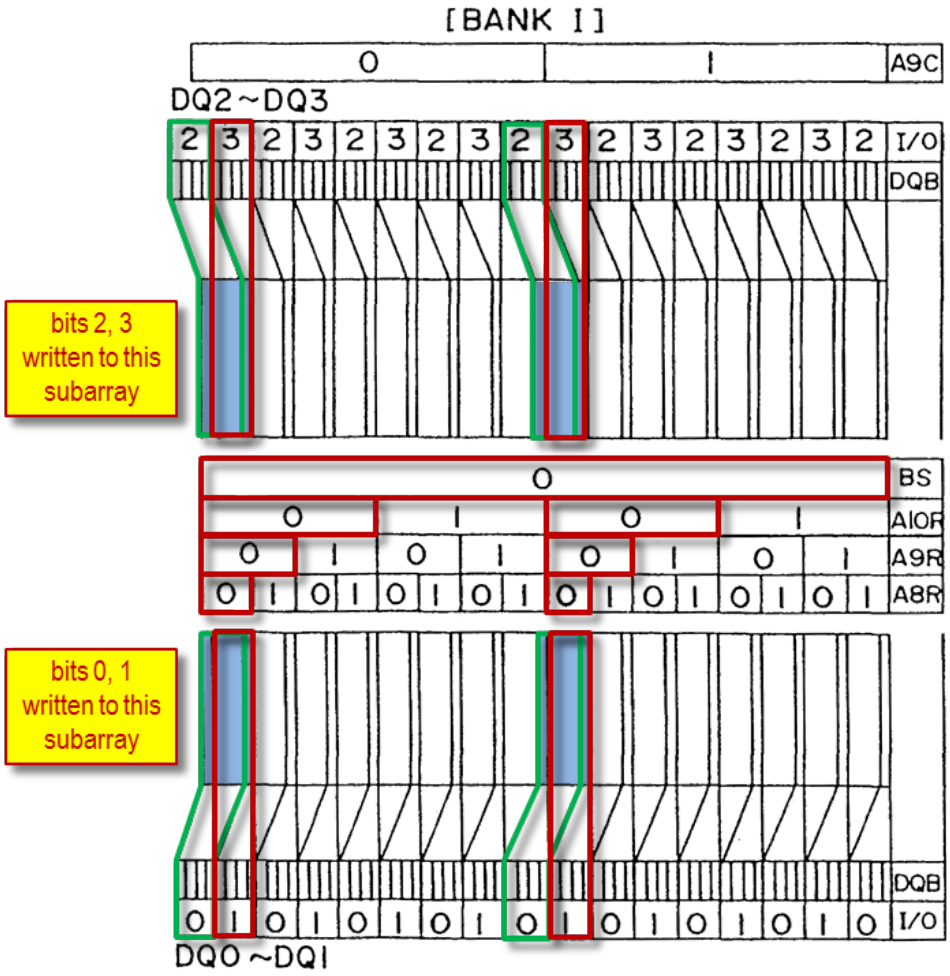
FIG. 2

MICRON-1005, Watanabe at Figure 2 (annotated).

The 4-bit DRAM includes a WRITE REG circuit for taking serial data and converting that data to parallel data. The data is stored by 4 bits in the DQ buffer. The 4-bits are then written simultaneously to a plurality of subarrays. *See id*. at 9:54-57 ("These registers are connected to the DQ buffer via RWD lines, respectively. The DQ buffer is a circuit for transferring data to the cell array sections through the DQ lines."), 19:17-24 ("As describe above, in the synchronous LSI memory device according to the present invention, the cell arrays are divided into two banks; there are provided the timing generators for generating accessing signals in synchronism with the masked CLK signal; the column systems

of the two-band cell arrays are pipeline-operated via DQ buffers and registers so that an access can be made once between the core sections for each two clocks.").

Watanabe at Figure 77 depicts the interrelation of the memory banks and the DQ buffer. For illustration purposes, only Bank I is depicted.



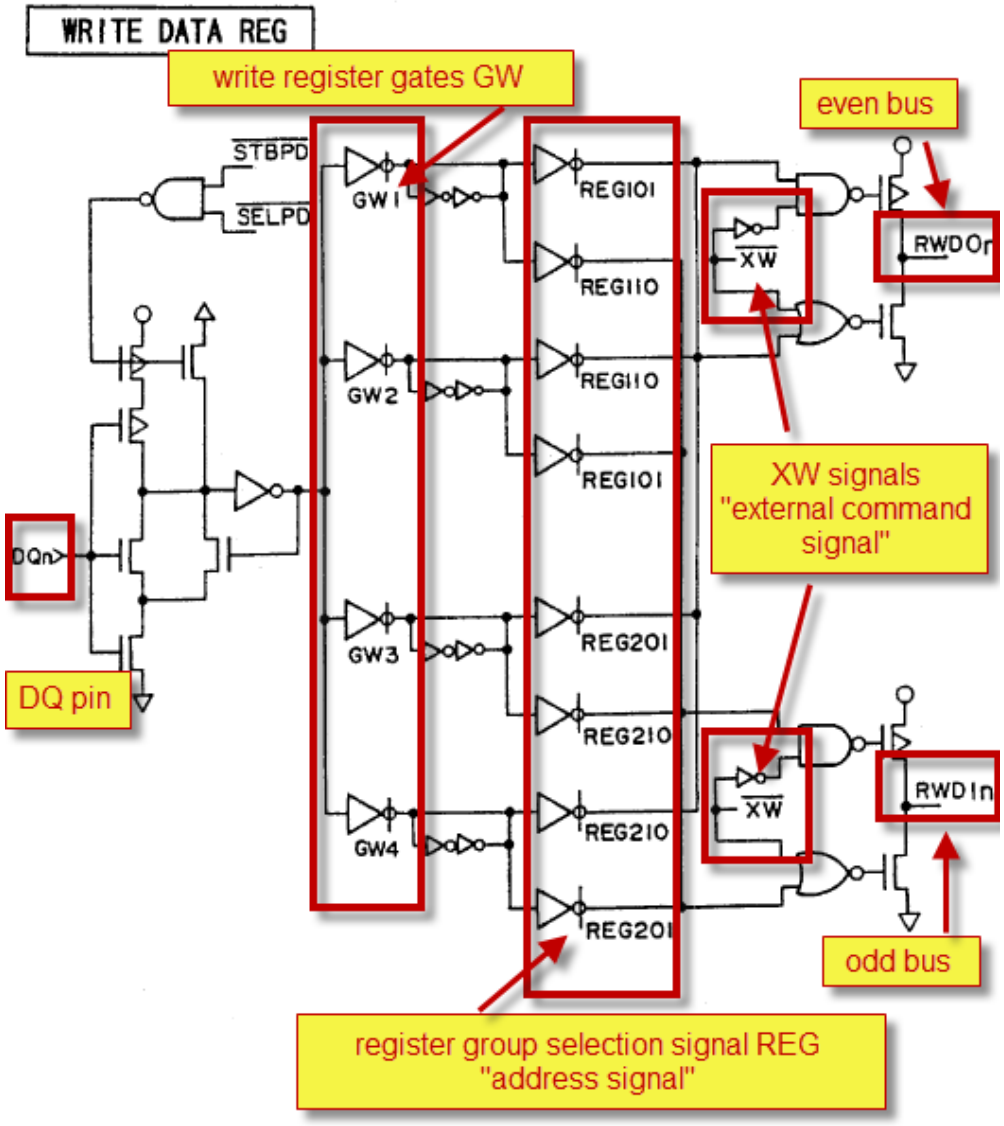
MICRON-1005, Watanabe at Figure 77 (annotated) (depicting only bank I).

When data is written, signals are decoded to determine which sub-arrays the data is to be written – *e.g.*, BS, A10R, A9R, and A8R. For example, if BS, A10R, A9R, and A8R are 0 (illustrated above), then data will be written from the DQ

buffer as shown above. The sub-arrays that the data is written to are shaded in blue. The first bits (0, 1) are written to the bottom left memory sub-array simultaneously with the second bits (2, 3) being written to the top memory sub-array. "When a plurality of cell arrays are serial-accessed, the serial access is so controlled that a plurality of cell arrays are accessed simultaneously." MICRON-1005, Watanabe at 19:7-9. "[T]here are four DQ buffers on either side of each cell array, in which the DQ buffers arranged on both sides of the activated cell array are activated." *Id.* at 9:66-10:2.

9.2.3. [1.2] a plurality of internal data buses for inputting and outputting data to and from said plurality of memory cell sub-arrays, in parallel; and

Watanabe discloses a semiconductor memory that comprises a plurality of internal data buses for inputting and outputting data to and from a plurality of memory cell sub-arrays, in parallel. Specifically, as discussed in the previous limitation, Watanabe at Figure 2 discloses even and odd RWD lines, which read and write data to and from the memory cell subarrays in parallel. *See id.* at Figure 28 (annotated), Table 15, 9:54-57, 11:19-27.



MICRON-1005, Watanabe at Fig. 28 (annotated).

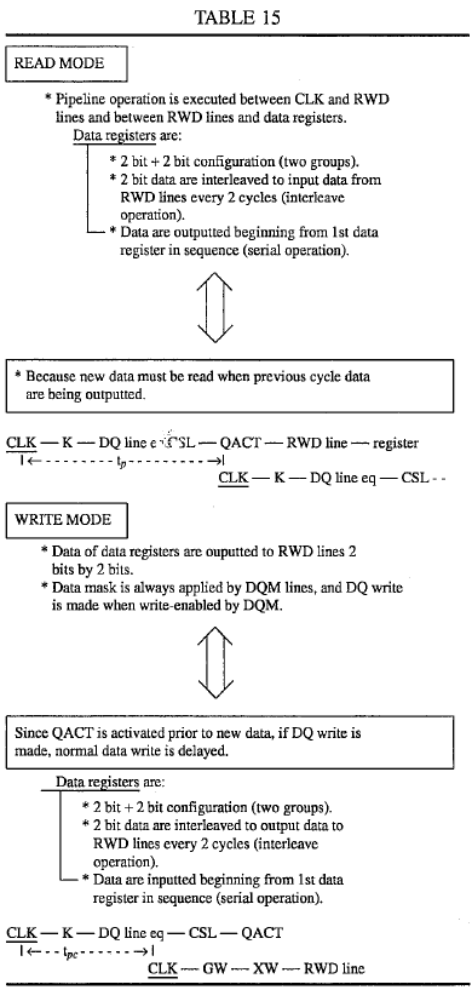


TABLE 15

READ MODE

* Pipeline operation is executed between CLK and RWD lines and between RWD lines and data registers.
  Data registers are:
  * 2 bit + 2 bit configuration (two groups).
  * 2 bit data are interleaved to input data from RWD lines every 2 cycles (interleave operation).
  * Data are outputted beginning from 1st data register in sequence (serial operation).

* Because new data must be read when previous cycle data are being outputted.

CLK — K — DQ line eq — CSL — QACT — RWD line — register
|← - - - - - - - - t_p - - - - - - - - →|
CLK — K — DQ line eq — CSL - -

WRITE MODE

* Data of data registers are ouputted to RWD lines 2 bits by 2 bits.
* Data mask is always applied by DQM lines, and DQ write is made when write-enabled by DQM.

Since QACT is activated prior to new data, if DQ write is made, normal data write is delayed.

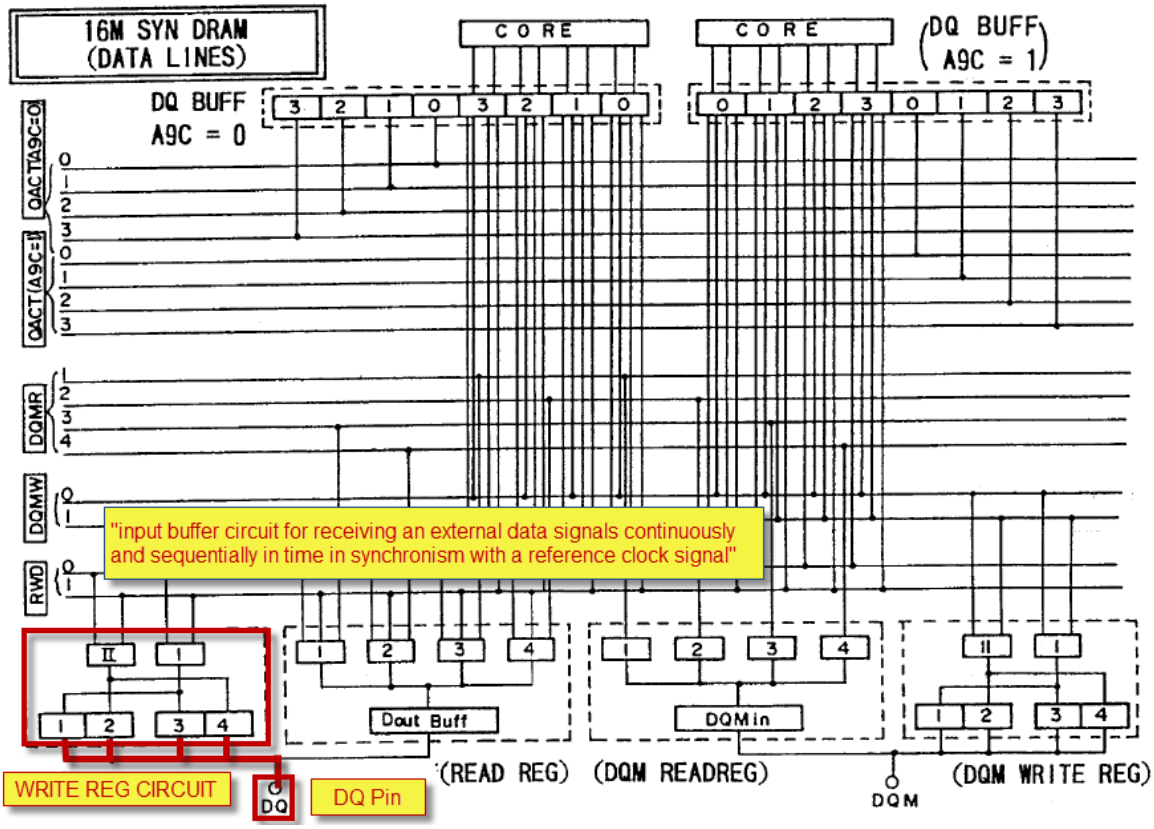
Data registers are:
* 2 bit + 2 bit configuration (two groups).
* 2 bit data are interleaved to output data to RWD lines every 2 cycles (interleave operation).
* Data are inputted beginning from 1st data register in sequence (serial operation).

CLK — K — DQ line eq — CSL — QACT
|← - - t_{pc} - - - - - - →|
CLK — GW — XW — RWD line

MICRON-1005, Watanabe at Table 15.

9.2.4. [1.3] an input buffer circuit receiving an external data signals continuously and sequentially in time in synchronism with a reference clock signal, for converting said receiving serial data into a parallel data under control of an external command signal and an external address signal, so as to distribute said parallel data to said plurality of internal data buses

Watanabe discloses an input buffer circuit that receives external data signals continuously and sequentially in time in synchronism with a reference clock signal. Namely, Watanabe discloses write data registers (WRITE REG) for receiving and writing data. *See* MICRON-1005, Watanabe at Figure 2.

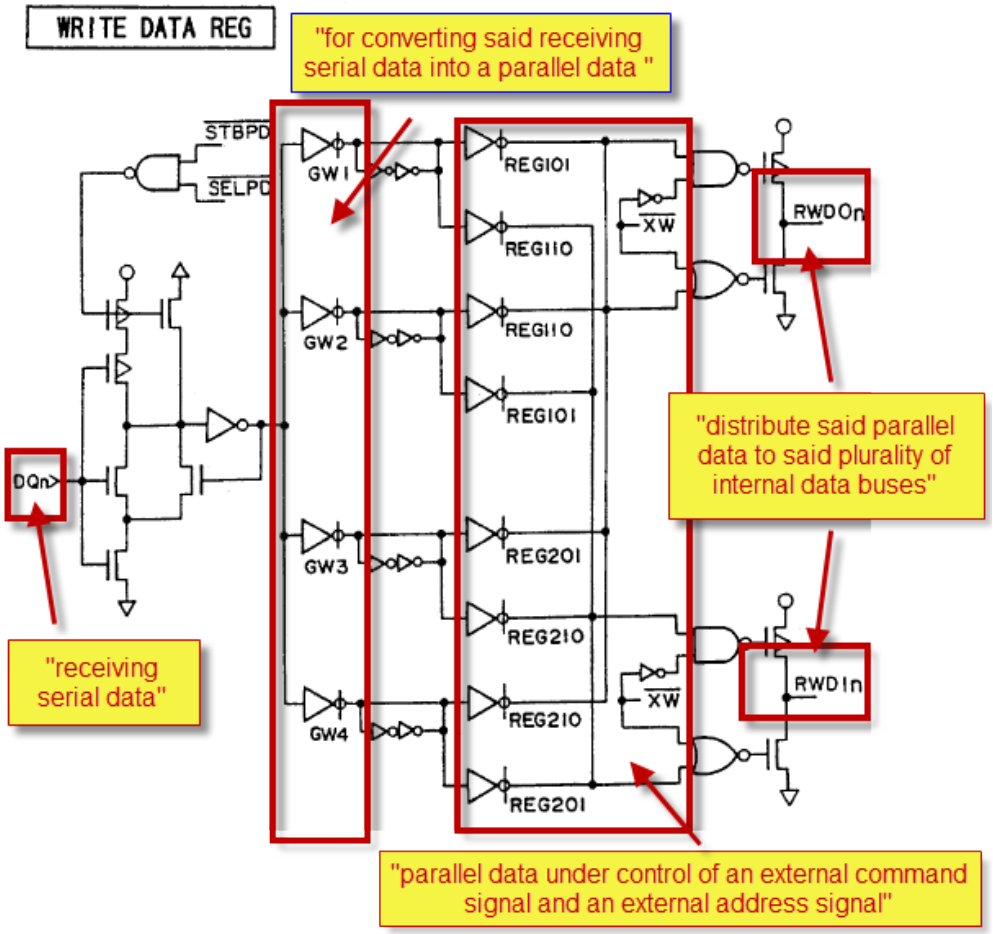


MICRON-1005, Watanabe at Figure 2 (annotated).

The data is received by the WRITE REG circuit continuously and sequentially in time in synchronism with a reference signal clock. Watanabe specifically states that "data register means (WRITE REGISTER) for **acquiring externally input data applied to first terminals (DQ) in synchronism with a clock signal (CLK)**, said data register means being provided with inputting registers (WRITE REGISTER) having a plurality of bits and connected to the respective first terminals; and when data are inputted, the inputting registers being controlled so that the

respective plural bits are set alternately to data input status (FIG. 61)." MICRON-1005, Watanabe at 7:24-34 (emphasis added).

The WRITE REG is detailed in Figure 28 of Watanabe (note there is a WRITE REG for each DQ pin).

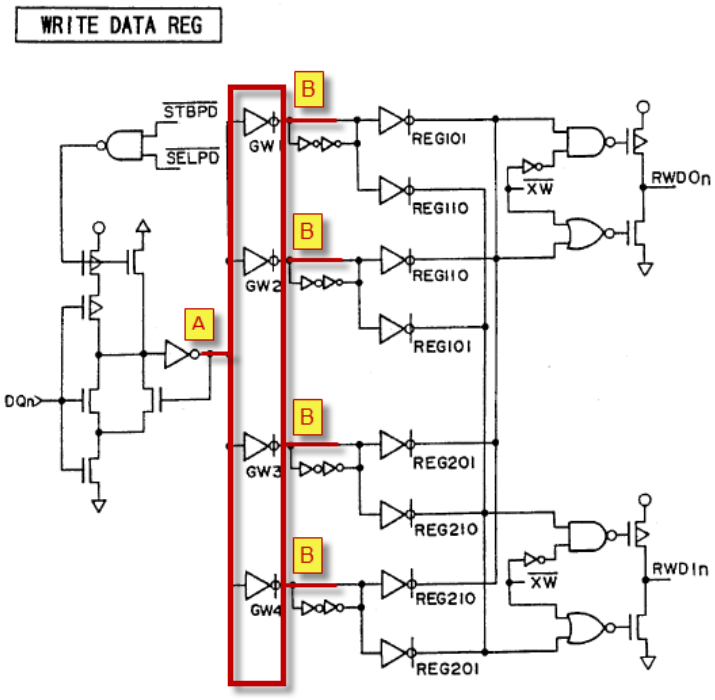


MICRON-1005, Watanabe at Figure 28 (annotated).

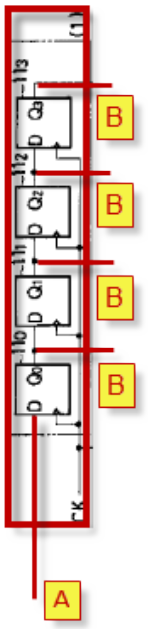
Thus, as shown, WRITE REG receives serial data at the DQ pin. *See also id.* at 7:24-34. And the serial data is converted into parallel data under control of an external command signal and an external address signal, so as to distribute said

parallel data to said plurality of internal data buses. It creates parallel data by using write register gates GW to distribute the data to different shift registers, which are maintained in parallel (*see* MICRON-1005, Watanabe at Figure 28, above). *Id.* at 11:29-32 ("In contrast with this, in the write mode, it is necessary that the write-mode register interleaves the register group two bits by two bits to transfer data from the registers to the RWD lines for each two cycles."); *See also id.* at 19:7-9; 19:17-24. The registers release the parallel data in response to REG signals (*i.e.,* address signals – *see* below) and the data is output to the internal data buses in response to $\overline{XW}$ signals (*i.e.*, external command signals).

Note, however, that claim 1 requires cascade-connected registers to create the parallel data – *see* next limitation. Watanabe's write register gates GW are not cascade-connected registers. Iwama, however, discloses cascade-connected registers for creating parallel data (discussed in detail in the next limitation). MICRON-1006, Iwama at (0012) ("FF 11_0-11_3 forms a serial-parallel conversion shift register and generates the output converted to the parallel data to the output Q_0-Q_3 by shifting the data input comprising a serial signal in response to a clock CK. The output Q_0-Q_3 of the serial-parallel conversion shift register sequentially is shifted one bit at a time."). Iwama's cascade-connected shift registers are substituted for Watanabe's write register gates GW for the reasons discussed in Section 9.1. Data is received by the cascade shift registers along line A.



MICRON-1005,
Watanabe at Fig. 28 (annotated).



MICRON-1006,
Iwama at Fig. 2 (annotated).

Once through the cascade-connected registers, the data has been converted to parallel data, output along lines B, and is under control of an external command signal and an external address signal. Specifically, the parallel data is directed by two types of signals – REG signals and $\overline{XW}$ signals. These signals are depicted below:

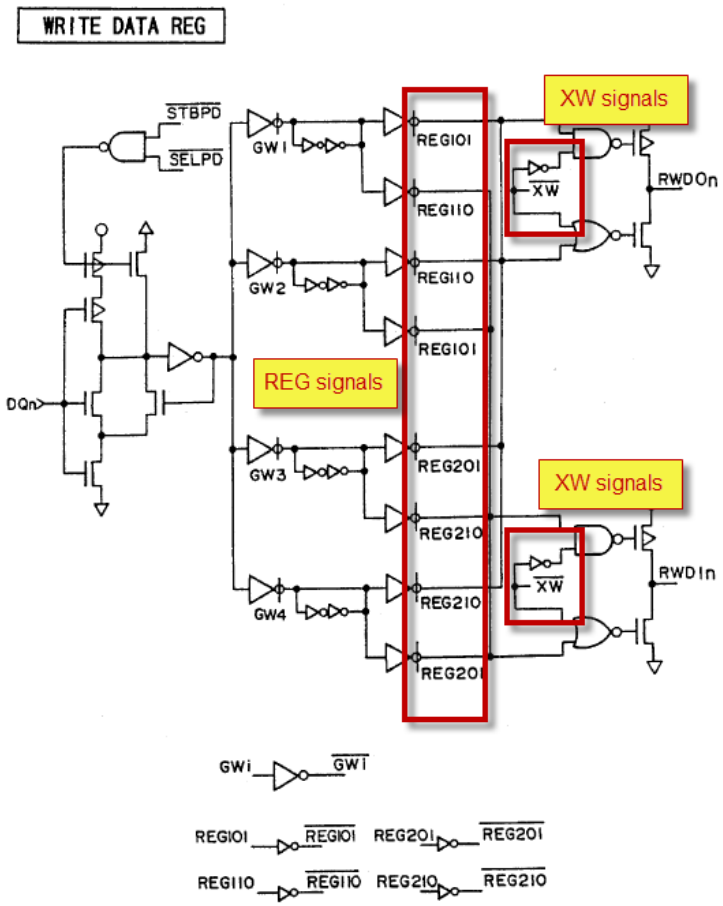


FIG. 28

MICRON-1005, Watanabe at Figure 28 (annotated).

The REG signals are the "external address signal." The REG signals are generated in the transfer selection generating circuit. The REG signal is generated from the ALT0 signal, which is address A0. This relationship is seen in Watanabe at Figures 26 (the transfer selection generating circuit) and 30(C) (a table listing the relationship between ALT0 and address A0):

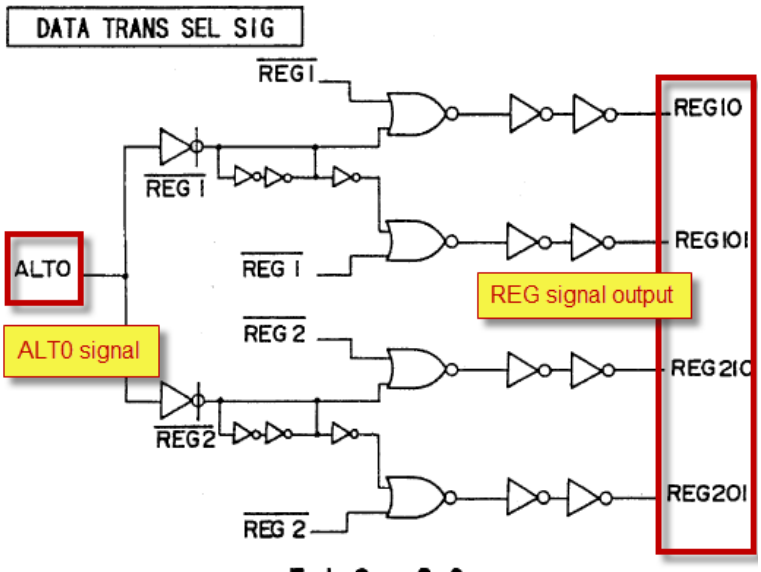


FIG. 26

ADDRESS	SIG NAME	DESTINATION
A0	ALT0	XR, XW, QACT SEL, CDRV SEL
A1	ALT1	QACT SEL, CDRV SEL
	AIN3	CTR
A4	AIN4	CTR
A5	AIN5	CTR
A6	AIN6	CTR
A7	AIN7	CTR
A8	AIN8	CTR
A9	ALT9	QACT SEL
A10		ROW
BS	BSCL	KI/II

Address A0 is the ALT0 signal

FIG. 30 (C)

MICRON-1005, Watanabe at Figure 26 and Figure 30(C) (annotated).

Thus, the parallel data is under control of an external address (A0), so as to distribute the data to even and odd internal buses.

The $\overline{XW}$ signals are the "external command signals." Watanabe at Figure 27 depicts the circuit, the write data transfer signal generating circuit, for generating external command signal $\overline{XW}$. Note that it is generated based on WECL, which is generated based on WE (write enable) (*see* MICRON-1005, Watanabe at Figure 31A), which is an external signal. *See also id.* at Figure 1. In other words, WECL is essentially a buffered version of WE. As seen in Figure 28, above, the $\overline{XW}$

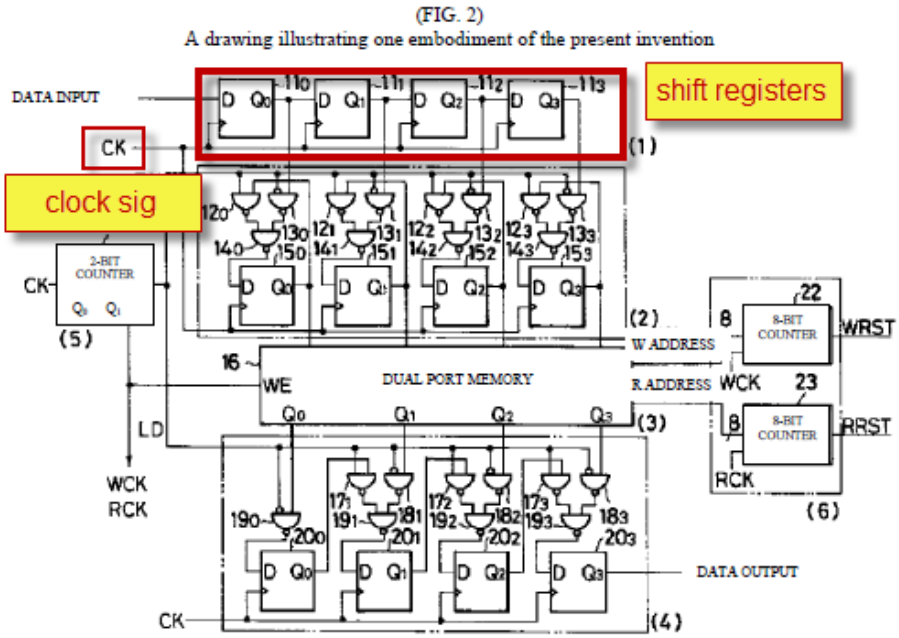
signals distribute the data onto the even and odd internal buses RWD0 and RWD1.[2]

In sum, Watanabe discloses an input buffer (write register) receiving an external data signals (*e.g.*, on DQ0 pin) continuously and sequentially in time in synchronism with a reference clock signal (*i.e.*, CLK) and converting said receiving serial data into a parallel data (via Iwama's cascade-connected registers) under control of an external command signal (*e.g.*, write enable ($\overline{XW}$)) and an external address signal (*e.g.*, A0), so as to distribute (in accordance with REG signals) said parallel data to said plurality of internal data buses (*e.g.*, RWD lines).

[2] The XW signals are enable signals because if XW is high, the output of the NAND gate will be high (which drives a PMOS) and the output of the NOR gate will be low (which drives a NMOS), which will tristate the RWD0n and RWD1n buses (no data passes). When XW is low (active), the NAND and NOR devices are enabled to drive the data signal to the pull-up and pull-down devices, thereby driving the RWD0n and RWD1n buses. See MICRON-1003, Baker Decl. Appx. A at claim [1.3].

9.2.5. [1.4a] the input buffer circuit including a shift register circuit composed of a plurality of cascade-connected registers and for latching and shifting said external data signals only in response to said reference clock signal, said cascade-connected registers outputting, in parallel, said data latched in said respective registers,

Iwama discloses an input buffer circuit comprising a shift register circuit composed of a plurality of cascade-connected registers. Specifically, Iwama's input buffer is depicted in Figure 2.



MICRON-1006, Iwama at Figure 2 (annotated).

The cascade-connected shift registers are labeled 11_0-11_3, which shift the data across the registers. *See* MICRON-1006, Iwama at (0010) ("FIG. 2 is a drawing illustrating one embodiment of the present invention, where 11_0-11_3 are flip-flops (FF) that constitute the shift register"); *see also id.* at (0012)-(0013) ((0012) "FF 11_0-11_3 forms a serial-parallel conversion shift register and generates the output

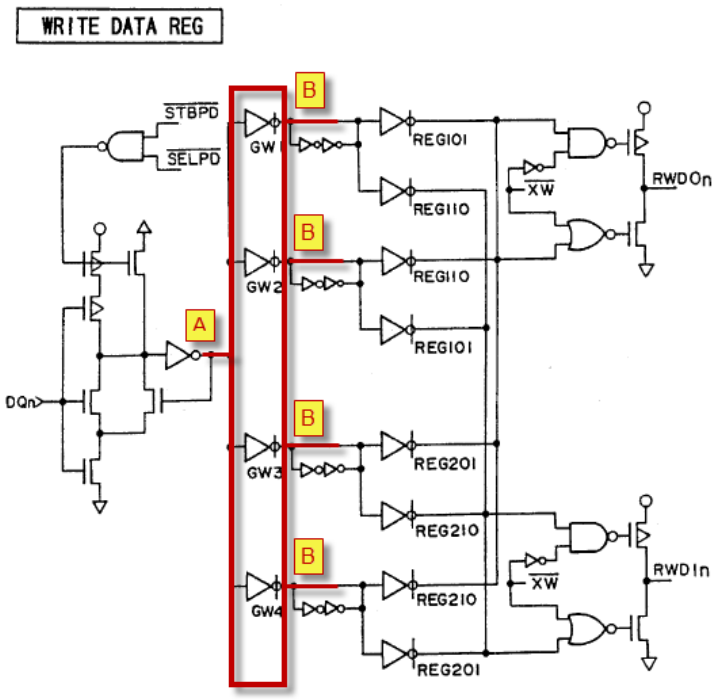
converted to the parallel data to the output Q_0-Q_3 by shifting the data input comprising a serial signal in response to a clock CK. The output Q_0-Q_3 of the serial-parallel conversion shift register sequentially is shifted one bit at a time. (0013) NAND gates 12_0-12_3, 13_0-13_3, and 14_0-14_3 and FF 15_0-15_3 forms a parallel data latch, incorporates the output Q_0-Q_3 of the serial-parallel conversion shift register to FF 15_0-15_3 at each 4 bits in response to the enable (EN) signal, and generates a parallel data of 4-bit length to the output Q_0-Q_3 of FF 15_0-15_3 by holding the incorporated data for 3-bit period.")

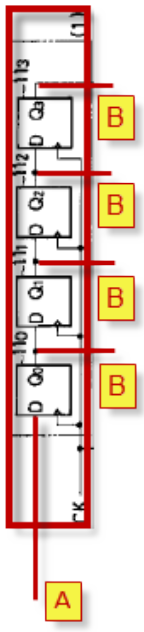
Iwama further discloses that the shift registers 11_0-11_3 shift the data only in response to a reference clock signal and the result data is output in parallel. Specifically, data D is latched and shifted only in response to signal CK. *See id.* at (0012) ("FF 11_0-11_3 forms a serial-parallel conversion shift register and generates the output converted to the parallel data to the output Q_0-Q_3 by shifting the data input comprising a serial signal in response to a clock CK.") The process of latching and shifting the data converts the serial data to parallel data. *Id.*

9.2.6. [1.4b][the input buffer circuit including a] register output selecting means receiving said data signals outputted in parallel from said cascade-connected registers, for distributing said received parallel data signals, in parallel, to said plurality of internal data buses in accordance with said external address signal.

Watanabe in view of Iwama discloses an input buffer circuit that includes a register output selecting means that receives the data signals that were outputted in

parallel from the cascade-connected registers. Recall that Watanabe discloses an input buffer WRITE REG in Figure 28, depicted below on the left.



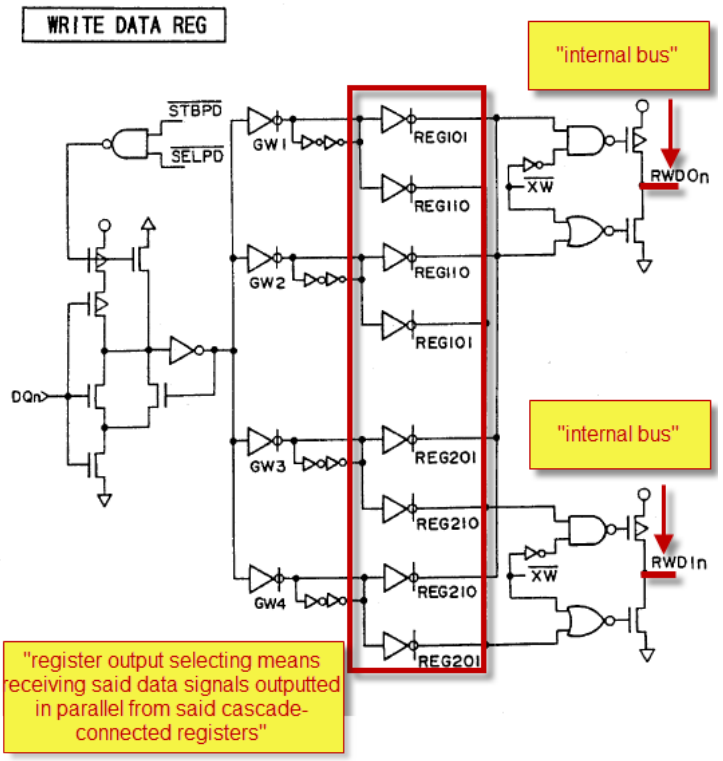


MICRON-1005, Watanabe at Fig. 28 (annotated).

MICRON-1006, Iwama at Fig. 2 (annotated).

In the combination of Watanabe and Iwama, Watanabe is adapted to replace Watanabe's GW gates with Iwama's cascade-connected shift registers (highlighted in red on the right, above). *See* MICRON-1006, Iwama at (0012) ("FF 11_0-11_3 forms a serial-parallel conversion shift register and generates the output converted to the parallel data to the output Q_0-Q_3 by shifting the data input comprising a serial signal in response to a clock CK. The output Q_0-Q_3 of the serial-parallel conversion shift register sequentially is shifted one bit at a time.").

The outputted data is now parallel, stored, and waiting to be distributed to the internal buses. MICRON-1005, Watanabe at 11:29-32 ("In contrast with this, in the write mode, it is necessary that the write-mode register interleaves the register group two bits by two bits to transfer data from the registers to the RWD lines for each two cycles."). This represents Watanabe's register output selecting means:

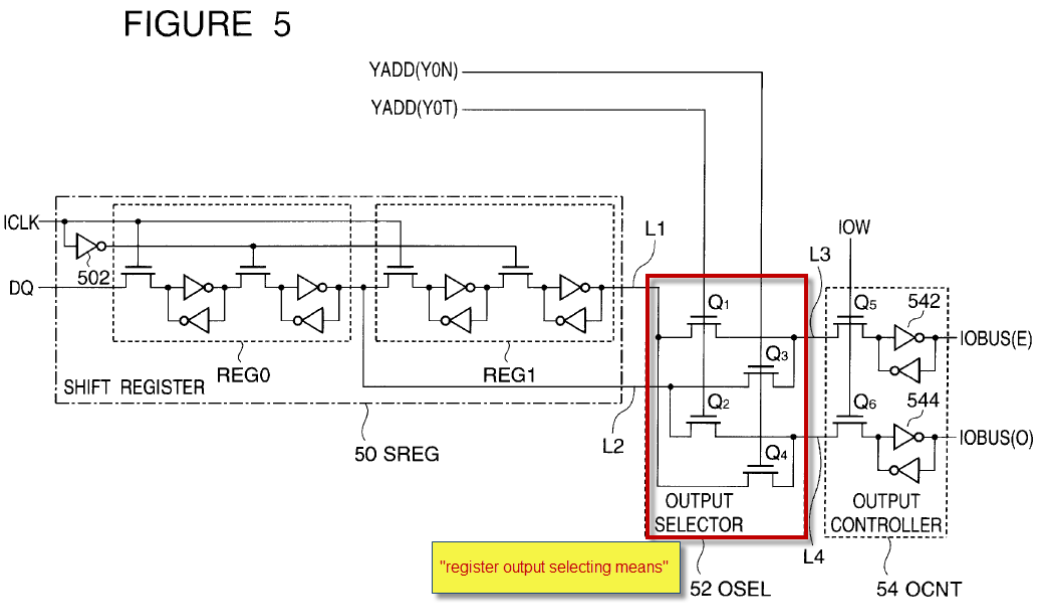


MICRON-1005, Watanabe at Figure 28 (annotated).

Thus, Watanabe in view of Iwama discloses an input buffer including a register output selecting means that receives data outputted in parallel from the cascade-connected registers of Iwama. This data is then selectively distributed in parallel to internal buses RWD0 and RWD1.

Watanabe further discloses that its register output selecting means selectively distributes its data in parallel to a plurality of internal data buses in accordance with an external address signal. As discussed in detail in reference to limitation [1.3], the data is selectively distributed in accordance with a REG signal. MICRON-1005, Watanabe at Figure 28. The REG signals are generated as a function of an ALT0 signal, which is address A0. *See id.* at Figures 26, 30(C) (correlating the ALT0 signal with address A0). Thus, Watanabe in view of Iwama discloses an input buffer (WRITE REG) including a register output selecting means (REG gates) that receives data signals outputted in parallel from cascade-connected registers (Iwama) and selectively distributes the data in parallel to a plurality of internal data buses (RWD0 and RWD1) in accordance with external address A0 (REG signal).

To the extent that "register output selecting means" is governed by 35 U.S.C. §112 ¶ 6, Watanabe's register output selecting means performs the identical function, in the same or equivalent way, to provide the same result. For comparison, the 504 Patent's register output selecting means is depicted below – 52 OSEL:

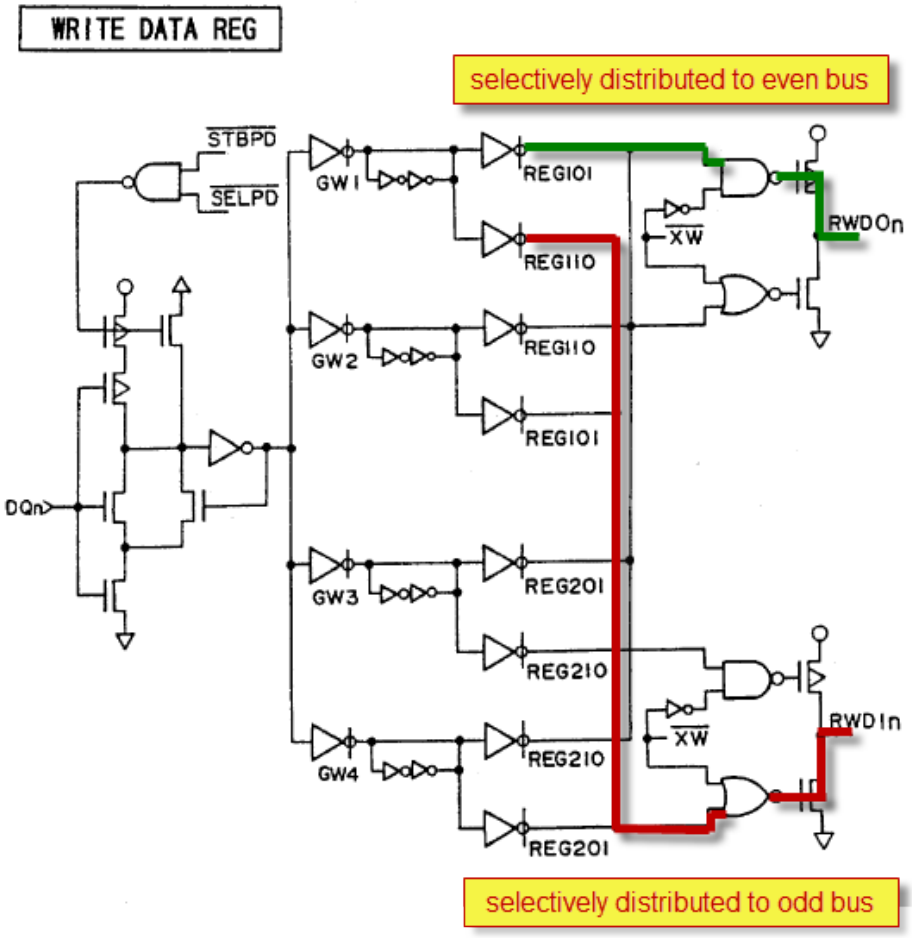


MICRON-1001, 504 Patent at Figure 5 (annotated).

Register output selecting means 52 OSEL includes transfer gates Q1-Q4. These gates selectively distribute data to either the even or odd internal bus based on the "internal column address signal YADD" and the "inverted signal YADD(Y0N) of the least significant bit YADD(Y0T) of the internal column address signal YADD." MICRON-1001, 504 Patent at 9:54-10:2. Thus, as discussed in Section 6.2.1, above, the corresponding structure is a plurality of transfer gate transistors responsive to the column address to selectively distribute data in parallel to either the even or odd internal buses and equivalents thereof.

Watanabe is no different. The data is distributed by transfer gates transistors (circuitry on the memory chip is implemented as transistors), *see* MICRON-1005, Watanabe at Figure 28, above, in accordance with REG signals, which are a

function of the address. *Id.* at Figures 26, 28, and 30(C). For example, in Watanabe the address may dictate that data in the GW1 register (one of the serial registers in Iwama) can be selectively distributed to the even or odd bus. Specifically, this data via REG101 is selectively distributed to the even bus while this data via REG110 is selectively distributed to the odd bus – *see* Figure 28 below.



MICRON-1001, 504 Patent at Figure 28 (annotated).

Both Watanabe in view of Iwama and the 504 Patent use transistors and an address signal to achieve this function. In both cases, the data is distributed to a plurality of buses based on an external address.

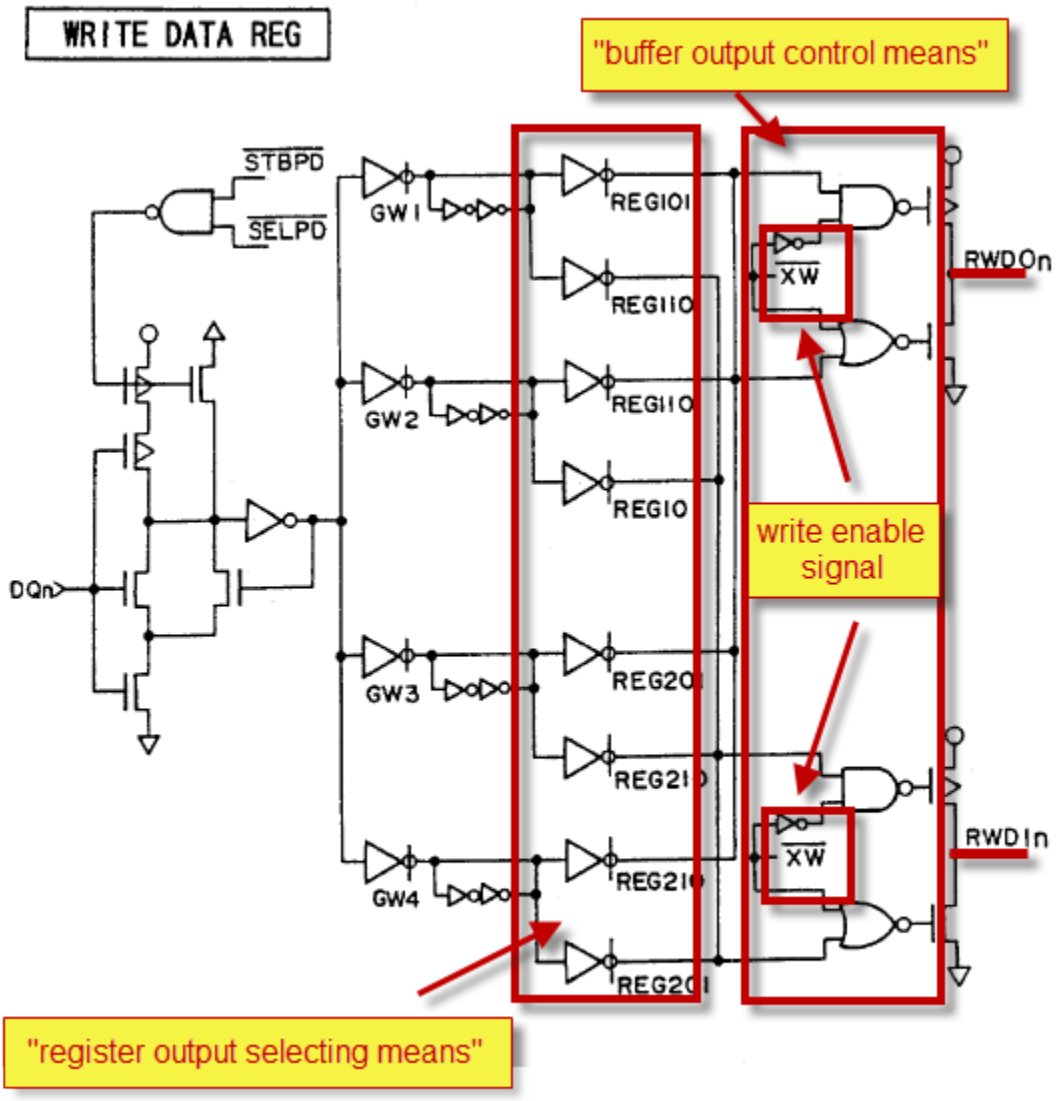
In sum, by disclosing transmission gate transistors responsive to the column address (REG signals which are derived from the A0 address), Watanabe in view of Iwama discloses an input buffer circuit including a register output selecting means receiving said data signals outputted in parallel from said cascade-connected registers, for distributing said received parallel data signals, in parallel, to said plurality of internal data buses in accordance with said external address signal. Moreover, Watanabe in view of Iwama discloses the same (or at least equivalent) structure, performing the identical function to achieve the same result.

9.3. Claim 2 is obvious over Watanabe in view of Iwama

9.3.1. [2.1] A semiconductor memory claimed in claim 1 wherein said input buffer circuit further includes a buffer output control means for transferring said outputs of said register output selecting means, simultaneously and in parallel, to said plurality of internal data buses, in synchronism with an edge of said reference clock signal by which said external data signal finally supplied to said shift register circuit is latched in said shift register circuit.

Watanabe discloses an input buffer that includes a buffer output control means for transferring the outputs of the register output selecting means, simultaneously and in parallel, to the plurality of internal data buses, in synchronism with an edge of the reference clock signal by which the external data

signal finally supplied to the shift register circuit is latched in said shift register circuit. Watanabe's buffer output control means is highlighted on the right, below:



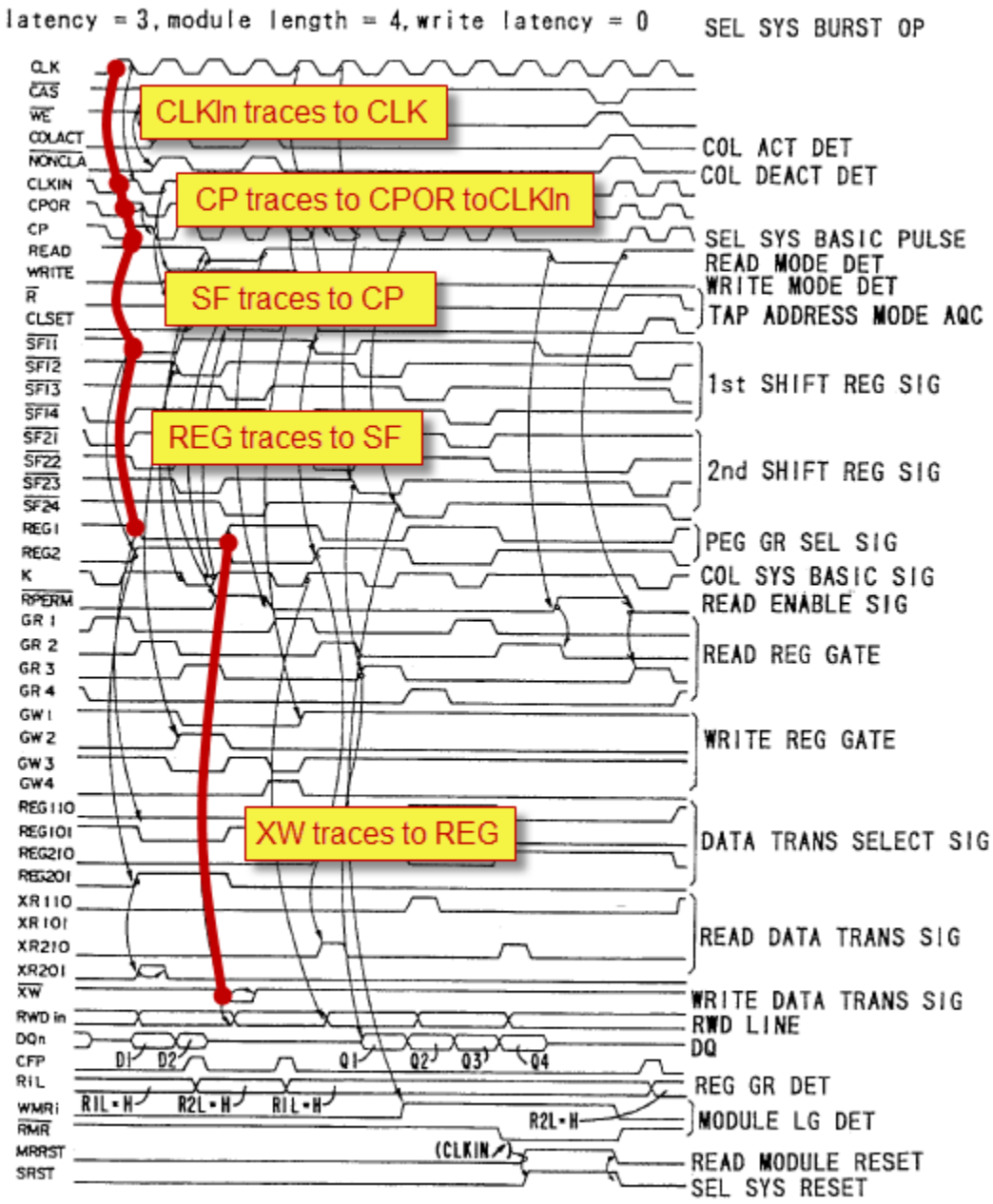
MICRON-1005, Watanabe at Figure 28 (annotated).

Watanabe's "buffer output control means" receives the output from "register output selecting means" (*i.e.*, REG gates). Watanabe takes this output and transfers it simultaneously and in parallel to internal buses RWD0 and RWD1

(even and odd buses) in response to signal $\overline{XW}$. MICRON 1005, Watanabe at 11:29-32 ("In contrast with this, in the write mode, it is necessary that the write-mode register interleaves the register group two bits by two bits to transfer data from the registers to the RWD lines for each two cycles."); *See also id.* at 19:7-9; 19:17-24.

The XW signals are enable signals that drive the internal buses. If XW is high, the output of the NAND gate will be high (which drives a PMOS) and the output of the NOR gate will be low (which drives a NMOS), which will tristate the RWD0n and RWD1n buses (no data passes). When XW is low (active), the NAND and NOR devices are enabled to drive the data signal to the pull-up and pull-down devices, thereby driving the RWD0n and RWD1n buses.

Signal $\overline{XW}$ is in synchronism with the edge of the reference clock. As an initial matter, Watanabe discloses a synchronous LSI memory device. That is, its operation is in synchronism with an external clock. This relationship is seen in Watanabe at Figure 97, which depicts the write operation in synchronism with clock signal CLK.

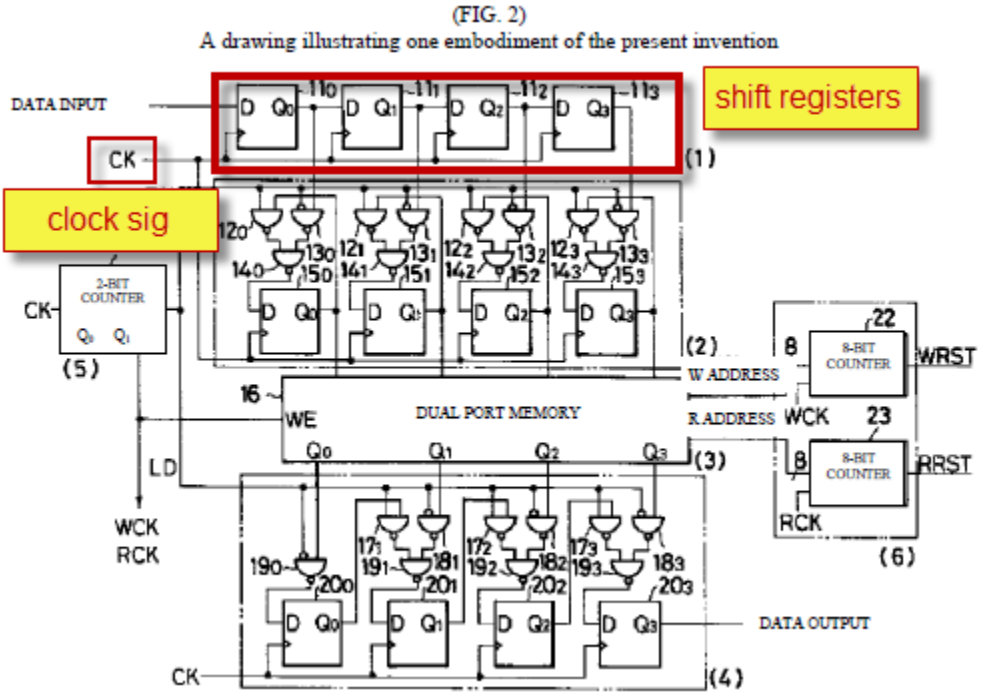


MICRON-1005, Watanabe at Figure 97 (annotated).

Specifically, Figure 97 depicts that signal $\overline{XW}$ can be traced back to the edge of the CP signal and then to the edge of the CLK signal, which releases the data to the internal buses in synchronism with CLK. *See also* MICRON 1005, Watanabe at Figures 4, 15-17, 27, and 28. It should be further noted that Watanabe discloses

a "synchronous LSI memory device." "Synchronous" means in synchronism with the clock. MICRON-1003, Baker Decl. ¶ 38.

Claim 2 requires that outputs of said register output selecting means are transferred in synchronism with the same reference clock used to latch the data in the shift register circuit. As seen above, Watanabe releases the data to the even and odd RWD lines in response to signal $\overline{XW}$, which is in synchronism with CLK. The clock signal is the same reference signal used in Iwama. Recall that Iwama uses the CK with its cascaded-connected registers to latch the data:

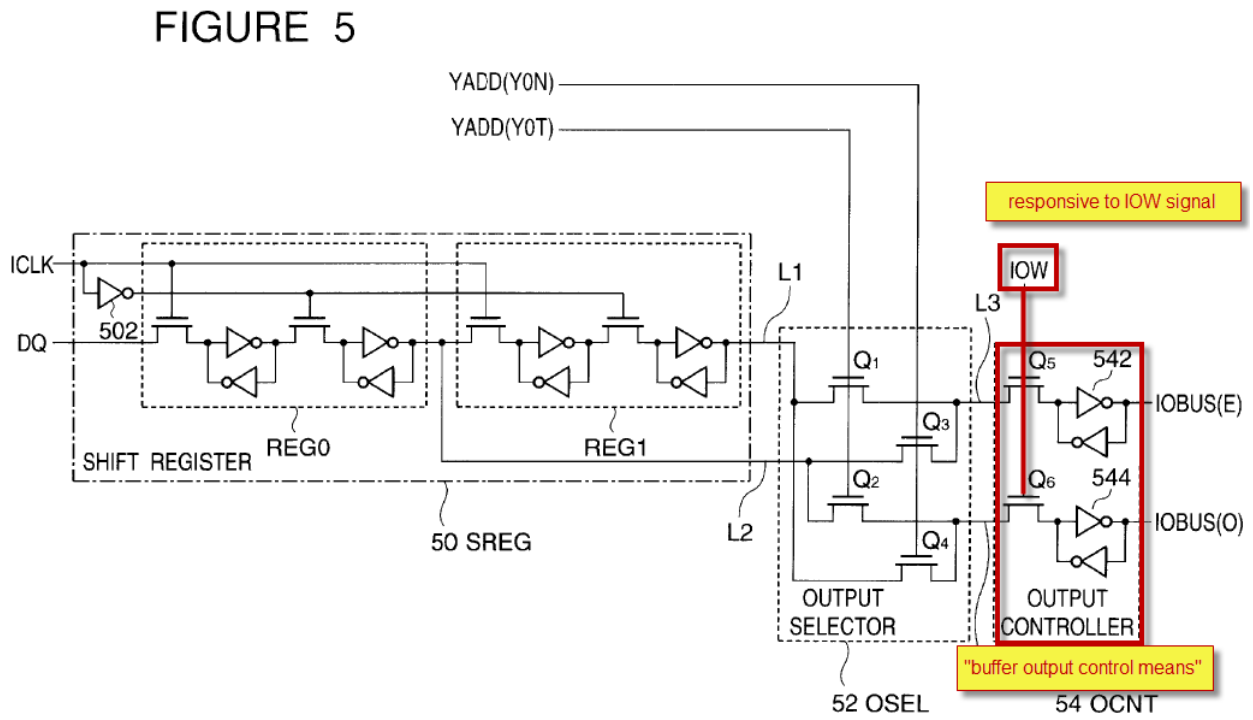


MICRON-1006, Iwama at Figure 2 (annotated).

Thus, Watanabe's output buffer control means (*i.e.*, write enable gates) transfers said outputs of said register output selecting means (*i.e.*, REG gates), simultaneously and in parallel to internal buses (*i.e.*, RWD0 and RWD1) in

synchronism with the edge of said reference signal (*i.e.*, clock signal). Where the reference signal is the same reference signal by which said external data finally supplied to said shift register circuit (*i.e.*, Iwama's cascade connected registers) is latched in said shift register circuit.

To the extent that "buffer output control means" is governed by 35 U.S.C. §112 ¶ 6, Watanabe's write enable gates perform the same function, in the same way, to provide the same result. For comparison, the 504 Patent's buffer output control means is depicted below – 54 OCNT:

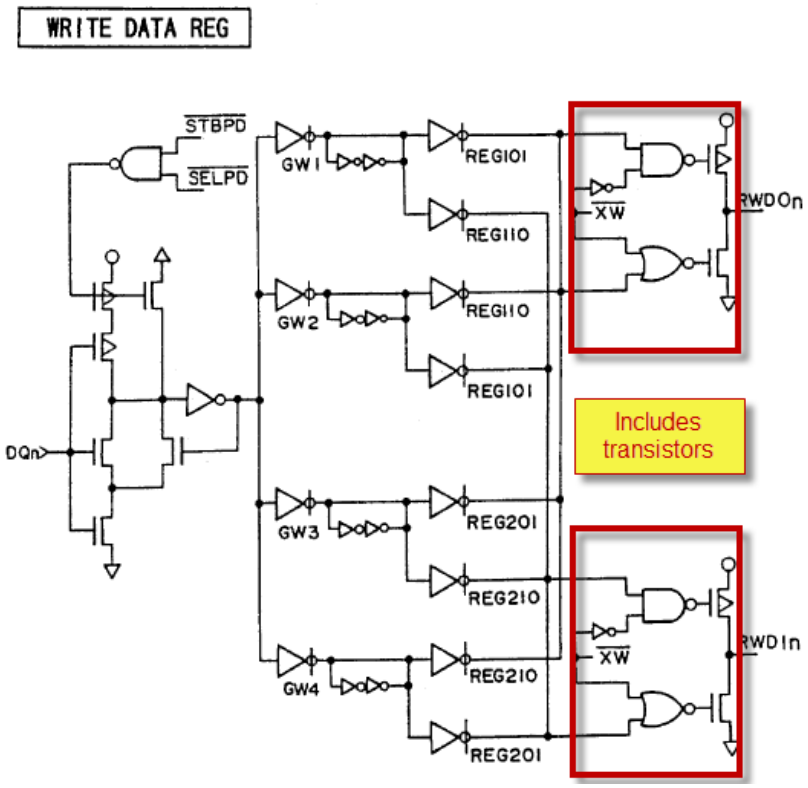


MICRON-1001, 504 Patent at Figure 5 (annotated).

Output controller 54 includes transfer gate transistors Q5 and Q6. MICRON-1001, 504 Patent at 10:18-34 ("output controller 54 includes a transfer gate transistor Q5 having one end connected to the line L3, another transfer gate transistor Q6 having

one end connected to the line L4, a latch 542 having an input connected to the other end of the transfer gate transistor Q5 and an output connected to the internal data bus IOBUS(E), and another latch 544 having an input connected to the other end of the transfer gate transistor Q6 and an output connected to the internal data bus IOBUS(O). The transfer gate transistors Q5 and Q6 are controlled in common by the data-in buffer output control signal IOW. Thus, under control of the data-in buffer output control signal IOW, the output controller 54 outputs the parallel two bits of data distributed and outputted from the register output selector 52, to the internal data bus IOBUS(E) and IOBUS(O), simultaneously and in parallel, respectively.”). Thus, the corresponding structure is a plurality of transfer gate transistors responsive to buffer output control signal (*e.g.*, IOW) or equivalents thereof.

The write enable gates have the same or equivalent structure. Specifically, the write enable gates include a plurality of transistors a control signal (*i.e.*, $\overline{XW}$). Indeed the signal $\overline{XW}$ is necessary to keep the distribution of data in synchronism with the CLK.



MICRON-1005, Watanabe at Figure 28 (annotated).

Moreover, the write enable gates serve the same function as the selector output controller 54. Namely, the write enable gates transfer the outputs of the register output selecting means (*i.e.*, REG gates in Watanabe at Figure 28, above), simultaneously and in parallel, to said plurality of internal data buses, in synchronism with an edge of said reference clock signal (*i.e.*, CLK). *See* above. The reference clock signal is the same reference clock signal used to latch the data in the cascade-connected registers of Iwama. MICRON-1006, Iwama at (0012)-(0013). This is the same or equivalent to the 504 Patent's IOW signal.

The write enable gates also achieve the same result as the register output selecting means. Namely, the write enable gates release the data simultaneously

and in parallel for storage. MICRON-1005, Watanabe at 11:29-32 ("In contrast with this, in the write mode, it is necessary that the write-mode register interleaves the register group two bits by two bits to transfer data from the registers to the RWD lines for each two cycles."), *see also id.* at 19:7-9; 19:17-24.

Note that the data is ultimately sent to the DQ buffers (latches) so the corresponding structure of Watanabe also includes latches for transferring data from the output selection means to the internal buses. *See id.* at Fig. 2 (RWD lines feeding to DQ buffers).

In sum, Watanabe in view of Iwama discloses an input buffer that includes a buffer output control means (*i.e.*, write enable gates) for transferring the outputs of the register output selecting means (*i.e.*, REG gates), simultaneously and in parallel, to the plurality of internal data buses (*i.e.*, RWD0 and RWD1), in synchronism with an edge of the reference clock signal (*i.e.*, CLK) by which the external data signal finally supplied to the shift register circuit is latched in said shift register circuit (*i.e.*, cascaded-connected shift registers). Watanabe's buffer output control means is the write enable gates, which are depicted in Watanabe in Figure 28. Moreover, Watanabe discloses the same (or at least equivalent) structure, performing the identical function, to achieve the same result. The write enable gates receive the parallel data from the WRITE REG circuit and transfers the data, simultaneously and in parallel, to the core memory. Moreover, Watanabe

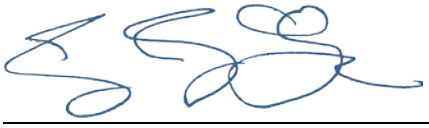
in view of Iwama discloses write enable gates that perform the identical function in the same or equivalent way to achieve the same result.

10. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1 and 2 of the 504 Patent is requested.

Respectfully submitted,

Dated: October 26, 2015

By: 

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	October 27, 2015
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 5,805,504 with Micron's Exhibit List Power of Attorney Exhibits MICRON-1001 through MICRON-1007
Persons served	Patent Owner's Address of Record: Young & Thompson 209 Madison Street Suite 500 Alexandria VA 22314 Additional Address Known as Likely to Effect Service: Jon A. Birmingham Fitch Even Tabin & Flannery LLP 21700 Oxnard Street Suite 1740 Woodland Hills, CA 91367

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