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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

ELBRUS INTERNATIONAL LIMITED
Patent Owner

U.S. Patent No. 6,366,130

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,366,130

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review of claims 1-3, 5-7, and 9 of U.S. Patent No. 6,366,130 ("the '130 Patent") (Ex. 1001), which Petitioner understands is assigned to Elbrus International Limited ("Patent Owner").[1] This Petition shows that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims, and thus a trial should be instituted. This Petition also establishes by a preponderance of the evidence that the challenged claims are unpatentable under 35 U.S.C. § 103. These claims should be canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Party-in-Interest: Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner identifies Samsung Electronics Co., Ltd. as the real party-in-interest.

Related Matters: In accordance with 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matters. Patent Owner asserted the '130 Patent against Petitioner in a patent litigation filed on July 24, 2014, in the Northern District of Illinois (case no. 1:14-cv-05691), which remains pending. Patent Owner also asserted the '130 Patent against Hynix Semiconductor, Inc. and SK Hynix Inc.

[1] Petitioner understands that the '130 Patent is exclusively licensed to Cascades Computer Innovation, LLC.

on June 27, 2011 in the Northern District of Illinois (case no. 1-11:cv-04356), but this case was dismissed on February 6, 2014. Hynix Semiconductor Inc. sought *inter partes* reexamination (control no. 95/000,657) on January 19, 2012, but that proceeding resulted in a reexamination certificate that issued on August 4, 2014.

Petitioner is concurrently filing a second petition for *inter partes* review also challenging claims 1-3, 5-7, and 9.

Counsel and Service Information: Lead counsel is Steven L. Park (Reg. No. 47,842), Paul Hastings LLP, 1170 Peachtree Street, NE, Suite 100, Atlanta, GA 30309, Telephone: (404) 815-2223, Fax: (404) 685-2223, E-mail: stevenpark@paulhastings.com. Back-up counsel is Naveen Modi (Reg. No. 46,224), Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Telephone: 202.551.1700, Fax: 202.551.1705, E-mail: naveenmodi@paulhastings.com. Petitioner consents to electronic service

III. PAYMENT OF FEES UNDER 37 C.F.R. §§ 42.15 AND 42.103

Petitioner submits the required fees with this petition. Please charge any additional fees required for this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING AND IDENTIFICATION OF CHALLENGE

Petitioner certifies that the ’130 Patent is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting such review of the ’130 Patent on the grounds identified below.

Petitioner challenges claims 1-3, 5-7, and 9 of the '130 Patent and requests that these claims be found unpatentable and canceled in view of the following prior art references: U.S. Patent No. 5,828,241 to Sukegawa ("*Sukegawa*") (Ex. 1005); U.S. Patent No. 6,108,254 to Watanabe et al. ("*Watanabe*") (Ex. 1006); U.S. Patent No. 6,249,469 to Hardee ("*Hardee*") (Ex. 1007); and "Half-V_{DD} Bit-Line Sensing Scheme in CMOS DRAM's," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 4 by Nicky Chau-Chun Lu et al. ("*Lu*") (Ex. 1008).

The '130 Patent attempts to claim priority to provisional application no. 60/120,531 ("the '531 provisional application"), filed February 17, 1999. For purposes of this proceeding, Petitioner has assumed that the '130 Patent is entitled to the February 17, 1999 date.[2] *Lu* was published more than one year before this date and is therefore prior art under pre-AIA 35 U.S.C. § 102(b). *Sukegawa* issued on October 27, 1998 and is thus prior art under pre-AIA 35 U.S.C. § 102(a). *Watanabe* and *Hardee* were both filed prior to February 17, 1999 and issued after that date, and are therefore prior art under pre-AIA 35 U.S.C. § 102(e).

Petitioner requests cancellation of the challenged claims on the following

[2] Petitioner does not concede that the '130 Patent claims comply with 35 U.S.C. § 112 or that they are entitled to the assumed priority date. Petitioner reserves the right to raise these and other issues in a district court or another forum.

grounds:

Ground 1: Claims 1-2, 5-6, and 9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over *Sukegawa* in view of *Lu*.

Ground 2: Claim 3 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over *Sukegawa* in view of *Lu* and *Watanabe*.

Ground 3: Claim 7 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over *Sukegawa* in view of *Lu* and *Hardee*.

V. BACKGROUND

The ’130 Patent issued from U.S. Patent Application No. 09/505,656 (“the ’656 application”), filed February 17, 2000, and attempts to claim priority to the ’531 provisional application. Ex. 1001 Title Page.

A. The ’130 Patent

The ’130 Patent is purportedly directed to a data transfer scheme that includes two bus drivers, a precharge circuit, two complementary bus lines, and a latching sense amplifier. Ex. 1001 2:1-8; Ex. 1002, ¶ 17. Fig. 1 of the ’130 Patent illustrates two bus drivers 11, 12 (consisting of transistors 20, 21, 22, and 23) and two complementary bus lines 14, 15 as inputs to a latching sense amplifier 16:

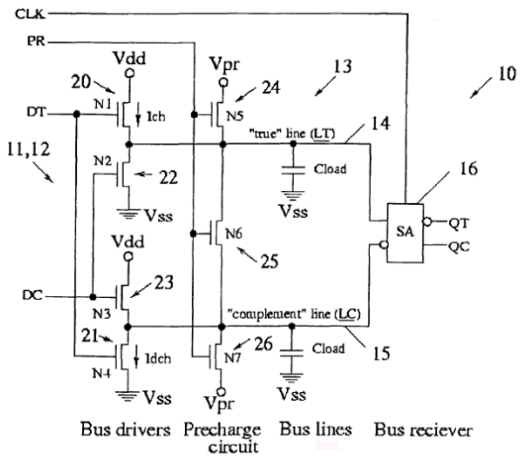

FIG.1.

See also, *e.g.*, Ex. 1002, ¶ 17. According to the patent, the data transfer scheme operates in two phases: a precharge phase and a data transfer phase (Ex. 1001 2:12-13; Ex. 1002, ¶ 18), with the bus drivers and complementary bus lines operating in opposite phases to the latching sense amplifier (Ex. 1001 2:43-44; Ex. 1002, ¶ 18). In other words, when the complementary bus lines and the bus drivers are in the precharge phase, the sense amplifier is in data transfer phase and vice versa. Ex. 1002, ¶ 18.

The ’130 Patent includes 9 claims with claims 1 and 8 being independent and claims 2-7 and 9 being dependent from claim 1. Claim 9 was added during reexamination. Independent claim 1 is reproduced below:

1. A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge

source; aid [sic]

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage;

wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor.

B. Prosecution History of the ’130 Patent

During prosecution, all claims of the ’656 application that eventually issued as the ’130 Patent were initially rejected as unpatentable over prior art. Ex. 1003, pp. 43-44. In response, claim 1 of the application was amended to clarify that the “latching sense amplifier” comprises of a “first stage including a cross-coupled latch coupled to a differential data bus” and an “output stage” coupled to the output of the “first stage.” *Id.*, p. 53. Applicants explained that the latching sense amplifier disclosed by the prior art did not include two stages, whereas amended claim 1 now included both a “first stage” and an “output stage” of a latching sense

amplifier. *Id.*, p. 50-51. Applicants also distinguished the purported invention over the cited prior art by noting the purported invention "teaches precharging the buses to a specific level *between ground and Vdd* (Vpr = K*Vdd, where K is precharging voltage factor)," rather than Vdd as taught by the prior art. *Id.*, p. 50 (emphasis added). Applicants later submitted a supplemental amendment to claim 1 to recite the intermediate precharge voltage Vpr (*id.*, p. 60-62), and a notice of allowance was issued shortly thereafter (*id.*, pp. 64-68).

C. Reexamination History of the '130 Patent

As noted above, Hynix filed an *inter partes* reexamination, i.e., control no. 95/000,657 ("the '657 proceeding"). *See* Ex. 1004 (excerpts from the '657 proceeding). During *inter partes* reexamination, claims 1-3 and 5-7 were confirmed. Patent Owner also submitted new claims, but all but one were rejected under 35 U.S.C. § 112. *Id.*, pp. 134-44. This one claim eventually issued as claim 9. Ex. 1001 Reexam Cert. 1:20-21.

D. Prior Art Raised in This Petition

This Petition relies on prior art that the U.S. Patent and Trademark Office ("PTO") did not have before it or did not fully consider during prosecution and reexamination. In fact, with the exception of *Watanabe*, none of the other prior art

references were cited during prosecution or reexamination.[3] As for *Watanabe*, it was cited in an Information Disclosure Statement during reexamination but was never discussed or relied on in any rejection. As explained below, the prior art discussed in this Petition renders obvious the claims of the '130 Patent, especially when considered in light of the declaration of Dr. R. Jacob Baker (Ex. 1002).

VI. CLAIM CONSTRUCTION

In an *inter partes* review, the Board applies the broadest reasonable interpretation ("BRI") standard to construe claim terms.[4] Under the BRI standard, claim terms are given their "broadest reasonable interpretation, consistent with the specification." *In re Yamamoto*, 740 F.2d 1569, 1571 (Fed. Cir. 1984); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,764 (Aug. 14, 2012). Claim terms are also "generally given their ordinary and customary meaning," which is

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[3] Hynix relied on European patent publication no. EP 0 597 231 during reexamination. This European publication is related to *Hardee*. *Hardee* was, however, never considered as presented herein, especially in light of the accompanying expert testimony.

[4] Petitioner notes that the district courts apply a different claim construction standard and reserves its rights to make arguments based on that standard in the district court.

the meaning that the term would have to a person of ordinary skill in the art.[5] *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312, 1313 (Fed. Cir. 2005) (*en banc*)). Petitioner proposes a construction for a few of the claim terms below and submits that the remaining terms in the '130 Patent should be given their plain and ordinary meaning under the BRI standard.

A. Latching Sense Amplifier (Claims 1, 3)

Claims 1 and 3 recite the term "latching sense amplifier." For purposes of this proceeding, "latching sense amplifier" should be construed to mean "a circuit, including a latch, that detects and amplifies signals." This construction is consistent with the use of the term in the claims and specification of the '130 Patent. Ex. 1002, ¶ 22.

Neither the claims nor the specification explicitly define "latching sense amplifier." The '130 Patent's specification describes its latching sense amplifier to include a latch (*see, e.g.*, Ex. 1001 2:39-40, 2:48-50) for detecting (*see, e.g.*, Ex.

[5] A person of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have had an undergraduate degree in Electrical Engineering or equivalent and at least two to three years of experience in the design and/or analysis of data transfer circuits or the equivalent. Ex. 1002, ¶ 15.

1001 2:33-38, 2:64-67) and amplifying received signals (*see, e.g.*, Ex. 1001 2:64-67). *See also* Ex. 1002, ¶ 22. Also, latching sense amplifiers were well known at the time of the alleged invention of the ’130 Patent by those skilled in the art, and such individuals would have understood the term to be consistent with the Petitioner’s proposed construction. Ex. 1002, ¶ 22. Indeed, Petitioner’s construction is consistent with dictionary definitions of similar terms. *See, e.g.*, Ex. 1009 at 679 (defining “sense amplifier” as “[a] circuit used to sense low-level voltages ... and to amplify these signals to the logic voltage levels of the system”); *see also* Ex. 1002, ¶ 22.

The claims additionally specify what a “latching sense amplifier” has to include. Ex. 1002, ¶ 22. For example, claim 1 requires that the “latching sense amplifier” include both a first stage with a cross-coupled latch and an output stage. *See, e.g.*, Ex. 1001 4:8-13; Ex. 1002, ¶ 22. Accordingly, in the context of the ’130 Patent, the broadest reasonable interpretation of “latching sense amplifier” is “a circuit, including a latch, that detects and amplifies signals,” wherein the claims further define what that circuit includes. Ex. 1002, ¶ 22.

B. Stage (Claims 1, 3, 9)

Claims 1, 3, and 9 recite the term “stage.” For purposes of this proceeding, “stage” should be construed to mean “portion of a circuit.” This construction is consistent with the use of the term in the claims and specification of the ’130

Patent as well as dictionary definitions for the term. Ex. 1002, ¶ 23.

Neither the claims nor the specification explicitly define "stage." However, independent claim 1 uses the term to indicate that a latching sense amplifier comprises of a "first stage" and an "output stage" and dependent claims 3 and 9 use the terms in context of particular circuitry found within a "first stage" and "output stage" of a latching sense amplifier. *See, e.g.*, Ex.1001 4:8-13, 4:21-23, Reexam Cert. at 1:20-21; Ex. 1002, ¶ 23. Claim 1 notes that the "first stage" of the latching sense amplifier must include cross-coupled latch circuitry. *See, e.g.*, Ex. 1001 4:8-13; Ex. 1002, ¶ 23. In claim 3, the "first stage" is described to include specific transistor circuitry and clock signals. *See, e.g.*, Ex. 1001 4:8-13; Ex. 1002, ¶ 23. The "output stage" of claim 9 includes circuitry for cross-coupled feedback. *See, e.g.*, Ex. 1001 Reexam Cert. at 1:20-21; Ex. 1002, ¶ 23. The specification uses the term "stages" once (Ex. 1001 3:4-5) and that usage is consistent with the definition proposed here. Ex. 1002, ¶ 23. In addition, the Modern Dictionary of Electronics (7th ed. 1999) defines "stage" as "[a] single section of a multisection circuit or device." Ex. 1009 at 728. Accordingly, in the context of the '130 Patent, the broadest reasonable interpretation of "stage" is "portion of a circuit."

VII. DETAILED EXPLANATION OF UNPATENTABILITY

A. Brief Description of the Prior Art

As explained in detail below, the prior art identified and applied in this

Petition discloses and/or suggests the limitations of claims 1-3, 5-7, and 9. Ex. 1002, ¶¶ 16, 24, 30-43. For example, *Sukegawa* describes "a type of signal transmission circuit wherein the signal is amplified and transmitted by means of the positive feedback of an intermediate amplifier circuit having input/output shared terminals." *Sukegawa* 1:11-15; *see also, e.g.*, Ex. 1002, ¶ 25. The signal transmission circuit disclosed sought to increase the signal transmission distance as well as increase the speed and lower the power consumption of a transmission. *Sukegawa* 4:52-55; *see also, e.g.*, Ex. 1002, ¶ 25. *Sukegawa* discloses that its signal transmission circuit comprises of "a driver circuit, a receiver circuit, an equalizer circuit, and an intermediate amplifier circuit." *Sukegawa* 4:62-65; *see also, e.g.*, Ex. 1002, ¶ 25. The intermediate amplifier circuit relies on positive feedback to amplify the signal provided by the driver circuit and transmit the amplified signal to the receiver circuit. *See, e.g.*, *Sukegawa* 5:1-4; *see also, e.g.*, Ex. 1002, ¶ 25.

Lu also describes a signal transmission system, and in particular, a sense amplifier utilized by DRAMs (Dynamic Random Access Memory). *See, e.g.*, *Lu* Abstract; Ex. 1002, ¶ 26. *Lu* introduces "a sensing scheme for CMOS DRAM's [sic] in which the bit line is precharge to half-V_{DD}." *Lu* 451; Ex. 1002, ¶ 26. Similar to *Sukegawa*, *Lu* discloses the need to develop signal transmission systems faster in speed and lower in power consumption. *See, e.g.*, *Lu* 453-54; Ex. 1002, ¶ 26.

Watanabe additionally relates to the transmission of signals in electronic

circuits. *See, e.g.*, *Watanabe* Abstract, 1:10-13; Ex. 1002, ¶ 27. Specifically, *Watanabe* introduces a "data transfer circuit incorporated in a DRAM." *Watanabe* 3:38-39; Ex. 1002, ¶ 27. "[T]he data transfer circuit comprises a differential amplifier circuit 10, an equalizing circuit 11, a data latch circuit 12, a pair of first data lines 13, a pair of second data lines 14, and a pair of data output lines 15." *Watanabe* 3:41-44; *see also, e.g.*, *id.* Fig. 1; Ex. 1002, ¶ 27. Like *Sukegawa* and *Lu*, the circuit disclosed by *Watanabe* was motivated by a need to increase the transmission speed of signals in electronic circuits. *See, e.g.*, *Watanabe.* 2:52-56 ("No time is therefore required to equalize either data lines, unlike in the conventional data transfer scheme. Hence, data can be transferred at high speed in DRAM according to the present invention."); Ex. 1002, ¶ 27.

Hardee is yet another prior art reference relating to signal transmission, and in particular, "integrated circuit memories" and "sense amplifiers for use therein." *See, e.g.*, *Hardee* 1:8-10; Ex. 1002, ¶ 28. *Hardee* introduces a sense amplifier highlighted by three "salient" features:

> (1) the connection of each sense amplifier via transistors or other switching devices to the power supply lines without directly connecting together power supply lines for multiple sense amplifiers;
> (2) the use of local read amplifiers;
> (3) the use of local write circuitry.

See Hardee 5:24-32; *see also, e.g.*, Ex. 1002, ¶ 28.

All the prior art references mentioned above relate to signal transmission and were motivated to improve the efficiency of such transmissions. Ex. 1002, ¶ 29. As such, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to combine the teachings of these references. Ex. 1002, ¶ 29.

B. Ground 1: *Sukegawa* and *Lu* Render Claims 1, 2, 5, 6, and 9 Obvious

1. Claim 1

i. "A data transfer arrangement comprising:"

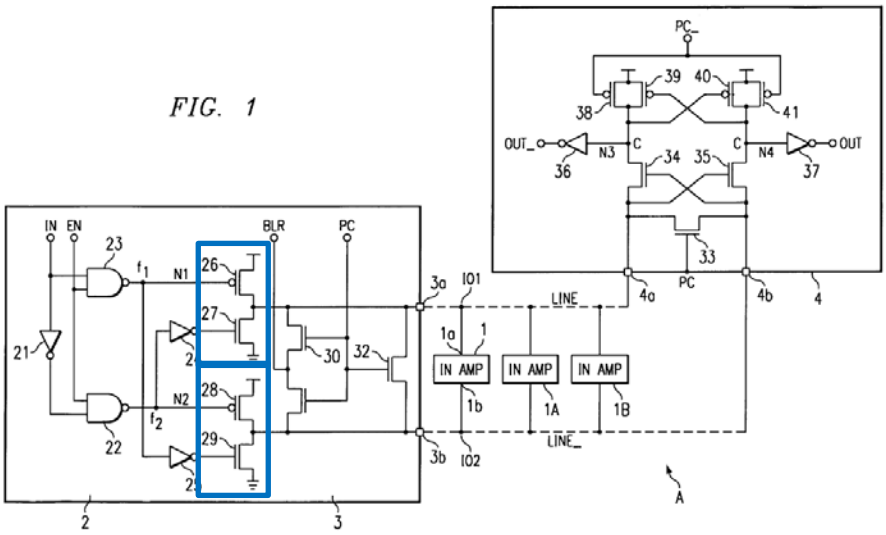
Sukegawa discloses a data transfer arrangement. *See, e.g.*, Ex. 1002, ¶ 31. For example, *Sukegawa* introduces "[a] signal transmission circuit which enables the distance of signal transmission as measured by the length of the wiring electrically connecting a driver circuit and a receiver circuit of the signal transmission circuit to be increased, while the signal delay and power consumption are reduced." *Sukegawa* Abstract; *see also, e.g., id.* 6:37-39, Fig. 1.

ii. "two bus drivers[6];"

Sukegawa discloses two bus drivers. *See, e.g.*, Ex. 1002, ¶ 31. For example,

[6] Petitioner has used color and annotated figures throughout this Petition to illustrate how the prior art discloses the various claimed features.

as demonstrated below in annotated Fig. 1 of *Sukegawa*, transistors 26-27 and transistors 28-29 serve as bus drivers for bus lines LINE and LINE_:



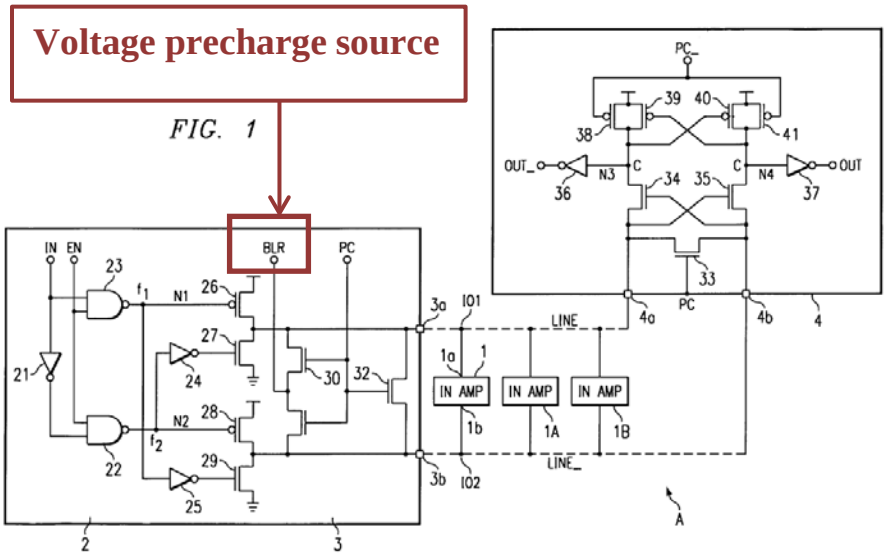
See also, e.g., Ex. 1002, ¶ 31. *Sukegawa* teaches:

> Driver circuit 2 comprises input terminal IN, enable EN terminal, NAND gates 22, 23, CMOS inverters 21, 24, 25, pMOS transistors 26, 28, and nMOS transistors 27, 29. The input terminal IN of driver circuit 2 is connected through CMOS inverter 21 to one input terminal of NAND gate 22, and the input terminal IN is also connected to one input terminal of NAND gate 23. Enable EN terminal is connected to the other input terminals of NAND gates 22, 23. In the driver circuit 2, in the initial precharge state, the enable EN terminal is at L level, while node N1 and node N2 on the output sides of NAND gates 22, 23 are at H level."

Sukegawa 8:11-23; *see also, e.g.*, *id.* 9:14-21; Ex. 1002, ¶ 31.

iii. "a voltage precharge source;"

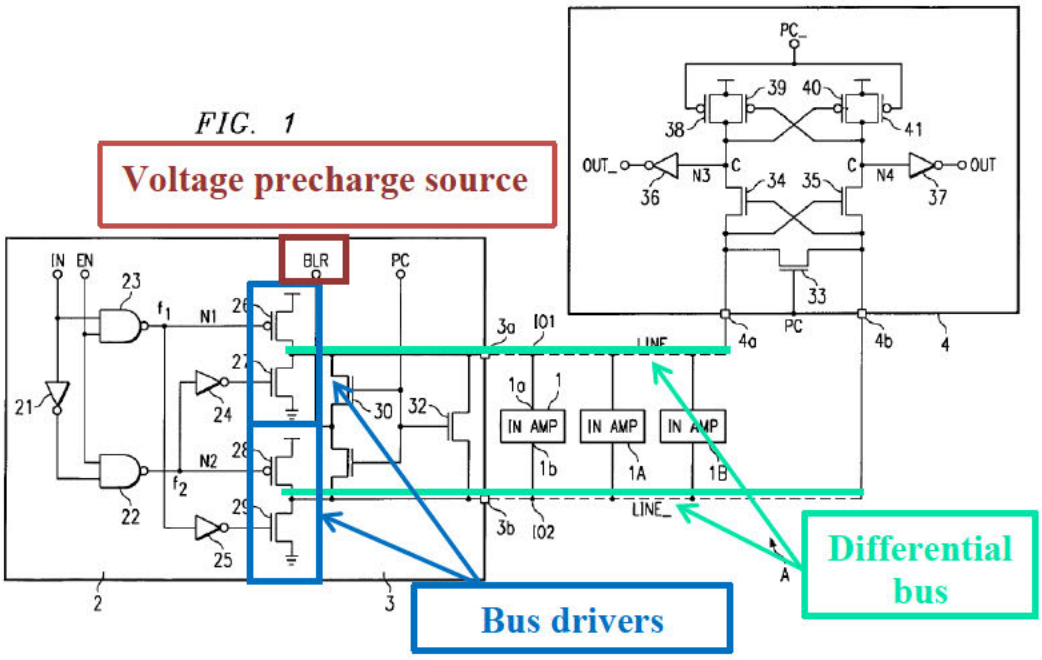
Sukegawa discloses a voltage precharge source. *See, e.g.*, Ex. 1002, ¶ 31. For example, as demonstrated below in annotated Fig. 1 of *Sukegawa*, the voltage precharge source is disclosed as BLR (*see, e.g.*, Ex. 1002, ¶ 31):



Sukegawa discloses that "BLR node becomes the power source voltage $V_{DD}/2$ in the initial *precharge* source." *Sukegawa* 8:29-31 (emphasis added), 7:29-37; Ex. 1002, ¶ 31.

iv. "a differential bus coupled to the bus drivers and to the voltage precharge source; aid [sic]"

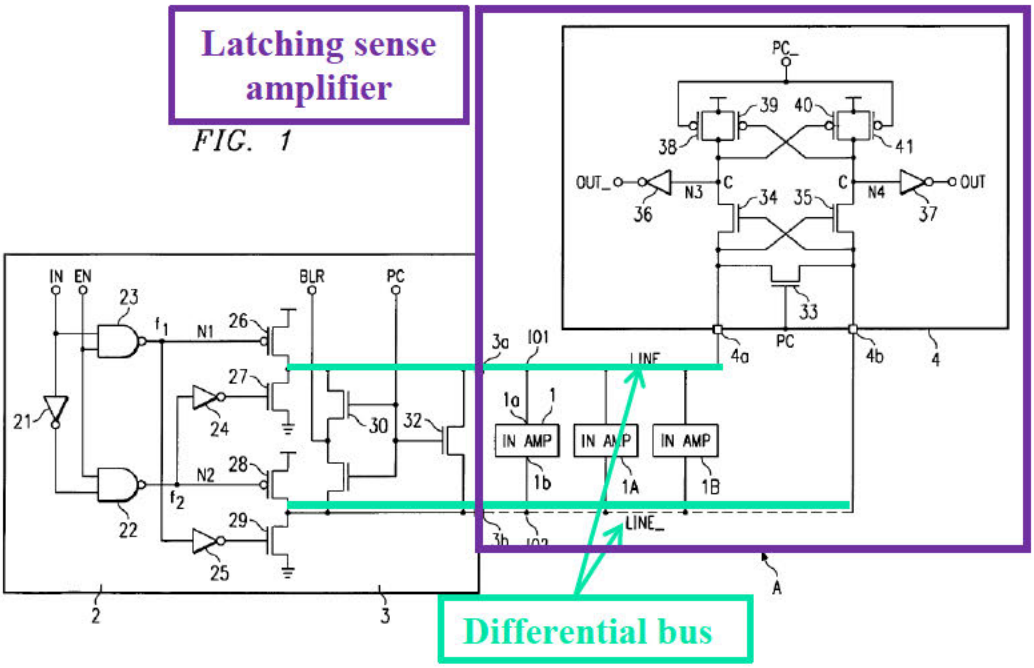
Sukegawa teaches a differential bus coupled to the bus drivers and voltage source. *See, e.g.*, Ex. 1002, ¶ 31. For example, as shown below in annotated Fig. 1 of *Sukegawa*, the differential bus LINE and LINE_ is coupled to the bus drivers (transistors 26-27 and transistors 28-29) and voltage precharge source BLR:



See also, e.g., *Sukegawa* 6:54-61; Ex. 1002, ¶ 31. One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have recognized that LINE and LINE_ constitute "the differential bus" because a voltage differential (i.e., a difference in voltages between the two bus lines) can develop on these two bus lines. *See, e.g.*, *Sukegawa* 7:38-43; Ex. 1002, ¶ 31.

v. "a latching sense amplifier coupled to the differential bus;"

Sukegawa discloses a latching sense amplifier (shown below in purple) coupled to the differential bus LINE and LINE_. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* Fig. 1 (annotated below).



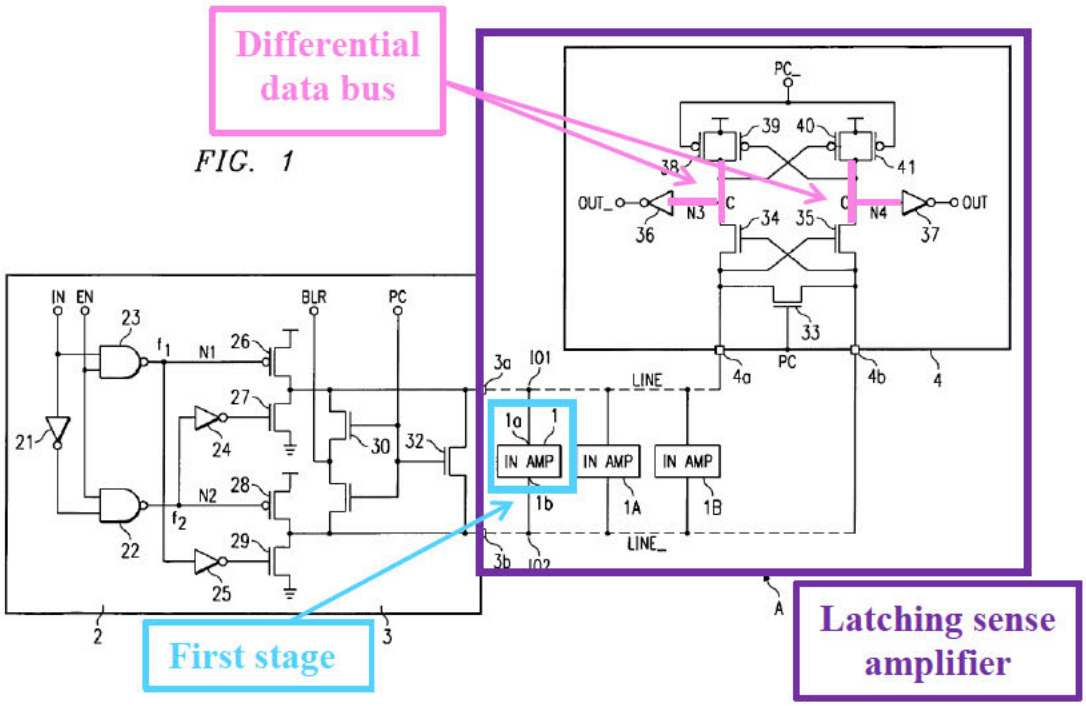
Consistent with Petitioner's proposed construction of "latching sense amplifier," the circuitry identified in above in annotated Fig. 1 of *Sukegawa* is a circuit, including a latch, that detects and amplifies signals. Ex. 1002, ¶ 31. Each intermediate amplifier 1, 1A, and 1B provides a latch that detects and amplifies the signal on LINE and LINE_. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* Fig. 2, 7:1-8:6.

Sukegawa discloses that "[a]s shown in FIG. 1, in this intermediate amplifier circuit 1, positive line LINE which connects connecting terminal 3a of equalizer circuit 3 and input terminal 4a of receiver circuit 4 is connected to input/output shared terminal 1a at node 101, and negative line N-LINE (where N- represents the negative side) which connects output terminal 3b of equalizing circuit 3 and input terminal 4b of receiver circuit 4 is connected to input/output shared terminal 1b at

node 102." *Sukegawa* 6:54-61.

vi. "wherein the latching sense amplifier comprises: a first stage including a cross-coupled latch coupled to a differential data bus; and"

Sukegawa teaches that its latching sense amplifier (shown below in purple) includes a first stage (shown below in light blue) with a cross-coupled latch coupled to a differential data bus (pink lines below). *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* Fig. 1 (annotated below).



See also, e.g., *Sukegawa* Fig. 2 (further disclosing circuitry of first stage). As indicated above, the circuitry identified as the first stage comprises of intermediate amplifier 1. Ex. 1002, ¶ 31. Consistent with Petitioner's proposal that "stage" be construed to mean "portion of a circuit," the elements identified as the "first stage"

are a portion of the latching sense amplifier circuit. Ex. 1002, ¶ 31. In particular, intermediate amplifier 1 latches and amplifies voltages received through nodes 1a and 1b, and outputs the amplified voltages through the same nodes. *See, e.g.*, *Sukegawa* 7:1-8:6; Ex. 1002, ¶ 31.

Sukegawa teaches that the first stage includes a cross-coupled latch consisting of transistors 10, 11, 14, and 15. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* Fig. 2 (annotated below).

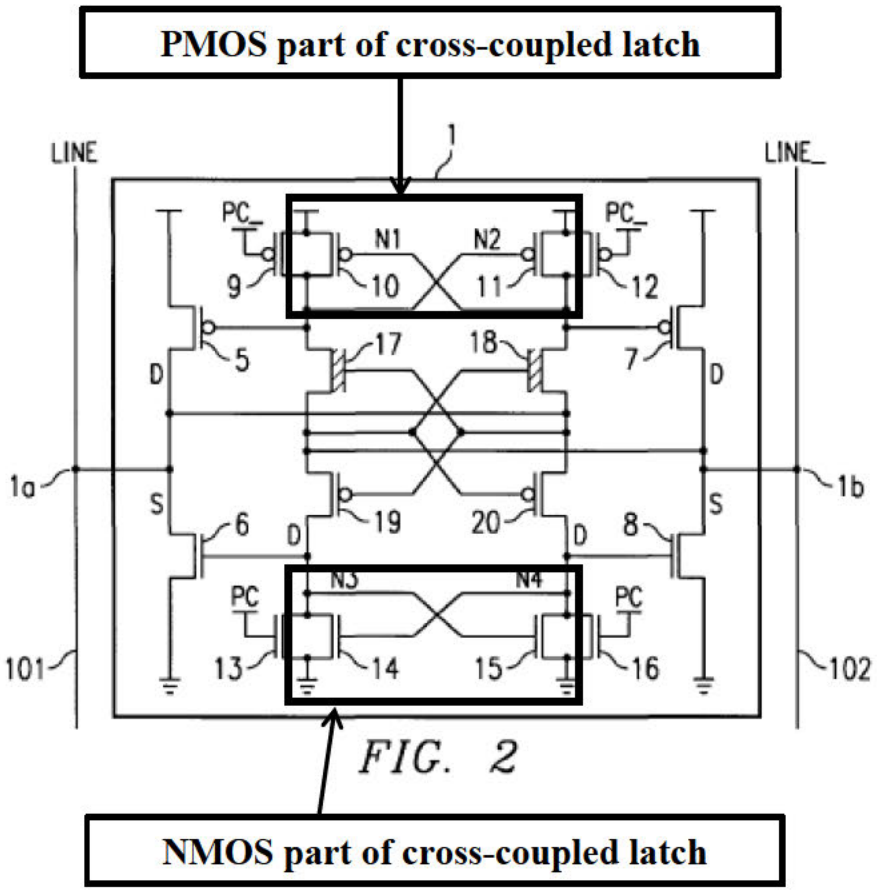
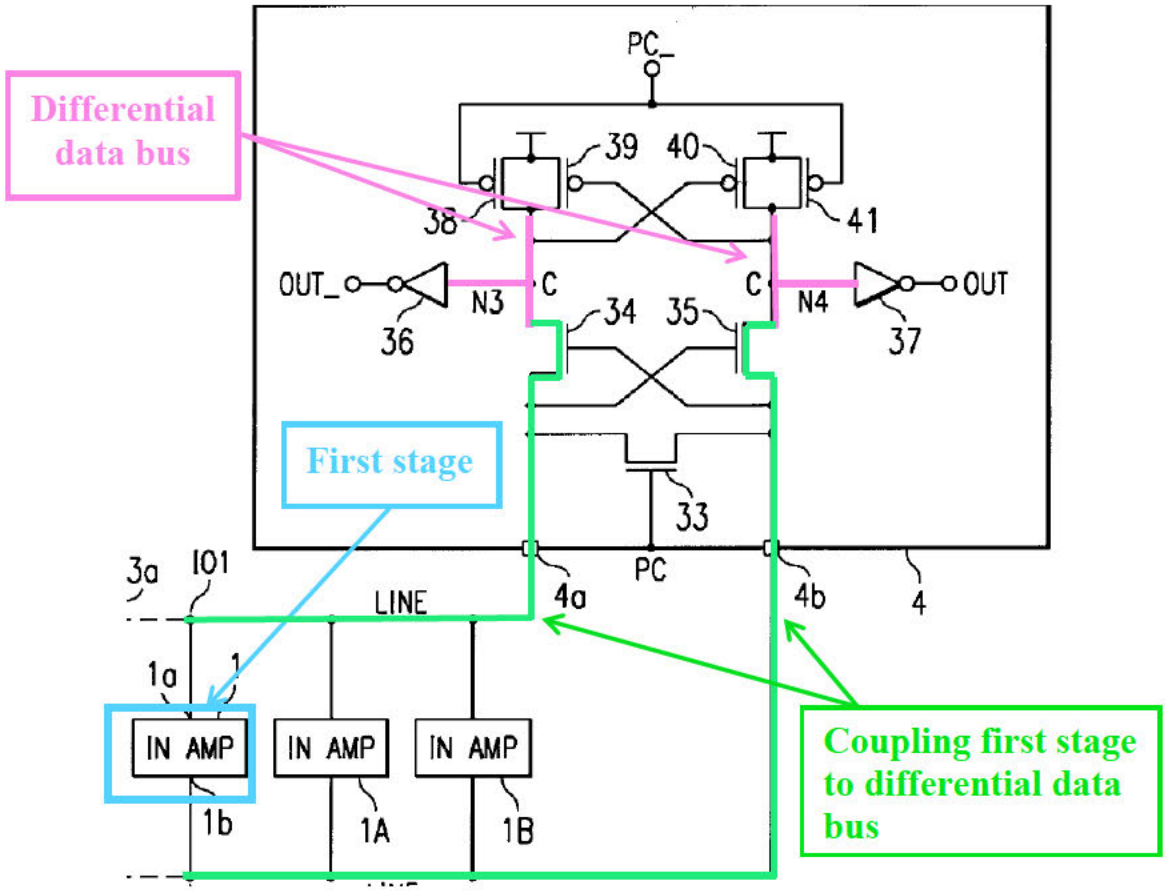


FIG. 2

One of ordinary skill in the art at the time of the alleged invention of the '130

Patent would have recognized, based on the disclosure of *Sukegawa*, that the cross-coupled latch comprises of transistors 10, 11, 14, and 15 because these transistors act to regenerate full logic levels (both high and low) on LINE and LINE_. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* 9:14-21. Moreover, these transistors are cross-coupled because the output of a first transistor (e.g., 10) is tied to the input of a second transistor (e.g., 11), and the output of the second transistor (e.g., 11) is tied to the input of the first transistor (e.g., 10). *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* Fig. 2. Similarly, the output of transistor 14 is tied to the input of transistor 15, and vice versa. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* Fig. 2.

The first stage of *Sukegawa* is also coupled to the differential data bus via LINE, LINE_ and transistors 34, 35. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* 6:54-61, Fig. 1 (annotated below).



One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have recognized lines associated with nodes C (shown above in pink) as the "differential data bus" because the pink highlighted lines represent an amplified voltage differential representative of the data to be read out by the latching sense amplifier. *See, e.g.*, *Sukegawa* 9:14-24; Ex. 1002, ¶ 31. Indeed, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood the pink highlighted lines to include differential data because of the amplified voltage differential on these lines. Ex. 1002, ¶ 31. Moreover, Fig. 5 of *Sukegawa* teaches one intermediate amplifier (i.e., first stage)

prior to the receiver circuit 4 (as discussed below, the receiver circuit is *Sukegawa*'s "output stage"), and thus the first stage and the differential data bus can be coupled without additional intermediate amplifiers (*see, e.g.*, Ex. 1002, ¶ 31):

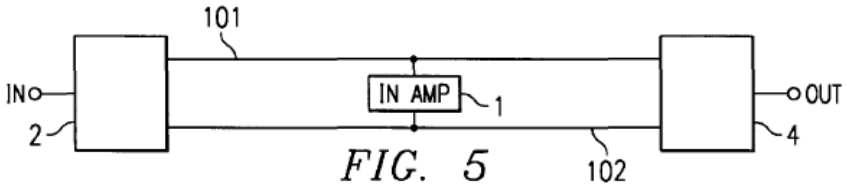
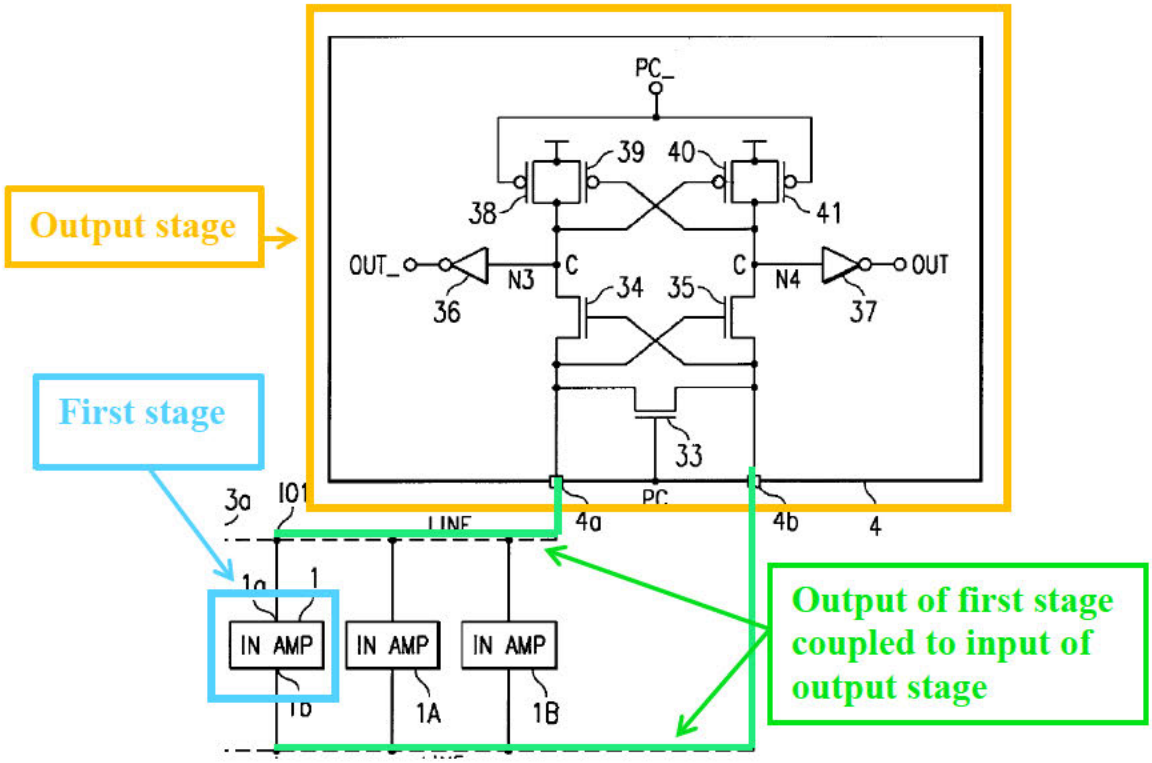


FIG. 5

vii. "an output stage coupled to an output of said first stage; wherein the output of the first stage is coupled to an input of the output stage;"

Sukegawa teaches a latching sense amplifier with an output stage (shown below in orange) coupled to an output of its first stage (shown below in light blue), and wherein the output of the first stage is coupled to an input of the output stage. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* Fig. 1 (annotated below).



As indicated above, the circuitry identified as the output stage comprises of receiver circuit 4. *See, e.g.*, Ex. 1002, ¶ 31; *Sukegawa* 8:50-9:24. Consistent with Petitioner's proposal that "stage" be construed to mean "portion of a circuit," the elements identified as the "output stage" are a portion of the latching sense amplifier circuit. Ex. 1002, ¶ 31. In particular, receiver circuit 4 receives and drives the output of an amplified voltage differential amplified by *Sukegawa*'s intermediate amplifier(s). Ex. 1002, ¶ 31; *Sukegawa* 8:50-9:24.

Sukegawa further discloses:

> A shown in FIG. 1, in this intermediate amplifier circuit 1, *positive line LINE which connects connecting terminal 3a of equalizer circuit 3 and input terminal 4a of receiver circuit 4* is connected to input/output shared terminal 1a

> at node 101, *and inverted line N-LINE (where N- represents the negative side) which connects output terminal 3b of equalizer circuit 3 and input terminal 4b of receiver circuit 4* is connected to input/output shared terminal 1b at node 102.

Sukegawa 6:54-61 (emphasis added).

viii. "wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor."

Sukegawa discloses the differential bus is precharged to an intermediate voltage Vdd/2, i.e., a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor. *See, e.g.*, Ex. 1002, ¶ 31. For example, *Sukegawa* explains:

> When intermediate amplifier circuit 1 is in the initial precharge state, pMOS transistors 5, 7 and nMOS transistors 6, 8 are all in OFF (nonconductive) state. In this case, *the voltage at nodes 101 and 102 becomes the intermediate voltage VDD/2*; gate node N1 of pMOS transistor 10 and gate node N2 of pMOS transistor 11 become the high level (referred to as 'H level' hereinafter); and gate node N3 of nMOS transistor 15 and gate node N4 of nMOS transistor 14 become the low level (referred to as 'L level' hereinafter). This is because, in the initial precharge state, the PC terminal

> becomes the H level, while the N-PC terminal becomes the L level.

Sukegawa 7:26-37 (emphasis added); *see also, e.g., id.* Figs. 1 (identifying nodes 101 and 102), 2 (same); Ex. 1002, ¶ 31. Further, "[t]he BLR node is connected to the drain of the nMOS transistor 30 and the drain of nMOS transistor 31, and the BLR node becomes the power source voltage VDD/2 in the initial precharge state." *Sukegawa* 8:28-31; *see also, e.g., id.* 9:14-21; Ex. 1002, ¶ 31.

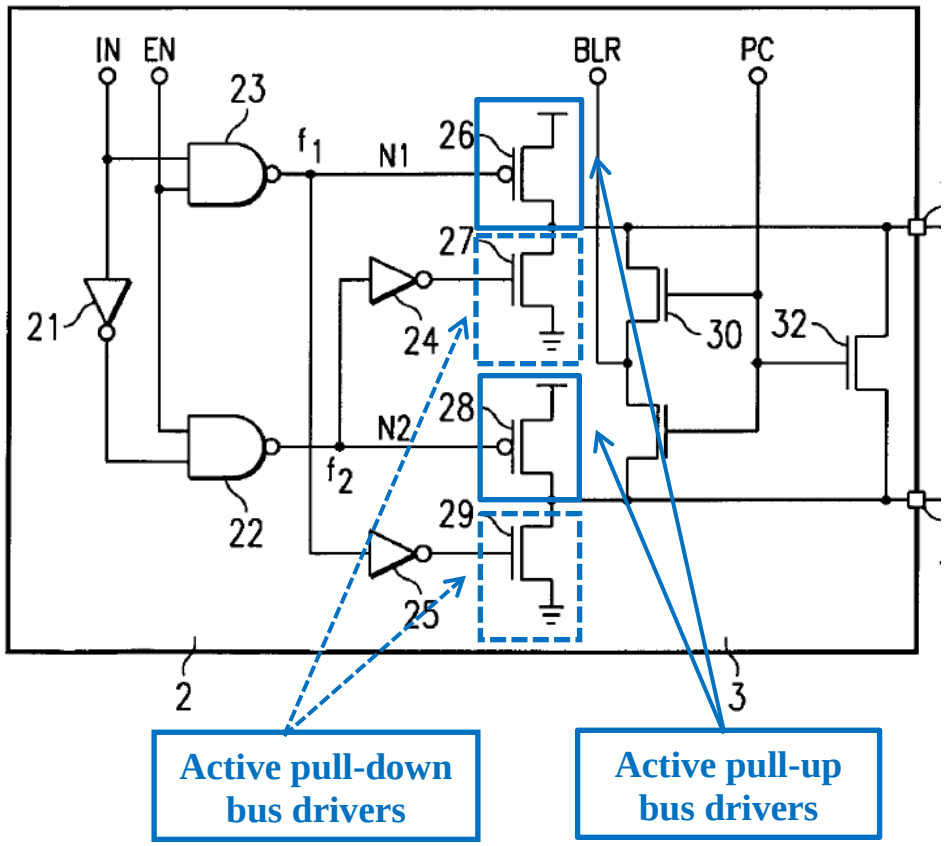
Further, *Sukegawa* discloses that the differential data bus is precharged to a voltage Vdd. *See, e.g., Sukegawa* 9:4-7. But one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have modified *Sukegawa* so that the differential data bus is precharged to an intermediate voltage Vdd/2 rather than Vdd. *See, e.g.*, Ex. 1002, ¶ 31. One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that precharging to an intermediate voltage would have been desirable to speed up operation of the circuit because pulling up or pulling down a node precharged to an intermediate voltage to full logic levels would require a smaller voltage swing (and thus be faster) versus a full Vdd voltage swing to pull down a node precharged to Vdd (as disclosed in *Sukegawa* with respect to the differential data bus). *See, e.g.*, Ex. 1002, ¶ 31. For example, pulling up or down a node precharged to Vdd/2 would merely require half the voltage change when compared to pulling down a node precharged to Vdd. Ex. 1002, ¶ 31. This reasoning is disclosed by, for example,

Lu: "At sensing and bit-line precharge in half-V_{DD} sensing, the pullup and pulldown of bitlines are balanced and have only half-V_{DD} swing." *Lu* 453. As discussed above, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to apply the teachings of *Lu* to *Sukegawa* given their overlapping subject matter and the apparent benefit of precharging to Vdd/2. *See supra* Section VII.A; *see also, e.g.*, Ex. 1002, ¶ 31. Indeed, such a skilled person would have recognized based on the disclosures of *Sukegawa* and *Lu*, that doing so would have amounted to nothing more than the use of a known technique to improve similar devices in the same way and would have yielded nothing more than predictable results. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

2. Claim 2

i. "The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers."

Sukegawa discloses that its bus drivers (transistors 26-27 and transistors 28-29) comprise of active pull-up and pull-down bus drivers. *See, e.g.*, Ex. 1002, ¶ 32; *Sukegawa* 8:11-23, Fig. 1 (annotated below).



Sukegawa teaches that the bus drivers comprise of active pull-up drivers because PMOS transistors 26 and 28 may couple LINE or LINE_ to Vdd (indicated by the flat line to the top of transistors 26 and 28) and thus pull up the output. *See, e.g.*, *Sukegawa* Fig. 1, 9:14-21; Ex. 1002, ¶ 32. Likewise, *Sukegawa* teaches that the bus drivers comprise of active pull-down drivers as NMOS transistors 27 and 29 may couple LINE or LINE_ to ground (indicated by the dashed lines in the shape of a triangle to the bottom of transistors 27 and 29) and thus pull down the outputs. *See, e.g.*, *Sukegawa* Fig. 1, 9:14-21; Ex. 1002, ¶ 32.

3. Claim 5

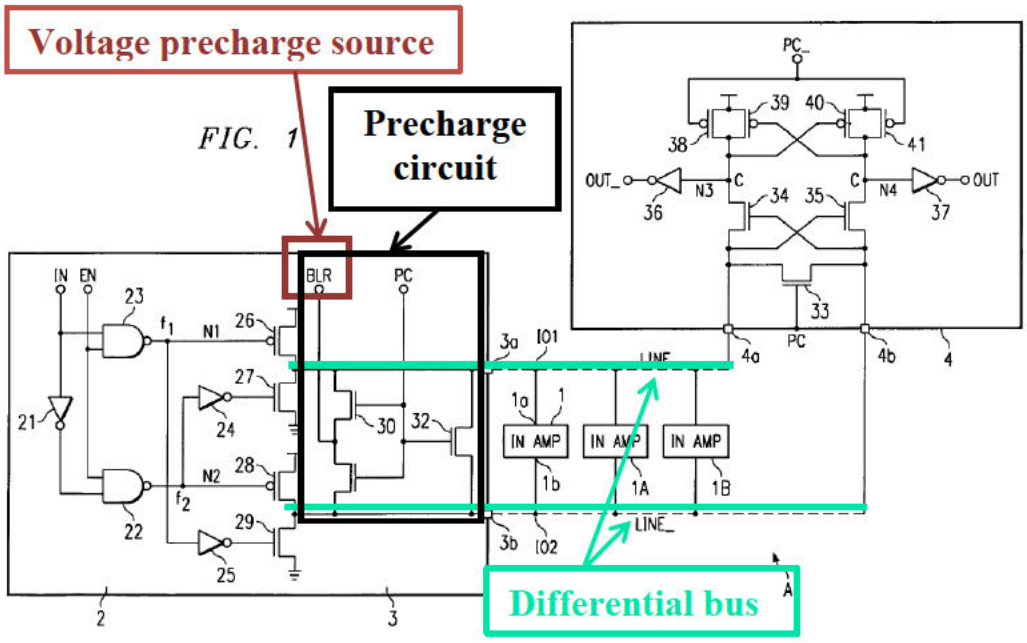
i. "The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage."

Sukegawa teaches that the differential bus LINE and LINE_ get precharged to a voltage less than a logic high and greater than a logic low as the bus lines are precharged to an intermediate voltage source Vdd/2 provided by BLR (i.e., the voltage precharge source). *See, e.g., Sukegawa* 7:26-37, 8:28-31, 9:14-21; Ex. 1002, ¶ 33.

4. Claim 6

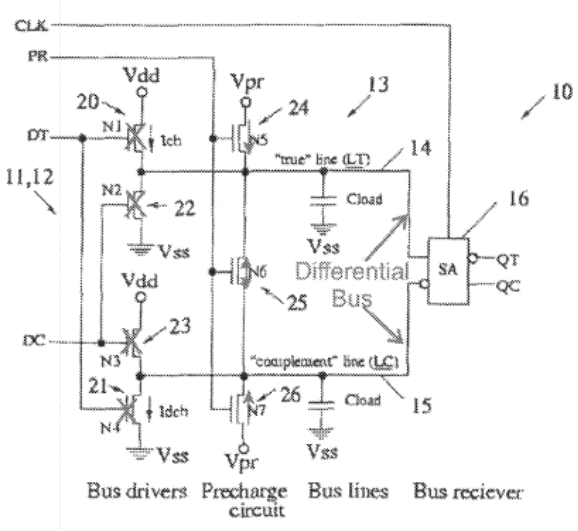
i. "The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus."

Sukegawa teaches a precharge circuit coupled between the precharge source BLR and the differential bus LINE and LINE_. *See, e.g.*, Ex. 1002, ¶ 34; *Sukegawa* Fig. 1 (annotated below).



Sukegawa discloses that the above identified precharge circuit provides a precharge voltage as follows: "[t]he PC node is connected to the gates of nMOS transistors 30, 31, and 32. In the initial precharge state, the PC node enters the H level; in the drive state, the PC node changes from H level to L level; in the precharge state, it changes from L level to H level. The BLR node is connected to the drain of the nMOS transistor 30 and the drain of nMOS transistor 31, and the BLR node becomes the power source voltage VDD/2 in the initial precharge state." *Sukegawa* 8:28-36; *see also, e.g.*, Ex. 1002, ¶ 34. The precharge circuit is between the voltage precharge source and the differential bus because the transistors within the precharge circuit connect the voltage precharge source to the differential bus. *Sukegawa* 8:28-36; *see also, e.g.*, Ex. 1002, ¶ 34. This is consistent with the '130 Patent's disclosure and the Patent Owner's characterization of the disclosure

during reexamination:

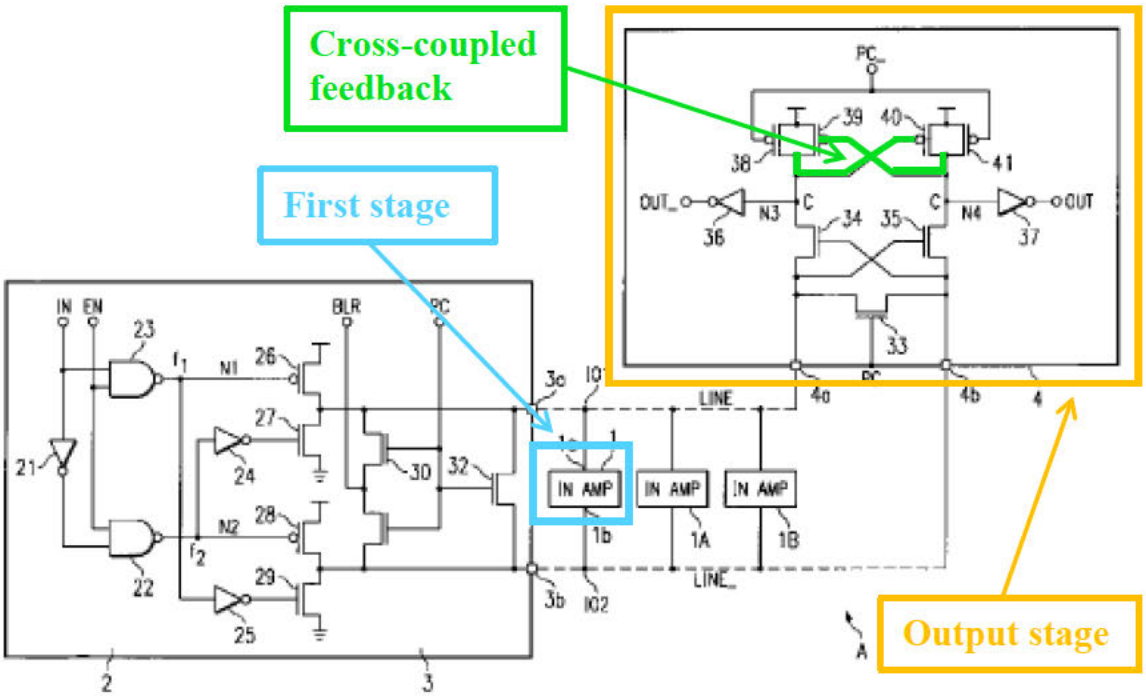


Ex. 1004, p. 68 (declaration of Dr. Philip Koopman disclosing precharge circuit 13 and the "differential bus"); Ex. 1002, ¶ 34.

5. Claim 9

i. "The data transfer arrangement of claim 1 wherein the output stage includes cross-coupled feedback."

Sukegawa teaches an output stage with cross-coupled feedback. *See, e.g.*, Ex. 1002, ¶ 35; *Sukegawa* Fig.1 (annotated below).



See also, e.g., *Sukegawa* 5:5-12; Ex. 1002, ¶ 35. The cross-coupled feedback identified above is consistent with the "cross-coupled feedback" identified by the Patent Owner during *inter partes* reexamination. Ex. 1002, ¶ 35. In particular, Patent Owner argued that "cross-coupled feedback" was demonstrated by Fig. 2 of the '130 Patent, which is nearly (if not entirely) identical with Petitioner's mapping of *Sukegawa*:

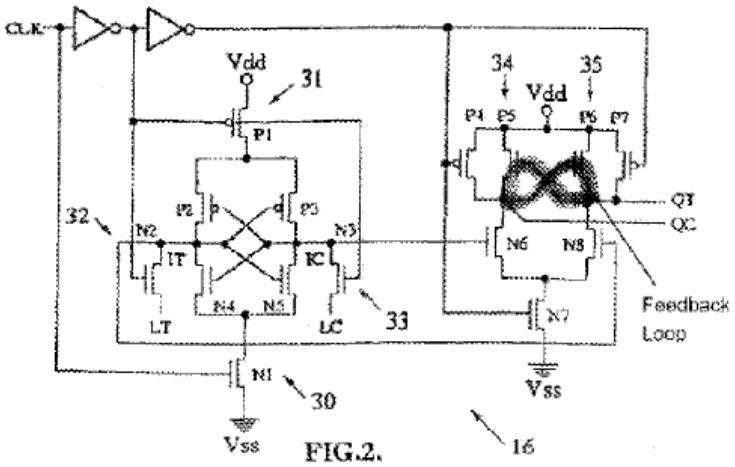


FIG.2.

Ex. 1004, p. 127; *see also* Ex. 1002, ¶ 35. Patent Owner argued that "feedback' should be construed to mean "a loop in the topography of a circuit where, in addition to its input being connected to its output, its output is also connected to its input via a different path." Ex. 1004, p. 126. The circuit in *Sukegawa* meets this definition as the output C above transistor 34 is tied to the input gate of transistor 40 and the output C above transistor 35 is tied to the input gate of transistor 39. Ex. 1002, ¶ 35; *see also, e.g.*, *Sukegawa* 8:59-64, Fig. 1. Indeed, this identical circuitry disclosed by Fig. 2 of the '130 Patent was not only sufficient to satisfy the "feedback" limitation of claim 9, but also the additional limitation that the feedback must be "cross-coupled." Ex. 1004, pp. 126-27, 139-40. Accordingly, *Sukegawa* discloses cross-coupled feedback like that recited in the claim. Ex. 1002, ¶ 35; *see also, e.g.*, *Sukegawa* 8:59-64.

C. Ground 2: *Sukegawa*, *Lu*, and *Watanabe* Render Claim 3 Obvious

While *Sukegawa* and *Lu* disclose a first stage of a latching sense amplifier,

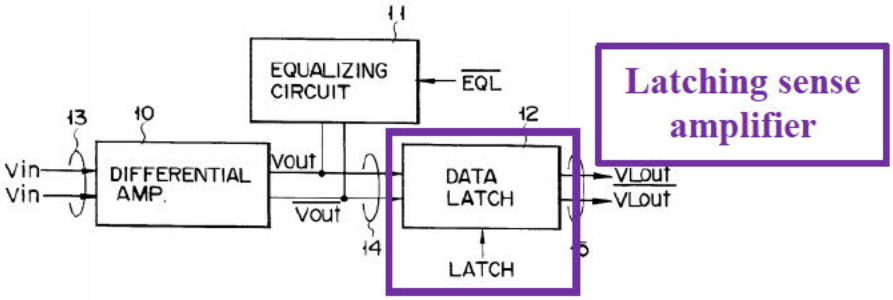
they do not expressly disclose each limitation recited in claim 3 of the ’130 Patent. However, one of ordinary skill in the art at the time of the alleged invention for the ’130 Patent would have found it obvious to modify the combined arrangement of *Sukegawa* and *Lu* to include such features in light of the disclosure of *Watanabe*. *See, e.g.*, Ex. 1002, ¶ 36-37.

All three references are related to the same field of technology – transmission of data through electronic circuits. *See, e.g.*, Ex. 1002, ¶ 36; *see supra* Section VII.A. Furthermore, one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have been motivated to modify the first stage of the latching sense amplifier of *Sukegawa* with the first stage of *Watanabe*’s latching sense amplifier as *Watanabe*’s first stage comprises fewer transistors, and thus would speed up the operation of the circuit. *See, e.g.*, Ex. 1002, ¶ 36. *Watanabe*’s first stage also has fewer control signals and a smaller circuit layout. *See, e.g.*, Ex. 1002, ¶ 36. Both of these benefits allow more circuitry to be placed into a fixed area on the chip, and for this additional reason, one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have been motivated to modify *Sukegawa*’s first stage with *Watanabe*’s first stage. *See, e.g.*, Ex. 1002, ¶ 36. Indeed, doing so amounts to nothing more than using a known technique to improve similar devices in the same way and yields nothing more than predictable results. *See KSR*, 550 U.S. at 417.

As demonstrated in the exemplary disclosures below, *Sukegawa*, *Lu*, and *Watanabe* disclose or suggest each and every feature recited in claim 3.

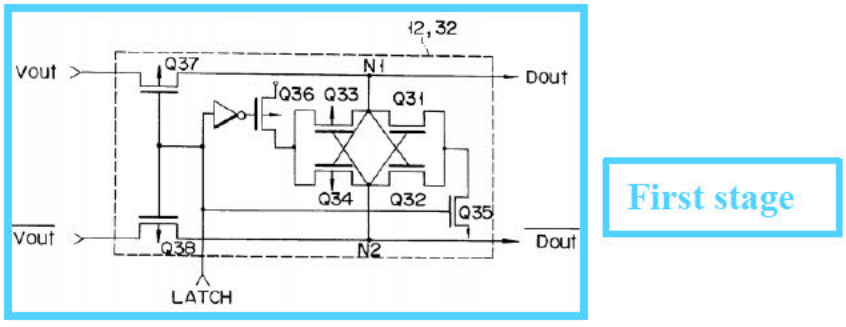
i. "3. The data transfer arrangement in accordance with claim 1,"

As discussed above for claim 1, *Sukegawa* and *Lu* discloses a data transfer arrangement including a latching sense amplifier with a first stage. *See supra* Section VII.B.1. *Watanabe* also discloses a data transfer arrangement including a latching sense amplifier with a first stage. *See, e.g.,* Ex. 1002, ¶ 37; *Watanabe* Fig. 1 (annotated below).



F I G. 1

The latching sense amplifier in *Watanabe* (i.e., data latch 12) includes a first stage (i.e., a portion of a circuit), which is further depicted in *Watanabe* Fig. 7. *See, e.g.,* Ex. 1002, ¶ 37; *Watanabe* Fig. 7 (annotated below), 4:13-16.



F I G. 7

ii. "wherein the first stage of the latching sense amplifier comprises: a plurality of input pass transistors each having a gate, a source terminal, and a drain; and"

Watanabe teaches that the first stage comprises of a plurality of input pass transistors each having a gate, source, and drain. *See, e.g.*, Ex. 1002, ¶ 37; *Watanabe* Fig. 7 (annotated below).

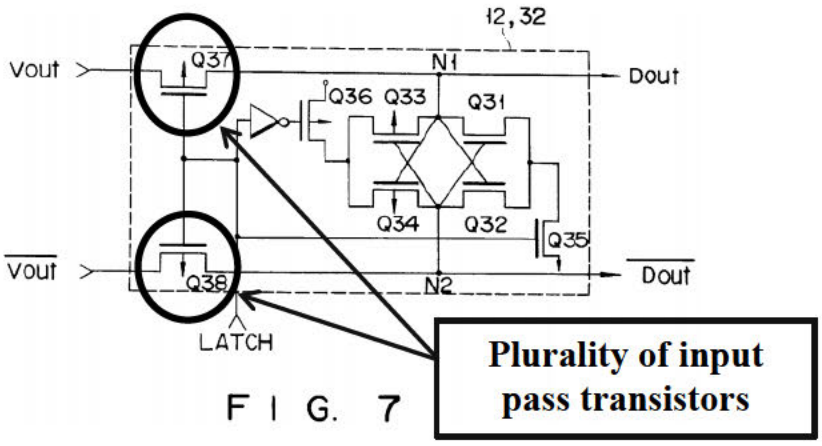
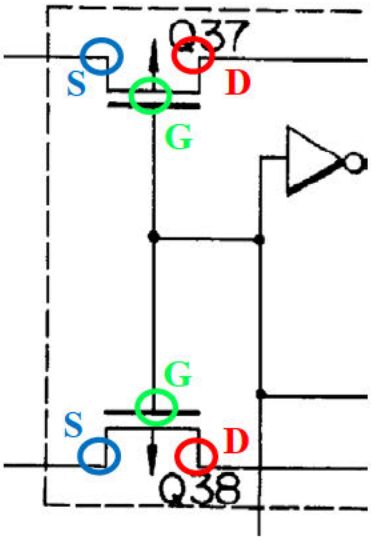


FIG. 7

Transistors Q37 and Q38 act as input pass transistors because they pass voltages from vout and $\overline{\text{vout}}$ to nodes N1 and N2, respectively. *See, e.g.*, *Watanabe* 4:22-30; *see also, e.g.*, Ex. 1002, ¶ 37.

One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the gate, source, and drain of the input pass transistors are as indicated in *Watanabe* Fig. 7, annotated below (sources in blue circles; drains in red circles; gates in green circles)[7]:

[7] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the sources and drains for



See also, e.g., Ex. 1002, ¶ 37.

iii. "a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain; and"

Watanabe teaches that the first stage comprises of a plurality of NMOS and PMOS transistors each having a gate, source, and drain. *See, e.g.*, Ex. 1002, ¶ 37; *Watanabe* Fig. 7 (annotated below).

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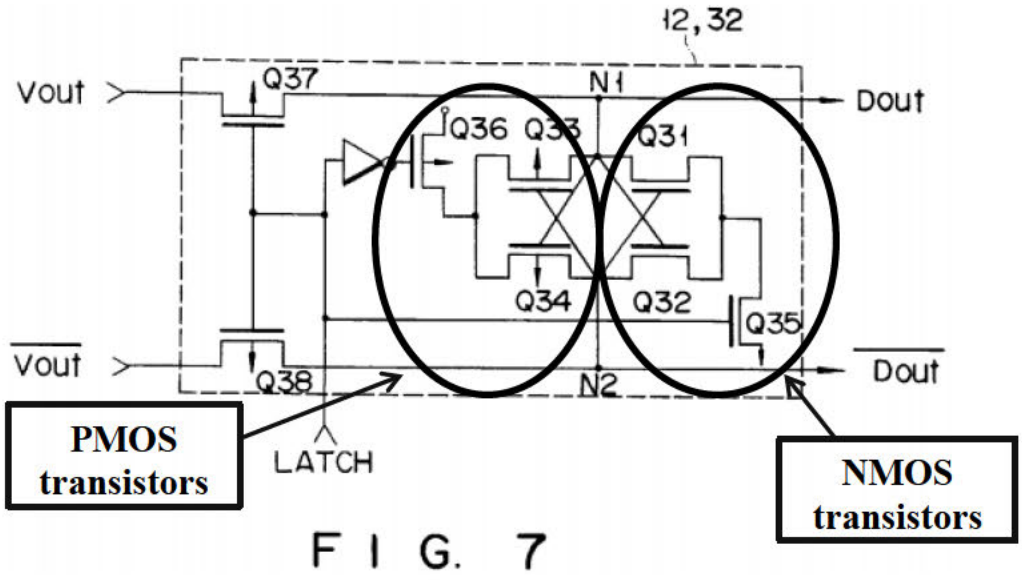
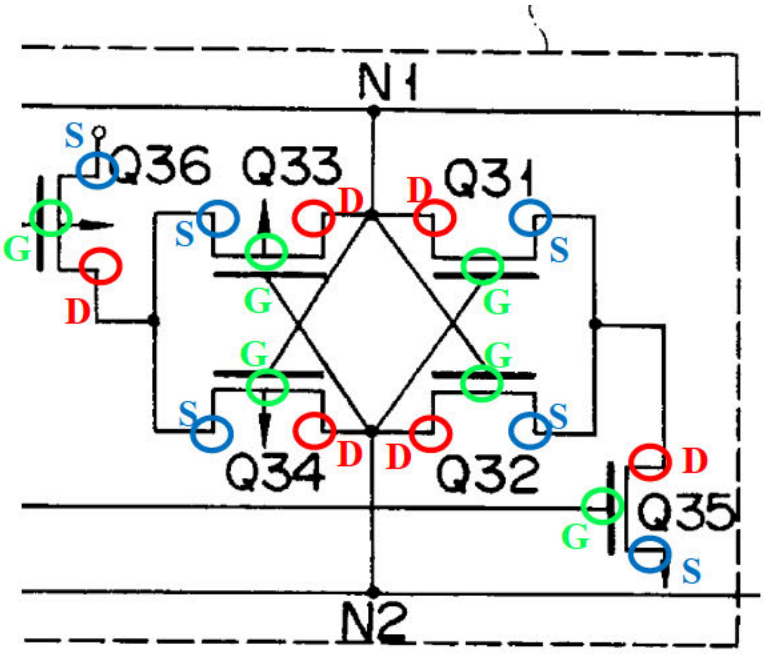
the input pass transistors is dependent on the voltage provided to the transistors from vout and $\overline{\text{vout}}$. Nonetheless, the identification of the sources and drains in annotated Fig. 7 of *Watanabe* is consistent with the '130 Patent's specification and identification of sources and drains for the claimed input pass transistors. *See, e.g.*, Ex. 1002, ¶ 37, n.1.



F I G. 7

Watanabe discloses that "[t]he data latch circuit shown in FIG. 7 comprises a pair of *three n-channel MOS transistors Q31, Q32 and Q35 and five p-channel MOS transistors Q33, Q34, Q36, Q37 and Q38*. The MOS transistors Q31, Q32, Q33 and Q34 constitute a flip-flop. The MOS transistors Q35 and Q36 are used to activate the flip-flop. The MOS transistors Q37 and Q38 are latch control elements." *Watanabe* 4:16-22 (emphasis added).

One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the gate, source, and drain of the plurality of NMOS and PMOS transistors are as indicated in *Watanabe* Fig. 7, annotated below (sources in blue circles; drains in red circles; gates in green circles):

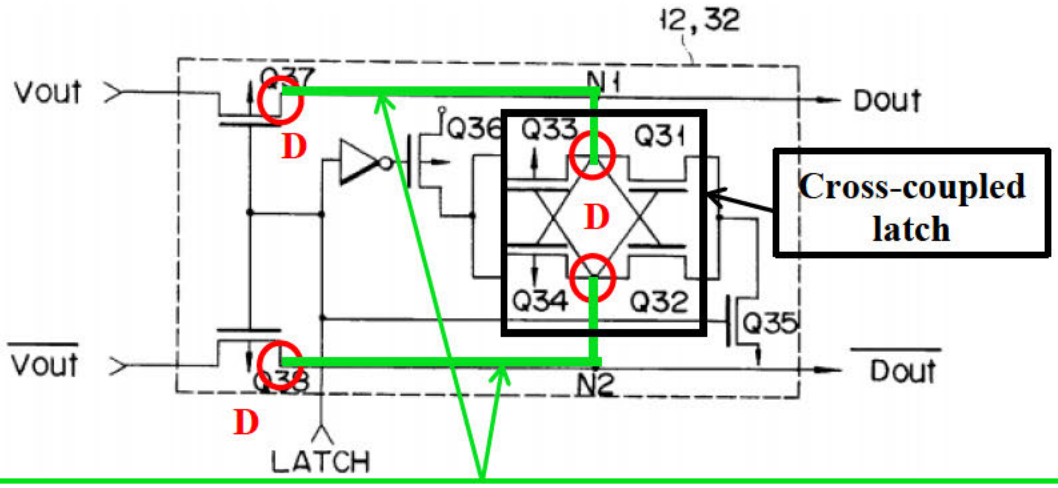


See also, e.g., Ex. 1002, ¶ 37.

iv. "wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors,

Watanabe discloses a first stage of a latching sense amplifier wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors. *See, e.g.*, Ex. 1002, ¶ 37. *Watanabe* explains that "[t]he MOS transistors Q37 and Q38 are latch control elements. In operation, the p-channel MOS transistors Q37 and Q38 are turned on when the latch control signal LATCH falls to a low level, whereby the input data is transferred to the nodes N1 and N2 of the flip-flop. When the control signal LATCH rises to a high level, the transistors Q37 and Q38 are turned off, whereby the nodes N1 and N2 are disconnected from the input lines, and the flip-flop is

activated at the same to hold the data." *Watanabe* 4:21-30, Fig. 7 (drains in red circles; annotated below).[8]



See also, e.g., Ex. 1002, ¶ 37. Transistors Q31, Q32, Q33, and Q34 are cross-coupled because the output of a first transistor (e.g., Q31) is tied to the input of a second transistor (e.g., Q32), and the output of the second transistor (e.g., Q32) is

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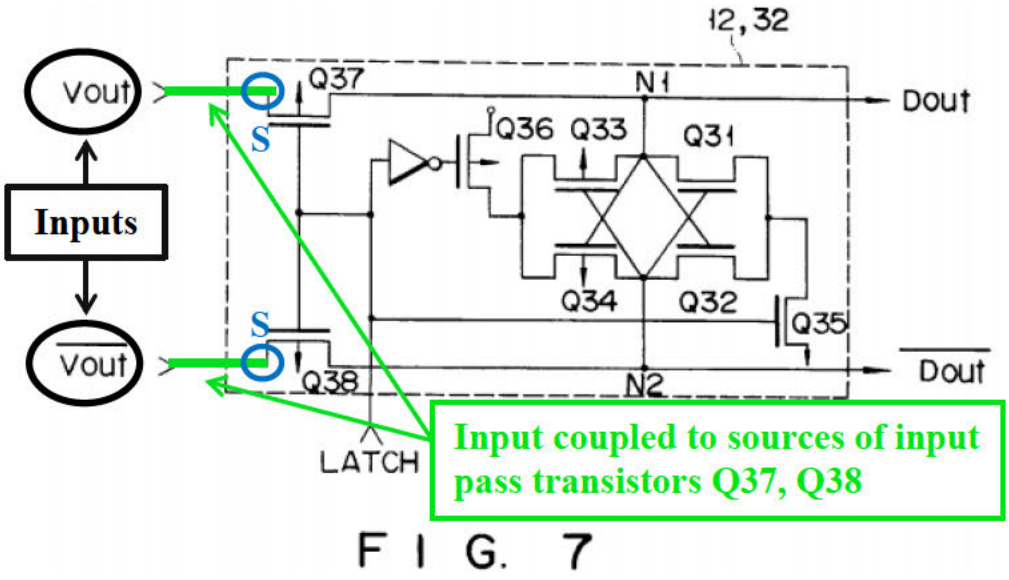
[8] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the drains for the input pass transistors is dependent on the voltage provided to the transistors from vout and $\overline{\text{vout}}$. Nonetheless, the identification of the drains in annotated Fig. 7 of *Watanabe* is consistent with the '130 Patent's specification and identification of drains for the claimed input pass transistors. *See, e.g.*, Ex. 1002, ¶ 37, n.2.

tied to the input of the first transistor (e.g., Q31). Ex. 1002, ¶ 37. Similarly, the output of transistor Q33 is tied to the input of transistor Q34, and vice versa. Ex. 1002, ¶ 37.

v. each source terminal of the input pass transistor is coupled to an input,

Watanabe discloses a first stage of a latching sense amplifier wherein each source terminal of the input pass transistors is coupled to an input. *See, e.g.*, Ex. 1002, ¶ 37; *Watanabe* 4:13-16, Fig. 7 (sources in blue circles; annotated below).[9]

[9] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the sources for the input pass transistors is dependent on the voltage provided to the transistors from vout and $\overline{\text{vout}}$. Nonetheless, the identification of the sources in annotated Fig. 7 of *Watanabe* is consistent with the '130 Patent's specification and identification of sources for the claimed input pass transistors. *See, e.g.*, Ex. 1002, ¶ 37, n.3.



F I G. 7

See also, e.g., Ex. 1002, ¶ 37.

vi. the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor coupled to a clock signal input, and

Watanabe discloses a first stage of a latching sense amplifier wherein the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor. *See, e.g.*, Ex. 1002, ¶ 37. *Watanabe* Fig. 7. *Watanabe* discloses that "[i]n operation, the p-channel MOS transistors Q37 and Q38 are turned on when the latch control signal LATCH falls to a low level, whereby the input data is transferred to the nodes N1 and N2 of the flip-flop. When the control signal LATCH rises to a high level, the transistors Q37 and Q38 are turned off, whereby the nodes N1 and N2 are disconnected from the input lines, and the flip-flop is activated at the same to hold the data." *Watanabe* 4:23-30, Fig. 7 (sources in blue circles; drains in red circles; annotated below).

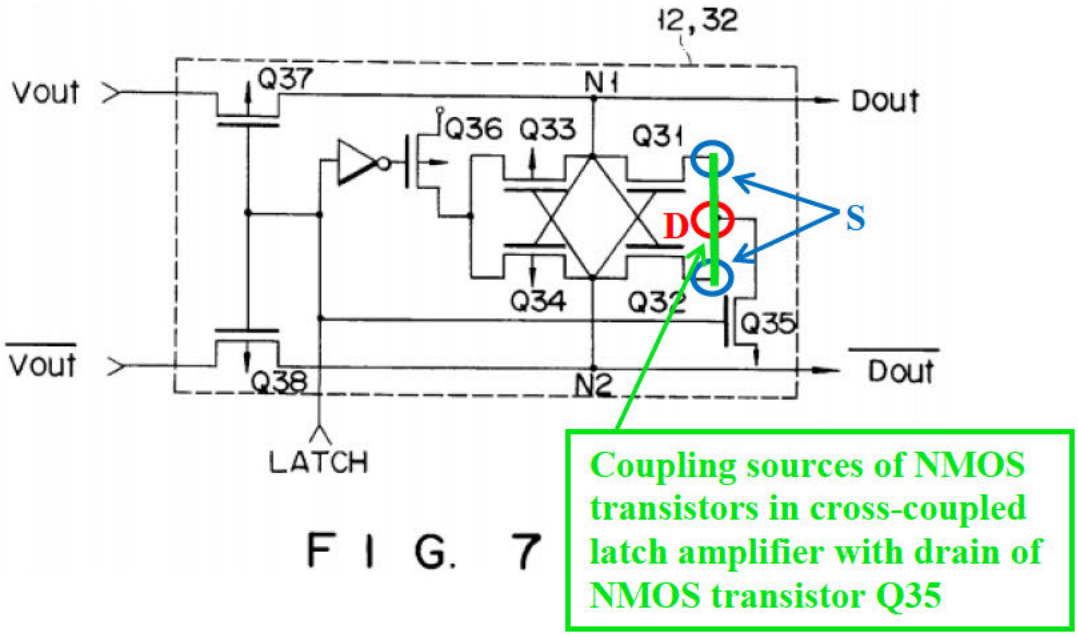


FIG. 7

See also, e.g., Ex. 1002, ¶ 37. *Watanabe* further teaches that NMOS transistor Q35 is coupled to a clock signal input LATCH. *See, e.g.*, *Watanabe* Fig. 7 (annotated below), 4:23-30; Ex. 1002, ¶ 37.

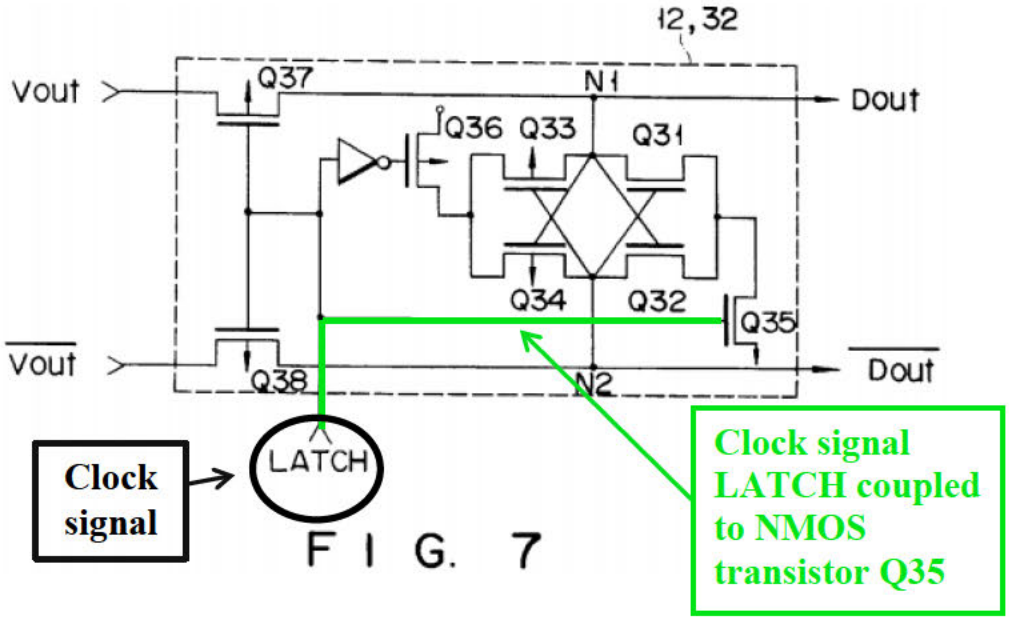


FIG. 7

See also, e.g., Ex. 1002, ¶ 37.

vii. the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input."

Watanabe discloses a first stage of a latching sense amplifier wherein the sources of the cross-coupled latch amplifier PMOS transistors are coupled to the drain of the PMOS transistor. *See, e.g.*, Ex. 1002, ¶ 37; *Watanabe* Fig. 7 (sources in blue circles; drains in red circles; annotated below).

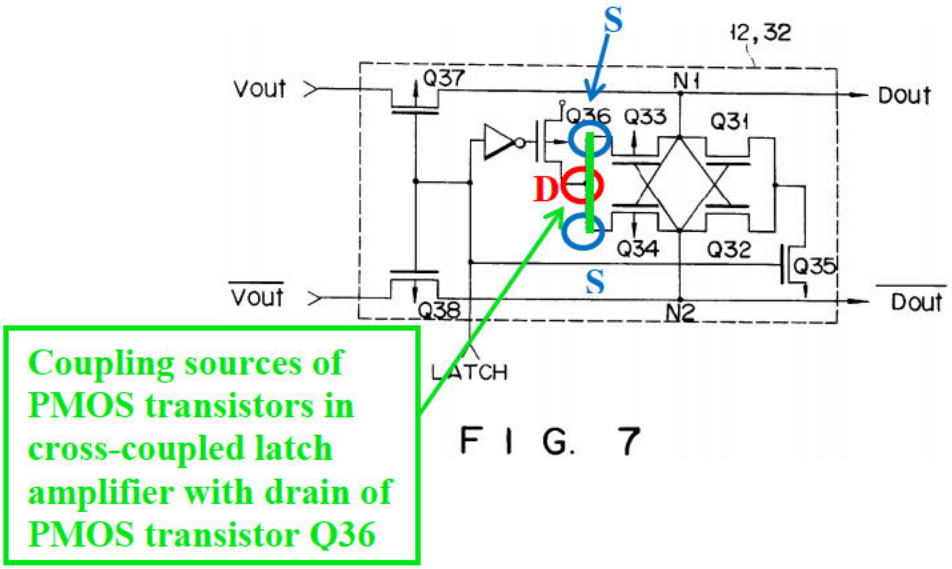


FIG. 7

See also, e.g., Ex. 1002, ¶ 37. *Watanabe* further teaches that the gate of PMOS transistor Q36 is coupled to an inverted clock signal (i.e., the inverse of clock signal LATCH). *See, e.g.*, *Watanabe* Fig. 7 (annotated below), 4:23-30; Ex. 1002, ¶ 37.

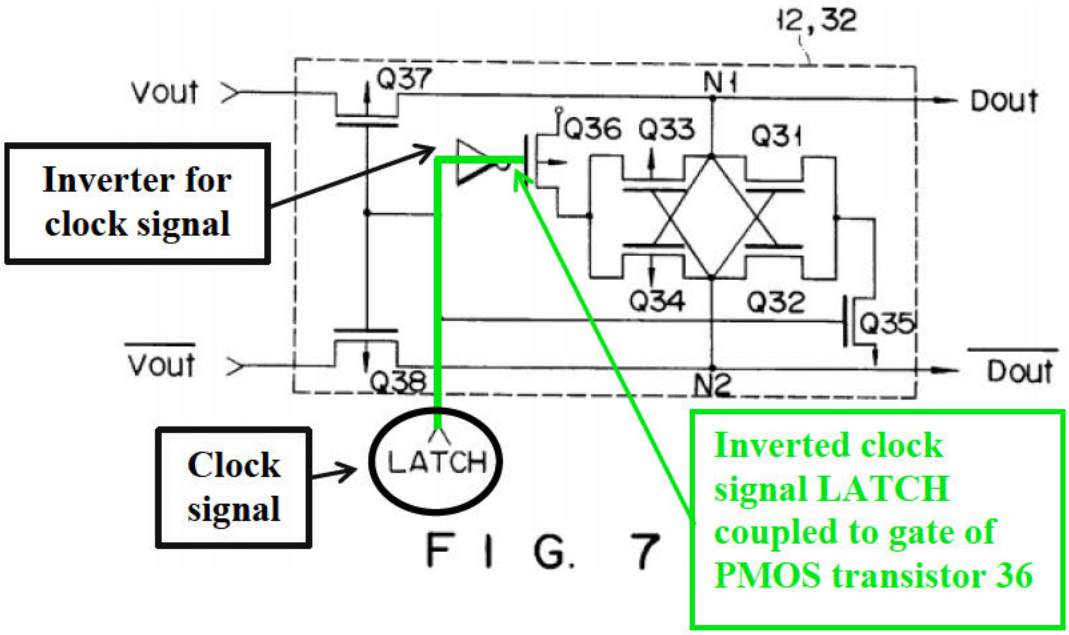


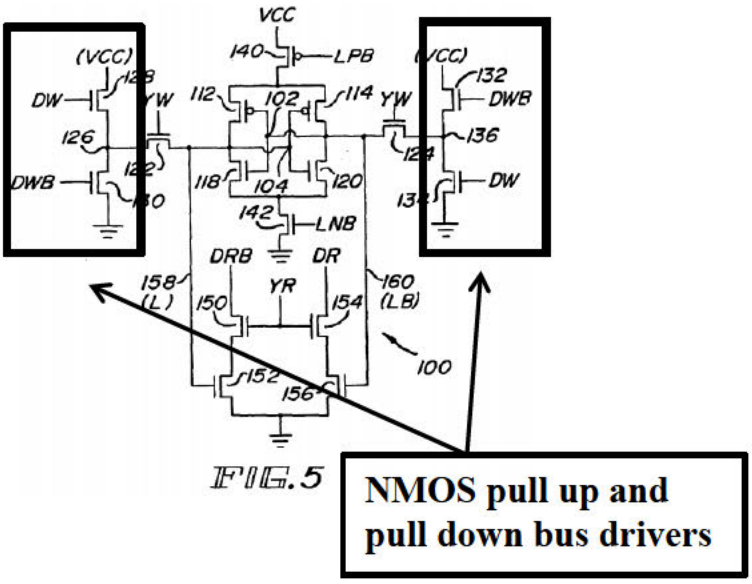
FIG. 7

See also, e.g., Ex. 1002, ¶ 37.

D. Ground 3: *Sukegawa*, *Lu*, and *Hardee* Render Claim 7 Obvious

i. "7. The data transfer arrangement in accordance with claim 2 wherein the active pull up and active pull down bus drivers are NMOS transistors."

While *Sukegawa* and *Lu* disclose active pull down drivers that are NMOS transistors, they do not expressly disclose active pull up drivers that are NMOS transistors. However, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have found it obvious to use NMOS transistors for pull up and pull down bus drivers in light of *Hardee*. *See, e.g.*, Ex. 1002, ¶¶ 39-42. It was well known at the time of the alleged invention of the '130 Patent that active pull up and pull down bus drivers could be designed with NMOS transistors, as shown, for example, by Fig. 5 of *Hardee*, annotated below:



See also, e.g., *Hardee* 6:28-46; Ex. 1002, ¶ 40. Given the teachings of *Hardee*, which is in the same field of technology as *Sukegawa* and *Lu* (*see supra* Section VII.A), one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to reconfigure the circuit and bus drivers in *Sukegawa* and *Lu* with NMOS pull up and pull down bus drivers to reduce the layout area and avoid latch-up. *See, e.g.*, Ex. 1002, ¶ 41. A smaller layout size can be important when connecting the drivers up to an array of transistors, as used in a memory, or when driving a parallel data bus where the data signals are laid out directly adjacent to each other. *See, e.g.*, Ex. 1002, ¶ 41. A smaller layout size is achieved with NMOS transistors as it eliminates the need for the n-well used in the construction of PMOS transistors. *See, e.g.*, Ex. 1002, ¶ 41.

Further, modifying the PMOS transistors in the bus drivers with NMOS transistors allows the driver to become immune to latch-up. *See, e.g.*, Ex. 1002, ¶

41. One skilled in the art at the time of the alleged invention of the ’130 Patent would have been motivated to avoid latch-up as latch-up causes a wire to short circuit to a power supply Vdd or ground. *See, e.g.*, Ex. 1002, ¶ 41. Avoiding latch-up is especially important when driving a signal off-chip, where the driver is connected to a bonding wire which is inductive and thus can produce ringing voltages. *See, e.g.*, Ex. 1002, ¶ 41.

Moreover, implementing pull up and pull down bus drivers using solely NMOS transistors in *Sukegawa* and *Lu* is merely a design choice that one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have certainly understood. *See, e.g.*, Ex. 1002, ¶ 42. This follows from the fact that there were a small finite number of MOSFET configurations for implementing pull up and pull down bus drivers (e.g., NMOS, PMOS, or CMOS – both NMOS and PMOS). *See, e.g.*, Ex. 1002, ¶ 42. Indeed, doing so amounts to nothing more than using a known technique to improve similar devices in the same way and yields nothing more than predictable results. *See KSR*, 550 U.S. at 417.

VIII. STATEMENT REGARDING OTHER PETITION

As noted, Petitioner is filing another petitioner concurrently with this Petitioner. This Petition presents an obviousness ground based on *Sukegawa* and *Lu*, while the other petition presents an anticipation ground based on a different primary reference. The Board should institute review based on both petitions.

Petitioner has attempted to streamline the petitions by raising grounds based on only one primary reference in each petition. This achieves the goal of "just, speedy and inexpensive resolution" consistent with 37 C.F.R. § 42.1(b). In addition, the two petitions present independent, distinctive, and non-redundant grounds at least because Patent Owner may attempt to distinguish the primary references with different arguments.

IX. CONCLUSION

For the reasons given above, Petitioner requests *inter partes* review and cancellation of claims 1-3, 5-7, and 9 of the '130 Patent.

Respectfully submitted,

Dated: June 26, 2015

By: /Steven L. Park/
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Paul Hastings LLP

Counsel for Samsung Electronics Co., Ltd.

CERTIFICATE OF SERVICE

The undersigned certifies service under 37 C.F.R. §§ 42.6(e) and 42.105 by Express Mail of a true and correct copy of this Petition For *Inter Partes* Review and supporting material on June 26, 2015, upon counsel for the Patent Owner at the correspondence address below:

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Phone: 708-528-9092

The undersigned also certifies service under 37 C.F.R. §§ 42.6(e) and 42.105 by Express Mail of a true and correct copy of this Petition For *Inter Partes* Review and supporting material on June 26, 2015, upon the Patent Owner's lead litigation counsel at the correspondence address below:

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