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Filed on behalf of: Samsung Electronics Co., Ltd.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

ELBRUS INTERNATIONAL LIMITED
Patent Owner

U.S. Patent No. 6,366,130

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,366,130

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review of claims 1-3, 5-7, and 9 of U.S. Patent No. 6,366,130 ("the '130 Patent") (Ex. 1001), which Petitioner understands is assigned to Elbrus International Limited ("Patent Owner").[1] This Petition shows that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims, and thus a trial should be instituted. This Petition also establishes by a preponderance of the evidence that the challenged claims are unpatentable under 35 U.S.C. §§ 102 and/or 103. These claims should be canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Party-in-Interest: Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner identifies Samsung Electronics Co., Ltd. as the real party-in-interest.

Related Matters: In accordance with 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matters. Patent Owner asserted the '130 Patent against Petitioner in a patent litigation filed on July 24, 2014, in the Northern District of Illinois (case no. 1:14-cv-05691), which remains pending. Patent Owner also asserted the '130 Patent against Hynix Semiconductor, Inc. and SK Hynix Inc.

[1] Petitioner understands that the '130 Patent is exclusively licensed to Cascades Computer Innovation, LLC.

on June 27, 2011 in the Northern District of Illinois (case no. 1-11:cv-04356), but this case was dismissed on February 6, 2014. Hynix Semiconductor Inc. sought *inter partes* reexamination (control no. 95/000,657) on January 19, 2012, but that proceeding resulted in a reexamination certificate that issued on August 4, 2014.

Petitioner is concurrently filing a second petition for *inter partes* review also challenging claims 1-3, 5-7, and 9.

Counsel and Service Information: Lead counsel is Steven L. Park (Reg. No. 47,842), Paul Hastings LLP, 1170 Peachtree Street, NE, Suite 100, Atlanta, GA 30309, Telephone: (404) 815-2223, Fax: (404) 685-2223, E-mail: stevenpark@paulhastings.com. Back-up counsel is Naveen Modi (Reg. No. 46,224), Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Telephone: 202.551.1700, Fax: 202.551.1705, E-mail: naveenmodi@paulhastings.com. Petitioner consents to electronic service

III. PAYMENT OF FEES UNDER 37 C.F.R. §§ 42.15 AND 42.103

Petitioner submits the required fees with this petition. Please charge any additional fees required for this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING AND IDENTIFICATION OF CHALLENGE

Petitioner certifies that the ’130 Patent is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting such review of the ’130 Patent on the grounds identified below.

Petitioner challenges claims 1-3, 5-7, and 9 of the '130 Patent and requests that these claims be found unpatentable and canceled in view of the following prior art references: U.S. Patent No. 6,052,328 to Ternullo et al. ("*Ternullo*") (Ex. 1005); U.S. Patent No. 5,828,241 to Sukegawa ("*Sukegawa*") (Ex. 1006); and U.S. Patent No. 6,249,469 to Hardee ("*Hardee*") (Ex. 1007).

The '130 Patent attempts to claim priority to provisional application no. 60/120,531 ("the '531 provisional application"), filed February 17, 1999. For purposes of this proceeding, Petitioner has assumed that the '130 Patent is entitled to the February 17, 1999 date.[2] *Sukegawa* issued on October 27, 1998 and is thus prior art under pre-AIA 35 U.S.C. § 102(a). *Ternullo* and *Hardee* were both filed prior to February 17, 1999 and issued after that date, and are therefore prior art under pre-AIA 35 U.S.C. §102(e).

Petitioner requests cancellation of the challenged claims on the following grounds:

Ground 1: Claims 1-3 and 5-6 are unpatentable under pre-AIA 35 U.S.C. § 102(e) as anticipated by *Ternullo*.

[2] Petitioner does not concede that the '130 Patent claims comply with 35 U.S.C. § 112 or that they are entitled to the assumed priority date. Petitioner reserves the right to raise these and other issues in a district court or another forum.

Ground 2: Claim 7 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over *Ternullo* in view of *Hardee*.

Ground 3: Claim 9 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over *Ternullo* in view of *Sukegawa*.

V. BACKGROUND

The ’130 Patent issued from U.S. Patent Application No. 09/505,656 (“the ’656 application”), filed February 17, 2000, and attempts to claim priority to the ’531 provisional application. Ex. 1001 Title Page.

A. The ’130 Patent

The ’130 Patent is purportedly directed to a data transfer scheme that includes two bus drivers, a precharge circuit, two complementary bus lines, and a latching sense amplifier. Ex. 1001 2:1-8; Ex. 1002, ¶ 17. Fig. 1 of the ’130 Patent illustrates two bus drivers 11, 12 (consisting of transistors 20, 21, 22, and 23) and two complementary bus lines 14, 15 as inputs to a latching sense amplifier 16:

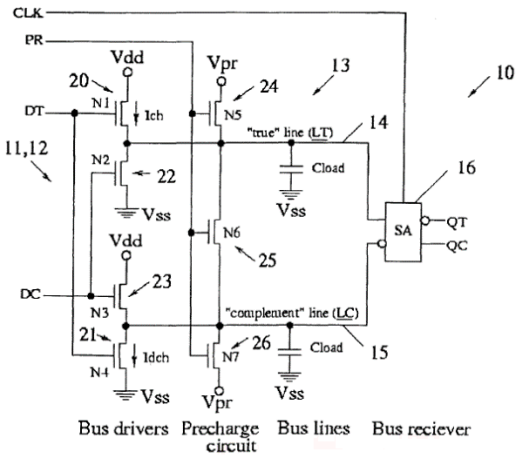

FIG.1.

See also, e.g., Ex. 1002, ¶ 17. According to the patent, the data transfer scheme operates in two phases: a precharge phase and a data transfer phase (Ex. 1001 2:12-13; Ex. 1002, ¶ 18), with the bus drivers and complementary bus lines operating in opposite phases to the latching sense amplifier (Ex. 1001 2:43-44; Ex. 1002 ¶ 18). In other words, when the complementary bus lines and the bus drivers are in the precharge phase, the sense amplifier is in data transfer phase and vice versa. Ex. 1002, ¶ 18.

The ’130 Patent includes 9 claims with claims 1 and 8 being independent and claims 2-7 and 9 being dependent from claim 1. Claim 9 was added during reexamination. Independent claim 1 is reproduced below:

1. A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; aid [sic]

a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage;

wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor.

B. Prosecution History of the ’130 Patent

During prosecution, all claims of the ’656 application that eventually issued as the ’130 Patent were initially rejected as unpatentable over prior art. Ex. 1003, pp. 43-44. In response, claim 1 of the application was amended to clarify that the “latching sense amplifier” comprises of a “first stage including a cross-coupled latch coupled to a differential data bus” and an “output stage” coupled to the output of the “first stage.” *Id.*, p. 53. Applicants explained that the latching sense amplifier disclosed by the prior art did not include two stages, whereas amended claim 1 now included both a “first stage” and an “output stage” of a latching sense amplifier. *Id.*, p. 50-51. Applicants also distinguished the purported invention over the cited prior art by noting the purported invention “teaches precharging the buses to a specific level *between ground and Vdd* (Vpr = K*Vdd, where K is precharging voltage factor),” rather than Vdd as taught by the prior art. *Id.*, p. 50 (emphasis added). Applicants later submitted a supplemental amendment to claim 1 to recite

the intermediate precharge voltage Vpr (*id.*, p. 60-62), and a notice of allowance was issued shortly thereafter (*id.*, pp. 64-68).

C. Reexamination History of the ’130 Patent

As noted above, Hynix filed an *inter partes* reexamination, i.e., control no. 95/000,657 (“the ’657 proceeding”). *See* Ex. 1004 (excerpts from the ’657 proceeding). During *inter partes* reexamination, claims 1-3 and 5-7 were confirmed. Patent Owner also submitted new claims, but all but one were rejected under 35 U.S.C. § 112. *Id.*, pp. 134-44. This one claim eventually issued as claim 9. Ex. 1001 Reexam Cert. 1:20-21.

D. Prior Art Raised in This Petition

This Petition relies on prior art that the U.S. Patent and Trademark Office (“PTO”) did not have before it or did not fully consider during prosecution and reexamination. None of the prior art references relied on in this Petition were cited during prosecution or reexamination.[3] As explained below, the prior art discussed

[3] Hynix relied on European patent publication no. EP 0 597 231 during reexamination. This European publication is related to *Hardee*. *Hardee* was, however, never considered as presented herein, especially in light of the accompanying expert testimony.

in this Petition anticipates or renders obvious the claims of the ’130 Patent, especially when considered in light of the declaration of Dr. R. Jacob Baker (Ex. 1002).

VI. CLAIM CONSTRUCTION

In an *inter partes* review, the Board applies the broadest reasonable interpretation (“BRI”) standard to construe claim terms.[4] Under the BRI standard, claim terms are given their “broadest reasonable interpretation, consistent with the specification.” *In re Ya amoto*, 740 F.2d 1569, 1571 (Fed. Cir. 1984); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,764 (Aug. 14, 2012). Claim terms are also “generally given their ordinary and customary meaning,” which is the meaning that the term would have to a person of ordinary skill in the art.[5] *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (quoting *Phillips v.*

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[4] Petitioner notes that the district courts apply a different claim construction standard and reserves its rights to make arguments based on that standard in the district court.

[5] A person of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have had an undergraduate degree in Electrical Engineering or equivalent and at least two to three years of experience in the design and/or analysis of data transfer circuits or the equivalent. Ex. 1002, ¶ 15.

AWH Corp., 415 F.3d 1303, 1312, 1313 (Fed. Cir. 2005) (*en banc*)). Petitioner proposes a construction for a few of the claim terms below and submits that the remaining terms in the ’130 Patent should be given their plain and ordinary meaning under the BRI standard.

A. Latching Sense Amplifier (Claims 1, 3)

Claims 1 and 3 recite the term “latching sense amplifier.” For purposes of this proceeding, “latching sense amplifier” should be construed to mean “a circuit, including a latch, that detects and amplifies signals.” This construction is consistent with the use of the term in the claims and specification of the ’130 Patent. Ex. 1002, ¶ 22

Neither the claims nor the specification explicitly define “latching sense amplifier.” The ’130 Patent’s specification describes its latching sense amplifier to include a latch (*see, e.g.*, Ex. 1001 2:39-40, 2:48-50) for detecting (*see, e.g.*, Ex. 1001 2:33-38, 2:64-67) and amplifying received signals (*see, e.g.*, Ex. 1001 2:64-67). *See also* Ex. 1002, ¶ 22. Also, latching sense amplifiers were well known at the time of the alleged invention of the ’130 Patent by those skilled in the art, and such individuals would have understood the term to be consistent with the Petitioner’s proposed construction. Ex. 1002, ¶ 22. Indeed, Petitioner’s construction is consistent with dictionary definitions of similar terms. *See, e.g.*, Ex. 1008 at 679 (defining “sense amplifier” as “[a] circuit used to sense low-level

voltages … and to amplify these signals to the logic voltage levels of the system"); *see also* Ex. 1002, ¶ 22.

The claims additionally specify what a "latching sense amplifier" has to include. Ex. 1002, ¶ 22. For example, claim 1 requires that the "latching sense amplifier" include both a first stage with a cross-coupled latch and an output stage. *See, e.g.*, Ex. 1001 4:8-13; Ex. 1002, ¶ 22. Accordingly, in the context of the '130 Patent, the broadest reasonable interpretation of "latching sense amplifier" is "a circuit, including a latch, that detects and amplifies signals," wherein the claims further define what that circuit includes. Ex. 1002, ¶ 22.

B. Stage (Claims 1, 3, 9)

Claims 1, 3, and 9 recite the term "stage." For purposes of this proceeding, "stage" should be construed to mean "portion of a circuit." This construction is consistent with the use of the term in the claims and specification of the '130 Patent as well as dictionary definitions for the term. Ex. 1002, ¶ 23.

Neither the claims nor the specification explicitly define "stage." However, independent claim 1 uses the term to indicate that a latching sense amplifier comprises of a "first stage" and an "output stage" and dependent claims 3 and 9 use the terms in context of particular circuitry found within a "first stage" and "output stage" of a latching sense amplifier. *See, e.g.*, Ex.1001 4:8-13, 4:21-23, Reexam Cert. 1:20-21; Ex. 1002, ¶ 23. Claim 1 notes that the "first stage" of the

latching sense amplifier must include cross-coupled latch circuitry. *See, e.g.*, Ex. 1001 4:8-13; Ex. 1002, ¶ 23. In claim 3, the "first stage" is described to include specific transistor circuitry and clock signals. *See, e.g.*, Ex. 1001 4:8-13; Ex. 1002, ¶ 23. The "output stage" of claim 9 includes circuitry for cross-coupled feedback. *See, e.g.*, Ex. 1001 Reexam Cert. 1:20-21; Ex. 1002, ¶ 23. The specification uses the term "stages" once (Ex. 1001 3:4-5) and that usage is consistent with the definition proposed here. Ex. 1002, ¶ 23. In addition, the Modern Dictionary of Electronics (7th ed. 1999) defines "stage" as "[a] single section of a multisection circuit or device." Ex. 1008 at 728. Accordingly, in the context of the '130 Patent, the broadest reasonable interpretation of "stage" is "portion of a circuit."

VII. DETAILED EXPLANATION OF UNPATENTABILITY

A. Brief Description of the Prior Art

As explained in detail below, the prior art identified and applied in this Petition discloses and/or suggests the limitations of claims 1-3, 5-7, and 9. Ex. 1002, ¶¶ 16, 24, 29-45. For example, *Ternullo* describes "a method and apparatus that accomplishes a high performance, random read/write SDRAM design by synchronizing the read and write operation at the data line sense amplifier." *Ternullo* Abstract; *see also, e.g.*, Ex. 1002, ¶ 25. As such, *Ternullo* generally relates to the transmission of signals in an electronic circuit. Ex. 1002, ¶ 25. *Ternullo* sought to overcome the challenges of using the same set of lines for

efficient read and write operations (*see, e.g., Ternullo* 2:9-35), and in doing so, teaches, *inter alia*, a "high performance write process without impacting the critical read path" (*id.* 1:9-10). *See also, e.g.*, Ex. 1002, ¶ 25.

Sukegawa describes "a type of signal transmission circuit wherein the signal is amplified and transmitted by means of the positive feedback of an intermediate amplifier circuit having input/output shared terminals." *Sukegawa* 1:11-15; *see also, e.g.*, Ex. 1002, ¶ 26. The signal transmission circuit disclosed sought to increase the signal transmission distance as well as increase the speed and lower the power consumption of a transmission. *Sukegawa* 4:52-55; *see also, e.g.*, Ex. 1002, ¶ 26. *Sukegawa* discloses that its signal transmission circuit comprises of "a driver circuit, a receiver circuit, an equalizer circuit, and an intermediate amplifier circuit." *Sukegawa* 4:62-65; *see also, e.g.*, Ex. 1002, ¶ 26. The intermediate amplifier circuit relies on positive feedback to amplify the signal provided by the driver circuit and transmit the amplified signal to the receiver circuit. *See, e.g.*, *Sukegawa* 5:1-4; *see also, e.g.*, Ex. 1002, ¶ 26.

Hardee is yet another prior art reference relating to signal transmission, and in particular, "integrated circuit memories" and "sense amplifiers for use therein." *See, e.g., Hardee* 1:8-10; Ex. 1002, ¶ 27. *Hardee* introduces a sense amplifier highlighted by three "salient" features:

> (1) the connection of each sense amplifier via transistors or other switching devices to the power supply lines without directly connecting together power supply lines for multiple sense amplifiers;
> (2) the use of local read amplifiers;
> (3) the use of local write circuitry.

See Hardee 5:24-32; *see also, e.g.*, Ex. 1002, ¶ 27.

All the prior art references mentioned above relate to signal transmission and were motivated to improve the efficiency of such transmissions. Ex. 1002, ¶ 28. As such, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to combine the teachings of these references. Ex. 1002, ¶ 28.

B. Ground 1: *Ternullo* Anticipates Claims 1, 3, 5, and 6

1. Claim 1

i. "A data transfer arrangement comprising:"

Ternullo discloses a data transfer arrangement. *See, e.g.*, Ex. 1002, ¶ 31. For example, *Ternullo* states that its "present invention provides a method and apparatus that accomplishes a high performance, random read/write SDRAM design by synchronizing the read and write operations at the data line sense amplifier." *Ternullo* Abstract; *see also, e.g.*, Ex. 1002, ¶ 31. In particular, *Ternullo* teaches that "[d]uring a read operation, read *data is transferred* from the memory cells of the device across a series of consecutive pairs of data lines to an

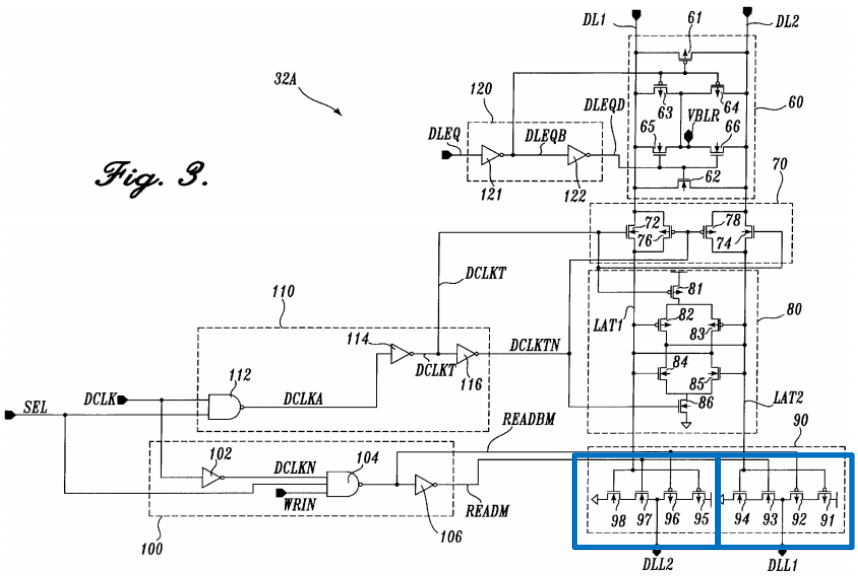
input/output port of the memory device." *Ternullo* Abstract (emphasis added); *see also, e.g.*, Ex. 1002, ¶ 31.

A data transfer arrangement is further disclosed through "a schematic diagram of the read circuitry 32A that is formed in accordance with the present invention as it may be implemented as part of the data sense line sense amplifier and supporting circuitry 32 (FIG. 1). The read circuitry 32A is required for performing a read operation." *Ternullo* 4:63-67, Figs. 1-2; *see also, e.g.*, Ex. 1002, ¶ 31.

ii. "two bus drivers[6];"

Ternullo discloses two bus drivers. *See, e.g.*, Ex. 1002, ¶ 31. For example, as shown below in annotated Fig. 3 of *Ternullo*, transistors 91-94 and transistors 95-98 serve as bus drivers:

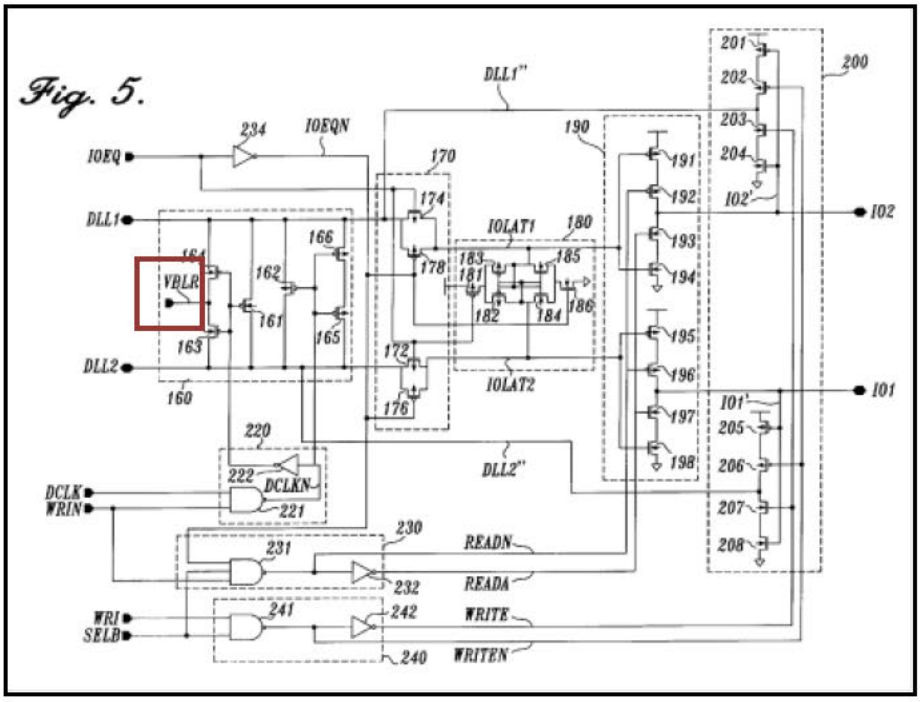
[6] Petitioner has used color and annotated figures throughout this Petition to illustrate how the prior art discloses the various claimed features.



See also, e.g., Ex. 1002, ¶ 31. *Ternullo* discloses: "read driver coupled to latch line LAT2 includes PFET transistors 91 and 92 and NFET transistors 93 and 94. The read driver coupled to latch line LAT1 includes PFET transistors 95 and 96 and NFET transistors 97 and 98." *Ternullo* 7:15-18; *see also, e.g.*, Ex. 1002, ¶ 31. The two bus drivers drive the outputs of Fig. 3 on lines DLL1 and DLL2. *See, e.g.*, *Ternullo* 7:31-37 ("The read driver operates such that when the signal on the latch line LAT2 is low, PFET transistor 91 is biased on, and if the signal READBM is also low at that time, a high signal will be passed to the line DLL1. If the latch line LAT2 is high, then the NFET transistor 94 will be biased on, and if the signal READM is high, then a low signal will be passed to the line DLL1."), 7:18-22 (same for LAT1); Ex. 1002, ¶ 31.

iii. "a voltage precharge source;"

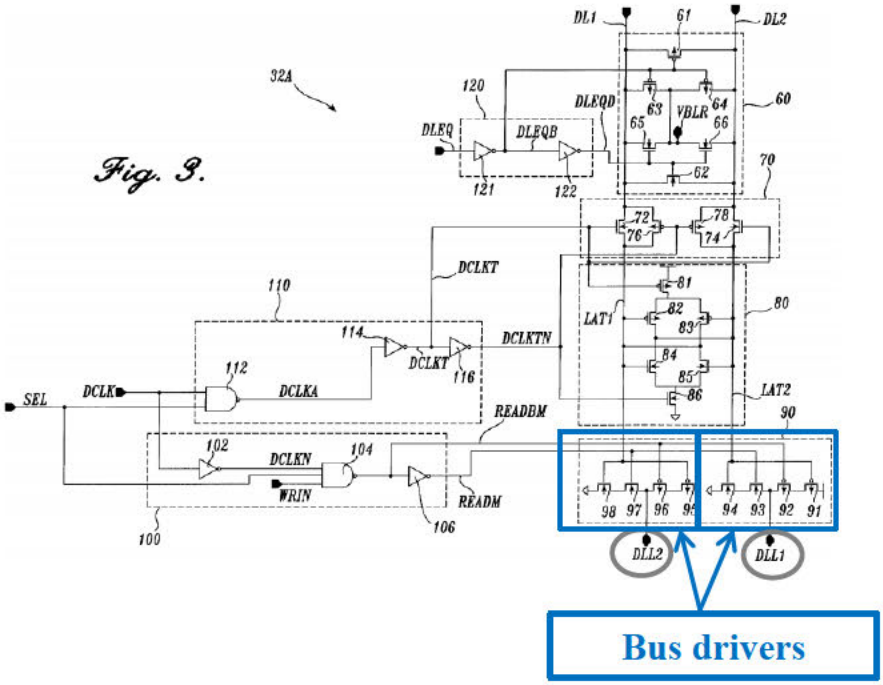
Ternullo discloses a voltage precharge source. *See, e.g.*, Ex. 1002, ¶ 31. For example, Fig. 5 of *Ternullo*, annotated below, discloses a voltage precharge source VBLR:

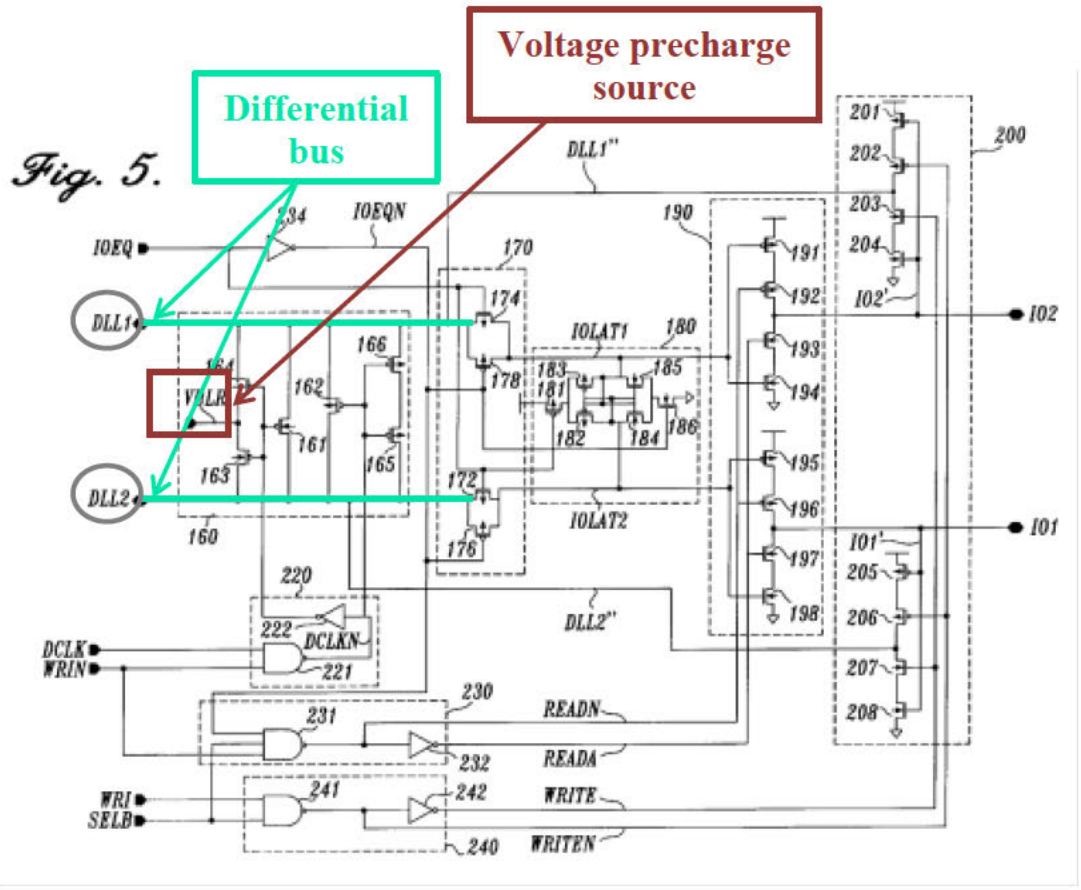


See also, e.g., Ex. 1002, ¶ 31. VBLR acts as a voltage precharge source to DLL1 and DLL2 because prior to receiving data on lines DLL1 and DLL2, these lines are precharged to the midlevel voltage VBLR. *See, e.g.*, *Ternullo* 8:28-32 (stating that "when control signal DCLKD is high and signal DCLKN is low, NFET transistor 161 and PFET transistor 162 couple line DLL1 to line DLL2, while NFET transistors 163 and 164 and PFET transistors 165 and 166 *couple the lines DLL1 and DLL2 to the midlevel voltage source VBLR*") (emphasis added), 10:35-40; *see also, e.g.*, Ex. 1002, ¶ 31.

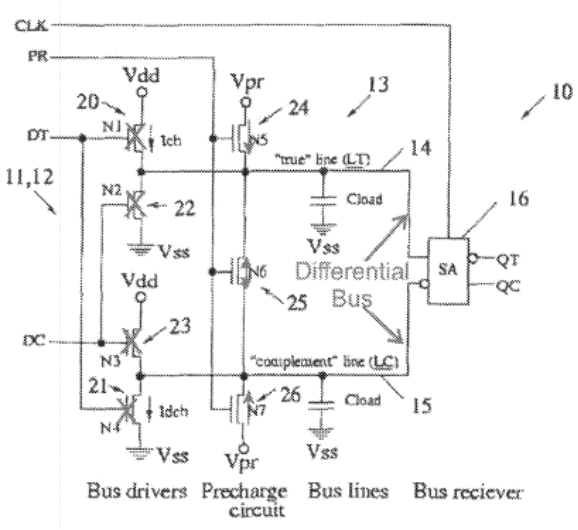
iv. "a differential bus coupled to the bus drivers and to the voltage precharge source; aid [sic]"

Ternullo teaches a differential bus coupled to the bus drivers and to the voltage precharge source. *See, e.g.*, Ex. 1002, ¶ 31. For example, as shown below in annotated Figs. 3 and 5 of *Ternullo*, the differential bus (i.e., lines DLL1 and DLL2) is coupled to the bus drivers (transistors 91-94 and 95-98) and the voltage precharge source VBLR:





See also, e.g., Ex. 1002, ¶ 31. One of ordinary skill in the art would have recognized at the time of the alleged invention of the '130 Patent that DLL1 and DLL2 represent the "differential bus" because a voltage differential (i.e., a difference in voltages between the two bus lines) can develop on these two bus lines. *See, e.g.*, *Ternullo* 10:35-43; Ex. 1002, ¶ 31. Moreover, as discussed below, differential bus DLL1 and DLL2 precede the isolation circuit 170 within *Ternullo*'s latching sense amplifier (*see, e.g.*, *Ternullo* Figs. 4-5; Ex. 1002, ¶ 31), and is consistent with Patent Owner's mapping of the "differential bus" in the '657 proceeding (Ex. 1002, ¶ 31):

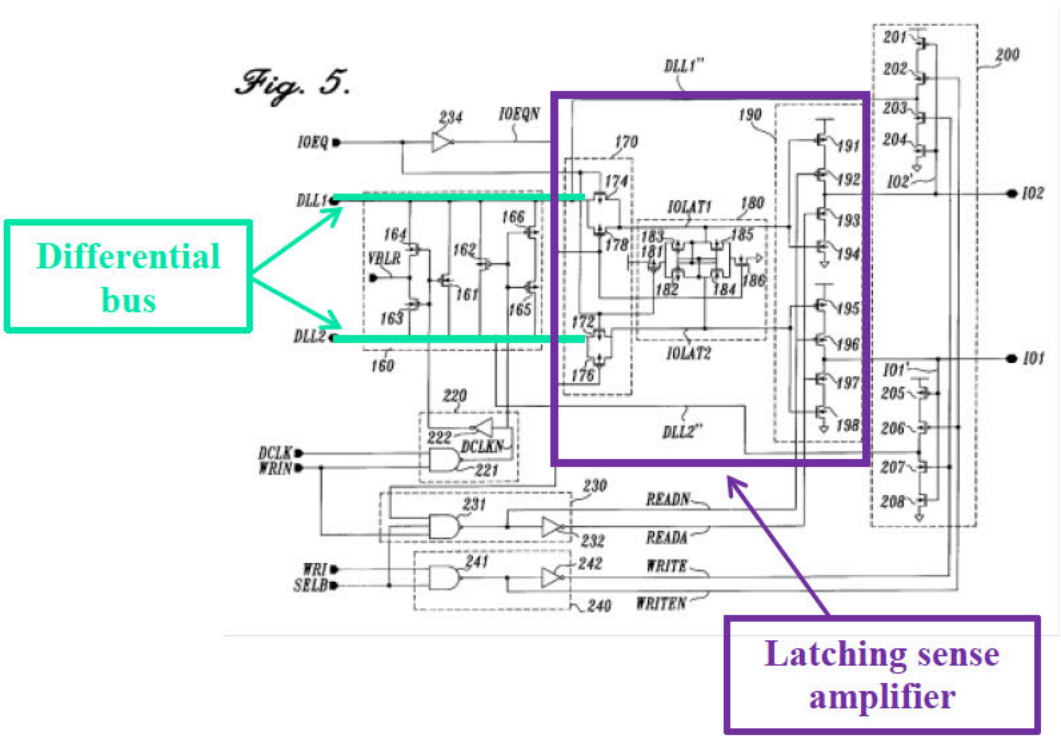


Ex. 1004, p. 68 (declaration of Dr. Philip Koopman submitted by Patent Owner; alleged differential bus LT and LC precedes sense amplifier 16).

The bus drivers are coupled to the differential bus (i.e., lines DLL1 and DLL2), shown in annotated Fig. 3 above, as the outputs of that figure. *See*, *e.g.*, Ex. 1002, ¶ 31; *Ternullo* 7:13-18. The differential bus (i.e., lines DLL1 and DLL2) is also coupled to the voltage precharge source VBLR because "when control signal DCLKD is high and signal DCLKN is low, NFET transistor 161 and PFET transistor 162 couple line DLL1 to line DLL2, while NFET transistors 163 and 164 and PFET transistors 165 and 166 *couple* the lines DLL1 and DLL2 to the midlevel voltage source VBLR." *Ternullo* 8:28-32 (emphasis added), 10:35-40; *see also, e.g.*, Ex. 1002, ¶ 31. The DLL1 and DLL2 indicated in Fig. 3 is the same DLL1 and DLL2 indicated in Fig. 5 respectively. *See, e.g.*, Ex. 1002, ¶ 31; *Ternullo* Figs. 1-5.

v. "a latching sense amplifier coupled to the differential bus;"

Ternullo discloses a latching sense amplifier (shown below in purple) coupled to the differential bus DLL1 and DLL2. *See, e.g.*, Ex. 1002, ¶ 31; *Ternullo* Fig. 5 (annotated below).

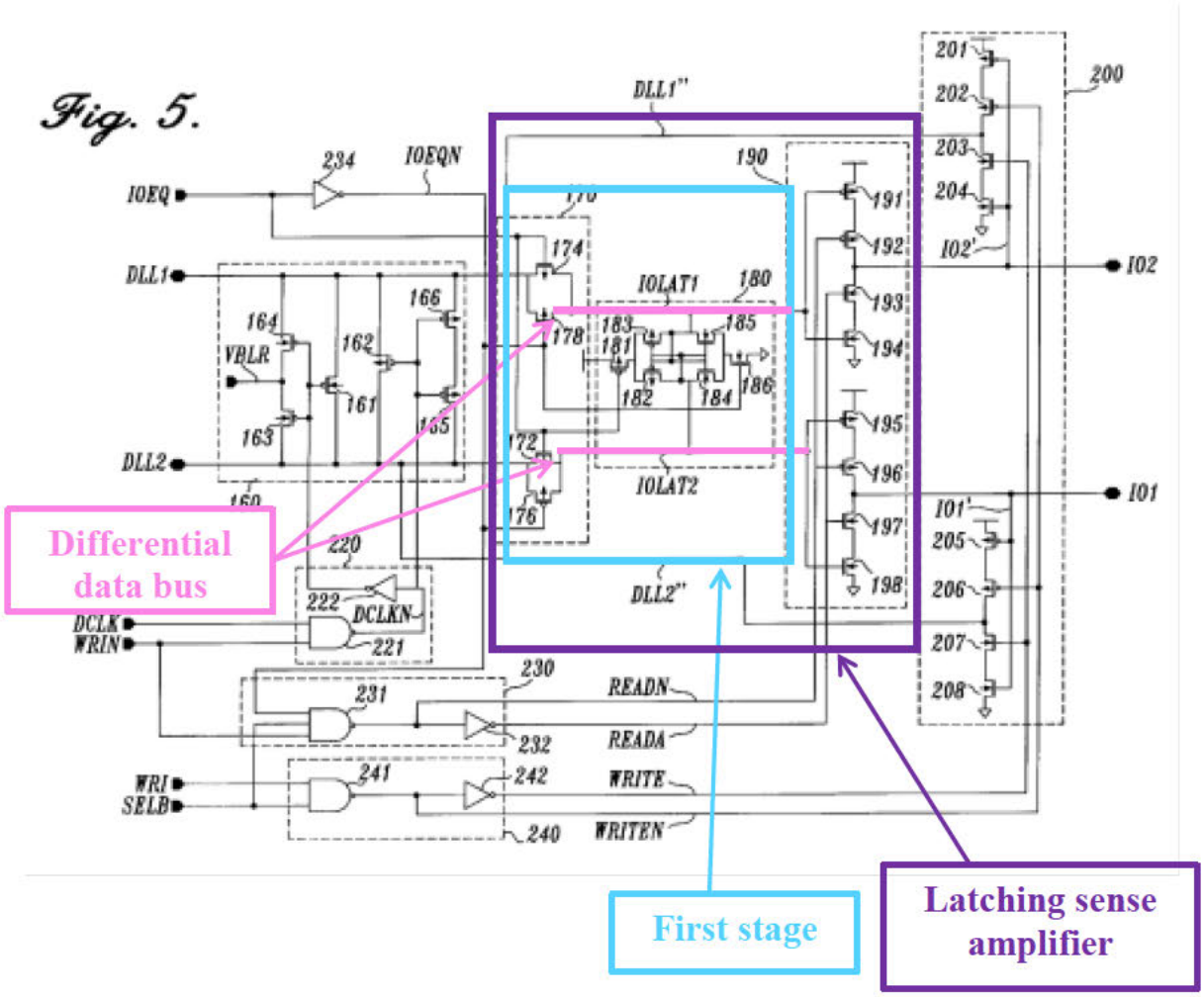


Consistent with Petitioner's proposed construction of "latching sense amplifier," the circuitry identified above in annotated Fig. 5 of *Ternullo* is a circuit, including a latch, that detects and amplifies signals. *See, e.g.*, Ex. 1002, ¶ 31. Input/output latch 180 provides a latch that detects and amplifies the signal on DLL1 and DLL2 received through isolation circuit 170. *See, e.g.*, Ex. 1002, ¶ 31; *Ternullo* 7:58-8:3, 8:51-55, 10:46-49.

Regarding the operation of *Ternullo*'s latching sense amplifier, *Ternullo* discloses that "[w]hen NFET transistor 186 is biased on by a high on control signal IOEQN and when PFET transistor 181 is biased on by a low on control signal IOEQ, the input/output latch 180 is turned on. Once the input/output latch 180 is turned on, when a high or low signal appears on either of the lines IOLAT1 or IOLAT2, the other line IOLAT1 or IOLAT2 is correspondingly driven to the opposite state by the function of the latch." *Ternullo* 8:48-55; *see also, e.g.*, Ex. 1002, ¶ 31.

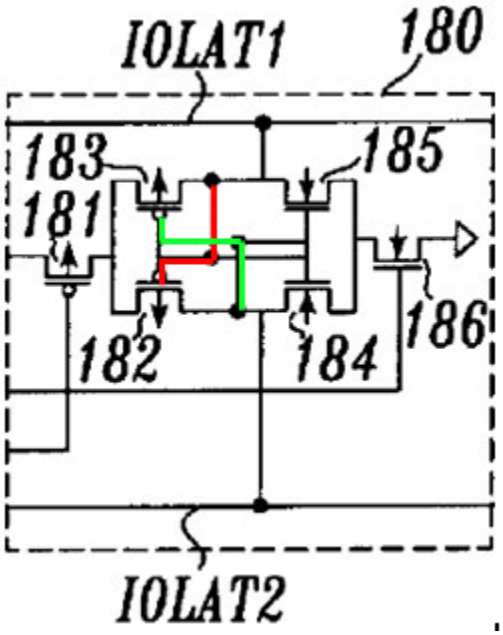
vi. "wherein the latching sense amplifier comprises: a first stage including a cross-coupled latch coupled to a differential data bus; and"

Ternullo teaches that the latching sense amplifier (shown below in purple) includes a first stage (shown below in light blue) with a cross-coupled latch coupled to a differential data bus (i.e., lines IOLAT1 and IOLAT2). *See, e.g.*, Ex. 1002, ¶ 31; *Ternullo* Fig. 5 (annotated).



As indicated above, the circuitry identified as the first stage includes isolation circuit 170 and input/output latch 180. Ex. 1002, ¶ 31. Consistent with Petitioner's proposal that "stage" be construed to mean "portion of a circuit," the elements identified as the "first stage" are a portion of the latching sense amplifier circuit. Ex. 1002, ¶ 31. In particular, isolation circuit 170 passes the differential voltage on DLL1 and DLL2 to input/output latch 180, which eventually latches and amplifies the differential voltage. *See, e.g.*, *Ternullo* 7:58-8:3, 8:48-55, 10:35-43; Ex. 1002, ¶ 31.

Input/output latch 180 is a cross-coupled latch because the output of a first transistor is tied to the input of a second transistor, and the output of the second transistor is tied to the input of the first transistor. Ex. 1002, ¶ 31. Annotated Fig. 5 of *Ternullo* below[7] discloses the cross-coupling (*see also, e.g.*, Ex. 1002, ¶ 31):



[7] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that input/output latch 180 in Fig. 5 is mistakenly drawn incorrectly. *See, e.g.*, Ex. 1002, ¶ 31. Indeed, *Ternullo* notes "input/output latch operate[s] similarly to … data line latch 80 in FIG. 2" (*Ternullo* 7:63-65), and data line latch 80, as further disclosed in *Ternullo* Fig. 3, is drawn correctly without the transistor gates connected to each other (*see, e.g.*, *Ternullo* Fig. 3, 6:52-67; Ex. 1002, ¶ 31).

Further, one of ordinary skill in the art would have recognized at the time of the alleged invention of the ’130 Patent that IOLAT1 and IOLAT2 represent the “differential data bus” because it represents an amplified voltage differential representative of the data to be read out by the latching sense amplifier. *See*, *e.g.*, *Ternullo* 8:45-55; Ex. 1002, ¶ 31. Indeed, one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have understood IOLAT1 and IOLAT2 to include differential data because of the amplified voltage differential on these lines. Ex. 1002, ¶ 31.

vii. “an output stage coupled to an output of said first stage; wherein the output of the first stage is coupled to an input of the output stage;”

As shown below in an annotated version of Fig. 5, *Ternullo* discloses a latching sense amplifier (shown below in purple) with an output stage (shown below in orange) coupled to an output of its first stage (shown below in light blue), wherein the output of the first stage is coupled to an input of the output stage. *See*, *e.g.*, Ex. 1002, ¶ 31; *Ternullo* Fig. 5.

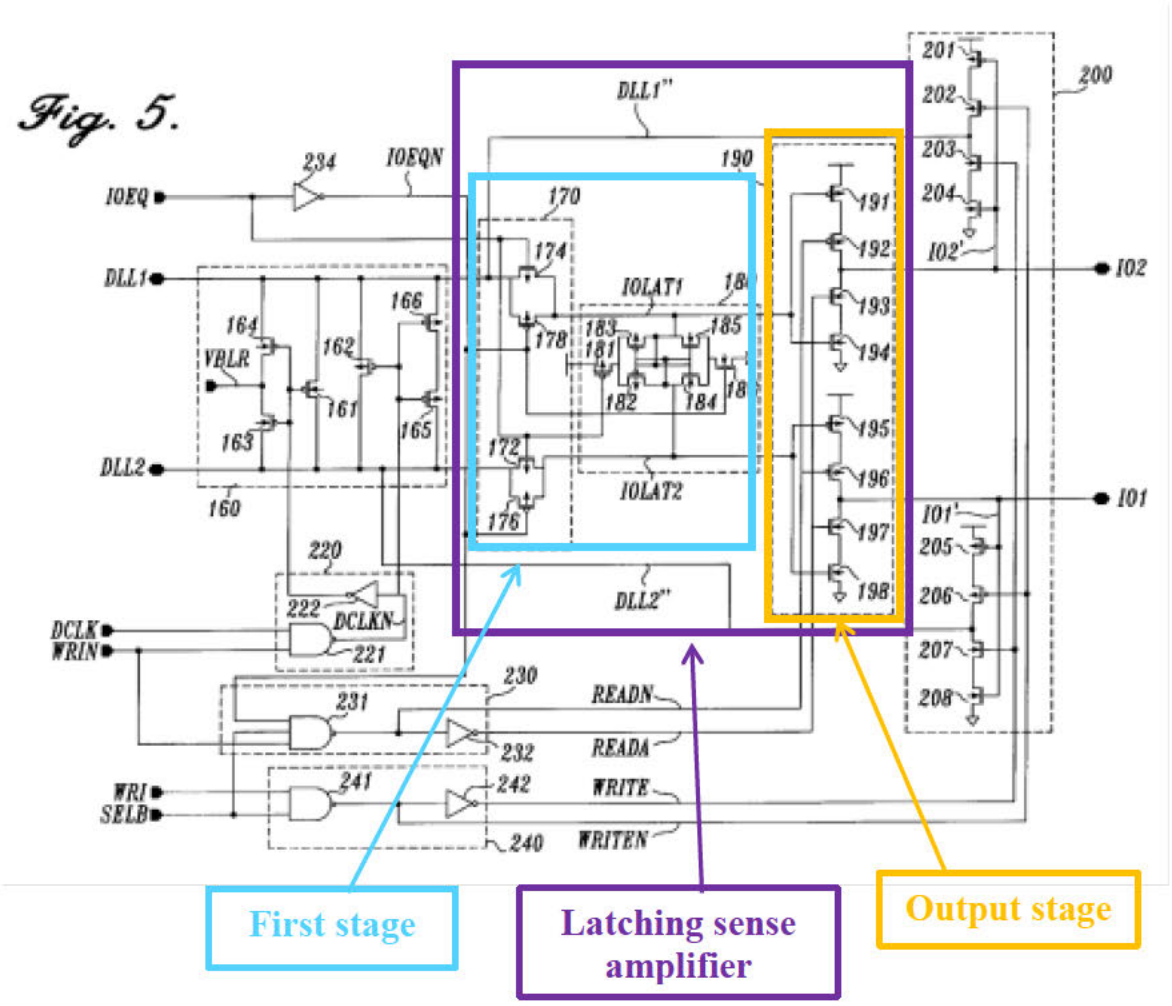
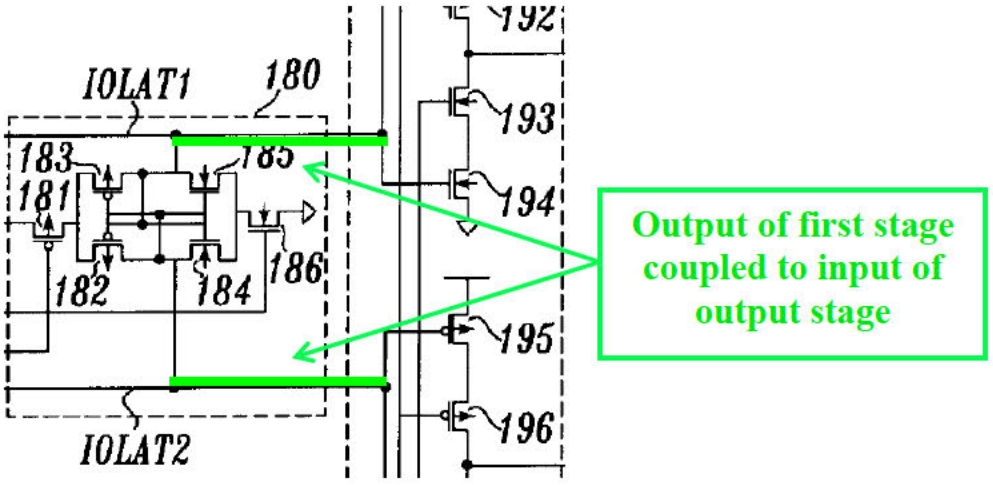


Fig. 5.
DLL1"
IOEQN
IOEQ
DLL1
DLL2
VBLR
IOLAT1
IOLAT2
DLL2"
DCLK
WRIN
DCLKN
READN
READA
WRI
SELB
WRITE
WRITEN
IO2
IO1
First stage
Latching sense amplifier
Output stage


IOLAT1
IOLAT2
Output of first stage coupled to input of output stage

As indicated above, the circuitry identified as the output stage includes read drivers 190. *See, e.g.*, *Ternullo* 8:56-67; Ex. 1002, ¶ 31. Consistent with Petitioner's proposal that "stage" be construed to mean "portion of a circuit," the elements identified as the "output stage" are a portion of the latching sense amplifier circuitry. Ex. 1002, ¶ 31. In particular, the identified "output stage" performs the particular function of driving the output of *Ternullo*'s latching sense amplifier. *See, e.g.*, Ex. 1002, ¶ 31; *Ternullo* 8:7-10, 8:56-62.

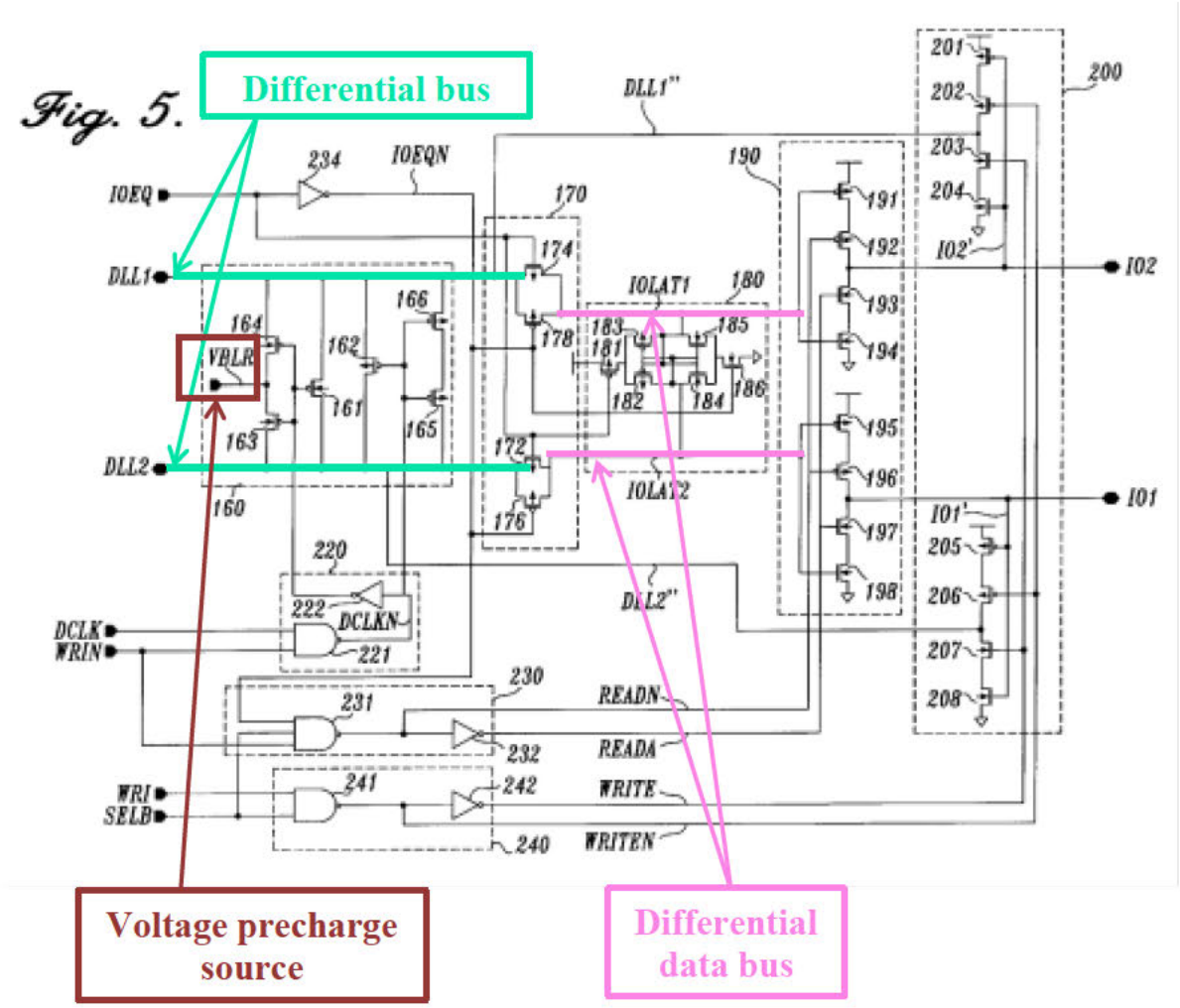
viii. "wherein the differential bus and the differential data bus are precharge to a voltage Vpr between Vdd and ground, where Vpr = K*Vdd, and K is a precharging voltage factor."

Ternullo discloses the differential bus DLL1 and DLL2 and differential data bus IOLAT1 and IOLAT2 are precharged to a voltage Vpr between Vdd and ground. *See, e.g.*, Ex. 1002, ¶ 31; *Ternullo* Fig. 5. As discussed above (*see supra* Section VII.B.1.iv), the differential bus is precharged to the midlevel voltage VBLR (i.e., a voltage between Vdd and ground) due to the precharge voltage source VBLR:

> "FIG. 5 illustrates a practical implementation of the circuit of FIG. 4. As shown in FIG. 5, equalizing circuit 160 includes NFET transistors 161, 163, and 164, and PFET transistors 162, 165, and 166. Equalizing circuit 160 is constructed and operates similarly to equalizing circuit 60 of FIG. 2. Thus, when control signal DCLKD

is high and signal DCLKN is low, NFET transistor 161 and PFET transistor 162 couple line DLL1 to line DLL2, while NFET transistors 163 and 164 and PFET transistors 165 and 166 couple the lines DLL1 and DLL2 to the *midlevel voltage source VBLR*."

Ternullo 8:23-33 (emphasis added), Fig. 5 (annotated below); *see also, e.g.*, Ex. 1002, ¶ 31.

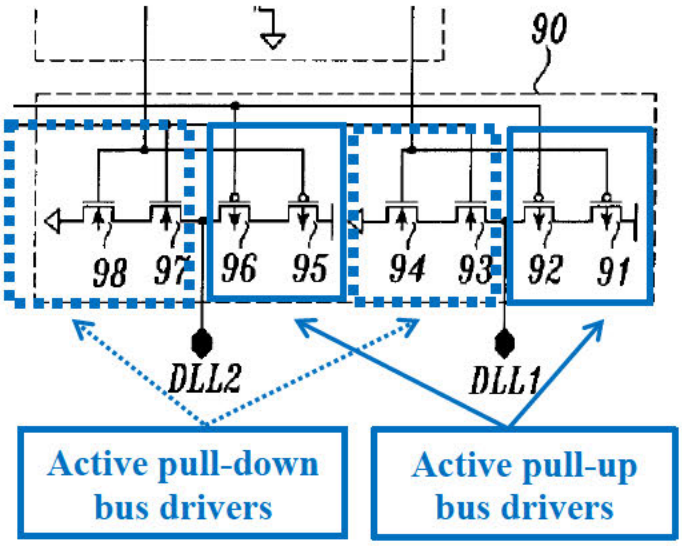


Moreover, *Ternullo* discloses that the differential data bus (IOLAT1 and IOLAT2) is also precharged to midlevel voltage VBLR, as the voltage VBLR applied to the differential bus is passed to the differential data bus through isolation circuit 170. *See, e.g.*, *Ternullo* 5:24-27, 6:21-51, 8:34-42, 8:45-55; *see also, e.g.*, Ex. 1002, ¶ 31.

2. Claim 2

i. "The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers."

Ternullo discloses bus drivers that comprise of active pull-up and pull-down bus drivers. *See, e.g.*, Ex. 1002, ¶ 32; *Ternullo* Figs. 3, 5. As annotated below in *Ternullo* Fig. 3:



Ternullo teaches that the bus drivers comprise of active pull-up drivers because PMOS transistors 91, 92, 95, and 96 may couple the outputs DLL1 and DLL2 to

Vdd (indicated by the flat line to the right of transistors 91 and 95) and thus pull up the output. *See, e.g., Ternullo* 7:15-37; Ex. 1002, ¶ 32. Likewise, *Ternullo* teaches that the bus drivers comprise of active pull-down drivers as NMOS transistors 93, 94, 97, and 98 may couple DLL1 and DLL2 to ground (indicated by the triangle to the left of transistors 94 and 98) and thus pull down the outputs. *See, e.g., Ternullo* 7:15-37; Ex. 1002, ¶ 32.

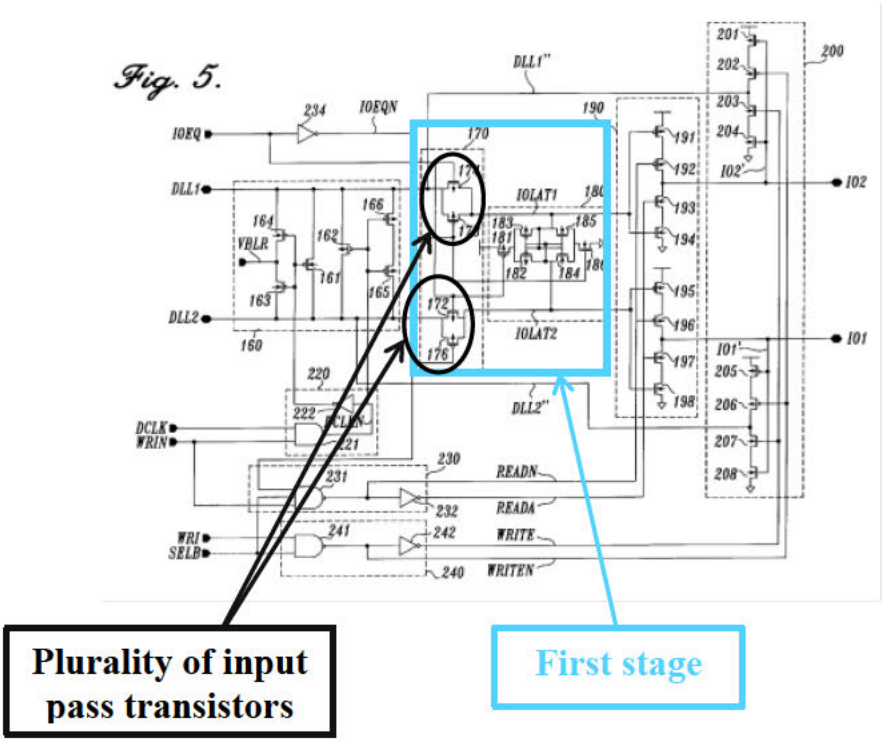
3. Claim 3

i. "The data transfer arrangement in accordance with claim 1,:"

As discussed above, *Ternullo* discloses a data transfer arrangement in accordance with claim 1. *See supra* Section VII.B.1; Ex. 1002, ¶ 31.

ii. "wherein the first stage of the latching sense amplifier comprises: a plurality of input pass transistors each having a gate, a source terminal, and a drain; and"

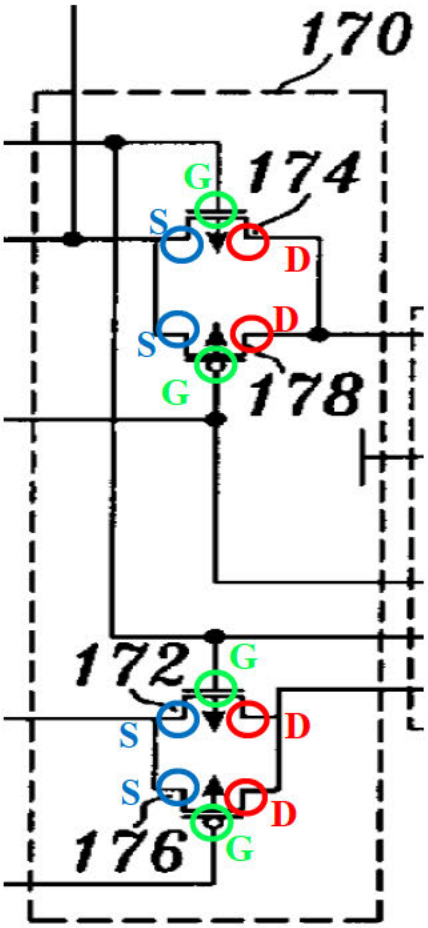
Ternullo teaches that the first stage (shown below in light blue) comprises of a plurality of input pass transistors each having a gate, source, and drain. *See, e.g.*, Ex. 1002, ¶ 33; *Ternullo* Fig. 5 (annotated below).



Transistors 172, 174, 176, and 178 in *Ternullo*'s isolation circuit 170 act as input pass transistors because they pass the voltages from DLL1 and DLL2 to IOLAT1 and IOLAT2, respectively. *See, e.g.*, *Ternullo* 8:37-42; *see also, e.g.*, Ex. 1002, ¶ 33.

One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the gate, source, and drain of the input pass transistors are as indicated below in annotated Fig. 5 of *Ternullo* (sources in blue circles; drains in red circles; gates in green circles)[8]:

[8] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the sources and drains for



See also, e.g., Ex. 1002, ¶ 33.

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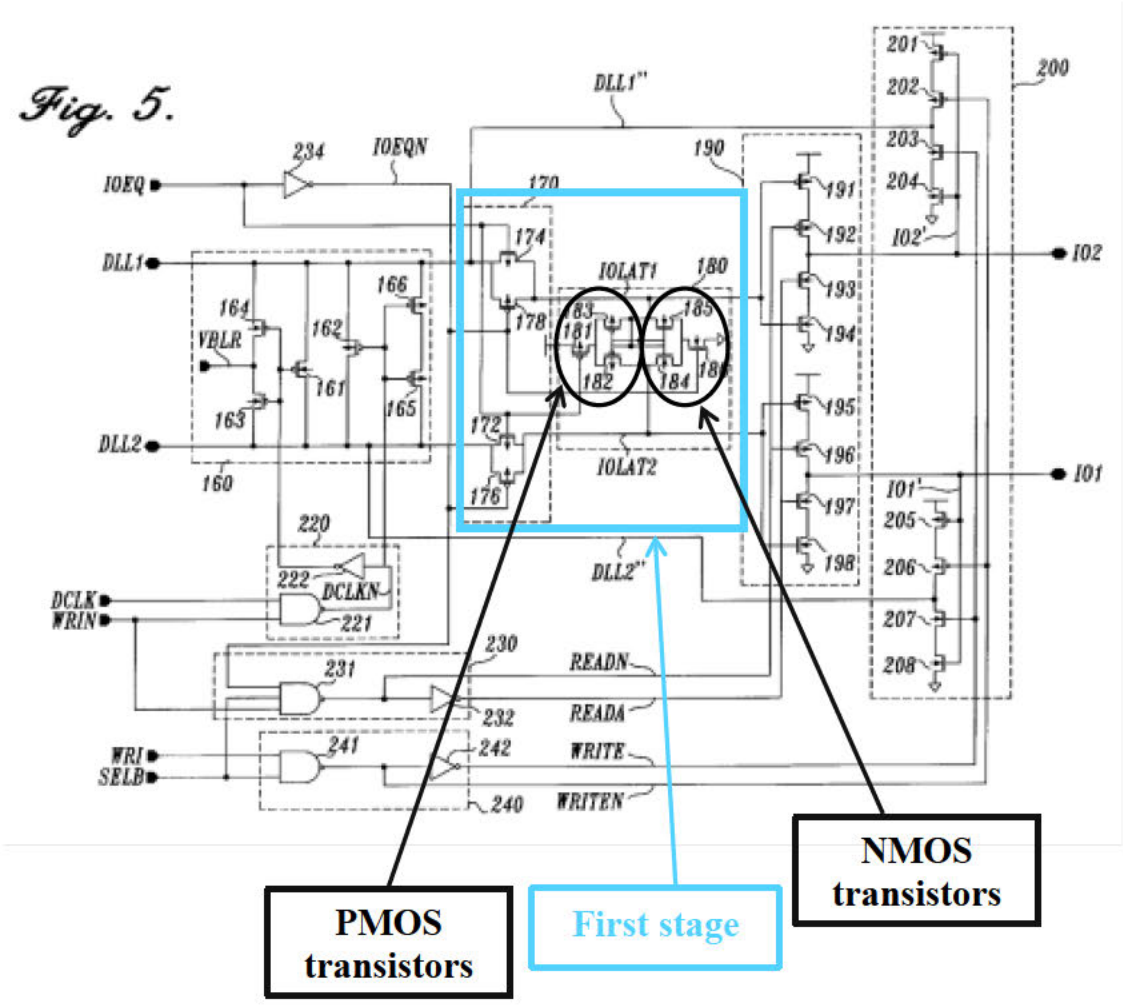
the input pass transistors is dependent on the voltage provided to the transistors through DLL1 and DLL2. Nonetheless, the identification of the sources and drains in annotated Fig. 5 of *Ternullo* is consistent with the '130 Patent's specification and identification of sources and drains for the claimed input pass transistors. *See, e.g.*, Ex. 1002 ¶ 33, n.1.

iii. "a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain; and"

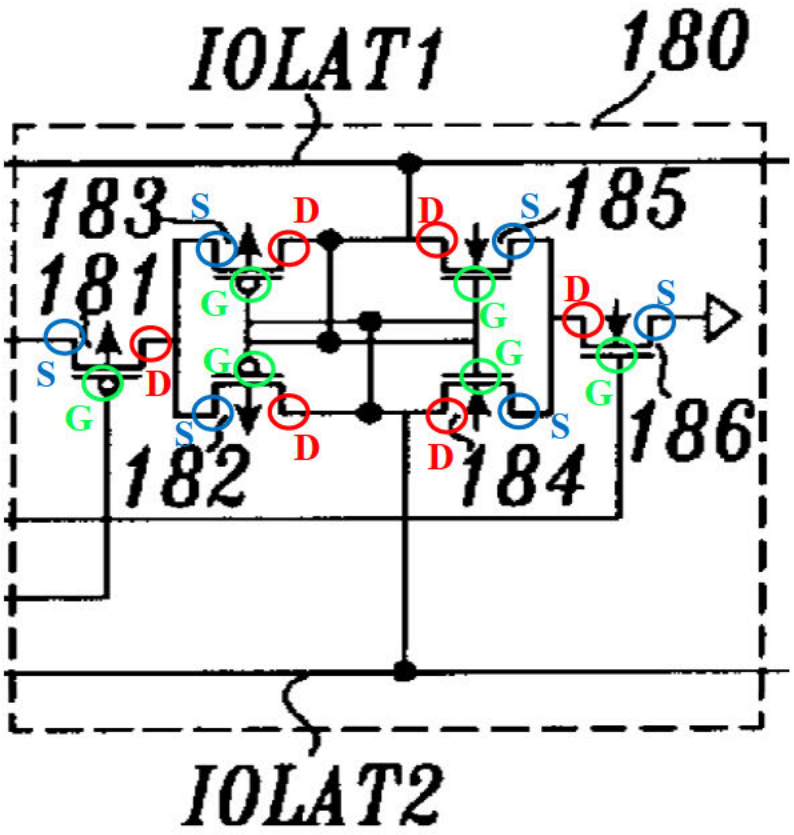
Ternullo teaches that the first stage (shown below in light blue) comprises of a plurality of NMOS and PMOS transistors each having a gate, source, and drain. *See, e.g.*, Ex. 1002, ¶ 33; *Ternullo* Fig. 5 (annotated below).



Ternullo discloses that "[i]nput/output latch 180 includes *PFET transistors 181, 182 and 183 and NFET transistors 184, 185 and 186*."[9] *Ternullo* 8:45-46 (emphasis added); *see also, e.g.*, Ex. 1002, ¶ 33.

One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the gate, source, and drain of the NMOS and PMOS transistors are as indicated below in annotated Fig. 5 of *Ternullo* (sources in blue circles; drains in red circles; gates in green circles):

[9] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that a p-channel MOSFET was often referred to as PFET or PMOS and that an n-channel MOSFET was often referred to as NFET or NMOS. *See* Ex. 1002, ¶ 33, n.2.



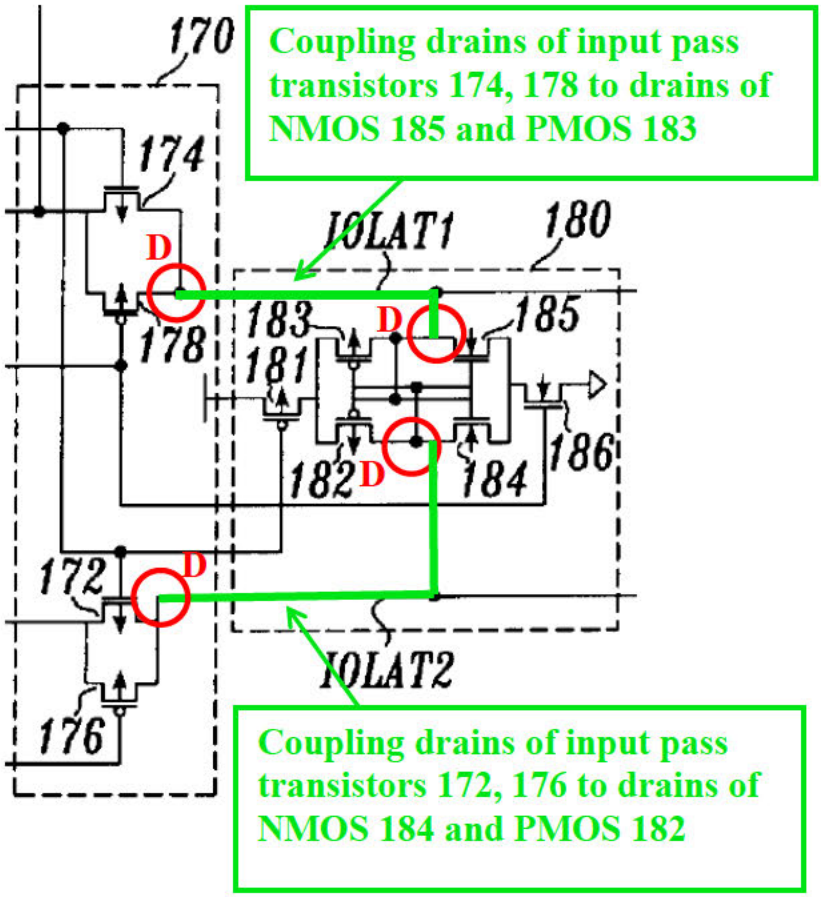
See also, e.g., Ex. 1002, ¶ 33.

iv. "wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors,

Ternullo discloses a first stage of a latching sense amplifier wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors. *See, e.g.*, Ex. 1002, ¶ 33. *Ternullo* teaches that "[i]solation circuit 170 includes NFET transistors 172 and 174 and PFET transistors 176 and 178. Isolation circuit 170 is constructed and operates similarly to isolation circuit 70 in FIG. 2. Thus, when NFET transistors 172 and 174 are biased on by a high signal on control signal IOEQ, and PFET transistors

176 and 178 are biased on by a low signal on control signal IOEQN, *lines DLL1 and DLL2 are coupled to the input/output latch lines IOLAT1 and IOLAT2*, respectively." *Ternullo* 8:34-42 (emphasis added); *Ternullo* Fig. 5 (drains in red circles; annotated below).[10]

[10] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the drains for the input pass transistors is dependent on the voltage provided to the transistors through DLL1 and DLL2. Nonetheless, the identification of the drains in annotated Fig. 5 of *Ternullo* is consistent with the '130 Patent's specification and identification of drains for the claimed input pass transistors. *See, e.g.*, Ex. 1002 ¶ 33, n.3.

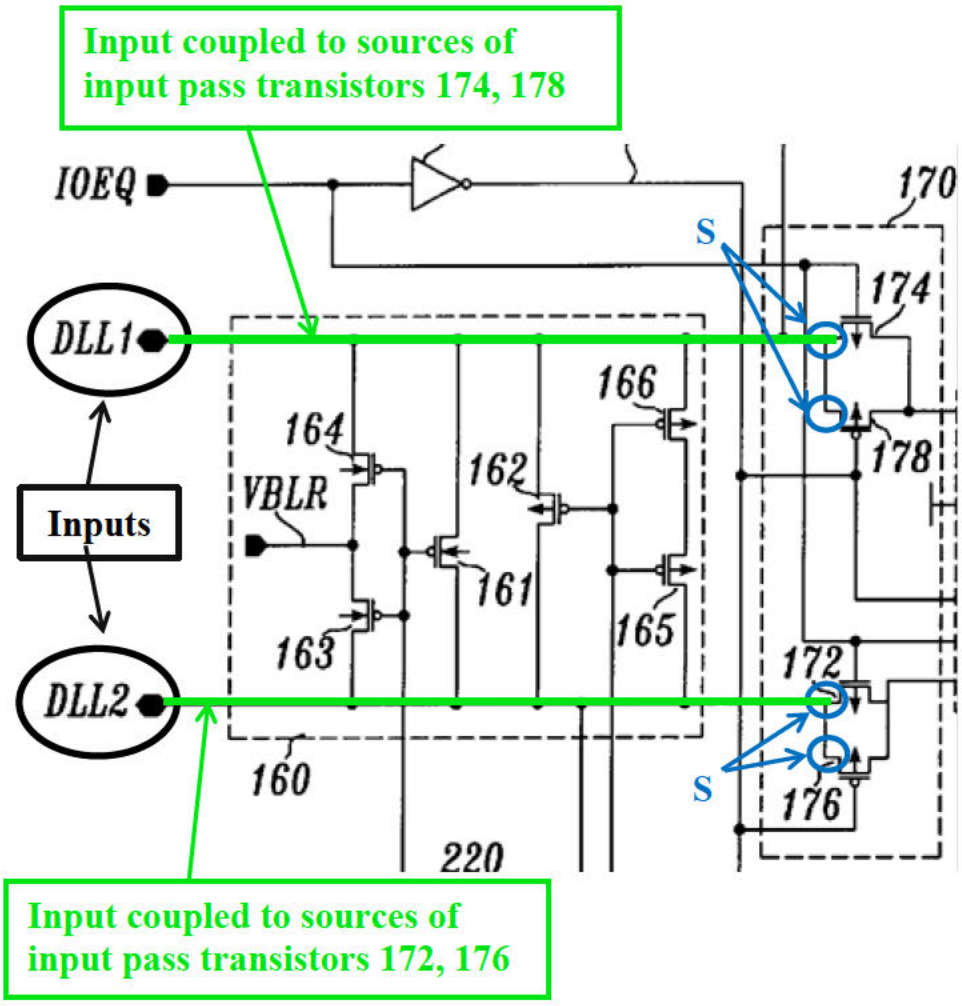


See also, e.g., Ex. 1002, ¶ 33.

v. each source terminal of the input pass transistor is coupled to an input,

Ternullo discloses a first stage of a latching sense amplifier wherein each source terminal of the input pass transistors is coupled to an input. *See, e.g.*, Ex. 1002, ¶ 33; *Ternullo* Fig. 5 (sources in blue circles; annotated below).[11]

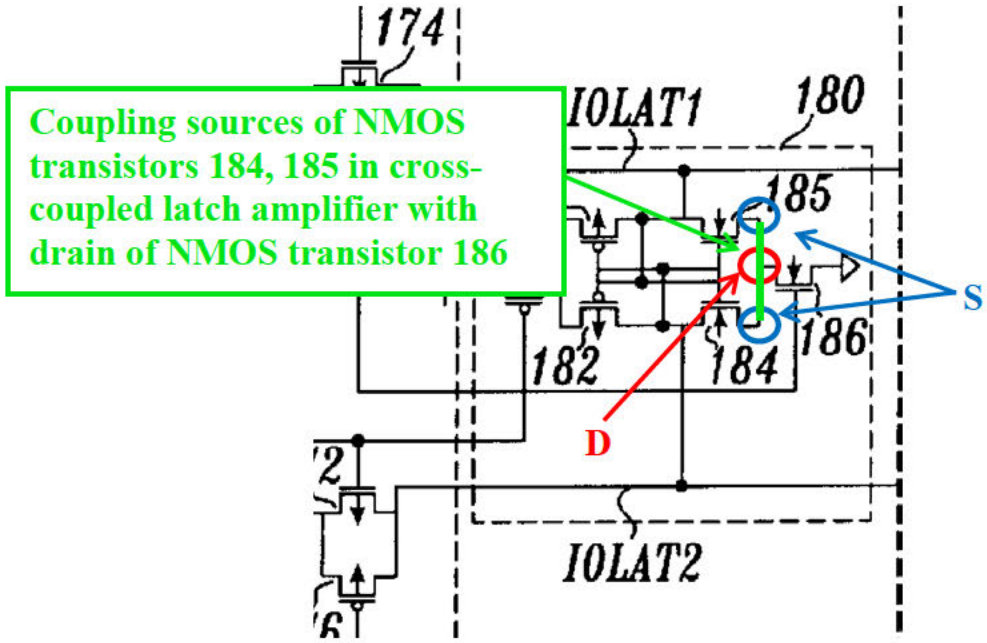
[11] One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that the identification of the sources for the input pass transistors is dependent on the voltage provided to the transistors through



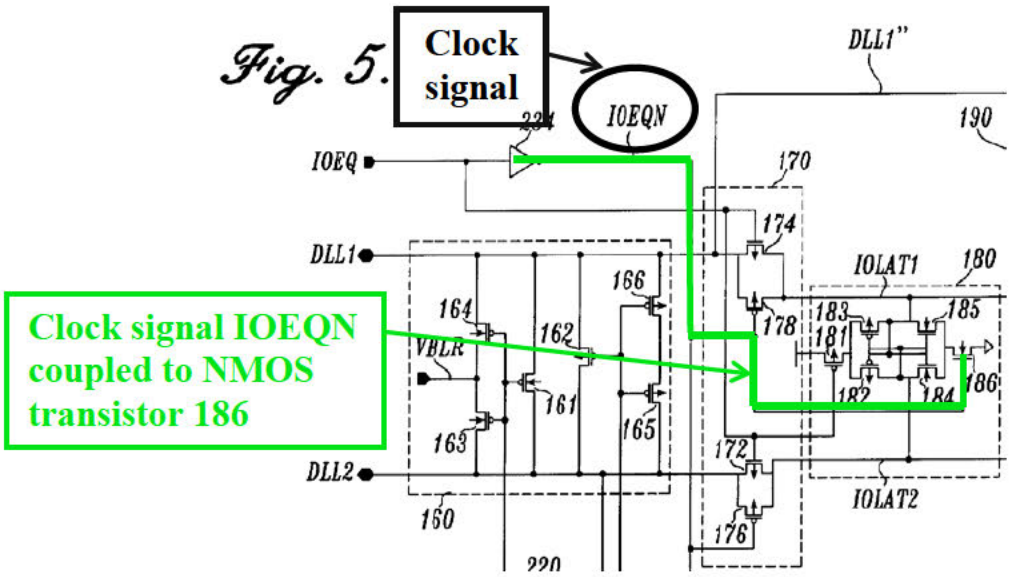
DLL1 and DLL2. Nonetheless, the identification of the sources in annotated Fig. 5 of *Ternullo* is consistent with the '130 Patent's specification and identification of sources for the claimed input pass transistors. *See, e.g.*, Ex. 1002 ¶ 33, n.4.

vi. the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor coupled to a clock signal input, and

Ternullo discloses a first stage of a latching sense amplifier wherein the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor. *See, e.g.*, Ex. 1002, ¶ 33; *Ternullo* Fig. 5 (sources in blue circles; drains in red circles; annotated below).

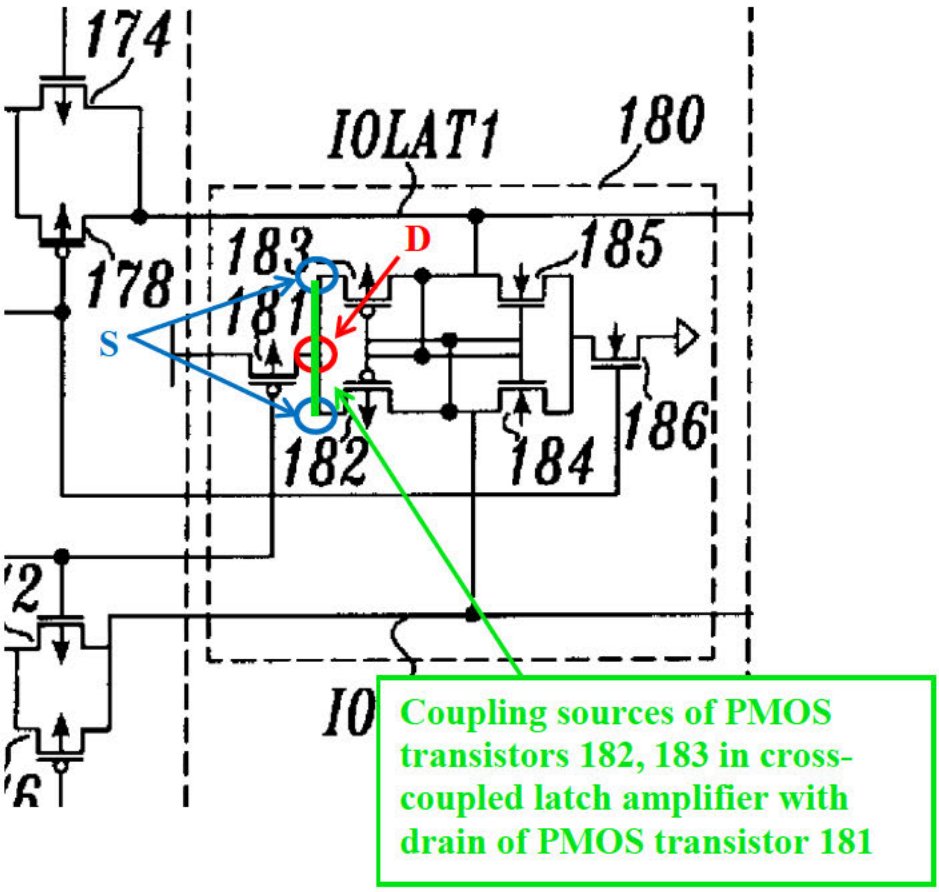


Ternullo further teaches that NMOS transistor 186 is coupled to a clock signal input IOEQN. *See, e.g.*, *Ternullo* 8:48-51, 12:41-44, 15:14-23, Fig. 5 (annotated below); Ex. 1002, ¶ 33.

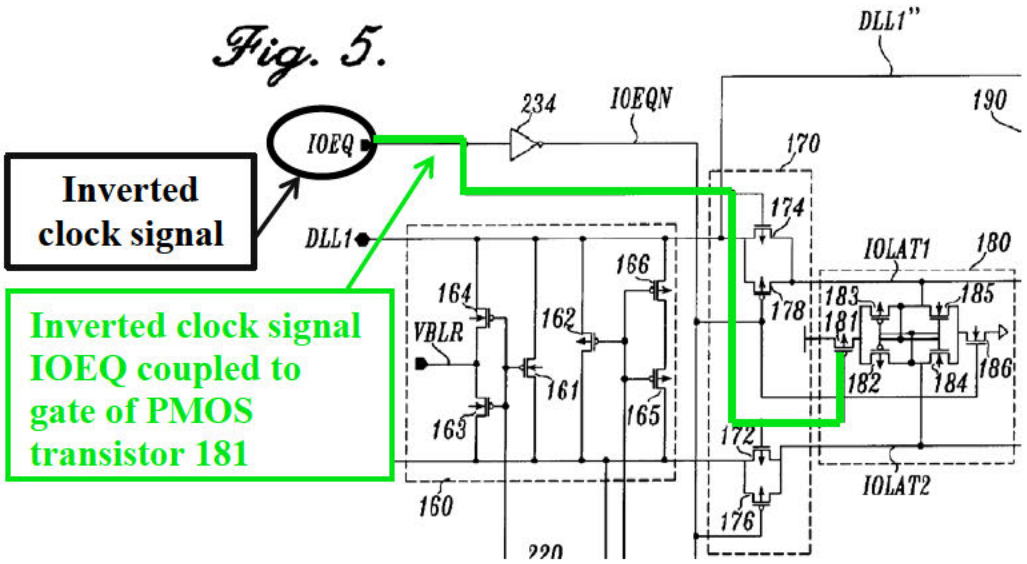


vii. the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input."

Ternullo discloses a first stage of a latching sense amplifier wherein the sources of the cross-coupled latch amplifier PMOS transistors are coupled to the drain of the PMOS transistor. *See, e.g.*, Ex. 1002, ¶ 33; *Ternullo* Fig. 5 (sources in blue circles; drains in red circles; annotated below).



Ternullo teaches that PMOS transistor 181 is coupled to an inverted clock signal input IOEQ. *See, e.g.*, *Ternullo* 8:48-51, 12:41-44, 15:14-23, Fig. 5 (annotated below); Ex. 1002, ¶ 33.



4. Claim 5

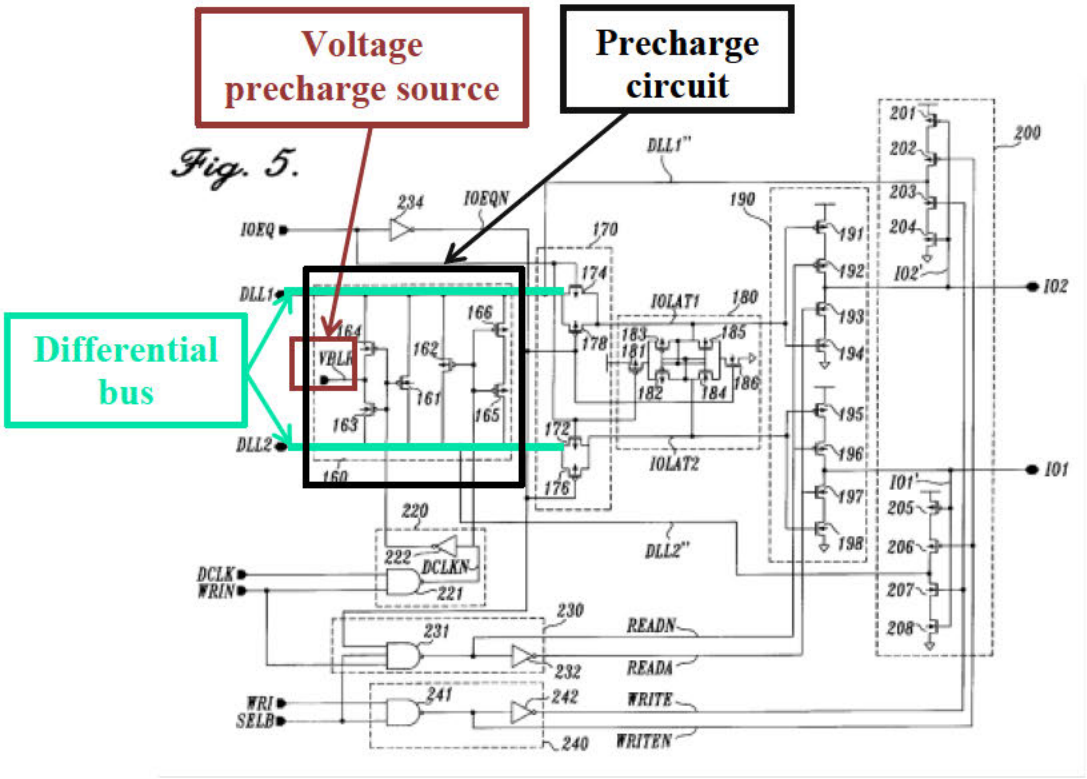
i. "The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage."

Ternullo teaches that the differential bus DLL1 and DLL2 get precharged to a voltage less than a logic high and greater than a logic low as the bus lines are precharged to an intermediate voltage VBLR (i.e., the voltage precharge source). *See, e.g.*, *Ternullo* 8:23-33 ("Thus, when control signal DCLKD is high and signal DCLKN is low, NFET transistor 161 and PFET transistor 162 couple line DLL1 to line DLL2, while NFET transistors 163 and 164 and PFET transistors 165 and 166 couple the lines DLL1 and DLL2 to the *midlevel voltage source VBLR*.") (emphasis added); Ex. 1002, ¶ 34.

5. Claim 6

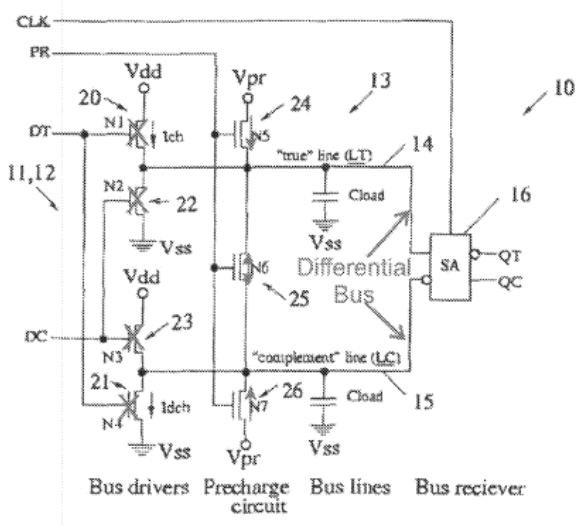
i. "The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus."

Ternullo's equalization circuit 160 serves as a precharge circuit coupled between the precharge source VBLR and the differential bus DLL1 and DLL2. *See, e.g.*, Ex. 1002, ¶ 35; *Ternullo* Figs. 4, 5 (annotated below).



Equalization circuit 160 provides circuitry that precharges the differential bus to the midlevel voltage VBLR: "equalizing circuit 160 includes NFET transistors 161, 163, and 164, and PFET transistors 162, 165, and 166. Equalizing circuit 160 is constructed and operates similarly to equalizing circuit 60 of FIG. 2. Thus, when

control signal DCLKD is high and signal DCLKN is low, NFET transistor 161 and PFET transistor 162 couple line DLL1 to line DLL2, while NFET transistors 163 and 164 and PFET transistors 165 and 166 couple the lines DLL1 and DLL2 to the midlevel voltage source VBLR." *Ternullo* 8:24-33; *see also, e.g., id.* 7:50-57; Ex. 1002, ¶ 35. The precharge circuit is between the voltage precharge source and the differential bus because the transistors within the precharge circuit connect the voltage precharge source to the differential bus. *See, e.g., Ternullo* 8:24-33; Ex. 1002, ¶ 35. This is consistent with the '130 Patent's disclosure and the Patent Owner's characterization of the disclosure during reexamination:



Ex. 1004, p. 68 (declaration of Dr. Philip Koopman disclosing precharge circuit 13 and the "differential bus"); Ex. 1002, ¶ 35.

C. Ground 2: *Ternullo* and *Hardee* Render Claim 7 Obvious

i. "7. The data transfer arrangement in accordance with claim 2 wherein the active pull up and active pull down bus drivers are NMOS transistors."

While *Ternullo* discloses active pull up drivers that are NMOS transistors, it does not expressly disclose active pull down drivers that are NMOS transistors. However, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have found it obvious to use NMOS transistors for pull up and pull down bus drivers in light of *Hardee*. *See, e.g.*, Ex. 1002, ¶¶ 37-40. It was well known at the time of the alleged invention of the '130 Patent that active pull up and pull down bus drivers could be designed with NMOS transistors, as demonstrated, for example, by Fig. 5 of *Hardee*, annotated below:

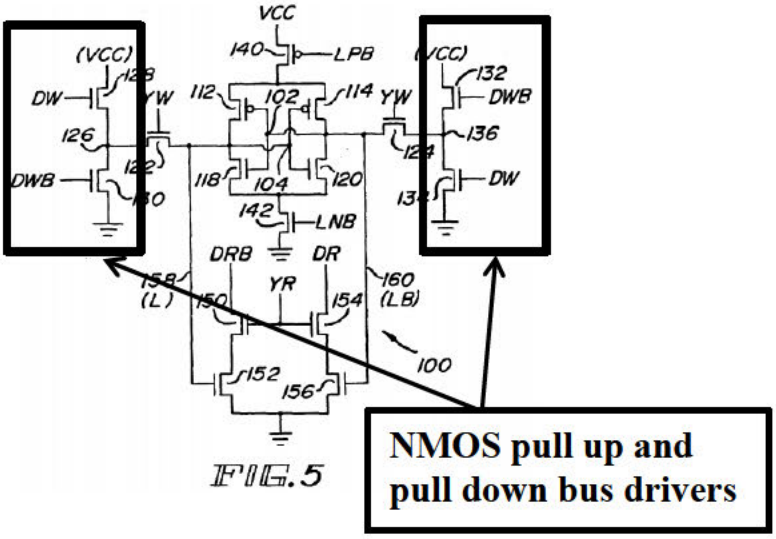


FIG. 5

See also, e.g., *Hardee* 6:28-46; Ex. 1002, ¶ 38. Given the teachings of *Hardee*, which is in the same field of technology as *Ternullo* (*see supra* Section VII.A), one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have been motivated to reconfigure the circuit and bus drivers in *Ternullo* with NMOS pull up and pull down bus drivers to reduce the layout area and avoid latch-up. *See, e.g.*, Ex. 1002, ¶ 39. A smaller layout size can be important when connecting the drivers up to an array of transistors, as used in a memory, or when driving a parallel data bus where the data signals are laid out directly adjacent to each other. *See, e.g.*, Ex. 1002, ¶ 39. A smaller layout size is achieved with NMOS transistors as it eliminates the need for the n-well used in the construction of PMOS transistors. *See, e.g.*, Ex. 1002, ¶ 39.

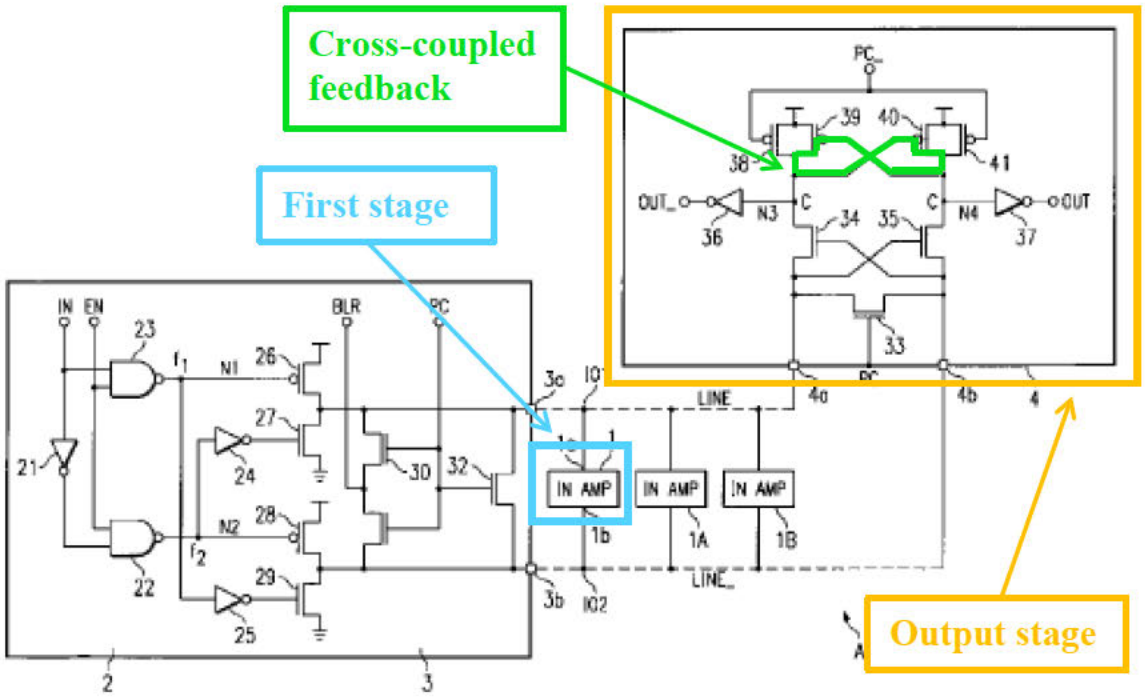
Further, modifying the PMOS transistors in the bus drivers with NMOS transistors allows the driver to become immune to latch-up. *See, e.g.*, Ex. 1002, ¶ 39. One skilled in the art at the time of the alleged invention of the ’130 Patent would have been motivated to avoid latch-up as latch-up causes a wire to short circuit to a power supply Vdd (i.e., Vcc) or ground. *See, e.g.*, Ex. 1002, ¶ 39. Avoiding latch-up is especially important when driving a signal off-chip, where the driver is connected to a bonding wire which is inductive and thus can produce ringing voltages. *See, e.g.*, Ex. 1002, ¶ 39.

Moreover, implementing pull up and pull down bus drivers using solely NMOS transistors in *Ternullo* is merely a design choice that one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have certainly understood. *See, e.g.*, Ex. 1002, ¶ 40. This follows from the fact that there were a small finite number of MOSFET configurations for implementing pull up and pull down bus drivers (e.g., NMOS, PMOS, or CMOS – both NMOS and PMOS). *See, e.g.*, Ex. 1002, ¶ 40. Indeed, doing so amounts to nothing more than using a known technique to improve similar devices in the same way and yields nothing more than predictable results. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

D. Ground 3: *Ternullo* and *Sukegawa* Render Claim 9 Obvious

i. “9. The data transfer arrangement of claim 1 wherein the output stage includes cross-coupled feedback.”

While *Ternullo* discloses an output stage, it does not expressly disclose an output stage with cross-coupled feedback. But one of ordinary skill in the art at the time of the alleged invention of the ’130 Patent would have found it obvious to use an output stage with cross-coupled feedback in light of *Sukegawa*. *See, e.g.*, Ex. 1002, ¶¶ 42-44. It was well known at the time of the alleged invention of the ’130 Patent to include cross-coupled feedback in an output stage of a latching sense amplifier, as demonstrated, for example, by annotated Fig. 1 of *Sukegawa*:



See also, e.g., *Sukegawa* 5:5-12; Ex. 1002, ¶ 43. The cross-coupled feedback identified above is consistent with the "cross-coupled feedback" identified by the Patent Owner during *inter partes* reexamination. Ex. 1002, ¶ 43. In particular, Patent Owner argued that "cross-coupled feedback" was demonstrated by Fig. 2 of the '130 Patent, which is nearly (if not entirely) identical with Petitioner's mapping of *Sukegawa*:

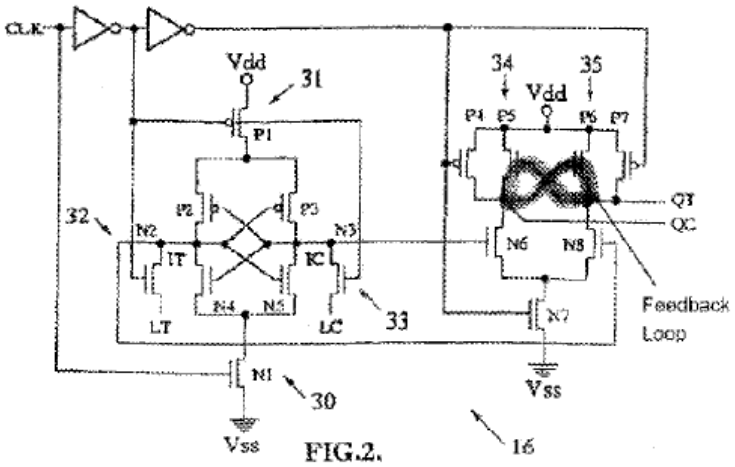


FIG.2.

Ex. 1004, p. 127; *see also* Ex. 1002, ¶ 43. Patent Owner argued that "feedback' should be construed to mean "a loop in the topography of a circuit where, in addition to its input being connected to its output, its output is also connected to its input via a different path." Ex. 1004, p. 126. The circuit in *Sukegawa* meets this definition as the output C above transistor 34 is tied to the input gate of transistor 40 and the output C above transistor 35 is tied to the input gate of transistor 39. Ex. 1002, ¶ 43; *see also, e.g.*, *Sukegawa* 8:59-64, Fig. 1. Indeed, this identical circuitry disclosed by Fig. 2 of the '130 Patent was not only sufficient to satisfy the "feedback" limitation of claim 9, but also the additional limitation that the feedback must be "cross-coupled." Ex. 1004, pp. 126-27, 139-40. Accordingly, *Sukegawa* discloses cross-coupled feedback like that recited in the claim. Ex. 1002, ¶ 43; *see also, e.g.*, *Sukegawa* 8:59-64.

Further, one of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have recognized that the output stage of *Sukegawa* is

analogous to the output stage of *Ternullo*, especially given that these two references are in the same field of technology. *See supra* Section VII.A; *see also, e.g.*, Ex. 1002, ¶ 44. Similar to *Ternullo*, the output stage of *Sukegawa* receives signals after the signals have been amplified by a differential amplifier, and thus structurally, one of ordinary skill at the time of the alleged invention of the '130 Patent could have modified the output stage of the latching sense amplifier disclosed in *Ternullo* with the output stage disclosed in *Sukegawa*. *See, e.g.*, Ex. 1002, ¶ 44. One of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have been motivated to do so because *Sukegawa*'s output stage employs positive feedback, which could have achieved faster switching, a desirable result in high-speed signal transmissions. *See, e.g.*, Ex. 1002, ¶ 44. Indeed, such a skilled person would have recognized that doing so would have amounted to nothing more than the use of a known technique to improve similar devices in the same way and would have yielded nothing more than predictable results. *See KSR*, 550 U.S. at 417.

VIII. STATEMENT REGARDING OTHER PETITION

As noted, Petitioner is filing another petitioner concurrently with this Petitioner. This Petition presents an anticipation ground based on *Ternullo*, while the other petition presents an obviousness ground based on a different primary reference. The Board should institute review based on both petitions. Petitioner has

attempted to streamline the petitions by raising grounds based on only one primary reference in each petition. This achieves the goal of "just, speedy and inexpensive resolution" consistent with 37 C.F.R. § 42.1(b). In addition, the two petitions present independent, distinctive, and non-redundant grounds at least because Patent Owner may attempt to distinguish the primary references with different arguments.

IX. CONCLUSION

For the reasons given above, Petitioner requests *inter partes* review and cancellation of claims 1-3, 5-7, and 9 of the '130 Patent.

Respectfully submitted,

Dated: June 26, 2015

By: /Steven L. Park/
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Counsel for Samsung Electronics Co., Ltd.

CERTIFICATE OF SERVICE

The undersigned certifies service under 37 C.F.R. §§ 42.6(e) and 42.105 by Express Mail of a true and correct copy of this Petition For *Inter Partes* Review and supporting material on June 26, 2015, upon counsel for the Patent Owner at the correspondence address below:

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The undersigned also certifies service under 37 C.F.R. §§ 42.6(e) and 42.105 by Express Mail of a true and correct copy of this Petition For *Inter Partes* Review and supporting material on June 26, 2015, upon the Patent Owner's lead litigation counsel at the correspondence address below:

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