IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

United States Patent No: 6,836,290	§	Attorney Docket No.:
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Formerly Application No.: 09/302,090	§	
Issue Date: December 28, 2004	§	Petitioner:
Filing Date: April 29, 1999	§	Samsung Electronics Co. Ltd.
Former Group Art Unit: 2612	§	Samsung Electronics America, Inc.
Former Examiner: Ngoc Yen T Vu	§	Samsung Semiconductor, Inc.

For: COMBINED SINGLE-ENDED AND DIFFERENTIAL SIGNALING INTERFACE

MAIL STOP PATENT BOARD
Patent Trial and Appeal Board
United States Patent and Trademark Office
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PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 6,836,290

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Pursuant to §§ 311-319 and Rule 42,[1] the undersigned, on behalf of and acting in a representative capacity for Samsung Electronics Co. Ltd., Samsung Electronics America, Inc. and Samsung Semiconductor, Inc. ("Samsung" or "Petitioner") hereby petition for *inter partes* review of claims 1 and 10 ("Challenged Claims") of U.S. Patent No. 6,836,290 ("the '290 patent"), currently assigned to Imperium IP Holdings (Cayman), Ltd. ("Patent Owner"). Petitioner asserts that there is a reasonable likelihood that at least one of the Challenged Claims is unpatentable for the reasons set forth herein and respectfully requests review of, and judgment against, the Challenged Claims as unpatentable under §§ 102 and/or 103.

I. INTRODUCTION

The '290 patent relates to data interface circuits. Ex. 1001 1:10-15. The supposed "invention" of the Challenged Claims relates to a data interface "that can be either a single-ended interface or a differential interface." *Id*. 3:21-23. The type of interface is selectable based on whether a single-ended output (which uses a single transmission line) or a differential output (which uses two lines) is desired. *Id.* 4:3-22. Claim 1 is directed to a generic data interface, whereas claim 10 uses this generic data interface to connect a CMOS image sensor and an image processor.

There is nothing new in the Challenged Claims. Single-ended and differen-

[1] All section cites herein are to 35 U.S.C. or 37 C.F.R., as the context indicates. All emphasis is added unless otherwise indicated.

tial interfaces were well known well before the filing of the ’290 patent, as was a combined data interface that allows selection between a single-ended or differential interface based on the desired output. And using single-ended and differential interfaces in a CMOS imager was similarly well known in the art. Indeed, as explained herein, every claim element of the supposed inventive data interface of the Challenged Claims is anticipated, or at minimum obvious, in view of the prior art.

U.S. Patent No. 5,929,655 (“Roe”) and Japanese Patent Publication No. 1997-006592 (“Toshiba”) – which were not before the USPTO during prosecution of the ’290 patent – are prior art patents directed to solving the very same problems as the ’290 patent. Like the ’290 patent, Roe and Toshiba address the problems of limited compatibility with external devices while minimizing pin count and board space to reduce chip costs, and teach ***the same supposed solution*** – a combined single-ended and differential interface configured in exactly the same way as the interface of claim 1. *See, e.g.*, Ex. 1001 2:45-61, 3:20-37; Ex. 1004 3:38-49; Ex. 1005 ¶¶ 5-7, 11. Claim 10 takes the generic interface of claim 1 and uses it as the data interface between a CMOS image sensor and an image processor. As explained herein, it certainly would have been obvious to one of skill in the art to use the advantageous interface of either Roe or Toshiba as the interface between a CMOS image sensor and an image processor.

For example, U.S. Patent No. 6,452,632 (“Umeda,” Ex. 1006) and U.S. Pa-

tent No. 6,115,482 ("Sears," Ex. 1007) each disclose a data interface between a CMOS image sensor and an image processor. Both Umeda and Sears expressly disclose both single-ended and differential interfaces and explicitly suggest using a data interface that meets certain design goals, such as high versatility, high performance, low cost, minimal chip size and low pin count. These very goals are met by the data interface of either Roe or Toshiba, and a person of ordinary skill in the art ("POSITA") would have been motivated and certainly would have found it obvious to employ their interfaces in either Umeda or Sears. Furthermore, implementing the Roe and Toshiba data interfaces in the systems disclosed by Umeda or Sears would have been routine, consistent with industry trends and demands, and well within the skill of POSITA.

In summary, as demonstrated herein, every element of Challenged Claim 1 is disclosed in or, at minimum, rendered obvious by the prior art, and Challenged Claim 10, at most, is nothing more than a routine and predictable combination of using the data interface of claim 1 in a CMOS imager. Thus, Petitioner respectfully requests that the Board find that the Challenged Claims are unpatentable.

II. MANDATORY NOTICES UNDER § 42.8

A. Samsung Is the Real Party in Interest Under § 42.8(b)(1)

The real parties-in-interest are Petitioners Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; and Samsung Semiconductor, Inc.

B. Related Matters Under § 42.8(b)(2)

Imperium has asserted claims 1 and 10 of the '290 patent against Petitioner in *Imperium IP Holdings (Cayman) v. Samsung Electronics Co., et al*, Case No. 4:14-cv-00371 (ALM) (E.D.T.X., filed June 9, 2014) ("EDTX").[2]

C. Lead and Back-Up Counsel Under § 42.8(b)(3) and Service Information under § 42.8(b)(4)

Lead and backup counsel, and service information are in the signature block.

III. PETITION HAS STANDING

A. Grounds for Standing Under 37 C.F.R § 42.104(a)

Petitioner certifies, pursuant to § 42.104(a), that the '290 patent is eligible for *inter partes* review and that Petition is not barred or estopped from requesting

[2] In EDTX, Imperium sued Petitioners, along with Samsung Telecommunications America, LLC ("STA") and Samsung Techwin Co., LTD. and Samsung Opto-Electronics America, Inc. (together "Samsung Techwin"). Effective January 1, 2015, STA merged with Samsung Electronics America, Inc., and STA ceased to exist as a separate corporate entity. *See* EDTX, Dkt. No. 67. On January 7, 2015, the court severed Imperium's case against Samsung Techwin, following briefing that established that Samsung Techwin and Petitioners are separate parties represented by separate counsel. *See id.*, Dkt. No. 66. Samsung Techwin is not a privy to a Petitioner or a party-in-interest in the current proceeding.

inter partes review of the patent. Petitioner was served with a Complaint asserting infringement of the patent on or after June 9, 2014, and neither Petitioner nor any other real party-in-interest or privy of Petitioner was served with a complaint before that date, or has initiated a civil action challenging validity of the '290 patent.[3]

B. Claims and Statutory Grounds Under § 42.22 and § 42.104(b)

Petitioner requests *inter partes* review of claims 1 and 10 and asserts that these claims are unpatentable under §§ 102 and/or 103 as set forth below:

Grounds 1 & 2: Claim 1 is anticipated under § 102 by Roe or at minimum rendered obvious under § 103 by Roe and knowledge of a POSITA;

Ground 3 & 4: Claim 1 is anticipated under § 102 by Toshiba or at minimum rendered obvious under § 103 by Toshiba and knowledge of a POSITA;

Ground 5: Claim 10 is obvious under § 103 over Umeda in view of Roe;

Ground 6: Claim 10 is obvious under § 103 over Umeda in view of Toshiba;

Ground 7: Claim 10 is obvious under § 103 over Sears in view of Roe; and

Ground 8: Claim 10 is obvious under § 103 over Sears in view of Toshiba.

None of the art in grounds 1-8 was considered by the Patent Office during prosecu-

[3] The date that Samsung Techwin was served with a Complaint alleging infringement of the '290 patent is irrelevant, as it is not a privy of a Petitioner or a party-in-interest in this proceeding. In any case, Samsung Techwin was served with a Complaint asserting infringement of the '290 patent on or after June 9, 2014.

tion of the ’290 patent. Section V below provides claim charts specifying how the relied upon prior art renders unpatentable claims 1 and 10. In further support of the proposed grounds of rejection, this Petition is accompanied by a Declaration of technical expert R. Jacob Baker. Ex. 1008.

IV. SUMMARY OF THE ’290 PATENT AND ITS FIELD

A. Overview of the ’290 Patent

The ’290 patent, “Combined Single-ended and Differential Signaling Interface,” was filed April 29, 1999, and issued December 28, 2004. Ex. 1001. As its title suggests, the patent is directed to a data interface “that can be either a single-ended interface or a differential interface.” *Id.* 3:21-23. A single-ended interface uses *one* wire to communicate a signal. Ex. 1008 ¶¶ 16, 38. In contrast, a differential interface uses *two* wires to communicate one signal. *Id.* ¶ 17, 49.

The ’290 patent admits that single-ended interfaces were “the most common and simplest implementation for data transfer” and that use of single-ended interfaces in CMOS imagers was well-known. Ex.1001 1:27-28; 4:50-51. Despite the simplicity and widespread adoption of single-ended interfaces, the ’290 patent admits that differential interfaces were also known and offer an advantage over single-ended interfaces in terms of reduced noise and power consumption. *Id.* 1:35-65; 4:53-54. The ’290 patent states, however, that differential interfaces suffer from the problem of limited compatibility: “existing image processing devices may

only support the common single-ended interface…and not the differential interface." *Id.* 2:38-42. To address this problem, the '290 patent states that "[it] is possible to place both interfaces on the imager in order to support both types of companion chips [*i.e.*, chips that receive single-ended and differential signals]." But, as the '290 patent points out, "this would add pins and cost." *Id.* 2:42-44.

The '290 patent states that its data interface circuit solves this problem by providing support for both single-ended and differential signaling while using minimal pins and thus saving costs. Specifically, the '290 patent states it combines both the single-ended and differential interfaces into one circuit and uses a selection signal to selectively output data from either interface, thereby increasing compatibility with existing devices. *Id.* 3:21-25; 4:3-21. Further, the circuit reuses the same set (as opposed to separate sets) of pins to output data from both interfaces. *Id.* Fig. 5; 2:45-52. The patent states that by reusing output pins for both interfaces, the data interface circuit provides increased compatibility with external devices while reducing pins and cost. *Id.* Abstract, 3:27-30, 2:45-52.

B. Overview of the Field of the Claimed Invention

By April 29, 1999, the filing date of the '290 patent, all components and functionality of the Challenged Claims were well known and, as established herein, their configuration as claimed was also well known or, at minimum, obvious.

By April 1999, the single-ended interface was the most popular interface to communicate data. *See, e.g.,* Ex. 1008 ¶ 39. The '290 patent, for example, admits that single-ended interfaces were common, simple to implement, and compatible with many external devices. *Id.* 1:27-28; 2:37-52; 3:23-25. Numerous prior art references confirm the popularity of single-ended interfaces. *See, e.g.,* Ex. 1004 2:66-3:4; Ex. 1005 ¶¶ 5-6; Ex. 1009 at pp. 107, 155-156; Ex. 1010 at pp. 55-66.

And given the ubiquity of single-ended interfaces, by April 1999, it was also well known to use CMOS sensors with single-ended interfaces to communicate image data. The '290 patent itself concedes that "[a]ll known prior art CMOS imagers have used single-ended interfaces." Ex. 1001 4:50-52. In fact, Umeda and Sears – which were both filed prior to the '290 patent – disclose using single-ended interfaces with CMOS imagers. Umeda discloses using a "PC Card" or "the like" to interface a CMOS image sensor and an image processor. Ex. 1006 Fig. 14. Sears discloses a PCMCIA or CardBus, both of which were well-known PC cards, to interface a CMOS sensor and an image processor. Ex. 1007 6:52-67. PC Cards were well-known interfaces that supported single-ended signaling, and a POSITA would have known that they could have been readily used to transfer image data from a CMOS sensor to an image processor. *See, e.g.,* Ex. 1008 ¶¶ 37, 48, 41-44.

Differential interfaces were also well known by April 1999. *See, e.g.,* Ex. 1001 1:35-2:37; Ex. 1004 3:4-9; Ex. 1005 ¶ 5; Ex. 1008 ¶¶ 49-56. And, as any

POSITA would have known, compared to single-ended interfaces, differential interfaces advantageously provide faster data transfer, lower noise, and lower power consumption. *See, e.g.*, Ex. 1008 ¶ 55; Ex. 1001 1:35-65, 4:53-54; Ex. 1005 ¶ 5; Ex. 1013 at p. 2; Ex. 1009 at p. 108; Ex. 1010 at pp. 62-63.

Given these advantages, by April 1999, it was known in the art to use differential interfaces with CMOS image sensors, which required faster data transfer. Ex. 1008 ¶ 57. Indeed, during prosecution of the '290 patent, the examiner took "official notice" (*and the Applicant did not contest*) that it was well known to use differential signaling to transfer digital signals from a CMOS image sensor to an image processor. Ex. 1002 at p. 96. And, in fact, both Umeda and Sears disclose that the IEEE 1394 interface, a well-known differential interface, could be used to transmit data from a CMOS image sensor to a personal computer to perform "high-speed processing" of motion detection data. *See e.g.*, Ex. 1008 ¶ 55; Ex. 1006 18:32-47; Ex. 1007 6:52-57.

Accordingly, by April 1999, it was well understood that while single-ended interfaces provided compatibility with many external imaging devices, differential interfaces provided higher data rates that were often required for imaging devices. *See, e.g.*, Ex. 1001 2:39-42; 4:50-54; Ex. 1004 3:4-27; Ex. 1005 ¶¶ 5-6; Ex. 1009 at p. 107-108; Ex. 1010 at p. 66; Ex. 1013 at p. 1; Ex.1014 at p. 3. Not surprisingly, given the widespread recognition of the benefits of both differential interfaces and

more traditional single-ended interfaces, implementations enabling use of, and interchangeability among, single-ended and differential interfaces were also well known by April 1999. Roe and Toshiba, in particular, expressly disclose interface circuits that selectively output data from either a single-ended or a differential interface. For example, Roe states that:

> The present invention provides . . . apparatuses for providing dual-purpose I/O circuits for use with a combined LINK/PHY circuit on a single circuit die, wherein each of the dual-purpose I/O circuits can be configured to support either one, or both, single-ended and differential I/O signaling modes…. ***The control logic is arranged to selectively enable and disable at least one of the first single-ended, second single-ended and differential I/O cells***.

Ex. 1004 3:37-4:4. Toshiba described the state of the art as follows:

> Dramatic improvements in the internal frequencies of semiconductor integrated circuits in recent years require that I/O circuits also be made faster. ***Therefore, a single-ended interface (hereinafter described as SE) signal transmission mode, which uses a single transmission path, had been used, but a dual transmission path differential interface signal transmission mode, which operates at smaller***

amplitudes than SE and is therefore capable of higher processing speeds, has come into use.

Ex. 1005 ¶ 5. Toshiba then went to state that its purpose was to "make it possible to selectively use a differential interface and a single-ended interface without changing boards, and to broaden peripheral large-scale integration (LSI) options." *Id.* ¶ 7. The prior art was teeming with other interfaces that could operate as either a single-ended interface or a differential interface to provide compatibility with a greater variety of external devices. *See, e.g.*, Ex. 1008 ¶¶ 37, 58-63; *see generally* Ex. 1019; Ex.1020; Ex.1021.

The design of these prior art systems was driven by well-known industry demands in the late 1990s for high compatibility with existing single-ended interfaces, as well as with the high speed performance, low noise, low power consumption, and low cost of differential interfaces. Ex. 1008 ¶¶ 45, 64-65. Indeed, compatibility with existing interfaces and applications was highly encouraged in the interface industry in the 1999 timeframe. *See, e.g.*, Ex. 1008 ¶ 64; Ex. 1012 at p. 1; Ex. 1010 at p. 63; Ex. 1005 ¶¶ 5-6; Ex. 1006 2:44-52; Ex. 1018 at p. 5.

Thus, as illustrated by these background examples and the prior art detailed below in Section V (including the primary prior art references, Roe and Toshiba), long before April 1999, numerous disclosures identified the very problem that the '290 patent purports to solve***, as well as the "solution" purportedly claimed by***

the '290 patent as its applicants' sole property. As outlined in more detail below, the challenged claims are unpatentable under §§ 102 and/or 103.

C. Overview of the Prosecution History of the '290 Patent

Prosecution of the '290 patent was brief. Both Challenged Claims were allowed in the first Office Action. Ex. 1002 at pp. 94, 96. Then-pending independent claim 14 (corresponding to issued claim 17) was rejected under § 103(a) in view of U.S. Patent No. 5,761,244 ("Hedberg"). In the rejection, the Examiner took Official Notice that it was well known in the art to use Hedberg's Low Voltage Differential Signaling system (a differential interface) to transfer digital signals from CMOS image sensing pixels to a digital signal processor. *Id.* at p. 96. Notably, Applicants did not refute this statement and instead narrowed claim 14 to overcome Hedberg. *Id.* at pp. 101-107, 110-117.

The '290 patent is a continuation-in-part of U.S. Patent Application No. 09/062,343 ("the parent"). The Challenged Claims are not entitled to the filing date of the parent because, *inter alia*, the parent app. does not disclose a data interface circuit that is selectable between a single-ended interface output and a differential interface output, as required by the Claims. Ex. 1008 ¶ 14; Ex. 1003 at pp. 32-46. Prosecution of the parent does confirm, however, that it was well known in the art to use a differential interface to transfer data from CMOS image sensors to

an image processor. *See, e.g.,* Ex. 1002 at p. 96. The claims, as originally filed, were directed to this very concept. Claim 1 of the parent is representative:

> 1. The CMOS imaging apparatus comprising:
>
> a CMOS image sensor;
>
> a CMOS image processor; and
>
> a plurality of low voltage differential signaling circuits connected between said image sensor and said image processor.

See also, e.g., claims 11, 17. But the claims of the '343 application were rejected numerous times, and the parent was eventually abandoned after the applicants were unable to overcome the prior art cited by the Examiner – an admission by the applicants that this subject matter was already known. *See, e.g.,* Ex. 1003 at pp. 32-46, 59-66, 68-85, 86-92, 94-107, 108-116, 117-119.

V. THERE IS A REASONABLE LIKELIHOOD THAT PETITIONER WILL PREVAIL WITH RESPECT TO AT LEAST ONE CLAIM OF THE '290 PATENT AS REQUIRED BY § 314(A)

A. Claim Construction Under § 42.104(b)(3)

Pursuant to § 42.100(b), for the purposes of this review, the claim language is to be construed such that it is "given its broadest reasonable construction in light of the specification of the patent in which it appears." The parties in EDTX have proposed constructions for disputed claim terms (and have agreed to constructions for others) under the different standard applicable there, enunciated by the Federal

Circuit in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*see* Ex. 1026). Petitioner, however, does not believe that any of the proposed constructions for the disputed terms impacts the analysis in this Petition (Ex. 1008 ¶ 28), and respectfully submits that – because the prior art presented herein renders the claims unpatentable even under the potentially narrower constructions proposed in litigation – there is no need to consider and construe here the outer bounds of the scope of these claims term under the broader standard of § 42.100(b). Nevertheless, Petitioner believes its constructions from EDTX are appropriate, as discussed below:

"single-ended interface"/"differential interface" – While the parties initially had different constructions for single-ended interface (*see* Ex. 1026), Petitioner has agreed to adopt Imperium's broader construction to narrow the issues for the Court: "an interface that uses a single line to transmit a signal." Ex. 1001 Figs. 1, 2, 5; 1:27-34. The parties have agreed that differential interface means "an interface that uses two lines to communicate a signal."[4] *Id*. 1:35-37; 3:12-15; Fig. 3.

[4] A POSITA would have understood that a differential interface requires a normal signal and a complementary signal. *See, e.g.*, Ex. 1008 ¶¶ 49-50; Ex. 1015 at p. 11; Ex. 1014 at p. 4; Ex. 1009 at p. 164; Ex. 1001 3:12-18. Because the language of claims 1 and 10 expressly includes this requirement, it is unnecessary to include this language (*i.e.*, a normal signal and a complementary signal) in the construction.

"wherein an output of the data interface circuit is selectable between a single-ended interface output and a differential interface output" – Petitioner in EDTX has proposed that this phrase means "wherein either the single-ended interfaces or the differential interface can be selected to output data from the data interface circuit." Imperium has stated that, if construed, it means "a single-ended interface output or a differential interface output can be chosen." Petitioner's construction is correct because (unlike Imperium's) it clarifies the meaning of "single-ended interface output" and "differential interface output." Ex. 1001 4:3-49.

"the sensor having a data interface circuit" – Petitioner has proposed that this term means "the CMOS image sensor including a circuit that communicates image data." Imperium has stated that, if construed, it means "the CMOS image sensor has a data interface circuit." Petitioner's construction is correct because it makes clear that the interface is communicating image data. This term appears in claim 10, which claims a "CMOS ***imaging*** apparatus" with a data interface circuit that connects a "CMOS ***image*** sensor" to an "***image*** processor." Thus, the claim language establishes that the communicated data must be ***image*** data. This is confirmed by the specification. *See id*. Fig. 4; 2:18-37; 1:17-34; 2:62-3:11; 4:3-15.

"an image processor connected to the CMOS image sensor to receive the signals output by the data interface circuit" – Petitioner has proposed in EDTX that this term means "a processor connected to the CMOS image sensor for pro-

cessing image data received from the single-ended and the differential interfaces." Imperium has stated that plain and ordinary meaning applies. Petitioner submits that its construction ***is*** the plain and ordinary meaning of this phrase. In particular, Petitioner's construction makes clear that an "image processor" is "a processor . . . for processing image data." *See, e.g., id.* 2:14-26; 1:11-15; 1:16-34, 3:64-4:2.

Petitioner submits that any remaining terms may also be construed for purposes of this Petition based on their plain and ordinary meaning under the required broadest reasonable interpretation consistent with the specification of the '290 patent in view of a POSITA's knowledge. Because the claim construction standard at the PTO is different than litigation, *see In re Am. Acad. of Sci. Tech Ctr.,* 367 F.3d 1359, 1364, 1369 (Fed. Cir. 2004); MPEP § 2111, Petitioner reserves the right to argue in litigation constructions for any term, as appropriate to that proceeding.

B. Level of Ordinary Skill in the Art and State of the Art

Petitioner submits that the applicable person of ordinary skill in the art relating to the technology of the '290 patent as of April 29, 1999 would have, at minimum, a Bachelor's degree in the field of electrical engineering, computer engineering, physics, or the equivalent, and two years of experience in the field of interface design and/or a comparable field; or a Master's degree in electrical engineering, physics, computer engineering, or the equivalent, and one year of experience in the field of interface design and/or a comparable field. Ex. 1008 ¶¶ 23-26.

C. Grounds 1 & 2: Claim 1 is anticipated under § 102 by Roe (Ground 1) or at minimum rendered obvious under § 103 by Roe and knowledge of a POSITA (Ground 2)

1. Overview of Roe

Roe, titled "Dual-Purpose I/O/ Circuit In A Combined Link/Phy Integrated Circuit," filed March 25, 1997, and issued July 27, 1999, is prior art under at least § 102(e). Ex. 1004. Roe discloses a dual-purpose I/O circuit that uses a selection signal (*e.g.*, DIFF_EN) to allow the I/O circuit to output data through either a single-ended interface or differential interface. *See, e.g., id.* Fig. 2c; Ex. 1008 ¶ 67, pp. 97-98. And Roe expressly discloses that its versatile dual-purpose I/O circuit "can be used for ***any integrated circuit*** that requires the inputting and outputting of signals." *See, e.g.,* Ex. 1004 3:46-49; Ex. 1008 at pp. 84, 109, 114.

Roe explains that its dual-purpose I/O circuit advantageously supports both single-ended and differential I/O signaling to achieve signaling compatibility with a greater variety of applications "without having to greatly increase the size of the die or the number of I/O pins." *See, e.g., id*. Abstract; 3:29-35; 3:44-46; 5:46-51; Ex. 1008 ¶¶ 68-70, pp. 98, 113, 124-125. As an example, Roe repeatedly mentions using its interface "to support IEEE 1394 standard buses and communications" as an intended target application. *See, e.g.,* Abstract; Fig. 2a; 5:3-6; 5:23-63; 1:56-2:42; Ex. 1008 ¶ 69, pp. 112-113, pp. 125-126. Moreover, by reusing the same pins to output data from both interfaces, Roe is able to reduce pin count and board

space, thus reducing chip manufacturing costs. Ex. 1008 ¶ 70, pp. 113, 125.

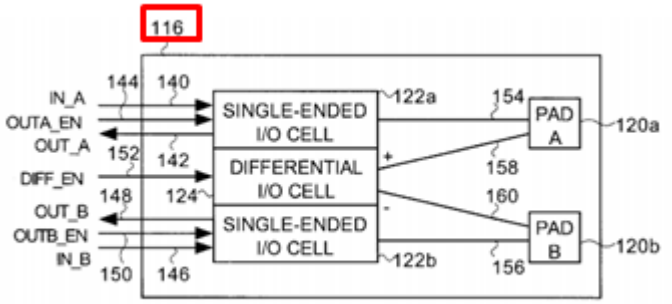
2. Claim 1 is anticipated under § 102 over Roe

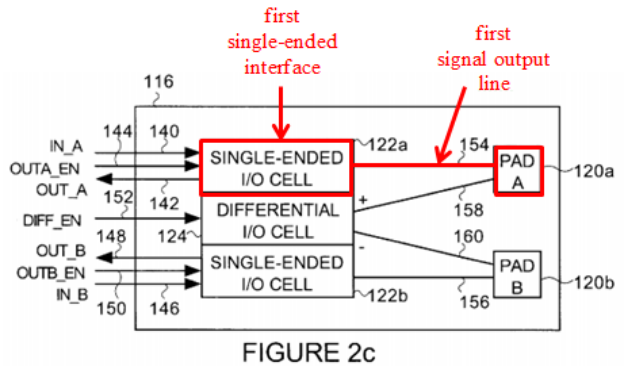
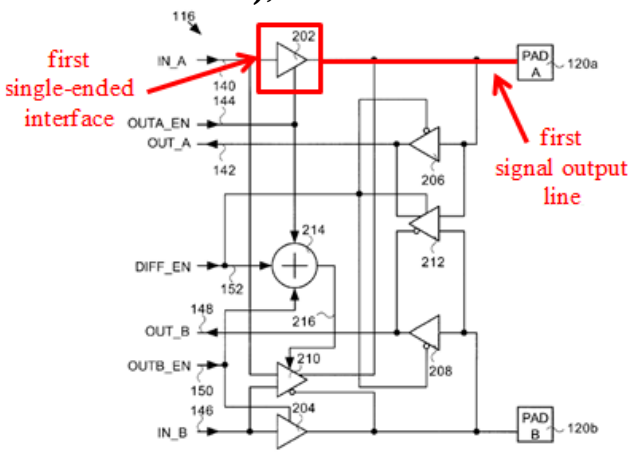
As detailed in the chart below, Roe discloses (in the exemplary excerpts and cites provided herein) each and every limitation of claim 1, rendering it invalid as anticipated under § 102 (Ground 1).[5]

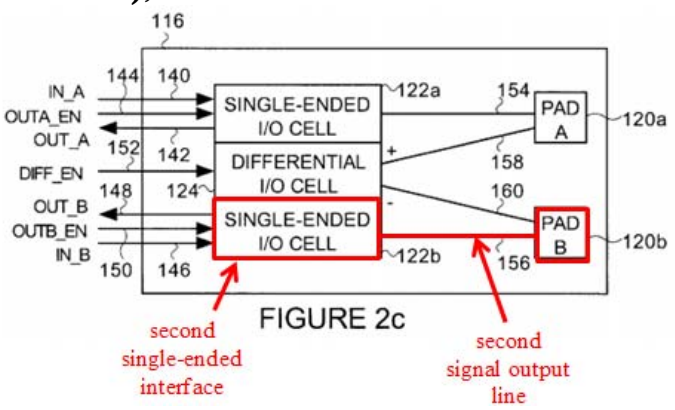
Claim 1	**Roe**
[Preamble][6] A data interface circuit comprising:	**Roe discloses a data interface circuit (*e.g.*, dual-purpose I/O circuit 116). *See, e.g.*, Ex. 1004 3:38-60** ("The present invention provides methods and apparatuses for providing *dual-purpose I/O circuits* for use with a combined LINK/PHY circuit on a single circuit die, wherein each of the dual-purpose I/O circuits can be configured to support either one, or both, single-ended and differential I/O signaling modes. Because of their reduced size, the dual-purpose I/O circuits can be implemented without significantly reducing the available space on a circuit die for the LINK/PHY circuit. The *dual-purpose I/O circuits*…can be used for any integrated circuit that requires the inputting and outputting of signals…The *dual-purpose I/O circuit* includes two conducting pads, two single-ended cells and one differential I/O cell."); **6:49-54** ("FIG. 2*c* is a block diagram of a *dual-purpose I/O circuit 116* . . . 120*b*, a first single-

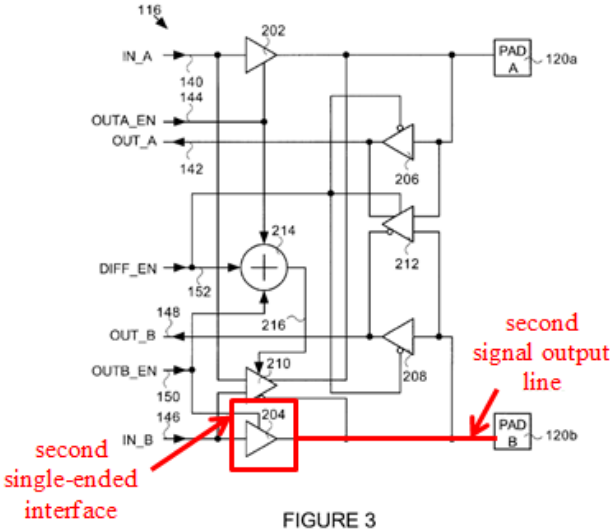
[5] To the extent Roe does not meet any element, claim 1 would have at minimum been obvious to a POSITA under § 103 in light of Roe (Ground 2) based on the same disclosures provided in the context of anticipation. Ex. 1008 at ¶¶ 66, 110, pp. 84-102.

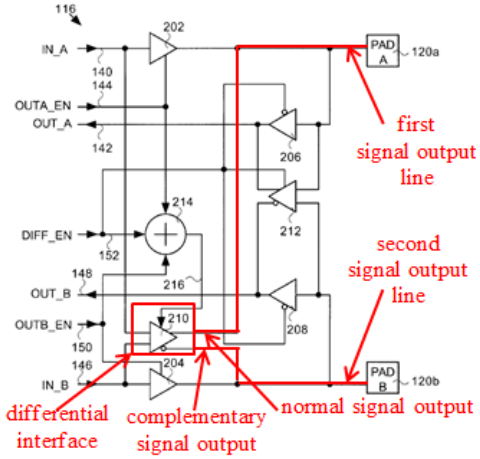
[6] Petitioner includes an analysis of the preambles in the Challenged Claims in the event the preambles are determined to be limitations.

Claim 1	Roe
	ended I/O cell 122*a*, a second single-ended I/O cell 122*b*, and a differential I/O cell 124."); **5:15-17** ("*FIG. 3 is a block diagram of a dual-purpose I/O circuit as in FIGS. 2b and 2c*, in accordance with one embodiment of the present invention…"); **Fig. 2c (annotated below)**;  FIGURE 2c **7:65-8:5** ("FIG. 3 is a block diagram of a *dual-purpose I/O circuit 116* . . . . As shown, dual-purpose I/O circuit 116 includes a first single-ended output buffer 202, a second single-ended output buffer 204, a first single-ended input buffer 206, a second single-ended input buffer 212, a summer 214, and conducting pads 120*a* and 120*b*. "). ***See, e.g.*, Abstract; 1:11-19; 2:43-4:45; 3:61-4:4; 5:3-35; 5:46-63; 6:49-54; 8:51-9:1; 11:24-12:14; claim 1; Figs. 2a, 2b, 3, 4; Table 1; Ex. 1008 ¶¶ 67, 71-72, 75, 78, pp. 84-87.**
[1.1] a first single-ended interface connected to a first signal output line;	**Roe discloses a first single-ended interface (*e.g.*, single-ended I/O cell 122a in Fig. 2c, which includes first single-ended output buffer 202 in Fig. 3, which comprises NOR gate 302, NAND gate 304, and transistors 306 and 308 in Fig. 4) connected to a first signal output line (*e.g.*, output line connected to conducting pad 120a in Figs. 2c and 3). *See, e.g.*, Ex. 1004 6:55-62** ("*First single-ended I/O cell 122a is arranged to transfer a first I/O signal between first conducting pad 120a (via line 154)*, and an input line IN_A 140 and an output line OUT_A 142 which are coupled to primary circuit 114. . . . ."); **Fig. 2c (annotated below)**;

Claim 1	Roe
	 FIGURE 2c **5:15-17** ("*FIG. 3 is a block diagram of a dual-purpose I/O circuit as in FIGS. 2b and 2c …*"); **7:65-8:19** ("FIG. 3 is a block diagram of a dual-purpose I/O circuit 116 . . . . *As shown, dual-purpose I/O circuit 116 includes a first single-ended output buffer 202* . . . and conducting pads 120a and 120b. *First single-ended output buffer 202 is coupled to line IN_A 140 and outputs the I/O signal received therefrom to pad 120a when enable signal on line OUTA_EN 144 is logical high…*"); **Fig. 3 (annotated below)**;  FIGURE 3 ***See also, e.g.*, Abstract; 3:38-4:4; 5:3-20; 5:18-20; 5:47-62; 6:7-9; 6:48-54; 7:25-34; 8:51-9:40; 11:24-50, 11:56-58; 11:62-12:14; claims 1, 3, 6, 7, 17; Figs. 2a, 2b, 4; Table 1; Ex. 1008 ¶¶ 72-73, 76, 80-81, pp. 87-89.**
[1.2] a second single-ended interface connected to a second	**Roe discloses a second single-ended interface (*e.g.*, second single-ended I/O cell 122b of Fig. 2c, which includes second single-ended output buffer 204 in Fig. 3, which comprises NOR gate 338, NAND gate 340, and transistors 342 and 344**

Claim 1	Roe
signal output line; and	**in Fig. 4) connected to a second signal output line (*e.g.*, output line connected to conducting pad 120b in Figs. 2c and 3). *See, e.g.*, Ex. 1004 6:63-7:4** ("Similarly, *second single-ended I/O cell 122b is arranged to transfer a second I/O signal between second conducting pad 120b (via line 156)* . . . . Second single-ended I/O cell 122b is further coupled to control signal line OUT_EN 150 to receive an enable signal."); **Fig. 2c (annotated below)**;  FIGURE 2c **5:15-17** ("*FIG. 3 is a block diagram of a dual-purpose I/O circuit as in FIGS. 2b and 2c*, in accordance with one embodiment of the present invention…"); **7:65-8:19** ("FIG. 3 is a block diagram of a dual-purpose I/O circuit 116, in accordance with one embodiment of the present invention. As shown, dual-purpose I/O circuit 116 includes a first single-ended output buffer 202, *a second single-ended output buffer 204*, a first single-ended input buffer 206, a second single-ended input buffer 212, a summer 214, and conducting pads 120a and 120b…*second single-ended output buffer 204 is coupled to line IN_B 146 and outputs the 1(0[sic] signal received therefrom to pad 120b when the enable signal on line OUTB_EN 150 is logical high*…"); **Fig. 3 (annotated below)**;

Claim 1	Roe
	 FIGURE 3 ***See also, e.g.*, Abstract; 3:38-4:4; 5:3-20; 5:18-20; 5:47-62; 6:7-9; 6:48-7:8; 7:25-34; 8:13-19; 9:22-40; 11:24-58; 11:62-12:14; claims 1, 3, 6, 7, 17; Figs. 2a, 2b, 4; Ex. 1008 ¶¶ 72-73, 76, 80-81, pp. 91-94.**
[1.3] a differential interface having a normal signal output connected to the first output line and a complementary signal output connected to the second signal output line;	**Roe discloses a differential interface (*e.g.*, differential I/O cell 124 of Fig. 2c, which includes differential output buffer 210 in Fig. 3, which comprises transistors 324, 326, 328, 330, 332, 334, 322 and 326 in Fig. 4) having a normal signal output (e.g., positive differential I/O signal) connected to the first output line (*e.g.*, output line connected to conducting pad 120a in Figs. 3 and 4) and a complementary signal output (e.g., negative differential I/O signal) connected to the second signal output line (*e.g.*, output line connected to conducting pad 120b in Figs. 3 and 4). *See, e.g.*, Ex. 1004 7:5-20** ("*Differential I/O cell 124 is coupled to first single-ended I/O cell 122a, second single-ended I/O cell 122b, first conducting pad 120a (via line 158), and second conducting pad 120b (via line 160)…When differential I/O cell 124 is enabled, dual-purpose I/O circuit 116 essentially acts as a differential I/O cell with respect to the I/O signals present on conducting pads 120a and 120b*, lines IN_A 140, OUT_A 142, IN_B 146, and OUT_B 148."); **5:15-17** ("*FIG. 3 is a block diagram of a dual-purpose I/O circuit as in FIGS. 2b and 2c*, in accordance with one embodiment of the present invention…"); **8:20-34** ("*Differential output buffer 210* is coupled to lines IN_A 140 and IN_B 146, and to summer 214…*Differential output buffer 210*

Claim 1	Roe
	outputs differential signal based on the difference between the logical I/O signals on lines IN_A 140 and IN_B 146 to pads 120a and 120b. As shown, a positive differential I/O signal is applied to pad 120a, and a negative differential I/O signal is applied to pad 120b when summer 214 outputs a logical high on line 216." Id. 8:20-34."); **Fig. 3 (annotated below)**;  ***See, e.g.*, Abstract; 3:38-4:4; 5:18-20; 5:3-20; 5:47-62; 6:7-9; 6:48-54; 7:5-25; 7:35-51; 8:20-50; 10:9-11:44; 11:51-12:14; claims 1, 4, 8, 9, 17; Figs. 2a-c, 4; Table 1; Ex. 1008 ¶¶ 72-78, 82, pp. 94-97.**
[1.4] wherein an output of the data interface circuit is selectable between a single-ended interface output and a differential interface output.	**Roe discloses that an output of the data interface circuit (*e.g.*, I/O signal outputted from conducting pads 120a or 120b) is selectable (*e.g.*, via enable/disable signal DIFF_EN) between a single-ended interface output (*e.g.*, output from first single-ended output buffer 202 or output from second single-ended output buffer 204 in Fig. 3 when DIFF_EN is logical low) and a differential interface output (*e.g.*, output from differential output buffer 210 in Fig. 3 when DIFF_EN is logical high). *See, e.g.*, Ex. 1004 Abstract** ("A control logic is connected to at least one of the first single-ended, second single-ended and differential I/O cells. *The control logic is arranged to selectively enable and disable at least one of the first single-ended, second single-ended and differential I/O cells…*"); **5:46-53**("*The dual-purpose I/O circuit provides the capability to send and receive I/O signals in either a single-ended or differential mode.*"); **Table 1 (annotated below)**;

Claim 1	Roe

TABLE 1

Operating Mode:	OUTA_EN	OUTB_EN	DIFF_EN	PAD 120a	Pad 120b	OUT_A	OUT_B
Single-Ended Input Mode	"0"	"0"	"0"	"Z"	"Z"	=Pad 120a	=Pad 120b
Single-Ended Output Mode	"1"	"1"	"0"	=IN_A	=IN_B	"X"	"X"
Differential Input Mode	"0"	"0"	"1"	"Z"	"Z"	=Pad 120a	=Pad 120b
Differential Output Mode	"1"	"1"	"1"	=IN_A DIFF+	=IN_A DIFF-	"X"	"X"

[sic] should be "IN_B"

7:16-24 ("*When differential I/O cell 124 is enabled, dual-purpose I/O circuit 116 essentially acts as a differential I/O cell with respect to the I/O signals present on conducting pads 120a and 120b*, lines IN_A 140, OUT_A 142, IN_B 146, and OUT_B 148. *When differential I/O cell 124 is disabled, dual-purpose I/O circuit 116 essentially acts [sic] two separate single-ended I/O cells with respect to the I/O signals present on conducting pad 120a*, lines IN_A 140 and OUT_A 142, *and conducting pad 120b*, lines IN_B and OUT_B 148."); **Fig. 2c (annotated);**

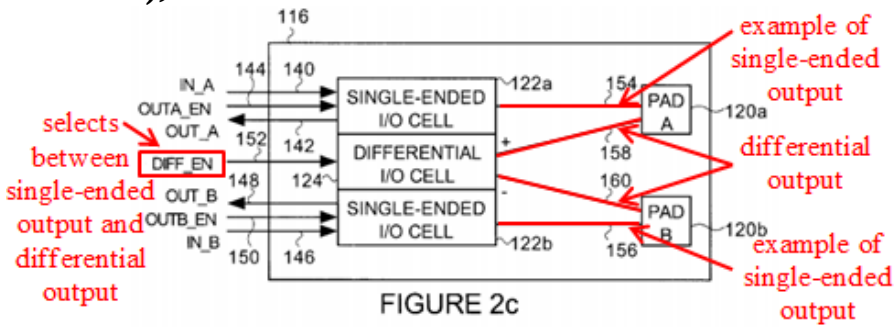
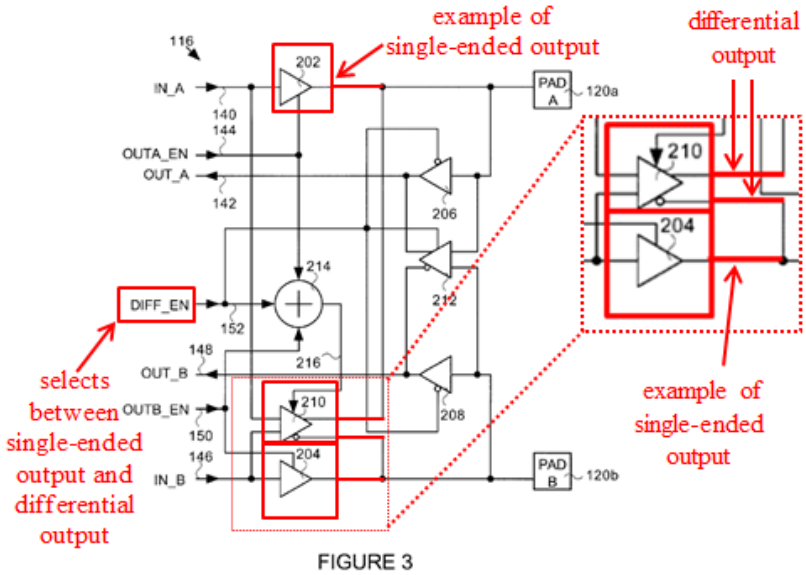


FIGURE 2c

5:15-17 ("*FIG. 3 is a block diagram of a dual-purpose I/O circuit as in FIGS. 2b and 2c*, in accordance with one embodiment of the present invention…"); **8:6-41** ("…*First single-ended output buffer 206 is coupled to pad 120a and outputs the I/O signal received therefrom to line OUT_A 142 when the enable signal on line DIFF_EN 144 is logical low…*Similarly, second single-ended output buffer 204 is coupled to line IN_B 146 and outputs the 1(0[sic] signal received therefrom to pad 120b when the enable signal on line OUTB_EN 150 is logical high…*Differential output buffer 210 outputs differential signals based on the difference between the logical I/O signals on lines IN_A 140 and IN_B 146 to pads 120a and 120b. As shown, a positive differential I/O signal is applied to pad 120a, and a*

Claim 1	Roe
	negative differential I/O signal is applied to pad 120b when summer 214 outputs a logical high on line 216…"); **Fig. 3 (annotated below)**;  FIGURE 3 ***See also, e.g.*, 3:38-49; 4:1-29; 5:18-20; 7:51-64; 8:42-50; 9:3-10:46; 11: 51-55; 11:59-12:14; claims 1, 5-9, 13, 17-26; Figs. 2a-c, 4; Ex. 1008 ¶¶ 67, pp. 97-102.**

D. Grounds 3 & 4: Claim 1 is anticipated under § 102 by Toshiba (Ground 3) or at minimum rendered obvious under § 103 over Toshiba and knowledge of a POSITA (Ground 4)

1. Overview of Toshiba

Toshiba, titled "Semiconductor Integrated Circuit," filed in the Japanese Patent Office on June 22, 1995, published on January 10, 1997, is prior art under at least § 102(b). Ex. 1005. Toshiba discloses an I/O circuit that "selectively use[s] a differential interface and an SE [single-ended] interface" via a selection signal (*e.g.*, MODE_O) to output data to peripherals "without changing boards." *Id.* ¶ 7; Ex. 1008 ¶¶ 84-85, 88, pp. 141, 153-154, 166-167. Toshiba states that its circuit

can be used in "all semiconductor integrated circuits" for a "wide range of uses" and "broad range of applications." Ex. 1005 ¶¶ 16, 28, 37, 41.

Toshiba's I/O circuit is designed to solve the problem of limited compatibility of interface circuits with peripheral devices. *Id.* ¶ 6; Ex. 1008 ¶¶ 86-87, pp. 154, 165-166. Toshiba explains that while differential interfaces were known to offer various advantages over single-ended interfaces (*e.g.*, higher processing speeds), single-ended interfaces were the "only type of signal transmission mode interface" provided in conventional semiconductor integrated circuits. Ex. 1005 ¶ 6; Ex. 1008 ¶ 87, pp. 154, 165-166. To solve the problem of limited peripheral compatibility, Toshiba designed an I/O circuit that has "no reliance upon" and is "independent" of peripheral interface implementations. Ex. 1005 ¶¶ 16, 41; Ex. 1008 ¶ 87, pp. 141. By reusing output pins for both the single-ended and differential interfaces, Toshiba reduces board space, thus minimizing chip manufacturing costs. Ex. 1008 ¶ 88, pp. 153-154, 167.

2. Claim 1 is anticipated under § 102 over Toshiba

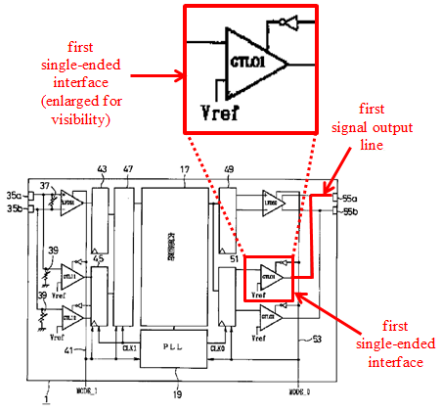
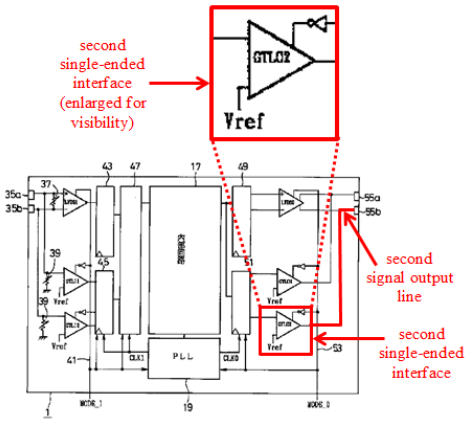
As detailed in the chart below, Toshiba discloses (in the exemplary excerpts and cites provided herein) each and every limitation of claim 1, rendering it invalid as anticipated under § 102.[7]

[7] To the extent it is argued that Toshiba does not meet any given element, claim 1 would at minimum have been obvious to a POSITA under § 103 in light of

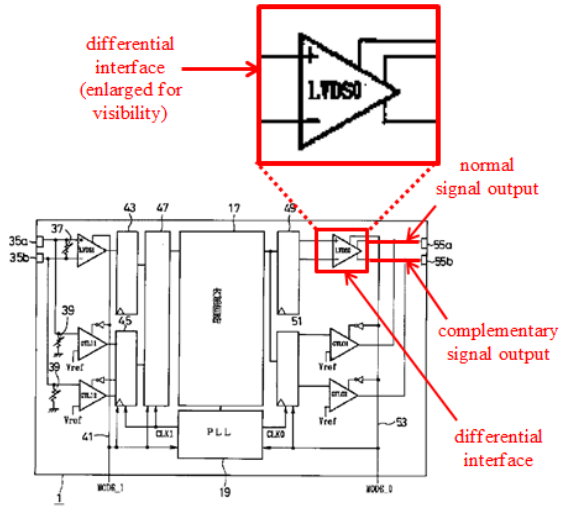
Claim 1	**Toshiba**
[Preamble] A data interface circuit comprising:	**Toshiba discloses a data interface circuit (*e.g.*, I/O circuit of semiconductor integrated circuit 1 in Fig. 2). *See, e.g.*, Ex. 1005 ¶ 1** ("The present invention relates to a semiconductor integrated circuit, and more particularly to a semiconductor integrated circuit comprising an *I/O circuit for interfacing with the outside*.") **¶ 4** ("*This I/O circuit serves as an interface between an external peripheral LSI [large-scale integration] or the like and the internal circuit by converting data from the outside to a desired data used by the internal circuit, and converting data from the internal circuit to a desired data.*"); **Fig. 2; *See also id*. Abstract; ¶¶ 2, 5-7, 9, 14, 28-29, 40; claims 2, 4; p. 36; Ex. 1008 ¶¶ 84, 89, pp. 133-134.**
[1.1] a first single-ended interface connected to a first signal output line;	**Toshiba discloses a first single-ended interface (*e.g.*, GTLO1 using Gunning Transceiver Logic (GTL) for single-ended transmissions) connected to a first signal output line (*e.g.*, line from GTLO1 to signal output pad 55a).** **Toshiba discloses that GTLO1 is an output buffer that uses GTL to output data to signal output pad 55a through a signal output line at, *e.g.*, Fig. 2 (annotated below); ¶¶ 16, 38, 31, 24, 15, 5; *see also, e.g.*, ¶¶ 31, 39, 9, 11, 12, 22, 25, 26, 32, 35, 36; claims 2, 3, 4; Figs. 1, 3, 4; pp. 36-43; Ex. 1008 ¶¶ 41, 90-93, pp. 134-136.** [8]

Toshiba (Ground 4) standing alone based on the same disclosures provided below in the context of anticipation. Ex. 1008 at pp. 133-143.

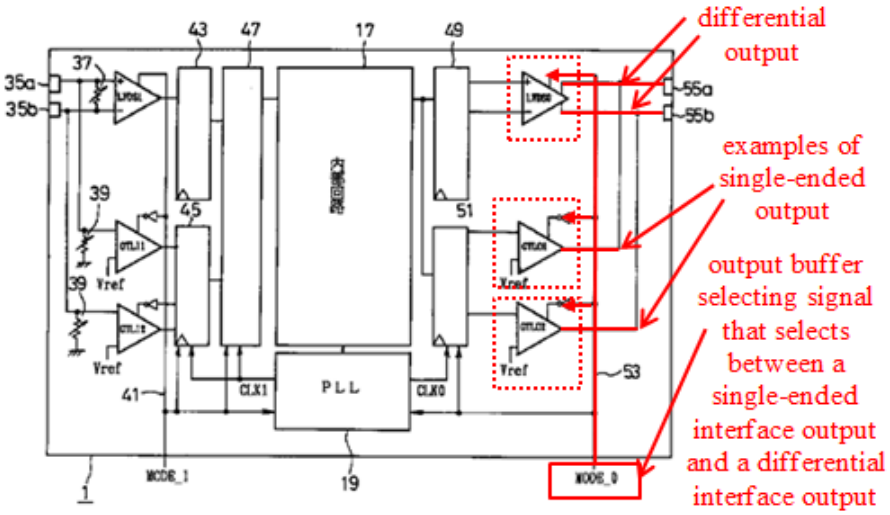
[8] Toshiba discloses that GTL ("Gunning Transceiver Logic") is used for single-ended transmissions at, *e.g.*, ¶¶ 24, 15, 5; *see also* ¶¶ 9, 11, 12; claims 2, 4, 5**.**

Claim 1	Toshiba
	
[1.2] a second single-ended interface connected to a second signal output line; and	**Toshiba discloses a second single-ended interface (*e.g.*, GTLO2 using Gunning Transceiver Logic (GTL) for single-ended transmissions) connected to a second signal output line (*e.g.*, line from GTLO2 to signal output pad 55b).** **Toshiba discloses that GTLO2 uses GTL[9] to output data to signal output pad 55b through a signal output line at, *e.g.*, Fig. 2 (annotated below); ¶¶ 16, 38, 31, 24, 15, 5; *see also, e.g.*, ¶¶ 31, 39, 9, 11, 12, 22, 25, 26, 32, 35, 36; claims 2, 3, 4; Figs. 1, 3, 4; pp. 36-43; Ex. 1008 ¶¶ 41, 90-93, pp. 137-139.** 
[1.3] a differential interface having a normal signal output connected to the	**Toshiba discloses a differential interface (*e.g.*, LVDSO) having a normal signal output (*e.g.*, normal signal output of LVDSO) connected to the first output line (*e.g.*, line from LVDSO to signal output pad 55a) and a complementary signal output (*e.g.*, complementary signal output of LVDSO) connected to the second signal output line (*e.g.*, line from**

[9] *See* n. 8 (explaining that GTL is used for single-ended transmissions).

Claim 1	Toshiba
first output line and a complementary signal output connected to the second signal output line;	**LVDSO to signal output pad 55b).** **Toshiba discloses that LVDS (Low Voltage Differential Signaling) is used for differential transmissions at, *e.g.*, ¶ 23.[10] Toshiba discloses that LVDSO (emphasis added) uses LVDS to output data to signal output pads 55a and 55b. *See, e.g.*, Fig. 2 (annotated below); ¶¶ 16, 31, 39, 23; Ex. 1008 ¶¶ 84, 94-96, 53, 50, pp. 139-141; *see also, e.g.*, Ex. 1015 at p. 11; Ex. 1014 at p. 4; Ex. 1009 at p. 164; Ex. 1001 1:48; 3:51-52.** 
[1.4] wherein an output of the data interface circuit is selectable between a sin-	**Toshiba discloses that an output of the data interface circuit (*e.g.*, data outputted from signal output pad 55a or 55b) is selectable (*e.g.*, via output buffer selecting signal MODE_O) between a single-ended interface output (*e.g.*, output of GTLO1 or output of GTLO2) and a differential interface output (*e.g.*, output of LVDSO). *See, e.g.*, Ex. 1005 Abstract** ("[Purpose] *To*

[10] LVDS (Low Voltage Differential Signaling), by definition, is a type of differential signaling that requires transmitting a signal via a differential pair of wires, where one wire carries a normal (*i.e.*, true) signal and the other wire carries a complementary signal. *See, e.g.*, Ex. 1015 at p. 11; Ex. 1014 at p. 4; Ex. 1009 at p. 164; Ex. 1001 1:48; 3:51-52; Fig. 3; Ex. 1008 ¶¶ 50, 53, 95.

Claim 1	Toshiba
gle-ended interface output and a differential interface output.	*make it possible to selectively use a differential interface and a single-ended interface* without changing boards, and to broaden peripheral LSI options…"); **¶ 11** ("A third feature of the invention is the provision of an interface circuit having:…*an output buffer selection circuit for outputting an output buffer selection signal in accordance with either a differential transmission mode or a single-ended (hereinafter described as SE) transmission mode for the data outputted from said semiconductor integrated circuit…*"); **Fig. 2 (annotated below)**;  **¶ 31** ("…*An output buffer selecting signal (indicated in the drawing as MODE_O) sent by this signal line (41) is inputted to the LVDS (O), and the inverted signal for MODE_O is inputted to the GTLs (O1, O2)…In short, the LVDS (0) is selected when MODE_O = 1, and the GTLs (O1, O2) are selected when MODE_O = 0.*"); **¶ 39** ("The LVDS alone is enabled when MODE_O=1, and the GTLs (I1, I2) are enabled when MODE_I=0. *Either is outputted to the signal output pads (55a, 55b) from the enabled output buffer.*"); ***see also, e.g., Id.* Figs. 1, 3, 5; claims 1, 2, 3, 4; ¶¶ 16, 27, 29, 30, 35-38; pp. 36-43; Ex. 1008 ¶¶ 84-85, 90, 94, pp. 141-143.**

E. Grounds 5 & 6: Claim 10 is rendered obvious under § 103 over Umeda in view of Roe; Claim 10 is rendered obvious under § 103 over Umeda in view of Toshiba

1. Overview of Umeda

Umeda, "Solid State Image Sensor and Video System Using the Same," was filed on January 30, 1998, issued on September 17, 2002, and is prior art under at least § 102(e). *See* Ex. 1006. Umeda discloses a video system that uses a camera with a CMOS image sensor. *See, e.g.*, Ex. 1008 ¶ 98, pp. 103-106, 144-147. For example, Figure 14 shows a camera (camera 301) that includes "image sensor 100." Ex. 1006 13:35-41, Fig. 14; Ex. 1008 ¶ 98, pp. 103-106, 144-147. Umeda states that image sensor 100 may "use[] a CMOS type image sensor." Ex. 1006. 14:44-48; Ex. 1008 ¶ 98, pp. 104-109, 145-150. Figure 31 is an embodiment of image sensor 100 that could be utilized in camera 301. Ex. 1006 17:52-56; Ex. 1008 ¶ 98, pp. 105-106, 146-147. As shown in Figure 14, camera 301 is connected to PC 300. Ex. 1006 13:60-14:2, Fig. 14; Ex. 1008 ¶ 98, pp. 103-107, 144-148.

Image sensor 100 includes an interface circuit (*e.g.*, "interface section 108") "for outputting digital video data to the outside." *See, e.g.*, Ex. 1006 9:15-17; Fig. 31; Ex. 1008 ¶ 100, pp. 106-109, 147-150. In the embodiment shown in Figure 31, the interface circuit outputs digital video data from the CMOS image sensor to an external image processor (*e.g.*, "video data compression circuit 400" that is "externally connected" to the CMOS image sensor). *See, e.g.*, Ex. 1006 Fig. 31; 18:32-58; Ex. 1008 ¶ 100, pp. 116-118, 157-159. This compression circuit 400 performs various high-speed image processing functions, including motion data compression, on the video data received from the CMOS image sensor. *See, e.g.*, Ex. 1006

18:32-58; 19:24-40; 11:4-9; 2:1-6; Ex. 1008 ¶ 100, pp. 116-118, 157-159. As expressly stated in Umeda, "a large circuit size and high-speed processing are required" for the video compression circuit 400 to process the motion vector data detected by the CMOS image sensor. Ex. 1006 18:32-42.

To accommodate these requirements, a POSITA would have understood that the video compression circuit 400 could have advantageously resided on and utilized a processor residing on a personal computer (*e.g.*, PC 300 in Fig. 14), which has more space and processing power to perform the intensive video compression functions on the motion data received from the CMOS sensor. *See, e.g.*, Ex. 1008 ¶¶ 101-103; Ex. 1006 18:32-42; Fig. 6; 11:20-36; pp. 110, 151.

Umeda explicitly indicates that the communications interface (*e.g.*, interface section 108) in Figure 14 could be a "PC Card, IEEE 1394 interface, or the like." Ex. 1006 Fig. 14; ¶ 98-99, pp. 106, 110-111, 147, 151-152. The IEEE 1394 interface was a well-known interface that supported differential signaling, and PC Cards were well known interfaces that supported single-ended signaling. *See, e.g.*, Ex. 1008 ¶¶ 44- 45, 48, 54, 99; pp. 111, 152, 164, 171.

2. Umeda in Combination with either Roe or Toshiba

a. State of the Art in April 1999

As detailed above in the "Overview of the Field of the Claimed Invention," a POSITA in April 1999 would have understood the state of the art to include: (1)

single-ended and differential interfaces, and their advantages and disadvantages; (2) data interface circuits that could selectively choose between a single-ended and differential interface; and (3) using single-ended and differential interfaces to connect CMOS sensors to image processors. *See* Section IV, Ex. 1008 ¶¶ 35-65.

b. Motivation to Combine Umeda with Roe or Toshiba

A POSITA in April 1999 would have been motivated and would have found it obvious and straightforward to implement Umeda's video system according to either Roe's or Toshiba's teaching of a dual interface. *See* Ex. 1008 ¶¶ 97, 104, pp. 109-15, 150-56. Indeed, Umeda, Roe, and Toshiba are all in the same field of optimizing interface circuits to communicate data and, as explained below, although not actually required for obviousness, they actually include ***express statements*** that would motivate a POSITA to combine their teachings. *Id.*

Umeda, for example, states that "it is urgently necessary to realize a high-performance, high-versatility solid state image sensor using a MOS type image sensor which can meet those demands [*i.e.*, high-performance and high-versatility]" and stresses the requirement of choosing an "appropriate" interface circuit that "make[s] the most of [these] characteristics features." Ex. 1006 1:61-64; Ex. 1008 ¶ 104, pp. 106, 109-110, 147, 150-151. At the same time, Umeda cautions against the selection of an interface that requires a "large number of pins," which would "result in an increase in the chip area of the sensor or the size of the

package" and unavoidably increase costs. *Id.*

Umeda, moreover, discloses that image data from image sensor 100 is sent to an image processor (*e.g.*, video compression circuit 400 in Fig. 31). *See, e.g.*, Ex. 1006, *e.g.*, 18:32-55; 1008 ¶ 100, pp. 110, 116-118, 151, 157-159. As noted above, because video compression requires "a large circuit size and high-speed processing," a POSITA would have been motivated to advantageously implement the video compression circuit such that it resided on and utilized the existing processor in PC 300. *Id.* 18:39-42; Ex. 1008 ¶¶ 102-103, pp. 110-111, 151-152. Umeda lists various single-ended (*e.g.*, "PC Card"), and differential interfaces (*e.g.*, "IEEE 1394") that could interchangeably be used to connect a CMOS image sensor to a personal computer. Ex. 1006 Fig. 14; Ex. 1008 ¶¶ 48, 54, 57, 63, 99; pp. 106, 110-111, 147, 151-152.

Even if the video compression circuit 400 that is "externally connected" to CMOS image sensor 100 is not located on the personal computer (*e.g.*, 300 in Fig. 14), a POSITA would still have found it advantageous for the interface circuit in the CMOS image sensor to be compatible with both single-ended and differential signaling. Ex. 1008 ¶ 103, pp. 111-112, 152-153. Indeed, Umeda explicitly highlights signaling compatibility as a way for an image sensor to achieve higher versatility and "easily cope with existing systems." Ex. 1006 27:51-55; Ex. 1008 ¶ 103, pp. 111-112, 152-153. While Umeda lists compatibility with both analog and digi-

tal signals as an example of increasing versatility, a POSITA would have recognized that existing video compression circuits could be configured to receive either single-ended or differential signals. Ex. 1008 ¶¶ 103, 47-48, 57, 63, pp. 111-112, 152-153. As a result, to achieve a "highly versatile" CMOS sensor and to better "cope with existing" video compression circuits, a POSITA would have been motivated to utilize an interface circuit that is compatible with both single-ended and differential signaling. *Id.* ¶ 103, pp. 111-112, 152-153.

Thus, in summary, Umeda provides strong motivations for a POSITA to implement an interface circuit that fulfills the following demands: (1) enhancing the versatility and performance of the CMOS image sensor by providing compatibility with both single-ended and differential signals, and (2) minimizing pin and board usage, which reduces costs. Roe's or Toshiba's teaching of dual interfaces meet these very demands. *Id.* ¶¶ 66-70, 83-88, 97, 99, 101-104, pp. 109-115, 150-156.

Roe's dual interface, for example, is capable of receiving and sending I/O signals in both single-ended and differential modes, thereby enhancing the performance (especially in differential mode) and versatility of image sensors, as "urgently" desired by Umeda. *See, e.g*, Ex. 1004 5:51-53; Ex. 1008 ¶¶ 67-70, pp. 113. Further, Roe's dual interface circuit reuses the same pins to output data from both single-ended and differential interfaces, thereby reducing chip size and cost due to reduced pin count and board space, as desired by Umeda. Ex. 1004 5:41-63; Ex.

1008 ¶¶ 70, pp. 113. Indeed, Roe highlights these reductions as among the chief benefits of its dual interface. *See, e.g.,* Ex. 1004 5:51-53; Ex. 1008 at pp. 113.

Furthermore, in addition to disclosing single-ended interfaces, Roe repeatedly refers to the "IEEE 1394" standard as a target application for its dual-purpose I/O circuit and even incorporates one of the earlier specifications (P1394 draft 8.0 Version 2) by reference. *See, e.g.*, Ex. 1004 Abstract; Fig. 2a; 1:56-2:4; 5:3-6, 5:24-35; Ex. 1008 ¶ 69, pp. 112-113. The IEEE 1394 standard was developed for the express purpose of providing high speed data transfer for peripheral video applications. *See, e.g.*, Ex. 1017 at pp. 4, 293; Ex. 1016 at pp. 16, 26; Ex. 1008 ¶ 45, 54, pp. 112-113. Indeed, the standard discloses connecting a video camera to a computer CPU through the IEEE 1394 interface – the same configuration as the video system disclosed in Umeda. Ex. 1017 at p. 263; Ex. 1008 ¶ 69, pp. 112-113. Indeed, as mentioned above, Umeda itself lists the IEEE 1394 interface as a suitable interface for connecting a CMOS sensor to a personal computer in its video system. Ex. 1006 Fig. 14; Ex. 1008 ¶¶ 98-99, pp. 106, 110-111, 147, 151-152. Taken together, these overlapping teachings of Umeda and Roe further confirm how well their two systems fit together, thereby providing yet another motivation for a POSITA to implement the interface in Umeda according to the teachings of Roe. Ex. 1008 at pp. 110-115.

Toshiba, similarly, discloses a dual interface that "selectively use[s] a differ-

ential interface and an SE [single-ended] interface" via a selection signal (*e.g.*, MODE_O) to output data to peripheral devices, thereby enhancing the performance and versatility of image sensors, as "urgently" desired by Umeda. Ex. 1005 ¶ 7; Ex. 1008 ¶ 84, 104, pp. 152-155. Further, Toshiba discloses that its I/O circuit provides these benefits "without changing boards." Ex. 1005 ¶ 7; Ex. 1008 ¶ 88, pp.153-154. In particular, Toshiba reuses the ***same pins*** to output data from both single-ended and differential interfaces, thereby reducing chip size and cost due to reduced pin count and board space. Ex. 1005 ¶ 7; Ex. 1008 ¶¶ 84, 88, 93, 96, pp. 153-154. Thus, Toshiba's dual interface provides high versatility and performance while minimizing pin count and cost and, for the same reasons as discussed above, a POSITA would be motivated to apply Toshiba's advantageous teachings of a dual interface in implementing Umeda. Ex. 1008 ¶ 87-88, pp. 150-156.

Implementing Umeda's video system using Roe's or Toshiba's teachings of dual interfaces would have been routine and well within the knowledge and skill of a POSITA. *Id*. at p. 113-115, 154-156. Both Roe and Toshiba expressly state that their interfaces can be used for ***any*** integrated circuit in ***any*** application involving the reception and transmission of signals. *See* Ex. 1004 3:46-49; Ex. 1005 ¶¶ 16, 28, 37, 41, Ex. 1008 at pp. 109, 150. Single-ended and differential interfaces are fundamental circuits and were well known in April 1999. *See*, *e.g.*, Ex. 1012 at pp. 1-10; Ex. 1009 at pp. 155-157; Ex. 1010 at pp. 55-66; Ex. 1005 ¶¶ 24, 15, 5; Ex.

1001 1:35-2:37; Ex. 1004 3:4-9; Ex. 1011 at pp. 60-61; 64-67; *see also* Ex. 1013; Ex. 1014; Ex. 1015; Ex. 1008 ¶¶ 38-45, 49-56, pp. 110-111, 151-152. The specific interfaces disclosed by both Roe and Toshiba use standard, well known components, such as circuits for driving both single- and differential-signals off-chip via the bonding pads, and could be readily implemented using known methods that were well within the skill of a POSITA. *Id*. at pp. 114, 155. For example, it would have been routine for a POSITA to use known methods to design a photo detector, readout circuitry, and interface circuitry. *Id*. The combination of these standard components assembled according to known methods would have been understood by a POSITA to yield an expected, predictable result. *Id.* at pp. 113-14, 155-56.

A POSITA, moreover, would have been familiar with industry trends in interface design and would have understood that compatibility with both existing single-ended and differential interfaces was important in the marketplace. *See, e.g.*, Ex. 1012 at p. 1; Ex. 1010 at p. 63; Ex. 1005 ¶¶ 5-6; Ex. 1006 2:44-52; Ex. 1018 at p. 5; Ex. 1008 ¶ 64, pp. 114, 156. A POSITA also would have understood that even though the industry was trending toward differential interfaces, the industry also placed importance on the option for a single-ended interface to ensure compatibility with existing external devices that used single-ended interfaces. *See, e.g.*, *id.* ¶¶ 51, 55-56, 38, pp. 111-13, 153-55. The industry demands to support both single-ended and differential interfaces while minimizing pin count and cost

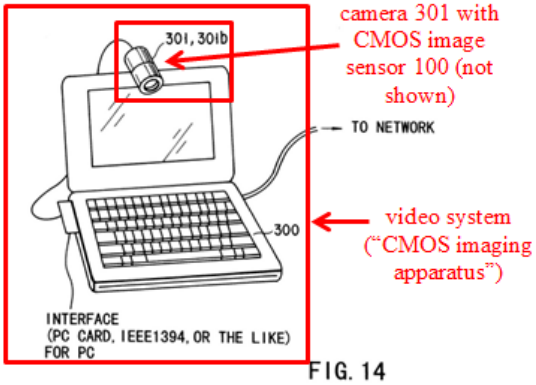
provide a further motivation to use Roe's and Toshiba's teaching of dual interfaces in implanting the video system of Umeda. *See, e.g. id.* ¶¶ 64, 70, 88, pp. 114, 156.

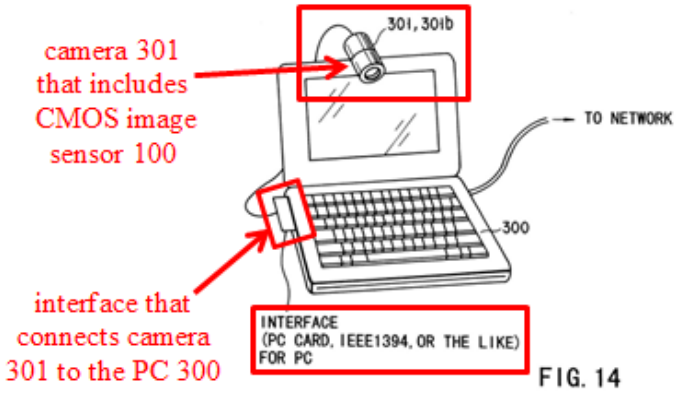
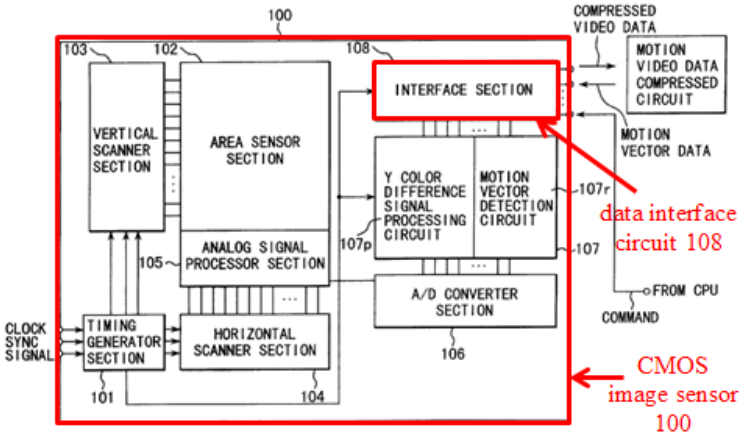
In summary, Umeda expressly discloses single-ended and differential interfaces and explicitly suggests using a data interface that meets certain design goals: high versatility and performance while minimizing chip size and cost. *See, e.g., id.* ¶¶ 104, 99, pp. 109-11, 150-51. These very design goals are met by the data interfaces taught by Roe and Toshiba. *Id.* at pp. 112-13, 153-55. And implementing the data interfaces of Roe and Toshiba in the video system of Umeda would have been routine, consistent with industry trends and demands, and well within the knowledge and skill of a POSITA. *Id.* at pp. 113-15, 155-56. Accordingly, it would have been obvious to a POSITA to use the teachings of the dual interface of either Roe or Toshiba to interface the CMOS sensor and image processor in Umeda, as required by claim 10. *See, e.g., id.* ¶¶ 97, 104, pp. 109-115, 150-56.

3. Claim 10 is rendered obvious under § 103 over Umeda in view of Roe (Ground 5); Claim 10 is rendered obvious under § 103 over Umeda in view of Toshiba (Ground 6)

As detailed in the chart below, Umeda in view of Roe or Toshiba discloses (in the exemplary excerpts and cites provided herein) each and every limitation of claim 10, rendering it unpatentable as obvious under § 103.

Claim 10	**Umeda in view of Roe or Toshiba**
[Preamble] A CMOS imaging	**Umeda discloses a CMOS imaging apparatus (*e.g.*, video system of Fig. 14, which uses a camera with a CMOS image**

Claim 10	Umeda in view of Roe or Toshiba
apparatus comprising:	**sensor 100). *See, e.g.*, Ex. 1006 1:6-8** ("*The present invention relates to the structure of a solid state image sensor and a system using the solid state image sensor.*"); **2:55-60** ("It is an object of the present invention to provide a compact, *high-performance solid state image sensor having high general versatility and using a MOS type image sensor capable of energy-saving. It is another object of the present invention to provide a video system using this solid state image sensor.*"); **13:21-35** ("*a camera 301 using the image sensor 100 of the present invention, as shown in FIG. 14, i.e., a system in which a camera 301a for a personal computer is connected to a personal computer 300* through an IF (interface)…"); **14:44-48** ("For example, *an image sensor 100 of the present invention uses a CMOS type image sensor as an area sensor*…"); **Fig. 14 (annotated below)**;  FIG. 14 ***See also e.g.*, 1:59-2:6; 2:55-5:14; 5:56-62; 6:1-6; 6:56-58; 8:47-51; 9:19-26; 13:36-14:19; 19:24-40; Fig. 1; 5:23-25; 9:1-18; Fig. 17; 14:19-23; Fig. 88; 27:16-63; 31; 18:32-58; 16:57-65; 5:57-59; 5:63-67; 8:47-51; Figs. 13, 15-16, 18, 39; Fig. 31; 18:32-58; 14:44-48; Ex. 1008 ¶¶ 98, 100, pp. 103-06, 146-47.**
[10.1] a CMOS image sensor, the sensor having a data interface circuit comprising:	**Umeda discloses a CMOS image sensor (*e.g.*, CMOS image sensor 100 used in the video system of Fig. 14), the sensor having a data interface circuit (*e.g.*, interface section 108). *See, e.g.*, 5:60-62** ("FIG. 14 is a perspective view of a personal computer to which the *solid state image sensor* of the present invention is connected."); **13:21-35** ("a camera 301 using the *image sensor 100 of the present invention*, as shown in FIG. 14, *i.e.*, a system in which a camera 301a for a personal computer is

Claim 10	Umeda in view of Roe or Toshiba
	connected to a personal computer 300 through an IF (interface)…"); **14:44-48** ("For example, *an image sensor 100 of the present invention uses a CMOS type image sensor as an area sensor*…"); **Fig. 14 (annotated below)**;  FIG. 14 **5:23-25** ("FIG. 1 is a block diagram showing the *basic structure of a solid state image sensor* according to an embodiment of the present invention."); **9:1-18** ("…FIG. 1 is a block diagram showing the schematic internal structure of an image sensor according to an embodiment of the present invention. Referring to FIG. 1, *an image sensor 100 incorporates …an area sensor section 102,*…and *an interface section 108 for outputting digital video data to the outside and receiving command data from the outside.*"); **Fig. 31 (annotated below);**  FIG. 31 ***See also e.g.*, Fig. 1; 1:60-67; 2:44-52; 9:27-38; 11:1-9; 12:43-64; 17:66-18:58; 20:20-49; 27:10-30:64; 27:46-31:5; Figs. 2-8, 13, 15-18, 30, 37-45, 47, 49-55, 57, 58, 62, 64, 66, 68, 70-72, 78, 88, 89, 90; Ex. 1008 ¶¶ 99-100, pp. 106-09, 147-50.**

Claim 10	Umeda in view of Roe or Toshiba
[10.2] a first single-ended interface [of the data interface circuit of element 10.1] connected to a first signal output line;	**Umeda discloses a data interface circuit of a CMOS image sensor (*e.g.*, interface section 108). *See* element [10.1].** **Roe[11] discloses a data interface circuit (*e.g.*, dual-purpose I/O circuit 116) comprising a first single-ended interface (*e.g.*, first single-ended output buffer 202 in Fig. 3) connected to a first signal output line. *See supra,* claim element [1.1] in view of Roe.** **Alternatively, Toshiba[12] also discloses a data interface circuit (*e.g.*, I/O circuit) comprising a first single-ended interface (*e.g.*, GTLO1) connected to a first signal output line (*e.g.*, line from GTLO1 to signal output pad 55a). *See supra,* claim element [1.1] in view of Toshiba.**
[10.3] a second single-ended interface [of the data interface circuit of 10.1]	**Umeda discloses a data interface circuit of a CMOS image sensor (*e.g.*, interface section 108). *See, supra,* claim element [10.1].** **Roe[13] discloses a data interface circuit (*e.g.*, dual-purpose**

[11] A POSITA would have been motivated and would have found it obvious to implement the data interface in Umeda's CMOS sensor according to the teachings of Roe's dual interface for at least the reasons discussed in Section E.2, *supra*. Thus, Umeda in combination with Roe renders this claim element obvious.

[12] A POSITA would have been motivated and would have found it obvious to implement the data interface in Umeda's CMOS sensor according to the teachings of Toshiba's dual interface for at least the reasons discussed in Section E.2, *supra*. Thus, Umeda in combination with Toshiba renders this claim element obvious.

[13] *See*, *supra, n.* 11.

Claim 10	Umeda in view of Roe or Toshiba
connected to a second signal output line; and	**I/O circuit 116) comprising a second single-ended interface (*e.g.*, second single-ended output buffer 204 in Fig. 3) connected to a second signal output line. *See supra,* claim element [1.2] in view of Roe.** **Alternatively, Toshiba[14] also discloses a data interface circuit (*e.g.*, I/O circuit) comprising a second single-ended interface (*e.g.*, GTLO2) connected to a second signal output line (*e.g.*, line from GTLO2 to signal output pad 55b). *See supra,* claim element [1.2] in view of Toshiba.**
[10.4] a differential interface [of the data interface circuit of 10.1] having a normal signal output connected to the first output line and a complementary signal output connected to the second signal output line;	**Umeda discloses a data interface circuit of a CMOS image sensor (*e.g.*, interface section 108). *See, supra,* claim element [10.1].** **Roe[15] discloses a data interface circuit (*e.g.*, dual-purpose I/O circuit 116) comprising a differential interface (*e.g.*, differential output buffer 210) having a normal signal output (*e.g.*, positive differential I/O signal) connected to the first output line and a complementary signal output (*e.g.*, negative differential I/O signal) connected to the second signal output line. *See supra,* claim element [1.3] in view of Roe.** **Alternatively, Toshiba[16] also discloses a data interface circuit (*e.g.*, I/O circuit) comprising a differential interface (*e.g.*, LVDSO) having a normal signal output (*e.g.*, normal signal output of LVDSO) connected to the first output line (*e.g.*, line from LVDSO to signal output pad 55a) and a complementary signal output (*e.g.*, complementary signal output of LVDSO) connected to the second signal output line (*e.g.*, line from LVDSO to signal output pad 55b). *See supra,* claim element [1.3] in view of Toshiba.**

[14] *See*, *supra*, *n.*12.

[15] *See*, *supra*, *n.* 11.

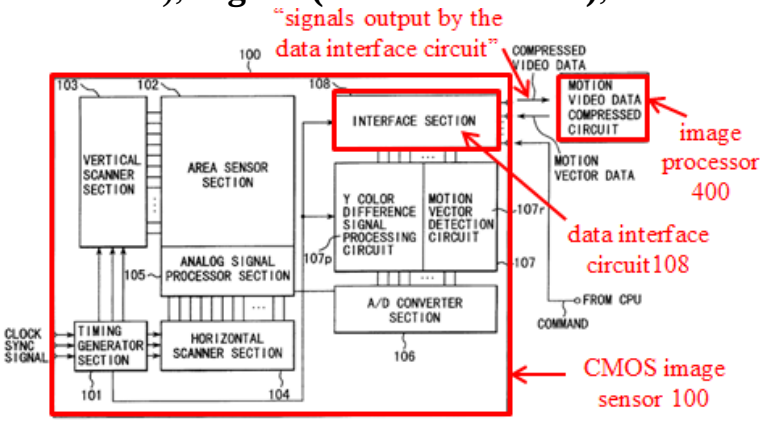
[16] *See*, *supra*, *n.* 12.

Claim 10	Umeda in view of Roe or Toshiba
[10.5] wherein an output of the data interface circuit is selectable between a single-ended interface output and a differential interface output.	**Umeda discloses a data interface circuit of a CMOS image sensor (*e.g.*, interface section 108). *See, supra,* claim element [10.1].** **Roe[17] discloses a data interface circuit (*e.g.*, dual-purpose I/O circuit 116), wherein an output of the data interface circuit (*e.g.*, I/O signal outputted from conducting pads 120a or 120b) is selectable (*e.g.*, via an enable/disable signal DIFF_EN) between a single-ended interface output (*e.g.*, output from first single-ended output buffer 202 or output from second single-ended output buffer 204 in Fig. 3 when DIFF_EN is logical low) and a differential interface output (*e.g.*, output from differential output buffer 210 in Fig. 3 when DIFF_EN is logical high). *See supra,* claim element [1.4] in view of Roe.** **Alternatively, Toshiba[18] also discloses a data interface circuit (*e.g.*, I/O circuit), wherein an output (*e.g.*, data outputted from output pad 55a or 55b) of the data interface circuit is selectable (*e.g.*, via output buffer selecting signal MODE_O) between a single-ended interface output (*e.g.*, output of GTLO1 or output of GTLO2 when MODE_O is set to 0) and a differential interface output (*e.g.*, output of LVDSO when MODE_O is set to 1). *See supra*, claim element [1.4] in view of Toshiba.**
[10.6] an image processor connected to the CMOS image sensor to receive the signals out-	**Umeda discloses an image processor (*e.g.*, video data compression circuit 400) connected to the CMOS image sensor (*e.g.*, CMOS type image sensor 100) to receive the signals output by the data interface circuit[19] (*e.g.*, interface section 108). *See, e.g.*, Ex. 1006 18:32-58** ("*When the video data compression circuit 400 is externally connected to the image*

[17] *See*, *supra*, n. 11.

[18] *See*, *supra*, n. 12.

[19] *See*, *supra*, element 10.2 and n. 11, n. 12.

Claim 10	Umeda in view of Roe or Toshiba
put by the data interface circuit.	*sensor 100, as shown in FIG. 31, the motion vector detected by the digital signal processor section 107 in the image sensor 100 is encoded and sent to the video data compression circuit 400 on the next stage through the interface section 108...*" *Id.* 18:32-58."); **Fig. 31 (annotated below)**;  FIG. 31 **17:52-57** ("*[A] video data compression circuit 400 for compressing motion video data follows the image sensor 100, as shown in FIG. 31.* The image sensor incorporates a motion vector detection circuit 107r."); ***see also*, *e.g.*, 2:1-6; 2:55-5:14; 11:4-9; 18:55-19:9; 19:24-41; 27:16-62; Figs. 13, 14, 17, 39, 40, 41, 88; Ex. 1008 ¶¶ 98-100, pp. 116-118, 157-59**.

F. Grounds 7 & 8: Claim 10 is rendered obvious under § 103 over Sears in view of Roe; Claim 10 is rendered obvious under § 103 over Sears in view of Toshiba

1. Overview of Sears

Sears, titled "Voice-Output Reading System with Gesture-Based Navigation," was filed on October 22, 1998, and issued to Ascent Technology, Inc. on September 5, 2000, is prior art under at least § 102(e). Sears discloses an electronic reading system that includes a camera with a CMOS imaging sensor that communicates with a main system computer over a communications interface, such as

the "IEEE 1394" interface.[20] *See, e.g.*, Ex. 1007 6:58-65; Ex. 1008 ¶¶ 106, 108, pp. 119-20. Sears discloses that the choice of interface is selected based on factors such as cost and throughput. *See, e.g.*, Ex. 1008 ¶¶ 106, pp. 121, 122, 162, 163. The main system performs various image processing functions on the image data received from the CMOS image sensor. *See, e.g., id.* 5:34-67; 7:34-65; 7:1-12; Ex. 1008 ¶ 107, pp. 129, 161. A POSITA would have known that the CMOS sensor would have necessarily included a data interface circuit in order to transfer image data over the communications interface to the main system computer. Ex. 1008 ¶ 107, pp. 120, 129, 161, 170. Simply put, without the data interface circuit, there would be no way for the data to be transferred to the main system computer. Thus, Sears inherently discloses a data interface circuit as part of the CMOS sensor. *Id.* To the extent it is not inherently disclosed, it would have been obvious to a POSITA to implement a data interface circuit in the CMOS sensor. Ex. 1008 ¶ 107.

To increase the performance and reduce costs of Sears' electronic reading

[20] While the October 22, 1998 filing date of the application that led to Sears is sufficient to establish Sears as prior art under 102(e), Petitioner notes that Sears' parent, Appln. No. 08/930,156, filed February 11, 1997, also discloses a CMOS camera that communicates with a computing device (*e.g.*, a processor) over a communications interface. *See, e.g.*, Ex 1029 at pp. 25-28, 32-33, 121-22, 131, 134.

system, Sears explicitly encourages the use of "ubiquitous" general-purpose computers to perform the computationally intensive image processing functions of the electronic reading system. Ex. 1007 26:59-27:8; 27:22-33; 5:34-44; 7:1-23; Ex. 1008 ¶ 108, p. 123. To interoperate with these various computers, the CMOS sensor of Sears' electronic reading system should be compatible with a wide variety of communications interfaces. Ex. 1008 ¶¶ 106, 108, pp. 123, 164. As explicitly listed in Sears, "the image sensor may communicate through various means with the main system 35 computer, including the parallel, universal serial bus (USB), IEEE 1394, or 16-bit PCMCIA or 32-bit (CardBus)." Ex. 1007 6:58-65.

2. Sears in Combination with Roe or Toshiba

a. State of the Art in April 1999

As stated above, a POSITA in April 1999 would have understood the state of the art to include: (1) single-ended and differential interfaces, and their advantages and disadvantages; (2) data interface circuits that could selectively choose between a single-ended and differential interface; and (3) using single-ended and differential interfaces to connect CMOS image sensors to image processors. *See* Section IV.B, Ex. 1008 ¶¶ 35-65.

b. Motivation to Combine Sears with Roe or Toshiba

A POSITA in April 1999 would have been motivated and would have found it obvious and straightforward to use either Roe's or Toshiba's teaching of a dual

interface in the electronic reading system of Sears. *See* Ex. 1008 ¶¶ 105, 108, pp. 122, 163; *Dystar Textilfarben GMBH v. C.H. Patrick Co.*, 464 F.3d 1356 (Fed. Cir. 2006). Indeed, Sears, Roe, and Toshiba are all in the same field of art of optimizing interface circuits to communicate data and, as explained below, although not actually required for obviousness, they actually include *express statements* that would motivate a POSITA to combine their teachings. Ex. 1008 at pp. 122, 163.

Sears teaches that the selection of the interface connecting CMOS imaging sensor 41 to the main system 35 computer is based on factors such as cost and throughput. *See, e.g.*, Ex. 1007 6:52-57; Ex. 1008 ¶¶ 105-106, pp. 122, 163. Further, to increase the performance and reduce the costs of Sears' electronic reading system, Sears encourages the use of general-purpose computers to perform the computationally intensive image processing functions of the electronic reading system. *See, e.g.*, Ex. 1007 26:59-27:8; Ex. 1008 ¶ 108, pp. 123, 164. As stated in Sears, these computers "are becoming ubiquitous in office and home environments" and provide "computing power necessary, as well as ancillary input and output devices…Thus, the price of the system for the end-user who already has a suitable computer will be very inexpensive." Ex. 1007 26:59-27:8.

Sears highlights the portability of its electronic reading system as an advantageous feature that provides greater usage flexibility for its users. For example, Sears states that its electronic reading system is "easily made portable," *e.g.*, as an

eyeglass or a fingertip apparatus, "so that reading can be performed wherever and whenever printed material is encountered, whether at school, at work, at the store or at a restaurant." Ex. 1007 27:56-65; Figs. 3, 4, 5a-d; Ex. 1008 at pp. 123, 164.

Sears, moreover, discloses using both single-ended and differential interfaces to connect a CMOS image sensor to an image processor. Ex. 1007 6:58-65; Ex. 1008 ¶¶ 106, pp. 123-24. With respect to single-ended interfaces, Sears discloses that a "16-bit PCMCIA or 32-bit (CardBus) connections" could be used to connect the CMOS image sensor to an image processor. *Id.* A POSITA would have recognized that such interfaces (and various other interfaces such as SCSI, RS-232, RS-423) were well-known interfaces that supported single-ended signaling and could have been readily used as the interface to transfer image data from Sears' CMOS imaging sensor to a greater number of main system computers (*e.g.*, older personal computers) with conventional interfaces that only supported single-ended transmission. Ex. 1008 ¶¶ 41-44, 51-54, pp. 123-24. Sears also explicitly discloses that the IEEE 1394 differential interface could be used as the interface to transmit image data from CMOS sensor to a main system computer to perform computationally-intensive image processing functions. *See, e.g.*, Ex. 1007 6:58-65; 27:31-34; 5:34-44; 7:1-23; Ex. 1008 ¶¶ 106-107, p. 123. Thus, in summary, Sears expressly teaches using both single-ended and differential interfaces and selecting a data interface that enables it to achieve the expressly stated desirable goals of

high throughput, low cost, increased portability and compatibility with general purpose computers. Ex. 1008 ¶¶ 106, 108-109, pp. 122-23.

Roe's and Toshiba's express teachings of dual interfaces meet the precise requirements and goals Sears sets forth for its data interface circuit. Ex. 1008 at pp. 122-27, 162-69. Roe and Toshiba both each disclose a data interface with both single-ended and differential interfaces that provide high throughput and high compatibility with peripheral devices while minimizing cost and enhancing portability. *Id.* ¶¶ 70, 87-88, pp. 122-26, 162-67. These data interfaces are compatible with a wide range of interfaces to allow connection to a greater variety of personal computers. *Id*. This increased compatibility enhances the throughput and lowers the cost of Sears' CMOS imaging sensor, design goals that are expressly desired in Sears. *See, e.g.,* Ex. 1007 6:52-57; Ex. 1008 ¶¶ 108, pp. 122-26, 162-67.

Roe's dual interface, for example, is capable of receiving and sending I/O signals in both single-ended and differential modes, thereby enhancing the performance (especially in differential mode), as expressly desired by Sears, and versatility of image sensors, which enables the CMOS imaging sensor in Sears to be interoperable with a greater variety of main system 35 processors. Ex. 1004, *e.g.*, 5:51-53; Ex. 1008 ¶¶ 66-70, 108, pp. 122-25. Further, Roe's dual interface reuses ***the same pins*** to output data from both single-ended and differential interfaces. *See, e.g.*, Ex. 1004 5:41-63; Ex. 1008 ¶¶ 70, p. 25. This reuse of pins and board

space for both interfaces reduces chip cost and enhances portability, both of which are expressly desired in Sears. Ex. 1008 at p. 125. Indeed, Roe highlights the reductions in chip cost and size as among the chief benefits of its dual interface. *See, e.g.*, Ex. 1004 5:51-53; Ex. 1008 at p. 113.

Furthermore, as detailed above, Roe repeatedly refers to the "IEEE 1394" standard (a differential interface developed for the purpose of providing high speed data transfer for video applications) as a target application to be supported by its dual interface. *See, e.g., id.* Abstract; Fig. 2a; 5:3-6, 5:24-35; Ex. 1008 ¶ 69, p. 125. And, as noted above, the standard discloses a system that connects a video camera to a computer through the IEEE 1394 interface. *See, e.g.*, Ex. 1017 at pp. 4, 293; Ex. 1016 at pp. 16, 26; Ex. 1008 ¶ 45, 54, pp. 112-13. Sears, in fact, discloses that an IEEE 1394 interface can be used to interface an image sensor to a computer. Ex. 1007 6:58-65; Ex. 1008 ¶ 106, p. 125. Taken together, these disclosures in both Sears and Roe further confirm how well their two systems fit together, thereby providing yet another motivation for a POSITA to implement the interface in Sears according to the teachings of Roe. Ex. 1008 at pp. 125-26.

Toshiba discloses a dual interface that "selectively use[s] a differential interface and an SE [single-ended] interface" via a selection signal (*e.g.,* MODE_O) to output data to peripheral devices, thereby enhancing data throughput and compatibility with external devices, as desired in Sears. Ex. 1005 ¶ 7; Ex. 1008 ¶¶ 84, 104,

pp. 166. Further, Toshiba discloses that such an interface provides these benefits "without changing boards." Ex. 1005 ¶ 7; Ex. 1008 ¶ 88, p. 167. In particular, Toshiba reuses ***the same pins*** to output data from both single-ended and differential interfaces, thereby reducing chip size and cost due to reduced pin count and board space. Ex. 1005 ¶ 7; Ex. 1008 ¶¶ 84, 88, 93, 96, p. 167 . Thus, Toshiba's dual interface provides high versatility and performance while minimizing pin count and cost and, for the same reasons as discussed above, a POSITA would be motivated to apply Toshiba's advantageous teachings of a dual interface in implementing Sears. Ex. 1008 ¶¶ 87-88, pp.163-69.

Implementing the electronic reading system of Sears using Roe's or Toshiba's teachings of a dual interface would have been routine and well within the knowledge and skill of a POSITA. Ex. 1008 pp. 126, 168. Both Roe and Toshiba expressly state that their interfaces can be used for *any* integrated circuit in *any* application involving the reception and transmission of signals. *See*, *e.g.*, Ex. 1004 3:46-49; Ex. 1005 ¶¶ 16, 28, 37, 41. Single-ended and differential interfaces are fundamental circuits and were well known in April 1999. Ex. 1008 at pp. *See*, *e.g.*, Ex. 1012 at pp. 1-10; Ex. 1009 at pp. 155-157; Ex. 1010 at pp. 55-66; Ex. 1005 ¶¶ 24, 15, 5; Ex. 1001 1:35-2:37; Ex. 1004 3:4-9; Ex. 1011 at pp. 60-61; 64-67; *see also* Ex. 1013; Ex. 1014; Ex. 1015; Ex. 1008 ¶¶ 38-45, 49-56, pp. 123-124, 130, 151-152. The specific interfaces disclosed by both Roe and Toshiba use standard,

well known components, such as circuits for driving both single- and differential-signals off-chip via the bonding pads, and could be readily implemented using known methods that were well within the skill of a POSITA. *Id*. at pp. 126-27, 167-68. For example, it would have been routine for a POSITA to use known methods to design a photo detector, readout circuitry, and interface circuitry. *Id*.. The combination of these standard components assembled according to known methods would have been understood by a POSITA to yield an expected, predictable result. *See, e.g., id.*.

A POSITA, moreover, would have been familiar with industry trends in interface design and would have understood that compatibility with both existing standards for single-ended and differential interfaces was extremely important. *See, e.g.*, Ex. 1012 at p. 1; Ex. 1010 at p. 63; Ex. 1005 ¶¶ 5-6; Ex. 1006 2:44-52; Ex. 1018 at p. 5; Ex. 1008 ¶ 64, pp. 123-25, 164-65. A POSITA also would have understood that even though the industry in April 1999 was trending toward differential interfaces, the industry also placed importance on the option for a single-ended interface to ensure compatibility with existing devices that used single-ended interfaces. *See, e.g.*, Ex. 1008 ¶¶ 51, 55-56, 38, pp. 124-25; 165-67. The industry demands to support both single-ended and differential interfaces while minimizing pin count and cost provide a further motivation to use Roe's and Toshiba's teach-

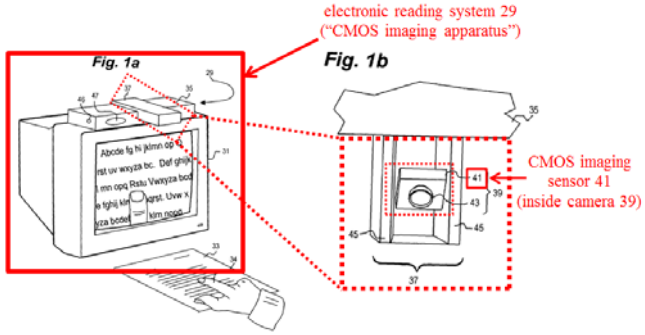
ings of dual interfaces in implementing the electronic reading system of Sears. *See, e.g. id.* ¶¶ 64, 70, 88, pp. 125-26, 167.

In summary, Sears expressly discloses single-ended and differential interfaces and strongly suggests using a data interface that meets certain design goals: high versatility and performance while minimizing chip size and cost. *Id.* ¶¶ 106, 108. These very design goals are met by Roe's and Toshiba's teachings of dual interfaces. *Id.* at pp. 124-26, 165-67. And implementing the dual interfaces as taught by Roe and Toshiba in the electronic reading system of Sears would have been routine, consistent with industry trends and demands, and well within the knowledge and skill of a POSITA. *Id.* at pp. 126-27, 167-69. Accordingly, it would have been obvious to a POSITA to use teachings of the dual interface of either Roe or Toshiba to interface the CMOS image sensor and image processor in Sears, as required by Challenged Claim 10. *Id.* ¶ 105, 108, pp. 122-27, 163-69.

3. Claim 10 is rendered obvious under § 103 over Sears in view of Roe; Claim 10 is rendered obvious under § 103 over Sears in view of Toshiba

As detailed in the chart below, Sears in view of Roe or Toshiba discloses (in the exemplary excerpts and cites provided herein) each and every limitation of claim 10, rendering it unpatentable as obvious under § 103. Ex. 1008 ¶ 110.

Claim 10	**Sears in view of Roe or Toshiba**
[Preamble] A CMOS imaging	**Sears discloses a CMOS imaging apparatus (*e.g.*, electronic reading machine 29 that uses a camera 39 with a CMOS**

Claim 10	Sears in view of Roe or Toshiba
apparatus comprising:	**imaging sensor 41).** ***See, e.g.*****, Ex. 1007 4:62-5:12** ("FIG. 1a is a perspective diagram of the first preferred embodiment of the present invention. *The electronic reading machine 29* is mounted on top of a video monitor 31 with the field of view onto the surface below on which printed material 33 is placed…*The electronic reading machine 29 comprises a main system 35, from which a camera mount 33[sic] protrudes. The camera mount 37 comprises one or more electronic imaging devices* (such as CCD or *CMOS 35[sic] cameras*). *A view of the camera mount 37 from the underside is shown in FIG. 1b, a perspective diagram. A camera 39,* which may comprise a CCD or *CMOS imaging sensor 41* along with an attached lens 43, is angled away from the main system 35 . . . ."); **Figs. 1a, 1b (annotated below)**;  **5:34-43** ("The image or images obtained by the camera 39 are transmitted to an electronic computing device located within the main system 35…"); **Ex. 1008 ¶¶ 106, pp. 119-20, 160-61.**
[10.1] a CMOS image sensor, the	**Sears discloses a CMOS image sensor (*e.g.*, CMOS imaging sensor 41), the sensor having a data interface circuit.[21]** ***See,***

[21] The CMOS imaging sensor 41 in Sears communicates with main system computer 35 over a communications interface (*e.g.*, USB, IEEE 1394 PCMCIA, CardBus, etc.). In order to transfer signals over the communications interface to main system 35 computer, CMOS imaging sensor 41 disclosed in Sears would necessarily, and thus inherently, include a data interface circuit. Ex. 1008 ¶ 107, pp. 120.

Claim 10	Sears in view of Roe or Toshiba
sensor having a data interface circuit comprising:	***e.g.*, 6:52-67**("*Either CMOS or CCD sensors may be used for the image sensor 41*, and are selected on the basis of cost, pixel density, noise and other variables. *The image sensor may communicate through various means with the main system 35 computer, including parallel, universal serial bus (USB), IEEE 1394, or 16-bit (PCMCIA) or 32-bit (CardBus) connections . . .* . The choice of communications interface is made on the basis of cost, throughput, and DMA capabilities."); ***see also id*. Figs. 1a, 1b; 5:7-12; 4:62-5:6; Figs. 3-5; 5:34-43; 3:66-4:19; 16:11-26:58; claim 31; Ex. 1008 ¶¶ 107, pp. 120-22, 161-63.**
[10.2] a first single-ended interface [of the data interface circuit of 10.1] connected to a first signal output line;	**Sears discloses a data interface circuit. *See, supra,* claim element [10.1] and n. 21.** **Roe[22] discloses a data interface circuit (*e.g.,* dual-purpose I/O circuit 116) comprising a first single-ended interface (*e.g.,* first single-ended output buffer 202 in Fig. 3) connected to a first signal output line. *See supra,* claim element [1.1] in view of Roe.** **Alternatively, Toshiba[23] also discloses a data interface cir-**

To the extent it is not inherently disclosed, it would have been obvious to a POSITA to implement a data interface circuit in the CMOS sensor. Ex. 1008 ¶ 107.

[22]A POSITA would have been motivated and would have found it obvious to implement the data interface in Sears' sensor according to the teachings of Roe's dual interface for at least the reasons discussed in Section F.2, *supra*. Thus, Sears in combination with Roe renders this element obvious. Ex. 1008 at pp. 122-27.

[23] A POSITA would have been motivated and found it obvious to implement the data interface circuit in Sears' sensor according to the teachings of Toshiba's dual

Claim 10	Sears in view of Roe or Toshiba
	cuit (*e.g.*, I/O circuit) comprising a first single-ended interface (*e.g.*, GTLO1) connected to a first signal output line (*e.g.*, line from GTLO1 to signal output pad 55a). *See supra,* claim element [1.1] in view of Toshiba.
[10.3] a second single-ended interface [of the data interface circuit of 10.1] connected to a second signal output line; and	**Sears discloses a data interface circuit. *See, supra,* claim element [10.1] and n. 21.** **Roe[24] discloses a data interface circuit (*e.g.*, dual-purpose I/O circuit 116) comprising a second single-ended interface (*e.g.*, second single-ended output buffer 204 in Fig. 3) connected to a second signal output line. *See supra,* claim element [1.2] in view of Roe.** **Alternatively, Toshiba[25] also discloses a data interface circuit (*e.g.*, I/O circuit) comprising a second single-ended interface (*e.g.*, GTLO2) connected to a second signal output line (*e.g.*, line from GTLO2 to signal output pad 55b). *See supra,* claim element [1.2] in view of Toshiba.**
[10.4] a differential interface [of the data interface circuit of 10.1] having a normal signal output connected to the first output line and a complementary signal	**Sears discloses a data interface circuit. *See, supra,* claim element [10.1] and n. 21.** **Roe[26] discloses a data interface circuit (*e.g.*, dual-purpose I/O circuit 116) comprising a differential interface (*e.g.*, differential output buffer 210) having a normal signal output (*e.g.*, positive differential I/O signal) connected to the first output line and a complementary signal output (*e.g.*, negative differential I/O signal) connected to the second signal output line. *See supra,* claim element [1.3] in view of Roe.**

interface for at least the reasons discussed in Section F.2, *supra*. Thus, Sears in combination with Toshiba renders this element obvious. Ex. 1008 at pp. 163-69.

[24] *See*, *supra*, n. 22.

[25] *See*, *supra*, n. 23.

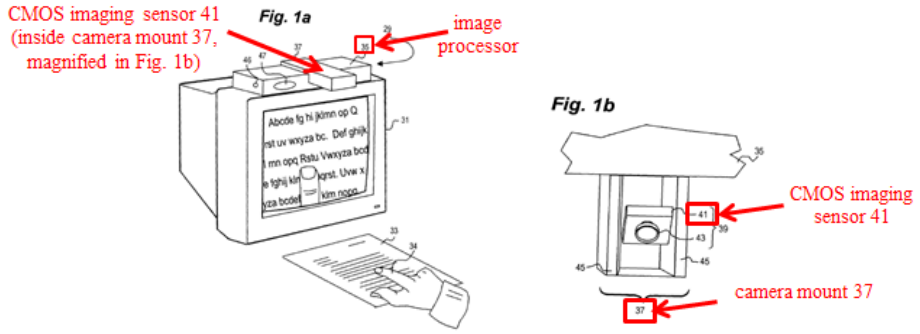
[26] *See*, *supra*, n. 22.

Claim 10	Sears in view of Roe or Toshiba
output connected to the second signal output line;	**Alternatively, Toshiba[27] also discloses a data interface circuit (*e.g.*, I/O circuit) comprising a differential interface (*e.g.*, LVDSO) having a normal signal output (*e.g.*, normal signal output of LVDSO) connected to the first output line (*e.g.*, line from LVDSO to signal output pad 55a) and a complementary signal output (*e.g.*, complementary signal output of LVDSO) connected to the second signal output line (*e.g.*, line from LVDSO to signal output pad 55b). *See supra*, claim element [1.3] in view of Toshiba.**
[10.5] wherein an output of the data interface circuit is selectable between a single-ended interface output and a differential interface output.	**Sears discloses a data interface circuit. *See, supra*, claim element [10.1] and n. 21.** **Roe[28] discloses a data interface circuit (*e.g.*, dual-purpose I/O circuit 116), wherein an output (*e.g.*, I/O signal outputted from conducting pads 120a or 120b) of the data interface circuit is selectable (*e.g.*, via an enable/disable signal DIFF_EN) between a single-ended interface output (*e.g.*, output from first single-ended output buffer 202 or output from second single-ended output buffer 204 in Fig. 3) and a differential interface output (*e.g.*, output from differential output buffer 210 in Fig. 3). *See supra*, claim element [1.4] in view of Roe.** **Alternatively, Toshiba[29] also discloses a data interface circuit (*e.g.*, I/O circuit), wherein an output (*e.g.*, data outputted from output pad 55a or 55b) of the data interface circuit is selectable (*e.g.*, via output buffer selecting signal MODE_O) between a single-ended interface output (*e.g.*, output of GTLO1 or output of GTLO2) and a differential interface output (*e.g.*, output of LVDSO). *See supra*, claim**

[27] *See*, *supra*, n. 23.

[28] *See*, *supra*, n. 22.

[29] *See*, *supra*, n. 23.

Claim 10	Sears in view of Roe or Toshiba
	element [1.4] in view of Toshiba.
[10.6] an image processor connected to the CMOS image sensor to receive the signals output by the data interface circuit.	**Sears discloses an image processor (*e.g.*, main system 35) connected to the CMOS image sensor (*e.g.*, CMOS imaging sensor 41) to receive the signals output by the data interface circuit.**[30] ***See, e.g.*, Ex. 1007 5:34-67** ("*The image or images obtained by the camera 39 are transmitted to an electronic computing device located within the main system 35.* The device may comprise either a general-purpose personal computer, or an embedded computer optimized for use in the reading system. *The computing device processes the images in order to optimize the contrast and brightness of the image, and then further processes the image in order to extract textual information (e.g. by optical character recognition (OCR)) or to interpret graphical information.*"); **6:52-67** ("*…Either CMOS or CCD sensors may be used for the image sensor 41*, and are selected on the basis of cost, pixel density, noise and other variables. *The image sensor may communicate through various means with the main system 35 computer, including parallel, universal serial bus (USB), IEEE 1394, or 16-bit (PCMCIA) or 32-bit (CardBus) connections* . . . . The choice of communications interface is made on the basis of cost, throughput, and DMA capabilities."); **Fig. 1a and 1b (annotated below)**;  ***see, e.g.*, 7:1-12, 34-65; Figs. 3-5; 4:62-5:12; 6:34-48; 14:56-15:22; 16:11-27:8; Ex. 1008 ¶ 107, pp. 129-132, 170-74**.

[30] *See supra*, element 10.2 (Sears in view of Roe or Toshiba), n. 21, n. 22, n. 23.

VI. CONCLUSION

Because this Petition, if unrebutted, shows that there is a reasonable likelihood that these claims are unpatentable, Petitioner requests this Petition be instituted and the Challenged Claims be found unpatentable and canceled. Per §§ 1.33(c), 42.105, and 42.100, a copy of the present Request, in its entirety, is being served on the Patent Owner at the address of record as reflected in the publicly available records of the PTO as designated in the PAIR system. The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this proceeding by this firm) to Deposit Account 06-1075, under Order No. 110797-0018-651.

Respectfully submitted by: /J. Steven Baughman/ May 21, 2015

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

United States Patent No: 6,836,290	§	Attorney Docket No.:
Inventors: Randall M. Chung,	§	110797-0018-651
Ferry Gunawan,	§	
Dino D. Trotta	§	Customer No.: 28120
Formerly Application No.: 09/302,090	§	
Issue Date: December 28, 2004	§	Petitioner:
Filing Date: April 29, 1999	§	Samsung Electronics Co. Ltd.
Former Group Art Unit: 2612	§	Samsung Electronics America, Inc.
Former Examiner: Ngoc Yen T Vu	§	Samsung Semiconductor, Inc.

For: COMBINED SINGLE-ENDED AND DIFFERENTIAL SIGNALING INTERFACE

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Alexandria, Virginia 22313-1450

CERTIFICATE OF SERVICE

It is certified that a copy of the following documents has been served in its entirety on the patent owner as provided in 37 CFR § 42.205:

1. Petition For Inter Partes Review Of United States Patent No. 6,836,290 and accompanying exhibits:

Exhibit	Description
Ex. 1001	U.S. Patent No. 6,836,290
Ex. 1002	File History to U.S. Patent No. 6,836,290
Ex. 1003	File History to U.S. Patent Application No. 09/062,343
Ex. 1004	U.S Patent No. 5,929,655 (“Roe”)
Ex. 1005	Japanese Patent Publication No. 1997-006592 (“Toshiba”)

Ex. 1006	U.S. Patent No. 6,452,632 ("Umeda")
Ex. 1007	U.S. Patent No. 6,115,482 ("Sears")
Ex. 1008	Expert Declaration of R. Jacob Baker
Ex. 1009	Electronic Packaging of High Speed Circuitry," Stephen G. Konsowski and Arden R. Helland, McGraw-Hill (1997)
Ex. 1010	"Microcomputer Interfacing," Harold S. Stone, Addison-Wesley Publishing Company(1982)
Ex. 1011	"Interfacing Techniques in Digital Design with Emphasis on Microprocessors," Ronald L. Krutz, John Wiley & Sons(1988)
Ex. 1012	"Summary of Well Known Interface Standards," John Goldie, National Semiconductor Corporation (July 1998)
Ex. 1013	"An Overview of LVDS Technology," John Goldie, National Semiconductor Corporation (July 1998)
Ex. 1014	"LVDS Owner's Manual," National Semiconductor (Spring 1997)
Ex. 1015	"IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)," IEEE Computer Society (1996)
Ex. 1016	"Universal Serial Bus Specification," Compaq Computer Corporation et al. (January 15, 1996)
Ex. 1017	"IEEE P1394 Draft 8.0v2, " IEEE Standards Department (July 7, 1995)
Ex. 1018	"A General Control System For Imaging Arrays," Unewisse et al., Measurement Science & Technology, Vol. 5, No. 4 (April 1994)
Ex. 1019	"Dual Differential (EIA-4220A)/Quad Single-Ended (EIA-423-A) Line Drivers," Motorola Inc. (1995)
Ex. 1020	U.S. Patent No. 5,751,978 ("Tipple")
Ex. 1021	U.S. Patent No. 5,715,409 ("Bucher")
Ex. 1022	U.S. Patent No. 4,441,125 ("Parkinson ")
Ex. 1023	"MicronEye Operator's Manual," Micron Technology Incorporated (1984)
Ex. 1024	"The Programmer's Guide to SCSI," Brian Sawert, Addison-Wesley (1998)
Ex. 1025	"+5 V Powered RS-232/RS-422 Transceiver AD7306," Analog Devices (8/1994)

Ex. 1026	Joint Claim Construction and Prehearing Statement in *Imperium IP Holdings (Cayman), Ltd. V. Samsung Electronics Co., Ltd.*, case no. 4:14-cv-00371ALM (E.D. Tex.), Dkt No.86
Ex. 1027	"The MicronEye," Dr. Chris Wieland, Byte Magazine, Vol. 8, No. 10 (October 1983)
Ex. 1028	DAQCard™ -500 User Manual: Multifunction I/O Card for Type II PCMCIA Bus," National Instruments Corporation (1996)
Ex. 1029	File History to U.S. Patent Application No. 08/930,156
Ex. 1030	Declaration of William M. Serra

The copy has been served on May21, 2015 by causing the aforementioned documents to be deposited in the United States Postal Service as Express Mail (Label No. EF 070 059 612 US) postage pre-paid in an envelope addressed to:

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Respectfully submitted,

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/s/ Ginny Blundell