UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILERGY CORPORATION

Petitioner

v.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner

Patent No. 8,283,758

Title: MICROELECTRONIC PACKAGES WITH ENHANCED HEAT DISSIPATION AND METHODS OF MANUFACTURING

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,283,758 CHALLENGING CLAIMS 1-7

TABLE OF CONTENTS

Page

TABLE OF CONTENTS
(continued)

Page

EXHIBIT LIST

Exhibit #	*Description*
Ex. 1001	U.S. Patent No. 8,283,758 to Jiang
Ex. 1002	File History of U.S. Patent No. 8,283,758
Ex. 1003	Declaration of Professor R. Jacob Baker, Ph.D.
Ex. 1004	U.S. Patent No. 5,508,556 to Lin ("Lin '556")
Ex. 1005	U.S. Patent No. 7,705,476 to Bayan et al. ("Bayan")
Ex. 1006	U.S. Patent No. 7,221,055 to Lange ("Lange")
Ex. 1007	U.S. Patent No. 8,330,270 to Lin et al. ("Lin '270")
Ex. 1008	U.S. Patent No. 8,680,658 to Shi et al. ("Shi")
Ex. 1009	U.S. Patent No. 7,384,826 to Richieri
Ex. 1010	U.S. Patent No. 6,376,910 to Munoz
Ex. 1011	Y. Xiao et al., *Flip-Chip Flex-Circuit Packaging for 42V/16A Integrated Power Electronics Module Applications*, in proceedings of the 17th Annual IEEE Applied Power Electronics Conference and Exposition (March 2002)
Ex. 1012	Sung K. Kang et al, *An Overview of Pb-free, Flip-Chip Wafer Bumping Technologies,* IBM Research Report RC24582 (June 11, 2008)
Ex. 1013	The Institute of Electrical and Electronics Engineers, "The New IEEE Standard Dictionary of Electrical and Electronics Terms," Fifth Edition 1993, p. 1488
Ex. 1014	McGraw-Hill, Inc., "McGraw-Hill Dictionary of Scientific and Technical Terms," Fifth Edition 1994, p. 2163
Ex. 1015	Curriculum Vitae of Professor R. Jacob Baker, Ph.D.
Ex. 1016	ADVANCED ELECTRONIC PACKAGING (William D. Brown, ed., 1999) (excerpts)
Ex. 1017	HANDBOOK OF LEAD-FREE SOLDER TECHNOLOGY FOR MICROELECTRONIC ASSEMBLIES (Karl J. Puttlitz & Kathleen A. Stalter, eds., 2004) (excerpts)

PETITION FOR *INTER PARTES* REVIEW

Pursuant to the provisions of 35 U.S.C. § 311 and 37 C.F.R. § 42.100 *et seq*., Petitioner Silergy Corporation ("Silergy") hereby petitions the Patent Trial and Appeal Board to institute an *Inter Partes* Review ("IPR") of claims 1-7 of United States Patent No. 8,283,758 ("the '758 patent," Ex. 1001) that issued on October 9, 2012 to Hunt Hang Jiang and, according to USPTO records, is assigned to Monolithic Power Systems, Inc. ("MPS" or "Patent Owner").

I. MANDATORY NOTICES

A. Real Parties-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner identifies Silergy Corporation, Silergy Technology, Compal Electronics, Inc., and Bizcom Electronics, Inc. as real parties-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

As of the filing date of this petition, the '758 patent is involved in litigation in the Northern District of California, captioned *Monolithic Power Systems, Inc. v. Silergy Corporation, et al.*, Case No. 3:14-cv-01745-VC, which was originally filed as Case No. 2:13-cv-08122-MWF in the Central District of California, and then transferred to the Northern District of California on April 14, 2014. Petitioner is not aware of any other judicial or administrative matter involving the '758 patent

that would affect, or be affected by, a decision in the requested IPR.[1]

C. Lead and Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Pursuant to 37 C.F.R. §§ 42.8(b)(3) and 42.10(a), Petitioner designates counsel as follows:

Lead Counsel	***Back-up Counsel***
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D. Service Information Under 37 C.F.R. §§ 42.8(b)(4)

Pursuant to 37 C.F.R. §42.8(b)(4), counsel agrees to service by mail as detailed above, and to electronic service by email to the email address silergy_ipr.service@morganlewis.com.

E. Power of Attorney Under 37 C.F.R. § 42.10(b)

A Power of Attorney executed by Petitioner accompanies this Petition.

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[1] Petitioner has concurrently filed a Petition for *inter partes* review of U.S. Patent No. 8,361,899, also asserted in the U.S. District Court Proceeding.

F. Payment of Fees Under 37 C.F.R. § 42.103(a)

The required fees are submitted herewith. If any additional fees are due at any time during this proceeding, the Office is authorized to charge such fees to Deposit Account No. 50-0310 (order no. 0002519-00-0008).

G. Service on the Patent Owner

Pursuant to 37 C.F.R. § 42.105(a), this Petition and its exhibits were served simultaneously with this filing on Patent Owner at the correspondence address of record on file at the USPTO for the '758 patent, as shown in the attached Certificate of Service. This petition and its exhibits were also electronically served on MPS' counsel in the above-referenced Northern District of California proceeding.

II. GROUNDS FOR STANDING

Pursuant to 37 C.F.R. § 42.104, Petitioner certifies that the '758 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the claims of the '758 patent because it is not a party to any other post-grant or *inter partes* review of the '758 patent. This petition is filed within one year of real party-in-interest Silergy Technology being served (on February 24, 2014) with a complaint for infringement of the '758 patent. Petitioner has not filed any separate civil actions challenging the validity of any claims of the '758 patent.

III. THE '758 PATENT AND ITS PROSECUTION

A. Summary of the '758 Patent

The '758 patent relates to semiconductor packaging—a very crowded field. In particular, it is directed to managing the heat generated while a semiconductor device, such as a chip, is operating.

To achieve "enhanced heat dissipation," the '758 patent claims a variety of elements: a thermally conductive material attached to a semiconductor die and exposed through the encapsulant to aid in heat dissipation, barrier layers to prevent diffusion, solder balls connecting the die to the leadframe, solder paste to transfer heat away from the chip, and materials like alloys of titanium, nickel, and silver chosen for their adhesive, thermal, or electrical properties. Fig. 5 of the '758 patent (annotated below) illustrates these elements:

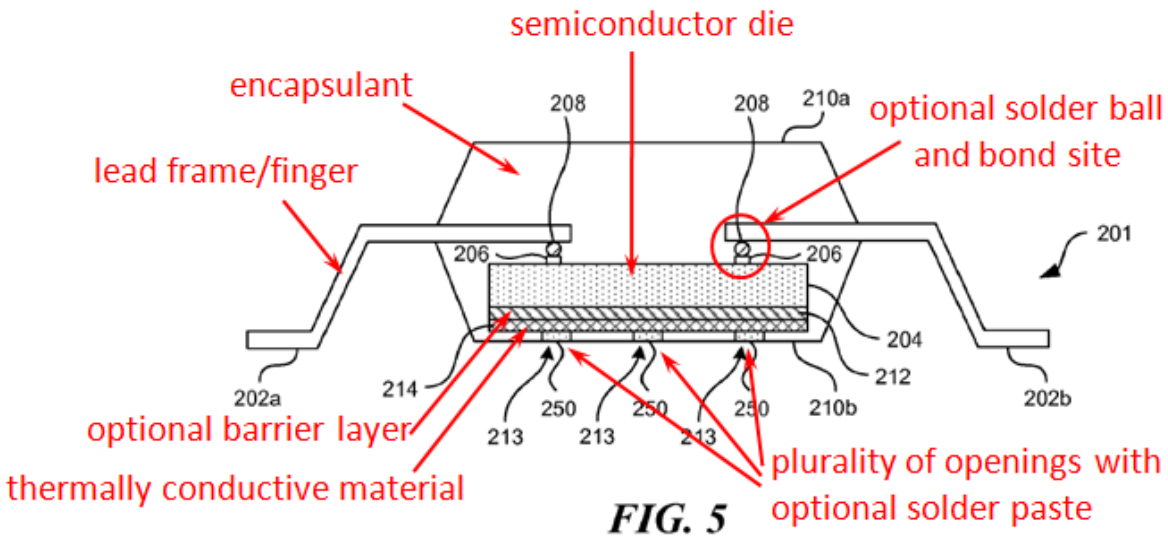


FIG. 5

As will be shown below, however, the '758 patent merely collects and

rearranges a variety of well-known prior art elements. Thermally conductive materials attached to the die, openings in the encapsulant, barrier layers, solder balls, solder paste and titanium/nickel/silver alloys were known, described and used in the art long before the '758 patent was filed. *See* Ex. 1003 at ¶¶ 35-38. Indeed, during prosecution, struggling to find any novel subject matter, the Applicant resorted to importing into each independent claim a limitation requiring the encapsulant to have a "plurality of openings"—a limitation supported by only a single sentence in the last substantive paragraph of the specification.

B. Prosecution History of the '758 Patent

The application that led to the '758 patent was filed on December 16, 2010, and included 3 independent claims and 17 dependent claims. Ex. 1002 at 13-19. After an election in response to a restriction requirement, 2 independent claims and 13 dependent claims remained. *Id.* at 45-51. These elected independent claims lacked the limitations of a "plurality of openings in the encapsulant" and the limitations that the thermally conductive material must be exposed through this plurality of openings. *See id.* claims 1 & 8.[2] Instead, these limitations appeared in dependent claims. *See, e.g., id.* claims 3, 6, 14. In a non-final Office Action, the examiner rejected each of the claims over an application that later issued as Bayan (here, Ex. 1005) and U.S. Publication 2007/0018291 ("Huang"). Ex. 1002 at 55-

[2] Original claims 1 and 8 issued as amended claims 1 and 5, respectively.

67.

In response, the Applicant amended the independent claims to include the limitations from the dependent claims requiring a plurality of openings and exposing the thermally conductive material through the openings, and cancelled or amended the dependent claims accordingly. Ex. 1002 at 76-83, 88-91. After these amendments, the remaining 7 claims were allowed. Ex. 1002 at 92-99.

IV. STATEMENT OF THE RELIEF REQUESTED

A. Challenged Claims and Statutory Grounds of Challenge

Petitioner asks that the Board review the accompanying prior art and analysis, institute a trial for *inter partes* review of claims 1-7 of the '758 patent, and cancel those claims as unpatentable under 35 U.S.C. §§ 102 and 103, based on one or more of the following five grounds:

	Statute	***References***	***Claims***
1	35 U.S.C. § 102(b)	Lin '556	5
2	35 U.S.C. § 103(a)	Lin '556 in combination with Bayan	1-4, 6-7
3	35 U.S.C. § 103(a)	Lin '556 in combination with Bayan and further in view of Lange	2
4	35 U.S.C. § 102(e)	Lin '270	5
5	35 U.S.C. § 102(b)	Shi	5

The application that led to the '758 patent was filed on December 16, 2010 and claims no earlier priority.

U.S. Patent No. 5,508,556 to Lin, entitled "Leaded Semiconductor Device Having Accessible Power Supply Pad Terminals" ("Lin '556" or "Ex. 1004"), was

issued on April 16, 1996. Lin '556 is prior art to the '758 patent under pre-AIA 35 U.S.C. § 102(b) because it was issued more than one year before the '758 patent's priority date.

U.S. Patent No. 7,705,476 to Bayan et al., entitled "Integrated Circuit Package" ("Bayan" or "Ex. 1005"), was published on May 7, 2009. Bayan is prior art to the '758 patent under pre-AIA 35 U.S.C. § 102(b) because it was published more than one year before the '758 patent's priority date.

U.S. Patent No. 7,221,055 to Lange, entitled "System and Method for Die Attach Using a Backside Heat Spreader" ("Lange" or "Ex. 1006"), was published on November 23, 2006. Lange is prior art to the '758 patent under pre-AIA 35 U.S.C. § 102(b) because it was published more than one year before the '758 patent's priority date.

U.S. Patent No. 8,330,270 to Lin et al., entitled "Integrated Circuit Package Having a Plurality of Spaced Apart Pad Portions" ("Lin '270" or "Ex. 1007"), was filed on December 9, 2004. Lin '270 is prior art to the '758 patent under pre-AIA 35 U.S.C. § 102(e) because it was filed before the '758 patent's priority date.

U.S. Patent No. 8,680,658 to Shi et al., entitled "Conductive Clip for Semiconductor Device Package" ("Shi" or "Ex. 1008"), was published on December 3, 2009. Shi is prior art to the '758 patent under pre-AIA 35 U.S.C.

§ 102(b) because it was published more than one year before the '758 patent's priority date.

The application that led to the issuance of Bayan (Ex. 1005) was considered by the Examiner during prosecution of the '758 patent, but not in combination with Lin '556 or Lange. None of Petitioner's grounds relies solely on Bayan, and Petitioner presents different arguments and additional evidence not considered by the PTO, including the declaration of R. Jacob Baker, Ph.D. Thus, Bayan is a proper ground for *inter partes* review. *See Chimei Innolux Corp. v. Semiconductor Energy Laboratory Co., Ltd.,* IPR2013-00038, Paper No. 9 at 6 (instituting *inter partes* review despite Patent Owner's objection under 35 U.S.C. § 325(d) that certain of the prior art references had been considered by the Examiner during prosecution.) None of the other identified prior art references was before the Patent Office during prosecution of the '758 patent.

B. The Person of Ordinary Skill in the Art

As explained by Dr. R. Jacob Baker, who is an expert in this field, a person of ordinary skill in the art at the time of the '758 patent's invention would have had at least a bachelor's degree in Electrical Engineering, Computer Engineering. or a related field and 1-2 years of experience in semiconductor packaging. Ex. 1003 at ¶¶ 24-25.

C. Claim Construction

Pursuant to 37 C.F.R. § 42.100(b), and for purposes of this petition and *inter partes* review, Petitioner construes the claim language to give claim terms their broadest reasonable interpretation in light of the specification. *In re Am. Acad. of Sci. Tech Ctr*., 367 F.3d 1359, 1364, 1369 (Fed. Cir. 2004). Because this standard differs from the standard applied by district courts, *see id.*, Petitioner reserves the right to argue alternative constructions in any district court or appellate litigation.

1. "thermally conductive material"

One of ordinary skill in the art, or even a layperson, can appreciate that "thermally conductive material" should encompass "a material capable of transferring heat" (as opposed to a material which retards or prevents the transfer of heat, *i.e.*, an insulator) especially given that the '758 patent's title contains the phrase "enhanced heat dissipation." The '758 patent describes "thermally conductive material" expansively but does not deviate from that conceptual understanding. Despite initially describing "thermally conductive material" self-referentially as "a material that is thermally conductive" (Ex. 1001 at 3:22-23), the '758 patent's specification then recites a wide variety of exemplary (if mostly metallic) thermally conductive materials: a titanium/nickel/silver tri-metal alloy; copper, aluminum or silver; metals or metal alloys (*see id.* at 3:27-32); and a copper or aluminum foil (*id*. at 5:37-38), which are all known to be capable of

transferring heat. Based on this expansive and non-limiting discussion, one of ordinary skill in the art would appreciate that a thermally conductive material must be one that transfers heat (as opposed to retarding the transfer of heat like an insulator) and thus understand that the broadest reasonable interpretation of "thermally conductive material," in light of the specification, is indeed "a material capable of transferring heat." *See* Ex. 1003 at ¶¶ 31, 45.

2. "formed on the second side of the semiconductor die"

According to the '758 patent's specification, the thermally conductive material can be formed on the second side of the semiconductor die "using CVD [chemical vapor deposition], ALD [atomic layer deposition], sputtering, electro-deposition and/or other suitable techniques," and may be "screen-printed, adhesively attached, and/or otherwise bonded to the optional barrier material." Ex. 1001 at 4:47-53. The thermally conductive material is not limited to a material "*deposited* onto the optional barrier material" but may also be "*preformed and fastened* to the semiconductor die using other suitable mechanisms." *Id.* at 5:30-35 (emphasis added). The thermally conductive material can include "a thermally conductive foil (e.g. a copper or aluminum foil)" or a "preform having a thermally conductive layer and an adhesive layer," and may be attached "either before or after encapsulation with the encapsulant." *Id*. at 5:35-45 (numerals omitted). One of ordinary skill in the art, reading these passages, would find that the '758 patent's

specification places hardly any limit on how the thermally conductive material is "formed on" the die—the material can be "formed" on the second side of the semiconductor in almost *any* conceivable way. Ex. 1003 at ¶¶ 46-48. What is consistent, however, is that the material must be "on" the second side of the die (or on the optional barrier material on the second side of the die). Ex. 1003 at ¶ 49. Reflecting this spatial limitation, the broadest reasonable interpretation of "formed on the second side of the semiconductor die," in light of the specification, is "disposed at the second side of the semiconductor die."

3. "generally solderable"

Solder is one of the most basic substances used in semiconductor packaging, and one of ordinary skill in the art would readily understand that if a material is "solderable," it means that the material can be easily attached with heated solder (*e.g.*, during a reflow process). Ex. 1003 at ¶¶ 32, 52. A person of ordinary skill would also appreciate that a "solderable" material is typically metallic, and thus also both thermally and electrically conductive. Ex. 1003 at ¶¶ 50, 52. Lest there be any doubt, the '758 patent explicitly defines the term, consistent with that understanding: "As used herein, the term 'solderable' generally refers to having a material property that permits ready attachment with a solder during reflow." Ex. 1001 at 3:23-26. Two sentences later, that definition is repeated more succinctly as "attachable to a solder during reflow." *Id.* at 3:31. Therefore, the broadest

reasonable interpretation of "generally solderable," in light of the specification, is "readily attachable with a solder during reflow."

4. "barrier material"

A "barrier material" is one of the additional limitations of dependent claim 2. There is, however, no plain and ordinary meaning of "barrier material" in the semiconductor packaging field. Ex. 1003 at ¶ 54. The '758 patent explains that the "optional barrier material 212 is between the semiconductor die and the thermally conductive material 214." Ex. 1001 at 3:4-6. But the "optional barrier material" is of course, optional, and so "may be omitted." *Id.* at 3:7. As to the nature of the "barrier material," the '758 patent recites a wide variety of properties. It can include insulating materials such as silicon oxide or silicon nitride. *Id*. at 3:14-15. But it can also include refractory metals like Tantalum, Tungsten, and Rhenium (*Id.* at 2:16-18), which are conductive of both heat and electricity. Ex. 1003 at ¶ 54. Moreover, the barrier material can also "include a combination of the foregoing materials arranged in layers and/or in a homogeneous form." Ex. 1001 at 2:20-21. And, just as with the thermally conductive material, the '758 patent does not limit how the barrier material is formed, saying only that techniques for forming it "can include chemical vapor deposition ('CVD'), atomic layer deposition ('ALD'), and/or other suitable deposition techniques." *Id.* at 3:42-44. In light of this expansive and non-limiting discussion of "barrier material," all that is

certain is that the barrier material, if present, must be between the die and the thermally conductive material. Thus, the broadest reasonable interpretation of "barrier material" in light of the specification is "a material disposed between the die and the thermally conductive material." Ex. 1003 at ¶ 56.

5. "in series"

The term "in series" is used to describe the sequential arrangement of the semiconductor die, the optional barrier material, and the thermally conductive material in claim 2 ("wherein the barrier material and the thermally conductive material are formed on the second side of the semiconductor die *in series*") and claim 5 ("the semiconductor die further including a thermally conductive material formed on the second side of the semiconductor die *in series*"). The term appears nowhere in the specification of the '758 patent, but, as discussed above with respect to "barrier material," the specification discloses a semiconductor die, then an optional barrier material formed on the second side, and then a thermally conductive material formed on the barrier material (or, if no barrier material is present, formed on the second side of the semiconductor die.) Ex. 1001 at 3:1-9. One of ordinary skill in the art would thus appreciate that "in series" embodies the relative sequence of these elements, one after the other: the die, *then* the barrier material, *then* the thermally conductive material. Ex. 1003 at ¶ 58. Thus, "in series," interpreted most broadly in light of the specification, means "in sequence."

D. Legal Standards

1. Anticipation Under 35 U.S.C. § 102

A claim is anticipated if every element set forth in the claim is present, either expressly or inherently, in a single prior art reference. MPEP § 2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631(Fed. Cir. 1987)). An element is inherently present if an additional reference or extrinsic evidence makes clear that "the missing descriptive matter is necessarily present in the thing described in the reference." MPEP § 2131.01(III) (citing *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991)).

2. Obviousness Under 35 U.S.C. § 103(a)

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill at the time of invention. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

V. DETAILED GROUNDS FOR UNPATENTABILITY

As shown in Ground 1 below, Lin '556 discloses all of the elements and limitations of, and thus anticipates, independent claim 5.

Ground 2 is the combination of Lin '556 and Bayan, which it would have been obvious for one of ordinary skill in the art to combine. Lin '556 discloses all of the elements and limitations of independent claim 1 except for solder balls, which are taught by Bayan. Similarly, Bayan discloses all of the elements and

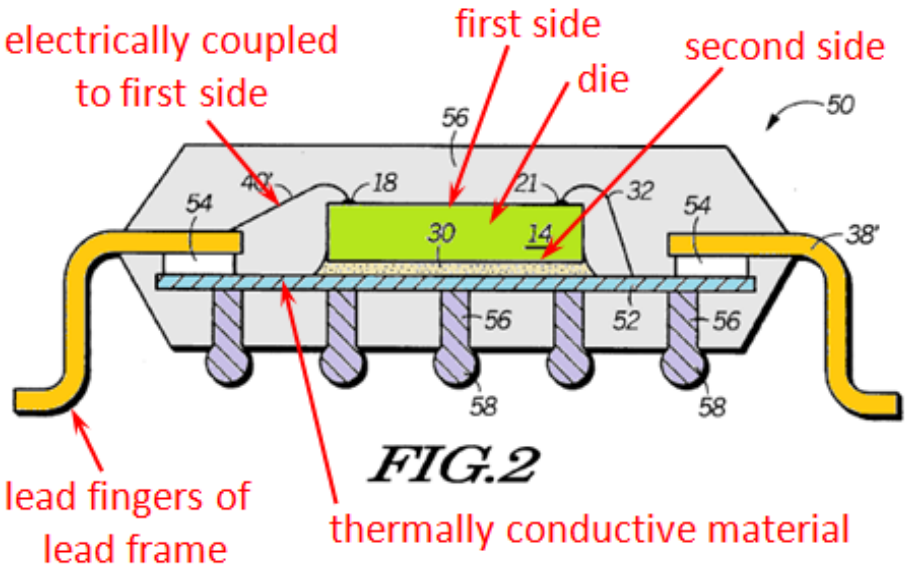
limitations of claim 1 except for a plurality of openings, which are taught by Lin '556. Lin '556 also discloses the additional limitations of dependent claim 2 (a barrier material and a lead finger extending partially beyond the encapsulant), claim 3 (recessing the thermally conductive material in the openings), and claim 4 (solder paste in the openings). In addition, Bayan discloses the additional limitation of claim 6 (a titanium/nickel/silver alloy), and the combination of Lin '556 and Bayan thus discloses the additional limitations of claim 7 (titanium/ nickel/silver alloy in contact with solder paste.)

In Ground 3, to the extent that the combination of Lin '556 and Bayan do not disclose a barrier material, Lange discloses a barrier material, and it would have been obvious to a person of ordinary skill to combine those references.

In Ground 4, Lin '270 is shown to anticipate claim 5, and in Ground 5, Shi is also shown to anticipate claim 5.

A. Ground 1: Claim 5 is anticipated under 35 U.S.C. § 102(b) by Lin '556.

Claim 5 as disclosed by Lin '556
5. A microelectronic package, comprising:
"The present invention relates to a semiconductor device in general, and more specifically, to a *leaded semiconductor device having accessible power supply pad terminals underneath the package body* and a method for making the same." Lin '556 (Ex. 1004) at 1:16-19 (emphasis added); *see also* Ex. 1004 at Abstract (describing the structure and packaging of the invention).

(5.a)[3] a semiconductor die having a first side and a second side opposite the first side, the semiconductor die further including a thermally conductive material formed on the second side of the semiconductor die in series;
"*The semiconductor die 14 is mounted onto a ground plane 52* which is nonplanar with the leads 38'. … *The adhesive 30 used to attach the die to the ground plane can be either electrically conductive or insulative, although in either case it is preferably thermally conductive*." Lin '556 (Ex. 1004) at 4:22-28 (emphasis added).    FIG.2 Ex. 1004 at Fig. 2 (annotated). "The insulative tape 54 *prevents the ground plane 52 from shorting to the leads* 38'." Lin '556 (Ex. 1004) at 4:32-33 (emphasis added). "The ground bonding pad 21 is *connected to the ground plane 52 with wire bonds* 32." Lin '556 (Ex. 1004) at 4:37-39 (emphasis added). "Ground solder bumps 58 are disposed along the bottom surface of the package body to provide the external electrical connections to the ground plane 52." Lin '556 (Ex. 1004) at 4:58-60. "[A] third embodiment of the present invention … is substantially similar to that shown in FIG. 2 with a variation in the ground plane element. The ground plane 62 is composed of a *metallic mesh instead of a solid plane*." Lin '556 (Ex. 1004) at 5:8-14 (emphasis added).
(5.b) a lead frame proximate the semiconductor die, the lead frame having a lead finger electrically coupled to the first side of the semiconductor die;

[3] Claim indices (*i.e.*, 1.a, 1.b, …) are provided in the charts for ease of reference.

"The signal *bonding pad 18 of the semiconductor die 14 is connected to the lead 38' with wire bond 40'*." Lin '556 (Ex. 1004) at 4:34-35 (emphasis added). *See also id.* at Fig. 2, above.

"Signal bonding pads (18) on the die are wire bonded to corresponding leads (38) of a leadframe." Lin '556 (Ex. 1004) at Abstract.

(5.c) an encapsulant at least partially encapsulating the semiconductor die and the lead frame, the encapsulant having a first surface opposite a second surface, and the encapsulant also including a plurality of openings extending toward the semiconductor die from the second surface; and

"Also illustrated in FIG. 2 is a *plastic package body 56 which encapsulates the semiconductor die 14, the bonding wires 18 and 32, the ground plane 52, and a portion of the leads 38'*. The package body 56 can be composed of any number of suitable molding compounds or encapsulants commercially available. As shown, *package body 56 has a plurality of apertures 58 in the bottom half of the body*. These apertures 56 [sic] are formed during the molding of the package body 56 through the use of ejector pins or something substantially similar. The diameter of these apertures should be approximately in a range of 5 to 15 mils (0.1 to 0.4 mm). *The apertures allow external accessibility to the ground plane 52 which is otherwise encapsulated within the package body 56*." Lin '556 (Ex. 1004) at 4:45-58 (emphasis added).

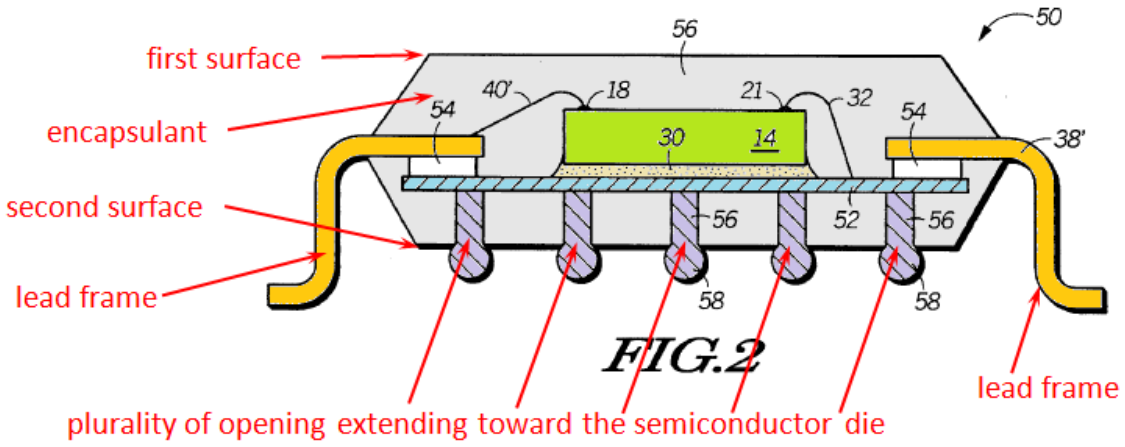


FIG.2

Lin '556 (Ex. 1004) at Fig. 2 (annotated).

(5.d) wherein the plurality of openings individually expose a portion of the thermally conductive material and the thermally conductive material is generally solderable.

"The *apertures allow external accessibility to the ground plane 52 which is otherwise encapsulated within the package body 56*." Lin '556 (Ex. 1004) at 4:56-58 (emphasis added).

"The bumps are made from a *solder paste which fills the apertures 56 to provide a direct electrical path*." Lin '556 (Ex. 1004) at 4:60-62 (emphasis added).
See also, e.g., Lin '556 (Ex. 1004) at Fig. 2, above.

i. Lin '556 discloses the preamble

With reference to the claim chart above, Lin '556 discloses all of the elements and limitations of claim 5. First, to the extent that the preamble is a limitation of the claim, Lin '556 discloses a microelectronic package, as required by the preamble, because it describes a semiconductor die, a leadframe with leads, and the package body, which are aspects of a microelectronic package. Lin '556 (Ex. 1004) at Abstract. *See also* Ex. 1003 at ¶ 61.

ii. Lin '556 discloses limitation 5.a

With respect to limitation 5.a, as shown in the claim chart above, Lin '556 discloses a semiconductor die (*e.g.*, semiconductor die 14) having a first side (*e.g.*, the "top side" as shown in Fig. 2) and a second side opposite the first side (*e.g.*, the "bottom side" in Fig. 2), the semiconductor die further including a thermally conductive material (*e.g.*, ground plane 52) formed on the second side of the semiconductor die (disposed at the second side of the die because it is adhesively connected to the second side) in series (in sequence—first the die, then the adhesive, then the ground plane). *See* Ex. 1003 at ¶¶ 62-63.

One of ordinary skill in the art would understand that the disclosed ground plane is a thermally conductive material (a material capable of transferring heat) such as a metal, for at least three reasons:

First, Lin '556 discloses that the adhesive 30 between the die and ground plane 52 is "preferably thermally conductive." Ex. 1004 at 4:27-28. One of ordinary skill in the art would appreciate that if a thermally conductive adhesive is used to transfer heat away from the die, the next material "in series" or "in sequence" would also be capable of transferring heat so as to continue the heat transfer process. Ex. 1003 at ¶ 64 And consistent with this understanding, the ground plane is in contact with a solder paste (which, being metallic, is also thermally conductive), thus continuing the thermal path from the die to the exterior of the package. *See id*.

Second, as seen in the claim chart above, this chain of materials from the die to the outside of the package is described as electrically conductive: The adhesive 30 may be electrically conductive, but in any event there is a bond wire 32 connecting ground plane 52 to ground bonding pad 21. There is solder paste in the openings in contact with the ground plane. And the ground plane is attached to the leads with an electrically insulative tape 54 to prevent the ground plane from shorting the leads adhesive 54. A person of ordinary skill in the art would readily

understand that the ground plane is electrically conductive and thus metallic, and that metals are typically thermally conductive. *See* Ex. 1003 at ¶ 65.

Finally, Lin '556 discloses an alternative embodiment that varies only in the ground plane element—it is "composed a metallic mesh instead of a solid plane." Ex. 1004 at 5:8-14. The fact that the only difference in the embodiments is the form of the ground plane—a mesh versus a solid—confirms that the solid ground plane 52 would also be composed of a metal, which is capable of transferring heat. *See* Ex. 1003 at ¶ 66.

iii. Lin '556 discloses limitation 5.b

With respect to limitation 5.b, as shown in the claim chart above including annotated Fig. 2, Lin '556 discloses a lead frame proximate the semiconductor die, the lead frame having a lead finger (*e.g.,* leads 38') electrically coupled to the first side of the semiconductor die (*e.g.*, signal bonding pad 18 connected to lead 38' with wire bond 40'), which are all of the elements of limitation 5.b. *See* Ex. 1003 at ¶ 68.

iv. Lin '556 discloses limitation 5.c

With respect to limitation 5.c, as shown in the claim chart above including annotated Fig. 2, Lin '556 discloses an encapsulant (*e.g.*, plastic package body 56) at least partially encapsulating the semiconductor die and the lead frame, the encapsulant having a first surface (*e.g.*, the top surface in the figure) opposite a

second surface (*e.g.*, indicated bottom surface), and the encapsulant also including a plurality of openings (58) extending toward the semiconductor die from the second surface, which are all of the elements of limitation 5.c. Ex. 1003 at ¶ 69.

v. Lin '556 discloses limitation 5.d

With respect to limitation 5.d, as shown in the claim chart above, Lin '556 discloses that the plurality of openings individually expose a portion of the thermally conductive material (*e.g.*, "allow external accessibility to the ground plane 52"). Ex. 1003 at ¶ 70. As to the "generally solderable" limitation, one of ordinary skill in the art would understand that the thermally conductive material (*e.g.*, ground plane 52) was "generally solderable," since a solder paste is used to provide a direct electrical connection or "path" to it, and this solder would be reflowed by heating when "subsequently mounted to appropriate pads on a board." Ex. 1004 at 4:62-63. Ex. 1003 at ¶¶ 64-66, 70. Finally, Lin '556 discloses that the ground plane may be a metal mesh or plane (Ex. 1004 at 5:8-14) and metals are well-known to be "readily attachable with a solder." *See* Ex. 1003 at ¶¶ 50, 52, 70.

B. Ground 2: Claims 1-4 and 6-7 are obvious under 35 U.S.C. § 103(a) over Lin '556 and Bayan.

1. The combination of Lin '556 and Bayan discloses all of the elements of claim 1

i. It would have been obvious to one of ordinary skill in the art to combine Lin '556 and Bayan

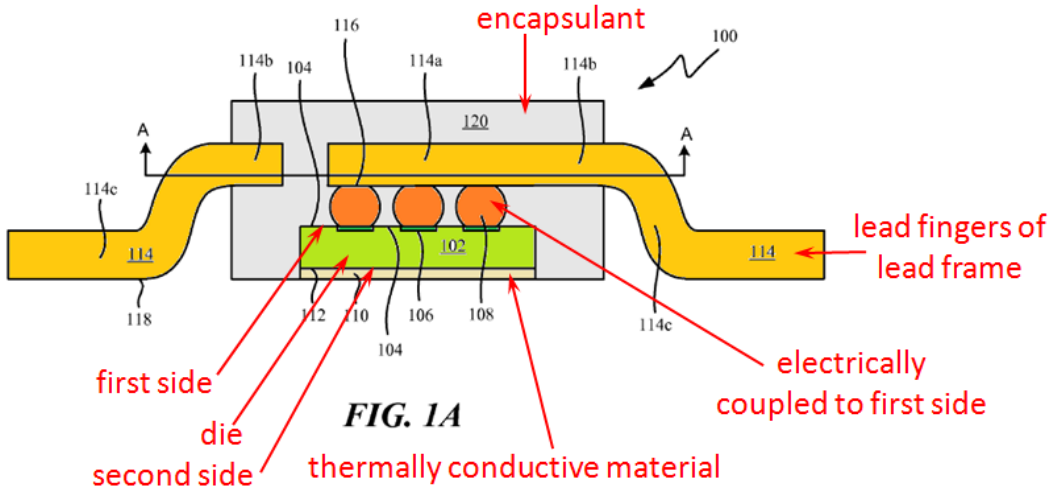
It would have been obvious to one of ordinary skill in the art to combine Lin '556 and Bayan. *First*, as Dr. Baker confirms, Lin '556 and Bayan are in the same field of endeavor, that is, semiconductor packaging. *See* Ex. 1003 at ¶ 74. And *second*, both Lin '556 and Bayan address the problem of thermal performance and managing the heat generated by a semiconductor during operation. Lin '556 teaches that "it has been revealed that embodiments of the invention improve electrical and *thermal performance* of a semiconductor device as compared to a standard QFP or CQFP."[4] Ex. 1004 at 5:31-34 (emphasis added). Lin '556 also teaches that its "invention … may also be applied to low lead count packages for increased electrical and *thermal performance*." *Id.* at 5:60-62 (emphasis added). In turn, Bayan similarly teaches: "[A]n exposed IC die package having increased *thermal performance* is described." Ex. 1005 at 1:6-7 (emphasis added). Bayan further teaches that connecting a thermally conductive layer to a printed circuit board (PCB) "provides an efficient and direct mechanism for *dissipating heat out*

[4] QFP and CQFP stand for "Quad Flat Package" and "Ceramic Quad Flat Package," which are standard semiconductor package types.

of the die. … [B]y soldering or otherwise connecting the metallic layer on the back surface of the die to the PCB, a *direct thermally conductive path* is created between the die and the PCB. In this way, the contact surface and PCB serves as a heat sink for *dissipating thermal energy out of the die*." Ex. 1005 at 6:15-22 (numerals omitted, emphasis added). *See* Ex. 1003 at ¶¶ 75-77.

With respect to specific limitations, claim 1 recites solder balls—which are disclosed by Bayan but not by Lin '556, and a plurality of openings—which are disclosed by Lin '556 but not by Bayan. Because Lin '556 and Bayan are in the same field of endeavor and both address thermal management, it would have been natural for one of ordinary skill to look to either of these references, and incorporate each of their teachings as appropriate into the other. As will be shown in more detail below, it would have been well within the capability of one of ordinary skill in the art to use Bayan's solder balls in Lin '556's package, or alternatively to use Lin '556's plurality of openings in Bayan's package.

Claim 1 as disclosed by Lin '556 and Bayan
1. A microelectronic package, comprising:
Lin '556 discloses the preamble: *See* preamble of claim 5 in chart for Ground 1, above.
Bayan discloses the preamble: "In one aspect, *an integrated circuit (IC) package* is described." Bayan (Ex. 1005) at 1:39-40 (emphasis added).
(1.a) a semiconductor die having a bond site at a first side and a second side opposite the first side, the semiconductor die further including a thermally

conductive material formed on the second side of the semiconductor die;
Lin ’556 discloses limitation 1.a: *See* limitation 5.a in chart for Ground 1, above. “The signal *bonding pad 18 of the semiconductor die 14 is connected to the lead 38′ with wire bond 40′*.” Lin ’556 (Ex. 1004) at 4:34-35 (emphasis added). *See also id.* at Fig. 2, reproduced in chart for Ground 1, above.
Bayan discloses limitation 1.a: “IC package 100 includes an IC die 102 having an *active surface 104 that includes a plurality of bond pads 106* … .” Bayan (Ex. 1005) at 3:32-34 (emphasis added). In various embodiments, the *IC die 102 includes a thin metallic layer 110 deposited onto the back surface 112* of the die as best illustrated in FIG. 1C, which illustrates the bottom surface of the package 100. *The thin metallic layer 110 may be formed from any suitable metal or metallic alloy. By way of example, the thin metallic layer 110 may be an alloy of titanium, nickel and silver. The thin metallic layer 110 may also be applied to the back surface 112 of the die 102 by any suitable means including, for example, sputtering. The metallic layer 110 may serve as a heat dissipation medium for transferring thermal energy out of the die 102.* In various embodiments, the back surface 112 of the die 102 is intended to be soldered directly to a desired substrate, such as a PCB, to provide for enhanced heat dissipation out of the die. Since solder does not generally adhere well to Si, the metallic layer serves as an intermediary between the solder and the Si. In other embodiments, such as in analog applications, it is desirable to electrically connect the back surface 112 of the die 102 to a PCB to allow control over the electrical potential of the back region of the die.” Bayan (Ex. 1005) at 3:44-63 (emphasis added).    *FIG. 1A*

Bayan (Ex. 1005) at Fig. 1A (annotated).

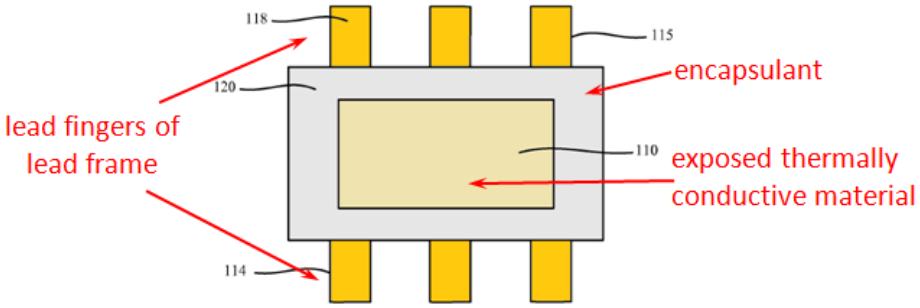


FIG. 1C

Bayan (Ex. 1005) at Fig. 1C (annotated).

(1.b) a lead frame proximate the semiconductor die, the lead frame having a lead finger;

Lin '556 discloses limitation 1.b.

See limitation 5.b in chart for Ground 1, above.

Bayan discloses limitation 1.b:

"Package 100 additionally includes a *lead frame having a plurality of leads* 114 and 115." Bayan (Ex. 1005) at 3:64-67 (emphasis added). *See also* Ex. 1005 at Fig. 1A (annotated), above.

(1.c) a solder ball between the bond site of the semiconductor die and the lead finger, the solder ball forming an electrical connection between the bond site of the semiconductor die and the lead finger of the lead frame;

Lin '556 discloses an electrical connection formed by a wire bond:

See limitation 5.b in chart for Ground 1, above.

Bayan discloses limitation 1.c:

"The inner lead portions 114*a* and 115*a* are arranged such that the solder pads 116 are positioned over corresponding bond pads 106 on the active surface 104 of the die 102. *Each bond pad 106 is physically and electrically connected to one of the associated leads 114 or 115 with a solder ball joint 108*." Bayan (Ex. 1005) at 4:35-40 (emphasis added).

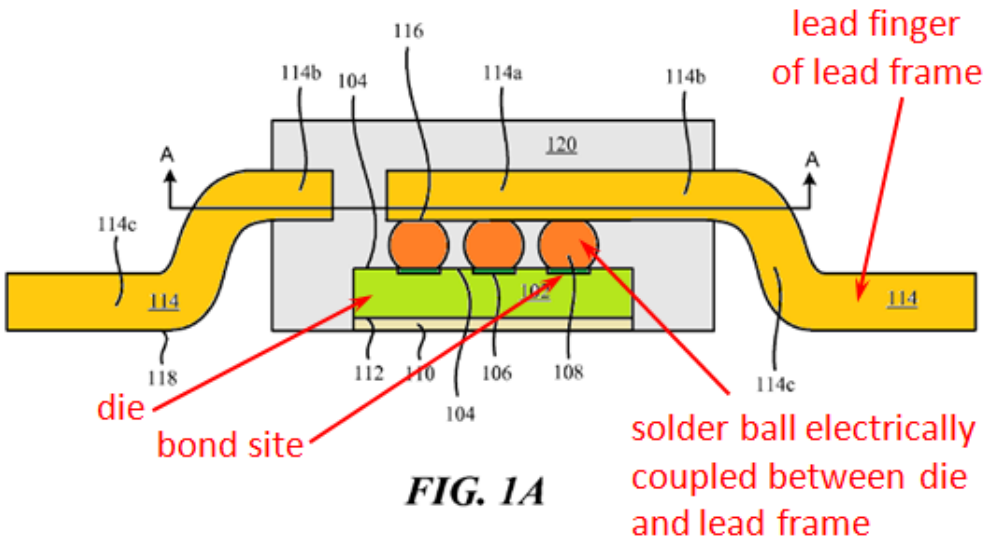


FIG. 1A

Bayan (Ex. 1005) at Fig. 1A (annotated).

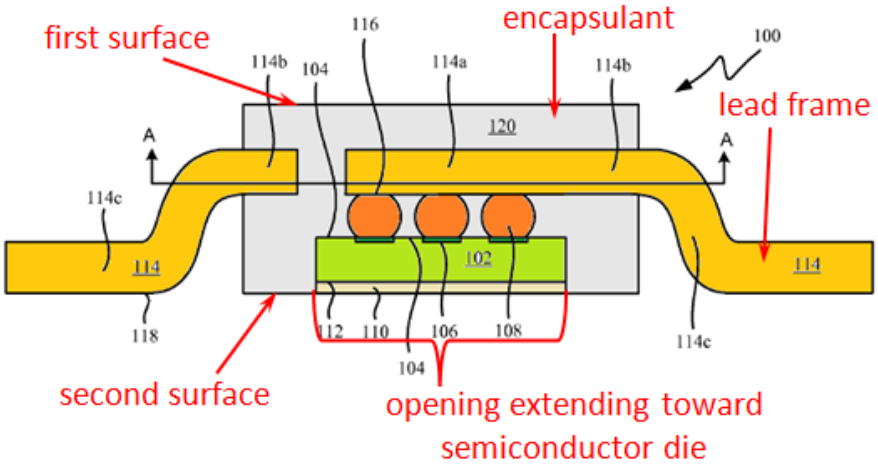
(1.d) an encapsulant at least partially encapsulating the semiconductor die, the lead frame, and the solder ball, the encapsulant having a first surface opposite a second surface, and the encapsulant also including a plurality of openings extending toward the semiconductor die from the second surface; and

Lin '556 discloses limitation 1.d, except for the solder ball:

See limitation 5.d in chart for Ground 1, above.

Bayan discloses limitation 1.d, with the encapsulant having an opening:

"In the embodiment illustrated in FIGS. 1A-1C, *portions of the die 102 and leads 114 and 115 are encapsulated with a molding material or compound 120*. The molding compound is generally a non-conductive plastic or resin having a low coefficient of thermal expansion. *Package 100 is encapsulated in such a way as to prevent molding material 120 from covering or intruding over the metallic layer 110 on the back surface 112 of the die 102. The molding material does encapsulate other portions of the die 102, the solder joints 108, and generally at least the inner portions 114a and 115a and middle portions 114b and 115b of the leads 114 and 115.*" Bayan (Ex. 1005) at 5:57-67 (emphasis added).



Bayan (Ex. 1005) at Fig. 1A (annotated).

(1.e) wherein the plurality of openings individually expose a portion of the thermally conductive material and the thermally conductive material is generally solderable.
Lin discloses limitation 1.e: *See* limitation 5.d in chart for Ground 1, above.
Bayan discloses this limitation with respect to its single opening: *"Package 100 is encapsulated in such a way as to prevent molding material 120 from covering or intruding over the metallic layer 110* on the back surface 112 of the die 102." Bayan (Ex. 1005) at 5:61-64. Bayan discloses that the thermally conductive material is generally solderable: *See* Bayan (Ex. 1005) at 3:54-59 (explaining that because the silicon (Si) back surface 112 of the die cannot be soldered to directly, the "*metallic layer serves as an intermediary between the solder and the Si.*") "More particularly, *by soldering or otherwise connecting the metallic layer 110 on the back surface 112 of the die 102* to the PCB 224, a direct thermally conductive path is created between the die 102 and the PCB 224." Bayan (Ex. 1005) at 6:16-20. *See also* Bayan (Ex. 1005) at Fig. 1C, reproduced in limitation 1.a, above.

ii. Both Lin '556 and Bayan disclose the preamble

The preamble of claim 1 is identical to the preamble of claim 5, and, to the extent that the preamble is a limitation, is disclosed by Lin '556. *See* section

V(A)(i) (*i.e.*, Ground 1–preamble), above. Bayan also discloses a microelectronic package, as required by the preamble, because it describes "an integrated circuit (IC) package," which is a type of microelectronic package. Ex. 1005 at 1:39-40; *see also* Ex. 1003 at ¶ 80.

iii. Both Lin '556 and Bayan disclose limitation 1.a

As shown in section V(A)(ii) (*i.e.*, Ground 1–limitation 5.a) Lin '556 discloses a semiconductor die (14) having a first side (the top side in Fig. 2) and a second side (the bottom side in Fig. 2), and a thermally conductive material (ground plane 52) formed on (*i.e.*, disposed at) the second side of the semiconductor die. Lin '556 further discloses a bond site (bonding pad 18), which, as can be seen in Fig. 2, is at the first side (*i.e.*, on the top side) of the die. *See* Lin '556 (Ex. 1004) at 4:34-35 ("The signal bonding pad 18 of the semiconductor die 14 is connected to the lead 38' with wire bond 40'."). Therefore, Lin '556 discloses limitation 1.a. *See* Ex. 1003 at ¶ 81.

Bayan also discloses this limitation. As shown in the chart above, Bayan discloses a semiconductor die (*e.g.,* IC die 102) having a bond site (*e.g.*, bond pad 106) at a first side (*e.g.,* active surface 104) and a second side (*e.g.,* back surface 112) opposite the first side, the semiconductor die further including a thermally conductive material (*e.g.,* thin metallic layer 110) formed on the second side of the semiconductor die in series. Thin metallic layer 110 is "thermally conductive"

(*i.e.*, capable of transferring heat) because it is metal and because it "may serve as a heat dissipation medium for transferring thermal energy out of the die." Ex. 1005 at 3:52-54. And because metallic layer 110 is "deposited onto the back surface 112 of the die," it is "disposed at the second side" of the die. *See* Ex. 1005 at 3:44-46. *See* Ex. 1003 at ¶¶ 82-83.

iv. Both Lin '556 and Bayan disclose limitation 1.b

As shown in the claim chart for claim 5, Lin '556 discloses a lead frame proximate the semiconductor die, the lead frame having a lead finger (*e.g.,* leads 38') electrically coupled to the first side of the semiconductor die (*e.g.*, signal bonding pad 18 connected to lead 38' with wire bond 40'). *See* section V(A)(iii) (*i.e.*, Ground 1–limitation 5.b) above.

Bayan also discloses this limitation. As shown in the chart above, including annotated Fig. 1A, Bayan discloses a lead frame proximate the semiconductor die (*e.g.*, IC die 102), the lead frame having a lead finger (*e.g.,* lead 114). *See* Ex. 1003 at ¶¶ 84-86.

v. Lin '556 and Bayan in combination disclose the elements of limitation 1.c

As shown in the chart above, Bayan discloses that "[e]ach bond pad 106 is physically and electrically connected to one of the associated leads 114 or 115 with a solder ball joint 108." Ex. 1005 at 4:35-40. Thus, Bayan discloses this limitation of a solder ball (*e.g.*, solder ball 108) between a bond site (*e.g.*, bond pad 106) of a

semiconductor die (*e.g.*, IC die 102) and the lead finger (*e.g.*, leads 114 and 115), the solder ball forming an electrical connection between the bond site of the semiconductor die and the lead finger of the lead frame. *See* Ex. 1003 at ¶ 88.

Lin '556 does not disclose a solder ball, instead disclosing a wire bond between the die and the lead finger. *See* section V(A)(iii) (*i.e.*, Ground 1– limitation 5.b), above. But it would have been obvious to one of ordinary skill in the art, in combining Lin '556 and Bayan, to replace the wire bonds in Lin '556 with solder balls as taught by Bayan.

As Dr. Baker explains, solder balls were well-known in the art long before Bayan used them. *See* Ex. 1003 at ¶¶ 27-28. Incorporating solder balls, as disclosed by Bayan into Lin '556's package would be a simple substitution of one well-known element (*i.e.*, a solder ball) for another (*i.e.*, a wire bond) to obtain predictable results. *See KSR*, 550 U.S. 398 at 415-21; MPEP §§ 2141, 2143; *see also* Ex. 1003 at ¶ 89. Further, Bayan teaches that solder balls improve heat dissipation and thermal performance:

> Those familiar with the art will appreciate that the current carrying and heat dissipation capabilities of *solder ball joints* far exceed those of *bonding wires*. Generally, as the number and diameter of the solder ball joints increase, the current carrying and heat dissipation capabilities of the die increase. Additionally, as the diameters of the solder ball joints increase, the resistance through the solder ball joints decreases. As a result of their larger diameters

> and the relatively shorter distance traveled through a solder ball joint as compared to a typical bonding wire, the electrical resistance through solder ball joints is far below that of typical bonding wires. By way of example, a typical solder ball joint may have a resistance of approximately 0.5 mΩ while a corresponding bonding wire used in a similar application may have a resistance in the range of approximately 60 to 100 mΩ.

Ex.. 1005 at 5:42-56 (emphasis added, numerals omitted). As such, incorporating solder balls would not only yield predictable results and improve the heat dissipation (and electrical performance) of the package, but would also do so in a predictable way. *See KSR*, 550 U.S. at 401; MPEP § 2143(I)(C); *see also* Ex. 1003 at ¶ 90.

vi. Lin '556 and Bayan in combination disclose the elements of limitation 1.d

As shown in the claim chart for claim 5, Lin '556 discloses an encapsulant at least partially encapsulating the semiconductor die and the lead frame, the encapsulant having a first surface opposite a second surface, and the encapsulant also including a plurality of openings extending toward the semiconductor die from the second surface. *See* section V(A)(iv) (*i.e.*, Ground 1–limitation 5.c) above. If using Bayan's solder balls in Lin '556's package (which as shown above would have been obvious to do), the solder balls would also be encapsulated, as Lin

’556’s encapsulant covers the space between the die and the lead frame—where the solder balls are located. *See* Ex. 1003 at ¶¶ 91-92.

As shown in the chart above, including annotated Fig. 1A, Bayan also discloses an encapsulant (*e.g.*, molding compound 120) at least partially encapsulating the semiconductor die (*e.g.*, IC die 102), the lead frame (leads 114), and the solder ball (108), the encapsulant having a first surface opposite a second surface and the encapsulant including an opening extending toward the semiconductor die from the second surface. *See* Ex. 1003 at ¶ 93.

It would have been obvious to one of ordinary skill in the art to combine Lin ’556 with Bayan, incorporating Lin ’556’s plurality of openings into Bayan’s package, for at least the following reasons:

First, Lin ’556 teaches the advantages of a plurality of openings. For example, multiple small solder connections do not “interfere with the seating plane of the device during board mount” (Ex. 1004 at 4:66-5:1) and “embodiments of the invention improve electrical and thermal performance of a semiconductor device as compared to a standard QFP or CQFP.” Ex. 1004 at 5:32-34. Incorporating a plurality of openings into Bayan’s package would be well within the capability of an ordinarily skilled artisan, and would be nothing more than using known techniques to improve a similar device in the same way. *KSR*, 398 U.S. at 401; MPEP § 2143(I)(C); *see also* Ex. 1003 at ¶¶ 94-95.

Second, Lin '556 discloses that the plurality of openings are "formed during the molding of the package body through the use of ejector pins or something substantially similar." Ex. 1004 at 4:52-54 (numerals omitted). Incorporating a plurality of openings in a package as taught by Bayan would be combining prior art elements according to known methods to produce predictable results. *KSR,* 398 U.S. at 401; *see also* Ex. 1003 at ¶ 96.

vii. Lin '556 and Bayan in combination disclose the elements of limitation 1.e

Limitation 1.e is identical to limitation 5.d, and as shown in section V(A)(v) (*i.e.,*, Ground 1, limitation 5d), above, Lin '556 discloses this limitation. And, incorporating Bayan's solder balls into Lin 556's package, which as shown earlier would have been obvious to do, would not alter this aspect of Lin '556's package. *See* Ex. 1003 at ¶ 99.

As shown in the chart above, Bayan also discloses an opening in the encapsulant that exposes a portion of the thermally conductive material, because the package is encapsulated so as to prevent the molding material from covering the metallic layer. And while one of ordinary skill would readily appreciate that a *metallic* layer is solderable, Bayan nevertheless expressly discloses that it is solderable. Incorporating Lin 556's plurality of openings into Bayan's package, which as discussed above would have been obvious to do, would result in the

plurality of openings exposing Bayan's solderable, thermally conductive material, thus achieving limitation 5.e. *See* Ex. 1003 at ¶¶ 97-100.

2. Lin '556 and Bayan in combination disclose the limitations of dependent claim 2.

Claim 2 as disclosed by Lin '556 and Bayan
The microelectronic package of claim 1 wherein:
(2.a) the semiconductor die further includes a barrier material, wherein the barrier material and the thermally conductive material are formed on the second side of the semiconductor die in series;
"*The semiconductor die 14 is mounted onto a ground plane 52* which is nonplanar with the leads 38'. … *The adhesive 30 used to attach the die to the ground plane can be either electrically conductive or insulative, although in either case it is preferably thermally conductive*." Lin '556 (Ex. 1004) at 4:22-28 (emphasis added). *See also* Lin '556 (Ex. 1004) at Fig. 2, as annotated in the claim chart for Ground 1 (limitation 5.a)
(2.b) the lead finger includes a first portion in contact with the solder ball and a second portion extending beyond the encapsulant.
"Each bond pad 106 is physically and electrically connected to one of the associated leads 114 or 115 with a solder ball joint 108." Bayan (Ex. 1005) at 4:38-40. "In the embodiment illustrated in FIGS. 1A-1C, portions of the die 102 and leads 114 and 115 are encapsulated with a molding material or compound 120. … In the embodiment illustrated in FIGS. 1A-1C, the outer portions of the leads 114 and 115 extend from the sides of the encapsulated package … ." Bayan (Ex. 1005) at 5:57-6:3.

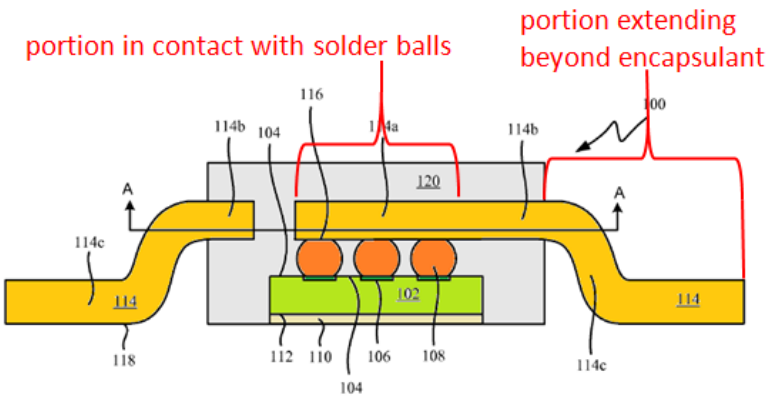


FIG. 1A

Ex. 1006 at Fig. 1A (annotated).

"The signal bonding pad 18 on the die surface 16 is electrically connected to the signal lead 38 with a third wire bond 40. … These leads extend outside the package body to provide peripheral leads for the device." Lin '556 (Ex. 1004) at 3:60-4:1.

i. Lin '556 discloses limitation 2.a

As shown in the chart above, Lin '556 discloses that the semiconductor die (14) further includes a barrier material (*e.g.*, adhesive 30), wherein the barrier material and the thermally conductive material (*e.g.*, ground plane 52) are formed on the second side of the semiconductor die in series (*e.g.*, in sequence—first the die, then the adhesive, then the ground plane). The broadest reasonable interpretation of barrier material is "a material disposed between the die and the thermally conductive layer," and Lin '556's adhesive is a material so disposed. *See* Ex. 1003 at ¶¶ 53-56, 102-103.

ii. The combination of Lin '556 and Bayan discloses limitation 2.b

As shown in the claim chart above, Bayan discloses that the lead finger (*e.g.*, lead 114) includes a portion in contact with the solder ball (*e.g.*, solder ball joint 108) and a second portion extending beyond the encapsulant (*e.g.,* molding material or compound 120). And as also shown in the chart, Lin '556 also discloses that the lead finger (*e.g.*, one of leads 38) has a first portion bonded to the die with a wire bond, and a second portion extending beyond the encapsulant. Further, incorporating the barrier layer as taught by Lange would not affect the contact between the lead finger and the solder ball or the lead finger's protrusion from the encapsulant. *See* Ex. 1003 at ¶¶ 104-106.

3. Lin '556 discloses the limitations of dependent claim 3.

Claim 3 of the '758 patent reads as follows:

The microelectronic package of claim 1 wherein:
the thermally conductive material is recessed in the openings at the second surface of the encapsulant.

As discussed above, the combination of Lin '556 and Bayan discloses the microelectronic package of claim 1. Further, as shown in Fig. 2 of Lin '556, the thermally conductive material (*e.g.*, ground plane 52) is recessed in the openings in the second surface of the molding material because the illustrated ground plane 52 sits spatially above the bottom surface of the encapsulant:

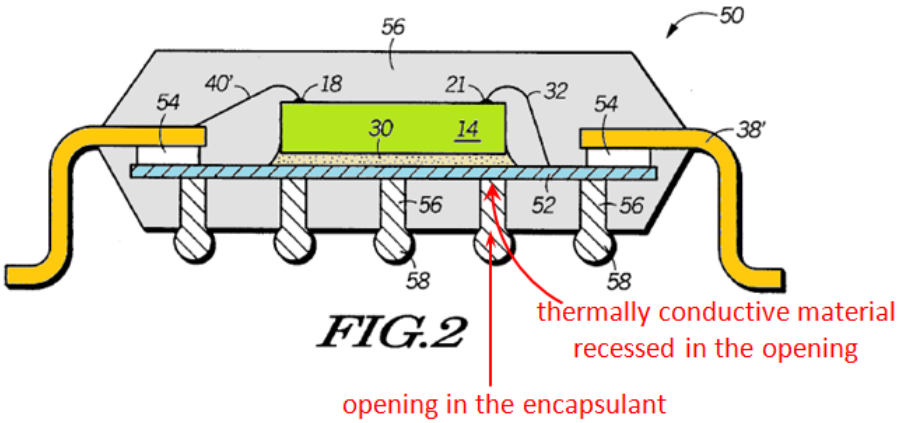


FIG.2

See also claim chart and discussion of limitations 5.d and 5.e in section V(A) (*i.e.*, Ground 1), above. And one of ordinary skill in the art would have no need to alter Lin 556's openings when incorporating the solder balls disclosed by Bayan, in order to achieve the invention of claim 1. *See* Ex. 1003 at ¶¶ 107-110.

4. Lin '556 discloses the limitations of dependent claim 4.

Claim 4 of the '758 patent reads as follows:

The microelectronic package of claim 1 wherein:
the microelectronic package further includes a solder paste in the openings, the solder paste being in contact with the thermally conductive material.

As discussed above, the combination of Lin '556 and Bayan discloses the microelectronic package of claim 1. Lin '556 further discloses a solder paste in the openings, the solder paste being in contact with the thermally conductive material. Ex. 1004 at 4:60-62 ("The bumps are made from a solder paste which fills the apertures 56 to provide a direct electrical path."). *See also* Ex. 1004 at Fig. 2, reproduced above in the claim chart for Ground 1. The solder paste is necessarily

in contact with the thermally conductive material (*e.g.*, ground plane 52) since it provides a "direct electrical path." *See* Ex. 1003 at ¶¶ 111-114.

5. Lin '556 in combination with Bayan discloses the limitations of dependent claim 6.

Claim 6 of the '758 patent reads as follows (claim indices added):

The microelectronic package of claim 5 wherein:
(6.a) the thermally conductive material includes a titanium/nickel/silver (Ti/Ni/Ag) tri-metal alloy formed on the second side of the semiconductor die;
(6.b) the openings individually expose a portion of the titanium/nickel/silver (Ti/Ni/Ag) tri-metal alloy at the second side of the semiconductor die.

As shown above in section V(A) (*i.e.*, Ground 1), Lin '556 discloses the microelectronic package of claim 5. And as shown above with respect to claim 1, it would have been obvious for one of ordinary skill in the art to combine Lin '556 with Bayan. *See* section V(B)(1)(i), above.

With respect to limitation 6.a, Bayan discloses that the thermally conductive material formed on the second side of the die includes a titanium/nickel/silver (Ti/Ni/Ag) tri-metal alloy:

> In various embodiments, the IC die 102 includes a thin metallic layer 110 deposited onto the back surface 112 of the die as best illustrated in FIG. 1C, which illustrates the bottom surface of the package 100. The thin metallic layer 110 may be formed from any suitable metal or metallic alloy. By way of example, *the thin metallic layer 110 may be an alloy of titanium, nickel and silver*. … . The metallic layer 110

> may serve as a heat dissipation medium for transferring thermal energy out of the die 102.

Ex. 1005 at 3:44-54 (emphasis added). As Dr. Baker explains, use of various metal alloys in semiconductor packaging, including tri-metal alloys of titanium, nickel, and silver, was well-known in the art. Ex. 1003 at ¶ 30. Just as incorporating Bayan's solder balls into Lin's package would be obvious to one of skill in the art (for claim 1 and its associated dependent claims), incorporating Bayan's teaching of a titanium, nickel, and silver alloy into Lin's package would be a combination of known prior art elements that would be both technically simple and would yield predictable results, including improved adhesion, heat transfer, solderability, and electrical conductivity, and thus would be obvious to one of ordinary skill in the art. *See* Ex. 1003 at ¶ 118; *see also KSR*, 550 U.S. at 401.

With respect to limitation 6.b, Lin discloses openings which individually expose a portion of the thermally conductive material, and Bayan also has an opening exposing the thermally conductive material. *See* discussion of limitation 5.d in Ground 1, above, and discussion of limitation 1.e, above. Thus, if the thermally conductive material is a Ti/Ni/Ag tri-metal alloy, as taught by Bayan, the openings would necessarily expose a portion of that Ti/Ni/Ag tri-metal alloy. *See* Ex. 1003 at ¶ 120.

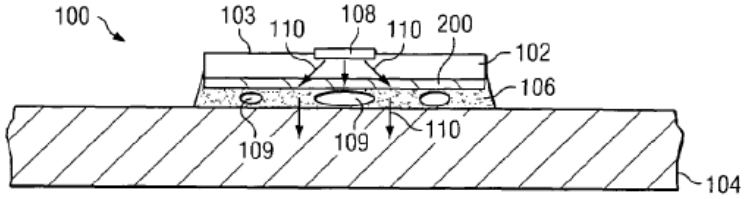
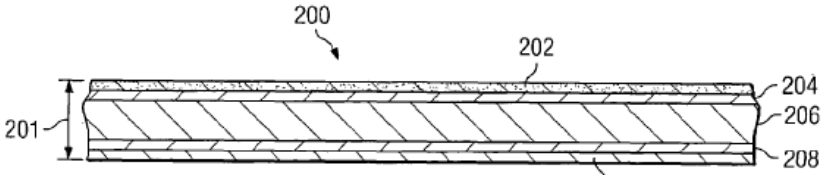
6. Lin ’556 in combination with Bayan discloses the limitations of dependent claim 7.

Claim 7 of the ’758 patent reads as follows (claim indices added):

The microelectronic package of claim 5 wherein:
(7.a) the thermally conductive material includes a titanium/nickel/silver (Ti/Ni/Ag) tri-metal alloy formed on the second side of the semiconductor die;
(7.b) the openings individually expose a portion of the titanium/nickel/silver (Ti/Ni/Ag) tri-metal alloy at the second side of the semiconductor die; and
(7.c) the microelectronic package further includes a solder paste in the plurality of openings, the solder paste being in contact with the titanium/nickel/silver (Ti/Ni/Ag) tri-metal alloy.

As shown above in Ground 1, Lin ’556 discloses the microelectronic package of claim 5. Limitations 7.a-b are identical to limitations 6.a-b, and as shown above in regard to claim 6, the combination of Lin ’556 and Bayan discloses those limitations. As to limitation 7.c , as shown above in section V(B)(4) (*i.e.*, Ground 2–claim 4), Lin ’556 discloses a solder paste in the openings in contact with the thermally conductive material. Since the thermally conductive material is a Ti/Ni/Ag tri-metal alloy (as disclosed by Bayan), the solder paste in the openings (as disclosed by Lin ’556) would necessarily be in contact with that Ti/Ni/Ag tri-metal alloy. *See* Ex. 1003 at ¶¶ 121-125.

C. Ground 3: Claim 2 is obvious under 35 U.S.C. § 103(a) over Lin '556 and Bayan in view of Lange.

Claim 2 as disclosed by Lin, Bayan and Lange
The microelectronic package of claim 1 wherein:
(2.a) the semiconductor die further includes a barrier material, wherein the barrier material and the thermally conductive material are formed on the second side of the semiconductor die in series;
"FIG. 1 is a cross-sectional view of a die attach system 100 according to one embodiment of the invention. In the illustrated embodiment, system 100 includes a *semiconductor chip 102* having a *heat conductive backside metal layer 200*." Lange (Ex. 1006) at 2:1-5 (emphasis added). "Referring to FIG. 2 … *heat conductive backside metal layer 200* includes an adhesive metal layer 202, *a barrier metal layer 204,* a metal layer 206, a barrier metal layer 208, and a solderable metal layer 210." Lange (Ex. 1006) at 2:35-44 (emphasis added).    *FIG. 1*    *FIG. 2* Lange (Ex. 1006) at Figs. 1-2.
(2.b) the lead finger includes a first portion in contact with the solder ball and a second portion extending beyond the encapsulant.
See chart for limitation 2.b in section V(B)(2) (*i.e.*, Ground 2, claim 2, above).

As shown above in section V(B)(1) (*i.e.*, Ground 2, claim 1), it would have been obvious to one of ordinary skill in the art to combine Lin '556 and Bayan to arrive at the microelectronic package of claim 1. To the extent that, as argued in

section V(B)(2) (*i.e.*, Ground 2–claim 2) above, Lin '556's adhesive layer is found not to be a barrier material and the combination of Lin '556 and Bayan does not disclose limitation 2.a, Lange discloses this limitation. As shown in the claim chart above, Lange discloses limitation 2.a: semiconductor die (chip 102) includes a barrier material (barrier metal layer 204 attached by means of adhesive metal layer 202), wherein the barrier material and the thermally conductive material (metal layer 206) are formed on the second side of the die in series (*e.g.*, in sequence). The broadest reasonable interpretation of barrier material is "a material disposed between the die and the thermally conductive layer," and Lange's layers 202 and 204 are a material so disposed. *See* Ex. 1003 at ¶¶ 130-132.

It would have been obvious to one of ordinary skill in the art to combine Lange with Lin '556 and Bayan, to include a barrier material formed between the die and the thermally conductive material, for at least the following reasons:

1) As Dr. Baker explains, Lin '556, Bayan, and Lange are all in the field of semiconductor packaging. *See* Ex. 1003 at ¶ 127.

2) As discussed above in section V(B)(1) (*i.e.*, Ground 2, claim 1), Lin '556 and Bayan address problems of heat dissipation out of the die. Lange is directed at the same problem. "[A] heat conductive backside metal layer facilitates improved heat dissipation from a chip surface to a heatsink. In addition, such a heat conductive backside metal layer may be soldered directly on a board or

electrical substrate … .” Ex. 1006 at 1:34-38. As such, one of ordinary skill in the art would know to incorporate Lange’s teachings and disclosures in addressing a similar problem. *See* Ex. 1003 at ¶ 128.

3) Barrier layers were well known in the art, and incorporating a barrier layer, as disclosed by Lange, would be using known techniques to improve a similar device in a similar way. *See KSR*, 550 U.S. at 415-21; MPEP §§ 2141, 2143; *see also* Ex. 1003 at ¶ 29. Further, consistent with the knowledge in the art, Lange teaches that the barrier “acts as a diffusion barrier for metal layer 206.” Ex. 1006 at 2:64-65. As such, incorporating a barrier layer would not only yield predictable results, but improve the package in a predictable way. *See KSR*, 550 U.S. at 421; MPEP § 2143(I)(C); *see also* Ex. 1003 at ¶ 129.

As to limitation 2.b, the combination of Lin ’556 and Bayan disclose it, as shown in section V(B)(2) (*i.e.*, Ground 2–claim 2) above. *See also* Ex. 1003 at ¶¶ 133-134.

D. Ground 4: Claim 5 is anticipated under 35 U.S.C. § 102(e) by Lin ’270.

Claim 5 as disclosed by Lin ’270
5. A microelectronic package, comprising:
“An integrated circuit package …” Lin ’270 (Ex. 1007) at Abstract.
(5.a) a semiconductor die having a first side and a second side opposite the first side, the semiconductor die further including a thermally conductive material formed on the second side of the semiconductor die in series;
“The resulting leadframe strip 32 includes a plurality of units, one of which is

shown in the Figures. Each unit includes the generally centrally located die attach pad 22. The die attach pad 22 includes a continuous portion 34 on one side of the die attach pad 22 and the plurality of pad portions 36 that extend from the continuous portion 34, to the opposite side of the die attach pad 22." Lin '270 (Ex. 1007) at 4:11-18.

"A singulated s*emiconductor die 26 is then mounted to the continuous portion 34 of the die attach pad 22* using, for example, epoxy (FIG. 1F)." Lin '270 (Ex. 1007) at 4:39-41 (emphasis added).

"*[T]hermal performance of the IC package is improved by providing a direct thermal path from the exposed die attach pad to the motherboard*." Lin '270 (Ex. 1007) at 1:51-53 (emphasis added).

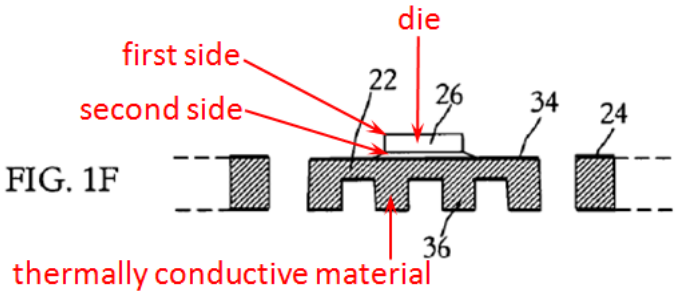


FIG. 1F

Lin '270 (Ex. 1007) at Fig. 1F (annotated).

(5.b) a lead frame proximate the semiconductor die, the lead frame having a lead finger electrically coupled to the first side of the semiconductor die;

"Each unit also includes the *plurality of contact pads 24 that circumscribe the die attach pad 22*." Lin '270 (Ex. 1007) at 4:18-19 (emphasis added).

"Gold *wire bonds 28 are then bonded between bond pads of the semiconductor die 26 and the contact pads 24* (FIG. 1G)." Lin '270 (Ex. 1007) at 4:41-43 (emphasis added).

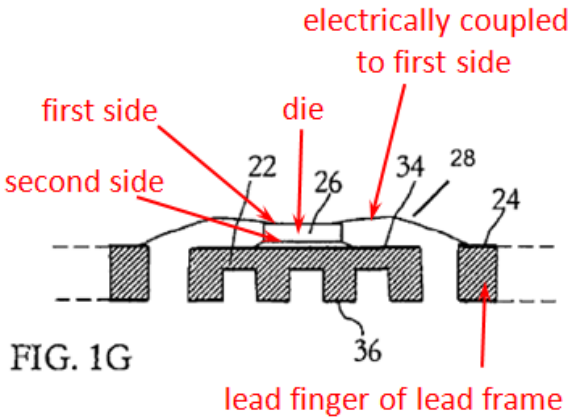


FIG. 1G

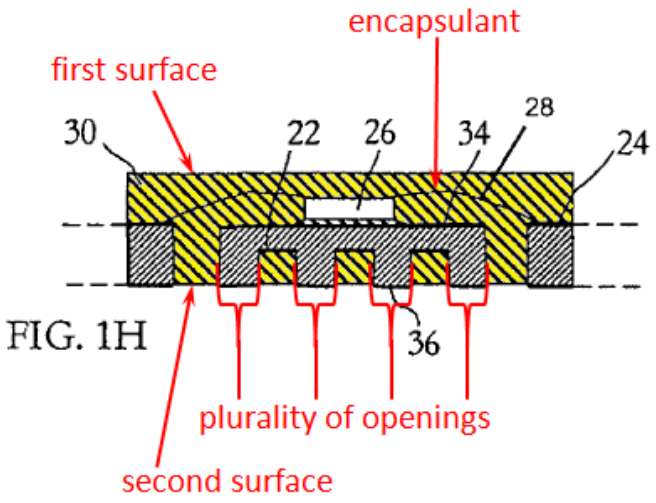
Lin '270 (Ex. 1007) at Fig. 1G (annotated).

See also Lin '270 (Ex. 1007) at Fig. 2B, reproduced in 5.c below.

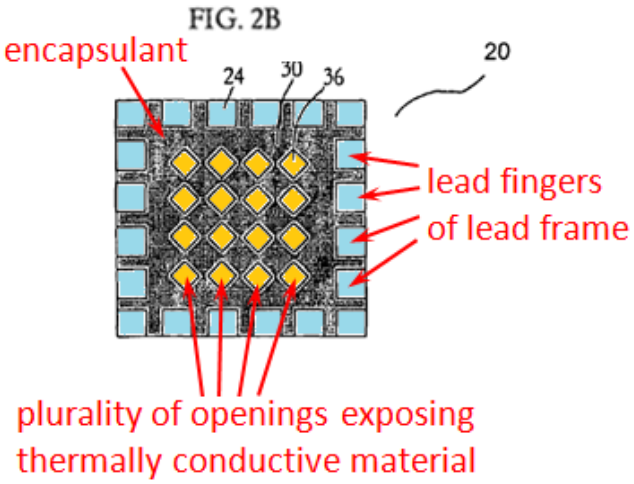
(5.c) an encapsulant at least partially encapsulating the semiconductor die and the lead frame, the encapsulant having a first surface opposite a second surface, and the encapsulant also including a plurality of openings extending toward the semiconductor die from the second surface; and

"The leadframe strip 32 is then molded using a suitable mold …. As indicated above, the pad portions 36 are oriented with corners of the pad portions 36 pointing in the direction of the molding material flow during molding to aid in the flow of molding material 30 around the pad portions 36 under the continuous portion 34 of the die attach pad 22. Clearly, the sides of the pad portions 36 are oriented at an oblique angle with the sides of the molding material 30 after molding.

The molding material 30 encapsulates the semiconductor die 26, the wire bonds 28, and all except one surface of the leadframe strip 32. In the orientation shown in FIG. 1H, a bottom surface of each of the contact pads 24 and a bottom surface of each of the pad portions 36 of the die attach pad 22 is exposed. FIG. 2B shows a bottom view of the integrated circuit package of FIG. 1H and best shows the exposed surfaces of the contact pads 24 and the pad portions 36." Lin '270 (Ex. 1007) at 4:44-62 (emphasis added).



Lin '270 (Ex. 1007) at Fig. 1H (annotated).

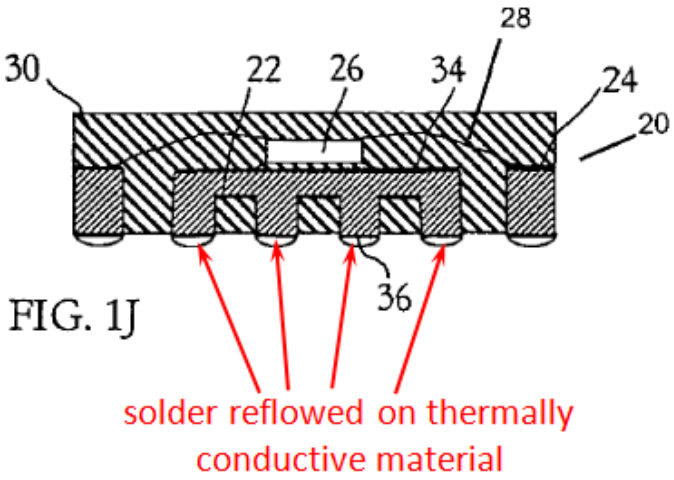


Lin '270 (Ex. 1007) at Fig. 2B (annotated).

(5.d) wherein the plurality of openings individually expose a portion of the thermally conductive material and the thermally conductive material is generally solderable.

See Ex. 1007 at 4:44-62 and Figs. 1H and 2B, above.

"Next, *solder paste is applied to the contact pads 24 and to the pad portions 36* by screen printing, as will be understood by those skilled in the art. After solder paste printing, *the solder is reflowed using known reflow technique*." Lin '270 (Ex. 1007) at 4:63-65 (emphasis added).



Lin '270 (Ex. 1007) at Fig 1J (annotated)

With reference to the claim chart above, Lin '270 discloses all of the elements and limitations of claim 5. As an initial matter, to the extent the preamble

of the claim is a limitation, Lin '270 describes the invention in the Abstract as "[a]n integrated circuit package" which is a type of microelectronic package, as called for in the '758 patent's preamble. *See* Ex. 1003 at ¶ 136.

With respect to limitation 5.a, as shown in the chart above including annotated Fig. 1F, Lin '270 discloses a semiconductor die (*e.g.*, semiconductor die 26) having a first side (*e.g.*, top side in the figure) and a second side opposite the first side (*e.g.*, bottom side in the figure), the semiconductor die further including a thermally conductive material (*e.g.*, die attach pad 22) formed on the second side of the semiconductor die in series. The die attach pad is a "thermally conductive material" because, as Lin '270 explains, "thermal performance of the IC package is improved by providing a *direct thermal path from the exposed die attach pad* to the motherboard" (Ex. 1007 at 1:51-53 (emphasis added)) which can only be achieved if the die attach pad is thermally conductive. Ex. 1003 at ¶ 137. Further, Lin '270 describes how the die attach pad 22 is formed from leadframe strip 32 which is copper. *See* Ex. 1007 at 4:10-20 (forming die attach pad) and 3:49-51 ("a copper (Cu) panel substrate … forms the raw material of the leadframe strip 32"). Copper is well-known to be a thermally conductive material. Ex. 1003 at ¶ 137; Ex. 1016 at 213 (showing copper having a thermal conductivity of 381, the highest listed). And the die is "formed on," that is, "disposed at" the second side of the

die. *See, e.g.*, '758 patent (Ex. 1001) at 5:30-45 (describing how the thermally conductive material may be "preformed" and adhesively attached).

With respect to limitation 5.b, as shown in the chart above, Lin '270 discloses a lead frame proximate the semiconductor die, the lead frame having a lead finger (*e.g.*, contact pad 24) electrically coupled (*e.g.*, via gold wire bonds 28) to the first side of the semiconductor die. *See* Ex. 1007 at 4:18-19 and 4:41-43; *see also* Ex. 1003 at ¶ 138.

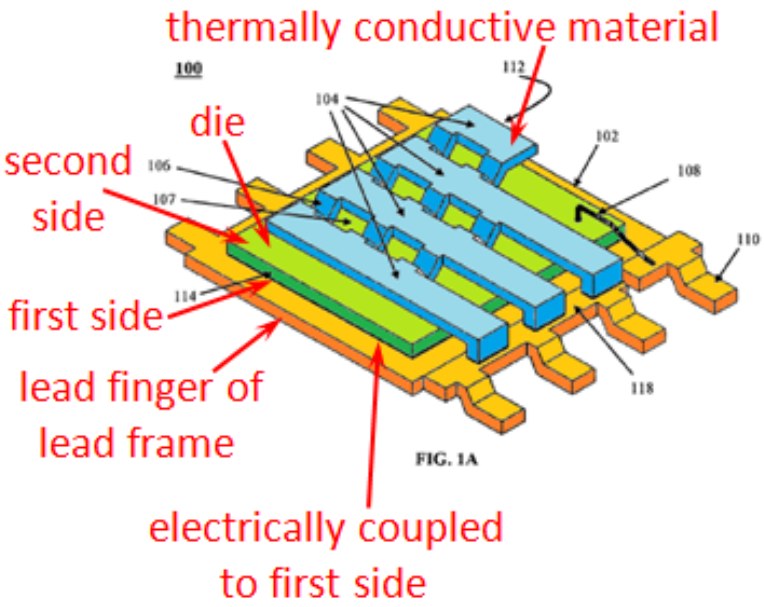
With respect to limitation 5.c, as shown in the chart above, Lin '270 discloses an encapsulant (*e.g.*, molding material 30) at least partially encapsulating the semiconductor die and the lead frame, the encapsulant having a first surface opposite a second surface, and the encapsulant also including a plurality of openings extending toward the semiconductor die from the second surface. The encapsulant necessarily has a plurality of openings because the plurality of pad portions 36 is exposed at the bottom (second) surface of the encapsulant, and the openings extend towards the die. *See* Ex. 1003 at ¶ 139.

With respect to limitation 5.d, as shown in the chart above, Lin '270 discloses that the plurality of openings individually expose a portion of the thermally conductive material. As shown in Figs. 1H and 2B, multiple openings each expose a pad portion (numbered "36"), which is part of the thermally conductive material (die attach pad 22). And the thermally conductive material—

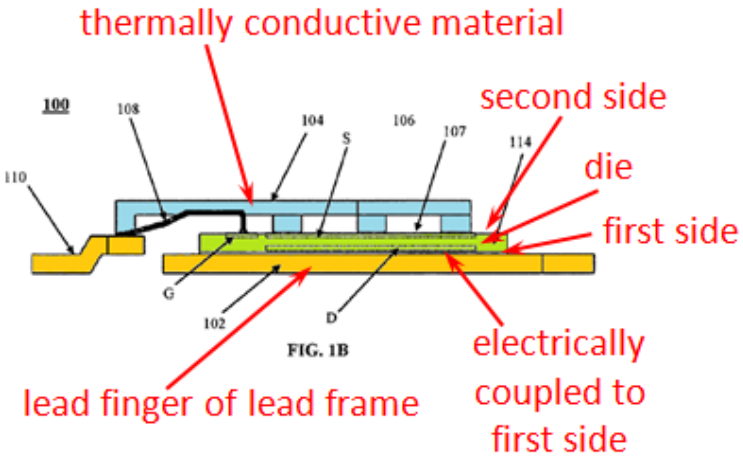
pad portions 36—is necessarily solderable since a solder paste can be applied to it and then reflowed. *See* Ex. 1003 at ¶ 140.

E. Ground 5: Claim 5 is anticipated under 35 U.S.C. § 102(b) by Shi.

Claim 5 as disclosed by Shi
5. A microelectronic package, comprising:
"This invention generally relates to *semiconductor die packages* and more particularly to the use of a source clip in a die package to provide electrical contact in a way that lowers spreading resistance and enhances heat dissipation." Shi (Ex. 1008) at 1:6-9 (emphasis added).
(5.a) a semiconductor die having a first side and a second side opposite the first side, the semiconductor die further including a thermally conductive material formed on the second side of the semiconductor die in series;
"According to an embodiment of the present invention, *the semiconductor device package 100 includes a clip 112, which includes separate parallel conductive fingers 104 that are electrically and mechanically connected to each other by conductive bridges 106 adapted to make electrical contact with a top source of the semiconductor device 114*." Shi (Ex. 1008) at 3:35-40 (emphasis added). "In a preferred embodiment, the *clip 112 is formed from a single piece of material, e.g., by stamping from a single sheet of metal*." Shi (Ex. 1008) at 3:58-60 (emphasis added). "The bridges are adapted to provide electrical connection to a top semiconductor region of a semiconductor device and *may also provide [a] heat dissipation path when a top surface of the fingers is exposed*." Shi (Ex. 1008) at abstract (emphasis added). "Optionally, a *heat sink may be attached to the exposed top surface of the fingers* 104." Shi (Ex. 1008) at 6:66-67 (emphasis added).



Shi (Ex. 1008) at Fig. 1A (annotated).

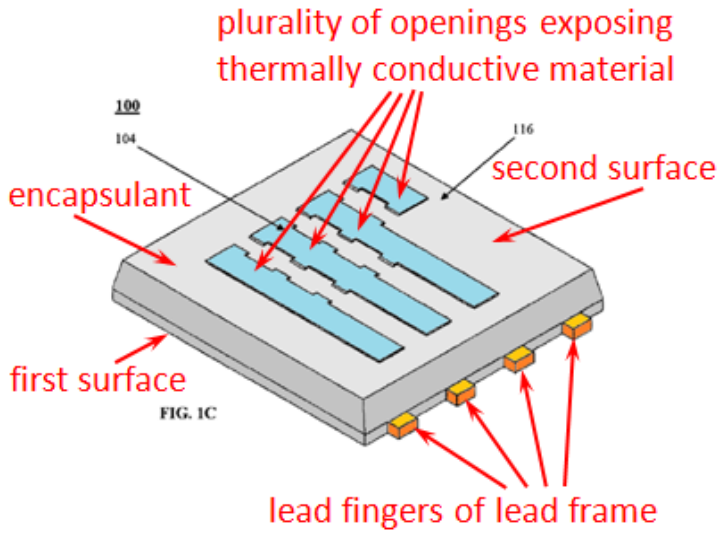


Shi (Ex. 1008) at Fig. 1B (annotated).

(5.b) a lead frame proximate the semiconductor die, the lead frame having a lead finger electrically coupled to the first side of the semiconductor die;

"According to one embodiment of the present invention, as depicted in FIGS. 1A-1B, a semiconductor device package 100 may have a V-shaped clip with a non-exposed gate wire bonded to a *lead frame*. As shown in FIG. 1A, the device *package 100 includes a fused lead frame 102* and a semiconductor device 114, e.g., a MOS device having a top source S, a top gate G and a *bottom drain D located on top of the lead frame 102 with the bottom drain D contacting the main portion of the lead frame 102*." Shi (Ex. 1008) at 3:18-26 (emphasis added).

See also, e.g., Shi (Ex. 1008) at Figs. 1A-B, above.

(5.c) an encapsulant at least partially encapsulating the semiconductor die and the lead frame, the encapsulant having a first surface opposite a second surface, and the encapsulant also including a plurality of openings extending toward the semiconductor die from the second surface; and
"As shown in FIG. 1C, the s*emiconductor device package 100 may be encapsulated with molding compound 116 and leave the tops of the fingers 104 exposed*." Shi (Ex. 1008) at 4:8-10 (emphasis added).    Shi (Ex. 1008) at Fig. 1C (annotated).
(5.d) wherein the plurality of openings individually expose a portion of the thermally conductive material and the thermally conductive material is generally solderable.
See Shi (Ex. 1008) at 4:8-10 and Fig. 1C, above. "In a preferred embodiment, the *clip 112 is formed from a single piece of material, e.g.*, by stamping from *a single sheet of metal*." Shi (Ex. 1008) at 3:58-60 (emphasis added). "[A] solder reflow can be performed to form the solder joints … between the semiconductor device 114 and clip 112" Shi (Ex. 1008) at 6:55-58.

With reference to the claim chart above, Shi discloses all of the elements and limitations of claim 5. As an initial matter, to the extent that the preamble of claim 5 is a limitation, Shi describes the invention as relating to "semiconductor die

packages" which are types of microelectronic packages, as recited in the '758 patent's preamble. *See* Ex. 1003 at ¶ 143.

With respect to limitation 5.a, as shown in the claim chart above, Shi discloses a semiconductor die (*e.g.*, semiconductor device 114) having a first side (*e.g.*, the "lower" surface in the figures) and a second side opposite the first side (*e.g.*, the upper surface in the figures), the semiconductor die further including a thermally conductive material (*e.g.*, clip 112) formed on the second side of the semiconductor die in series (in sequence—first the die, then the clip). The clip is thermally conductive first and foremost because it is made of metal (Ex. 1008 at 3:58-60), and also because Shi teaches that the bridges (part of the clips) provide a heat dissipation path (*i.e.*, a thermal path requiring conductivity) when exposed outside the package (*id.* at Abstract), such a heat sink may be attached to the exposed top surface of the clip's fingers (*id.* at 6:66-67), which confirms that the clip is thermally conductive. *See* Ex. 1003 at ¶ 144. Similarly, because it makes a physical connection to the second side of the die (upper surface in the figures), the clip is "disposed at the second side of the semiconductor die."

With respect to limitation 5.b, as shown in the chart above, Shi discloses a lead frame (*e.g.*, lead frame 102) proximate the semiconductor die, the lead frame having a lead finger electrically coupled to the first side of the semiconductor die.

Ex. 1008 at 3:18-26 ("bottom drain D contacting the main portion of the lead frame 102.") *See* Ex. 1003 at ¶ 145.

To summarize, Shi's illustrations of its semiconductor package (Figs. 1A and 1B), show the "first side" of the die 114 to be the bottom side, which rests on and is electrically connected to the lead frame 102, and the "second side" to be the top side, on which the fingers 104 of clip 102 are formed (*i.e.*, "disposed at" according to the broadest reasonable claim construction), disclosing limitation 5.a and 5.b.

With respect to limitation 5.c, as shown in the chart above, Lin discloses an encapsulant (*e.g.*, molding compound 116) at least partially encapsulating the semiconductor die and the lead frame, the encapsulant having a first surface opposite a second surface, and the encapsulant also including a plurality of openings extending toward the semiconductor die from the second surface. One of ordinary skill in the art would appreciate that in order to leave the surfaces of fingers 104 of clip 112 exposed, there must be openings in the encapsulant extending towards the semiconductor die. *See* Ex. 1003 at ¶ 146.

Finally, with respect to limitation 5.d, Shi discloses that the plurality of openings individually expose a portion of the thermally conductive material by disclosing that the tops of the fingers are exposed. And Shi discloses that the thermally conductive material is generally solderable–*first*, because the fingers are

preferably "stamped from a single sheet of metal" and metal is well-known to be "readily attachable with a solder during reflow" and *second*, because Shi discloses that "a solder reflow can be performed to form the solder joints … between the semiconductor device 114 and clip 112" (Ex. 1008 at 6:55-58), which confirms that the clip must be "readily attachable with a solder during reflow." *See* Ex. 1003 at ¶ 147.

VI. CONCLUSION

In light of the above, it is respectfully submitted that the claims 1-7 of the '758 patent are unpatentable under pre-AIA 35 U.S.C. §§ 102 and 103. Petitioner respectfully requests that an *inter partes* review be instituted and the subject claims cancelled.

Date: February 24, 2015

Respectfully submitted,

By /Andrew J. Gray IV/

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CERTIFICATE OF SERVI CE

The undersigned hereby certifies that a copy of the foregoing Petition for *inter partes* review of United States Patent No. 8,283,758 and all exhibits and other documents filed together with the petition were served on February 24, 2015 via FIRST CLASS MAIL on the attorney of record for the Patent Owner at the current correspondence address on file with the PTO:

Perkins Coie LLP – Monolithic Power Systems
P.O.Box 1247
Seattle, WA 98111-1247

A copy of the foregoing Petition, exhibits and all other documents filed together with the petition were also served on February 24, 2015 via FedEx to MPS's counsel in the Northern District of California proceedings:

John P. Schnurer, Esq.
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San Diego, CA 92130-2594

The foregoing Petition, exhibits and documents were also served by email to:

MPS-SilergyPerkinsService@perkinscoie.com

Date: February 24, 2015

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