IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Banks	
U.S. Patent No.:	5,764,571	Attorney Docket No.: 36144.0014IP1
Issue Date:	June 9, 1998	
Appl. Ser. No.:	08/410,200	
Filing Date:	February 27, 1995	
Title:	Electrically Alterable Non-Volatile Memory With N-Bits Per Cell	

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PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 5,764,571 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

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EXHIBITS

MICRON-1001	U.S. Patent No. 5,764,571 to Banks (“the ’571 patent”)
MICRON-1002	Excerpts from the Prosecution History of the ’571 patent (“Prosecution History”)
MICRON-1003	Declaration of R. Jacob Baker (“Expert Declaration”)
MICRON-1004	U.S. Patent No. 5,172,338 to Mehrotra et al. (“Mehrotra”)
MICRON-1005	U.S. Patent No. 4,952,821 to Kokubun (“Kokubun”)
MICRON-1006	U.S. Patent No. 5,319,348 to Lee et al. (“Lee”)
MICRON-1007	Excerpt of April 27, 2010, Tutorial Transcript, *MLC Flash Memory Devices and Products Containing Same*, Inv. No. 337-TA-683, (January 19, 2011) (Completed)
MICRON-1008	Excerpts from “An Introduction to Analog and Digital Communications,” by Simon S. Haykin (1989)
MICRON-1009	Excerpts from “MACMILLAN DICTIONARY OF MICRO-COMPUTING,” Third Edition (1985)
MICRON-1010	Certified Translation of Japanese Patent Application Kokai No. S62-34398 (A) (Ex. 1015) (“Kitamura”) (annotated with paragraph numbers)
MICRON-1011	MLC’s December 5, 2014, confidential infringement contentions from *MLC Intellectual Property, LLC v. Micron Technology, Inc.*, No. 3:14-cv-03657 (N.D. Cal. August 12, 2014)
MICRON-1012	Excerpts from “VLSI Design Techniques for Analog and Digital Circuits,” by Geiger, Allen, and Strader, McGraw-Hill, March 1989
MICRON-1013	Excerpts from “Fundamentals of Digital Systems Design,” by

	Rhyne, 1973
MICRON-1014	U.S. Patent No. 5,095,344 to Harari ("Harari")
MICRON-1015	Japanese Patent Application Kokai No. S62-34398 (A)

Micron Technology, Inc. (“Petitioner”) petitions for *Inter Partes* Review (“IPR”) under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42 of claims 1, 9, 10, 12, 30, 32, 42, and 45 (“the Challenged Claims”) of U.S. Patent No. 5,764,571 (“the ’571 patent”). As explained below, there exists a reasonable likelihood that Petitioner will prevail in demonstrating unpatentability of at least one of the Challenged Claims based on the teachings of the references presented in this petition.

I. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner, Micron Technology, Inc., is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any previous disclaimers, reexamination certificates or petitions for *inter partes* review for the ’571 patent. Petitioner is aware of the following civil actions involving the ’571 patent: *MLC Intellectual Property, LLC v. Micron Technology, Inc*., No. 3:14-cv-03657 (N.D. Cal. August 12, 2014); *BTG International Inc. v. Apple Inc. et al*, No. 2:09-cv-00223 (E.D. Tex. July 20, 2009); *BTG International Inc. v. Samsung Electronics Co. LTD et al*, No. 2:08-cv-00482 (E.D. Tex. December 29, 2008); and *MLC Flash Memory Devices and Products Containing Same*, Inv. No. 337-TA-683, (January 19, 2011) (Completed).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner designates Timothy W. Riffe, Reg. No. 43,881, as Lead Counsel and Adam R. Shartzer, Reg. No. 57,264, as Backup Counsel, both available at

3200 RBC Plaza, 60 South Sixth Street, Minneapolis, MN 55402 (T: 202-783-5070; F: 202-783-2331).

D. Service Information

Address all correspondence and service to counsel at the address provided in Section I(C). Petitioner consents to email service at IPR36144-0014IP1@fr.com.

II. PAYMENT OF FEES – 37 C.F.R. § 42.103

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 06-1050 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to same.

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that the '571 patent is available for IPR. Petitioner was served with a complaint alleging infringement of the '571 patent on August 19, 2014. Petitioner is not barred or estopped from requesting this review challenging the Challenged Claims on the identified grounds.

B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds set forth below, and requests the Challenged Claims be found unpatentable. An explanation of unpatentability under the statutory grounds identified below is provided in the

form of detailed description and claim charts that follow, indicating where each element is found in the cited prior art, and the relevance of that prior art. Additional explanation and support for each ground of rejection is set forth in Exhibit 1003, the Declaration of Dr. R. Jacob Baker, referenced throughout this Petition.

Ground	'571 Patent Claims	Basis for Rejection
Ground 1	1, 9, 10, 12, 30, 42, and 45	Obvious under § 103(a) over Kitamura
Ground 2	1, 9, 12, 30, 32, 42, and 45	Obvious under § 103(a) over Mehrotra

The '571 patent claims to be a divisional of U.S. Patent No. 5,394,362 filed on June 4, 1993, which, in turn, claims to be a continuation of U.S. Patent No. 5,218,569 filed on February 8, 1991. Thus, the earliest effective filing date for the claims of the '571 patent is February 8, 1991.

Kitamura, Japanese Unexamined Patent Application Publication No. S62-34398, qualifies as prior art under 35 U.S.C. § 102(b). Specifically, the publication date of Kitamura (Ex. 1010) is February 14, 1987. Kitamura was filed on August 8, 1985. Thus, both Kitamura's publication date and priority date predate by more than one year the earliest priority date of the '571 patent.

Mehrotra, U.S. Patent No. 5,172,338, qualifies as prior art under 35 U.S.C. § 102(e). Specifically, the filing date of Mehrotra (Ex. 1004) is April 11, 1990. Mehrotra claims priority to and is a continuation-in-part of U.S. Appl. Ser. No.

07/337,579 filed on April 13, 1989[1]. Thus, both Mehrotra's filing date and priority date predate the earliest priority date of the '571 patent.

C. Claim Construction under 37 C.F.R. §§ 42.104(b)(3)[2]

A claim subject to IPR is given its "broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). Thus, the words of the claim are given their plain meaning unless that meaning is inconsistent with the specification. *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). For this proceeding, Petitioner submits constructions for the following terms.[3] All remaining terms should be given their broadest reasonable plain meaning.[4]

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[1] U.S. Appl. Ser. No. 07/337,579 fully supports the disclosures of Mehrotra relied on in this Petition thereby entitling Mehrotra to the priority date of April 13, 1989.

[2] Exhibit 1011 is MLC's infringement contentions from *MLC Intellectual Property, LLC v. Micron Tech., Inc.*, No. 3:14-cv-03657 (N.D. Cal. August 12, 2014).

[3] Because the standards of claim interpretation applied in litigation can differ from PTO proceedings, any interpretation of claim terms in this IPR is not binding upon Petitioner in any litigation related to the subject patent. *See In re Zletz*, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

[4] When a patent is set to expire during the pendency of an *inter partes* review then the standard for claim construction shifts from the broadest reasonable interpretation standard to the *Markman* standard. The constructions proposed herein are

(i) Reference voltage selecting means for selecting one of a plurality of reference voltages / Selecting device which selects one of a plurality of reference signals / Selecting one of a plurality of reference signals

The claim term "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information" is a means-plus-function term governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "selecting one of a plurality of reference voltages in accordance with said input information" and the corresponding structure described in the specification is the verify reference voltage select circuit 222. *See* Ex. 1003 at ¶¶ 45-52.

The '571 patent describes, at col. 8, lines 26-29, that the "verify reference voltage select circuit 222 **provides** an analog voltage reference level signal X to one input terminal of an analog comparator 202," (emphasis added) and, at col. 8, lines 40-43, that the "verify reference voltage select circuit 222 is controlled by the 2-output bits from a 2-bit input latch/buffer circuit 224, which receives binary input bits from the I/O terminals 162 and 164." The "verify reference voltage select circuit 222 analog output voltage X is determined by decoding the output of the n-bit input latch/buffer 224 (n=2 in the illustrative form)." Ex. 1001 at 9:11-14.

Further, with respect to a digital implementation of the '571 patent device,

consistent with the specification and claims (*i.e.*, the instrinsic evidence) and therefore should not be affected by the standard applied.

the "digital comparator would use the encoded data from the encode circuitry 160 which represents the current contents of the EANVM cell 102" and the "verify reference voltage select [circuit] 222 would provide **the voltage to be encoded with the input** coming from the output of the n-bit input latch/buffer 224, representing the data to be programmed." *Id*. at 11:50-56 (emphasis added). Thus, in this implementation, the verify reference voltage select circuit 222 receives input information from the n-bit input latch/buffer 224 and selects and provides an encoded (*e.g*., in digital form) reference signal to the digital comparator that represents the input information. *See* Ex. 1003 at ¶¶ 39-42, 46-52.

The '571 patent describes no other device or process for further manipulating or handling the reference signal from the verify reference voltage select circuit 222, which should be in an encoded, digital form for use by the digital comparator. This confirms that the verify reference voltage select circuit 222 selects and provides such a reference voltage to the comparator. *See* Ex. 1003 at ¶¶ 39-42.

The '571 patent describes that the "input information" can be in an n-bit format (*e.g*., a digital format). *See* Ex. 1001 at 8:40-43. For example, for a four memory state/two-bit digital implementation the memory states can be as follows: a first state (0,0); a second state (0,1); a third state (1,0); and a fourth state (1,1).

See id. at 7:9-15, 7:30-39.[5] Thus the input to the reference voltage select circuit 222 can be in the form of two, digital, binary bits corresponding to the memory state to which the memory cell is to be programmed. *See* Ex. 1003 at ¶ 39.

As such, a person of ordinary skill in the art would have interpreted this feature to be broad enough to include and be met by a device or process that takes input information (*e.g*., in an n-bit form) and selects, for a given cell's program/verify cycle, a reference voltage from a plurality of reference voltages, where the selected reference voltage is based on the input information (*e.g*., desired memory state). *See* Ex. 1003 at ¶¶ 45-52. The reference voltage provided by the reference voltage selecting means can be in either an analog or digital form. *See* Ex. 1003 at

[5] During the 2010 ITC case, referenced above in Section I(B), the expert for the predecessor-in-interest of the '571 patent, BTG, described the operation of the reference voltage select circuit 222: "Then it says a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state. Let me stop there. The circuit shows that I'm going to store two bits, and you can see this arrow and that little slash means that this is really not one wire, it's really two wires. **And depending on whether that is a 0-0, a 0-1, et cetera, all the way to 1-1, information is going to come into this verify reference select** . . . ." Ex. 1007 at 54:12-22 (Emphasis added).

¶¶ 48-50, 53. Such selection would include selecting a reference voltage in accordance with the input information, *e.g*., for (1,1) two-bit information input the reference voltage would be provided as a 5 Volt "High", 5 Volt "High" digital voltage waveform[6]. *See* Ex. 1003 at ¶¶ 45-52.

Petitioner asserts that the construction in the preceding paragraph is applicable to claim terms "selecting device which selects one of a plurality of reference signals," whether or not determined to be a means-plus-function limitation, and "selecting one of a plurality of reference signals." *See* Ex. 1003 at ¶¶ 51-52.

(ii) Reference voltage(s) / Reference signal(s)[7]

As noted, the term "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information" is broad enough to cover both the analog and digital comparison implementations with corresponding analog and digital reference signals. *See* Ex. 1003 at ¶¶ 45-52, 53-58.

The '571 patent describes that the "verify reference voltage select circuit 222

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[6] This reference voltage could, for example, be provided through two serial "high" signals where each high signal corresponds to a "1" bit. *See* Ex. 1003 at ¶ 42. Or the reference voltage could be provided in the parallel manner on two data lines through two concurrently sent "high" signals. *See* Ex. 1003 at ¶ 42.

[7] The '571 patent at times uses reference voltage(s) interchangeably with reference signal(s). *See* Ex. 1001 at claims 1 and 6.

provides an **<u>analog voltage reference level signal X</u>** to one input terminal of an analog comparator 202." *See* Ex. 1001 at 8:26-29 (emphasis added). For example, the analog reference signals could be 0.5, 1.5, 2.5 and 3.5 Volts. *See* Section V(A)(ii). The '571 patent discloses that the reference signal can also be a digital signal, as described in connection with the implementation of a digital comparator. *See id*. at 11:50-56 (the "verify reference voltage select 222 would provide **<u>the voltage to be encoded with the input</u>** coming from the output of the n-bit input latch/buffer 224, representing the data to be programmed.") (emphasis added).

As noted above, in this digital context, the '571 patent describes no other device(s) or process(es) for further manipulating or handling the reference signal from the verify reference voltage select circuit 222, which should be in an encoded, digital form for use by the digital comparator. *See* Ex. 1003 at ¶¶ 39-42. Thus, as an example in the digital context, the respective "plurality of reference signals" for four memory states, *e.g.*, (0,0), (0,1), (1,0), and (1,1), could be voltage signals of 0 Volts, 0 Volts (*e.g.*, a first reference voltage); 0 Volts, 5 Volts (*e.g.*, a second reference voltage); 5 Volts, 0 Volts (*e.g.*, a third reference voltage); and 5 Volts, 5 Volts (*e.g.*, a fourth reference voltage) transmitted serially or in parallel. *See* Ex. 1003 at

¶¶ 42-43. Thus the ’571 patent describes that the selected reference voltage / reference signal[8] can be analog or digital.

As such, a person of ordinary skill in the art would have interpreted these features to be broad enough to include and be met by either a digital reference voltage/signal or an analog reference voltage/signal. *See* Ex. 1003 at ¶¶ 53-58.

IV. SUMMARY OF THE ’571 PATENT

A. Brief Description

Generally, the ’571 patent is directed to a non-volatile, electrically-alterable memory device with memory cells each having more than two memory states, *e.g.*, four memory states to store two bits of information in each cell. *See* Ex. 1001 at Abstract, Ex. 1003 at ¶ 26. Such a memory cell structure providing for more than two memory states is commonly known as a multilevel cell (MLC) memory. *See* Ex. 1003 at ¶¶ 24-27.

More specifically, the ’571 patent describes a MLC reading process, to determine the current memory state of the memory cell, and a programming and veri-

[8] A person of ordinary skill in the art would understand that the term “reference signal” and term “reference voltage” are used without meaningful distinction in the ’571 patent, and that both terms nevertheless cover analog and digital waveforms. *See* Ex. 1003 at ¶¶ 53-58.

fication process, to program the memory cell to the desired memory state and verify that the programming is correct. *See* Ex. 1003 at ¶¶ 26-44.

Regarding the reading process for a memory cell configured to store two bits of information, and thus having four memory states such as (0,0), (1,0), (0,1), and (1,1), the '571 patent describes using three sense amplifiers (154, 156 and 158) to determine the current memory state of the memory cell, as shown in Figure 6 below. *See* Ex. 1003 at ¶¶ 27-30; *see also* Ex. 1001 at 7:8-55.

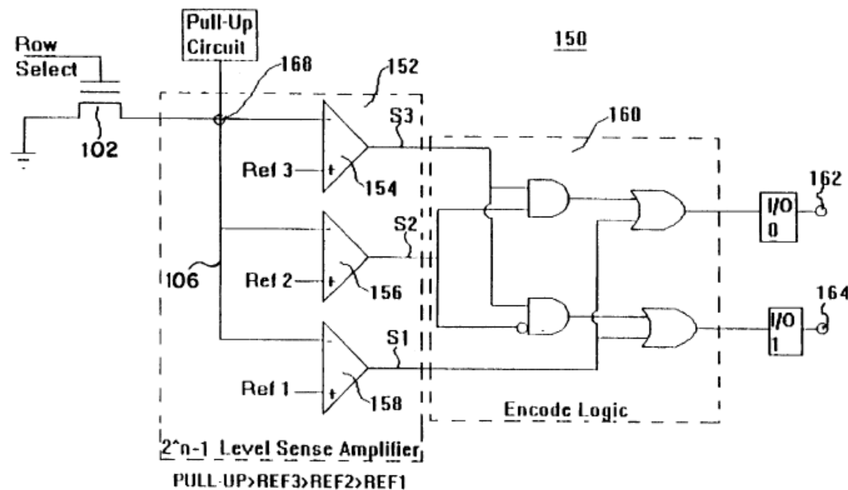


Figure 6

Particularly, each of the three sense amplifiers 154, 156 and 158 uses as an input a respective different reference signal/voltage (*i.e.*, Ref 1, Ref 2, and Ref 3) to collectively distinguish between the four memory states, as shown in Figure 7. Thus, by comparing the bit line output of the memory cell to each of the three reference voltages, the system can determine the current memory state of the memory

cell. *See id*. The two bit representation of the memory state is provided at I/O terminals 162 and 164. *See* Ex. 1001 at 7:31-38 (explaining the encode logic used by the circuit 160 to generate the two bit representation of the memory state).

With reference to the programming and verification process, the ’571 patent describes that programming a memory cell to its desired memory state involves an iterative process during which programming pulses are applied to the memory cell and, after each programming pulse, a verification process compares the current memory state of the memory cell (*e.g*., by use of the cell’s bit line voltage) to a reference signal corresponding to the desired memory state. *See, e.g*., Ex. 1001 at Abstract; 10:14-60 (“Programming . . . is verified by selecting a reference signal corresponding to the information to be stored and comparing a signal of the cell with the selected reference signal”); *see also* Ex. 1003 at ¶¶ 31-44. When the verify process confirms the memory cell is programmed to the desired memory state, *e.g*., based on a comparison indicating the bit line signal exceeds the reference signal corresponding to the desired memory state, programming is stopped. *See* Ex. 1001 at 10:26-37, 10:52-60; *see also* Ex. 1003 at ¶¶ 31, 38.

Figure 11 shows this iterative, stair-step programming pulse and verification process, where the memory cell is being programmed to the desired memory state (1,0), as shown on the y-axis, corresponding the reference signal Vref3. *See id*. Each stair step in the illustrated time-changing voltage of the memory cell (*e.g*., bit

line voltage) represents an additional programming pulse applied to the memory cell to drive the voltage towards a reference voltage within the voltage range defining the desired memory state (*i.e.*, in between Vt2 and Vt3 defining the memory state (1,0)). *See* Ex. 1001 at 8:26-40, Ex. 1003 at ¶¶ 32-34. In this example, the determination of when the cell is programmed to the desired memory state is based on a comparison between the cell's bit line voltage, which is proportional to its threshold voltage, and Vref3. *See id*. In other words, the programming pulses are applied to the memory cell until the bit line voltage representing the cell's current memory state exceeds Vref3, which corresponds to memory state (1,0), indicating that the cell has been correctly programmed to the (1,0) memory state. *See id.*

Figure 8 shows a functional-level block diagram implementation of the memory read and program and verification processes.

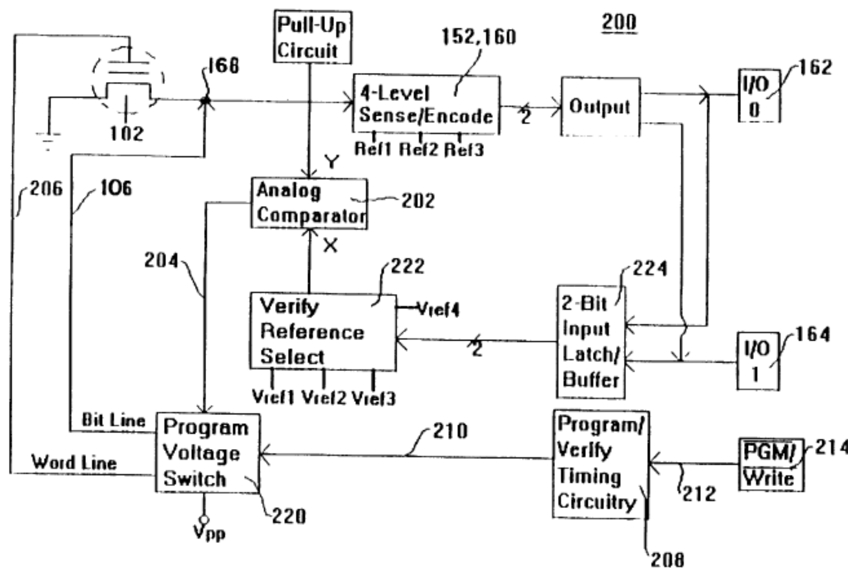


Figure 8

For example, the memory cell read process described above is implemented by the 4-Level Sense/Encode device 152,160 in Figure 8. *See* Ex. 1001 at 8:8-40; *see also* Ex. 1003 at ¶¶ 27-30.

The ’571 patent describes that the verification process can be implemented in both digital and analog designs. *See* Ex. 1001 at 9:64-65, Ex. 1003 at ¶ 36. With respect to the analog implementation, the verification process is implemented through the Verify Reference Select device 222 and the Analog Comparator device 202. *See* Ex. 1001 at 8:40-9:24; Ex. 1003 at ¶¶ 36-38. Specifically, the Verify Reference Select device 222 receives the desired memory state information from I/O input devices 162, 164, through the 2-Bit Input Latch/Buffer 224. *See* Ex. 1001 at 8:40-9:24; *see also* Ex. 1003 at ¶ 37. The Verify Reference Select device 222 uses this information to select a reference signal corresponding to the desired memory state (*e.g.*, selects reference voltage Vref3 representing memory state (1,0)). *See id*. The Verify Reference Select device 222 then provides the reference signal to the Comparator device 202. *See id.*

The Analog Comparator device 202 compares the reference signal, corresponding to the desired memory state, to the signal (*e.g.*, the bit line voltage) seen at output terminal 168 of the memory cell 102, which represents the current memory state of the cell. *See* Ex. 1001 at 8:40-9:24; Ex. 1003 at ¶¶ 36-38. If this comparison, *e.g.*, through Analog Comparator output 204, indicates the memory

cell is programmed to the desired memory state then the Program Voltage Switch 220 is disabled, stopping the programming process. *See id*. ("The output signal from the analog comparator is provided on a signal line 204 as an enable/disable signal for the program voltage switch 220. An output signal line 206 from the program voltage switch 220 provides the word line program voltage to the control gate of the EANVM cell 102. Another output signal line 106 constitutes the bit line and provides the bit line programming voltage to the bit line terminal 168 of EANVM cell 102."). If not, the Program Voltage Switch 220 allows programming to continue until the desired memory state is reached. *See id.*

The '571 patent further describes that a digital comparator can be used in place of the Analog Comparator device 202. *See* Ex. 1001 at 11:49-58; 9:64-65 ("The comparator can be either digital or analog"). Specifically, the '571 patent describes that the encoded signal (*e.g*., 2-bit binary digital representation) from the encode circuit 160, which is part of the read process, is provided as one input to the digital comparator to represent the current memory state of the cell. *See id*; *see also* Ex. 1003 at ¶¶ 39-43. The other input to the digital comparator is provided by the Verify Reference Select device 222 in the form of an encoded voltage (*e.g*., representing the desired memory state) derived from the output of the 2-Bit Input Latch/Buffer 224, which receives binary input information from the I/O terminals 162 and 164 corresponding to the desired memory state. *See id*. For example, the

Verify Reference Select device 222 selects and provides to the digital comparator an encoded, digital reference voltage signal of 5 Volts, 0 Volts to represent a two-bit binary input (*e.g.*, desired memory state) of (1,0).[9] *See* Ex. 1003 at ¶¶ 39-43. Thus, the '571 patent describes both analog and digital implementations for the verify process. *See* Ex. 1003 at ¶¶ 39.

In the Background of the Invention section, the '571 patent describes prior art non-volatile MLC devices such as MLC read only memory (ROM) devices. *See* Ex. 1001 at 1:40-57. The '571 patent touts the benefits of nonvolatile memory, such as ROM, not requiring a power source to maintain its memory state. *See id*. at 2:31-35. The '571 patent also describes prior art electrically alterable MLC devices (*e.g.*, devices with the ability to be electrically programmed and/or changed to a given memory state post manufacture) such as MLC dynamic random access

[9] The Verify Reference Select device 222 could select among any of the possible reference signal(s) to represent the input information (*e.g.*, desired memory state). For example, the reference signals (0 Volts, 0 Volts); (5 Volts, 0 Volts); (0 Volts, 5 Volts) and (5 Volts, 5 Volts) could respectively represent the four memory states (0,0), (1,0), (0,1), and (1,1), and the Verify Reference Select device 222 provides the reference signal that corresponds to the desired memory state to the comparator. *See* Ex. 1003 at ¶¶ 41-43.

memory (DRAM) devices. *See id.* at 2:13-17. Although acknowledging the benefits of the DRAM's electrical alterability, the '571 patent notes the DRAM's requirement for constant power to keep its memory state(s). *See id.* at 2:21-30.

The '571 patent and prosecution history indicate its patentability lies in combining these two well-known types of MLC memory devices to create a non-volatile, electrically-alterable MLC device to address the well-known concerns with each. *See* Ex. 1001 at 2:31-46. During the prosecution of the '200 application, from which the '571 patent issued, the Applicant attempted to distinguish over Examiner-cited prior art by arguing that the Examiner-cited prior art was (i) not electrically alterable, non-volatile memory, (ii) did not disclose the selection of a reference voltage, and (iii) did not disclose comparing the selected reference voltage with the cell voltage and generating a control signal indicating that the cell is correctly programmed. *See* Ex. 1002 at pages 164-165. The Applicant further indicated that these alleged deficiencies in the prior art were reasons for allowance. *See* Ex. 1002 at page 166.

However, as described in more detail in Section V, several prior art references clearly disclose the allegedly novel and non-obvious features.

B. Summary of the Prosecution History of the '571 Patent

U.S. Patent No. 5,764,571 was filed on February 27, 1995, as U.S. Patent Appl. Ser. No. 08/410,200 ("the '200 application"), and issued on June 9, 1998.

See Ex. 1001. The ’571 patent claims to be a divisional of U.S. Patent No. 5,394,362 filed on June 4, 1993, which, in turn, claims to be continuation of U.S. Patent No. 5,218,569 filed on February 8, 1991. *See id*.

The USPTO issued an office action on December 17, 1996, rejecting or objecting to all of the original twenty-three claims of the ’200 application over Suzuki (U.S. Patent No. 4,809,224) as being “drawn to a basic multi-level memory with comparator as shown by Suzuki et al.” *See* Ex. 1002 at page 108.

In response, the Applicant amended certain claims to add limitations directed to selecting a reference voltage for use in comparing to a signal representing the current state of the memory cell. *See* Ex. 1002 at pages 149-163. The Applicant then argued that it “is apparent that Suzuki neither teaches nor suggests a multi-level memory device having the aforementioned features of Claim 1. Note, for example, that Suzuki discloses a conventional ROM which is not electrically alterable . . . . Further, Suzuki lacks any suggestion whatsoever of the reference voltage selecting means and comparator means, both as now defined.” Ex. 1002 at page 165.

The USPTO subsequently allowed all pending claims in a Notice of Allowance, which did not include any reasons for allowance or an examiner’s amendment. *See* Ex. 1002 at page 169.

V. MANNER OF APPLYING CITED PRIOR ART TO EVERY

CLAIM FOR WHICH IPR IS REQUESTED, THUS ESTABLISHING A REASONABLE LIKELIHOOD THAT AT LEAST ONE CLAIM OF THE ’571 PATENT IS UNPATENTABLE

As detailed below, this Petition shows a reasonable likelihood that Petitioner will prevail with respect to at least one of the Challenged Claims of the ’571 patent. Indeed, the prior art references Kitamura, Mehrotra, Lee, and Kokubun show that features claimed in the ’571 patent were known and disclosed in several different contexts and through several different techniques[10]. The grounds presented below show that each of the Challenged Claims of the ’571 patent is unpatentable.

A. GROUND 1 – Kitamura renders obvious all Challenged Claims of the ’571 Patent

Kitamura renders obvious all Challenged Claims of the ’571 patent.

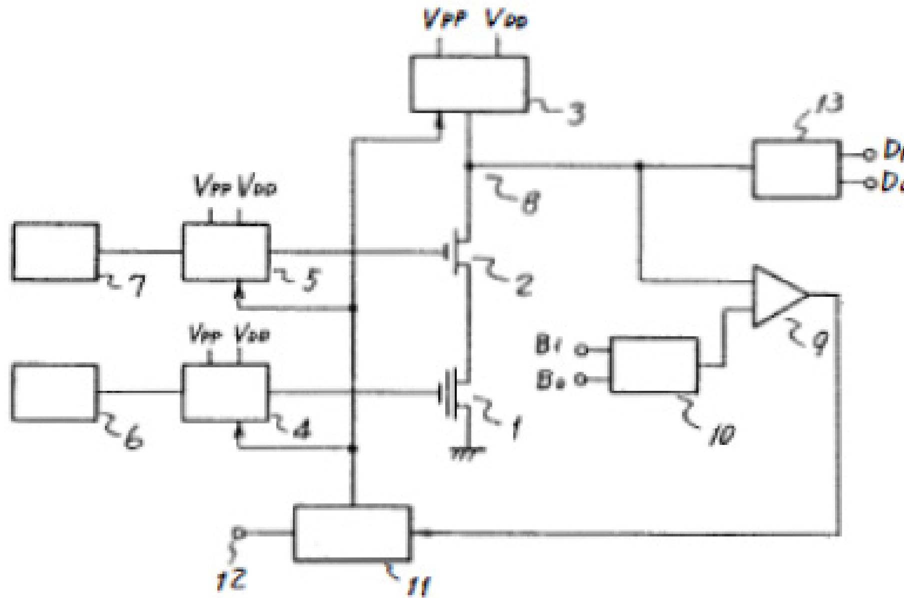
i. *Electrically Alterable Non-Volatile Memory Cell (claims 1, 9, 12, 30, 42, 45)*[11]

Kitamura discloses an electrically alterable, non-volatile memory device with a memory cell capable of storing two bits of information, requiring four memory states. *See* Ex. 1010 at ¶¶ [01], [06], [09], [14], Ex. 1003 at ¶¶ 59-60, 65-66.

[10] *See* paragraphs 15-17 of the Expert Declaration for a description of a person of ordinary skill in the art.

[11] Like forms of this claim element appear in each of the Challenged Claims.

Specifically, Kitamura describes its MLC memory device, in part, with reference to Fig. 1, reproduced below.



Kitamura Fig. 1

As depicted in Fig. 1, the Kitamura memory device includes a memory cell 1 (depicted as a floating gate metal oxide semiconductor (MOS) transistor) capable of storing two bits of information corresponding to four memory states (*i.e.*, 2^2 memory states). *See* Ex. 1003 at ¶¶ 65-66; *see also* Ex. 1010 at ¶¶ [01], [06], [09], [13], [14]. The Kitamura memory device, like the claimed ’571 memory device, can program the memory cell 1 to one of four memory states based on desired memory state input information (in the case of Kitamura, input information bits B_0 and B_1).[12] *See id.*

[12] The transistor 2 is used to select the memory cell 1, for example, to be read. *See*

The Kitamura memory device programs the memory cell 1 by iteratively applying writing signals/programming pulses to the cell 1 to move the memory state of the memory cell 1 to the desired memory state (*e.g.*, from memory state 0 to memory state 1, as shown in Table 1 in Section V(A)(ii) below). *See* Ex. 1003 at ¶¶ 69-72; Ex. 1010 at ¶¶ [06]-[10], [13], [14]. Programming ceases when the Kitamura device determines that the memory cell 1 is correctly programmed to its desired memory state based on a comparison of a signal representing the current memory state of the cell 1 (*e.g.*, on the bit line) with a signal representing the desired memory state, which corresponds to B_0 and B_1. *See* Ex. 1003 at ¶¶ 69-73; *see also* Ex. 1010 at ¶¶ [06]-[10], [13], [14].

Particularly, the Kitamura memory device includes an A/D (analog-to-digital) conversion circuit 13 to read and output the current state of the memory cell 1, a D/A (digital-to-analog) conversion circuit 10 to select (based on input bits B_0 and B_1) the reference signal/information corresponding to the desired memory state for the cell 1, and comparator 9 to compare the current memory state of the cell 1 to the desired memory state, from the D/A conversion circuit 10, to determine/verify

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Ex. 1003 at ¶¶ 67-68. When the memory cell 1 is selected, the transistor 2 is "turned on" to act as a direct connection (*e.g.*, short) between the read point 8 and the memory cell 1. *See* Ex. 1003 at ¶¶ 67-68.

if and when the cell 1 is correctly programmed to the desired memory state. *See* Ex. 1003 at ¶¶ 65-79; *see also* Ex. 1010 at ¶¶ [06]-[11], [14].

ii. *Reference Voltage Selecting Means (claim 1) / Selecting Device (claims 9, 12, 30) / Selecting One of a Plurality of Reference Signals (claims 42, 45)*[13]

The inputs defining the desired state of the memory cell 1 (*i.e.*, the memory state to which the cell 1 is to be programmed) are digital input bits B_0 and B_1. *See* Ex. 1010 at ¶ [09], Fig. 1. Input bits B_0 and B_1 collectively define four memory states, *i.e.*, 0,0; 1,0; 0,1; and 1,1. *See* Ex. 1003 at ¶ 65. These desired memory state defining input bits are fed into the D/A conversion circuit 10. In turn, the D/A conversion circuit 10 converts the two digital bits B_0 and B_1 to an analog signal by selecting the analog signal that corresponds to bits B_0 and B_1. *See* Ex. 1010 at ¶¶ [07], [09]; Ex. 1003 at ¶¶ 74-79. For example, the mapping between the various values for B_0 and B_1 to their respective corresponding analog signal could be:

B_0, B_1	D/A Output Voltage	Memory State	A/D Input Voltage Range[14]

[13] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

[14] The A/D Input Voltage Range defines the range of analog voltages interpreted by the A/D conversion circuit 13 to be in a particular memory state. *See* Ex. 1003 at ¶¶ 74-75. This results in the output(s) of the D/A conversion circuit 10 being in the middle of the respective memory state voltage ranges of the A/D conversion

1, 1	0.5 Volts	1	0 to 1 Volts
0, 1	1.5 Volts	2	1.x to 2 Volts
1, 0	2.5 Volts	3	2.x to 3 Volts
0, 0	3.5 Volts	4	3.x to 4 Volts

Table 1

Here, the plurality of reference signals is 0.5, 1.5, 2.5 and 3.5 Volts.[15] *See* Ex. 1003 at ¶¶ 74-75. By way of example, if the values of input bits B_0 and B_1 are 1 and 0, respectively, the D/A conversion circuit 10 would select and provide an analog signal of 2.5 Volts to the comparator 9 to represent the memory state to which the memory cell 1 is to be programmed. *See* Ex. 1003 at ¶¶ 74-79.

iii. ***Memory Cell Programming Means (claim 1) / Programming Signal Source (claims 9, 12, 30) / Applying a Programming Signal*** [16]***(claims 42, 45)***[17]

circuit 13. *See id.*

[15] Although this example configuration suggests the reference signals are linearly proportional, they need not be. Kitamura does not preclude using any of linear, non-linear or randomly spaced reference voltages. *See* Ex. 1003 at ¶ 76.

[16] The discussion in this Section is applicable to terms “memory cell programming means,” “programming signal source” and “applying a programming signal.”

[17] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

The memory cell programming and verification process of Kitamura is similar to that described above in Section IV(A) with reference to the ’571 patent but accomplished through a slightly different approach (in terms of process and devices), and nevertheless would render the memory cell programming means, programming source, and application of the programming signal obvious to one of ordinary skill in the art as described below. Kitamura describes an iterative process whereby a writing signal/programming pulse is applied to the memory cell 1 followed by a read/verification process to determine if the writing signal put the memory cell 1 into its desired memory state. *See* Ex. 1003 at ¶¶ 69-73; Ex. 1010 at ¶¶ [06]-[10], [13], [14] (“This write mode signal causes the read/write switching signal generation circuit 11 to generate read/write signals that **periodically repeat** a write period whose level is one binary value and a read period whose level is the other binary value.”) (Emphasis added). The programming process continues (*e.g.*, serial writing signals/programming pulses are applied) until the memory cell is correctly programmed, as determined by the comparator 9. *See id*.

The read/write switching signal generation circuit 11 controls the writing signals/programming pulses applied to the memory cell 1. *See id*. The read/write switching signal generation circuit 11 is enabled by the output of the comparator 9. *See* Ex. 1010 at ¶ [09] (“[B]ut when the comparator 9 determines that V_O is higher

than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation."). The operation of the comparator 9 is described in more detail below in Section V(A)(iv).

The read/write switching signal generation circuit 11 controls the application of programming pulses to the memory cell 1 by generating read/write signals that then cause[18] the driver circuit 4 to provide a writing signal (V_{pp}) to the memory cell 1 on its word line and the load circuit 3 to couple a writing signal (V_{pp}) to the memory cell 1 on its bit line—these three devices perform a function similar to that of the single Program Voltage Switch 220 of the '571 patent but through a multi-device, stepped process (as noted above). It would have been obvious to one of ordinary skill in the art to combine the read/write switching signal generation circuit

[18] The read/write switching signal generation circuit 11 also causes driver circuit 5 to apply either V_{pp} or V_{dd} to transistor 2, for program and read processes respectively, to enable the memory cell 1 to be programmed or read, as applicable. *See* Ex. 1003 at ¶¶ 67, 71; Ex. 1010 at ¶¶ [07]-[10] ("In the write period, a voltage close to V_{PP} is outputted from the drivers 4 and 5 and provided to the memory cell 1 and the MOS transistor 2, and in the read period, a voltage close to V_{DD} is outputted and provided to the memory cell 1 and the MOS transistor 2.").

11, the driver circuit 4 and the load circuit 3 for use in performing the programming function *(e.g.*, applying a program signal) of the "memory cell programming means" and "programming signal source." *See* Ex. 1003 at ¶¶ 70-71; Ex. 1010 at ¶¶ [07]-[10] ("The switching circuit 3 supplies V_{PP} during the write period, and V_{DD} during the read period, to the read point 8;" "In the write period, a voltage close to V_{PP} is outputted from the drivers 4 and 5 and provided to the memory cell 1."). The application of these writing signals to the memory cell 1 causes the memory cell to change its threshold voltage, which, in turn, results in memory state changes. *See* Ex. 1010 at ¶¶ [09], Fig. 2; Ex. 1003 at ¶¶ 67, 70-72.

The read/write switching signal generation circuit 11 also controls the reading/verification of the memory cell to, in part, determine the cell's current memory state. *See* Ex. 1010 at ¶¶ [08], [10]. Namely, the read/write switching signal generation circuit 11 generates read/write signals that cause the driver circuit 4 to provide a reading signal (V_{dd}) to the word line and cause the load circuit 3 to couple a reading signal (V_{dd}) to the bit line. *See id.* With these signals applied, the current state of the memory cell is determined by observing (reading) the signal on the memory cell's bit line at "read point 8." *See* Exhibit 1010 at ¶¶ [08], [10] ("8 is a read point from the memory cell 1"), *see also* Ex. 1003 at ¶ 72. These programming and read/verification steps continue until the memory cell 1 is programmed to its desired memory state. *See* Ex. 1003 at ¶ 73; Ex. 1010 at ¶¶ [09], [14].

Kitamura's application of control signals to a memory cell's word line and bit line for programming purposes parallel those described in the '571 patent. *See* Ex. 1001 at 8:46-53 ("The output signal from the analog comparator is provided on a signal line 204 as an enable/disable signal for the program voltage switch 220. An output signal line 206 from the **program voltage switch 220 provides the word line program voltage to the control gate of the EANVM cell 102. Another output signal line 106 constitutes the bit line and provides the bit-line programming voltage to the bit-line terminal 168 of EANVM cell 102**.") (Emphasis added); Ex. 1003 at ¶ 71.

iv. *Comparator Means (claim 1) / Comparator (claim 9)/ Verifying Device (claim 12) / Control Device (claim 30) / Verifying Whether Said Memory Cell is Programmed to the State Indicated by Said Information (claim 42) / Detecting a Parameter Indicating the State of the Memory Cell (claim 42) / Controlling the Application of Said Programming Signal (claim 45)* [19]

After each writing signal/programming pulse in the programming and verification process of Kitamura, the comparator 9 compares the signal representing the current memory state of the memory cell (*i.e.*, by observing the voltage at "read point 8") with the signal representing the desired memory state to which the memory cell is to be programmed (*i.e.*, the analog voltage output by the D/A conversion circuit 10), in accord with input bits B_0 and B_1. *See* Ex. 1010 at ¶ [09]; Ex.

[19] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

1003 at ¶¶ 72-73. The programming process continues until the comparison indicates that the signal at read point 8 (representing the current memory state) is higher than the output of the D/A conversion circuit 10 (representing the desired memory state):

> Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals [B_0 and B_1].

Ex. 1010 at ¶ [09], *see also* Ex. 1003 at ¶ 74.

Thus when the memory cell 1 is programmed to the desired memory state, the output of comparator 9 causes the read/write switching signal generation circuit 11 to stop programming the memory cell 1. *See id.*; *see also* Ex. 1003 at ¶ 73.

v. ***Example Comparison of Kitamura and the ’571 Patent***

The following color-coded table and figures show the features of the ’571 patent disclosed by Kitamura in the context of figures from each.[20]

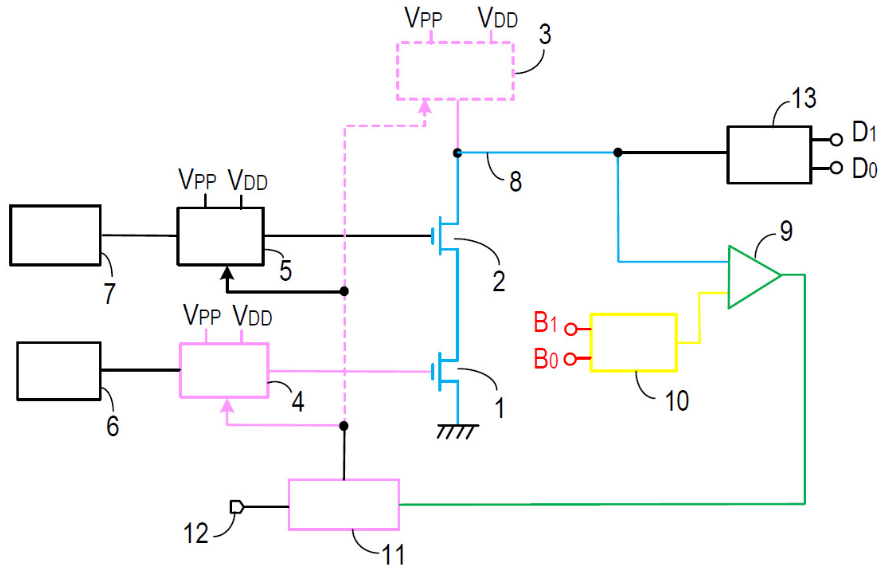
[20] This comparison does not represent Petitioner’s full or binding claim construction positions, but rather is a high-level, illustrative comparison of two example

	Kitamura	’571 Patent
Electrically alterable non-volatile memory cell	Memory cell 1	Memory cell 102
Input information corresponding to the desired memory state	B_0, B_1	I/O 0 (162), I/O 1 (164)
Selecting device / Selecting one of a plurality of reference signals in accordance with the input information	D/A conversion circuit 10	Verify Reference Select device 222
Verifying Device / Control Device / Verifying Whether Said Memory Cell is Programmed to the State Indicated by Said Information / Detecting a Parameter Indicating the State of the Memory Cell / Controlling the Application of Said Programming Signal	Comparator 9	Analog comparator 202
Programming signal source / Applying a programming signal[21]	Read/write switching signal generation circuit 11	Program voltage switch 220

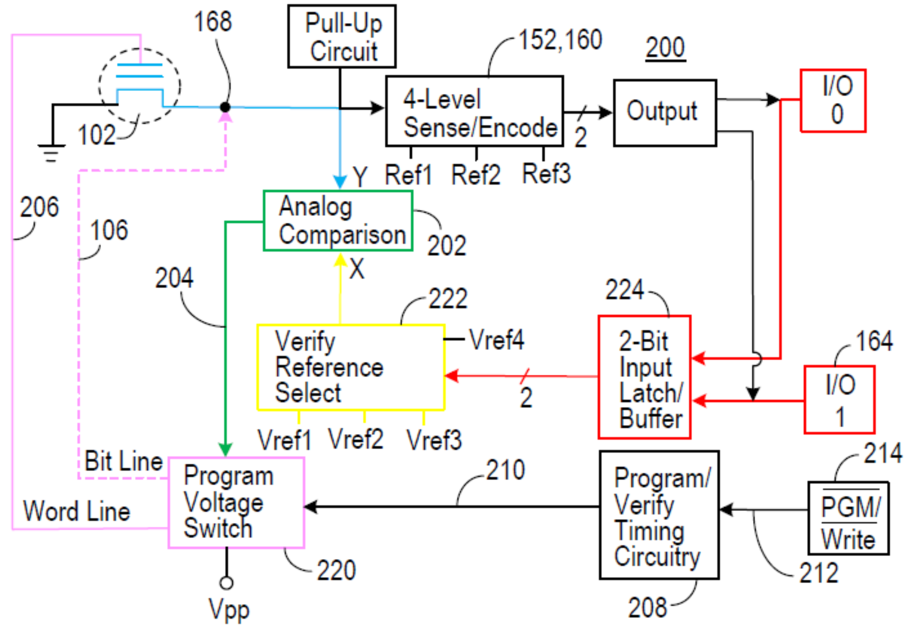
figures from the ’571 patent and Kitamura.

[21] Other components from Kitamura and the ’571 patent are also involved in the programming/verification process such as, in the context of the ’571 patent, the timing circuit 208, verify reference select device 222 and comparator 202. *See* Ex. 1001 at 10:14-36, 8:34-45.

Table 2



Kitamura, Fig. 1 (annotated)



’571 patent, Fig. 8 (annotated)

As explained in greater detail in the following Claim Chart I, the features of the Challenged Claims of the ’571 patent are rendered obvious by Kitamura, and

thus, unpatentable under 35 U.S.C. § 103. *See* Ex. 1003 at ¶¶ 60, 80.

[1a] A multi-level memory device comprising:	Kitamura discloses a multi-level memory device. "A non-volatile memory that includes a semiconductor non-volatile memory element whose characteristic is continuously varied by writing; a circuit that alternately switches between a write mode and a read mode at regular time intervals; a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that converts an analog signal that has been read into a digital signal." Ex. 1010 at ¶ [01]. "It is an object of the present invention to reduce the number of memory elements and lower the price by storing a plurality of bits in a single memory element." *Id*. at ¶ [05]. "Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." *Id.* at ¶ [09]. "As described above, with the present invention, writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14].

	See id. at Fig. 1, Ex. 1003 at ¶¶ 65-66.
[1b] an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;	Kitamura discloses an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$. "It is an object of the present invention to reduce the number of memory elements and lower the price by storing **a plurality of bits in a single memory element**." Ex. 1010 at ¶ [05] (emphasis added). "Meanwhile, **the two-bit input digital signals B_0 and B_1 to be written** are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. **Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2**." *Id.* at ¶ [09] (emphasis added). "As described above, with the present invention, writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion, and **this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits.**" *Id.* at ¶ [14] (emphasis added). "The working example in FIG. 1 shows the circuit of a one-element, two-bit nonvolatile memory . . . ." *Id.* at ¶ [12]. *See id.* at Fig. 1; Ex. 1003 at ¶¶ 65-66.

[1c] memory cell programming means for programming said multi-level memory cell in accordance with said input information;	Kitamura discloses a memory cell programming means for programming said multi-level memory cell in accordance with said input information. "When data is written, first an address for selecting the memory cell 1 is provided from the outside to the address decoders 6 and 7, and a write mode signal is provided to the mode switching terminal 12. **This write mode signal causes the read/write switching signal generation circuit 11 to generate read/write signals that periodically repeat a write period whose level is one binary value** and a read period whose level is the other binary value. **In the write period, a voltage close to V_{PP} is outputted from the drivers 4 and 5 and provided to the memory cell 1 and the MOS transistor 2**, and in the read period, a voltage close to V_{DD} is outputted and provided to the memory cell 1 and the MOS transistor 2. The switching circuit 3 supplies VPP during the write period, and V_{DD} during the read period, to the read point 8." Ex. 1010 at ¶ [08] (emphasis added). "Since the floating gate MOS transistor 1 and the MOS transistor 2 constitute a ratio circuit with the load circuit 3, when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3. **Meanwhile, the two-bit input digital signals B0 and B1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation**. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." *Id.* at ¶ [09] (emphasis added). "As described above, with the present invention, **writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a**

	voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). "The relation between the write time t of the memory cell 1 and the threshold voltage V_T of the memory cell 1 . . . is the relation shown in FIG. 2 under constant voltage conditions, and V_T rises as the write period lengthens." *Id.* at ¶ [09]. *See id.* at Figs. 1 and 2, Ex. 1003 at ¶¶ 69-71.
[1d] reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and	Kitamura discloses a reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states. "A non-volatile memory that includes . . . a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result . . . ." Ex. 1010 at ¶ [01]. "[W]hen the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes . . . . Meanwhile, the **two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals**, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." *Id.* at ¶ [09] (emphasis added). "As described above, with the present invention, writing and reading are repeated at short periods until the output voltage to

	an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting **a plurality of bits of digital signal to D/A conversion, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element**, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). *See id.* at Fig. 1, Ex. 1003 at ¶¶ 74-79.
[1e] comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage,	Kitamura discloses a comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage. "[T]he output voltage (V_O) of the read point 8 changes as shown in FIG. 3. Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." Ex. 1010 at ¶ [09] . "A non-volatile memory that includes . . . a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that converts an analog signal that has been read into a digital signal." *Id*. at ¶ [01]. "[A] D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; **a circuit that compares a read level from a memory cell to the level of the analog signal**, and ends a write operation according to this result . . . ." *Id*. at ¶ [06] (emphasis added). "The present invention will now be described through reference to the drawings. FIG. 1 is a circuit diagram of a working

	example of the present invention. 1 is a memory cell constituted by a floating gate MOS transistor, 2 is a MOS transistor, 3 is a load circuit that switches between a write-use high voltage power supply (V_{PP}) and a read-use low voltage power supply (V_{DD}), 4 and 5 are driver circuits that output a high voltage during writing and a low voltage during reading by switching the power supply between V_{PP} and V_{DD}, 6 and 7 are address decoders, **8 is a read point from the memory cell 1**, **9 is a comparator** . . . ." *Id.* at ¶ [07] (emphasis added). "As described above, with the present invention, **writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion**, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added). *See id.* at Figs. 1 and 3*,* Ex. 1003 at ¶¶ 72-73.
[1f] said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.	Kitamura discloses that said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information. "Since the floating gate MOS transistor 1 and the MOS transistor 2 constitute a ratio circuit with the load circuit 3, when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3. Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the

	V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." Ex. 1010 at ¶ [09]. "A non-volatile memory that includes . . . a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that converts an analog signal that has been read into a digital signal." *Id*. at ¶ [01]. "[A] D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, **and ends a write operation according to this result** . . . ." *Id*. at ¶ [06] (emphasis added). "The present invention will now be described through reference to the drawings. FIG. 1 is a circuit diagram of a working example of the present invention. 1 is a memory cell constituted by a floating gate MOS transistor, 2 is a MOS transistor, 3 is a load circuit that switches between a write-use high voltage power supply (V_{PP}) and a read-use low voltage power supply (V_{DD}), 4 and 5 are driver circuits that output a high voltage during writing and a low voltage during reading by switching the power supply between V_{PP} and V_{DD}, 6 and 7 are address decoders, **8 is a read point from the memory cell 1**, **9 is a comparator**, 10 is a two-bit D/A conversion circuit, 11 is a read/write switching signal generation circuit, 12 is a read/write switching terminal, and 13 is a two-bit A/D conversion circuit." *Id.* at ¶ [07] (emphasis added). "As described above, with the present invention, **writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion**, and this allows a plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits." *Id.* at ¶ [14] (emphasis added).

	See id. at Figs. 1 and 3, Ex. 1003 at ¶¶ 72-73.

Kitamura also renders obvious claims 9, 10, 12, 30, 42 and 45 of the ’571 patent, as shown in Chart III in Section V(B) below.

B. GROUND 2 - Mehrotra renders obvious all Challenged Claims of the ’571 Patent

Mehrotra renders all Challenged Claims of the ’571 patent obvious.[22]

i. *Electrically Alterable Non-Volatile Memory Cell (claim 1, 9, 12, 30, 42, 45)*[23]

Mehrotra discloses an electrically alterable, non-volatile memory device with memory cells each capable of storing more than one bit of information, for example, memory cells having four memory states to store two bits of information, as claimed in each of the independent claims of the ’571 patent. *See* Ex. 1004 at 2:14-15, Ex. 1003 at ¶¶ 59, 61, 81. To this end, and similar to the ’571 patent’s Fig. 11, Mehrotra’s Fig. 7A shows four voltage ranges, on the y-axis, corresponding to four possible memory states (*i.e.*, (0,0), (0,1), (1,0), (1,1)) of a memory cell.

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[22] Mehrotra is cited on the face of the ’571 patent, but was not relied on by the Office during the prosecution of the ’200 application. Mehrotra was cited in an information disclosure statement submitted by the Applicant on May 15, 1997, that included over 80 other references. *See* Ex. 1002 at pages 124-131.

[23] Like forms of this element appear in each of the ’571’s independent claims.

Mehrotra describes this MLC device, in part, with reference to Figure 5 below. As shown in Figure 5, the Mehrotra memory device 130 includes Read Circuits 220[24] to read the current memory state of a memory cell in the Addressable EEPROM Array 60, Read/Program Latches and Shift Registers (RPLSR) 190 to select and determine the reference signal corresponding to the desired memory state for a memory cell, and a Compare Circuit 200. *See* Ex. 1003 at ¶¶ 81-105.

As discussed in more detail below, the Compare Circuit 200 receives the reference signal/information from the RPLSR 190 and receives a signal/information corresponding to the current memory state of the memory cell through the Read Circuits 220, and compares the current memory state to the desired memory state to determine/verify if the memory cell is correctly programmed to the desired memory state. *See* Ex. 1004 at 20:4-16; *see also* Ex. 1003 at ¶¶ 92-98.

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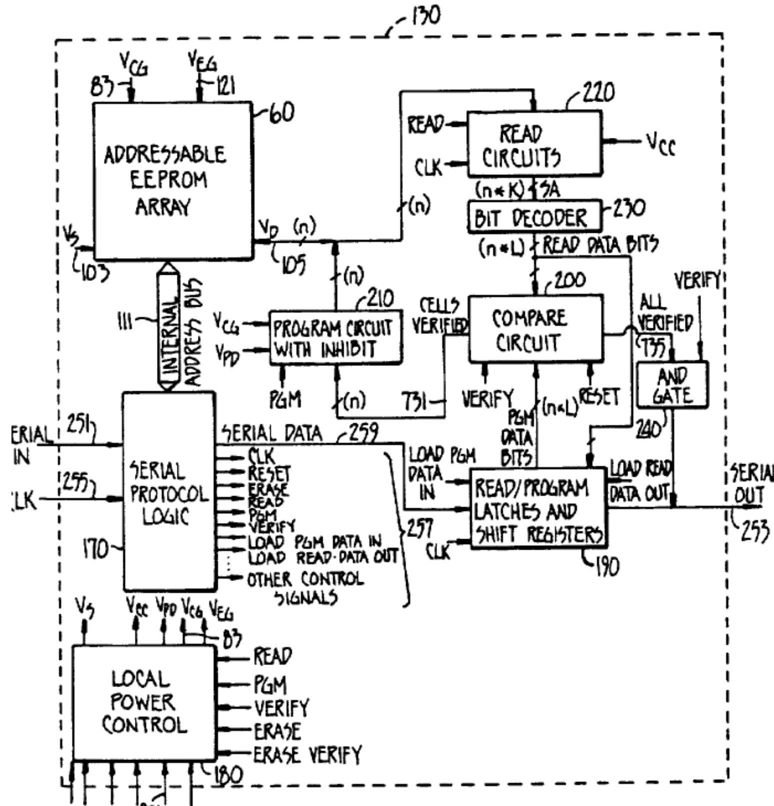
[24] Mehrotra and Harari (Ex. 1014) describe a similar read circuit configuration to that described in the '571 patent. *See* Ex. 1004 at 9:24-38; 11:55-65; 12:8-20; and Figures 9A, 9B, 9D; *see also* Ex. 1003 at ¶ 59, 61, 62, 83-91. Namely, Mehrotra's Read Circuit 220 can also use one or more sense amplifiers to compare signals corresponding to each of the possible memory states to a signal representing the current memory state of the memory cell and, thus, determine the current memory state of the memory cell. *See id*.



Mehrotra, Figure 5

ii. ***Reference Voltage Selecting Means (claim 1) / Selecting Device (claims 9, 12, 30) / Selecting One of a Plurality of Reference Signals (claims 42, 45)***[25]

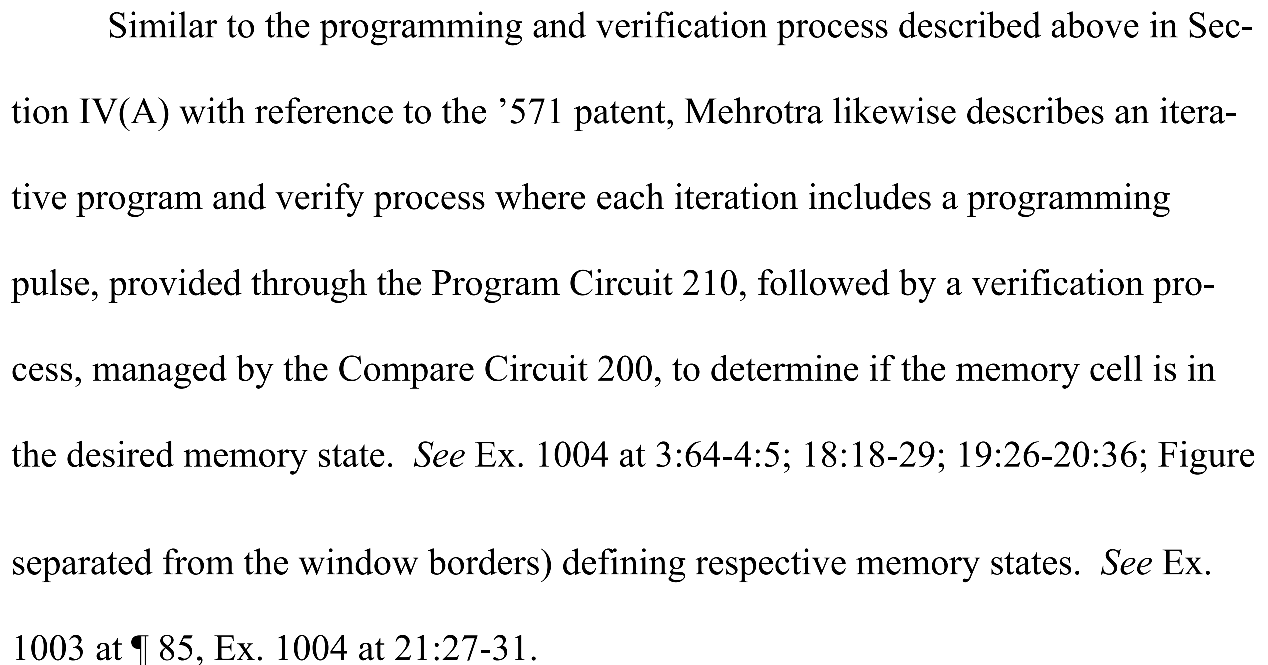
To provide the desired memory state information to the Compare Circuit 200, the Mehrotra memory device, *e.g.*, through the RPLSR 190, selects and provides a voltage or current signal(s) or waveform(s) that represents the desired memory state to the Compare Circuit 200.[26] *See* Ex. 1003 at ¶¶ 95-104.

[25] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

[26] Mehrotra describes that the reference signals can be within the windows (*e.g.*,

Thus, for example, assuming a 0 Volts signal corresponds to a binary input (0) and a 5 Volts signal corresponds to a binary input (1) then for a (0,1) desired memory state the RPLSR 190 selects and provides a 0 Volts, 5 Volts reference signal to the Compare Circuit 200 corresponding to the (0,1) input information. *See id*. As such, instead of choosing a 0 Volts, 0 Volts; 5 Volts, 0 Volts; or 5 Volts, 5 Volts signal respectively corresponding to input information (0,0); (1,0); or (1,1); the RPSR 190 chooses a 0 Volts, 5 Volts reference signal for the (0,1) input information/desired memory state. *See id*.

iii. ***Memory Cell Programming Means (claim 1) / Programming Signal Source (claims 9, 12, 30) / Applying a Programming Signal (claims 42, 45)***[27]



Similar to the programming and verification process described above in Section IV(A) with reference to the ’571 patent, Mehrotra likewise describes an iterative program and verify process where each iteration includes a programming pulse, provided through the Program Circuit 210, followed by a verification process, managed by the Compare Circuit 200, to determine if the memory cell is in the desired memory state. *See* Ex. 1004 at 3:64-4:5; 18:18-29; 19:26-20:36; Figure

separated from the window borders) defining respective memory states. *See* Ex. 1003 at ¶ 85, Ex. 1004 at 21:27-31.

[27] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

15; *see also* Ex. 1003 at ¶¶ 92-95. More specifically, the Program Circuit 210 applies programming pulses, one at a time, to a memory cell to be programmed. *See* Ex. 1004 at 3:64-4:5; 19:26-20:36; *see also* Ex. 1003 at ¶¶ 92-94.

iv. ***Comparator Means (claim 1) / Comparator (claim 9) / Verifying Device (claim 12) / Control Device (claim 30) / Verifying Whether Said Memory Cell is Programmed to the State Indicated by Said Information (claim 42) / Detecting a Parameter Indicating the State of the Memory Cell (claim 42) / Controlling the application of said programming signal (claim 45)***[28]

After each pulse, the Compare Circuit 200 of Mehrotra verifies whether the memory is correctly programmed to its desired memory state. *See id*. When the Compare Circuit 200 verifies that the memory cell is correctly programmed, it outputs a control signal on line 731 to the Program Circuit 210 indicating that the memory cell has been correctly programmed. *See id*. Such a control signal causes the Program Circuit 210 to inhibit further programming, which ends cell programming. *See id*. Conversely, if the Compare Circuit 200 determines that the memory cell is not yet correctly programmed, *i.e.*, not programmed to its desired memory state, then the iterative programming pulse/verify process continues until the memory cell is correctly programmed. *See id*.

v. ***Mehrotra renders obvious digital and analog implementations of the verification elements of the ’571 patent claims***

[28] One form of these claim elements appears in each of the Challenged Claims, and the discussion in this Section is applicable to each.

To the extent that the embodiment in Figure 5 of Mehrotra discloses a digital implementation (*e.g.*, a digital verify process through the Compare Circuit 200) and the Challenged Claims are construed to require an analog implementation, it would have been obvious to one of ordinary skill in the art to implement an analog version of Mehrotra. *See* Ex. 1003 at ¶¶ 98-104. For example, one of ordinary skill in the art would have looked to Mehrotra's description of an analog signal comparison in the sense amplifiers used in the memory cell reading process for motivation to implement an analog comparison with the Compare Circuit 200. *See* Ex. 1004 at 11:20-12:20; *see also* Ex. 1003 at ¶ 98. In addition, analog voltage comparison circuits for memory devices were generally well known in the art at the effective filing date of the '571 patent as shown, for example, in the Kokubun reference. *See* Ex. 1005 at 1:10-20, 4:55-5:43; Ex. 1003 at ¶¶ 59, 63, 98-102.

In addition, one of ordinary skill in the art would have been motivated to implement an analog version of the Mehrotra comparison process to, for example, reduce switching noise often associated with high-speed digital comparators, minimize the use of complex digital circuitry (and associated cost and comparatively large die size for such circuitry), and/or reduce power supply bounce that would otherwise be inherent challenges when implementing a low-noise digital comparator in a memory device. *See, e.g.*, Ex. 1006 at 2:23-54, Figure 3; Ex. 1003 at ¶¶ 59, 64, 98-102. For example, reducing noise improves the performance and reliability

of the memory device, and reducing the complexity and/or size of the devices improves the manufacturability and/or cost of the device. *See id*.

As Mehrotra is also directed to providing reliable, accurate, low-cost and easy to manufacture memory devices, one of ordinary skill in the art would look to readily known and available technologies to achieve these goals, including implementing an analog program/verify comparison process. *See, e.g.*, Ex. 1004 at 2:26-44; *see also* Ex. 1003 at ¶¶ 98-102.

Such an analog implementation in Mehrotra can be explained with reference to Figure 5 reproduced above in this Section. For example, the data path 105 from the Addressable EEPROM Array 60, which includes the memory cells, can convey the bit line signal from a given memory cell directly to a first input of the analog comparator (*e.g.*, Compare Circuit 200). *See* Ex. 1003 at ¶¶ 103-104. This bit line signal would represent the current memory state of the memory cell, similar to the "Y" input to Comparator 202 in Figure 8 of the '571 patent. *See id*.

The second input to the analog comparator would be fed by a device that functions similarly to the RPLSR 190 device in that such a device would select and supply a signal representing the desired memory state of the memory cell, *e.g.*, representing the "LOAD PGM DATA IN" input information provided to the RPLSR 190. *See* Ex. 1004 at Figure 5, 8:24-27; *see also* Ex. 1003 at ¶¶ 98-104. This second input is comparable to the "X" input to Analog Comparator 202 in Figure 8 of

the ’571 patent. *See* Ex. 1003 at ¶ 104. The output of the analog comparator would remain connected to the Program Circuit 210, and the program/verify process described by Mehrotra would otherwise operate in a similar manner.[29] *See id*.

As explained in greater detail in the following Claim Chart II, the features of the Challenged Claims of the ’571 patent are rendered obvious by Mehrotra, and thus, unpatentable under 35 U.S.C. § 103. *See* Ex. 1003 at ¶ 105.

[1a] A multi-level memory device comprising:	Mehrotra discloses a multi-level memory device. “Improvements in the circuits and techniques for read, write and erase of EEprom memory enable non-volatile multi-state memory to operate with enhanced performance over an extended period of time.” Mehrotra, Ex. 1004 at Abstract “Thus, for a multi-state EEprom memory cell, each cell stores two or more bits of data. The information that a given EEprom array can store is thus increased by the multiple of number of states that each cell can store.” *Id.* at 2:14-18. “These and additional objects are accomplished by improvements in EEprom array read and write circuits and techniques in order to provide multiple threshold levels that allow accurate reading and writing of more than two distinct states within

[29] Mehrotra describes that either serial or parallel memory cell reading process can be used in the programming and verification process. *See, e.g.*, Ex. 1004 at 19:1-20:51. The serial or parallel processing approach can readily be implemented through and is entirely consistent with an analog verification implementation, *e.g.*, through a multi-input analog comparator, which was well known at the effective filing date of the ’571 patent. *See* Ex. 1003 at ¶ 104 and footnote 25.

	each memory cell over an extended lifetime of the memory cells, so that more than one bit may be reliably stored in each cell." *Id.* at 2:51-57. "FIG. 7A illustrates the 4-state case where the threshold voltage window is partitioned into four regions 351, 353, 355, 357 by breakpoint levels 352, 354, 356 respectively. The cell is considered to be in state "3" or "2" or "1" or "0" if its V_{T1} is programmed to be within corresponding regions 351 or 353 or 355 or 357 respectively. A 4-state cell is able to store two bits of data. Thus, the four states may be encoded as (1,1), (1,0), (0,1) and (0,0) respectively." *Id.* at 9:24-32. *See also* Ex. 1003 at ¶¶ 81-82.
[1b] an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and K^n >2;	Mehrotra discloses an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and K^n >2. "Improvements in the circuits and techniques for read, write and erase of EEprom memory enable non-volatile multi-state memory to operate with enhanced performance over an extended period of time." Mehrotra, Ex. 1004 at Abstract. "Thus, for a multi-state EEprom memory cell, each cell stores two or more bits of data." *Id.* at 2:14-18. "The floating gate can hold a range of charge and therefore an Eprom memory cell can be programmed to any threshold level within a threshold window. The size of the threshold window, delimited by the minimum and maximum threshold levels of the device, depends on the device's characteristics, operating conditions and history. Each distinct threshold level within the window may, in principle, be used to designate a definite memory state of the cell." *Id.* at 1:30-39. "FIG. 7A illustrates the 4-state case where the threshold voltage window is partitioned into four regions 351, 353, 355, 357

	by breakpoint levels 352, 354, 356 respectively. The cell is considered to be in state "3" or "2" or "1" or "0" if its V_{T1} is programmed to be within corresponding regions 351 or 353 or 355 or 357 respectively. A 4-state cell is able to store two bits of data. Thus, the four states may be encoded as (1,1), (1,0), (0,1) and (0,0) respectively." *Id.* at 9:24-32. *See also id*. at Fig. 7A, Ex. 1003 at ¶¶ 81-86.
[1c] memory cell programming means for programming said multi-level memory cell in accordance with said input information;	Mehrotra discloses memory cell programming means for programming said multi-level memory cell in accordance with said input information. "According to another aspect of the present invention, where a programmed state is obtained by repetitive steps of programming and verifying from the "erased" state, a circuit verifies the programmed state after each programming step with the intended state and selectively inhibits further programming of any cells in the chunk that have been verified to have been programmed correctly. This enables efficient parallel programming of a chunk of data in a multi-state implementation." Mehrotra, Ex. 1004 at 3:64-4:5. "In FIG. 15(5), the N*L read bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200. In FIG. 15(6), if any read bit fails to compare with the program data bit, a further programming voltage pulse from the program circuit 210 is applied simultaneously to the chunk of cells. . . . Programming and verification are repeated until all the cells are correctly verified . . . ." *Id*. at 20:4-16. "A typical erase/program cycle begins with erase which reduces the threshold voltage of the cell to its Erase state level 345. Subsequent repetitive programming is used to increase the threshold voltage V_{T1} to the desired level. Rather than continuously applying programming voltages to the addressed cell for some fixed period of time corresponding to the state to which the cell is to be programmed, it is preferable to apply programming voltages in repetitive short pulses with a read operation occurring after each pulse to determine when it has been programmed to the desired . . . level, at which time the

	programming terminates. The programming voltages and duration of the pulses are such that the pulses advance V_{T1} across the various regions rapidly but each pulse is sufficiently fine to not overshoot any of the regions." *Id*. at 9:6-22. "As mentioned before, programming of an EEprom cell to a desired state is preferably performed in small steps starting from the "erase" state. After each programming step, the cell under programming is read to verify if the desired state has been reached. If it has not, further programming and verifying will be repeated until it is so verified." *Id*. at 18:62-68. "The program circuit 210 comprises N program with inhibit modules such as 801, 803. As illustrated in Table 1 and 2, in order to program the N cells, a voltage V_{PD} must be applied to each of the N cells' drain and a voltage V_{PG} applied to the control gates. . . . Since the signal in line 731 is from the output of the cell compare module 701 shown in FIG. 16, it follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a programming pulse is applied, it is only applied to those cells which have not yet reached their intended states. This selective programming feature is especially necessary in implementing . . . on chip verification in the multi-state case." *Id*. at 20:53-21:7. *See also id*. at 1:30-39, 6:49-51, and Ex. 1003 at ¶¶ 92-97.
[1d] reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined	Mehrotra discloses a reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states. "FIG. 7A illustrates the 4-state case where the threshold voltage window is partitioned into four regions 351, 353, 355, 357 by breakpoint levels 352, 354, 356 respectively. The cell is considered to be in state "3" or "2" or "1" or "0" if its V_{T1} is programmed to be within corresponding regions 351 or 353 or 355 or 357 respectively. A 4-state cell is able to store two bits of data. Thus, the four states may be encoded as (1,1), (1,0), (0,1) and (0,0) respectively." Mehrotra, Ex. 1004 at 9:24-32.

memory states; and	"In the meantime, if the operation is programming, the data is staged for programming the addressed cell by being sent via a serial data line 259 to a set of read/program latches and shift registers 190." *Id.* at 8:24-27. "[P]rogramming is under the control of the controller 140. The data to be programmed into the sector is sent chunk by chunk. The controller first sends a first chunk of N*L serial data bits together with addresses, control and timing information to the EEprom chip 130. L is the number of binary bits encoded per memory cell. For example, L=1 for a 2-state cell, and L=2 for a 4-state cell. Thus if N=64 and L=2, the chunk of data bits will be 128 bits wide. The N*L data bits are stored in latches and shift registers 190 where the serial bits are converted to N*L parallel bits. These data will be required for program verify in conjunction with the read circuits 220, bit decoder 230, compare circuit 200 and the program circuit with inhibit 210. "The program algorithm for a chunk of N cells is best described by referring to . . . FIG. 5 and FIGS. 15(1)-15(7) which illustrate the algorithm itself. . . . This is followed in FIG. 15(2) by programming the sector local reference cells (as shown in FIGS. 11(1)-(3)). In FIG. 15(3), the N*L bits of parallel data is latched in latches 190. In FIG. 15(4), the read circuits 220 access the N-channel data path 105 to read the states in the N chunk of cells. The read algorithm has already been described in conjunction with FIG. 12B or FIG. 13D. The N-cell reads generates N*K (K=number of states per cell) output states. These are decoded by bit decoder 230 into N*L binary bits. In FIG. 15(5), the N*L read bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200. In FIG. 15(6), if any read bit fails to compare with the program data bit, a further programming voltage pulse from the program circuit 210 is applied simultaneously to the chunk of cells." *Id*. at 19:42-20:10. *See also* Ex. 1003 at ¶¶ 83-85, 93, 96-97, 104.
[1e] comparator	Mehrotra discloses a comparator means for comparing a voltage of said multi-level memory cell with the selected reference

means for comparing a voltage of said multi-level memory cell with the selected reference voltage,	voltage. "In FIG. 15(5), the N*L read bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200. In FIG. 15(6), if any read bit fails to compare with the program data bit, a further programming voltage pulse from the program circuit 210 is applied simultaneously to the chunk of cells. However, an inhibit circuit within the program circuit 210 selectively blocks programming to those cells whose bits are correctly verified with the programmed data bits. Thus, only the unverified cells are programmed each time. Programming and verification are repeated until all the cells are correctly verified in FIG. 15(7)." Mehrotra, Ex. 1004 at 20:4-16. "FIG. 16 shows one embodiment of the compare circuit 200 of FIG. 5 in more detail. The circuit 200 comprises N cell compare modules such as 701, 703, one for each of the N cells in the chunk. In each cell compare module such as the module 701, the L read bits (L=number of binary bits encoded for each cell) are compared bit by bit with the corresponding program data bits. This is performed by L XOR gates such as 711, 713, 715. The output of these XOR gates pass through an NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the L bits are verified, and a "0" appears when otherwise. When the control signal VERIFY is true, this result is latched to a latch 721 such that the same result at the output of NOR gate 717 is available at the cell compare module's output 725. The compare circuit 200 performs the comparisons of L bits in parallel. The N compare module's outputs such as 725, 727 are available at an N-channel output line 731 to be fed to the program circuit with inhibit 210." *Id.* at 20:17-36. "According to another aspect of the present invention, where a programmed state is obtained by repetitive steps of programming and verifying from the "erased" state, a circuit verifies the programmed state after each programming step with the intended state and selectively inhibits further programming of any cells in the chunk that have been verified to have been programmed correctly." *Id*. at 3:64-4:4.

	"The read circuits and operation described are also employed in the programming and erasing of the memory cells, particularly in the verifying part of the operation. As described previously, programming is performed in small steps, with reading of the state programmed in between to verify if the desired state has been reached. As soon as the programmed state is verified correctly, programming stops." *Id*. at 18:18-25. "The memory state of a cell may be determined by measuring the threshold voltage V_{T1} . . . ." *Id*. at 10:30-32. *See also id.* at Fig. 5 (Compare Circuit 200), Ex. 1003 at ¶¶ 92-104.
[1f] said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.	Mehrotra discloses said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information. "[W]here a programmed state is obtained by repetitive steps of programming and verifying from the "erased" state, **a circuit verifies the programmed state** after each programming step with the intended state **and selectively inhibits further programming of any cells in the chunk that have been verified to have been programmed correctly**. This enables efficient parallel programming of a chunk of data in a multi-state implementation." Mehrotra, Ex. 1004 at 3:64-4:5 (emphasis added). "The read circuits and operation described are also employed in the programming and erasing of the memory cells, particularly in the verifying part of the operation. As described previously, programming is performed in small steps, with reading of the state programmed in between to verify if the desired state has been reached. As soon as the programmed state is verified correctly, programming stops." *Id*. at 18:18-25. "In FIG. 15(5), the N*L read bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200. In FIG. 15(6), if any read bit fails to compare with the program data bit, a further programming voltage pulse from the program circuit 210 is applied simultaneously to the chunk

	of cells. However, an inhibit circuit within the program circuit 210 selectively blocks programming to those cells whose bits are correctly verified with the programmed data bits. Thus, only the unverified cells are programmed each time. Programming and verification are repeated until all the cells are correctly verified in FIG. 15(7)." *Id.* at 20:4-16. "The circuit 200 comprises N cell compare modules such as 701, 703, one for each of the N cells in the chunk. In each cell compare module such as the module 701, the L read bits (L=number of binary bits encoded for each cell) are compared bit by bit with the corresponding program data bits. This is performed by L XOR gates such as 711, 713, 715. The output of these XOR gates pass through an NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the L bits are verified, and a "0" appears when otherwise. When the control signal VERIFY is true, this result is latched to a latch 721 such that the same result at the output of NOR gate 717 is available at the cell compare module's output 725. The compare circuit 200 performs the comparisons of L bits in parallel. **The N compare module's outputs such as 725, 727 are available at an N-channel output line 731 to be fed to the program circuit with inhibit 210 of FIG. 5.**" *Id.* at 20:17-36 (emphasis added). "The program circuit 210 comprises N program with inhibit modules such as 801, 803. As illustrated in Table 1 and 2, in order to program the N cells, a voltage V_{PD} must be applied to each of the N cells' drain and a voltage V_{PD} applied to the control gates. Each program module such as 801 serves to selectively pass V_{PD} on a line 805 to one of the drains through the one of the N-channel data path 105. . . . **Since the signal in line 731 is from the output of the cell compare module 701 shown in FIG. 16, it follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a programming pulse is applied, it is only applied to those cells which have not yet reached their intended states**. This selective programming feature is especially necessary in implementing parallel programming and on chip verification in the multi-state case." *Id.* at 20:52-21:8

	(emphasis added). *See also* Ex. 1003 at ¶¶ 92-104.

The following Claim Chart III includes citations to each of Kitamura and Mehrotra for claims 9, 10, 12, 30, 32, 42 and 45 of the '571 patent. References to claim element citations for Kitamura are to Chart I in Section V(A) above, and references to claim element citations for Mehrotra are to Chart II in Section V(B).

[9a] Multi-level memory apparatus, comprising:	Kitamura and Mehrotra each discloses a multi-level memory apparatus. Kitamura: *See* Chart I, element 1a. Mehrotra: *See* Chart II, element 1a.
[9b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura and Mehrotra each discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b. Mehrotra: *See* Chart II, element 1b.
[9c] a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Mehrotra each discloses a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Mehrotra: *See* Chart II, element 1d.
[9d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura and Mehrotra each discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c. Mehrotra: *See* Chart II, element 1c.

[9e] a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.	Kitamura and Mehrotra each discloses a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information. Kitamura: *See* Chart I, element 1e. Mehrotra: *See* Chart II, element 1e.
[10] Apparatus according to claim 9, wherein said comparator compares a bit line signal of said memory cell with the selected reference signal.	Kitamura discloses that said comparator compares a bit line signal of said memory cell with the selected reference signal. "Since the floating gate MOS transistor 1 and the MOS transistor 2 constitute a ratio circuit with the load circuit 3, when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3. Meanwhile, the two-bit input digital signals B0 and B1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2." Ex. 1010 at ¶ [09]. "[A] D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; **a circuit that compares a read level from a memory cell to the level of the analog signal**, and ends a write operation according to this result . . . ." *Id*. at ¶ [06] (emphasis added). *See* Ex. 1010 at Fig. 1; Ex. 1003 at ¶¶ 65-70, 72-73.
[12a] Multi-level memory	Kitamura and Mehrotra each discloses a multi-level

apparatus, comprising:	memory apparatus. Kitamura: *See* Chart I, element 1a. Mehrotra: *See* Chart II, element 1a.
[12b] an electrically alterable non-volatile memory cell having more than two predetermined memory states;	Kitamura and Mehrotra each discloses an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, element 1b. Mehrotra: *See* Chart II, element 1b.
[12c] a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Mehrotra each discloses a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Mehrotra: *See* Chart II, element 1d.
[12d] a programming signal source which applies a programming signal to said memory cell; and	Kitamura and Mehrotra each discloses a programming signal source which applies a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c. Mehrotra: *See* Chart II, element 1c.
[12e] a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.	Kitamura and Mehrotra each discloses a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f. Mehrotra: *See* Chart II, elements 1e, 1f.
[30a] Apparatus for programming an electrically alterable non-volatile memory cell having more than two	Kitamura and Mehrotra each discloses an apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states.

predetermined memory states, comprising:	Kitamura: *See* Chart I, elements 1a, 1b. Mehrotra: *See* Chart II, elements 1a, 1b.
[30b] a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Mehrotra each discloses a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d. Mehrotra: *See* Chart II, element 1d.
[30c] a programming signal source to apply a programming signal to said memory cell; and	Kitamura and Mehrotra each discloses a programming signal source to apply a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c. Mehrotra: *See* Chart II, element 1c.
[30d] a control device to control the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura and Mehrotra each discloses a control device to control the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f. Mehrotra: *See* Chart II, elements 1e, 1f.
[32] Apparatus according to claim 30, wherein said control device is constructed to compare a signal corresponding to the state of said memory cell with the selected reference signal, and to control the application of said programming signal to said memory cell based on a result of the comparison.	Mehrotra discloses that said control device is constructed to compare a signal corresponding to the state of said memory cell with the selected reference signal, and to control the application of said programming signal to said memory cell based on a result of the comparison. Mehrotra: *See* Chart II, elements 1e, 1f. *See* Ex. 1003 at ¶¶ 92-104.
[42a] A method of programming an electrically alterable non-volatile memory cell	Kitamura and Mehrotra each discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined

having more than two predetermined memory states, said method comprising:	memory states. Kitamura: *See* Chart I, elements 1a, 1b and corresponding described methods. Mehrotra: *See* Chart II, elements 1a, 1b and corresponding described methods.
[42b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Mehrotra each discloses selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. Mehrotra: *See* Chart II, element 1d and corresponding described method.
[42c] applying a programming signal to said memory cell;	Kitamura and Mehrotra each discloses applying a programming signal to said memory cell. Kitamura: *See* Chart I, element 1c and corresponding described method. Mehrotra: *See* Chart II, element 1c and corresponding described method.
[42d] detecting a parameter indicating the state of said memory cell; and	Kitamura and Mehrotra each discloses detecting a parameter indicating the state of said memory cell. Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods. Mehrotra: *See* Chart II, elements 1e, 1f and corresponding described methods.
[42e] verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.	Mehrotra discloses verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. Kitamura: *See* Chart I, elements 1e, 1f and corresponding described methods. Mehrotra: *See* Chart II, elements 1e, 1f and corresponding described methods.

[45a] A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:	Kitamura and Mehrotra each discloses a method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states. Kitamura: *See* Chart I, elements 1a, 1b and 1c and corresponding described methods. Mehtotra: *See* Chart II, elements 1a, 1b, and 1c and corresponding described methods.
[45b] selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;	Kitamura and Mehrotra each discloses selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell. Kitamura: *See* Chart I, element 1d and corresponding described method. Mehrotra: *See* Chart II, element 1d and corresponding described method.
[45c] applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal.	Kitamura and Mehrotra each discloses applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal. Kitamura: *See* Chart I, elements 1c, 1e and 1f and corresponding described methods. Mehrotra: *See* Chart II, elements 1c, 1e and 1f and corresponding described method.

VI. MEANINGFUL BENEFIT TO INSTITUTING ON BOTH GROUNDS

Petitioner respectfully submits that the Board should institute IPR on both Grounds 1 and 2 because of the meaningful benefit from doing so. For example,

Kitamura describes that when the memory cell is verified to be correctly programmed no additional programming pulses are applied. *See* Ex. 1010 at ¶ [09]. This management of program pulses is similar to that disclosed in the ’571 patent. *See* Ex. 1001 at 9:3-7. Mehrotra, on the other hand, describes that even after a memory cell is verified to be correctly programmed, programming pulses can continue. *See* Ex. 1004 at 20:7-14. However, Mehrotra further describes that these post-verification programming pulses are blocked (*e.g.*, inhibited from having effect on the cell).[30] *See id*.

As compared with Kitamura, Mehrotra has a more robust description concerning the iterative program and verify processes along with more detailed figures (and attendant discussions) (*see* Figs. 7A and 7B) illustrating the relationship between the multiple memory states and the reference signals/voltages. As compared with using additional references (*e.g.*, Lee and/or Kokubon) to illustrate the analog verification process made obvious by Mehrotra, Kitamura explicitly describes such an analog implementation.

Additionally, as Mehrotra is 102(e) prior art it is possible that the ’571 patent owner may attempt to swear behind Mehrotra by, for example, demonstrating conception of the ’571 patent invention prior to the Mehrotra priority date, and

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[30] Mehrotra’s program inhibiting features are similar to how the ’571 patent owner interprets the claims in its infringement contentions. *See* Ex. 1011 at pages 3-5.

showing diligence from conception of the '571 invention to the filing date of the application that issued as the '571 patent. Because Kitamura is a 102(b) reference, the '571 patent owner cannot swear behind it so Kitamura is arguably superior in this respect. Lastly, Grounds 1 and 2 include non-overlapping challenged claims.

In sum, the two grounds presented in this petitions do not impede "the just, speedy and inexpensive resolution of [this] proceeding" as required by 37 C.F.R. § 42.1(b). For at least the above reasons, Petitioner respectfully requests that the Board institute rejections on both grounds presented in this Petition as each of Grounds 1 and 2 have meaningful benefits (and differences) relative to each other for purposes of challenging the Challenged Claims.

VII. CONCLUSION

The cited prior art references identified in this Petition contain pertinent technological teachings (both cited and uncited), either explicitly or inherently disclosed, at least some of which were not previously considered in the manner presented herein, or relied upon on the record during original examination of the '571 patent. In sum, these references provide non-cumulative technological teachings which indicate a reasonable likelihood of success as to Petitioner's assertion that the Challenged Claims of the '571 patent are not patentable pursuant to the grounds presented in this Petition. Accordingly, Petitioner respectfully requests institution of an IPR for those claims of the '571 patent for each ground herein.

Respectfully submitted,

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(Trial No. IPR2015-00504)

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(1) and 42.205(a), the undersigned certifies that on December 24, 2014, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via FedEx to the Patent Owner by serving the correspondence address of record as follows:

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