IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Braceras *et al.*:	
U.S. Patent No. 6,967,861	Petition for *Inter Partes* Review
Issued: November 22, 2005	
Title: METHOD AND APPARATUS FOR IMPROVING CYCLE TIME IN A QUAD DATA RATE SRAM DEVICE	Attorney Docket No.: 351479-15.861
	Customer No.: 26379
	Real Party-in-Interest: GSI Technology, Inc.

PETITION FOR *INTER PARTES* REVIEW

Mail Stop Patent Board
Patent Trial and Appeal Board
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the provisions of 35 U.S.C. § 311 and 37 C.F.R. § 42.100, GSI Technology, Inc. ("Petitioner") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-3, 9-11, 17-20, 26-28 and 34 of United States Patent No. 6,967,861 (the "'861 patent").

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EXHIBIT LIST

Exhibit Number	**Description**
GSI-1001	U.S. Patent No. 6,967,861
GSI-1002	File History for U.S. Patent No. 6,967,861
GSI-1003	U.S. Patent No. 7,162,657 to Takahashi ("Takahashi")
GSI-1004	Japanese Patent Application Kokai No. 2000-173270 to Okuyama ("Okuyama")
GSI-1005	U.S. Patent No. 6,647,478 to Tsuchida ("Tsuchida")
GSI-1006	Declaration of R. Jacob Baker
GSI-1007	Certified English Translation of Japanese Patent Application Kokai No. 2000-173270 to Okuyama ("Okuyama")

I. MANDATORY NOTICES

A. Real Party-in-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), GSI Technology, Inc. ("Petitioner") is the real party-in-interest for this petition.

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), the '861 patent is presently the subject of a patent infringement lawsuit brought by the assignee, Cypress Semiconductor Corporation, which may affect or be affected by a decision in this proceeding: *Cypress Semiconductor Corp. v. GSI Technology, Inc.*, N.D. Cal., Case Nos. 3:13-cv-02013-JST (JCS) and 4:13-cv-03757-JST (JCS).

As of the filing of this petition, no other judicial or administrative matters are known to Petitioner that would affect, or be affected by, a decision in an *inter partes* review of the '861 patent.

C. Lead and Back-up Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3) and 42.10(a), Petitioner provides the following designation of counsel.

Lead Counsel	Back-up Counsel
Timothy W. Lohse	Kevin C. Hamilton
DLA PIPER LLP (US)	DLA PIPER LLP (US)
2000 University Avenue	401 B Street, Suite 1700

East Palo Alto, CA 94303 Phone: (650) 833-2055 Fax: (650) 687-1183 timothy.lohse@dlapiper.com USPTO Customer No. 26379 USPTO Reg. No. 35,255	San Diego, CA 92101 Phone: (619) 699-2634 Fax: (619) 764-6633 kevin.hamilton@dlapiper.com USPTO Customer No. 26379 USPTO Reg. No. 67,593

D. Service Information

Pursuant to 37 C.F.R. § 42.8(b)(4), papers concerning this matter should be served on either Timothy Lohse or Kevin Hamilton identified above and copying, as appropriate, the following email address: GSI-DLA-Team@dlapiper.com.

II. GROUNDS FOR STANDING

Pursuant to 37 C.F.R. § 42.104(a), Petitioner hereby certifies that the '861 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review challenging the claims of the '861 patent on the grounds identified herein.

III. RELIEF REQUESTED

Petitioner asks that the Board review the accompanying prior art and analysis, institute a trial for *inter partes* review of claims 1-3, 9-11, 17-20, 26-28 and 34 of the '861 patent, and cancel claims 1-3, 9-11, 17-20, 26-28 and 34 as invalid for the reasons set forth below.

IV. THE REASONS FOR THE REQUESTED RELIEF

A. Summary of Reasons

The ’861 patent relates to a method and apparatus for improving cycle time in a Quad Data Rate SRAM device in which a self-timed, read to write operation in the SRAM is implemented. GSI-1001 at Title, Abstract. The ’861 patent was issued on a first office action allowance without any prior art rejections. GSI-1002 at Notice of Allowance. In the specification, the patentee emphasizes the aspect that achieves the improvement in the cycle time as: “Briefly stated, an improvement in the cycle time is achieved by implementing a self-timed read to write protocol in which write addresses and data are captured and buffered during a given read to write cycle are actually written in the next read to write cycle. **As such, the write operation (of data and address captured in the previous cycle) may be timed immediately after the read operation of the current cycle**.” GSI-1001 at 3:24-32 (emphasis added). However, as set forth below, this feature, as well as others claimed in the ’861 patent, were well known in the art long before the ’861 patent was filed.

B. The ’861 Patent

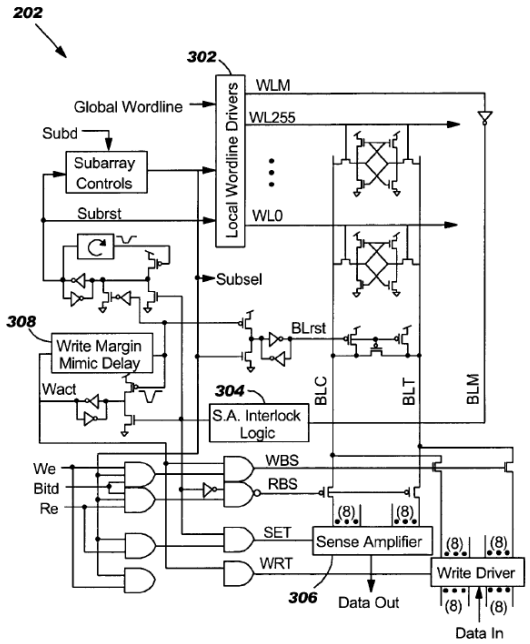
1. Overview

The ’861 patent, entitled “METHOD AND APPARATUS FOR IMPROVING CYCLE TIME IN A QUAD DATA RATE SRAM DEVICE,” issued on November 22, 2005, from an application filed on February 27, 2004, by

named inventors George Braceras and Harold Pilo. The ’861 patent does not claim priority to any earlier filing.

The ’861 patent discloses read-to-write interlock circuitry 202 (shown in detail in Figure 3, which is reproduced below) that generates control signals to a sense amplifier 306 that senses read data on bit lines from the memory array and a write driver that drives write data into the memory array.

FIG. 3

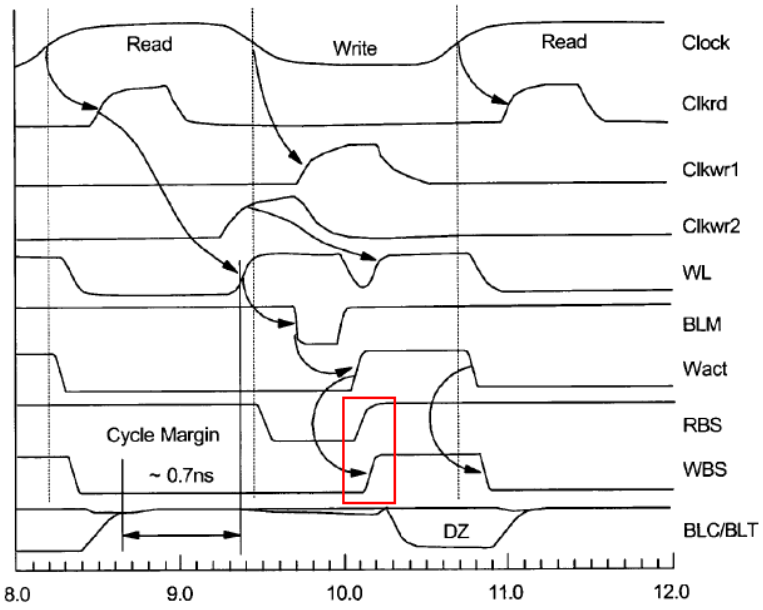


GSI-1001 at Fig. 3.

The read-to-write interlock circuitry 202 generates a control signal (RBS) for a pair of read bit switches to couple the sense amplifier to the bit lines (BLC, BLT) during a read operation and a control signal (WBS) for a pair of write bit switches to couple the write driver to the bit lines during a write operation. *Id.*

Figure 4 of the ’861 patent (reproduced below in annotated form) shows the timing of the read bit switch control signal (RBS) and the write bit switch control signal (WBS) with respect to the timing between the read operation and the write operation. As shown in Figure 4, when the RBS signal goes high (which turns off the read bit switches because those switches are PMOS transistors as shown in Figure 3) the sense amplifier is isolated from the bit lines. Immediately after the sense amplifier is isolated from the bit lines, the write driver may be connected to the bit lines (shown by the WBS signal going high, which turns on the write bit switches because those switches are NMOS transistors as shown in Figure 3) which allows the write data to be written into the memory array using the bit lines. *Id.* at 2:55-65, 3:22-32, 4:50-62, Figs. 3-4. As shown in Figure 4 (annotated with the red box), the RBS signal transitions high (disconnecting the sense amplifier from the bit lines) as soon as the WBS signal transitions high (connecting the write driver to the bit lines) which allows the write operation (indicated by the transition of the WBS signal to high) to be timed immediately after the read operation (indicated by the transition of the RBS signal to high). *Id.*

FIG. 4



2. Prosecution History

The ’861 patent matured from Patent Application No. 10/708,379, which was filed on February 27, 2004. The examiner issued the ’861 patent on a Notice of Allowance mailed on July 20, 2005, without a prior art rejection. GSI-1002 at Notice of Allowance.

In the Notice of Allowance, the examiner indicated that the reasons for allowance were that the prior art identified by the examiner failed to teach the limitation of “wherein said write operation uses a previous write address captured during a preceding clock cycle; and capturing a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle; wherein said

commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle" (independent claims 1 and 9) or "wherein said write operation uses a previous write address captured during a preceding clock cycle; and capturing, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle; wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle" (independent claims 18 and 25). GSI-1002 at Notice of Allowance at 2-3.

C. Identification of Challenges

Petitioner requests *inter partes* review of the '861 patent in view of the following references:

- GSI-1003 U.S. Patent No. 7,162,657 to Takahashi ("Takahashi")
- GSI-1004 Japanese Patent Application Kokai No. 2000-173270 to Okuyama ("Okuyama")
- GSI-1005 U.S. Patent No. 6,647,478 to Tsuchida ("Tsuchida")

1. Challenged Claims

Petitioner requests that claims 1-3, 9-11, 17-20, 26-28 and 34 of the '861 patent be found unpatentable.

2. Statutory Grounds for Challenges

Challenge #1: Claims 1, 9, 18 and 26 are anticipated by Takahashi. The '861 patent's earliest filing date is February 27, 2004. Takahashi was filed August 12, 2003, and published on February 19, 2004, and is prior art to the '861 patent under 35 U.S.C. §§ 102(a) and (e) (pre-AIA). GSI-1003 at cover page.

Challenge #2: Claims 2-3, 10-11, 19-20 and 27-28 are obvious over Takahashi. Takahashi is prior art to the '861 patent as established above.

Challenge #3: Claims 17 and 34 are obvious over Takahashi and Tsuchida. Takahashi is prior art to the '861 patent as established above. Tsuchida was filed June 20, 2002, published on October 31, 2002, and issued on November 11, 2003, and is prior art to the '861 patent under 35 U.S.C. § 102(b) (pre-AIA). GSI-1005 at cover page.

Challenge #4: Claims 1-3, 9-11, 17-20, 26-28 and 34 are obvious over Okuyama alone or in combination with Takahashi or Tsuchida. Okuyama was filed December 4, 1998, and was published on June 23, 2000, and is prior art to the '861 patent under 35 U.S.C. § 102(b) (pre-AIA). GSI-1004 at cover page. Takahashi and Tsuchida are prior art to the '861 patent as established above.

3. Claim Construction

Pursuant to 42 C.F.R. §§ 42.100(b) and 42.204(b)(3), a claim subject to *inter partes* review receives the "broadest reasonable construction in light of the

specification of the patent in which it appears." 42 C.F.R. § 42.100(b). Claim terms are given their ordinary and accustomed meaning as they would be understood by one of ordinary skill in the art, unless the inventor, as a lexicographer, has set forth a special meaning for a term. *Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473, 1477 (Fed. Cir. 1998); *York Prods., Inc. v. Central Tractor Farm & Family Ctr.*, 99 F.3d 1568, 1572 (Fed. Cir. 1996).

In the '861 patent, the inventors did not act as lexicographers and did not provide a special meaning for any of the claim terms. Accordingly, using the broadest reasonable interpretation standard, the terms should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art and consistent with the disclosure. One key term is discussed below:

- *as soon as*: "immediately, without delay." In the '861 patent, the specification discloses that the write operation is timed "immediately after the read operation" and "begin[s] the write operation immediately after the sense amplifier captures the read data." GSI-1001 at 2:55-60, 4:50-62. This is consistent with how one skilled in the art interprets this term. GSI-1006 at ¶ 18. Thus, this construction is consistent with and supported by the patent specification.

The proposed claim construction is presented using the broadest reasonable interpretation standard applied for purposes of *inter partes* review. Petitioner

reserves the right to advocate a different claim interpretation in any other forum in accordance with the claim construction standards applied in such forum.

4. Level of Ordinary Skill in the Art

Petitioner proposes that one of ordinary skill in the art at the time the ’861 patent was filed would have an undergraduate degree in electrical engineering, computer engineering, computer science or physics, and at least two years working in the field of digital semiconductor chip design. GSI-1006 at ¶ 10.

5. Identification of How the Claims Are Unpatentable

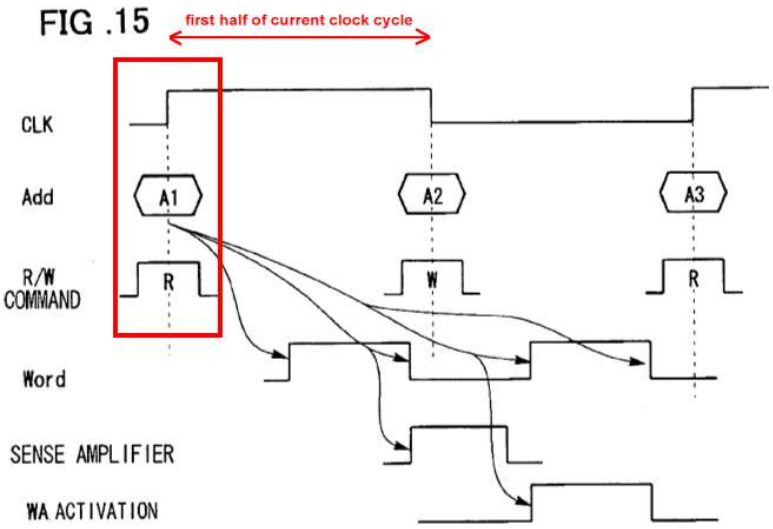
i. **Challenge #1: Takahashi Anticipates Claims 1, 9, 18 and 26**

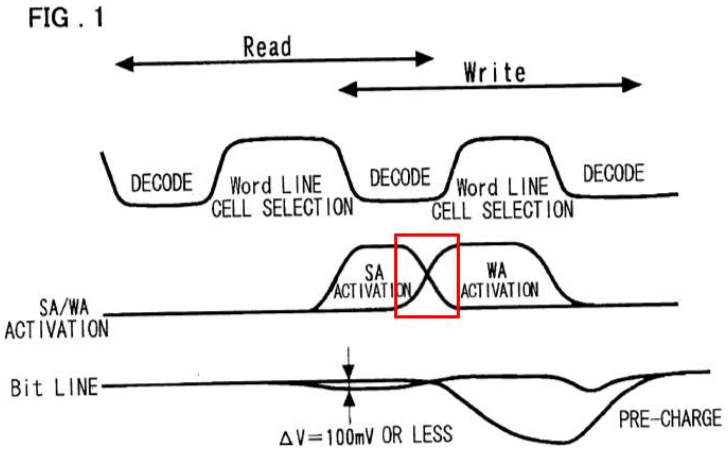
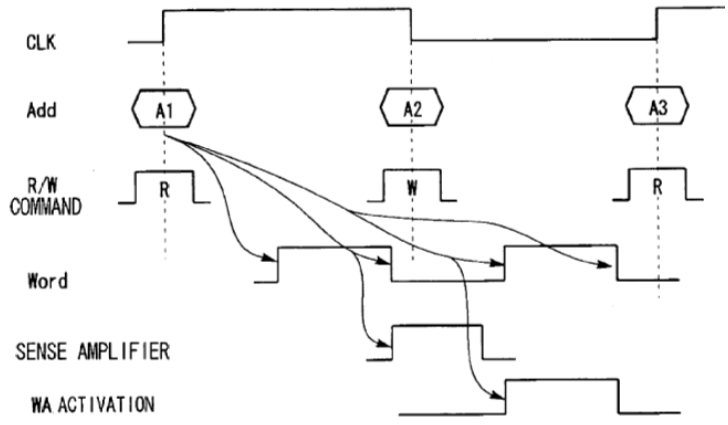
Takahashi anticipates claims 1, 9, 18 and 26 of the ’861 patent under pre-AIA 35 U.S.C. §§ 102(a) and (e). Takahashi discloses the same technology that allegedly is the invention of the ’861 patent. Specifically, Takahashi discloses a self-timed read to write operation in a memory storage device, including capturing a read address during a first half of a current clock cycle and commencing a read operation corresponding to the captured read address. Takahashi discloses commencing a write operation for the current clock cycle so as to cause write data to appear on the pair of bit lines as soon as the read data from the captured read address is amplified by the sense amplifier, wherein the write operation uses a previous write address captured during a preceding clock cycle. These elements

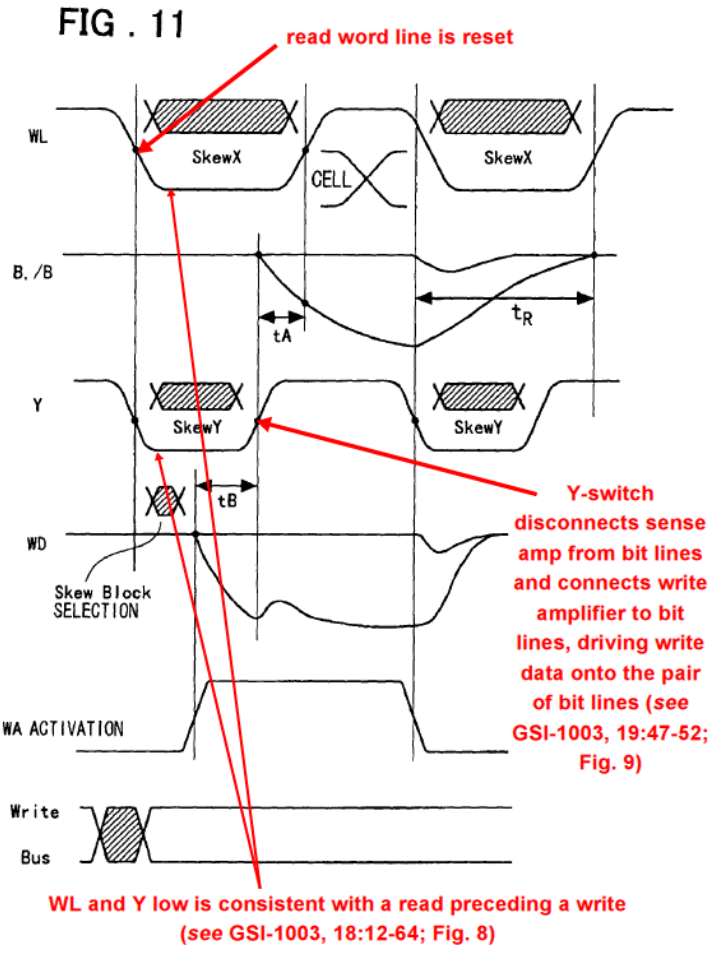
are depicted in Figures 2 and 11 of Takahashi and discussed below in the chart. GSI-1003 at Figs. 2, 11.

Takahashi discloses each limitation recited in claims 1, 9, 18 and 26. The following claim chart demonstrates, on a limitation-by-limitation basis, how Takahashi anticipates claims 1, 9, 18 and 26 of the '861 patent under pre-AIA 35 U.S.C. §§ 102 (a) and (e).

Claim Element	**Disclosure in Takahashi**
[1 preamble] A method for implementing a self-timed, read to write operation in a memory storage device, the method comprising:	Takahashi discloses a method for implementing self-timed (GSI-1003 at 9:28-37), read to write operation (*id.* at 9:28-30) in a memory storage device (*id.* at 9:28). Self-timing is accomplished by "a circuit for controlling the timing so that the sense operation by the sense amplifier in the read cycle and the address decoding operation by the decoder in the write cycle in a cycle next following the read cycle occur in parallel (105, 106, 107 in Fig. 2). This configuration is effective to raise the frequency of the driving clock signals." (*Id.* at 9:28-37). Figure 1 of Takahashi illustrates a read to write operation implemented in a semiconductor storage device. (*Id.* at Fig. 1, 11:3-9).
[1 a] capturing a read address during a first half of a current clock cycle;	Takahashi discloses this step. For example, Figure 15 (annotated in red below) illustrates that the read address A1 is captured on the rising edge of the CLK signal. The rising edge of the CLK signal marks the beginning of the first half of the current clock cycle.

Claim Element	**Disclosure in Takahashi**
	 (GSI-1003 at Fig. 15). Furthermore, Takahashi states that the read address (A1) is sampled on the rising edge of the clock (CLK). (*Id.* at 21:6-13).
[1 b] commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	Takahashi discloses this step. For example, Takahashi states: In the above mentioned circuit configuration, during a read cycle, the voltage appearing on a bit line responsive to data stored in the selected memory cell is amplified by a sense amplifier which composes a read circuit for outputting read data. During a write cycle, a bit line is driven with a (GSI-1003 at 2:34-38, 11:35-41, 11:55-12:11). Takahashi further explains that the captured read address is used to generate X-address, Y-address and block selection address signals. (*Id.* at 1:65-2:11, 12:36-51). The X-address, Y-address and block selection address signals are used to select the memory cell corresponding to the captured read address. (*Id.* at 1:65-2:11, 12:36-51). Figure 8 shows read data corresponding to the captured read address being read onto a pair of bit lines (B and /B). (*Id.* at Fig. 8, 18:30-19:3).
[1 c] commencing a write operation for said current clock cycle so as to cause write data to appear	Takahashi discloses this step. For example, Takahashi discloses minimizing the total read-to-write cycle time by overlapping portions of the read and write cycles. (GSI-1003 at 11:35-41, 14:54-60). Overlapping the read and write cycles

Claim Element	**Disclosure in Takahashi**
on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier,	(shown in the red box annotation of Figure 1 below) enables writing data onto the bit lines as soon as the read data is amplified by the sense amplifier, so the clock period can be reduced to its allowable limit. (*Id*. at 12:19-32, 14:54-60). FIG . 1  (*Id*. at Fig. 1). Takahashi discloses that the read and write operations occur alternately within the current clock cycle. (*Id*. at 9:28-37, 9:53-54, 11:56-12:3). Figure 15 shows that the read to write operation illustrated in Figure 1 occurs in the current clock cycle. FIG .15  (*Id*. at Fig. 15). Takahashi discloses that in a read-to-write operation, there is no need to precharge the bit line pair after the read data is captured by the sense amplifier, and that write data can be

Claim Element	**Disclosure in Takahashi**
	driven onto the bit lines as soon as the read data sense operation is complete. (*Id*. at 12:19-32). Figure 11 (annotated in red below) shows that after sensing read data on a bit line pair using a sense amplifier, instead of precharging the bit lines after sensing the read data, the read word line is reset, a Y-switch disconnects the sense amplifier from the bit lines, and the write data is driven onto the pair of bit lines. (*Id*.).  (*Id*. at Fig. 11).

The ’861 patent was filed more than 6 months after Takahashi was filed. Like Takahashi, the ’861 patent specification explains that after sensing read data on a bit line pair using a sense amplifier, write data can be driven onto the bit lines

as soon as the read data is amplified by the sense amplifier because there is no need to precharge the bit line pair before writing the data. GSI-1001 at 5:5-10. Instead of precharging the bit lines after sensing the read data, the read word line is reset, the read bit switch is disabled to disconnect the sense amplifier from the bit lines, and the write data is driven onto the pair of bit lines. *Id*. This is the same operation disclosed in Takahashi. *See* step [1 c] above. The similarities of Takahashi (left below) and ’861 patent (right below) disclosures are shown below.

In the present embodiment, the signal amplitude on the bit line is reduced (the differential voltage ΔV of the bit line pair during read is usually 100 mV or less on the line Bit of FIG. **1**), such that there is no necessity of providing a pre-charge period on the bit line after reading. It is because the amplitude of the signal to be written during the next write cycle is large as compared to the differential voltage ΔV appearing on the bit line pair and hence the write operation on the bit line is possible even if no pre-charging is performed. That is, memory cell selection and write amplifier activation may be effected so that the write data on the bit line will be presented during the period when the bit line is to be pre-charged after the sense amplifier SA is activated to read the data.

data (DZ) onto the bit line pair. There is no need to precharge the bit line pair once the read data is captured by the sense amplifier BL restore after the read operation; as can be seen in FIG. **4**, once the read word line signal is reset and the read bit switches are disabled (RBS goes high), the bit line pair is driven by write data. Finally, after the execution of the

Takahashi (GSI-1003 at 12:19-32) **’861 patent (GSI-1001 at 5:5-10)**

Likewise, the figures of Takahashi and the ’861 patent show similar circuits for writing data onto the bit lines as soon as the read data is amplified by a sense amplifier. Figure 9 of Takahashi (left below) shows the read word line signal (WL, one of many, in red box annotations), the Y-switches (transistors controlled by Y signal in green box annotations) and the bit line pair (B, /B) in blue box annotations. Figure 3 of the ’861 patent (right below) shows the corresponding read word line signal (one of WL0 … WL255) in red box annotations, read and

write bit switches (transistors controlled by RBS and WBS) in green box annotations and the bit line pair (BLC and BLT) in blue box annotations. In each disclosure, these are the circuit elements that implement the read to write operation in which the write data is driven onto the bit lines as soon as the read data has been amplified by the sense amplifier.

FIG . 9

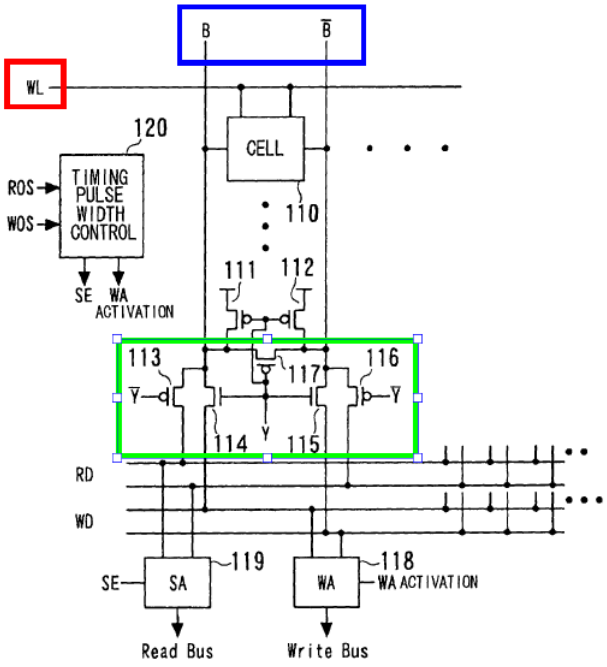
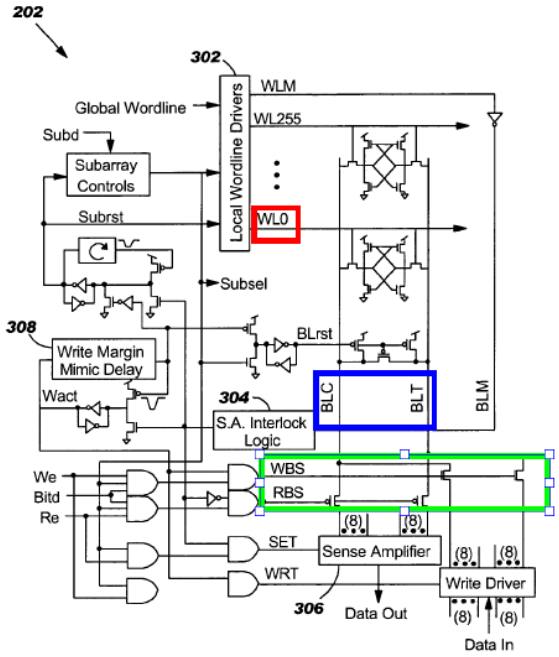
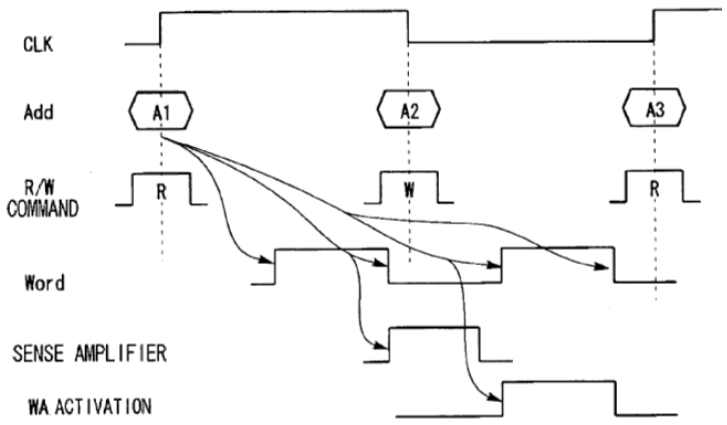


FIG. 3



Takahashi (GSI-1003) at Fig. 9 **'861 patent (GSI-1001) at Fig. 3**

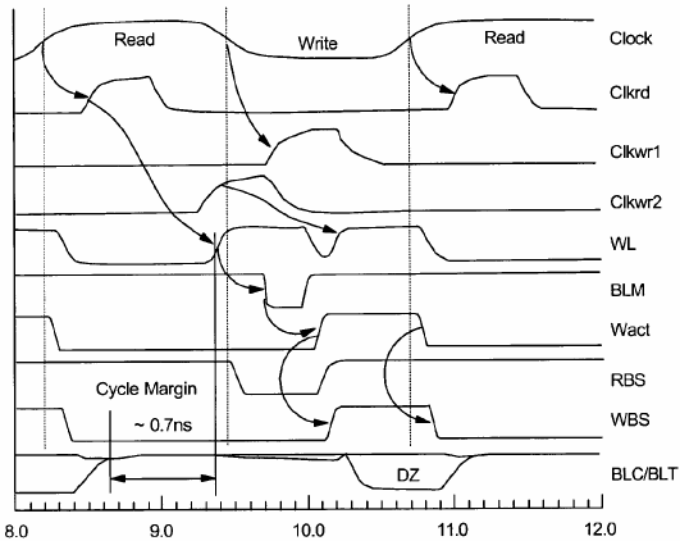
Claim Element	**Disclosure in Takahashi**
[1 d] wherein said write operation uses a previous write address captured during a	Takahashi discloses this step. For example, Takahashi states that in the write operation for the current clock cycle, the write address is decoded and the write amplifier is activated using only the rising edge of the clock signal. (GSI-1003 at 21:6-17). In Figure 15 below, the first and second pulses of the word line (read and write pulses of the Word signal, respectively) illustrate that the read and write addresses are decoded using only the rising edge of the clock (CLK) signal.

Claim Element	**Disclosure in Takahashi**
preceding clock cycle; and	FIG .15  (*Id*. at Fig. 15). The components of the write operation (*i.e.*, write address decoding, word line selection and write amplifier activation) do not depend upon waiting to capture write data and address information during the second half of the current clock cycle because such information was already captured in the prior clock cycle. (*Id*. at 4:44-49, 9:28-37, 21:6-17). In other words, in Figure 15 above, the write operation for the current clock cycle uses a previous write address captured during a preceding clock cycle, while the write address A2 (captured on the falling edge of CLK in the current clock cycle) is used in the next clock cycle. (*Id*. at 21:6-17).

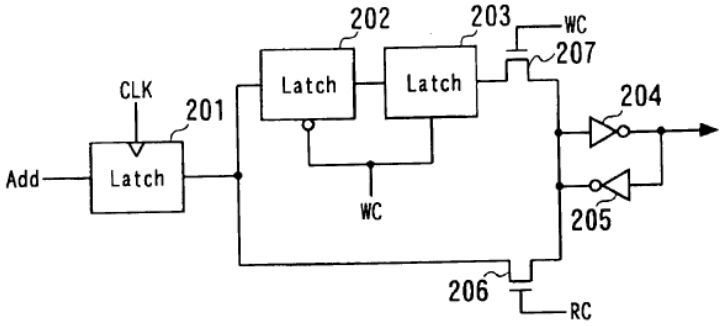
The ’861 patent, filed more than six months after Takahashi was filed, discloses the same write operation. Like Takahashi, the ’861 patent specification explains that during the current clock cycle, the write address is decoded and the write amplifier is activated using only the rising edge of the clock signal (GSI-1001 at 3:47-50, 4:57-62). Like Takahashi, the first and second pulses of the word line (WL) signal (read and write pulses, respectively) shown in Figure 4 below

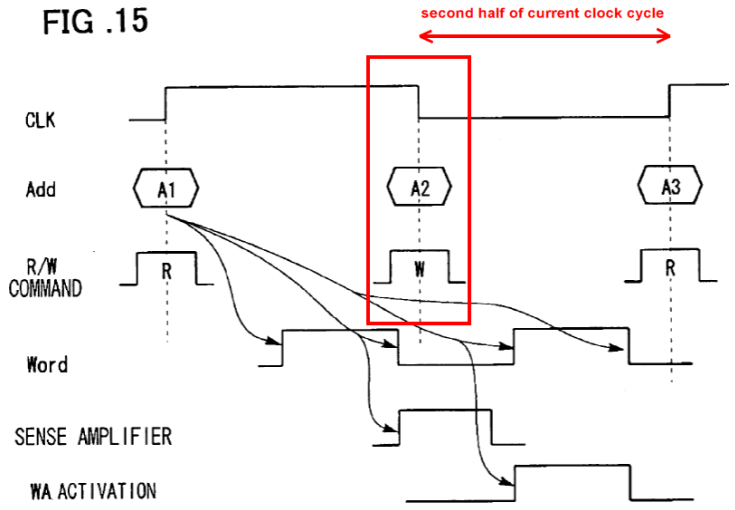
illustrate that the read and write addresses are decoded using only the rising edge of the clock signal.

FIG. 4



GSI-1001 at Fig. 4. Like Takahashi, the components of the write operation (*i.e.*, address decoding, word line selection and write amplifier activation) in the '861 patent do not depend upon waiting to capture write data and address information during the second half of the current clock cycle because such information was already captured in the prior cycle. *Id.* at 4:63-5:5. In other words, in Figure 4 above, the write operation for the current clock cycle uses a previous write address captured during a preceding clock cycle (*id.* at 4:67-5:5), while the write address (not shown, but captured on rise of Clkwr1, triggered by the falling edge of Clock in the current clock cycle) is used in the next clock cycle (*id.* at 2:62-65, 3:43-46, Fig. 4).

Claim Element	**Disclosure in Takahashi**
[1 e] capturing a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;	Takahashi discloses this step. For example, Takahashi discloses that: (1) an address clock generator 105 generates a read clock (RC) and a write clock (WC) based on the first and second transitions of the clock, respectively and (2) an address register 104 samples the input address based on the CLK signal and then outputs the address signals based on the read clock and write clock, respectively. (GSI-1003 at 8:27-49). In other words, in a given clock cycle, the address register 104 captures a current write address based on the clock signal, and the address register 104 outputs a previous write address captured during a previous clock cycle when the WC signal is received. Figure 2 further shows the address register 104. (*Id*. at Fig. 2). FIG . 7A  (*Id*. at Fig. 7A). Figure 7A shows the structure of address register 104 shown in Figure 2. (*Id*. at 17:9-14). Figure 7A shows that the current write address is captured in latch 201 during the current clock (CLK) cycle. Figure 7A shows latches 202 and 203 in the write address path between latch 201 and the output of address register 104. As configured, latches 202 and 203 act as a flip-flop clocked on the write clock WC. Consequently, in Figures 2 and 7A, the write address path has a one-clock-cycle delay relative to the read address path. Due to this delay, the captured write address will be used for a write operation implemented during a subsequent clock

Claim Element	**Disclosure in Takahashi**
	cycle. (*Id*. at 17:9-34). The example above describes an embodiment in which the read and write addresses are sampled on rising edges of the CLK signal. Takahashi discloses an alternative embodiment in which the write address is sampled on the falling edge of the clock (CLK) signal, that is, during the second half of the current clock cycle. (*Id*. at 21:6-13). Figure 15 below illustrates the capturing of the current write address (A2) during the second half of the current clock cycle:  (*Id*. at Fig. 15). Therefore, Takahashi discloses capturing a current write address (A2) during a second half of said current clock cycle (at the falling edge of the clock signal CLK).
[1 f] wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during	Takahashi discloses this limitation. For example, as explained in claim [1 d] above, the write operation for the current clock cycle uses a previous write address captured in a preceding clock cycle. (GSI-1003 at 4:44-49, 9:28-37, 21:6-17, Fig. 15). As explained in claim [1 e] above, the write address captured during the second half of the current clock cycle is not used in the write operation for the current clock cycle, but is used in a write operation of a

Claim Element	**Disclosure in Takahashi**
said second half of said current clock cycle.	subsequent clock cycle. (*Id.* at 8:27-49, 17:9-34, 21:6-13, Figs. 2, 15).

In Takahashi, the write operation for the current clock cycle uses an address captured during a previous clock cycle. GSI-1003 at 4:44-49, 9:28-37, 21:6-17, Fig. 15. A write address (A2) is captured during the second half of the current clock cycle, but that address is not used for the write operation of the current clock cycle. GSI-1003 at 8:27-49, 17:9-34, 21:6-13, Figs. 2, 15. Instead, the write address captured during the second half of the current clock cycle is used in a subsequent clock cycle. *Id*. Therefore, the write operation of the current clock cycle does not depend upon when in the current clock cycle the write address (A2) is captured (*e.g.*, early or late in the current clock cycle), or whether the write address (A2) is captured at all. GSI-1006 at ¶ 20. One of ordinary skill in the art at the time of the invention would have understood that this means the write operation for the current clock cycle is timed independent of the current write address captured during the second half of the current clock cycle. *Id*. The timing independence of the write address captured in the current clock cycle and the write operation in the current clock cycle is a necessary consequence of the limitations recited in claim elements [1 d] and [1 e] of the ’861 patent because these limitations require that the write address captured in the current clock cycle is not

used in the write operation of the current clock cycle. *Id*. Therefore, Takahashi inherently discloses this limitation.

Claim 9

The preamble of claim 9 recites "A method for implementing a self-timed, read to write protocol for a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device," which is disclosed in Takahashi. Takahashi discloses a Quad Data Rate SRAM and method for implementing data transfers. GSI-1003 at 1:13-32, 22:32-35, Fig. 2; *see also* claim [1 preamble] above. Thus, Takahashi discloses this element.

Takahashi also discloses the other elements of claim 9:

Claim Element	**Disclosure in Takahashi**
[9 a] capturing a read address during a first half of a current clock cycle;	*See* claim [1 a] above.
[9 b] commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	*See* claim [1 b] above.
[9 c] commencing a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier,	*See* claim [1 c] above.
[9 d] wherein said write operation uses a previous write address captured during a preceding clock cycle; and	*See* claim [1 d] above.
[9 e] capturing, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a	*See* claim [1 e] above.

Claim Element	**Disclosure in Takahashi**
subsequent clock cycle;	
[9 f] wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.	*See* claim [1 f] above.

Claim 18

Claim Element	**Disclosure in Takahashi**
[18 preamble] A semiconductor memory storage device, comprising:	*See* element [1 preamble] above. Takahashi further discloses a semiconductor storage device. (GSI-1003 at Title, Abstract, 1:6-9).
[18 a] circuitry configured to capture a read address during a first half of a current clock cycle;	*See* claim [1 a] above. Takahashi further discloses an address register 104 that samples the address signal. (GSI-1003 at 1:65-67; *see also id.* at 12:36-48). Figure 2 further illustrates that address register 104 captures the address signal Add. (*Id*. at Fig. 2).
[18 b] circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	*See* claim [1 b] above. Takahashi further discloses circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines. (GSI-1003 at 1:62-2:11, 8:27-49, 18:11-57, 20:16-44, 21:18-22:14, Figs. 2, 7A, 8, 9, 13, 16A, 17).
[18 c] circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier,	*See* claim [1 c] above. Takahashi further discloses circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier. (GSI-1003 at 9:28-37, 12:52-62, 19:4-17, 21:18-22:14, Figs. 2, 7A, 9, 13, 16A, 17).
[18 d] wherein said write operation uses a previous	*See* claim [1 d] above.

Claim Element	**Disclosure in Takahashi**
write address captured during a preceding clock cycle; and	
[18 e] circuitry configured to capture a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;	*See* claim [1 e] above. Takahashi further discloses circuitry configured to capture a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle. (GSI-1003 at 8:27-49, 17:9-58, 21:6-13, Figs. 2, 7A, 15).
[18 f] wherein said write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.	*See* claim [1 f] above.

Claim 26

Takahashi discloses each element of claim 26:

Claim Element	**Disclosure in Takahashi**
[26 Preamble] A Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, comprising:	*See* claim [18 preamble] above.
[26 a] circuitry configured to capture a read address during a first half of a current clock cycle;	*See* claim [18 a] above.
[26 b] circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	*See* claim [18 b] above.
[26 c] circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier,	*See* claim [18 c] above.
[26 d] wherein said write operation uses a previous write	*See* claim [18 d]

Claim Element	**Disclosure in Takahashi**
address captured during a preceding clock cycle; and	above.
[26 e] circuitry configured to capture, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;	*See* claim [18 e] above.
[26 f] wherein said write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.	*See* claim [18 f] above.

ii. Challenge #2: Takahashi Renders Claims 2-3, 10-11, 19-20 and 27-28 Obvious

Claims 2-3, 10-11, 19-20 and 27-28 depend from claims 1, 9, 18 and 26. Takahashi discloses each element of claims 1, 9, 18 and 26 as set forth in the above charts.

Claims 2, 10, 19 and 27

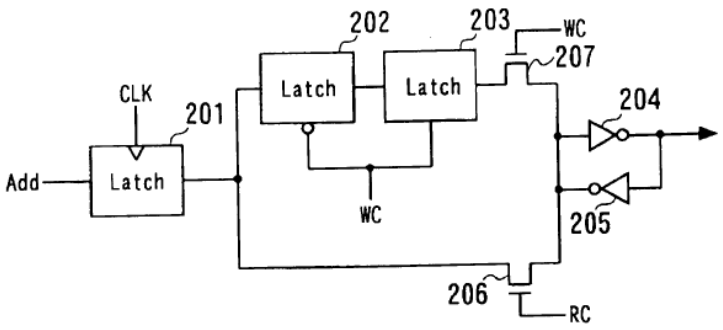
Claims 2, 10, 19 and 27 further recite generating read and write clock signals (or circuitry for generating those read and write clock signals), which limitation is not inventive in view of Takahashi.

"Internal Read Clock Signal" Element

Takahashi discloses: (1) element [2 a] "generating an internal read clock signal from a main clock signal"; (2) element [10 a] "generating an internal read clock signal from a main clock signal"; (3) element [19 a] "circuitry configured to generate an internal read clock signal from a main clock signal"; and (4) element

[27 a] "circuitry configured to generate an internal read clock signal from a main clock signal." Takahashi discloses generating an internal read clock signal (RC) from the main clock signal (CLK). GSI-1003 at 8:33-38, Fig. 7B. The internal read clock signal (RC) is used to capture a read address in a flip-flop formed by inverters 204 and 205, shown in Figure 7A below. *Id*. at 8:33-38, 17:13-19, 17:28-30, Figs. 7A, 7B.

FIG . 7A



Id. at Fig. 7A.

"First Internal Write Clock Signal" Element

Takahashi discloses: (1) element [2 b] "generating a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address"; (2) element [10 b] "generating a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address"; (3) element [19 b] "circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current

write address"; and (4) element [27 b] "circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address." Takahashi discloses a write clock signal (CLK) used to capture a current write address in address register 104 on the falling edge of the clock signal (CLK). *Id.* at 21:6-13, Figs. 2, 7A, 15. Figure 7A (reproduced above) shows the structure of address register 104 and the clock signal (CLK). *Id.* at Fig. 7A, 7:9-14.

One of ordinary skill in the art would have understood that the main external clock signal shown in Figure 2 would be internally buffered to generate an internal CLK signal to drive the latch 201 shown in Figure 7A. GSI-1006 at ¶ 21. In a memory system such as that of Takahashi, the main clock signal is heavily loaded. *Id*. The main clock signal CLK must be internally buffered to guarantee signal integrity, ensure adequate noise immunity, and to minimize clock skew and insertion delay. *Id*. Therefore, Takahashi inherently discloses circuitry for generating a first internal write clock signal (CLK input of latch 201 in Figure 7A) from a main clock signal (CLK signal in Figure 2), said first internal write clock signal used for capturing a current write address. *Id*.

"Second Internal Write Clock Signal" Element

Takahashi also discloses: (1) element [2 c] "generating a second internal write clock signal from said main clock signal, said second internal write clock

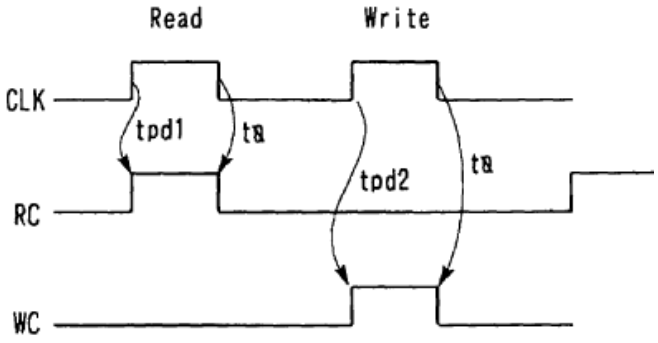
signal used for commencing a write operation for said current clock cycle"; (2) element [10 c] "generating a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle"; (3) element [19 c] "circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle"; and (4) element [27 c] "circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle." Takahashi discloses generating a second internal write clock signal (WC) from the main clock signal (CLK). GSI-1003 at 8:33-38. The second internal write clock signal (WC) is used to commence a write operation for the current clock cycle by launching an internal write address from a current buffered write address previously captured by the first internal write clock (CLK input of latch 201). *Id.* at 1:62-2:11, 12:52-62, 17:15-34, Figs. 2, 7A, 7B, 15. The current buffered write address previously captured by the first internal write clock is buffered in a flip-flop formed by master/slave latches 202 and 203, shown in Figure 7A above. *Id*. at 17:15-34, Figs. 2, 7A.

"Delayed Version" Element

Takahashi discloses: (1) element [2 d] "wherein said second internal write clock signal is also a delayed version of said internal read clock signal"; (2) element [10 d] "wherein said second internal write clock signal is also a delayed version of said internal read clock signal"; (3) element [19 d] "wherein said second internal write clock signal is also a delayed version of said internal read clock signal"; and (4) element [27 d] "wherein said second internal write clock signal is also a delayed version of said internal read clock signal." Figure 7B of Takahashi (reproduced below) shows that the second internal write clock signal (WC) follows the internal read clock signal (RC). GSI-1003 at 17:12-14, Fig. 7B. Takahashi explains that in a read operation, the read address is decoded to activate the selected word line signal based upon the internal read clock signal (RC) (*id.* at 11:56-65, 12:36-48), while in a write operation, the write address is decoded to activate the selected word line signal based upon the second internal write clock signal (WC). *Id.* at 12:52-59, 14:29-37. The read and write word line pulses generated from the RC and WC signals are shown as the first and second pulses of the word line (Word), respectively, in Figure 15 (reproduced above). *Id*. The RC and WC signals are both generated from the rising edge of the main clock signal (CLK). *Id.* at 8:33-38, 21:14-17, Fig. 15. Because the write clock signal (WC) follows the read clock signal (RC), and both signals are generated from the rising

edge of the main clock signal, the second internal write clock signal (WC) is a delayed version of the internal read clock signal (RC).

FIG . 7B



Id. at Fig. 7B.

Like Takahashi, Figure 2A of the ’861 patent shows that the internal read clock (Clkrd) and second internal write clock signal (Clkwr2) are both generated from the rising edge of the main clock signal (Clock). GSI-1001 at Fig. 2A, 3:40-43. Because the Clkwr2 signal follows the Clkrd signal (*see id.* at Fig. 4), and both signals are generated from the rising edge of the main clock signal, the second internal write clock signal (Clkwr2) is a delayed version of the internal read clock signal (Clkrd).

Claims 3, 11, 20 and 28

Claims 3, 11, 20 and 28 depend from claims 2, 10, 19 and 27, which are obvious over Takahashi for the reasons set forth immediately above.

Claims 3, 11, 20 and 28 further recite implementing sense amplifier interlock logic (or the sense amplifier interlock logic), which limitation is not inventive in view of Takahashi.

For example, claim 3 recites "implementing sense amplifier interlock logic to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier," which is disclosed by Takahashi. For example, Takahashi discloses:

> The semiconductor storage device according an embodiment of the present invention includes a circuit for performing control to effect the read cycle and the write cycle alternately (see FIG. **17**), and a circuit for controlling the timing so that the sense operation by the sense amplifier in the read cycle and the address decoding operation by the decoder in the write cycle in a cycle next following the read cycle occur in parallel (**105**, **106**, **107** in FIG. **2**). This configuration is effective to raise the frequency of the driving clock signals.

GSI-1003 at 9:28-37.

As discussed in claim [1 c], the write operation causes the write data to appear on the pair of bit lines (B and /B) as soon as the read data from the captured read address is amplified by the sense amplifier. *See also* claim [1 c].

Furthermore, Takahashi discloses sense amplifier interlock logic (and the circuitry) configured to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier. GSI-1003 at 9:28-37, 21:50-22:51, Figs. 2, 17.

Elements of the sense amplifier interlock logic (105, 106, 107 and each element in Figure 17) are depicted in Figures 2 and 17. Thus, claim 3 (and claims 11, 20 and 28) are disclosed by Takahashi.

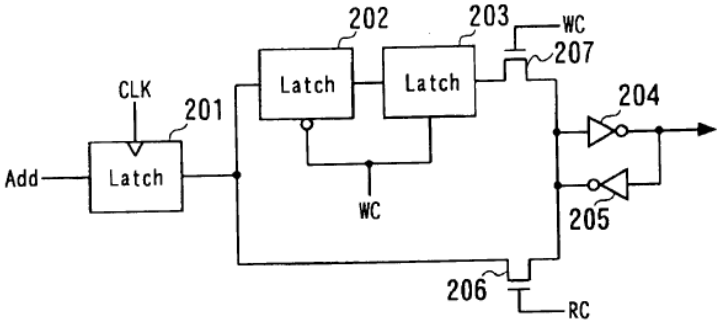
iii. **Challenge #3: Takahashi and Tsuchida Render Claims 17 and 34 Obvious**

Claims 17 and 34 add the features of "comparing said current write address in said write address buffer with said current read address; and upon determining a match between said current read address and said current write address, fetching said read data from a write data buffer" (claim 17) and "a comparator configured to compare said current write address in said write address buffer with said current read address; and circuitry configured to fetch said read data from a write data buffer upon determination of a match between said current read address and said current write address" (claim 34).

These claims depend from claims 9 and 26. Takahashi, as set forth above, discloses all of the elements of claims 9 and 26.

Furthermore, Takahashi discloses storing the current write address and the current read address. For example, the address register 104 stores the current read and write addresses. Figure 7A (reproduced below) shows the structure of address register 104. GSI-1003 at 17:9-14.

FIG . 7A



Id. at Fig. 7A. In Figure 7A, latches 202 and 203 store the current write address. *Id.* at 17:15-28. Latch 201 stores the current read address. *Id.* at17:15-19.

There is nothing new or nonobvious about forwarding late write data to the output in the event of a read request made to a late write address. GSI-1006 at ¶ 22. A person of ordinary skill would have found it obvious to implement the memory device disclosed in Takahashi using address comparison and data forwarding logic. *Id*. Takahashi is directed to a static random access memory (SRAM), and a person of ordinary skill would have known that SRAM addressing can involve data hazards. *Id*. The simple addition of one known element (address comparison and data forwarding logic) would have been within the reach of a person of ordinary skill. *Id*. The results of such substitution would have been predictable to a person of ordinary skill. *Id*. Thus, in applying the teachings of the primary reference, the person of ordinary skill would have had a finite number of identified, predictable ways to implement the RAM, each with a reasonable expectation of success.

In addition, U.S. Patent No. 6,647,478 to Tsuchida ("Tsuchida") (GSI-1005) discloses comparing the current write address in the write address buffer with the current read address and upon determining a match between the current read address and the current write address, fetching the read data from a write data buffer. GSI-1005 at 12:32-55. Figure 15 illustrates the circuitry for performing the match (coherency detector 14) and fetching the read data from the write data buffer (input data register 4).

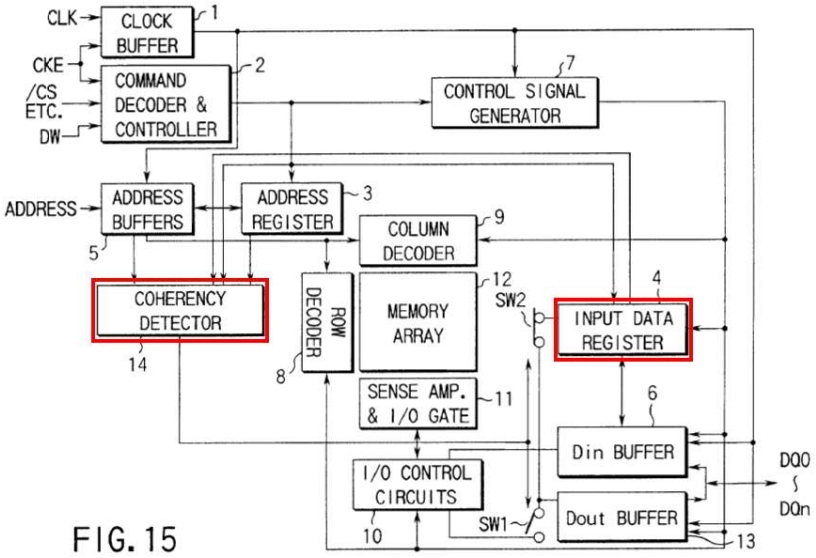


FIG. 15

Id. at Fig. 15. Thus, the prior art itself provides a teaching, suggestion and motivation to combine the references because both relate to design of memory. Moreover, design incentives and other market forces existed that would have caused a person of ordinary skill to apply Tsuchida's memory design to Takahashi's memory design to obtain a memory with improved read latency. This combination according to known methods would have yielded the predictable

result of the primary reference's memory having a write operation that is delayed by one or more clock cycles. As such, with the combination of Tsuchida and Takahashi, it would have been obvious to use Tsuchida's known memory design to improve the primary reference's similar device, ready for improvement, in the same way as taught in Tsuchida. GSI-1006 at ¶ 23. Thus, claims 17 and 34 are obvious over Takahashi alone or over Takahashi in view of Tsuchida.

iv. **Challenge #4: Okuyama Renders Claims 1-3, 9-11, 17-20, 26-28 and 34 Obvious Alone, in Combination with Takahashi or in Combination with Tsuchida**

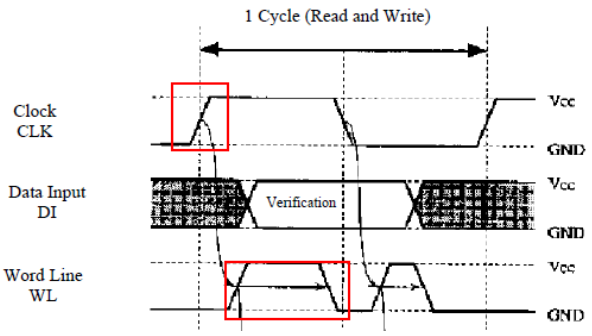
Okuyama, which was published on June 23, 2000 (four years before the '861 patent was filed), renders claims 1-3, 9-11, 17-20, 26-28 and 34 of the '861 patent obvious under 35 U.S.C. §§102(b) and 103 (pre-AIA) over Okuyama and Takahashi or obvious over Okuyama and Tsuchida. GSI-1004 is the Japanese Unexamined Patent Application Publication 2000-173270 to Okuyama. GSI-1007 is a certified English language translation of the Japanese Unexamined Patent Application Publication 2000-173270 to Okuyama ("Okuyama"), which includes an affidavit attesting to the accuracy of the translation pursuant to 37 C.F.R § 42.63(b). Citations to Okuyama in this section will be to GSI-1007.

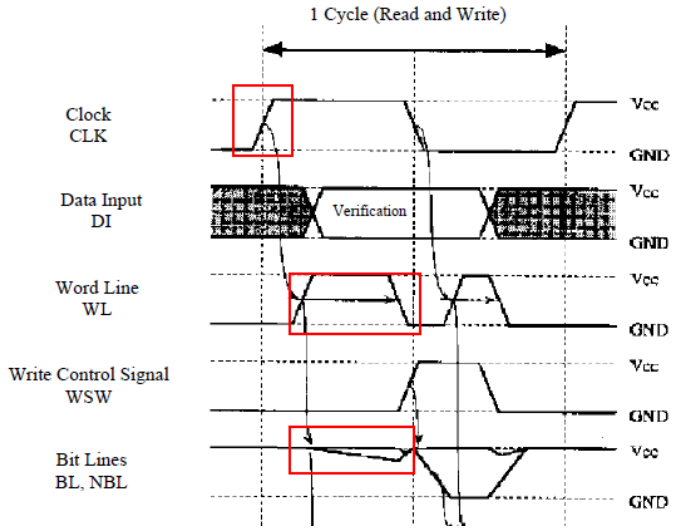
Okuyama renders claims 1-3, 9-11, 17-20, 26-28 and 34 of the '861 patent obvious under pre-AIA 35 U.S.C. § 103(a) in light the knowledge of one of ordinary skill in the art at the time of the invention, obvious over Okuyama and

Takahashi or obvious over Okuyama and Tsuchida. Okuyama discloses the same technology that allegedly is the invention of the '861 patent. Specifically, Okuyama discloses a self-timed read to write operation in a memory storage device, including circuitry for capturing a read address during a first half of a current clock cycle and circuitry for commencing a read operation corresponding to the captured read address. Okuyama discloses circuitry for commencing a write operation for the current clock cycle so as to cause write data to appear on the pair of bit lines as soon as the read data from the captured read address is amplified by the sense amplifier, wherein the write operation uses a captured write address. These elements are depicted in Figures 1 and 5 of Okuyama. GSI-1007 at Figs. 1, 5.

Okuyama discloses limitations recited in claims 1-3, 9-11, 17-20, 26-28 and 34 of the '861 patent that render each claim obvious. The following section demonstrates, on a limitation-by-limitation basis, how Okuyama, Okuyama and Takahashi, or Okuyama and Tsuchida disclose various elements of claims 1-3, 9-11, 17-20, 26-28 and 34 of the '861 patent and thus render the claims obvious under pre-AIA 35 U.S.C. § 103(a).

Claim Element	**Disclosure in Okuyama**
[1 preamble] A method for implementing a self-timed, read to write operation in a	Okuyama discloses a method for implementing a self-timed, read to write operation in a memory storage device. For example, Okuyama states:

Claim Element	**Disclosure in Okuyama**
memory storage device, the method comprising:	0020. Embodiments of the Invention. The semiconductor memory of the invention of Claim 1 is a static semiconductor memory that is equipped with a memory cell array comprising multiple memory cells and that executes read and write operations in one clock cycle, wherein there are: a word line control circuit that generates word line activation signals that set a word line to the activated state only for a fixed period during reading with the first clock edge as a standard, and set the word line to the activated state only for a fixed period during writing with the second clock edge as a standard; a circuit and a control means for it such that, after the data of a bit line pair is read into a sense circuit, cutoff is performed between the bit line pair and the sense circuit; and a circuit and a control means for it such that, after cutoff has been performed between the bit line pair and the sense circuit, write data is transferred from a write data line to the bit line pair; and writing is performed to the same memory cell simultaneously with reading in the one cycle required for reading. (GSI-1007 at ¶ 0020, Means of Solution section; *see also id.* at Fig. 5).
[1 a] capturing a read address during a first half of a current clock cycle;	Okuyama discloses this step. For example, Okuyama discloses that a word line is activated for a read operation based upon a read address captured on the first (*i.e.*, rising) clock edge (*i.e.*, during the first half of the current clock cycle). (GSI-1007 at claims 3, 5, Means of Solution section, Figs. 1,5, ¶¶ 0024, 0032, 0038, 0040-0042). The captured read address data is applied to the word line decoder 60 in Figure 1. (*Id*. at Fig. 1). Further, Figure 5 (a partial figure annotated in red below) shows that the word line WL is asserted during the first half of the clock cycle. As disclosed in claim 5 and Figures 1 and 5, asserting the word line during the first half of the clock cycle is in response to a read address captured on the AD input in Figure 1 during the first half of the current clock cycle. (*Id*. at claim 5, ¶¶ 0024, 0032, Figs. 1, 5). Figure 5  (*Id*. at Fig. 5).

Claim Element	**Disclosure in Okuyama**
[1 b] commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	Okuyama discloses this step. For example, Okuyama discloses that data in a memory cell is read onto a bit line pair (BL, NBL) in response to a first edge of a clock signal. (GSI-1007 at ¶¶ 0020, 0038, 0040, Fig. 5). Furthermore, Figure 5 (partially reproduced below with annotations) shows a read operation (commencing at the first rising edge of the clock signal CLK annotated in red) that reads data corresponding to the captured read address (the captured read address having already been decoded to assert word line WL annotated in red) onto a pair of bit lines (BL, NBL annotated in red). Figure 5  (*Id*. at Fig. 5).
[1 c] commencing a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified	Okuyama discloses this step. Okuyama describes a write operation for the current clock cycle immediately following the read operation. (GSI-1007 at ¶¶ 0020, 0035, 0041). In other words, as soon as the read data is adequately amplified by the sense circuit 30, the bit lines BL, NBL are cut off from the sense circuit 30 by the sense circuit cutoff switch 35 (shown in Figure 1) and connected to the data input buffer 50 by a write control switch 55 (shown in Figure 1) that allows write data to appear

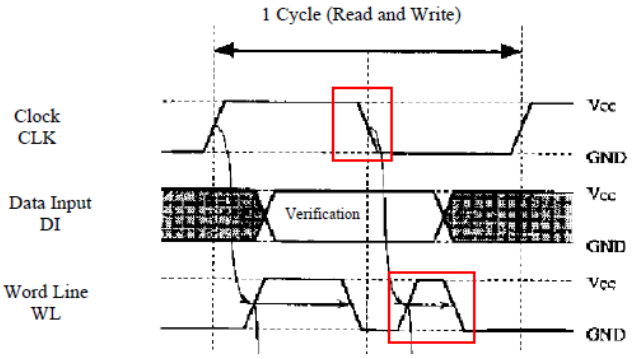
Claim Element	**Disclosure in Okuyama**
by a sense amplifier,	on the bit lines BL, NBL. Figure 1 also shows the sense circuit cutoff switch 35, the data input buffer 50, the write control switch 55, and the bit lines BL, NBL. (*Id*. at Fig. 1). Okuyama further states that the write data is driven on the pair of bit lines BL, NBL as soon as the read data from the captured read address is amplified by the sense amplifier circuit 30: 0045. As explained above, according to this first embodiment, a one-port SRAM cell (101) is used as the memory cell and control is performed so that a word line (WL) is put into the activated state only for fixed periods, with the first clock edge of the clock (CLK) as a standard during reading and its second clock edge as a standard during writing. Also, if a read access and a write access are generated during the same cycle, control is performed so that the word line (WL) is activated twice within the same cycle with those respective times as standards, and after the data that was read from the memory cell (101) has been transferred to the sense circuit (30), cutoff occurs between the bit line pair (BL, NBL) and the sense circuit (30), and the write data from the write circuit is transferred to the bit line pair (BL, NBL). In this way it is possible to simultaneously execute a read operation and a write operation to the same SRAM cell, that is, to the same address, in the one cycle required for a read operation, so it is possible to improve system throughput. (*Id*. at ¶ 0045).
[1 d] wherein said write operation uses a previous write address captured during a preceding clock cycle; and	As discussed in claim [1 c] above, Okuyama discloses a write operation. The write operation uses a captured write address. (GSI-1007 at claim 5).

There is nothing new or nonobvious about a write operation that uses a previous write address captured during a preceding clock cycle. GSI-1006 at ¶ 25. In fact, the term "late write," a well-known term of the art at the time the '861 patent was filed, embodies this principle. *Id*. A person of ordinary skill would have found it obvious to implement the memory in Okuyama as a late write part. *Id*. Okuyama discloses a semiconductor memory, and a person of ordinary skill would have known that a memory has a write operation, and that writing to an address captured during a preceding clock cycle (*i.e.*, late write) would improve the

performance of the overall memory design. *Id*. The simple substitution of one known element (a conventional write type memory) for another element (a late write type memory) would have been within the reach of a person of ordinary skill and the results of such substitution would have been predictable to a person of ordinary skill. *Id*. Therefore, in applying the teachings of Okuyama, the person of ordinary skill would have had a finite number of identified, predictable ways to implement the memory, each with a reasonable expectation of success. *Id*.

Furthermore, Takahashi (GSI-1003) discloses a write operation that uses a previous write address captured during a preceding clock cycle. *See* Challenge #1, claim [1 d] of Takahashi. One of ordinary skill in the art would be motivated to combine Okuyama with Takahashi because the prior art itself provides a teaching, suggestion and motivation to combine the references, because both relate to design of memory. Moreover, design incentives and other market forces existed that would have caused a person of ordinary skill to apply Takahashi's late write memory design to Okuyama's memory to obtain a late write memory. The combination of Okuyama and Takahashi according to known methods would have yielded the predictable result of Okuyama's memory being a late write part. As such, given the combination of Takahashi and Okuyama, it would have been obvious to use Takahashi's known late write memory design to improve

Okuyama's similar device, ready for improvement, in the same way as taught in Takahashi. GSI-1006 at ¶ 26.

Claim Element	**Disclosure in Okuyama**
[1 e] capturing a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;	Okuyama discloses this step. For example, Okuyama states that a word line is activated based upon a write address captured on the second (*i.e.*, falling) clock edge (*i.e.*, during the second half of the current clock cycle). (GSI-1007 at claim 5, Means of Solution section). Okuyama also discloses that a write address is captured on the second (*i.e.*, falling) clock edge, during the second half of the current clock cycle by a word line decoder from an address input AD. (*Id*. at claim 5, ¶ 0032, Figs. 1, 5). The captured write address data is applied to the word line decoder 60 shown in Figure 1. Figure 5 (partially reproduced below) shows that a word line WL (decoded from the read address captured on the falling edge of the CLK signal) is asserted during the second half of the clock cycle. The edge of the clock that captures the write address and the word line assertion resulting from decoding the captured write address are annotated in red below. Figure 5  (*Id*. at Figs. 1, 5).

There is nothing new or nonobvious about capturing a current write address and using the current write address for a write operation implemented during a

subsequent clock cycle. GSI-1006 at ¶ 27. In fact, the term "late write," a well-known term of art at the time the '861 patent was filed, embodies this principle. *Id*. A person of ordinary skill would have found it obvious to implement the memory in Okuyama this way. *Id*. Okuyama is directed to memories, and a person of ordinary skill would have known that a memory has a write operation that writes to a particular memory address, and that capturing a current write address and using the current write address for a write operation implemented during a subsequent clock cycle (*i.e.*, late write) could improve the performance of the overall memory design. *Id*. The simple substitution of one known element (a conventional write) for another (a late write) would have been within the reach of a person of ordinary skill. *Id*. The results of such substitution would have been predictable to a person of ordinary skill. *Id*. Thus, in applying the teachings of Okuyama, the person of ordinary skill would have had a finite number of identified, predictable ways to implement the memory, each with a reasonable expectation of success. *Id*.

Furthermore, Takahashi (GSI-1003) discloses capturing a current write address to be used for a write operation implemented during a subsequent clock cycle. *See* claim [1 f] of Takahashi. One of ordinary skill in the art would be motivated to combine Okuyama with Takahashi because the prior art itself provides a teaching, suggestion and motivation to combine the references, because

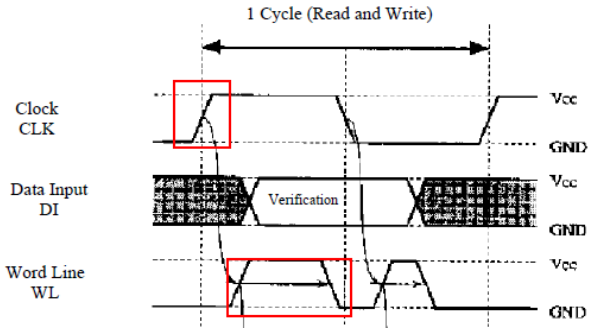
both relate to design of memory. Moreover, design incentives and other market forces existed that would have caused a person of ordinary skill to apply Takahashi's capturing of the write address for a subsequent write operation design to Okuyama's memory to obtain a late write memory. The combination of Okuyama and Takahashi according to known methods would have yielded the predictable result of the Okuyama's memory being a late write part that captures the write address for a subsequent write operation. As such, the combination of Takahashi and Okuyama would have been the use of Takahashi's known capturing of the write address for a subsequent write operation to improve Okuyama's similar device, ready for improvement, in the same way as taught in Takahashi. GSI-1006 at ¶ 28.

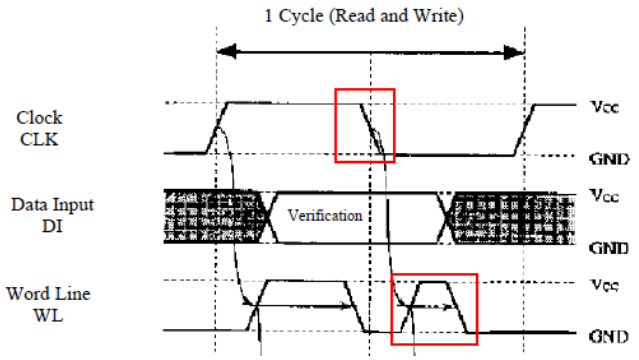
Claim Element	**Disclosure in Okuyama**
[1 f] wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.	As discussed in claim [1 c] above, Okuyama discloses commencing a write operation for the current clock cycle. As discussed in claim [1 e] above, Okuyama discloses capturing a current write address during the second half of the current clock cycle.

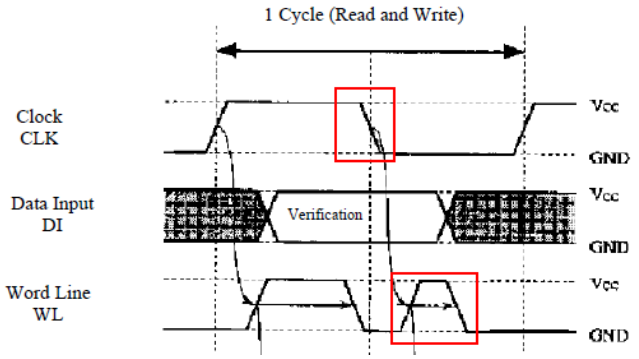
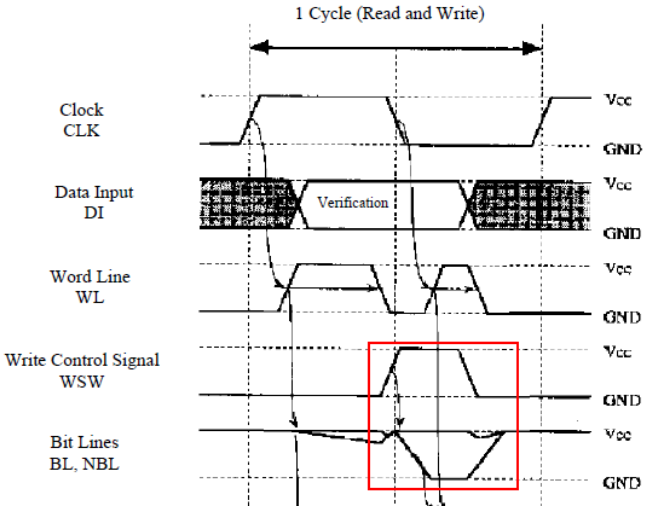
Claim [1 d] above requires that the write operation of the current clock cycle use a previous write address captured during a preceding clock cycle. Claim [1 e] requires that the current write address captured during the second half of the current clock cycle be used for a write operation implemented during a subsequent clock cycle. Therefore, the current write address captured during the second half

of the current clock cycle is not used for the write operation of the current clock cycle. GSI-1006 at ¶ 29. Thus, the write operation of the current clock cycle does not depend upon when in the current clock cycle the write address is captured (*e.g.*, early or late in the current clock cycle). *Id*. In fact, the write operation for the current clock cycle would operate correctly even if *no* write address is captured in the current clock cycle. *Id*. One of ordinary skill in the art at the time of the invention would have understood that this means the write operation for the current clock cycle is timed independent of the current write address captured during the second half of the current clock cycle. *Id*. The timing independence of the write address captured in the current clock cycle and the write operation in the current clock cycle is a necessary consequence of the limitations recited in claim elements [1 d] and [1 e] of the ’861 patent because these limitations require that the write address captured in the current clock cycle is not used in the write operation of the current clock cycle. *Id*. Therefore, claim 1 is obvious over Okuyama or Okuyama in view of Takahashi.

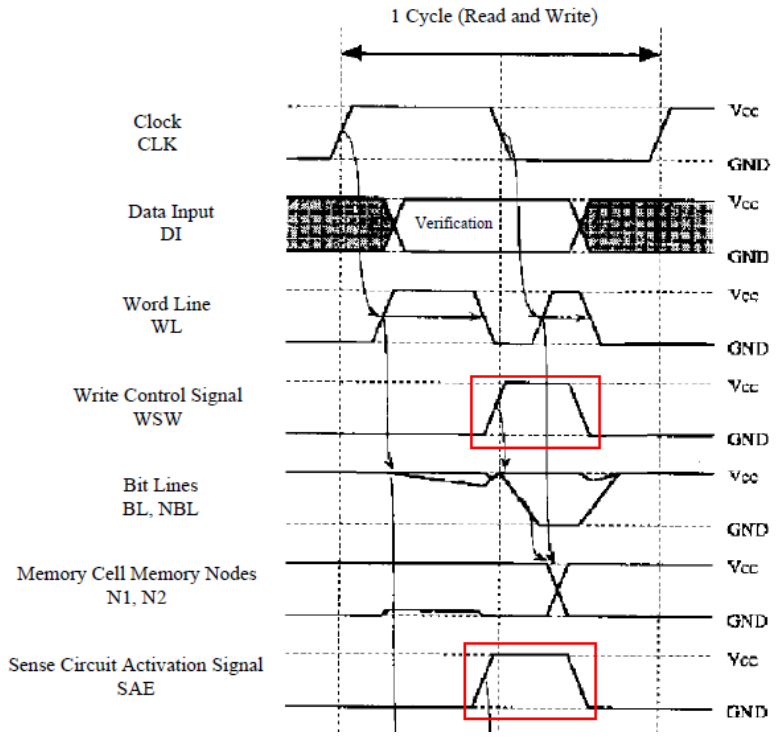
Claim Element	**Disclosure in Okuyama**
[2 preamble] The method of claim 1, further comprising:	*See* claim 1.
[2 a] generating an internal read clock signal	Okuyama discloses this step. For example, Okuyama discloses that the word line pulse control signal (810), which is generated from the main clock signal (CLK), causes word line driver (70) to activate the word line (WL)

Claim Element	**Disclosure in Okuyama**
from a main clock signal;	to read data from the selected memory cell on to the bit lines (BL, NBL). (GSI-1007 at ¶ 0038). Figure 1 shows the control line 810 from the word line pulse control generator circuit that control the word line driver 70 based on the clock CLK. (*Id*. at Fig. 1). Figure 5 (reproduced in part below) shows the generating of the first word line activation for the read. Therefore, Okuyama discloses generating an internal read clock signal (the word line pulse control signal 810) from the main clock signal (CLK). Figure 5  (*Id*. at Fig. 5). Alternatively, Okuyama discloses that a sense circuit activation signal (SAE) is generated by the timing control circuit (80) from the main clock (CLK). (*Id*. at ¶ 0038, Fig. 1). The sense circuit activation signal (SAE) is used to activate the sense circuit (30) to amplify the data read from the selected memory cell. (*Id*. at ¶ 0041). Therefore, the sense circuit activation signal (SAE) is a read clock. Therefore, Okuyama discloses generating an internal read clock signal (the sense circuit activation signal SAE) from the main clock signal (CLK).
[2 b] generating a first internal write clock signal from said main clock	Okuyama discloses this step. For example, Okuyama states that the word line pulse control signal (810) activates a second pulse of a word line (WL) within one clock cycle, the second pulse causing data to be written to the selected cell. (GSI-1007 at ¶¶ 0038-0040). The current write address determines which word line (WL) signal is

Claim Element	**Disclosure in Okuyama**
signal, said first internal write clock signal used for said capturing a current write address; and	activated, and thus which cell is selected for writing. When activating the second pulse of the word line (WL) (annotated in red in annotated partial Figure 5 below), the word line pulse control signal (810) causes the current write address to be captured and decoded into the second pulse of the word line (WL), thereby selecting the cell for writing. Figure 5  (*Id*. at Figs. 1, 5, ¶¶ 40-41). Figure 1 also shows that the word line pulse control signal (810) is generated from the main clock signal (CLK). (*Id*.)
[2 c] generating a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;	Okuyama discloses this step. For example, Okuyama discloses that a second pulse of a word line (WL) within one clock cycle causes data to be written to a selected cell in the current clock cycle. (GSI-1007 at ¶¶ 0039-0041). Figures 1 and 5 show that the second pulse of the word line (WL) is generated from the main clock signal (CLK). Therefore, Okuyama discloses generating a second internal write clock signal (the second pulse of the word line WL, annotated in red) from said main clock signal (CLK, annotated in red), said second internal write clock signal used for commencing a write operation for said current clock cycle.

Claim Element	Disclosure in Okuyama
	Figure 5  (*Id*. at Figs. 1, 5). Alternatively, Okuyama discloses that the write control signal (WSW) causes input data to be transferred from the input buffer (50) to the common bus line (25) and finally to the bit line pair (BL, NBL), where it is written to the selected memory cell in the current clock cycle. (*Id*. at ¶ 0039). Figures 1 and 5 show that the write control signal (WSW) is generated from the main clock signal (CLK). Therefore, Okuyama discloses generating a second internal write clock signal (WSW, annotated in red) from said main clock signal (CLK), said second internal write clock signal used for commencing a write operation for said current clock cycle. Figure 5  (*Id*. at Figs. 1, 5).

Claim Element	**Disclosure in Okuyama**
[2 d] wherein said second internal write clock signal is also a delayed version of said internal read clock signal.	Okuyama discloses this limitation. When the internal read clock signal is the word line pulse control signal (810), the second pulse of the word line WL (*i.e.*, the second internal write clock signal) is also a delayed version of the word line pulse control signal 810 (i.e., the internal read clock signal). (GSI-1007 at ¶ 0039). Figure 1 shows that the second pulse of the word line WL (*i.e.*, the second internal write clock signal) is a downstream – and thus delayed – version of the word line pulse control signal 810 (*i.e.*, the internal read clock signal). (*Id*. at Fig. 1). Alternatively, when the internal read clock signal is the sense circuit activation signal (SAE), the write control signal WSW (i.e., the second internal write clock signal) is a delayed version of the sense circuit activation signal SAE (*i.e.*, the internal read clock signal). (*Id*. at ¶ 0041). Figure 5 (reproduced below) show that the write control signal WSW (*i.e.*, the second internal write clock signal) is a delayed version of the sense circuit activation signal SAE (*i.e.*, the internal read clock signal).

Claim Element	**Disclosure in Okuyama**
	Figure 5  (*Id*. at Fig. 5).
3. The method of claim 2, further comprising implementing sense amplifier interlock logic to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured	*See* claim [1 c]. Furthermore, Okuyama discloses sense amplifier interlock logic (the sense amplifier cutoff switch 35, write control switch 55 and timing control circuit 80 in Figure 1) to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier. (GSI-1007 at Means of Solution Section,¶¶ 0020, 0035, 0038-0039, Fig. 1).

Claim Element	**Disclosure in Okuyama**
read address is amplified by said sense amplifier.	

Claim 9

The preamble of claim 9 recites "A method for implementing a self-timed, read to write protocol for a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device," which is disclosed in Okuyama. For example, Okuyama discloses an SRAM memory array with the attributes of a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, including separate data I/O and the ability to read and write data on both the rising and falling edges of the clock. GSI-1007 at ¶¶ 0034-0036, Figs. 1, 5.

In addition, there is nothing new or nonobvious about the claimed QDR SRAM. GSI-1006 at ¶ 30. To the extent that Okuyama does not disclose a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, a person of ordinary skill would have found it obvious to implement the memory device disclosed in Okuyama as a Quad Data Rate SRAM. *Id*. Okuyama is directed to a random access memory (RAM), and a person of ordinary skill would have known that a RAM can be implemented as a QDR SRAM. *Id*. The simple substitution of one known element (a RAM) for another (a QDR SRAM) would have been within the reach of a person of ordinary skill. *Id*. The results of such substitution would

have been predictable to a person of ordinary skill. *Id*. Thus, in applying the teachings of Okuyama, the person of ordinary skill would have had a finite number of identified, predictable ways to implement the RAM, each with a reasonable expectation of success. *Id*.

Furthermore, Takahashi (GSI-1003) discloses a QDR SRAM. *See* claim [9 preamble] of Takahashi. One of ordinary skill in the art would be motivated to combine Okuyama with Takahashi because using the techniques of Takahashi would have improved Okuyama in the same way, and applying the techniques disclosed in Takahashi to improve Okuyama would have yielded predictable results. GSI-1006 at ¶ 31.

Okuyama also discloses the other elements of claim 9:

Claim Element	**Disclosure in Okuyama**
[9 a] capturing a read address during a first half of a current clock cycle;	*See* claim [1 a] above.
[9 b] commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	*See* claim [1 b] above.
[9 c] commencing a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier,	*See* claim [1 c] above.
[9 d] wherein said write operation uses a previous write address captured during a preceding clock cycle; and	*See* claim [1 d] above.
[9 e] capturing, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;	*See* claim [1 e] above.

Claim Element	**Disclosure in Okuyama**
[9 f] wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.	*See* claim [1 f] above.

Furthermore, with respect to "capturing, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle," although not explicitly shown in Figure 1 of Okuyama, one of ordinary skill in the art at the time of the invention would have understood that the address value at the AD input in Figure 1 is captured and stored by a buffer. GSI-1007 at Fig. 1; GSI-1006 at ¶ 32. The use of a buffer at primary I/O boundaries (such as the AD input pin) is required in synchronous digital designs such as the SRAM disclosed in Okuyama in order to provide for independence between off-chip components (such as the devices driving the chip inputs or being driven by the chip outputs) and the on chip components (such as the word line decoder, word line driver, and sense amplifiers fanning out from the AD input pin). *Id*. Otherwise, the frequency at which the CLK pin could be driven would depend upon the delay of the circuits driving the chip's input pins. *Id*. Therefore, Okuyama inherently discloses a buffer at the AD input of Figure 1. *Id*.

Furthermore, Takahashi discloses capturing a write address in an input buffer 104. *See* Challenge #1 (Takahashi at claim [1 e]). To the extent that

Okuyama is found not to expressly or inherently disclose this element, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Okuyama with the teachings of Takahashi.

Claim 10

Okuyama discloses each element of claim 10 and thus renders claim 10 obvious for the same reasons as set forth in the chart above for claim 9 and elements [2 a], [2 b], [2 c] and [2 d], respectively of claim 2:

Claim Element	Disclosure in Okuyama
[10 a] generating an internal read clock signal from a main clock signal;	*See* claim [2 a] above.
[10 b] generating a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and	*See* claim [2 b] above.
[10 c] generating a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;	*See* claim [2 c] above.
[10 d] wherein said second internal write clock signal is also a delayed version of said internal read clock signal.	*See* claim [2 d] above.

Claim 11

Okuyama discloses each element of claim 11 ("The method of claim 10, further comprising implementing sense amplifier interlock logic to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier")

and thus renders claim 11 obvious for the same reasons as set forth in the chart above for claim 3.

Claim 17

Claim 17 recites "[t]he method of claim 9, further comprising: comparing said current write address in said write address buffer with said current read address; and upon determining a match between said current read address and said current write address, fetching said read data from a write data buffer."

As explained in claim [1 e], Okuyama discloses capturing a current write address. As explained in claim [9 e], it would have been obvious to store the write address in a write address buffer. As explained in claim [1 a], Okuyama discloses capturing a current read address.

Furthermore, there is nothing new or nonobvious about forwarding late write data to the output in the event of a read request made to a late write address. GSI-1006 at ¶ 34. A person of ordinary skill would have found it obvious to implement the memory device disclosed in Okuyama using address comparison and data forwarding logic. *Id*. Okuyama is directed to a static random access memory (SRAM), and a person of ordinary skill would have known that SRAM addressing can involve data hazards. *Id*. The simple addition of one known element (address comparison and data forwarding logic) would have been within the reach of a person of ordinary skill. *Id*. The results of such substitution would have been

predictable to a person of ordinary skill. *Id*. Therefore, in applying the teachings of Okuyama, the person of ordinary skill would have had a finite number of identified, predictable ways to implement the RAM, each with a reasonable expectation of success.

In addition, as detailed above, Tsuchida (GSI-1005) discloses comparing the current write address in the write address buffer with the current read address, and upon determining a match between the current read address and the current write address, fetching the read data from a write data buffer. GSI-1005 at 12:32-55. Furthermore, Figure 15 of Tsuchida illustrates the circuitry for performing the match (coherency detector 14) and fetching the read data from the from the write data buffer (input data register 4). *Id.* at Fig. 15. Tsuchida itself provides a teaching, suggestion and motivation to combine the references, because both relate to design of memory. Moreover, design incentives and other market forces existed that would have caused a person of ordinary skill to apply Tsuchida's memory design to memory of Okuyama to obtain a memory with improved read latency. The combination of Tsuchida and Okuyama according to known methods would have yielded the predictable result of the primary reference's memory having a write operation that is delayed by one or more clock cycles. As such, the combination of Tsuchida and Okuyama would have been the use of Tsuchida's

known memory design to improve the primary reference's similar device, ready for improvement, in the same way as taught in Tsuchida.

Claim Element	**Disclosure in Okuyama**
[18 preamble] A semiconductor memory storage device, comprising:	*See* claim [1 preamble]. Furthermore, Okuyama discloses a semiconductor memory. (GSI-1007 at Title, Abstract, ¶ 0020, Fig. 1).
[18 a] circuitry configured to capture a read address during a first half of a current clock cycle;	*See* claim [1 a]. Okuyama also discloses circuitry configured to capture a read address during a first half of a current clock cycle. (GSI-1007 at Fig. 1).
[18 b] circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	*See* claim [1 b]. Okuyama also discloses circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines. (GSI-1007 at Fig. 1).
[18 c] circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier,	*See* claim [1 c]. Okuyama also discloses circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier. (GSI-1007 at Fig. 1).
[18 d] wherein said write operation uses a previous write address captured during a preceding clock cycle; and	*See* claim [1 d].
[18 e] circuitry configured to capture a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;	*See* claim [1 e]. Okuyama also discloses circuitry configured to capture a current write address during a second half of said current clock cycle. (GSI-1007 at Fig. 1).
[18 f] wherein said write	*See* claim [1 f].

Claim Element	**Disclosure in Okuyama**
operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.	
[19 preamble] The memory storage device of claim 18, further comprising:	*See* claim 18.
[19 a] circuitry configured to generate an internal read clock signal from a main clock signal;	*See* claim [2 a]. Okuyama also discloses circuitry configured to generate an internal read clock signal from a main clock signal. (GSI-1007 at Figs. 1, 5).
[19 b] circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and	*See* claim [2 b]. Okuyama also discloses circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address. (GSI-1007 at Figs. 1, 5).
[19 c] circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;	*See* claim [2 c]. Okuyama also discloses circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle. (GSI-1007 at Figs. 1, 5).
[19 d] wherein said second internal write clock signal is also a delayed version of said internal read clock signal.	*See* claim [2 d].
20. The method of claim 19, further comprising sense amplifier interlock logic configured to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is	*See* claim 3. Okuyama also discloses sense amplifier interlock logic (sense circuit cutoff switch 35 and write control switch 55 in Figure 1) configured to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by

Claim Element	**Disclosure in Okuyama**
amplified by said sense amplifier.	said sense amplifier. (GSI-1007 at Figs. 1, 5).

Claim 26

Okuyama discloses each element of claim 26:

Claim Element	**Disclosure in Okuyama**
[26 Preamble] A Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, comprising:	*See* claim [18 preamble] above
[26 a] circuitry configured to capture a read address during a first half of a current clock cycle;	*See* claim [18 a] above.
[26 b] circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;	*See* claim [18 b] above.
[26 c] circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier,	*See* claim [18 c] above.
[26 d] wherein said write operation uses a previous write address captured during a preceding clock cycle; and	*See* claim [18 d] above.
[26 e] circuitry configured to capture, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;	*See* claim [18 e] above.
[26 f] wherein said write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.	*See* claim [18 f] above.

Claim 27

Okuyama discloses each element of claim 27 and thus renders claim 27 obvious for the same reasons as set forth in the chart above for elements [26 preamble], [19 a], [19 b], [19 c] and [19 d], respectively of claims 26 and 19:

Claim Element	Disclosure in Okuyama
[27 preamble] "The QDR SRAM device of claim 26, further comprising:	*See* claim 26.
[27 a] circuitry configured to generate an internal read clock signal from a main clock signal;	*See* claim [19 a].
[27 b] circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and	*See* claim [19 b].
[27 c] circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;	*See* claim [19 c].
[27 d] wherein said second internal write clock signal is also a delayed version of said internal read clock signal.	*See* claim [19 d].

Claim 28

Okuyama discloses each element of claim 28 ("The QDR SRAM device of claim 27, further comprising sense amplifier interlock logic configured to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier") and thus renders claim 28 obvious for the same reasons as set forth in the chart above for claim 20.

Claim 34

Okuyama discloses each element of claim 34 ("The QDR SRAM device of claim 26, further comprising: a comparator configured to compare said current write address in said write address buffer with said current read address; and circuitry configured to fetch said read data from a write data buffer upon determination of a match between said current read address and said current write address") and thus renders claim 34 obvious for the same reasons as set forth in the charts above for claims 17 and 26.

V. CONCLUSION

Petitioner has set forth multiple independent bases for finding a reasonable likelihood of prevailing on the unpatentability of claims 1-3, 9-11, 17-20, 26-28 and 34 of the '861 patent. Therefore, Petitioner asks that the Patent Office order an *inter partes* review trial and cancel these claims.

Respectfully submitted,

Dated: February 7, 2014

/Timothy W. Lohse/

Registration No. 35,255
DLA PIPER LLP (US)
2000 University Avenue
East Palo Alto, CA 94303-2214
Telephone:650.833.2055
Facsimile: 650.833.2001

CERTIFICATE OF SERVICE

The undersigned certifies service pursuant to 37 C.F.R. 37 C.F.R. §§ 42.6(e) and 42.105(b) on the Patent Owner by Express Mail of a copy of this Petition for *Inter Partes* Review and supporting material at the following correspondence address of record for the ’861 patent:

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE CA 95134-1709

Dated: February 7, 2014

/Timothy W. Lohse/
Timothy W. Lohse
Registration No. 35,255

DLA PIPER LLP (US)
2000 University Avenue
East Palo Alto, CA 94303-2215
Telephone:650.833.2055
Facsimile: 650.687.1183