IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
Alexandria Division

MACRONIX INTERNATIONAL CO., LTD, a Taiwanese corporation, Plaintiff, v. **SPANSION INC.**, a Delaware corporation, and **SPANSION LLC**, a Delaware corporation, Defendants.	**Civil Action No.: 3:13-cv-00679-REP**

MACRONIX INTERNATIONAL CO., LTD'S
FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Macronix International Co., Ltd. ("Macronix") brings this first amended complaint for patent infringement against Spansion, Inc. and Spansion LLC (collectively, the "Defendants"), and in support thereof states as follows:

INTRODUCTION

1. Macronix brings this action pursuant to the patent laws of the United States, including 35 U.S.C. § 271, et seq. Defendants have and continue to infringe one or more claims of U.S. Patent Nos. 5,619,052 ("the '052 Patent"); 5,836,772 ("the '772 Patent"); 5,998,826 ("the '826 Patent"); 6,031,757 ("the '757 Patent"); 6,421,267 ("the '267 Patent"); 8,341,324 ("the '324 Patent"); and 8,341,330 ("the '330 Patent") (collectively, the "Macronix Patents" or the "Patents-in-Suit"). True and correct copies of the Macronix Patents are attached hereto as Exhibits A through G, respectively.

THE PARTIES

2. Macronix International Co., Ltd. is a corporation organized under the laws of Taiwan, having its principal place of business at No. 16, Li-Hsin Road, Science Park, Hsin-chu, Taiwan, Republic of China. Macronix is the owner of all right, title and interest to the Macronix Patents, including the right to collect damages for past infringement of the Macronix Patents.

3. Upon information and belief, Spansion, Inc. is incorporated in Delaware and its headquarters are located at 915 DeGuigne Drive, Sunnyvale, CA 94085. Spansion, Inc. makes, uses, sells, offers to sell, and imports flash memory chips that infringe the Macronix Patents in this District and elsewhere.

4. Upon information and belief, Spansion LLC is a wholly owned operating subsidiary company of Spansion, Inc. Spansion LLC is incorporated in Delaware and its headquarters are located at 915 DeGuigne Drive, Sunnyvale, CA 94085. Spansion LLC makes, uses, sells, offers to sell, and imports flash memory chips that infringe the Macronix Patents in this District and elsewhere.

JURISDICTION AND VENUE

5. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

6. Upon information and belief, this Court has personal jurisdiction over Defendants for at least the following reasons: (i) Defendants have committed acts of willful patent infringement, and/or induced acts of patent infringement by others, in this District and elsewhere in Virginia and the United States; (ii) Defendants knowingly and intentionally place their

products, including the accused products, into the stream of commerce within this District and can reasonably be expected to be hailed into court here; and (iii) Defendants have voluntarily consented to the jurisdiction of this Court with regard to patent infringement actions involving flash memory devices, including because Spansion LLC previously filed a similar action within this District and further opposed transferring that case out of this District.

7. Upon information and belief, venue is proper in this District under 28 U.S.C. §§ 1391(b)-(c) and 1400(b) because Defendants are subject to personal jurisdiction in this District and have committed acts of infringement in this District. For instance, upon information and belief, Defendants have sold infringing products to downstream customers located in this District, including: Cornet Technology, Inc., Encore Networks, Power Monitors, Inc., Vidar Systems, and NAL Research.

BACKGROUND

8. Established in 1989, Macronix is a leading innovator of non-volatile memory semiconductor solutions. Led by scientists and researchers, Macronix dedicates a substantial portion of its revenue, upwards of $170 million annually, to research and development and regularly publishes and presents technical papers in major international conferences to help bring the next generation of non-volatile memory solutions to consumers all over the world. Macronix's cutting-edge technology is used in a wide range of products.

9. Macronix has made substantial investments in protecting its intellectual property. Macronix has over 5,000 patents issued to it worldwide, including over 1,700 United States patents. According to a 2011 study by the Patent Board™, among the 240 semiconductor

companies evaluated, Macronix's patent portfolio was ranked as the 18th worldwide and 1st in the Taiwanese semiconductor industry.

10. However, Macronix's ability to provide consumers with innovative technology is dependent upon its ability to protect its innovations. To that end, Macronix's ability to compete has been significantly compromised by the acts complained of in this Complaint.

ASSERTED PATENTS

11. Macronix is the owner of all rights, title, and interest in the Macronix Patents, including the right to bring this suit for injunctive relief and damages.

12. The '052 Patent, titled "Interpoly Dielectric Structure in EEPROM Device," was duly and legally issued by the United States Patent and Trademark Office on April 8, 1997.

13. The '772 Patent, titled "Interpoly Dielectric Process" was duly and legally issued by the United States Patent and Trademark Office on Nov. 17, 1998.

14. The '826 Patent, titled "Triple Well Floating Gate Memory and Operating Method with Isolated Channel Program, Preprogram and Erase Processes" was duly and legally issued by the United States Patent and Trademark Office on Dec. 7, 1999.

15. The '757 Patent, titled "Write Protected, Non-Volatile Memory Device with User Programmable Sector Lock Capability" was duly and legally issued by the United States Patent and Trademark Office on Feb. 29, 2000.

16. The '267 Patent, titled "Memory Array Architecture" was duly and legally issued by the United States Patent and Trademark Office on Jul. 16, 2002.

17. The ’324 Patent, titled “Serial Peripheral Interface and Method for Data Transmission” was duly and legally issued by the United States Patent and Trademark Office on Dec. 25, 2012.

18. The ’330 Patent, titled “Method and System for Enhanced Read Performance in Serial Peripheral Interface” was duly and legally issued by the United States Patent and Trademark Office on Dec. 25, 2012.

COUNT I

(INFRINGEMENT OF THE ’052 PATENT)

19. Plaintiff realleges and incorporates herein by reference the allegations in paragraphs 1 – 18 above as if fully set forth herein.

20. Upon information and belief, the Defendants have infringed, and continue to infringe, the ’052 Patent by making, using, offering for sale, and/or selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the ’052 Patent, including, but not limited to their S34ML01G1, S34ML02G1, S34ML04G1, S34ML08G1, S34ML01G2, S34ML04G2, S34MS01G1, and S34MS02G1 NAND Flash Memory Products. Such infringing products infringe, literally and/or under the doctrine of equivalents, at least the following valid and enforceable claims of the ’052 patent: 1, 3-8, 10, 12-18, and 21.

21. More specifically, on information and belief, the Defendants’ making, using, offering for sale, and/or selling in the United States, and/or importing into the United States of each of these NAND Flash Memory Products satisfies all elements of at least the aforementioned claims of the ’052 patent, literally and/or under the doctrine of equivalents, as follows:

a. Claim 1 recites "[a] dielectric insulating composite for insulating a floating gate from a control gate in a nonvolatile memory cell, the dielectric insulating composite comprising." Regardless of whether the preamble limits the scope of claim 1, the Defendants' products contain such a dielectric insulating composite.

b. Claim 1 further recites "a bottom layer of silicon dioxide formed on said floating gate." The Defendants' products contain such a bottom layer of silicon dioxide.

c. Claim 1 further recites "a layer of silicon nitride formed on said bottom silicon dioxide layer, said silicon nitride layer having a thickness which is less than said bottom silicon dioxide layer." The Defendants' products contain such a layer of silicon nitride.

d. Claim 1 further recites "a top layer of silicon dioxide formed on said nitride layer, said top silicon dioxide layer having a thickness which is greater than said silicon nitride layer." The Defendants' products contain such a top layer of silicon dioxide.

e. Claim 3 recites "[a] dielectric insulating composite according to claim 1 wherein said bottom silicon dioxide layer has a thickness equal to or less than about 100 A and said top silicon dioxide layer has a thickness equal to or less than about 100 A." The Defendants' products contain such bottom and top silicon dioxide layers.

f. Claim 4 recites "[a] dielectric insulating composite according to claim 3 wherein said bottom and top silicon dioxide layers are formed by high

temperature chemical vapor deposition." The Defendants' products contain such bottom and top silicon dioxide layers.

g. Claim 5 recites "[a] dielectric insulating composite according to claim 3 wherein said silicon nitride layer has a thickness less than about 80 A." The Defendants' products contain such a silicon nitride layer.

h. Claim 6 recites "[a] dielectric insulating composite according to claim 3 wherein said bottom silicon dioxide layer has a thickness between about 25 and 100 A, said silicon nitride layer having a thickness less than about 80 A and said top silicon dioxide layer having a thickness between about 40 and 100 A." The Defendants' products contain such bottom silicon dioxide, silicon nitride, and top silicon dioxide layers.

i. Claim 7 recites "[a] dielectric insulating composite according to claim 6 wherein the capacitively measured effective oxide thickness of said dielectric insulating composite is equal to or less than about 180 A." The Defendants' products contain such an oxide thickness.

j. Claim 8 recites "[a] dielectric insulating composite according to claim 6 wherein said bottom and top silicon dioxide layers are formed by high temperature chemical vapor deposition." The Defendants' products contain such bottom and top silicon dioxide layers.

k. Claim 10 recites "[a] nonvolatile memory cell comprising." Regardless of whether the preamble limits the scope of claim 10, the Defendants' products contain such a nonvolatile memory cell.

l. Claim 10 further recites "a) a first conductivity-type semiconductor substrate." The Defendants' products contain such a semiconductor substrate.

m. Claim 10 further recites "b) source and drain regions formed on a surface of said substrate." The Defendants' products contain such source and drain regions."

n. Claim 10 further recites "c) an insulating layer formed on said source and drain regions." The Defendants' products contain such an insulating layer.

o. Claim 10 further recites "d) a floating gate positioned on said insulating layer." The Defendants' products contain such a floating gate.

p. Claim 10 further recites "e) a dielectric composite positioned on said floating gate, said dielectric composite including a bottom layer of silicon dioxide formed on said floating gate; a layer of silicon nitride formed on said bottom silicon dioxide layer, said silicon nitride layer having a thickness which is less than said bottom silicon dioxide layer; and a top layer of silicon dioxide formed on said nitride layer, said top silicon dioxide layer having a thickness which is greater than said silicon nitride layer." The Defendants' products contain such a dielectric composite.

q. Claim 10 further recites "f) a control gate positioned on said dielectric composite." The Defendants' products contain such a control gate.

r. Claim 12 recites "[a] nonvolatile memory cell according to claim 10 wherein said bottom silicon dioxide layer has a thickness equal to or less than about 100 A and said top silicon dioxide layer has a thickness equal to or less than

about 100 A." The Defendants' products contain such bottom and top silicon dioxide layers.

s. Claim 13 recites "[a] nonvolatile memory cell according to claim 10 wherein the capacitively measured effective oxide thickness of said dielectric insulating composite is equal to or less than about 180 A." The Defendants' products contain such an oxide thickness.

t. Claim 14 recites "[a] nonvolatile memory cell according to claim 12 wherein said bottom and top silicon dioxide layers are formed by high temperature chemical vapor deposition." The Defendants' products contain such bottom and top silicon dioxide layers.

u. Claim 15 recites "[a] nonvolatile memory cell according to claim 10 wherein said silicon nitride layer has a thickness less than about 80 A." The Defendants' products contain such a silicon nitride layer.

v. Claim 16 recites "[a] nonvolatile memory cell according to claim 10 wherein said bottom silicon dioxide layer has a thickness between about 25 and 100 A, said silicon nitride layer having a thickness less than about 80 A and said top silicon dioxide layer having a thickness between about 40 and 100 A." The Defendants' products contain such bottom silicon dioxide, silicon nitride, and top silicon dioxide layers.

w. Claim 17 recites "[a] nonvolatile memory cell according to claim 16 wherein the capacitively measured effective oxide thickness of said dielectric insulating composite is equal to or less than about 180 A." The Defendants' products contain such an oxide thickness.

x. Claim 18 recites "[a] nonvolatile memory cell according to claim 16 wherein said bottom and top silicon dioxide layers are formed by high temperature chemical vapor deposition." The Defendants' products contain such bottom and top silicon dioxide layers.

y. Claim 21 recites "[a] dielectric insulator for insulating a floating gate from a control gate in a nonvolatile memory cell, the dielectric insulator comprising." Regardless of whether the preamble limits the scope of claim 21, the Defendants' products contain such a dielectric insulator.

z. Claim 21 further recites "a bottom silicon dioxide layer formed on said floating gate, a layer of silicon nitride formed on said bottom silicon dioxide layer, said silicon nitride layer having a thickness which is less than said bottom silicon dioxide layer; and a top layer of silicon dioxide formed on said nitride layer, said top silicon dioxide layer having a thickness which is greater than said silicon nitride layer, the dielectric insulator having a capacitively measured effective oxide thickness equal to or less than about 180 A." The Defendants' products contain such bottom silicon dioxide, silicon nitride, and top silicon dioxide layers.

22. Upon information and belief, the Defendants' acts of infringement herein have been made with full knowledge of Macronix's rights in the '052 patent. Such acts constitute willful and deliberate infringement, entitling Macronix to enhanced damages and reasonable attorneys' fees.

23. Upon information and belief, the Defendants' infringing activities have caused and will continue to cause Macronix irreparable injury unless and until enjoined by this Court.

24. As a result of the Defendants' infringing activities, Macronix has suffered and will continue to suffer damages in an amount yet to be determined. Under 35 U.S.C. §§ 283 and 284, Macronix is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT II

(INFRINGEMENT OF THE '772 PATENT)

25. Plaintiff realleges and incorporates herein by reference the allegations in paragraphs 1 – 18 above as if fully set forth herein.

26. Upon information and belief, the Defendants have infringed, and continue to infringe the '772 Patent by making, using, offering for sale, and/or selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '772 Patent, including, but not limited to their S34ML01G1, S34ML02G1, S34ML04G1, S34ML08G1, S34ML01G2, S34ML04G2, S34MS01G1, and S34MS02G1 NAND Flash Memory Products. These products are not materially changed after importation, and these acts of infringement occurred during the term of the process patent. Such infringing products infringe, literally and/or under the doctrine of equivalents, at least the following valid and enforceable claims of the '772 patent: 1, 3-6, and 9.

27. More specifically, on information and belief, the Defendants' making, using, offering for sale, and/or selling in the United States, and/or importing into the United States of each of these NAND Flash Memory Products satisfies all elements of at least the aforementioned claims of the '772 patent, literally and/or under the doctrine of equivalents, as follows:

a. Claim 1 recites "[a] process for fabricating a nonvolatile memory cell comprising." Regardless of whether the preamble limits the scope of claim 1, the Defendants' products include nonvolatile memory cells fabricated by a process.

b. Claim 1 further recites "a) forming source and drain regions on a first conductivity-type semiconductor substrate." The Defendants' products are fabricated by forming such source and drain regions.

c. Claim 1 further recites "b) forming an insulating layer on said source and drain regions." The Defendants' products are fabricated by forming such an insulating layer.

d. Claim 1 further recites "c) forming a floating gate positioned on said insulating layer." The Defendants' products are fabricated by forming such a floating gate.

e. Claim 1 further recites "d) forming a dielectric composite positioned on said floating gate, said dielectric composite including a bottom layer of silicon dioxide formed on said floating gate; a layer of silicon nitride formed on said bottom silicon dioxide layer, and a top layer of silicon dioxide formed on said nitride layer, wherein said silicon nitride layer of said composite has a thickness less than about 80 A and is thinner than said top or said bottom silicon dioxide layer." The Defendants' products are fabricated by forming such a dielectric composite with such bottom and top layers of silicon dioxide and a layer of silicon nitride.

f. Claim 1 further recites "e) forming a control gate positioned on said dielectric composite." The Defendants' products are fabricated by forming such a control gate.

g. Claim 3 recites "[a] nonvolatile memory cell according to claim 1 wherein the capacitively measured effective oxide thickness of said dielectric insulating composite is equal to or less than about 180 A." The Defendants' products are fabricated by forming a nonvolatile memory cell with such an oxide thickness.

h. Claim 4 further recites "[a] process for fabricating a nonvolatile memory cell according to claim 1 wherein said bottom and top silicon dioxide layers are formed by high temperature chemical vapor deposition." The Defendants' products are fabricated by forming such bottom and top silicon dioxide layers by high temperature chemical vapor deposition.

i. Claim 5 further recites "[a] process for fabricating a nonvolatile memory cell according to claim 1 wherein said bottom silicon dioxide layer has a thickness between about 25 and 80 A and said top silicon dioxide layer having a thickness between about 40 and 100 A." The Defendants' products are fabricated by forming such bottom and top silicon dioxide layers.

j. Claim 6 further recites "[a] process for fabricating a nonvolatile memory cell according to claim 5 wherein the capacitively measured effective oxide thickness of said dielectric insulating composite is equal to or less than about 180 A." The Defendants' products are fabricated by forming a dielectric insulating composite with such an oxide thickness.

k. Claim 9 recites "[a] process for fabricating a nonvolatile memory cell comprising." Regardless of whether the preamble limits the scope of claim 9, the Defendants' products include nonvolatile memory cells fabricated by a process.

l. Claim 9 further recites "a) forming source and drain regions on a first conductivity-type semiconductor substrate." The Defendants' products are fabricated by forming such source and drain regions.

m. Claim 9 further recites "b) forming an insulating layer on said source and drain regions." The Defendants' products are fabricated by forming such an insulating layer.

n. Claim 9 further recites "c) forming a floating gate positioned on said insulating layer." The Defendants' products are fabricated by forming such a floating gate.

o. Claim 9 further recites "d) forming a dielectric insulator positioned on said floating gate, said dielectric insulator including a first silicon dioxide layer and a second silicon dioxide layer formed by high temperature chemical vapor deposition on said first silicon dioxide layer." The Defendants' products are fabricated by forming such a dielectric insulator.

p. Claim 9 further recites "e) forming a control gate positioned on said dielectric composite." The Defendants' products are fabricated by forming such a control gate.

28. Upon information and belief, the Defendants' acts of infringement herein have been made with full knowledge of Macronix's rights in the '772 patent. Such acts constitute

willful and deliberate infringement, entitling Macronix to enhanced damages and reasonable attorneys' fees.

29. Upon information and belief, the Defendants' infringing activities have caused, and will continue to cause, Macronix irreparable injury unless and until enjoined by this Court.

30. As a result of the Defendants' infringing activities, Macronix has suffered and will continue to suffer damages in an amount yet to be determined. Under 35 U.S.C. §§ 283 and 284, Macronix is entitled to recover damages, as well as permanent injunctive relief, against further infringing activity.

COUNT III

(INFRINGEMENT OF THE '826 PATENT)

31. Plaintiff realleges and incorporates herein by reference the allegations in paragraphs 1 – 18 above as if fully set forth herein.

32. Upon information and belief, the Defendants have infringed, and continue to infringe, the '826 Patent by making, using, offering for sale, and/or selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '826 Patent, including, but not limited to their S29PL127J, S29PL064J, S29JL064J, S29PL032J, S29JL032J, S29CL032J, S29AL016J, S29CL016J, S29AL008J, S29CD032J, S29CD016J, S29AS016J, S29AS008J, S25FL064K, S25FL116K, S25FL132K, S25FL216K, S25FL208K, and S25FL204K NOR Floating Gate Flash Memory Products. Such infringing products infringe, literally and/or under the doctrine of equivalents, at least the following valid and enforceable claims of the '826 patent: 1, 2, 5, 7, 11-13, 17, and 27-29.

33. More specifically, on information and belief, the Defendants' making, using, offering for sale, and/or selling in the United States, and/or importing into the United States of each of these NOR Floating Gate Flash Memory Products satisfies all elements of at least the aforementioned claims of the '826 patent, literally and/or under the doctrine of equivalents, as follows:

a. Claim 1 recites "[a] floating gate memory cell in a semiconductor substrate including a region having a first conductivity type, the first conductivity type being one of n-type and p-type, and wherein the substrate is coupled to an external reference supply applying a ground potential and a positive supply potential, comprising." Regardless of whether the preamble limits the scope of claim 1, the Defendants' products contain such a floating gate memory cell in a semiconductor substrate.

b. Claim 1 further recites "a first well within the region of the substrate having a second conductivity type, being one of n-type and p-type and different than the first conductivity type." The Defendants' products contain such a first well.

c. Claim 1 further recites "a second well within the first well, having the first conductivity type." The Defendants' products contain such a second well.

d. Claim 1 further recites "a drain within the second well, having the second conductivity type." The Defendants' products contain such a drain.

e. Claim 1 further recites "a source within the second well, having the second conductivity type, and spaced away from the drain to define a channel area

between the drain and the source." The Defendants' products contain such a source and channel area.

f. Claim 1 further recites "a floating gate structure disposed over the channel area and extending substantially from the source to the drain, including a floating gate and a tunnel insulator between the floating gate and the substrate." The Defendants' products contain such a floating gate and tunnel insulator.

g. Claim 1 further recites "a control gate structure over the floating gate, including a control gate and an insulator between the floating gate and the control gate." The Defendants' products contain such a control gate and insulator.

h. Claim 1 further recites "circuits to induce tunneling of electrons out of the floating gate into the channel area of the substrate by applying a positive voltage higher than the supply potential to the second well, a positive voltage to the first well, and a negative voltage to the control gate, while the region of the substrate is grounded." The Defendants' products contain such circuits to induce such tunneling.

i. Claim 2 recites "[t]he floating gate memory cell of claim 1, wherein the first conductivity type is p-type." The Defendants' products contain such a first conductivity type.

j. Claim 5 recites "[a] floating gate memory array on a semiconductor substrate, including a region having a first conductivity type, the first conductivity type being one of n-type and p-type, and wherein the substrate

is coupled to an external reference supply applying a ground potential and a positive supply potential comprising." Regardless of whether the preamble limits the scope of claim 5, the Defendants' products contain such a floating gate memory array on such a semiconductor substrate.

k. Claim 5 further recites "a first well within the region of the substrate having a second conductivity type, being one of n-type and p-type and different than the first conductivity type." The Defendants' products contain such a first well.

l. Claim 5 further recites "a second well within the first well, having the first conductivity type." The Defendants' products contain such a second well.

m. Claim 5 further recites "an array of floating gate memory cells having respective drains, sources, channel areas between the respective sources and drains, floating gates, and control gates over the channel areas, the sources and drains being within the second well, and having the second conductivity type." The Defendants' products contain such an array of floating gate memory cells.

n. Claim 5 further recites "voltage supply circuits to induce F-N tunneling of electrons out of the floating gates into the channel areas of the substrate by applying a positive voltage higher than the supply potential to the second well, a positive voltage to the first well, and a negative voltage to the control gates of selected cells, while the region of the substrate is grounded." The Defendants' products contain such voltage supply circuits to induce such F-N tunneling.

o. Claim 7 recites "[t]he floating gate memory array of claim 5, wherein the first conductivity type is p-type." The Defendants' products contain such a first conductivity type.

p. Claim 11 recites "[t]he floating gate memory array of claim 5, wherein the floating gates of the array of floating gate memory cells are disposed over the respective channel areas and extend substantially between the respective sources and drains." The Defendants' products contain such floating gates.

q. Claim 12 recites "[a] floating gate memory array on a semiconductor substrate, including a region having a first conductivity type, the first conductivity type being one of n-type and p-type, and wherein the substrate is coupled to an external reference supply applying a ground potential and a positive supply potential comprising." Regardless of whether the preamble limits the scope of claim 12, the Defendants' products contain such a floating gate memory array on such a semiconductor substrate.

r. Claim 12 further recites "an isolation well within the region of the substrate having a second conductivity type, being one of n-type and p-type and different than the first conductivity type." The Defendants' products contain such an isolation well.

s. Claim 12 further recites "a plurality of channel wells within the isolation well, having the first conductivity type." The Defendants' products contain such a plurality of channel wells.

t. Claim 12 further recites "a plurality of arrays of floating gate memory cells within respective channel wells in the plurality of channel wells, the memory

cells having respective drains, sources, channel areas between the respective sources and drains, floating gates, and control gates over the channel areas, the sources and drains being within the respective channel wells, and having the second conductivity type." The Defendants' products contain such a plurality of arrays of floating gate memory cells.

u. Claim 13 recites "[t]he floating gate memory array of claim 12, wherein the first conductivity type is p-type." The Defendants' products contain such a first conductivity type.

v. Claim 17 recites "[t]he floating gate memory array of claim 12, wherein the floating gates of the plurality of arrays of floating gate memory cells are disposed over the respective channel areas and extend substantially between the respective sources and drains." The Defendants' products contain such floating gates.

w. Claim 27 recites "[a] method for flash erase of a floating gate memory cell, including a drain, a source, a floating gate and a control gate, on an integrated circuit having a substrate with a first conductivity type, the substrate including an isolation well having a second conductivity type different than the substrate, a channel well within the isolation well having the first conductivity type, and source and drain regions for the cell having the second conductivity type within the channel well, the integrated circuit further including only a supply pin and a ground pin for supplying power to the integrated circuit, the method comprising." Regardless of whether the

preamble limits the scope of claim 27, the Defendants' products perform such a method for flash erase of a floating gate memory cell.

x. Claim 27 further recites "generating a channel well voltage higher than the supply potential on the integrated circuit of a same polarity as that of an external voltage present on the supply pin." The Defendants' products perform such flash erase by generating such a channel well voltage.

y. Claim 27 further recites "applying the channel well voltage to the channel well during flash erase." The Defendants' products perform such flash erase by applying such channel well voltage to the channel well.

z. Claim 27 further recites "generating a control gate voltage on the integrated circuit of an opposite polarity as that of the external voltage present on the supply pin." The Defendants' products perform such flash erase by generating such a control gate voltage.

aa. Claim 27 further recites "applying the control gate voltage to the control gate during flash erase." The Defendants' products perform such flash erase by applying such a control gate voltage.

bb. Claim 28 recites "[t]he method of claim 27, wherein the channel well voltage has a magnitude higher than the external voltage." The Defendants' products perform such flash erase with such channel well voltage.

cc. Claim 29 further recites "[t]he method of claim 27, wherein the control gate voltage is negative." The Defendants' products perform such flash erase with such control gate voltage.

34. Upon information and belief, the Defendants' infringing activities have caused and will continue to cause Macronix irreparable injury unless and until enjoined by this Court.

35. As a result of the Defendants' infringing activities, Macronix has suffered, and will continue to suffer, damages in an amount yet to be determined. Under 35 U.S.C. §§ 283 and 284, Macronix is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT IV

(INFRINGEMENT OF THE '757 PATENT)

36. Plaintiff realleges and incorporates herein by reference the allegations in paragraphs 1 – 18 above as if fully set forth herein.

37. Upon information and belief, the Defendants have infringed, and continue to infringe, the '757 Patent by making, using, offering for sale, and/or selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '757 Patent, including, but not limited to their S70GL02GS, S70GL02GP, S29GL01GS, S29GL01GP, S29GL512S, S29GL512P, S29GL256S, S29GL256P, S29GL128S, S29GL128P, S29PL127J, S29GL064N, S29PL064J, S29GL032N, S29PL032J, S29CL032J, S29CL016J, S70FL01GS, S25FL512S, S25FL256S, S25FL128S, S29CD032J, S29CD016J, S29WS512P, S29WS256P, S29WS128P, S29WS064R, 71WS256PC0, S98WS064RA0, S29NS512P, S71GL032NA0, S71GL064NB0, and S98GL064NB0 NOR Flash Memory products. Such infringing products infringe, literally and/or under the doctrine of equivalents, at least the following valid and enforceable claims of the '757 patent: 1, 2, 4, 5, 7, 8, and 12-14.

38. More specifically, on information and belief, the Defendants' making, using, offering for sale, and/or selling in the United States, and/or importing into the United States of each of these NOR Flash Memory Products satisfies all elements of at least the aforementioned claims of the '757 patent, literally and/or under the doctrine of equivalents, as follows:

a. Claim 1 recites "[a]n integrated circuit memory, comprising." Regardless of whether the preamble limits the scope of claim 1, the Defendants' products contain such an integrated circuit memory.

b. Claim 1 further recites "an array of non-volatile erasable and programmable memory cells, including a plurality of sectors." The Defendants' products contain such an array of non-volatile erasable and programmable memory cells.

c. Claim 1 further recites "a plurality of control inputs for receiving a set of control signals." The Defendants' products contain such a plurality of control inputs.

d. Claim 1 further recites "address inputs for receiving address signals." The Defendants' products contain such address inputs.

e. Claim 1 further recites "data input/outputs for transferring data into and out of the array." The Defendants' products contain such data input/outputs.

f. Claim 1 further recites "command logic, coupled to the plurality of control inputs, and to at least one of the address inputs and the data input/outputs, which detects command sequences at the plurality of control inputs and the at least one of the address inputs and the data input/outputs, indicating operations for the array, including a program operation to program data in the

array, a sector erase operation to erase a sector of the array, a read operation to read data in the array, and a sector lock operation to set a sector lock signal for at least one sector in the array." The Defendants' products contain such command logic.

g. Claim 1 further recites "sector protect logic coupled to the command logic, including non-volatile, sector lock memory which stores the sector lock signal for at least one sector in the array indicating a protect status for a corresponding sector in the array; which inhibits the sector erase and program operations in a particular sector in response to a set sector lock signal corresponding to the particular sector and to a first state of control signals in the set of control signals." The Defendants' products contain such sector protect logic.

h. Claim 1 further recites "erase, program and read circuits responsive to the command logic and the sector protect logic to execute the sector erase, program and read operations, and to execute the sector lock operation." The Defendants' products contain such erase, program and read circuits.

i. Claim 2 recites "[t]he integrated circuit of claim 1, wherein the sector protect logic enables the sector erase and program operations in response to a reset sector lock signal corresponding to the particular sector and to the first state of control signals in the set of control signals." The Defendants' products contain such sector protect logic.

j. Claim 4 recites "[t]he integrated circuit of claim 1, wherein the command sequence detected by the command logic indicating a sector lock operation

includes a multi-cycle command pattern on the at least one of the address inputs and the data input/outputs." The Defendants' products contain such a command sequence.

k. Claim 5 recites "[t]he integrated circuit of claim 4, wherein the multi-cycle command pattern includes a cycle in which an address for a sector to be protected is supplied." The Defendants' products contain such a multi-cycle command pattern.

l. Claim 7 recites "[t]he integrated circuit of claim 1, wherein the integrated circuit receives a supply potential of about five volts or less, and the first state of the set of control signals includes a first control signal having a voltage state less than or equal to the supply potential and a second control signal having a voltage state less than or equal to the supply potential." The Defendants' products contain such an integrated circuit and such first state of the set of control signals.

m. Claim 8 recites "[t]he integrated circuit of claim 7, wherein the voltage states of the first and second control signals in the first state of control signals are high logic levels." The Defendants' products contain such voltage states.

n. Claim 12 recites "[t]he integrated circuit of claim 1, wherein the command logic includes logic which detects a command sequence indicating a sector unlock operation, and including circuits to reset the at least one sector lock signal in the sector lock memory in response to detection of a sector unlock command sequence by the command logic." The Defendants' products contain such command logic and such circuits.

o. Claim 13 recites "[t]he integrated circuit of claim 12, wherein the command sequence detected by the command logic indicating a sector unlock operation includes a multi-cycle command pattern on the at least one of the address inputs and the data input/outputs." The Defendants' products contain such a command sequence.

p. Claim 14 recites "[t]he integrated circuit of claim 13, wherein the multi-cycle command pattern includes a cycle in which an address for a sector to be unlocked is supplied." The Defendants' products contain such a multi-cycle command pattern.

39. Upon information and belief, the Defendants' acts of infringement herein have been made with full knowledge of Macronix's rights in the '757 patent. Such acts constitute willful and deliberate infringement, entitling Macronix to enhanced damages and reasonable attorneys' fees.

40. Upon information and belief, the Defendants' infringing activities have caused and will continue to cause Macronix irreparable injury unless and until enjoined by this Court.

41. As a result of the Defendants' infringing activities, Macronix has suffered and will continue to suffer damages in an amount yet to be determined. Under 35 U.S.C. §§ 283 and 284, Macronix is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT V

(INFRINGEMENT OF THE ’267 PATENT)

42. Plaintiff realleges and incorporates herein by reference the allegations in paragraphs 1 – 18 above as if fully set forth herein.

43. Upon information and belief, the Defendants have infringed, and continue to infringe, the ’267 Patent by making, using, offering for sale, and/or selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the ’267 Patent, including, but not limited to their S70GL02GS, S29GL01GS, S29GL512S, S29GL256S, S29GL128S, S70FL01GS, S25FL512S, S25FL256S, S25FL128S, S29WS064R, S98WS064RA0, S29XS256R, S29XS128R, S29XS064R, S72XS256RE0, S29VS256R, S29VS128R, S29VS064R, S71VS064RB0, S71VS128RB0, S71VS128RC0, S71VS256RC0, S71VS256RD0, and S72VS256RE0 family of NOR Mirror Bit Flash memory products. Such infringing products infringe, literally and/or under the doctrine of equivalents, at least the following valid and enforceable claims of the ’267 patent: 1-8.

44. More specifically, on information and belief, the Defendants’ making, using, offering for sale, and/or selling in the United States, and/or importing into the United States of each of these NOR Mirror Bit Flash memory products satisfies all elements of at least the aforementioned claims of the ’267 patent, literally and/or under the doctrine of equivalents, as follows:

a. Claim 1 recites “[a] memory array architecture, at least comprising.” Regardless of whether the preamble limits the scope of claim 1, the Defendants’ products contain such a memory array architecture.

b. Claim 1 further recites "a plurality of memory cells." The Defendants' products contain such a plurality of memory cells.

c. Claim 1 further recites "a plurality of select transistors connecting to the memory cells, wherein the select transistors include upper block select transistors and lower block select transistors." The Defendants' products contain such a plurality of select transistors.

d. Claim 1 further recites "a plurality of bit lines connecting to the select transistors, wherein odd bit lines connected to the upper block select transistors are located in a first metal layer and even bit lines connected to the lower block select transistors are located in a second metal layer." The Defendants' products contain such a plurality of bit lines.

e. Claim 2 recites "[t]he memory array architecture according to claim 1, wherein the memory cells are selected from the following types of memory cells: read only memory (ROM), programmable read only memory (PROM), erasable programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), Flash EEPROM, nitride ROM (NROM), dual bit ROM and dual bit NROM." The Defendants' products contain one or more of such types of memory cells.

f. Claim 3 recites "[t]he memory array architecture according to claim 1, wherein the upper block select transistors includes a first select transistor and a second select transistor, and the lower block select transistors includes a third select transistor and a fourth select transistor." The Defendants'

products contain such upper block select transistors and lower block select transistors.

g. Claim 4 recites "[t]he memory array architecture according to claim 3, further comprising first, second, third and fourth select lines connecting to each gate terminal of the corresponding first, second, third and fourth transistors, respectively." The Defendants' products contain such select lines.

h. Claim 5 recites "[t]he memory array architecture according to claim 3, wherein each odd bit line is connected to one common source/drain terminal of the first and second select transistors, and each even bit line is connected to one common source/drain terminal of the third and fourth select transistors." The Defendants' products contain such odd bit lines and even bit lines.

i. Claim 6 recites "[t]he memory array architecture according to claim 5, wherein another source/drain terminals of the first, second, third and fourth select transistors are connected to the memory cells." The Defendants' products contain such source/drain terminals.

j. Claim 7 further recites "[t]he memory array architecture according to claim 1, further comprising word lines respectively connected gate terminal of each memory cell." The Defendants' products contain such word lines.

k. Claim 8 recites "[t]he memory array architecture according to claim 1, wherein adjacent bit lines are located in different metal layers." The Defendants' products contain such adjacent bit lines.

45. Upon information and belief, the Defendants' infringing activities have caused, and will continue to cause, Macronix irreparable injury unless and until enjoined by this Court.

46. As a result of the Defendants' infringing activities, Macronix has suffered and will continue to suffer damages in an amount yet to be determined. Under 35 U.S.C. §§ 283 and 284, Macronix is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT VI

(INFRINGEMENT OF THE '324 PATENT)

47. Plaintiff realleges and incorporates herein by reference the allegations in paragraphs 1 – 18 above as if fully set forth herein.

48. Upon information and belief, the Defendants have infringed, and continue to infringe, the '324 Patent by making, using, offering for sale, and/or selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '324 Patent, including, but not limited to the Spansion SPI products in the S25FL Family, including S70FL01GS, S25FL512S, S25FL256S, S25FL128S, S25FL129P, S25FL132K, S25FL064P, S25FL064K, S25FL032P, and S25FL116K. Such infringing products infringe, literally and/or under the doctrine of equivalents, at least the following valid and enforceable claims of the '324 patent: 1, 2, 7, 8, and 15.

49. More specifically, on information and belief, the Defendants' making, using, offering for sale, and/or selling in the United States, and/or importing into the United States of each of these SPI Flash Memory Products satisfies all elements of at least the aforementioned claims of the '324 patent, literally and/or under the doctrine of equivalents, as follows:

a. Claim 1 recites "[a] serial peripheral interface of an integrated circuit, the serial peripheral interface comprising." Regardless of whether the preamble limits the scope of claim 1, the Defendants' products contain such a serial peripheral interface.

b. Claim 1 further recites "a plurality of pins coupled to the integrated circuit, wherein." The Defendants' products contain such a plurality of pins.

c. Claim 1 further recites "the integrated circuit receives an instruction through only one of the plurality of pins." The Defendants' products contain such an integrated circuit.

d. Claim 1 further recites "after receiving the instruction through the only one pin, the integrated circuit receives an address through the plurality of pins in continuity with the receipt of the instruction." The Defendants' products contain such an integrated circuit.

e. Claim 1 further recites "the integrated circuit sends read out data through the plurality of pins." The Defendants' products contain such an integrated circuit.

f. Claim 2 recites "[t]he serial peripheral interface according to claim 1, wherein the plurality of pins includes a first pin, a second pin, a third pin and a fourth pin." The Defendants' products contain such first, second, third, and fourth pins.

g. Claim 2 further recites "the integrated circuit receives the instruction only through one of the first pin, the second pin, the third pin and the fourth pin." The Defendants' products contain such an integrated circuit.

h. Claim 2 further recites "the integrated circuit receives the address through the first pin, the second pin, the third pin and the fourth pin." The Defendants' products contain such an integrated circuit.

i. Claim 2 further recites "the integrated circuit sends the read out data through the first pin, the second pin, the third pin and the fourth pin." The Defendants' products contain such an integrated circuit.

j. Claim 7 recites "[t]he serial peripheral interface according to claim 1, further comprising: a clock pin coupled to the integrated circuit for inputting a plurality of timing pulses." The Defendants' products contain such a clock pin.

k. Claim 7 further recites "wherein the plurality of pins transmit the instruction, the address or the read out data at rising edges, falling edges or both edges of the timing pulses." The Defendants' products contain such plurality of pins.

l. Claim 8 recites "[a] data transmitting method applied to a serial peripheral interface of an integrated circuit, the serial peripheral interface including a plurality of pins, the method comprising the steps of." Regardless of whether the preamble limits the scope of claim 8, the Defendants' products perform such a data transmitting method.

m. Claim 8 further recites "receiving an instruction through only one of the plurality of pins by the integrated circuits." The Defendants' products perform a data transmitting method by receiving such an instruction.

n. Claim 8 further recites "following the instruction received through the only one pin." The Defendants' products perform a data transmitting method by following such an instruction.

o. Claim 8 further recites "receiving an address through the plurality of pins by the integrated circuits." The Defendants' products perform a data transmitting method by receiving such an address.

p. Claim 8 further recites "wherein no other processes occur through the interface between the step of receiving the instruction through only one of the plurality of pins and the step of receiving the address through the plurality of pins." The Defendants' products perform a data transmitting method without such other processes occurring through the interface.

q. Claim 8 further recites "sending read out data through the plurality of pins by the integrated circuit." The Defendants' products perform a data transmitting method by sending such read out data.

r. Claim 15 recites "[t]he method according to claim 8, wherein the integrated circuit further includes further a clock pin coupled to the integrated circuit for inputting a plurality of timing pulses." The Defendants' products perform a data transmitting method with such an integrated circuit.

s. Claim 15 further recites "and the method further comprises the steps of: inputting a plurality of timing pulses by the clock pin." The Defendants' products perform a data transmitting method by such inputting a plurality of timing pulses.

t. Claim 15 further recites "transmitting the instruction, the address or the read out data by the plurality of pins at rising edges, falling edges or both edges of the timing pulses." The Defendants' products perform a data transmitting method by such transmitting.

50. Upon information and belief, the Defendants' infringing activities have caused, and will continue to cause, Macronix irreparable injury unless and until enjoined by this Court.

51. As a result of the Defendants' infringing activities, Macronix has suffered and will continue to suffer damages in an amount yet to be determined. Under 35 U.S.C. §§ 283 and 284, Macronix is entitled to recover damages, as well as permanent injunctive relief, against further infringing activity.

COUNT VII

(INFRINGEMENT OF THE '330 PATENT)

52. Plaintiff realleges and incorporates herein by reference the allegations in paragraphs 1 – 18 above as if fully set forth herein.

53. Upon information and belief, the Defendants have infringed, and continue to infringe, the '330 Patent by making, using, offering for sale, and/or selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '330 Patent, including, but not limited to the Spansion SPI products in the S25FL Family, including S70FL01GS, S25FL512S, S25FL256S, S25FL128S, S25FL129P, S25FL132K, S25FL064P, S25FL064K, S25FL032P, and S25FL116K. Such infringing products infringe, literally and/or under the doctrine of equivalents, at least the following valid and enforceable claims of the '330 patent: 1-4 and 7-11.

54. More specifically, on information and belief, the Defendants' making, using, offering for sale, and/or selling in the United States, and/or importing into the United States of each of these SPI Flash Memory Products satisfies all elements of at least the aforementioned claims of the '330 patent, literally and/or under the doctrine of equivalents, as follows:

a. Claim 1 recites "[a] method for conducting a read operation in an integrated circuit, the method comprising." Regardless of whether the preamble limits the scope of claim 1, the Defendants' products perform such a method for conducting a read operation in an integrated circuit.

b. Claim 1 further recites "receiving a read command." The Defendants' products perform a method for conducting a read operation in an integrated circuit by receiving such a read command.

c. Claim 1 further recites "receiving a first address in a clock cycle after receiving the read command." The Defendants' products perform a method for conducting a read operation in an integrated circuit by receiving such a first address.

d. Claim 1 further recites "receiving a first performance enhancement indicator in a clock cycle immediately after receiving the first address while before starting to send data out, for determining whether an enhanced read operation is to be performed." The Defendants' products perform a method for conducting a read operation in an integrated circuit by such receiving a first performance enhancement indicator.

e. Claim 1 further recites "performing the enhanced read operation, in case of determining that the enhanced read operation is to be performed." The

Defendants' products perform a method for conducting a read operation in an integrated circuit by such performing the enhanced read operation.

f. Claim 2 recites "[t]he method of claim 1, in case the enhanced read operation is performed, data in the integrated circuit are output using a plurality of input/output pins concurrently." The Defendants' products perform a method for conducting a read operation in an integrated circuit by such output of data in the integrated circuit.

g. Claim 3 recites "[t]he method of claim 1, wherein performing the enhanced read operation comprises: receiving a second address after starting to send data out." The Defendants' products perform a method for conducting a read operation in an integrated circuit by such receiving a second address.

h. Claim 3 further recites "receiving a second performance enhancement indicator in a clock cycle immediately after receiving the second address, for determining whether the enhanced read operation is to be performed based upon the second performance enhancement indicator." The Defendants' products perform a method for conducting a read operation in an integrated circuit by such receiving a second performance enhancement indicator.

i. Claim 3 further recites "waiting n clock cycles, where n is an integer, then outputting data in the integrated circuit, the data being associated with the second read address." The Defendants' products perform a method for conducting a read operation in an integrated circuit by such waiting and outputting.

j. Claim 4 recites "[t]he method of claim 1 wherein determining whether the enhanced read operation is to be performed comprises comparing a first bit in the first performance enhancement indicator with a second bit in the first performance enhancement indicator." The Defendants' products perform a method for conducting a read operation in an integrated circuit by such comparing or an equivalent thereof.

k. Claim 7 recites "[t]he method of claim 1, wherein the read command is a page read command and the first address indicates a page to be read." The Defendants' products perform a method for conducting a read operation in an integrated circuit with such a read command and first address.

l. Claim 8 recites "[t]he method of claim 1, wherein the first performance enhancement indicator is received during a waiting period which is just after receiving the first address and before starting to send data out." The Defendants' products perform a method for conducting a read operation in an integrated circuit by such receiving of the first performance enhancement indicator.

m. Claim 9 recites "[a] system for enhanced data read, the system comprising." Regardless of whether the preamble limits the scope of claim 9, the Defendants' products include such a system for enhanced data read.

n. Claim 9 further recites "one or more components configured to." The Defendants' products include such one or more components.

o. Claim 9 further recites "receive a read command." The Defendants' products include one or more components configured for such receiving.

p. Claim 9 further recites "receive a first address in a clock cycle after receiving the read command." The Defendants' products include one or more components configured for such receiving.

q. Claim 9 further recites "receive a first performance enhancement indicator in a clock cycle immediately after receiving the first address while before starting to send data out." The Defendants' products include one or more components configured for such receiving.

r. Claim 9 further recites "determine whether an enhanced read operation is to be performed based upon the first performance enhancement indicator." The Defendants' products include one or more components configured for such determining.

s. Claim 9 further recites "perform the enhanced read operation in case of determining that the enhanced read operation is to be performed." The Defendants' products include one or more components configured for such performing.

t. Claim 10 recites "[t]he system of claim 9, in case the enhanced read operation is performed, data in the integrated circuit are output using a plurality of input/output pins." The Defendants' products include a system for enhanced data read with such output of data in the integrated circuit.

u. Claim 11 recites "[t]he system of claim 9 wherein the one or more components are further configured to: receive a second address." The Defendants' products include one or more components configured for such receiving.

v. Claim 11 further recites "receive a second performance enhancement indicator in a clock cycle immediately after receiving the second address, for determining whether the enhanced read operation is to be performed." The Defendants' products include one or more components configured for such receiving.

w. Claim 11 further recites "waiting n clock cycles, where n is an integer, then outputting data in the memory array in the integrated circuit, the data being associated with the second read address." The Defendants' products include one or more components configured for such waiting and outputting data.

55. Upon information and belief, the Defendants' infringing activities have caused, and will continue to cause, Macronix irreparable injury unless and until enjoined by this Court.

56. As a result of the Defendants' infringing activities, Macronix has suffered and will continue to suffer damages in an amount yet to be determined. Under 35 U.S.C. §§ 283 and 284, Macronix is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

PRAYER FOR RELIEF

WHEREFORE, Macronix respectfully requests that this Court:

(a) Enter judgment that the Defendants have infringed, directly and/or indirectly, one or more claims of the Macronix Patents;

(b) Permanently enjoin the Defendants, and the directors, officers, agents, servants and employees of each of the Defendants, and those acting in concert or

participation with the Defendants from infringing, either directly or indirectly, the Macronix Patents;

(c) Enter a judgment and order permanently enjoining the Defendants and their parent corporations, subsidiaries, and affiliates from making, using, offering for sale, and selling within the United States, and/or importing into the United States, any devices containing infringing products;

(d) Order the Defendants to pay damages to compensate Macronix for Defendants' infringement, including all compensatory damages incurred in this case, including all pre-judgment and post-judgment interest and enhanced damages;

(e) Order an award of reasonable attorneys' fees under 35 U.S.C. § 285;

(f) Award any and all other relief as this Court may deem just and proper.

JURY DEMAND

Plaintiff demands a trial by jury of all issues triable as of right by a jury in this action.

Dated: November 20, 2013

Respectfully submitted,

By: /s/ Charles B. Molster, III

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