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Attorneys for Defendant
CYPRESS SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

CYPRESS SEMICONDUCTOR CORPORATION, Plaintiff, v. GSI TECHNOLOGY, INC., Defendant.	Case No. **COMPLAINT FOR PATENT INFRINGEMENT** **JURY TRIAL DEMANDED**

Plaintiff Cypress Semiconductor Corporation ("Cypress" or "Plaintiff") alleges:

PARTIES

1. Cypress is a corporation organized and existing under the laws of the State of Delaware with its principal place of business located at 198 Champion Court, San Jose, California. Cypress is a supplier of high-performance, mixed-signal, programmable solutions that provide customers with rapid time-to-market and exceptional system value. In addition, and as described in further detail below, Cypress also is an industry-leading supplier of Static Random-Access Memory (SRAM), including high-performance synchronous SRAMs, low-power asynchronous SRAMs, fast asynchronous SRAMs, non-volatile SRAMs, and dual-port SRAMs. Cypress's innovations are used in a wide variety of consumer electronics, such as networking and telecommunication equipment, touchscreen devices, mobile handsets, video and imaging devices, as well as in military communication devices.

2. On information and belief, Defendant GSI Technology, Inc. ("GSI") is a corporation organized and existing under the laws of the State of Delaware and having its principal place of business at 1213 Elko Drive, Sunnyvale, California. As further described below, GSI manufactures SRAM products that infringe multiple Cypress patents.

JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, 35 U.S.C. § 101, *et seq*. This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

4. This Court has personal jurisdiction over GSI and venue is proper in the Northern District of California pursuant to 28 U.S.C. § 1391(b) and (c) and § 1400(b). GSI's principal place of business is in this District, GSI transacts business within this District and GSI offers infringing products for sale in this District. On information and belief, GSI derives significant revenue from the sale of infringing products distributed and used within this district, and/or expects or should reasonably expect its actions to have consequences within this district, and derives substantial revenue from interstate and international commerce. Moreover, GSI has

already subjected itself to the personal jurisdiction of this Court by filing *GSI Technology, Inc. v. Cypress Semiconductor Corp.*, Case No. 11-cv-03613-EJD (N.D. Cal.).

INTRADISTRICT ASSIGNMENT

5. This is an Intellectual Property Action to be assigned on a district-wide basis pursuant to Civil Local Rule 3-2(c).

BACKGROUND

6. For over thirty years, Cypress has been a pioneer and market innovator in the SRAM field. SRAM "chips" are used to store instructions or data that can be read and modified. SRAM storage is generally volatile, meaning it must remain powered-up in order to preserve the instructions or data stored therein. Cypress's SRAM chips are used to store and retrieve data in networking, wireless infrastructure and handsets, computation, consumer, automotive, industrial and other electronic systems. Cypress's high-speed synchronous SRAM products include standard synchronous pipelined, No Bus Latency ("NoBL"), Quad Data Rate™ ("QDR®"), and Double Data Rate ("DDR") SRAMs, which are all typically used in networking applications, as well as industrial, military, and medical electronics.

7. Cypress has a consistent track record of extensive investment in research and development ("R&D"). Cypress's R&D efforts have been essential to its success as a supplier of semiconductor solutions. Cypress's R&D organization works closely with its manufacturing facilities, suppliers and customers to improve semiconductor designs and lower manufacturing costs.

8. The SRAM field historically has been highly competitive, and Cypress's continued success in the SRAM market depends on Cypress's continued dedication to R&D. To protect these critical R&D efforts, Cypress places a high value on its intellectual property. Cypress has applied for and received over 1800 patents in a variety of semiconductor-related technologies, and has over 900 pending patent applications. Of the issued patents, more than 200 are directed towards SRAM technology.

9. On information and belief, Defendant GSI was founded in San Jose, California in March 1995. GSI designs, develops and markets SRAMs primarily for the networking and

telecommunications markets. GSI is a longtime direct competitor of Cypress in the networking SRAM market. GSI and Cypress compete for the same customers and design wins.

10. In contrast to Cypress, on information and belief, GSI has not made any significant investment in the development and protection of intellectual property, holding less than approximately 8 patents. Instead, in order to compete with Cypress, GSI decided to take advantage of Cypress's hard work, including offering certain products that are "pin and function compatible" with Cypress's corresponding QDR® SRAM chips. Through these deliberate efforts, GSI has directly and indirectly infringed multiple Cypress patents.

11. Cypress has already taken steps to halt GSI's infringing acts by filing an action for patent infringement on March 30, 2011, entitled *Cypress Semiconductor Corp. v. GSI Technology, Inc.*, Case No. 11-cv-00789-PJS (D. Minn.), and a complaint with the United States International Trade Commission ("ITC"), *In re Static Random Access Memories and Products Containing Same* (Investigation No. 337-TA-792). As a reaction to Cypress's assertion of its lawful intellectual property rights in the Minnesota and ITC actions, GSI filed an antitrust complaint in this District, *GSI Technology, Inc. v. Cypress Semiconductor Corp.*, Case No. 11-cv-03613-EJD (N.D. Cal.).

12. GSI's antitrust action is meritless and was filed only because Cypress chose to protect its patent rights. Because GSI continues to take advantage of Cypress's hard work on SRAM chips and willfully infringes Cypress's patents without authorization or license, Cypress is filing the instant lawsuit to end GSI's infringement.

GENERAL ALLEGATIONS

13. On May 30, 2000, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,069,839 ("the '839 Patent"), entitled "Circuit and Method for Implementing Single-Cycle Read/Write Operation(s), and Random Access Memory Including the Circuit and/or Practicing the Method," to Cypress. Cypress owns the '839 Patent by assignment. A true and correct copy of the '839 Patent is attached as Exhibit A to this Complaint.

14. On September 18, 2001, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,292,403 ("the '403 Patent"), entitled "Circuit and

Method for Implementing Single-Cycle Read/Write Operation(s), and Random Access Memory Including the Circuit and/or Practicing the Method," to Cypress. Cypress owns the '403 Patent by assignment. A true and correct copy of the '403 Patent is attached as Exhibit B to this Complaint.

15. On May 7, 2002, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,385,128 ("the '128 Patent"), entitled "Random Access Memory Having a Read/Write Address Bus and Process for Writing to and Reading From the Same," to Cypress. Cypress owns the '128 Patent by assignment. A true and correct copy of the '128 Patent is attached as Exhibit C to this Complaint.

16. On September 3, 2002, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,445,645 ("the '645 Patent"), entitled "Random Access Memory Having Independent Read Port and Write Port and Process for Writing to and Reading from the Same" to Cypress. Cypress owns the '645 Patent by assignment. A true and correct copy of the '645 Patent is attached as Exhibit D to this Complaint.

17. On November 22, 2005, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,967,861 ("the '861 Patent"), entitled "Method and Apparatus for Improving Cycle Time in A Quad Data Rate SRAM Device," to International Business Machines Corporation. Cypress owns the '861 Patent by assignment. A true and correct copy of the '861 Patent is attached as Exhibit E to this Complaint.

18. The infringing SRAM parts manufactured by GSI include, but are not limited to, (a) GSI's SigmaQuad product line, such as the SigmaQuad-II, SigmaQuad-II+, and SigmaQuad-III families of products, which include, but are not limited to, parts with the GS79, GS813xx, GS834xx, GS818xx, GS866xx, and GS867xx part numbers, and (b) other products that incorporate similar circuitry and/or have similar features, functionality, and/or architecture (collectively, the "GSI Accused Products"). The identification of products and parts in this Complaint is by way of example only, and on information and belief, the exemplary parts identified in this Complaint are representative of all GSI products and parts with reasonably similar features, functionality and/or architecture, whether discontinued, current or future.

Making, selling, offering for sale, importing, or using any of the GSI Accused Products constitutes direct infringement of one or more claims of the '839, '403, '128, '645, and '861 patents.

19. The GSI Accused Products are designed for specific memory applications and have no substantial non-infringing use.

20. According to GSI's 2012 Annual Report and other publicly available documents, and on information and belief, the GSI Accused Products are sold to end customers in the United States, and through distributors. These end customers and distributors are supplied with datasheets that instruct downstream users how to operate the GSI Accused Products, and GSI supplies such datasheets while knowing that the GSI Accused Products infringe multiple Cypress patents. As detailed by the datasheets and other literature supplied by GSI, the GSI Accused Products infringe multiple Cypress patents. Sale or use of the GSI Accused Products in accordance with the datasheets constitutes direct infringement of the '839, '403, '128, '645, and '861 patents.

21. GSI is aware that the datasheets used by customers for the GSI Accused Products demonstrate infringement of multiple Cypress patents, both through the filing of this Complaint as well as the pleadings in the prior patent infringement lawsuits filed by Cypress against GSI. GSI also advertises that certain of its SigmaQuad parts are "pin and function compatible" with Cypress's corresponding QDR® chips, with the knowledge that Cypress's products incorporate Cypress's proprietary technology, including the inventions disclosed in the '839, '403, '128, '645, and '861 patents.

FIRST CLAIM FOR RELIEF
(Infringement of the '839 Patent)

22. Cypress incorporates and realleges the allegations of the preceding paragraphs as though set forth in full herein.

23. Cypress has not licensed or otherwise authorized GSI to make, use, offer for sale, sell, or import into the United States any products that embody the inventions of the '839 patent.

24. GSI has directly infringed and continues to directly infringe the '839 patent by making, using, importing, offering for sale or selling the GSI Accused Products in the United States.

25. GSI has had actual knowledge of the '839 patent since at least November 15, 2012.

26. GSI has indirectly infringed and continues to indirectly infringe the '839 patent by inducing end-users to infringe the '839 patent by using the GSI Accused Products. GSI intentionally took action that induced end-users to infringe the '839 patent by marketing, selling, and supporting the infringing devices. For example, GSI supplies end customers and distributors of the GSI Accused Products with datasheets that instruct downstream users how to operate the GSI Accused Products, with knowledge that use in accordance with such instructions infringes the '839 patent. As detailed by the datasheets and other literature supplied by GSI, the GSI Accused Products infringe multiple Cypress patents. Sale or use of the GSI Accused Products in accordance with the datasheets constitutes direct infringement of the '839 patent. GSI had awareness of the '839 patent and knew, or was willfully blind to the fact, that its actions would cause direct infringement by end-users.

27. GSI has indirectly infringed and continues to indirectly infringe the '839 patent by contributing to direct infringement by end-users who use the GSI Accused Products. GSI supplied a component whose use by downstream users is infringing; the component is not a common component suitable for non-infringing use; and GSI supplied the component with the knowledge of the '839 patent and knowledge that the component was especially made or adapted for use in an infringing manner.

28. GSI's actions are in violation of one or more of the provisions of 35 U.S.C. § 271.

29. Cypress has been damaged and irreparably injured by GSI's infringing activities and will continue to be so damaged and irreparably injured unless GSI's infringing activities are enjoined by this Court.

30. On information and belief, GSI's infringement has been, and continues to be, willful, wanton, and deliberate, without license or excuse and with full knowledge of the '839 patent.

SECOND CLAIM FOR RELIEF
(Infringement of the '403 Patent)

31. Cypress incorporates and realleges the allegations of the preceding paragraphs as though set forth in full herein.

32. Cypress has not licensed or otherwise authorized GSI to make, use, offer for sale, sell, or import into the United States any products that embody the inventions of the '403 patent.

33. GSI has directly infringed and continues to directly infringe the '403 patent by making, using, importing, offering for sale or selling the GSI Accused Products in the United States.

34. GSI has had actual knowledge of the '403 patent since at least November 15, 2012.

35. GSI has indirectly infringed and continues to indirectly infringe the '403 patent by inducing end-users to infringe the '403 patent by using the GSI Accused Products. GSI intentionally took action that induced end-users to infringe the '403 patent by marketing, selling, and supporting the infringing devices. For example, GSI supplies end customers and distributors of the GSI Accused Products with datasheets that instruct downstream users how to operate the GSI Accused Products, with knowledge that use in accordance with such instructions infringes the '403 patent. As detailed by the datasheets and other literature supplied by GSI, the GSI Accused Products infringe multiple Cypress patents. Sale or use of the GSI Accused Products in accordance with the datasheets constitutes direct infringement of the '403 patent. GSI had awareness of the '403 patent and knew, or was willfully blind to the fact, that its actions would cause direct infringement by end-users.

36. GSI has indirectly infringed and continues to indirectly infringe the '403 patent by contributing to direct infringement by end-users who use the GSI Accused Products. GSI supplied a component whose use by downstream users is infringing; the component is not a common component suitable for non-infringing use; and GSI supplied the component with the

knowledge of the '403 patent and knowledge that the component was especially made or adapted for use in an infringing manner.

37. GSI's actions are in violation of one or more of the provisions of 35 U.S.C. § 271.

38. Cypress has been damaged and irreparably injured by GSI's infringing activities and will continue to be so damaged and irreparably injured unless GSI's infringing activities are enjoined by this Court.

39. On information and belief, GSI's infringement has been, and continues to be, willful, wanton, and deliberate, without license or excuse and with full knowledge of the '403 patent.

THIRD CLAIM FOR RELIEF
(Infringement of the '128 Patent)

40. Cypress incorporates and realleges the allegations of the preceding paragraphs as though set forth in full herein.

41. Cypress has not licensed or otherwise authorized GSI to make, use, offer for sale, sell, or import into the United States any products that embody the inventions of the '128 patent.

42. GSI has directly infringed and continues to directly infringe the '128 patent by making, using, importing, offering for sale or selling the GSI Accused Products in the United States.

43. GSI has had actual knowledge of the '128 patent since at least November 15, 2012.

44. GSI has indirectly infringed and continues to indirectly infringe the '128 patent by inducing end-users to infringe the '128 patent by using the GSI Accused Products. GSI intentionally took action that induced end-users to infringe the '128 patent by marketing, selling, and supporting the infringing devices. For example, GSI supplies end customers and distributors of the GSI Accused Products with datasheets that instruct downstream users how to operate the GSI Accused Products, with knowledge that use in accordance with such instructions infringes the '128 patent. As detailed by the datasheets and other literature supplied by GSI, the GSI Accused Products infringe multiple Cypress patents. Sale or use of the GSI Accused Products in accordance with the datasheets constitutes direct infringement of the '128 patent. GSI had

awareness of the '128 patent and knew, or was willfully blind to the fact, that its actions would cause direct infringement by end-users.

45. GSI has indirectly infringed and continues to indirectly infringe the '128 patent by contributing to direct infringement by end-users who use the GSI Accused Products. GSI supplied a component whose use by downstream users is infringing; the component is not a common component suitable for non-infringing use; and GSI supplied the component with the knowledge of the '128 patent and knowledge that the component was especially made or adapted for use in an infringing manner.

46. GSI's actions are in violation of one or more of the provisions of 35 U.S.C. § 271.

47. Cypress has been damaged and irreparably injured by GSI's infringing activities and will continue to be so damaged and irreparably injured unless GSI's infringing activities are enjoined by this Court.

48. On information and belief, GSI's infringement has been, and continues to be, willful, wanton, and deliberate, without license or excuse and with full knowledge of the '128 patent.

FOURTH CLAIM FOR RELIEF
(Infringement of the '645 Patent)

49. Cypress incorporates and realleges the allegations of the preceding paragraphs as though set forth in full herein.

50. Cypress has not licensed or otherwise authorized GSI to make, use, offer for sale, sell, or import into the United States any products that embody the inventions of the '645 patent.

51. GSI has directly infringed and continues to directly infringe the '645 patent by making, using, importing, offering for sale or selling the GSI Accused Products in the United States.

52. GSI has had actual knowledge of the '645 patent since at least November 15, 2012.

53. GSI has indirectly infringed and continues to indirectly infringe the '645 patent by inducing end-users to infringe the '645 patent by using the GSI Accused Products. GSI intentionally took action that induced end-users to infringe the '645 patent by marketing, selling,

and supporting the infringing devices. For example, GSI supplies end customers and distributors of the GSI Accused Products with datasheets that instruct downstream users how to operate the GSI Accused Products, with knowledge that use in accordance with such instructions infringes the '645 patent. As detailed by the datasheets and other literature supplied by GSI, the GSI Accused Products infringe multiple Cypress patents. Sale or use of the GSI Accused Products in accordance with the datasheets constitutes direct infringement of the '645 patent. GSI had awareness of the '645 patent and knew, or was willfully blind to the fact, that its actions would cause direct infringement by end-users.

54. GSI has indirectly infringed and continues to indirectly infringe the '645 patent by contributing to direct infringement by end-users who use the GSl Accused Products. GSI supplied a component whose use by downstream users is infringing; the component is not a common component suitable for non-infringing use; and GSI supplied the component with the knowledge of the '645 patent and knowledge that the component was especially made or adapted for use in an infringing manner.

55. GSI's actions are in violation of one or more of the provisions of 35 U.S.C. § 271.

56. Cypress has been damaged and irreparably injured by GSI's infringing activities and will continue to be so damaged and irreparably injured unless GSI's infringing activities are enjoined by this Court.

57. On information and belief, GSI's infringement has been, and continues to be, willful, wanton, and deliberate, without license or excuse and with full knowledge of the '645 patent.

FIFTH CLAIM FOR RELIEF
(Infringement of the '861 Patent)

58. Cypress incorporates and realleges the allegations of the preceding paragraphs as though set forth in full herein.

59. Cypress has not licensed or otherwise authorized GSI to make, use, offer for sale, sell, or import into the United States any products that embody the inventions of the '861 patent.

60. On information and belief, GSI has directly infringed and continues to directly

infringe the '861 patent by making, using, importing, offering for sale or selling the GSI Accused Products in the United States.

61. GSI has had actual knowledge of the '861 patent since at least the filing of this Complaint.

62. On information and belief, GSI has indirectly infringed and continues to indirectly infringe the '861 patent by inducing end-users to infringe the '861 patent by using the GSI Accused Products. On information and belief, GSI intentionally took action that induced end-users to infringe the '861 patent by marketing, selling, and supporting the infringing devices. For example, on information and belief, GSI supplies end customers and distributors of the GSI Accused Products with datasheets that instruct downstream users how to operate the GSI Accused Products, with knowledge that use in accordance with such instructions infringes the '861 patent. As detailed by the datasheets and other literature supplied by GSI, on information and belief, the GSI Accused Products infringe multiple Cypress patents. On information and belief, sale or use of the GSI Accused Products in accordance with the datasheets constitutes direct infringement of the '861 patent. On information and belief, GSI had awareness of the '861 patent and knew, or was willfully blind to the fact, that its actions would cause direct infringement by end-users.

63. On information and belief, GSI has indirectly infringed and continues to indirectly infringe the '861 patent by contributing to direct infringement by end-users who use the GSI Accused Products. On information and belief, GSI supplied a component whose use by downstream users is infringing; the component is not a common component suitable for non-infringing use; and GSI supplied the component with the knowledge of the '861 patent and knowledge that the component was especially made or adapted for use in an infringing manner.

64. On information and belief, GSI's actions are in violation of one or more of the provisions of 35 U.S.C. § 271.

65. On information and belief, Cypress has been damaged and irreparably injured by GSI's infringing activities and will continue to be so damaged and irreparably injured unless GSI's infringing activities are enjoined by this Court.

66. On information and belief, GSI's infringement has been, and continues to be, willful, wanton, and deliberate, without license or excuse and with full knowledge of the '861 patent.

PRAYER FOR RELIEF

WHEREFORE, Cypress requests that this Court grant the following relief:

a. Enter judgment that the GSI Accused Products infringe the '839, '403, '128, '645, and '861 patents;

b. Enter an order permanently enjoining GSI and its officers, directors, agents, servants, employees, attorneys, licensees, successors, assigns, and customers, and those in active concert or participation with any of them, from making, using, offering to sell, or selling in the United States or importing into the United States any devices that infringe any claim of the Cypress Patents;

c. Award Cypress its damages, including lost profits, resulting from GSI's infringement in an amount to be determined at trial, pursuant to 35 U.S.C. § 284;

d. Find this to be an exceptional case pursuant to 35 U.S.C. § 285;

e. Award Cypress prejudgment interest and post-judgment interest on its damages and award Cypress its costs;

f. Perform an accounting of GSI's infringing sales not presented at trial and award Cypress additional damages from any such infringing sales; and

g. Award Cypress its costs and attorneys' fees and such other and further relief as the Court deems just and appropriate.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Cypress hereby demands trial by jury on all issues raised by the Complaint.

Dated: May 1, 2013

FISH & RICHARDSON P.C.

By: Frank Scherkenbach/ecf
Frank E. Scherkenbach

Attorneys for Defendant
CYPRESS SEMICONDUCTOR CORPORATION

EXHIBIT A

US006069839A

United States Patent [19]

Pancholy et al.

[11] **Patent Number: 6,069,839**

[45] **Date of Patent: May 30, 2000**

[54] **CIRCUIT AND METHOD FOR IMPLEMENTING SINGLE-CYCLE READ/WRITE OPERATION(S), AND RANDOM ACCESS MEMORY INCLUDING THE CIRCUIT AND/OR PRACTICING THE METHOD**

[75] Inventors: **Ashish Pancholy**, Milpitas; **Cathal G. Phelan**, Mountain View; **Simon J. Lovett**, Milpitas, all of Calif.

[73] Assignee: **Cypress Semiconductor Corp.**, San Jose, Calif.

[21] Appl. No.: **09/238,270**

[22] Filed: **Jan. 27, 1999**

Related U.S. Application Data

[60] Provisional application No. 60/078,718, Mar. 20, 1998.

[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/233**; 365/189.04

[58] **Field of Search** 365/189.04, 233

[56] **References Cited**

U.S. PATENT DOCUMENTS

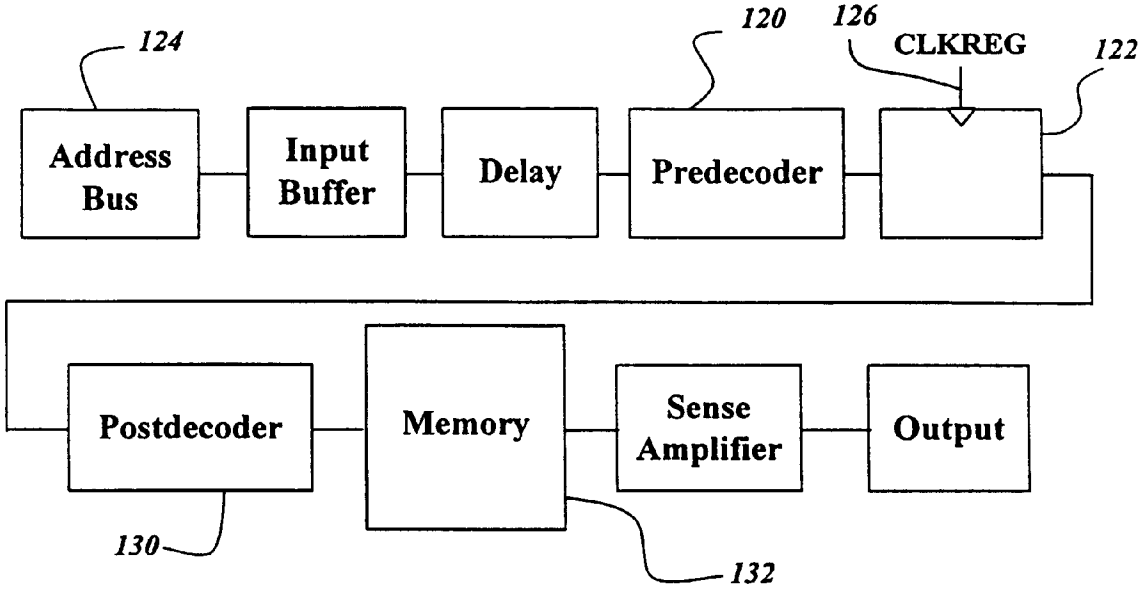
5,530,673 6/1996 Tobita et al. 365/185.09

Primary Examiner—Trong Phan
Assistant Examiner—M. Tran
Attorney, Agent, or Firm—Christopher P. Maiorana, P.C.

[57] **ABSTRACT**

A circuit including an address bus providing random addresses for a random access memory array, and a register configured to receive, store or transfer (i) a first random address from the address bus in response to a first periodic signal transition and (ii) a second random address from the address bus in response to a second periodic signal transition, wherein the first and second periodic signal transitions occur within a single periodic signal cycle, and are preferably complementary to each other. In a further embodiment, the invention concerns a random access memory having an address bus providing random address information for a random access memory array, a predecoder configured to at least partially decode the random address information from the address bus, a register configured to receive, store or transfer (i) a first at least partially decoded random address from the address bus in response to a first periodic signal transition and (ii) a second at least partially decoded random address from the address bus in response to a second periodic signal transition, wherein the first and second periodic signal transitions occur within a single periodic signal cycle; and a postdecoder configured to activate the random addresses in the random access memory in response to receiving the random addresses from the register.

22 Claims, 8 Drawing Sheets



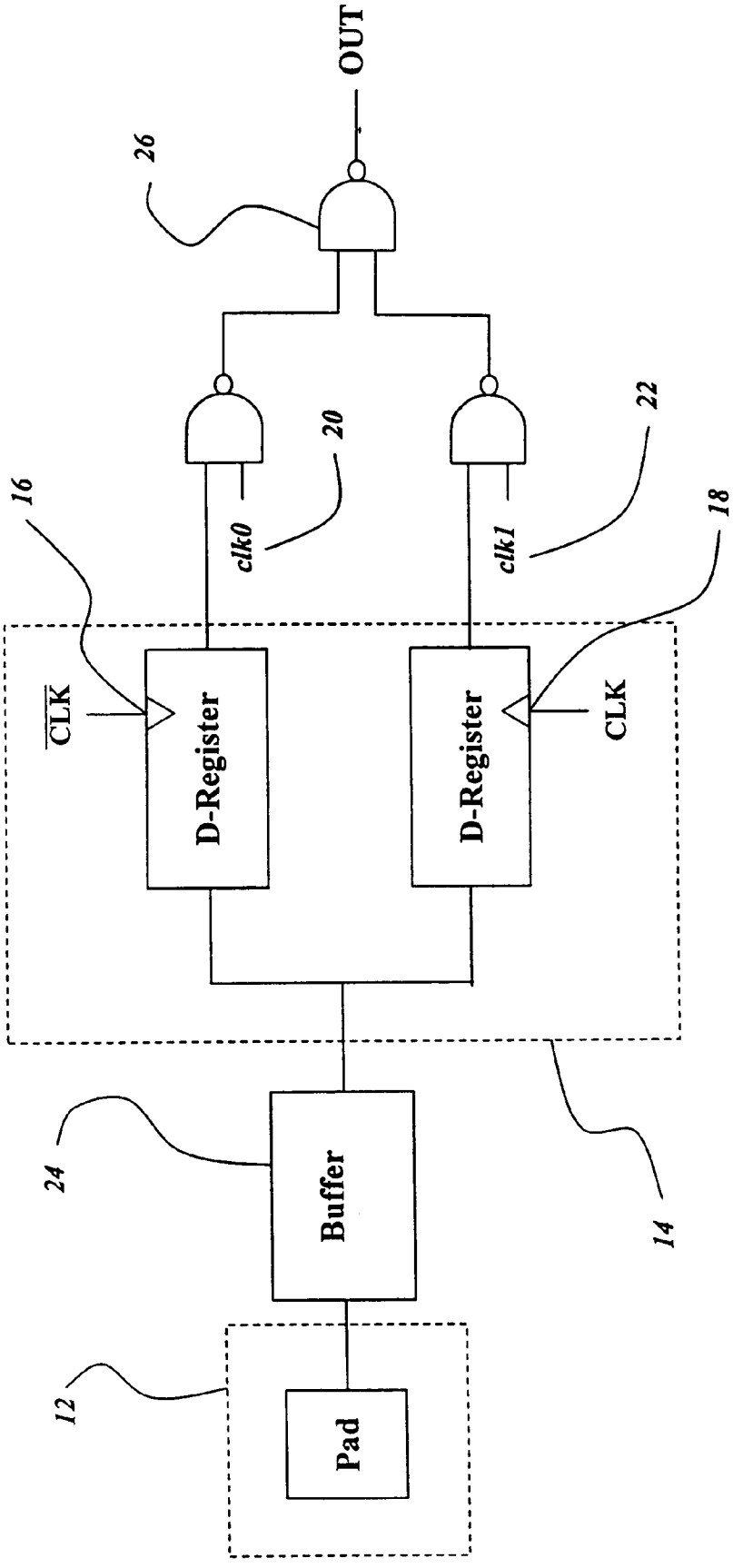


Fig. 1

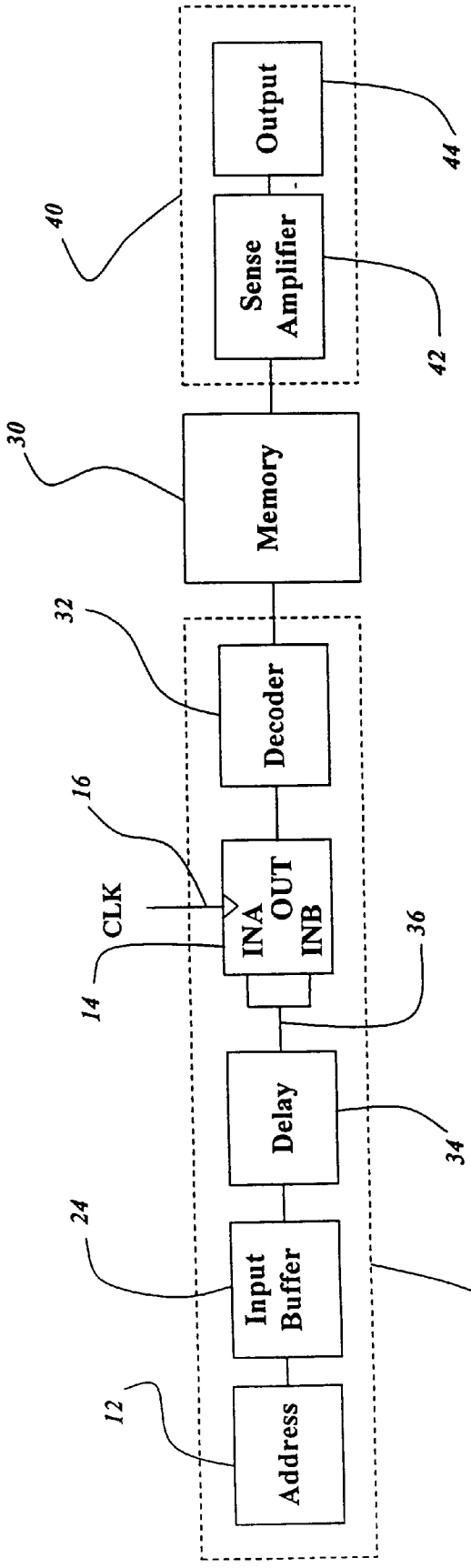


Fig. 2

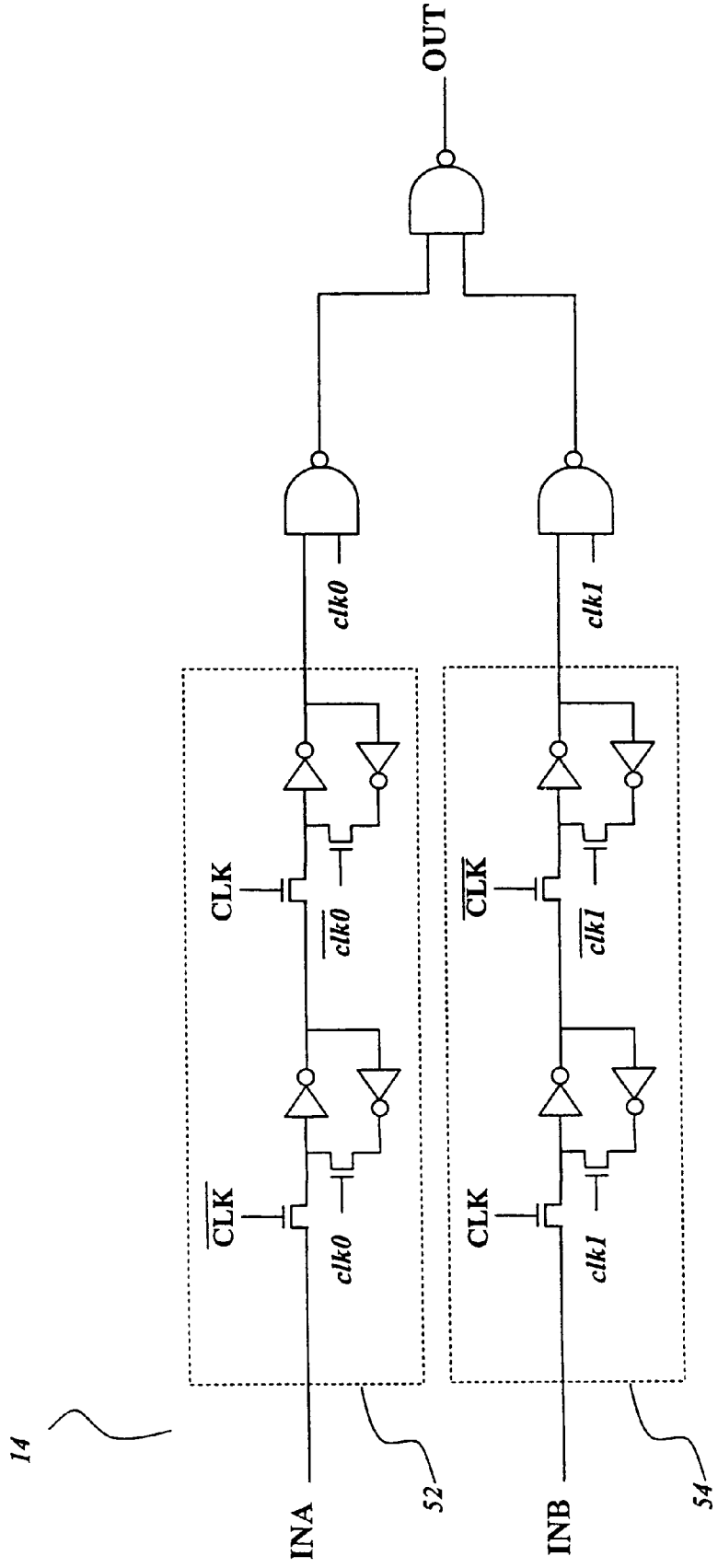


Fig. 3

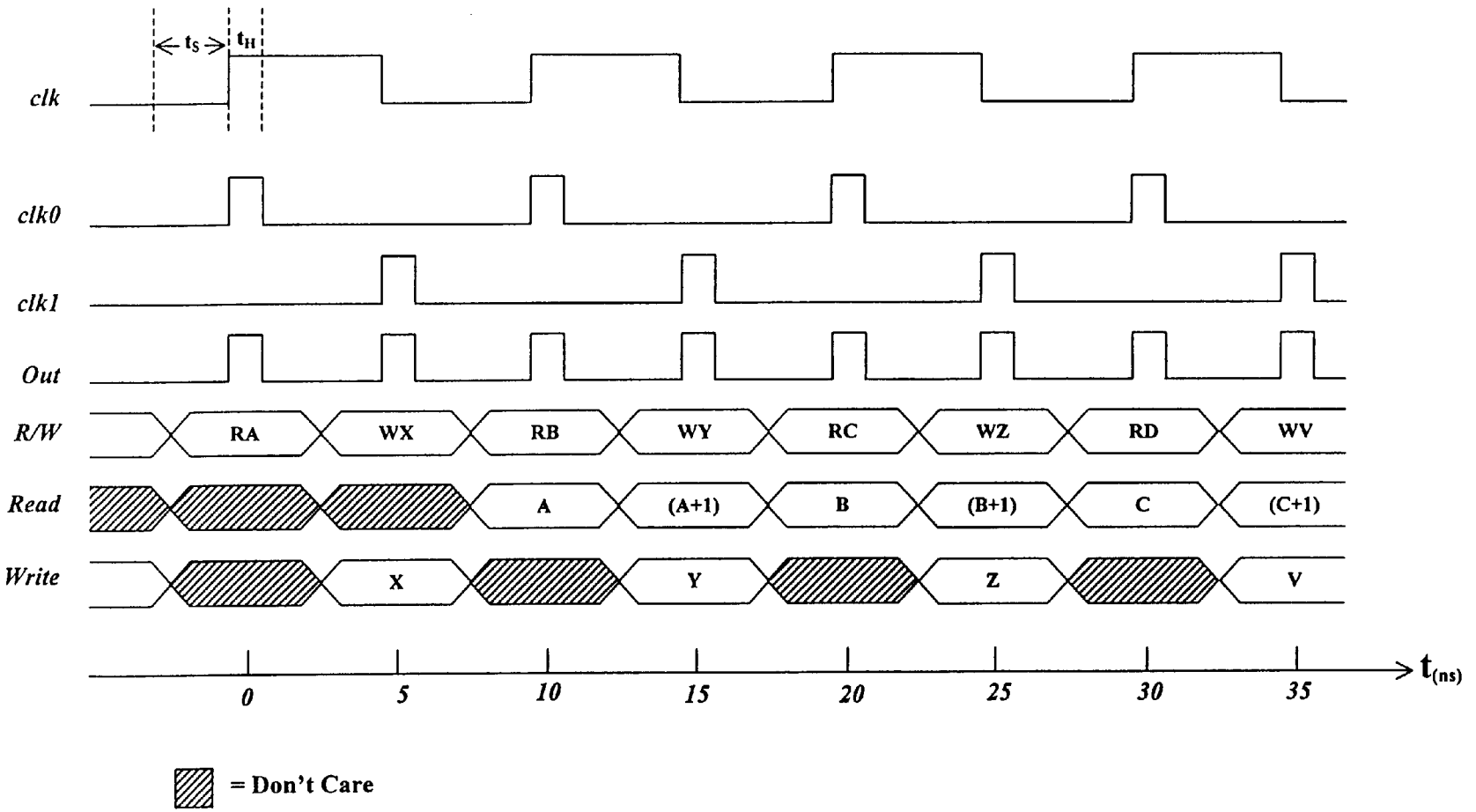


Fig. 4

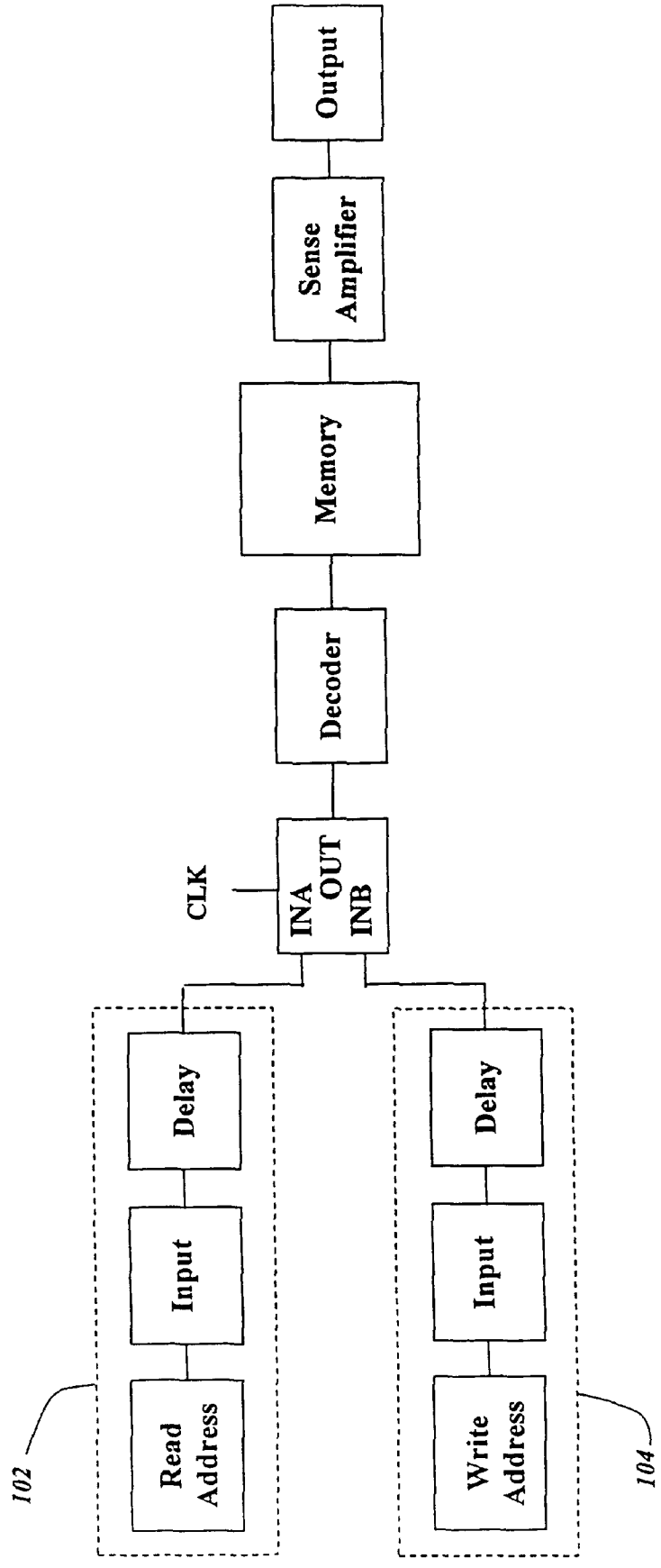


Fig. 5

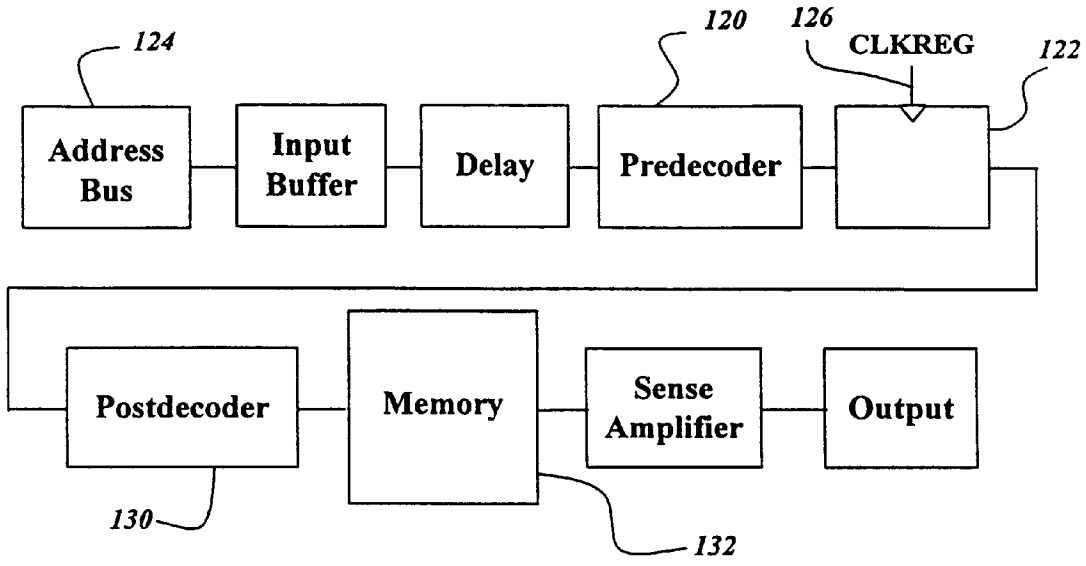


Fig. 6A

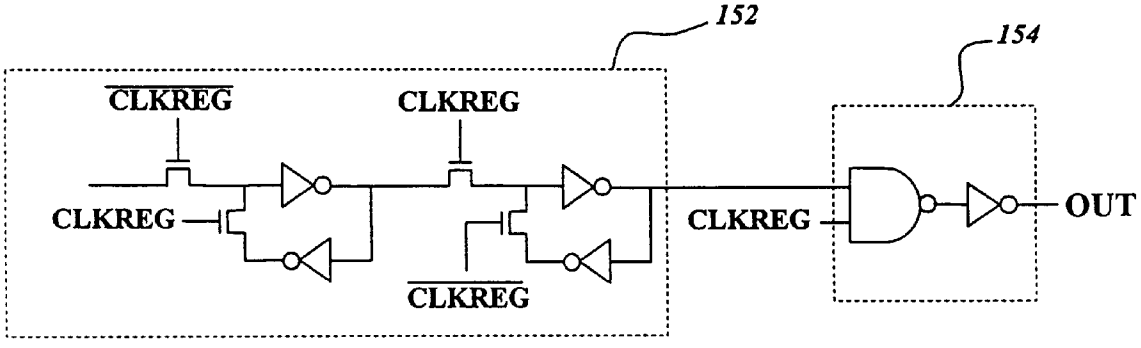


Fig. 6B

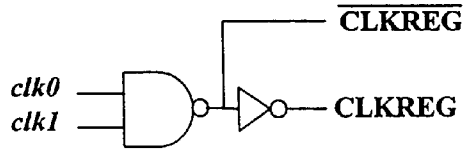


Fig. 6C

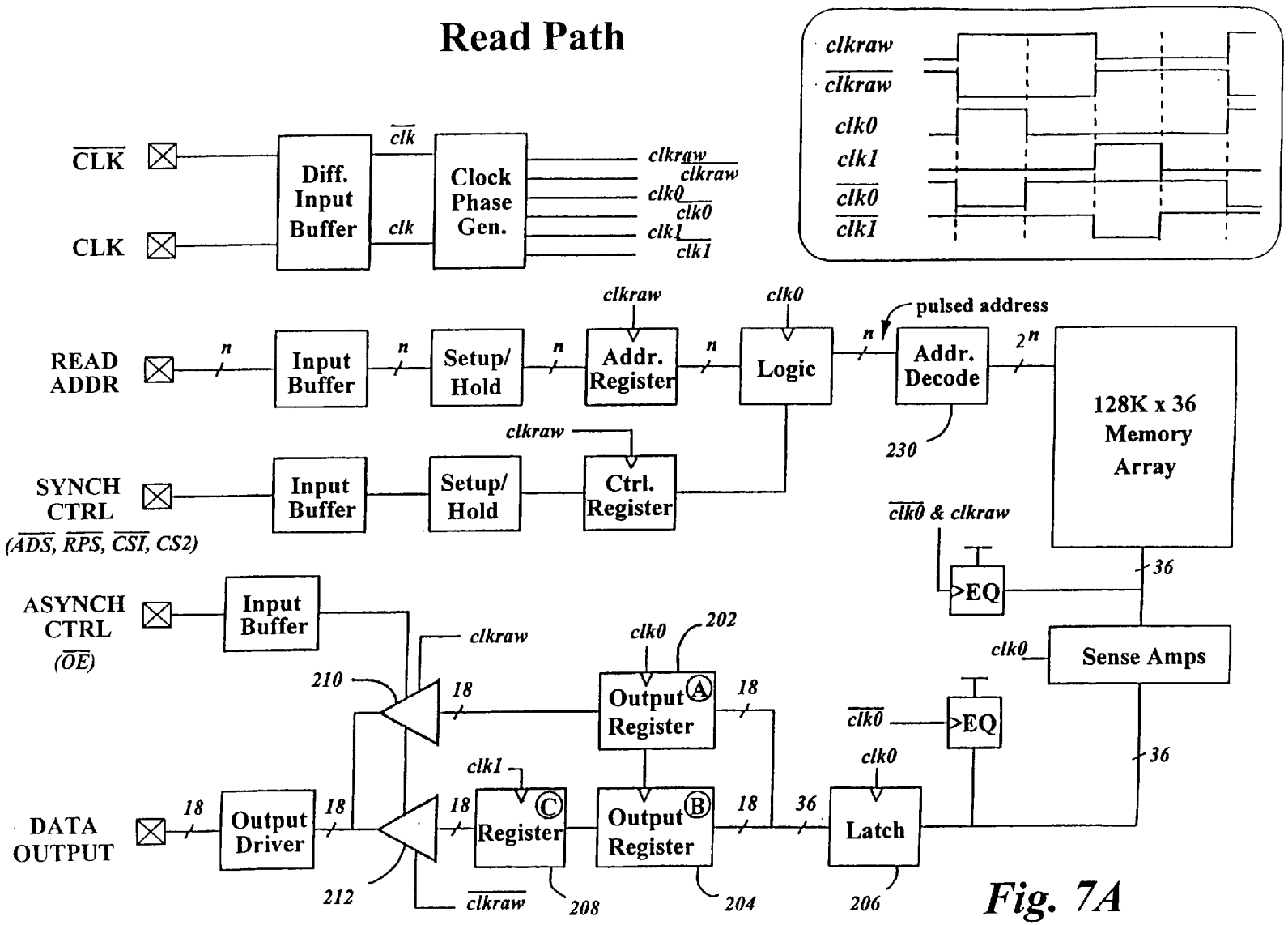


Fig. 7A

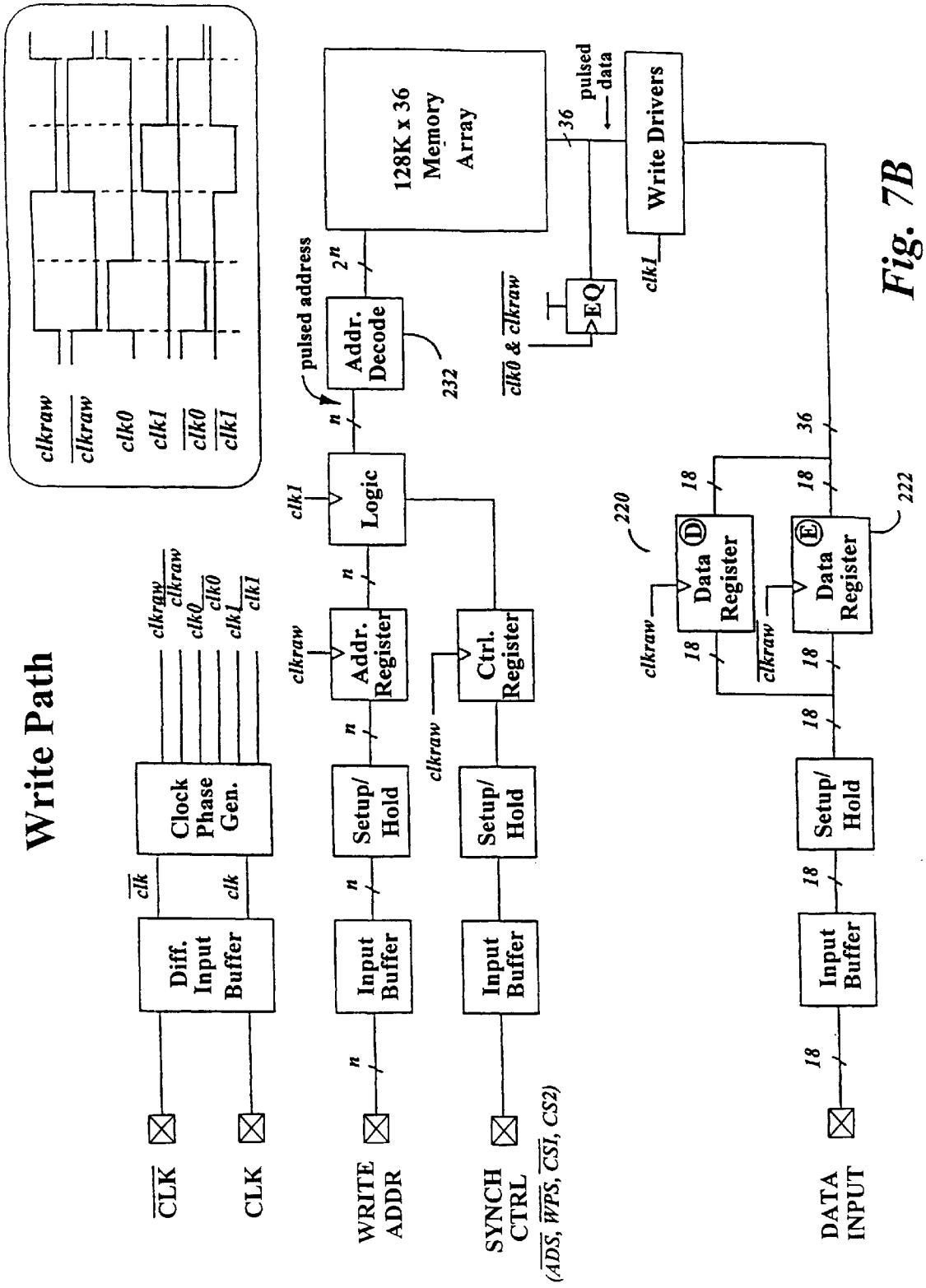


Fig. 7B

CIRCUIT AND METHOD FOR IMPLEMENTING SINGLE-CYCLE READ/WRITE OPERATION(S), AND RANDOM ACCESS MEMORY INCLUDING THE CIRCUIT AND/OR PRACTICING THE METHOD

This application claims the benefit of U.S. Provisional application Ser. No. 60/078,718, filed Mar. 20, 1998.

The invention described and claimed in this application may be related to subject matter described in one or more copending provisional applications entitled, "Random Access Memory And Process For Writing To And Reading From The Same," by Mathew R. Arcoleo, Cathal G. Phelan, Ashish Pancholy, and Simon J. Lovett, identified as Attorney Docket No. CD98022, and/or "Random Access Memory Having Read/Write Address Bus and Process For Writing To And Reading From The Same," by Mathew R. Arcoleo, Cathal G. Phelan, Ashish Pancholy, and Simon J. Lovett, identified as Attorney Docket No. CD98023, both of which were filed in the U.S. Patent and Trademark Office as a provisional patent application on Mar. 13, 1998, both of which are incorporated herein by reference in their entireties.

BACKGROUND OF THE INVENTION

This invention relates generally to the field of semiconductor and/or integrated circuit devices, particularly to a random access memory and process for writing to and reading from the same, and more particularly to a circuit and method for implementing single-cycle read/write operation (s) in a random access memory (RAM).

OBJECTS OF THE INVENTION

The primary object of the invention is to provide a circuit and method that enables reading from and writing to a random access memory in the same clock cycle.

Another object of the invention is to provide a circuit and method that enables reading from and writing to a random access memory in the same clock cycle, using a single read/write address bus or separate read and write address busses.

A further object of the invention is to provide a circuit that latches a new address on each edge, transition or level of a periodic and/or control signal.

A further object of the invention is to provide a random access memory that increases data throughput.

Still yet another object of the invention is to provide such a circuit and/or random access memory that reduces the chip area dedicated to transmitting and/or storing address information.

An even further object of the invention is to provide a random access memory and method of operating the same in which read and write operations may be executed in the same clock cycle.

Yet further objects of the invention include providing such a random access memory and method of operating the same in which fully random addresses may be employed, in which successive and/or asserted addresses may be completely unrelated, and/or in which no restrictions are placed on successive and/or asserted addresses.

Another object of the invention is to provide such a random access memory and method of operating the same in which the same address may be used to read from and write to the memory in the same clock cycle.

A further object of the invention is to provide such a random access memory and method of operating the same in which a periodic signal (e.g., a clock) is the only control-type signal essential to operability.

Other objects and advantages of the present invention will become apparent from the following description, taken in connection with the accompanying drawings, wherein, by way of illustration and example, embodiments of the present invention are disclosed.

SUMMARY OF THE INVENTION

The present invention concerns a circuit comprising an address bus providing random addresses for a random access memory array, and a register configured to store or receive (i) a first random address from the address bus to the random access memory array directly or indirectly in response to a first periodic signal transition and (ii) a second random address from the address bus to the random access memory array directly or indirectly in response to a second periodic signal transition, wherein the second periodic signal transition occurs in the same periodic signal cycle as, and preferably is complementary to, the first periodic signal transition.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings constitute a part of this specification and include exemplary embodiments to the invention, which may be embodied in various forms. The features and advantages of the present invention are illustrated by way of example in the drawings, in which:

FIG. **1** shows an overview of an embodiment of the present address scheme;

FIG. **2** shows an overview of a random access memory (RAM) architecture employing the address scheme shown in FIG. **1**;

FIG. **3** shows a detailed schematic diagram of the address register shown in FIG. **1**;

FIG. **4** shows various waveforms illustrating the relative timing of various signals in conjunction with exemplary read and/or write operations performed according to the invention;

FIG. **5** shows an overview of a random access memory (RAM) architecture employing a second embodiment of the present address scheme;

FIGS. **6**A–**6**C show an overview of a random access memory (RAM) architecture employing a third embodiment of the present address scheme (FIG. **6**A), a detailed schematic diagram of the address register shown in FIG. **6**A (FIG. **6**B), and an exemplary circuit configured to generate one or more pulses for latching address information in the address register shown in FIG. **6**B (FIG. **6**C); and

FIGS. **7**A and **7**B show an overview of a random access memory (RAM) architecture employing a fourth embodiment of the present address scheme, wherein FIG. **7**A shows components useful for conducting one or more read operations, and FIG. **7**B shows components useful for conducting one or more write operations.

It is to be understood that, in some instances, various aspects of the invention may be shown exaggerated or enlarged to facilitate an understanding of the invention, and in other instances, some aspects of the invention considered to be conventional may not be shown so as to avoid obfuscating more important aspects or features of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Detailed descriptions of the preferred embodiments are provided herein. It is to be understood, however, that the

present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure or manner.

In the present random access memory, each of the address bus, address register, data input bus, data output bus, and random access memory array may independently be n or m·n bits wide, where n is an integer ≧2, preferably ≧4, and more preferably ≧8, and m is independently an integer ≧2, preferably of 2–8, and more preferably of 2–4. In specific examples, n may be 8, 9, 16, 18, 32, 36, 64, 72, 128 or 144. The data input bus may receive data from an external source. In a preferred embodiment, each of the data input bus, data output bus, and address bus is unidirectional (i.e., data flows in one direction only).

In the present invention, a "periodic signal" refers to any signal that has an oscillating waveform, the frequency of which may be predicted and/or controlled in accordance with techniques known in the art, and that can be configured to control one or more circuit functions performed as part of a read operation or a write operation in a memory. The periodic signal may be configured to control one or more data transfer operations to or from a random access memory array in response to first and second transitions thereof, respectively, where the second transition occurs within the same periodic signal cycle as, and which may be complementary to, the first transition. Therefore, the memory may operate in a synchronous manner. For synchronous operations, the periodic signal may be an internal or external clock signal, or a periodic control signal such as write enable or output enable. There may be more than one independent periodic signal controlling read, write, register and/or data pass gate functions (e.g., a clock signal and its complement). Where appropriate and/or desirable, the periodic signals comprise a first clock signal and its complement. Alternatively, however, the periodic signal may comprise a pulse generated in response to a clock transition or, alternatively, a predetermined logic or voltage level of a clock signal.

Accesses to and from the memory array, including transmission of address information along an address path to the array, may be controlled by a single input clock or a pair of differential input clocks (CLK/CLK*, where a signal designated "X*" indicates the complement of the corresponding signal "X", similar to the signals in the Figures bearing an overstrike or "bar" designation). In the present application, a "complementary transition" may refer to either the same transition of complementary signals (e.g., the rising edges of both CLK and CLK*), or opposite transitions of the same signal (i.e., the rising and falling edges of CLK). All synchronous timing may be referenced from the cross point of the differential input clock signals. Accesses can be initiated on any edge of any periodic signal (preferably on the rising edge of a clock signal, assuming any other control signals are asserted at their active logic levels), but for ease and simplicity of logic circuitry, accesses to the array are initiated on the rising edge of the positive clock (CLK).

The present random access memory array may be configured to store and/or retrieve data at any random address therein. The address is defined by one or more signals on the address bus.

One (or More) Address Busses

As shown in FIG. **1**, the present invention concerns a circuit comprising an address bus **12** providing random addresses for a random access memory (RAM), and a register **14** configured to store or receive (i) a first random address from the address bus in response to a first periodic signal transition **16** and (ii) a second random address from the address bus in response to a second periodic signal transition **18**, wherein the second periodic signal transition occurs within the same periodic signal cycle as, and preferably is complementary to, the first periodic signal transition. The register may be further configured to transfer or output (i) the first random address to circuitry downstream from the register in the address path of the memory (e.g., a RAM array) in response to a first control signal **20** and (ii) the second random address in response to a second, independent control signal **22**.

As shown in FIG. **1**, the register may comprise two registers (each of which may independently comprise a D-type register, a T-type register, a master-slave register or a latch, but which preferably comprise a master-slave register or a D-type register) configured to store random address information from the address bus in response to the two complementary periodic signal transitions **16** and **18**. Each register may independently further comprise a logic gate **26** configured to output or provide the random address information (or the complement thereof) from the register in response to a periodic signal or pulse **20** or **22**. The periodic signals or pulses **20** and **22** may be independently the same as or different from (i) each other and/or (ii) the periodic signal(s) **16** and/or **18**.

Where the circuit employs two registers, the circuit may further comprise a logic gate **26** configured to provide random address information or its complement (e.g., OUT) from the logic gates receiving the address information stored in the registers. Such logic gates are conventional and known to those skilled in the art, and may comprise and combination of transistors and/or logic elements providing a NAND or AND function (an "AND-type logic gate").

FIG. **2** shows an overview of a random access memory (RAM) architecture employing the circuit shown in FIG. **1**. Thus, the present circuit may further comprise the random access memory **30** and circuitry operable to (i) read data into the random access memory array at the first random address and (ii) write data into the random access memory array at the second random address. The random access memory may further comprise a decoder **32** configured to activate the random address in the random access memory in response to receiving the random address from the register. Address input path **10** may further comprise (i) an input buffer **24** configured to receive random address information from the address bus and provide the random address information to the register, and/or (ii) a delay element **34** interposed between the input buffer **24** and register **14**. Delay element **34** may be configured in accordance with techniques and circuit elements known in the art to set up and hold the address information at node **36** for a length of time sufficient to enable register **14** to store or latch the address information.

Where a decoder located downstream from the address register(s) fully decodes the address information, the length of time for which address information is set up and held (e.g., at node **36**) may be minimized. This allows for greater variations in the periodic signal duty cycle. One notorious limitation to maximizing data throughput in synchronous RAMs is the length of time one must allow for variability in the periodic signal duty cycle, a parameter that effectively limits the maximum frequency of conventional clock circuits. In the present invention, practical limits to the data throughput rate may be determined by the set up and hold

window (e.g., $[t_S+t_H]$; see, for example, the CLK waveform in FIG. **4**) and the pulse widths of the control pulses that latch address information and/or data into a register in the corresponding input or output path (e.g., clk**0**, clk**1**; see FIGS. **3**, **4**, **7**A and **7**B).

The width of a control pulse in the present invention may be, for example, from (1/p) to (1–[1/p]) times the width of a half-cycle of the periodic signal (where p is, for example, from 1.1 to 10, preferably from 1.5 to 4). In the example shown in the waveforms inset into FIGS. **7**A and **7**B, p is about 2. The set up and hold window in the present invention may be, for example, about [(1/q)+(1/r)] times the width of a half-cycle of the periodic signal, where q is, for example, from 0.5 to 10, preferably from 0.75 to 4, and r is independently from 1 to 20, preferably from 1.5 to 10). In the example shown in FIG. **4**, q is 1 and r is 4.

The circuitry operable to write data into the array at a random address may do so in response to at least one transition of the periodic signal. Similarly, the present random access memory may further comprise circuitry operable to read data from a random address in the array may do so in response to at least one transition of the periodic signal. The periodic signal transitions to which the read circuitry and write circuitry respond are preferably, but not necessarily, complementary to each other. For example, when the memory comprises dedicated and/or independent data input and data output ports (see the copending provisional applications identified as Attorney Docket No. CD98022 and/or Attorney Docket No. CD98023), each transition of the periodic signal may be independently designated as a read operation or a write operation. In fact, when the memory comprises two or more independent address registers (and the data busses, data registers and memory array all have the same width), each transition of the periodic signal may be independently designated as a read operation, a write operation or both read and write operations.

The random access memory may further comprise an output path **40**, which may comprise one or more sense amplifiers **42** and one or more data outputs **44**. Each data output **44** may comprise a data bus and an output pad. The output data bus may be unidirectional.

Referring now to FIG. **3**, an exemplary address register operable in the circuits of FIGS. **1** and **2** is shown. The register may comprise two or more subregisters **52** and **54**, each of which may be a D-type or master-slave-type register. The address bus provides random address information one or more inputs to register **14** (e.g., INA and INB). Address information may be received by and/or pass into subregisters **52** and **54** in response to first and second periodic signal transitions, respectively (e.g., CLK* and CLK). As shown in FIG. **3**, the first and second periodic signal transitions may be complementary to each other.

Subregister **52** stores the random address information in response to a first periodic signal transition or pulse (e.g., CLK**0**) and outputs the random address information in response to a second periodic signal transition or pulse (e.g., CLK**0***). As shown in FIG. **3**, the periodic signal transitions or pulses that result in storing and outputting the random address information may be complementary to each other. When pulse generated in response to a rising or falling edge of a periodic signal such as a clock (see, e.g., clk**0** and/or clk**1** in FIG. **4**) controls receive, store, latch and/or output functions in a register, the receive, store, latch and/or output function may be considered to be at least indirectly responsive to a periodic signal transition. Subregister **54** operates in a manner similar to subregister **52**, but in response to different periodic signal transitions or pulses (e.g., CLK**1** and CLK**1***).

In one embodiment, the register stores two read addresses or two write addresses in a single cycle of the periodic signal (e.g., CLK). For example, register **14** stores the first random read address from the address bus in response to a first control pulse (e.g., CLK**0**) and the second random read address from the address bus in response to a second control pulse (e.g., CLK**1**). The control pulses may be generated in response to successive transitions of the periodic signal and/or its complement, such that the control pulses are in effect generated in response to complementary transitions of the periodic signal in a single cycle (see also waveforms CLK, clk**0** and clk**1** in FIG. **4**).

Thus, the present circuit may further comprise a pulse generator configured to generate a first pulse in response to at least one of the first and second transitions of the periodic signal, the first pulse latching at least one of the random addresses into the register. The pulse generator may be further configured to generate a second pulse in response to at least one of the first and second transitions of the same or different periodic signal, the pulse latching at least a second one of the random addresses into the register.

Multiple Registers

In a further embodiment, the present circuit may comprise three or more registers. In such a case, the periodic signal and/or pulse generating logic may further comprise circuitry to provide multiple periodic signals and/or pulses, each offset from the other by a predetermined phase delay in accordance with known techniques and circuits. For example, in an embodiment comprising four registers, conventional phase delay circuitry can generate a second periodic signal phase-offset from the first clock by 90° or t/4 ns, where t is the length of the clock cycle in nanoseconds. Additional control pulses (e.g., clk**2** and clk**3**) can be generated from the edges or transitions of this second, phase-offset clock to control third and fourth address registers in the manner described above. Periodic signals complementary to the second, phase-offset clock and its corresponding control pulses can control other functions in the third and fourth registers, and elsewhere in the RAM for circuitry associated with the third and fourth registers, in a manner similar to that described both above for first and second registers and herein below for associated circuitry.

Transferring Data To and From the Array (Reading and Writing)

FIG. **4** shows the sequence of data transfer events occurring during read and write operations. In FIG. **4**, the letters "A", "B", "C", etc., refer to addresses in the RAM array and the corresponding word or words to be written to or read from such addresses. The terms "RA", "RB", etc., refer to a read function at address A, B, etc. The terms "WX", "WY", etc., refer to a write function at address X, Y, etc. The terms "clk**0**" and "clk**1**" refer, for example, to the control pulses that latch address information in address register **14** as shown in FIG. **3**. the signal "OUT" refers to the output signal from the address register(s) and associated logic circuitry (if present) shown, for example, in FIGS. **1**–**3**. The term "R/W" refers to read or write address information that may be stored in the address register(s) shown, for example, in FIGS. **1**–**3**. Although the clock pulse CLK shown in FIG. **4** is a 125 MHz clock with a cycle time of 4 ns, a clock of any frequency (e.g., from 10 kHz to 10 GHz, preferably from

200 kHz to 4 GHz, more preferably from 1 MHz to 1 GHz) may be used. Examples of suitable clock frequencies include 12.5 MHz, 20 MHz, 25 MHz, 33 MHz, 50 MHz, 66 MHz, 75 MHz, 83 MHz, 100 MHz, 125 MHz, 133 MHz, 150 MHz, 166 MHz, 183 MHz, 200 MHz, 250 MHz, 333 MHz, etc.

Referring now to FIG. **4**, at time t=0 ns, address A is latched or written into the address register from the address bus by pulse clk0. As described above, pulse clk0 may be generated from the positive clock CLK transition from LOW to HIGH. Address A is present on the address bus at a time about t_S ns before the rising CLK transition. This is commonly known in the art as the "setup time". Address A is maintained on the address bus for a period of time of about (t_S+t_H) ns (the "setup and hold time"; see, e.g., waveform CLK in FIG. **4**). For a read operation, a read port select signal (see, e.g., "RPS*" in FIG. **7**A) may be asserted briefly (and preferably while the periodic signal(s) CLK and/or CLK* is/are transitioning at t=0 ns). The next rising transition of the periodic signal CLK, optionally in conjunction with a control pulse (e.g., clk0 and/or clk0*), senses the data at address A and latches the corresponding data word(s) from address A in the array through one or more (optional) latches **206** into one or more output registers (e.g., **202** and **204** in FIG. **7**A).

For either two n-bit-wide data words or one 2n-bit-wide data word stored in the array but output on an n-bit-wide data output bus, the HIGH logic level of CLK resulting from this initial transition at t=0 ns enables output buffer **210** and outputs a first n-bit-wide data word from address A to the data output bus. For n-bit-wide circuitry, a complementary transition of the periodic signal (e.g., a falling CLK transition or a rising CLK* transition) may then latch a second n-bit-wide data word from output register **204** into a shadow register (e.g., register **208** in FIG. **7**A). The LOW logic level of CLK resulting from this complementary CLK transition enables output buffer **212** and outputs the second n-bit-wide data word (e.g., "(A+1)", "(B+1)", "(C+1)", etc.) onto the data output bus and the data output pad(s).

In FIG. **4**, at time t=2 ns, address X is latched or written into the address register from the address bus by pulse clk**1**. As described above, pulse clk**1** may be generated from either (i) the negative clock CLK* transition from LOW to HIGH or (ii) the positive clock CLK transition from HIGH to LOW. Address X is also present on the address bus at a time about t_S ns before the rising CLK transition. Address X is also maintained on the address bus for a period of time of about (t_S+t_H) ns (the "setup and hold time"; see, e.g., waveform CLK in FIG. **4**). For a write operation, a write port select signal (see, e.g., "WPS*" in FIG. **7**B) may be asserted briefly (and preferably while the periodic signal(s) CLK and/or CLK* is/are transitioning at t=2 ns). This complementary transition of the periodic signal CLK/CLK*, optionally in conjunction with a control pulse (e.g., clk**1** and/or clk**1***), writes data stored in one or more data input registers (see, e.g., **220** and **222** in FIG. **7**B) into the array at address X.

More specifically, a rising periodic signal CLK transition latches an n-bit-wide data word D(X) on the Data In bus into the first write register **220**. Alternatively, for 2n-bit-wide circuitry, the rising transition of the positive periodic signal CLK latches a single 2n-bit-wide data word in a single 2n-bit-wide data input register. Similar but complementary to the read operation described immediately above, address X is latched or written into the address register from the address bus during the second, falling CLK transition from HIGH to LOW. The new address signal, or address transition from A to X, occurs at least about t_S ns before the crossover of the differential external clocks CLK and CLK* (see FIGS. **4** and **7**B). The falling transition of the CLK pulse, which may be sent on a clock generator-to-address register bus, enables the address register to store the X address that is on the address bus after the address transition.

Advantages

The RAM may access two data words with each read operation on the same clock edge as that which latches the read address. For example, referring to FIG. **7**A, the first or lower word of data may be driven onto the output data bus on the clock logic level resulting from the single clock edge that latches the data in the corresponding output register, provided any applied output control signal (e.g., an output enable signal OE) is asserted in an enabling state (e.g., LOW). On the subsequent clock transition, the second or higher order data word may be driven onto the output data bus on the clock logic level resulting from the clock transition that latches the second data word in the shadow register **208**, provided any applied output control signal remains asserted in an enabling state. In this configuration, all data may be available, for example, as soon as 5.5 or 6 ns after a clock rise (assuming a 125 MHz clock signal), thus providing a read operation with as little as one cycle of latency.

On the same transitions of the subsequent clock cycle, the next data word(s) stored in the array is/are latched in the output register(s), then driven through one or more (three-state) output buffers onto the data output bus/pads on the same clock logic levels as before. Read accesses can be initiated, for example, on every rising edge of the positive clock. Doing so will "pipeline" the data flow such that data is transferred out of the device on every rising and falling edge of the clock.

When deselected (e.g., in a multiple-RAM system configuration), the present RAM may first complete the pending read transactions. Synchronous internal circuitry may automatically three-state the outputs following the next rising edge of the positive clock. This will allow for a seamless transition between a port in the present RAM and any external device (including without limitation a second RAM according to the invention) without the insertion of wait states.

The input and output ports in the present RAM architecture (e.g., DATA OUTPUT in FIG. **7**A and DATA INPUT in FIG. **7**B) may operate independently of one another. One can read or write to any location in the memory array, regardless of the transaction address on the other port. Should the input and output ports access the same location on the same cycle of the periodic signal, the information presented to the data inputs may be forwarded to the data outputs (by, e.g., conventional bypass logic circuitry responsive to a control signal generated in response to an AND-type logic comparison of the read and write addresses), or alternatively, the data stored in the output register may first be output on the data output bus, then the same location written with the new data.

Two (or More) Address Busses

In a further embodiment, the present invention may comprise first and second address input paths **102** and **104**, as shown in FIG. **5**. More specifically, the circuit may further comprise a second address bus providing (i) a third random address in response to a first transition of the same or different periodic signal and (ii) a fourth random address in

response to a second transition of the same or different periodic signal; and a second register configured to store (i) the third random address from the second address bus in response to a third control pulse and (ii) a fourth random address from the second address bus in response to a fourth control pulse different from the third control pulse, the third and fourth control pulses being the same as or different from the first and second control pulses. Such a circuit may also further comprise a first and a second input buffer configured to receive first and second random address information from the first and second address busses, respectively, and to provide the first and second random address information to the first and second

The present address bus and/or circuit may comprise a read address bus and an independent write address bus. In such a case, the register may comprise (a) a read register configured to store (i) first random read address information from the read address bus in response to a first transition of a first periodic signal and (ii) second random read address information from the read address bus in response to a second transition of the first periodic signal, and (b) a write register configured to store (i) first random write address information from the write address bus in response to a first transition of a second periodic signal and (ii) second random write address information from the write address bus in response to a second transition of the second periodic signal, the first and second periodic signals being the same or different.

Predecoding

In a further embodiment, as shown in FIG. **6A**, the present invention may further concern a predecoder **120** configured to at least partially decode the random address information from the address bus **124** prior to storing the at least partially decoded random address information in the register **122**. Consequently, the register may be configured to store (i) a first at least partially decoded random address from the address bus in response to a first periodic signal transition (e.g., at input **126**) and (ii) a second at least partially decoded random address from the address bus in response to a second periodic signal transition, wherein the second transition is complementary to the first transition. The address input circuit and/or RAM may also further comprise a postdecoder **130** configured to activate the random addresses in the RAM array **132** in response to receiving the random addresses from the register.

Because some decoding is done prior to synchronously storing the address information, this embodiment may maximize the amount of time available to write data to and/or read data from the array. Maximizing the array "cycle time" (i.e., the amount of time to write data to and read data from the array) provides opportunities to increase wordline and/or bitline recovery times, thus reducing power and/or current consumption. It may also permit one to employ a larger array without requiring additional and/or more sophosticated logic circuitry, and/or to implement pulsed or self-resetting logic.

Suitable descriptions and examples of predecoder and postdecoder circuitry can be found in copending application Ser. No. 08/575,554 (entitled, "Method and Apparatus for Reducing Skew Among Input Signals Within an Integrated Circuit," filed Dec. 20, 1995) and in copending application Ser. No. 08/575,555 (entitled, "Method and Apparatus for Reducing Skew Among Input Signals and Clock Signals Within an Integrated Circuit," filed Dec. 20, 1995; abandoned in favor of continuing prosecution application Attorney Docket No. 016820.P128C, filed on Oct. 30, 1997). For example, a predecoder may decode from j to k bits of an m-bit-wide address, and the postdecoder may decode the remaining bits of the m-bit-wide address, where j, k and m are each an integer such that $j<k<m$, preferably such that $j \geqq 1$, 2 or 3; $k \leqq m-1$, $m-2$, or $m-3$; and m is at least 4, preferably at least 8, and more preferably at least 10.

The Single Register

In a further embodiment, and as exemplified in FIG. **6B**, the address input circuit may comprise a single register **152** (e.g., per address bit), which may replace register **14** in FIGS. **1** and **2**. Optionally, to better ensure compliance with timing parameters, the register may provide an output through a sinlge logic element **154**. As shown in FIG. **6C**, control signals and/or pulses for latching address information in and outputting address information from the register (e.g., CLKREG and CLKREG*) may be generated from pulses generated from transitions of a periodic signal (e.g., CLK**0** and CLK**1**; see FIGS. **3** and **4**). A logic gate providing a NOR or OR function (an "OR-type logic gate") is adequate for generating control signals and/or pulses for this single-register embodiment. Consequently, register **152** operates in essentially the same manner as register **14** in FIG. **3**.

The Detailed RAM Architecture

As shown in FIGS. **7A** and **7B**, the present random access memory (RAM) architecture may further comprise separate first and second ports (e.g., "DATA OUTPUT" [FIG. **7A**] and "DATA INPUT" [FIG. **7B**]) to access the memory array. The ports may be unidirectional, in which case each pair of ports (e.g., an input/output pair) may have a dedicated address bus.(e.g., "READ ADDR [FIG. **7A**] and WRITE ADDR" [FIG. **7B**]), in accordance with the emdominent described above for "Two (or More) Address Busses." Each data port and address path may comprise n inputs, a buffer or driver, and an n-bit register (as described above), where n is an integer of one or more, to maintain complete independence of the ports and their associated control logic. Separate data inputs and outputs eliminates the need to "turn around" the data bus as may be required with common or bidirectional I/O devices.

Accesses to the array through input and output ports may be somewhat independent of one another and are initiated synchronously with one or more periodic signals (e.g., an internal or external clock signal; a set of differential input clocks; etc.). In order to maximize data throughput, the input port transfers data on one of the rising or falling edges or during one of the sustained logic levels of the periodic signal cycle(s), and the output port transfers data on the other of the rising or falling edges or sustained logic levels of the periodic signal cycle(s). As described herein, data transfer may also be logic level-triggered; i.e., it may occur in response to a particular or predetermined logic level of one or more periodic signal(s).

The depth of the memory array may be, in effect, expanded with two or more arrays and/or independent RAM devices (e.g., integrated circuit chips), and their associated select logic circuitry. The control signals carried by such logic circuitry (e.g., port select inputs) allow each port to operate as if it was an independent device, thereby further allowing depth expansion independently on each port.

All synchronous data inputs may be passed through one or more write registers (or input registers) controlled by the periodic signal(s). All data outputs may be passed through one or more read registers (and/or output registers), also controlled by the same or different periodic signal(s).

All writes may be conducted with on-chip synchronous self-timed write circuitry to simplify the interface logic.

Example(s)

As shown in FIGS. **7**A and **7**B, the present RAM architecture is, in a preferred embodiment, configured as a synchronous pipelined burst static RAM (SRAM). Data may flow unidirectionally into the SRAM through the Data In bus, and/or unidirectionally out through the Data Out bus. Each bus may have its own pads for receiving or transmitting external signals. The present RAM array receives address information on a read address bus or a write address bus and may store or latch the address information in an address register. By separating the data input and data output ports, the present RAM avoids possible data contention and/or eliminates any need to "turn-around" the data bus.

All data inputs may pass through one or more n- or 2n-bit-wide input registers (e.g., n-bit-wide registers **220** and **222** as shown in FIG. **7**B), controlled by the rising or falling edge of a positive input clock (e.g., clkraw, generated from the crossover of differential input clocks CLK and CLK*). In the 2n-bit-wide input register case, the data input bus may have the same width as the input register(s).

The present random access memory may comprise one or more arrays (e.g., "128K×36") configured to store and/or retrieve data at a random read and/or write address therein. The arrays are generally oriented in rows and columns, where the nuimber of rows may be from 1 to 2^x+c, preferably from 4 to 2^x+c, and more preferably from 16 to 2^x+c, where x may be an integer of from 2 to 15, preferably from 3 to 14, and more preferably from 4 to 12, and c represents the number of redundant rows, which may be an integer of from 0 to 12, preferably from 0 to 8, and more preferably from 0 to (2^x/8), and the number of columns may independently be from 1 to 2^y+d, preferably from 4 to 2^y+d, and more preferably from 8 to 2^y+d, where y may be an integer of from 0 to 10, preferably from 2 to 9, and more preferably from 3 to 8, and d represents the number of redundant columns, which may be an integer of from 0 to 8, preferably from 0 to 4, and more preferably from 0 to (2^y/8).

The address is defined by n signals on the address bus, where n is an integer of one or more, preferably 3 or more and more preferably of from 5 to 2^y+d, where y and d are as defined above. Address information reaches the array from the address register through an address decoder **230** (FIG. **7**A) or **232** (FIG. **7**B), the signals from which identify the location(s) in the array where an operation is to be performed. The array, which may be n or m·n bits wide, preferably has the same total width as the total width of the input register(s) and/or the data input bus.

The present random access memory may further comprise an output data register, which may also be n or m·n bits wide, and may have the same width as the total width of the input register(s), the array, and/or the data input bus. Preferably, the data output bus is also n or m·n bits wide, more preferably the same width as the data input bus, the input register(s), the array, and/or the output register(s). The output port (e.g., DATA OUTPUT" in FIG. **7**A) may further comprise a plurality of pads for providing the data externally.

When the random access memory comprises a plurality of arrays, the first random access memory array may receive data from a first data input bus and/or write data register, and the second random access memory array may receive data from a second data input bus and/or write data register. Similarly, a random access memory comprising a plurality of arrays may further comprise a plurality of data output busses and/or read data registers, the first and second read data registers respectively storing data transferred from the first and second random access memory arrays, and the first and second data output busses respectively transmitting data from the first and second random access memory arrays or read data registers. In this case, each random access memory array may further comprise (a) first circuitry operable to write data to the random access memory array(s) at a first random address and (b) second circuitry operable to read data from the random access memory array(s) at a second random address, each in response to successive transitions or logic levels of a periodic signal, the second random address being the same as or different from the first random address. Each array may also have a unique address bus for providing both read and write address information.

As shown in FIG. **7**A, the present random access memory may further comprise an n-bits-wide data output bus, first and second (three-state) output buffers (e.g., buffers **210** and **212**), and first, second and third n-bits-wide output registers (e.g., **202**, **204** and **208**), wherein:

- each of the first and second output registers store data from the output register in response to a first periodic signal transition or level,
- the third output register stores data from the first output register in response to a second, complementary periodic signal transition or level,
- the first output buffer is enabled to provide data to the output data bus from the third output register by a third periodic signal transition or level (which may be [i] the same as or different from the second, complementary periodic signal transition or level, or [ii] a complement of the first periodic signal transition or level, and which preferably enables data output when in a particular or predetermined logic level or state), and
- the second output buffer is enabled to provide data to the output data bus from the second output register in response to a fourth periodic signal transition or level (which may be [i] the same as or different from the first periodic signal transition or level or [ii] a complement of the second periodic signal transition or level, and which also preferably enables data output when in a particular or predetermined logic level or state).

Control inputs (e.g., "SYNCH CTRL" and "ASYNCH CTRL" in FIG. **7**A, "SYNCH CTRL" in FIG. **7**B) may comprise one or more synchronous or synchronous external control signals. Such control signals may include one or more data input or write port select signals WPS or WPS*, one or more data output or read port select signals RPS or RPS*, a conventional asynchronous output enable signal (see OE* in FIG. **7**A), one or more conventional chip select signals (for multiple RAM applications; see, e.g., CS**1*** and/or CS**2** in FIGS. **7**A and **7**B), one or more address strobe or validity signals (e.g., "ADS*" in FIGS. **7**A and **7**B), etc. Synchronous external control signals may pass along the same or similar input path as address information, including passing through a control input register controlled by an edge or logic level of a periodic signal (e.g., clkraw).

One may advantageously employ multiple port select signals (e.g., WPS**1**, WPS**2**, WPS**1***, WPS**2***, RPS**1**, RPS**2**, RPS**1***, RPS**2***, etc.) when one includes multiple random access memories in a given application (e.g., a data, voice and/or video communications device, such as a network switch or router). Preferably, each RAM in a given multiple-RAM application has at least one unique combination of read and at write port select signals that activate the par-

ticular port (e.g., WPS1* and WPS2, WPS1 and WPS2*, RPS1* and RPS2, RPS1 and RPS2*, etc.). Alternatively, the different input and/or output port select signals can select (enable or disable) one read or write register of a multiple-register configuration.

The RAM shown in FIGS. 7A and 7B may further comprise one or more conventional logic circuits configured to control and/or gate the passage of address information to an address (post)decoder in response to a periodic signal and/or control pulse (e.g., clk0 [see FIG. 7A] or clk1 [see FIG. 7B]); one or more sense amplifiers interposed between the memory array and the output latch and/or output register (s); conventional sense line equalization circuitry, which may equalize one or more 2n-bit-wide busses, and which may respond to one or more periodic signals and/or control pulses (e.g., clkraw and/or clk0*; see FIG. 7A); one or more n- or 2n-bit-wide output latches which may latch output data is response to one or more periodic signals and/or control pulses (e.g., clk0; see FIG. 7A), which in turn may be the same as or different from the periodic signals and/or control pulses that latch output data into the output register(s); one or more write drivers interposed between the data input register(s) and the memory array, which may be configured to write data into the array in response to a periodic signal and/or control pulse (e.g., clk1 [see FIG. 7B]); conventional bitline equalization circuitry, which may equalize a predetermined number of bitlines and which may respond to one or more periodic signals and/or control pulses (e.g., clkraw* and/or clk1*; see FIG. 7B); one or more differential clock input buffers and one or more clock phase generators to generate the periodic signal(s) and/or control pulse(s) from the signal(s) output from the differential clock input buffer (s).

While the invention has been described in connection with certain preferred embodiments, it is not intended to limit the scope of the invention to the particular form set forth, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A circuit comprising:

an address bus providing random addresses for a random access memory array; and

a register configured to store (i) a first random address from the address bus directly or indirectly in response to a first periodic signal transition and (ii) a second random address from the address bus directly or indirectly in response to a second periodic signal transition, wherein the first and second periodic signal transitions occur within a single periodic signal cycle and are complementary transitions of a single periodic signal or are similar transitions of complementary periodic signals.

2. A circuit as claimed in claim 1 wherein said second periodic signal transition is complementary to said first periodic signal transition.

3. A circuit as claimed in claim 1 wherein said periodic signal comprises a member selected from the group consisting of (a) a clock signal and (b) a pulse generated in response to a clock signal transition.

4. A circuit as claimed in claim 1 further comprising:

said random access memory; and

circuitry operable to (i) read data into said random access memory array at said first random address and (ii) write data into said random access memory array at said second random address.

5. A circuit as claimed in claim 4 wherein said address bus comprises a read address bus, said circuit further comprises an independent write address bus, and said register comprises:

a read register configured to store (i) first random read address information from said read address bus in response to a first transition of a first periodic signal and (ii) second random read address information from said read address bus in response to a second transition of said first periodic signal; and

a write register configured to store (i) first random write address information from said write address bus in response to a first transition of a second periodic signal and (ii) second random write address information from said write address bus in response to a second transition of said second periodic signal, said first and second periodic signals being the same or different.

6. A circuit as claimed in claim 1 wherein said address bus provides a first random address to said register during one of said first and second periodic signal transitions, and said circuit further comprises a second address bus providing a second random address to said register during the remaining one of said first and second periodic signal transitions.

7. A circuit as claimed in claim 6 further comprising:

a first input buffer configured to receive first random address information from said first address bus and provide said first random address information to said register; and

a second input buffer configured to receive second random address information from said second address bus and provide said second random address information to said register.

8. A circuit as claimed in claim 7 further comprising

a second register configured to store said second random address information directly or indirectly in response to third and fourth periodic signal transitions, wherein the third and fourth periodic signal transitions occur within said single periodic signal cycle and are the same as or different from said second and first periodic signal transitions, respectively.

9. A circuit as claimed in claim 8 wherein:

said first register further comprises a first logic gate configured to provide said first random address information or its complement from said first register in response to a second periodic signal; and

said second register further comprises a second logic gate configured to provide said second random address information or its complement from said second register in response to a third periodic signal,

said second and third periodic signals being independently the same as or different from (i) each other and/or (ii) said first periodic signal.

10. A circuit as claimed in claim 9 wherein said second periodic signal transition is a first pulse signal generated in response to said first periodic signal transition, and said third periodic signal is a second pulse signal generated in response to a transition complementary to said first periodic signal transition.

11. A circuit as claimed in claim 1 wherein:

said address bus provides (i) a first random read address in response to said first periodic signal transition and (ii) a second random read address in response to said second periodic signal transition;

said register stores (i) said first random read address from said address bus in response to a first control pulse and

(ii) said second random read address from said address bus in response to a second control pulse different from said first control pulse; and

said circuit further comprises:

a second address bus providing (i) a first random write address in response to said first periodic signal transition and (ii) a second random write address in response to said second periodic signal transition; and

a second register configured to store (i) said first random write address from said second address bus in response to a third control pulse and (ii) a second random write address from said second address bus in response to a fourth control pulse different from said third control pulse, said third and fourth control pulses being the same as or different from said first and second control pulses.

12. A circuit as claimed in claim **11** wherein said third and fourth control pulses are complementary to said first and second control pulses, respectively.

13. A circuit as claimed in claim **1** further comprising a logic gate configured to provide random address information or its complement from said register in response to a third periodic signal transition, said third periodic signal transition being the same as or different from said first and second periodic signal transitions.

14. A circuit as claimed in claim **13** wherein said address register comprises a master-slave type register.

15. A circuit as claimed in claim **1** further comprising a pulse generator configured to generate a first pulse in response to at least a first transition of a periodic signal, said first pulse latching at least one of said random addresses into said register.

16. A circuit as claimed in claim **15** wherein said pulse generator is further configured to generate a second pulse in response to at least a second transition of said periodic signal, said pulse latching at least a second one of said random addresses into said register.

17. A circuit as claimed in claim **1** further comprising an input buffer configured to receive random address information from said address bus and provide said random address information to said register.

18. A random access memory, comprising

the circuit as claimed in claim **1**; and

a decoder configured to activate said random address in said random access memory in response to receiving said random address from said circuit.

19. A circuit as claimed in claim **1** wherein said register is further configured to transfer (i) said first random address to said random access memory array in response to a first control signal and (ii) said second random address to said random access memory array in response to a second, independent control signal.

20. A circuit as claimed in claim **1** wherein said register is further configured to transfer said first and second random address from the address bus to said random access memory array within a single periodic signal cycle.

21. A random access memory, comprising

an address bus providing random address information for a random access memory array;

a predecoder configured to at least partially decode said random address information from said address bus;

a register configured to store (i) a first at least partially decoded random address from said address bus in response to a first periodic signal transition and (ii) a second at least partially decoded random address from said address bus in response to a second periodic signal transition, wherein said first and second periodic signal transitions occur within a single periodic signal cycle; and

a postdecoder configured to activate said random addresses in said random access memory in response to receiving said random addresses from said register.

22. A random access memory as claimed in claim **21** wherein said second periodic signal transition is complementary to said first periodic signal transition.

* * * * *

EXHIBIT B

US006292403B1

(12) **United States Patent**
Pancholy et al.

(10) **Patent No.: US 6,292,403 B1**
(45) **Date of Patent: *Sep. 18, 2001**

(54) **CIRCUIT AND METHOD FOR IMPLEMENTING SINGLE-CYCLE READ/WRITE OPERATION(S), AND RANDOM ACCESS MEMORY INCLUDING THE CIRCUIT AND/OR PRACTICING THE METHOD**

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(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/521,190**

(22) Filed: **Mar. 7, 2000**

Related U.S. Application Data

(63) Continuation of application No. 09/238,270, filed on Jan. 27, 1999.
(60) Provisional application No. 60/078,718, filed on Mar. 20, 1998.

(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/189.05**; 365/233
(58) **Field of Search** 365/189.05, 233

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,169,284	9/1979	Hogan et al.	364/200
4,245,304	1/1981	Porter et al.	364/200
4,456,965	6/1984	Graber et al.	364/900
4,539,661	9/1985	Oritani	365/230
4,575,826 *	3/1986	Dean	365/222
4,599,708	7/1986	Schuster	365/189
4,783,732	11/1988	Morton	364/200
4,849,937	7/1989	Yoshimoto	365/189.05
4,882,709	11/1989	Wyland	365/189.02
5,023,838	6/1991	Herbert	365/189.08
5,309,395	5/1994	Dickinson et al.	365/189.04

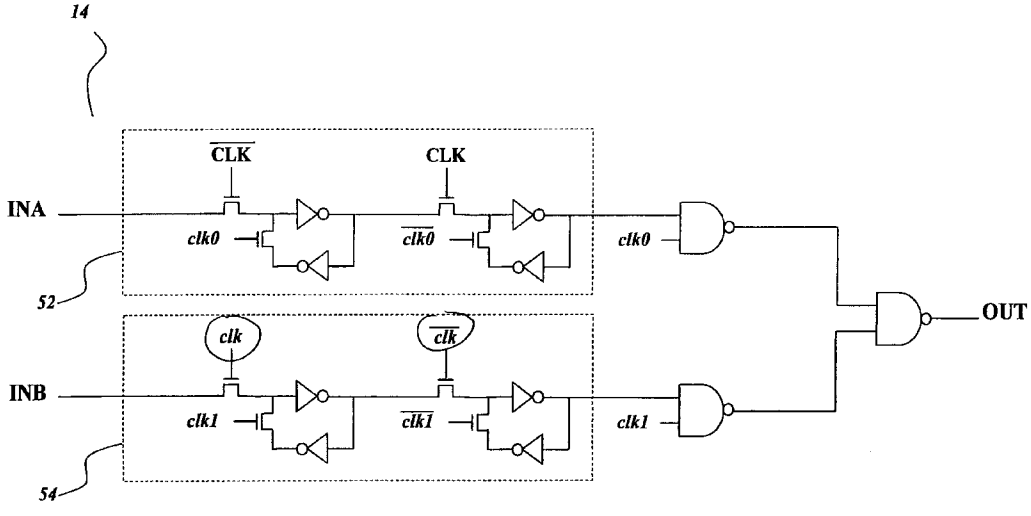
(List continued on next page.)

Primary Examiner—David Nelms
Assistant Examiner—M. Tran
(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana, P.C.

(57) **ABSTRACT**

A circuit including an address bus providing random addresses for a random access memory array, and a register configured to receive, store or transfer (i) a first random address from the address bus in response to a first periodic signal transition and (ii) a second random address from the address bus in response to a second periodic signal transition, wherein the first and second periodic signal transitions occur within a single periodic signal cycle, and are preferably complementary to each other. In a further embodiment, the invention concerns a random access memory having an address bus providing random address information for a random access memory array, a predecoder configured to at least partially decode the random address information from the address bus, a register configured to receive, store or transfer (i) a first at least partially decoded random address from the address bus in response to a first periodic signal transition and (ii) a second at least partially decoded random address from the address bus in response to a second periodic signal transition, wherein the first and second periodic signal transitions occur within a single periodic signal cycle; and a postdecoder configured to activate the random addresses in the random access memory in response to receiving the random addresses from the register.

20 Claims, 8 Drawing Sheets



U.S. PATENT DOCUMENTS

5,394,361		2/1995	Dickinson	365/189.04
5,440,717		8/1995	Bosshart	395/486
5,530,673		6/1996	Tobita et al.	365/185.09
5,546,569		8/1996	Proebsting et al.	395/550
5,561,781		10/1996	Braceras et al.	395/458
5,598,545		1/1997	Childers et al.	395/562
5,638,534		6/1997	Mote, Jr.	395/485
5,648,987	*	7/1997	Yang et al.	375/232
5,752,270		5/1998	Wada	711/169
5,828,606		10/1998	Mick	365/189.05
5,838,631		11/1998	Mick	365/233
5,841,732		11/1998	Mick	365/233
5,875,151		2/1999	Mick	365/233
5,926,426		7/1999	Han	365/205
5,983,328		11/1999	Potts et al.	711/157
6,069,839	*	5/2000	Pancholy et al.	365/233
6,081,478		6/2000	Mick et al.	365/233
6,094,399		7/2000	Mick	365/233

* cited by examiner

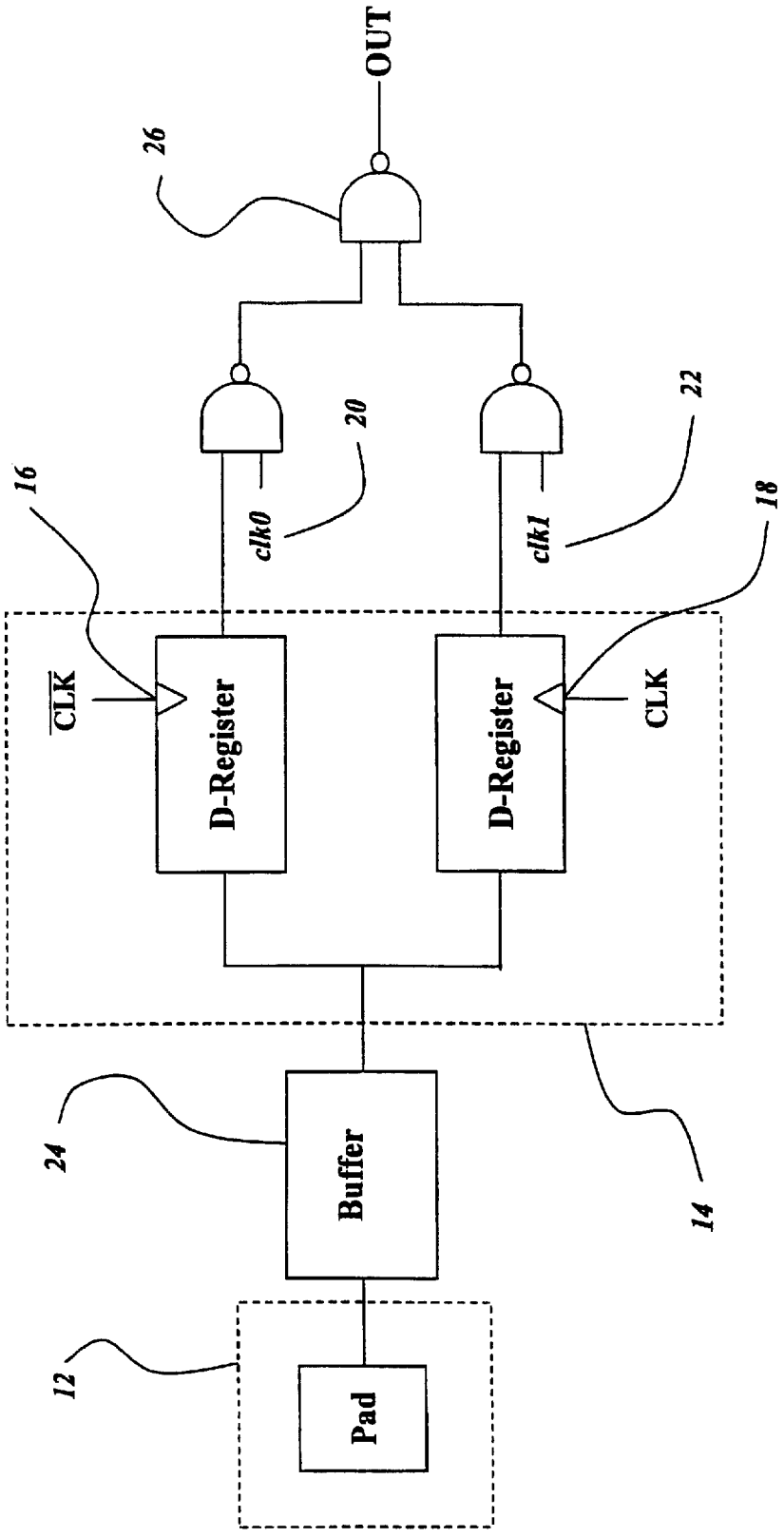


Fig. 1

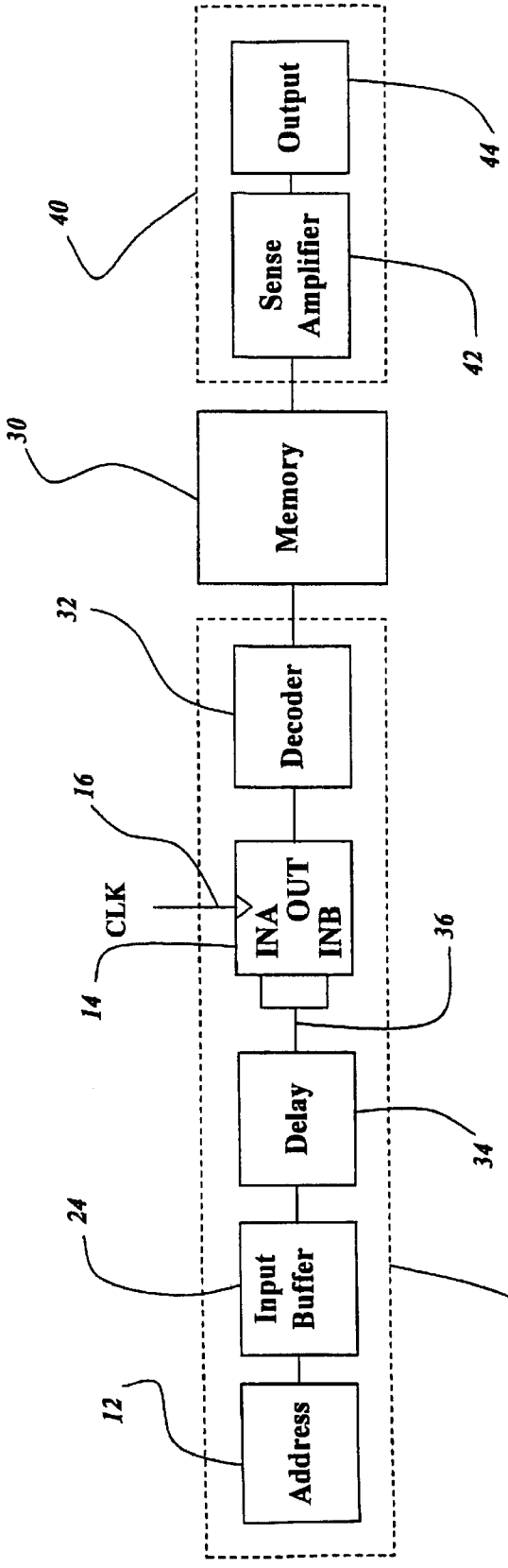


Fig. 2

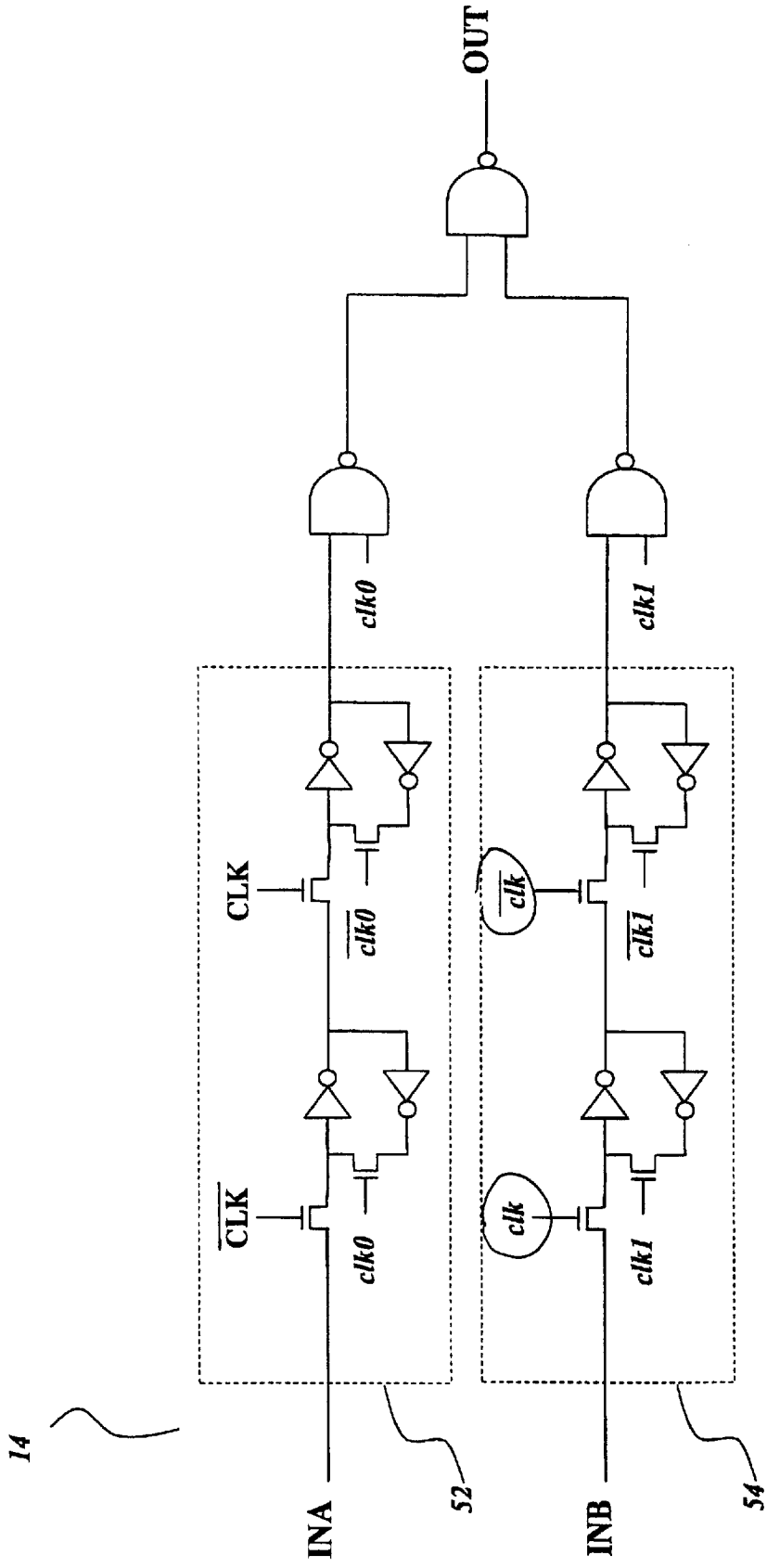


Fig. 3

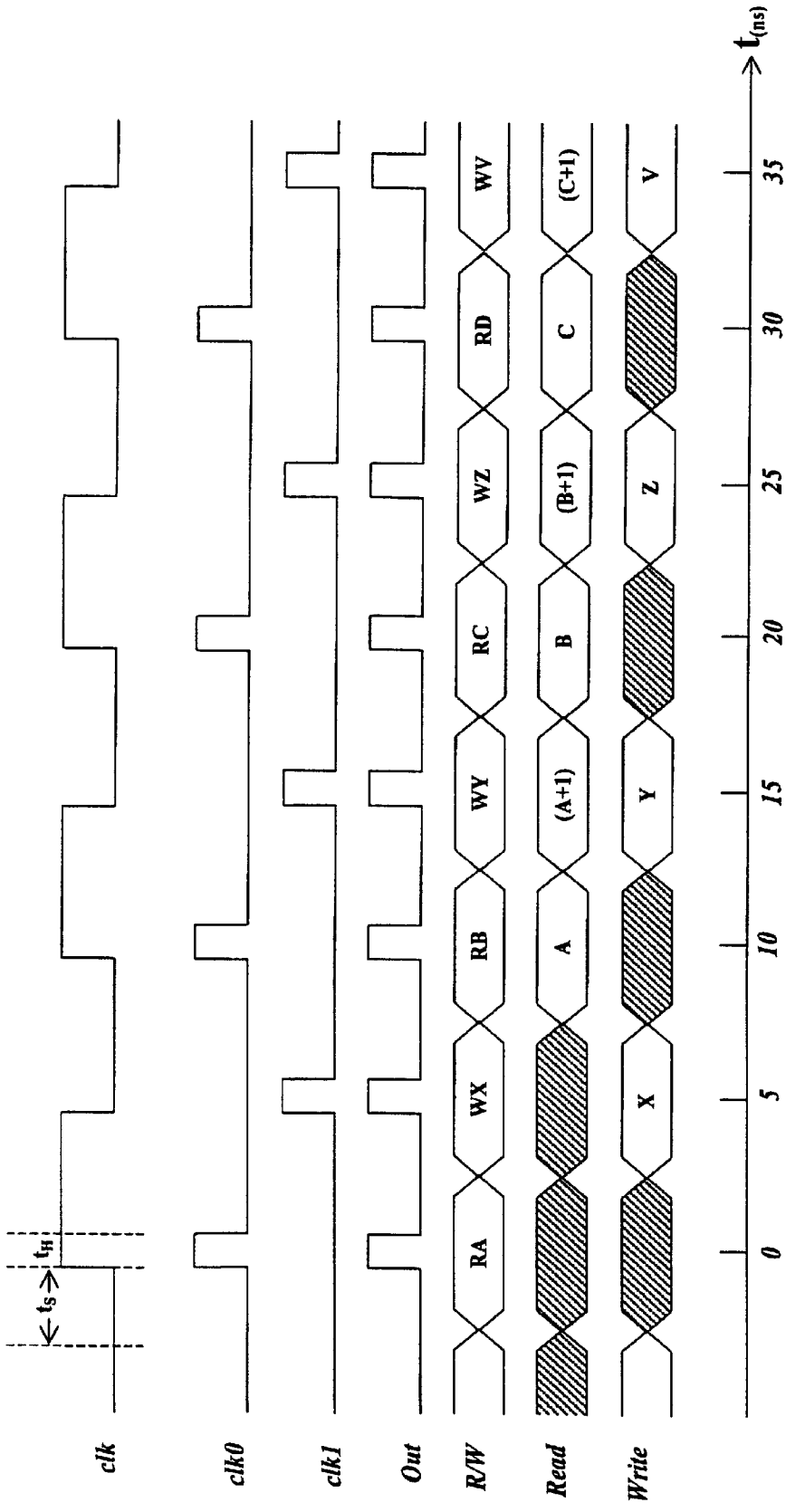


Fig. 4

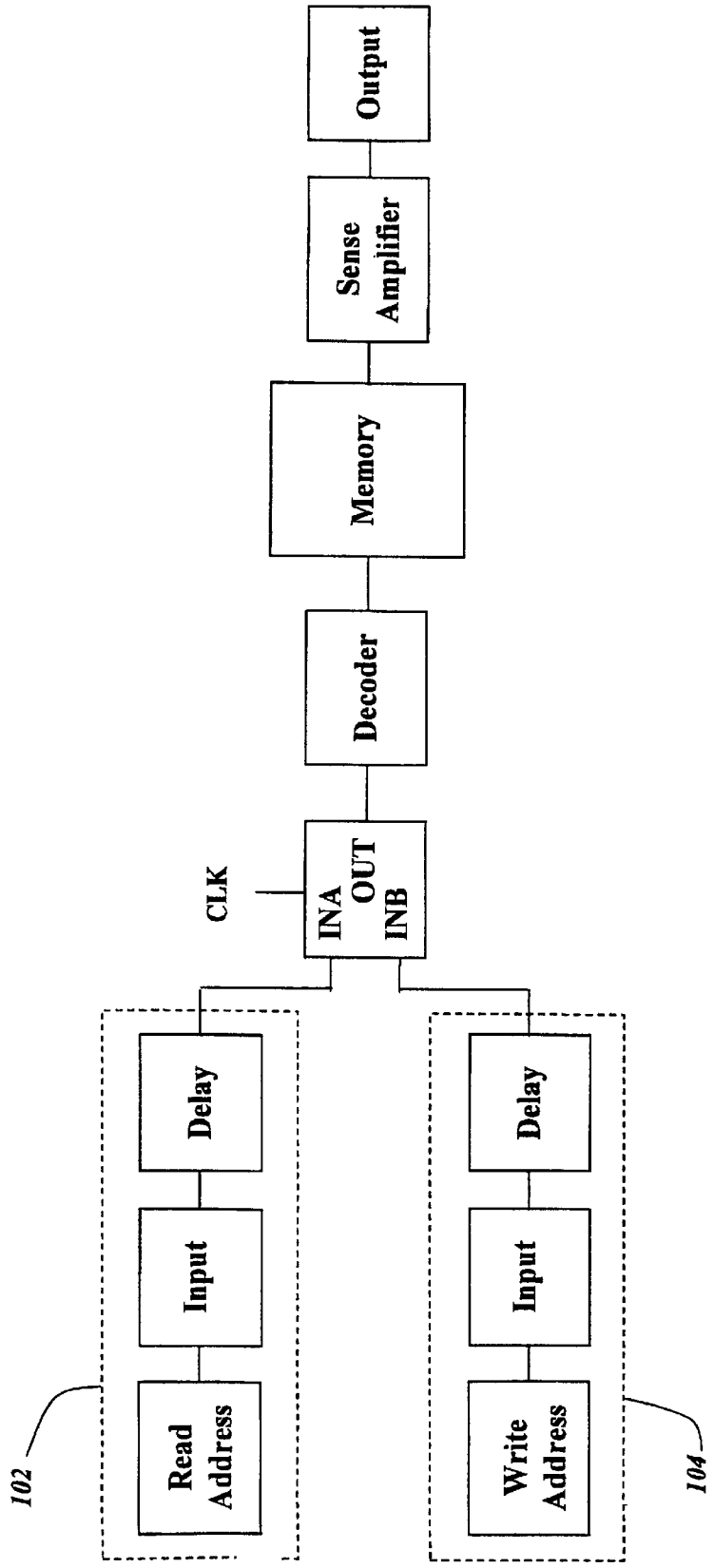

Output
Sense Amplifier
Memory
Decoder
CLK
INA
OUT
INB
Delay
Input
Read Address
Delay
Input
Write Address
102
104

Fig. 5

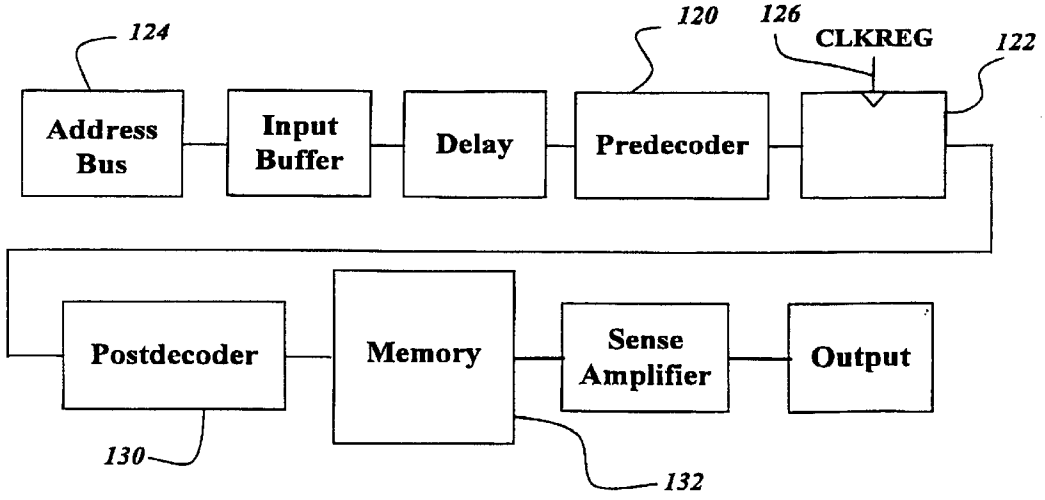


Fig. 6A

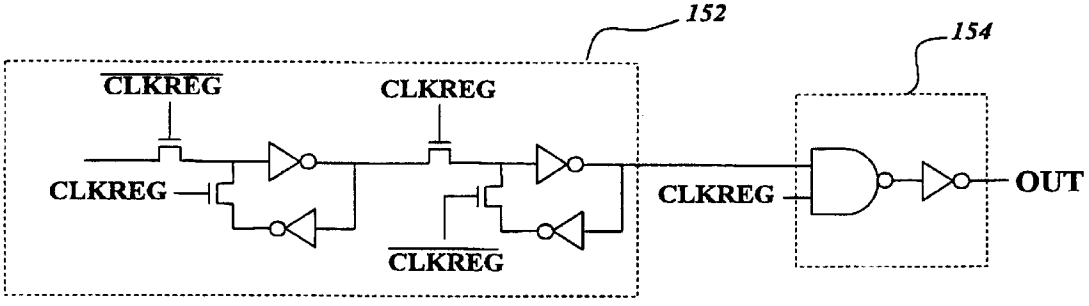


Fig. 6B

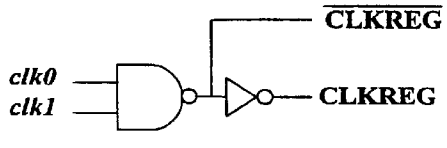


Fig. 6C

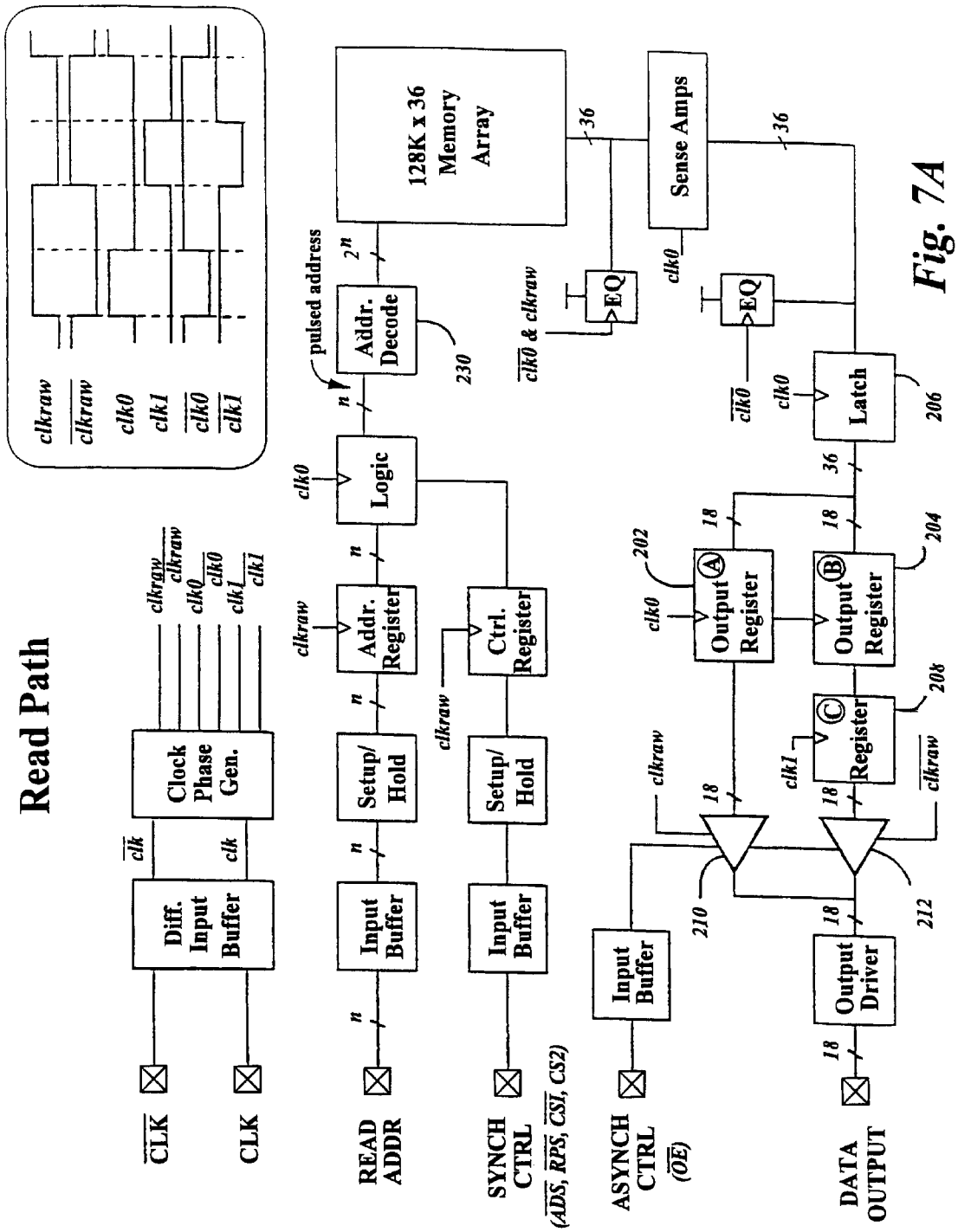


Fig. 7A

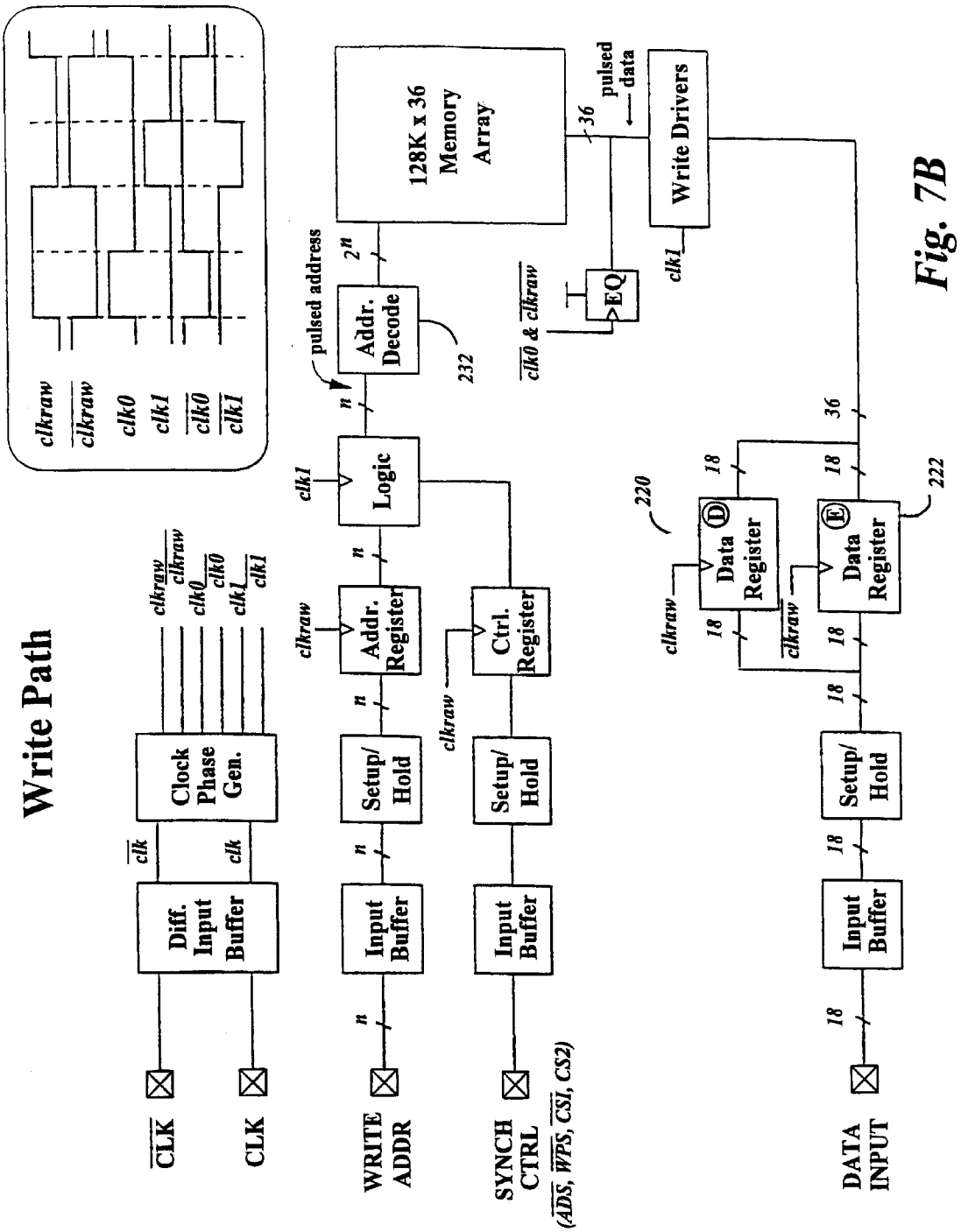


Fig. 7B

CIRCUIT AND METHOD FOR IMPLEMENTING SINGLE-CYCLE READ/WRITE OPERATION(S), AND RANDOM ACCESS MEMORY INCLUDING THE CIRCUIT AND/OR PRACTICING THE METHOD

This is a continuation of U.S. Ser. No. 09/238,270, filed Jan. 27, 1999.

The invention described and claimed in this application may be related to subject matter described in one or more copending provisional applications entitled, "Random Access Memory And Process For Writing To And Reading From The Same," by Mathew R. Arcoleo, Cathal G. Phelan, Ashish Pancholy, and Simon J. Lovett, identified as 60/077,982 and/or "Random Access Memory Having Read/Write Address Bus and Process For Writing To And Reading From The Same," by Mathew R. Arcoleo, Cathal G. Phelan, Ashish Pancholy, and Simon J. Lovett, identified as Ser. No. 60/078,029 both of which were filed in the U.S. Patent and Trademark Office as a provisional patent application on Mar. 13, 1998, both of which are incorporated herein by reference in their entireties.

This application is a continuation of Ser. No. 09/238,270 Jan. 27, 1999 which claim benefit of Ser. No. 60/078,718 Mar. 20, 1998.

BACKGROUND OF THE INVENTION

This invention relates generally to the field of semiconductor and/or integrated circuit devices, particularly to a random access memory and process for writing to and reading from the same, and more particularly to a circuit and method for implementing single-cycle read/write operation(s) in a random access memory (RAM).

OBJECTS OF THE INVENTION

The primary object of the invention is to provide a circuit and method that enables reading from and writing to a random access memory in the same clock cycle.

Another object of the invention is to provide a circuit and method that enables reading from and writing to a random access memory in the same clock cycle, using a single read/write address bus or separate read and write address busses.

A further object of the invention is to provide a circuit that latches a new address on each edge, transition or level of a periodic and/or control signal.

A further object of the invention is to provide a random access memory that increases data throughput.

Still yet another object of the invention is to provide such a circuit and/or random access memory that reduces the chip area dedicated to transmitting and/or storing address information.

An even further object of the invention is to provide a random access memory and method of operating the same in which read and write operations may be executed in the same clock cycle.

Yet further objects of the invention include providing such a random access memory and method of operating the same in which fully random addresses may be employed, in which successive and/or asserted addresses may be completely unrelated, and/or in which no restrictions are placed on successive and/or asserted addresses.

Another object of the invention is to provide such a random access memory and method of operating the same in which the same address may be used to read from and write to the memory in the same clock cycle.

A further object of the invention is to provide such a random access memory and method of operating the same in which a periodic signal (e.g., a clock) is the only control-type signal essential to operability.

Other objects and advantages of the present invention will become apparent from the following description, taken in connection with the accompanying drawings, wherein, by way of illustration and example, embodiments of the present invention are disclosed.

SUMMARY OF THE INVENTION

The present invention concerns a circuit comprising an address bus providing random addresses for a random access memory array, and a register configured to store or receive (i) a first random address from the address bus to the random access memory array directly or indirectly in response to a first periodic signal transition and (ii) a second random address from the address bus to the random access memory array directly or indirectly in response to a second periodic signal transition, wherein the second periodic signal transition occurs in the same periodic signal cycle as, and preferably is complementary to, the first periodic signal transition.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings constitute a part of this specification and include exemplary embodiments to the invention, which may be embodied in various forms. The features and advantages of the present invention are illustrated by way of example in the drawings, in which:

FIG. **1** shows an overview of an embodiment of the present address scheme;

FIG. **2** shows an overview of a random access memory (RAM) architecture employing the address scheme shown in FIG. **1**;

FIG. **3** shows a detailed schematic diagram of the address register shown in FIG. **1**;

FIG. **4** shows various waveforms illustrating the relative timing of various signals in conjunction with exemplary read and/or write operations performed according to the invention;

FIG. **5** shows an overview of a random access memory (RAM) architecture employing a second embodiment of the present address scheme;

FIGS. **6**A–**6**C show an overview of a random access memory (RAM) architecture employing a third embodiment of the present address scheme (FIG. **6**A), a detailed schematic diagram of the address register shown in FIG. **6**A (FIG. **6**B), and an exemplary circuit configured to generate one or more pulses for latching address information in the address register shown in FIG. **6**B (FIG. **6**C); and

FIGS. **7**A and **7**B show an overview of a random access memory (RAM) architecture employing a fourth embodiment of the present address scheme, wherein FIG. **7**A shows components useful for conducting one or more read operations, and FIG. **7**B shows components useful for conducting one or more write operations.

It is to be understood that, in some instances, various aspects of the invention may be shown exaggerated or enlarged to facilitate an understanding of the invention, and in other instances, some aspects of the invention considered to be conventional may not be shown so as to avoid obfuscating more important aspects or features of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Detailed descriptions of the preferred embodiments are provided herein. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure or manner.

In the present random access memory, each of the address bus, address register, data input bus, data output bus, and random access memory array may independently be n or m·n bits wide, where n is an integer≧2, preferably≧4, and more preferably≧8, and m is independently an integer≧2, preferably of 2–8, and more preferably of 2–4. In specific examples, n may be 8, 9, 16, 18, 32, 36, 64, 72, 128 or 144. The data input bus may receive data from an external source. In a preferred embodiment, each of the data input bus, data output bus, and address bus is unidirectional (i.e., data flows in one direction only).

In the present invention, a "periodic signal" refers to any signal that has an oscillating waveform, the frequency of which may be predicted and/or controlled in accordance with techniques known in the art, and that can be configured to control one or more circuit functions performed as part of a read operation or a write operation in a memory. The periodic signal may be configured to control one or more data transfer operations to or from a random access memory array in response to first and second transitions thereof, respectively, where the second transition occurs within the same periodic signal cycle as, and which may be complementary to, the first transition. Therefore, the memory may operate in a synchronous manner. For synchronous operations, the periodic signal may be an internal or external clock signal, or a periodic control signal such as write enable or output enable. There may be more than one independent periodic signal controlling read, write, register and/or data pass gate functions (e.g., a clock signal and its complement). Where appropriate and/or desirable, the periodic signals comprise a first clock signal and its complement. Alternatively, however, the periodic signal may comprise a pulse generated in response to a clock transition or, alternatively, a predetermined logic or voltage level of a clock signal.

Accesses to and from the memory array, including transmission of address information along an address path to the array, may be controlled by a single input clock or a pair of differential input clocks (CLK/CLK*, where a signal designated "X*" indicates the complement of the corresponding signal "X", similar to the signals in the Figures bearing an overstrike or "bar" designation). In the present application, a "complementary transition" may refer to either the same transition of complementary signals (e.g., the rising edges of both CLK and CLK*), or opposite transitions of the same signal (i.e., the rising and falling edges of CLK). All synchronous timing may be referenced from the cross point of the differential input clock signals. Accesses can be initiated on any edge of any periodic signal (preferably on the rising edge of a clock signal, assuming any other control signals are asserted at their active logic levels), but for ease and simplicity of logic circuitry, accesses to the array are initiated on the rising edge of the positive clock (CLK).

The present random access memory array may be configured to store and/or retrieve data at any random address therein. The address is defined by one or more signals on the address bus.

One (or More) Address Busses

As shown in FIG. **1**, the present invention concerns a circuit comprising an address bus **12** providing random addresses for a random access memory (RAM), and a register **14** configured to store or receive (i) a first random address from the address bus in response to a first periodic signal transition **16** and (ii) a second random address from the address bus in response to a second periodic signal transition **18**, wherein the second periodic signal transition occurs within the same periodic signal cycle as, and preferably is complementary to, the first periodic signal transition. The register may be further configured to transfer or output (i) the first random address to circuitry downstream from the register in the address path of the memory (e.g., a RAM array) in response to a first control signal **20** and (ii) the second random address in response to a second, independent control signal **22**.

As shown in FIG. **1**, the register may comprise two registers (each of which may independently comprise a D-type register, a T-type register, a master-slave register or a latch, but which preferably comprise a master-slave register or a D-type register) configured to store random address information from the address bus in response to the two complementary periodic signal transitions **16** and **18**. Each register may independently further comprise a logic gate **26** configured to output or provide the random address information (or the complement thereof) from the register in response to a periodic signal or pulse **20** or **22**. The periodic signals or pulses **20** and **22** may be independently the same as or different from (i) each other and/or (ii) the periodic signal(s) **16** and/or **18**.

Where the circuit employs two registers, the circuit may further comprise a logic gate **26** configured to provide random address information or its complement (e.g., OUT) from the logic gates receiving the address information stored in the registers. Such logic gates are conventional and known to those skilled in the art, and may comprise and combination of transistors and/or logic elements providing a NAND or AND function (an "AND-type logic gate").

FIG. **2** shows an overview of a random access memory (RAM) architecture employing the circuit shown in FIG. **1**. Thus, the present circuit may further comprise the random access memory **30** and circuitry operable to (i) read data into the random access memory array at the first random address and (ii) write data into the random access memory array at the second random address. The random access memory may further comprise a decoder **32** configured to activate the random address in the random access memory in response to receiving the random address from the register. Address input path **10** may further comprise (i) an input buffer **24** configured to receive random address information from the address bus and provide the random address information to the register, and/or (ii) a delay element **34** interposed between the input buffer **24** and register **14**. Delay element **34** may be configured in accordance with techniques and circuit elements known in the art to set up and hold the address information at node **36** for a length of time sufficient to enable register **14** to store or latch the address information.

Where a decoder located downstream from the address register(s) fully decodes the address information, the length of time for which address information is set up and held (e.g., at node **36**) may be minimized. This allows for greater variations in the periodic signal duty cycle. One notorious limitation to maximizing data throughput in synchronous RAMs is the length of time one must allow for variability in

the periodic signal duty cycle, a parameter that effectively limits the maximum frequency of conventional clock circuits. In the present invention, practical limits to the data throughput rate may be determined by the set up and hold window (e.g., $[t_S+t_H]$; see, for example, the CLK waveform in FIG. **4**) and the pulse widths of the control pulses that latch address information and/or data into a register in the corresponding input or output path (e.g., clk**0**, clk**1**; see FIGS. **3**, **4**, **7**A and **7**B).

The width of a control pulse in the present invention may be, for example, from (1/p) to (1–[1/p]) times the width of a half-cycle of the periodic signal (where p is, for example, from 1.1 to 10, preferably from 1.5 to 4). In the example shown in the waveforms inset into FIGS. **7**A and **7**B, p is about 2. The set up and hold window in the present invention may be, for example, about [(1/q)+(1/r)] times the width of a half-cycle of the periodic signal, where q is, for example, from 0.5 to 10, preferably from 0.75 to 4, and r is independently from 1 to 20, preferably from 1.5 to 10). In the example shown in FIG. **4**, q is 1 and r is 4.

The circuitry operable to write data into the array at a random address may do so in response to at least one transition of the periodic signal. Similarly, the present random access memory may further comprise circuitry operable to read data from a random address in the array may do so in response to at least one transition of the periodic signal. The periodic signal transitions to which the read circuitry and write circuitry respond are preferably, but not necessarily, complementary to each other. For example, when the memory comprises dedicated and/or independent data input and data output ports (see the copending provisional applications identified as Appln No. 60/077,982 and/or Appln. No. 60/078,029), each transition of the periodic signal may be independently designated as a read operation or a write operation. In fact, when the memory comprises two or more independent address registers (and the data busses, data registers and memory array all have the same width), each transition of the periodic signal may be independently designated as a read operation, a write operation or both read and write operations.

The random access memory may further comprise an output path **40**, which may comprise one or more sense amplifiers **42** and one or more data outputs **44**. Each data output **44** may comprise a data bus and an output pad. The output data bus may be unidirectional.

Referring now to FIG. **3**, an exemplary address register operable in the circuits of FIGS. **1** and **2** is shown. The register may comprise two or more subregisters **52** and **54**, each of which may be a D-type or master-slave-type register. The address bus provides random address information one or more inputs to register **14** (e.g., INA and INB). Address information may be received by and/or pass into subregisters **52** and **54** in response to first and second periodic signal transitions, respectively (e.g., CLK* and CLK). As shown in FIG. **3**, the first and second periodic signal transitions may be complementary to each other.

Subregister **52** stores the random address information in response to a first periodic signal transition or pulse (e.g., CLK**0**) and outputs the random address information in response to a second periodic signal transition or pulse (e.g., CLK**0***). As shown in FIG. **3**, the periodic signal transitions or pulses that result in storing and outputting the random address information may be complementary to each other. When pulse generated in response to a rising or falling edge of a periodic signal such as a clock (see, e.g., clk**0** and/or clk**1** in FIG. **4**) controls receive, store, latch and/or output functions in a register, the receive, store, latch and/or output function may be considered to be at least indirectly responsive to a periodic signal transition. Subregister **54** operates in a manner similar to subregister **52**, but in response to different periodic signal transitions or pulses (e.g., CLK**1** and CLK**1***).

In one embodiment, the register stores two read addresses or two write addresses in a single cycle of the periodic signal (e.g., CLK). For example, register **14** stores the first random read address from the address bus in response to a first control pulse (e.g., CLK**0**) and the second random read address from the address bus in response to a second control pulse (e.g., CLK**1**). The control pulses may be generated in response to successive transitions of the periodic signal and/or its complement, such that the control pulses are in effect generated in response to complementary transitions of the periodic signal in a single cycle (see also waveforms CLK, clk**0** and clk**1** in FIG. **4**.)

Thus, the present circuit may further comprise a pulse generator configured to generate a first pulse in response to at least one of the first and second transitions of the periodic signal, the first pulse latching at least one of the random addresses into the register. The pulse generator may be further configured to generate a second pulse in response to at least one of the first and second transitions of the same or different periodic signal, the pulse latching at least a second one of the random addresses into the register.

Multiple Registers

In a further embodiment, the present circuit may comprise three or more registers. In such a case, the periodic signal and/or pulse generating logic may further comprise circuitry to provide multiple periodic signals and/or pulses, each offset from the other by a predetermined phase delay in accordance with known techniques and circuits. For example, in an embodiment comprising four registers, conventional phase delay circuitry can generate a second periodic signal phase-offset from the first clock by 90° or t/4 ns, where t is the length of the clock cycle in nanoseconds. Additional control pulses (e.g., clk**2** and clk**3**) can be generated from the edges or transitions of this second, phas-offset clock to control third and fourth address registers in the manner described above. Periodic signals complementary to the second, phase-offset clock and its corresponding control pulses can control other functions in the third and fourth registers, and elsewhere in the RAM for circuitry associated with the third and fourth registers, in a manner similar to that described both above for first and second registers and herein below for associated circuitry.

Transferring Data to and from the Array (Reading and Writing)

FIG. **4** shows the sequence of data transfer events occurring during read and write operations. In FIG. **4**, the letters "A", "B", "C", etc., refer to addresses in the RAM array and the corresponding word or words to be written to or read from such addresses. The terms "RAGA", "RB", etc., refer to a read function at address A, B, etc. The terms "WV", "WY", etc., refer to a write function at address X, Y, etc. The terms "clk**0**" and "clk**1**" refer, for example, to the control pulses that latch address information in address register **14** as shown in FIG. **3**. These signal "OUT" refers to the output signal from the address register(s) and associated logic circuitry (if present) shown, for example, in FIGS. **1**–**3**. The term "R/W" refers to read or write address information that may be stored in the address register(s) shown, for example,

in FIGS. **1–3**. Although the clock pulse CLK shown in FIG. **4** is a 125 MHz clock with a cycle time of 4 ns, a clock of any frequency (e.g., from 10 kHz to 10 GHz, preferably from 200 kHz to 4 GHz, more preferably from 1 MHz to 1 GHz) may be used. Examples of suitable clock frequencies include 12.5 MHz, 20 MHz, 25 MHz, 33 MHz, 50 MHz, 66 MHz, 75 MHz, 83 MHz, 100 MHz, 125 MHz, 133 MHz, 150 MHz, 166 MHz, 183 MHz, 200 MHz, 250 MHz, 333 MHz, etc.

Referring now to FIG. **4**, at time t=0 ns, address A is latched or written into the address register from the address bus by pulse clk0. As described above, pulse clk0 may be generated from the positive clock CLK transition from LOW to HIGH. Address A is present on the address bus at a time about t_S ns before the rising CLK transition. This is commonly known in the art as the "setup time". Address A is maintained on the address bus for a period of time of about (t_S+t_H) ns (the "setup and hold time"; see, e.g., waveform CLK in FIG. **4**). For a read operation, a read port select signal (see, e.g., "RPS*" in FIG. **7**A) may be asserted briefly (and preferably while the periodic signal(s) CLK and/or CLK* is/are transitioning at t=0 ns). The next rising transition of the periodic signal CLK, optionally in conjunction with a control pulse (e.g., clk0 and/or clk0*), senses the data at address A and latches the corresponding data word(s) from address A in the array through one or more (optional) latches **206** into one or more output registers (e.g., **202** and **204** in FIG. **7**A).

For either two n-bit-wide data words or one 2n-bit-wide data word stored in the array but output on an n-bit-wide data output bus, the HIGH logic level of CLK resulting from this initial transition at t=0 ns enables output buffer **210** and outputs a first n-bit-wide data word from address A to the data output bus. For n-bit-wide circuitry, a complementary transition of the periodic signal (e.g., a falling CLK transition or a rising CLK* transition) may then latch a second n-bit-wide data word from output register **204** into a shadow register (e.g., register **208** in FIG. **7**A). The LOW logic level of CLK resulting from this complementary CLK transition enables output buffer **212** and outputs the second n-bit-wide data word (e.g., "(A+1)", "(B+1)", "(C+1)", etc.) onto the data output bus and the data output pad(s).

In FIG. **4**, at time t=2 ns, address X is latched or written into the address register from the address bus by pulse clk**1**. As described above, pulse clk**1** may be generated from either (i) the negative clock CLK* transition from LOW to HIGH or (ii) the positive clock CLK transition from HIGH to LOW. Address X is also present on the address bus at a time about t_S ns before the rising CLK transition. Address X is also maintained on the address bus for a period of time of about (t_S+t_H) ns (the "setup and hold time"; see, e.g., waveform CLK in FIG. **4**). For a write operation, a write port select signal (see, e.g., "WPS*" in FIG. **7**B) may be asserted briefly (and preferably while the periodic signal(s) CLK and/or CLK* is/are transitioning at t=2 ns). This complementary transition of the periodic signal CLK/CLK*, optionally in conjunction with a control pulse (e.g., clk**1** and/or Clk**1***), writes data stored in one or more data input registers (see, e.g., **220** and **222** in FIG. **7**B) into the array at address X.

More specifically, a rising periodic signal CLK transition latches an n-bit-wide data word D(X) on the Data In bus into the first write register **220**. Alternatively, for 2n-bit-wide circuitry, the rising transition of the positive periodic signal CLK latches a single 2n-bit-wide data word in a single 2n-bit-wide data input register. Similar but complementary to the read operation described immediately above, address X is latched or written into the address register from the address bus during the second, falling CLK transition from HIGH to LOW. The new address signal, or address transition from A to X, occurs at least about ts ns before the crossover of the differential external clocks CLK and CLK* (see FIGS. **4** and **7**B). The falling transition of the CLK pulse, which may be sent on a clock generator-to-address register bus, enables the address register to store the X address that is on the address bus after the address transition.

Advantages

The RAM may access two data words with each read operation on the same clock edge as that which latches the read address. For example, referring to FIG. **7**A, the first or lower word of data may be driven onto the output data bus on the clock logic level resulting from the single clock edge that latches the data in the corresponding output register, provided any applied output control signal (e.g., an output enable signal OE) is asserted in an enabling state (e.g., LOW). On the subsequent clock transition, the second or higher order data word may be driven onto the output data bus on the clock logic level resulting from the clock transition that latches the second data word in the shadow register **208**, provided any applied output control signal remains asserted in an enabling state. In this configuration, all data may be available, for example, as soon 5.5 or 6 ns after a clock rise (assuming a 125 MHz clock signal), thus providing a read operation with as little as one cycle of latency.

On the same transitions of the subsequent clock cycle, the next data word(s) stored in the array is/are latched in the output register(s), then driven through one or more (three-state) output buffers onto the data output bus/pads on the same clock logic levels as before. Read accesses can be initiated, for example, on every rising edge of the positive clock. Doing so will "pipeline" the data flow such that data is transferred out of the device on every rising and falling edge of the clock.

When deselected (e.g., in a multiple-RAM system configuration), the present RAM may first complete the pending read transactions. Synchronous internal circuitry may automatically three-state the outputs following the next rising edge of the positive clock. This will allow for a seamless transition between a port in the present RAM and any external device (including without limitation a second RAM according to the invention) without the insertion of wait states.

The input and output ports in the present RAM architecture (e.g., DATA OUTPUT in FIG. **7**A and DATA INPUT in FIG. **7**B) may operate independently of one another. One can read or write to any location in the memory array, regardless of the transaction address on the other port. Should the input and output ports access the same location on the same cycle of the periodic signal, the information presented to the data inputs may be forwarded to the data outputs (by, e.g., conventional bypass logic circuitry responsive to a control signal generated in response to an AND-type logic comparison of the read and write addresses), or alternatively, the data stored in the output register may first be output on the data output bus, then the same location written with the new data.

Two (or More) Address Busses

In a further embodiment, the present invention may comprise first and second address input paths **102** and **104**, as shown in FIG. **5**. More specifically, the circuit may further

comprise a second address bus providing (i) a third random address in response to a first transition of the same or different periodic signal and (ii) a fourth random address in response to a second transition of the same or different periodic signal; and a second register configured to store (i) the third random address from the second address bus in response to a third control pulse and (ii) a fourth random address from the second address bus in response to a fourth control pulse different from the third control pulse, the third and fourth control pulses being the same as or different from the first and second control pulses. Such a circuit may also further comprise a first and a second input buffer configured to receive first and second random address information from the first and second address busses, respectively, and to provide the first and second random address information to the first and second

The present address bus and/or circuit may comprise a read address bus and an independent write address bus. In such a case, the register may comprise (a) a read register configured to store (i) first random read address information from the read address bus in response to a first transition of a first periodic signal and (ii) second random read address information from the read address bus in response to a second transition of the first periodic signal, and (b) a write register configured to store (i) first random write address information from the write address bus in response to a first transition of a second periodic signal and (ii) second random write address information from the write address bus in response to a second transition of the second periodic signal, the first and second periodic signals being the same or different.

Predecoding

In a further embodiment, as shown in FIG. **6A**, the present invention may further concern a predecoder **120** configured to at least partially decode the random address information from the address bus **124** prior to storing the at least partially decoded random address information in the register **122**. Consequently, the register may be configured to store (i) a first at least partially decoded random address from the address bus in response to a first periodic signal transition (e.g., at input **126**) and (ii) a second at least partially decoded random address from the address bus in response to a second periodic signal transition, wherein the second transition is complementary to the first transition. The address input circuit and/or RAM may also further comprise a postdecoder **130** configured to activate the random addresses in the RAM array **132** in response to receiving the random addresses from the register.

Because some decoding is done prior to synchronously storing the address information, this embodiment may maximize the amount of time available to write data to and/or read data from the array. Maximizing the array "cycle time" (i.e., the amount of time to write data to and read data from the array) provides opportunities to increase wordline and/or bitline recovery times, thus reducing power and/or current consumption. It may also permit one to employ a larger array without requiring additional and/or more sophosticated logic circuitry, and/or to implement pulsed or self-resetting logic.

Suitable descriptions and examples of predecoder and postdecoder circuitry can be found in copending application Ser. No. 08/575,554 (entitled, "Method and Apparatus for Reducing Skew Among Input Signals Within an Integrated Circuit," filed Dec. 20, 1995) and in copending application Ser. No. 08/575,555 (entitled, "Method and Apparatus for Reducing Skew Among Input Signals and Clock Signals Within an Integrated Circuit," filed Dec. 20, 1995; abandoned in favor of continuing prosecution application Ser. No. 08/931,989 filed on Oct. 30, 1997). For example, a predecoder may decode from j to k bits of an m-bit-wide address, and the postdecoder may decode the remaining bits of the m-bit-wide address, where j, k and m are each an integer such that $j<k<m$, preferably such that $j \geqq 1$, 2 or 3; $k \geqq m-1$, $m-2$, or $m-3$; and m is at least 4, preferably at least 8, and more preferably at least 10.

The Single Register

In a further embodiment, and as exemplified in FIG. **6B**, the address input circuit may comprise a single register **152** (e.g., per address bit), which may replace register **14** in FIGS. **1** and **2**. Optionally, to better ensure compliance with timing parameters, the register may provide an output through a single logic element **154**. As shown in FIG. **6C**, control signals and/or pulses for latching address information in and outputting address information from the register (e.g., CLKREG and CLKREG*) may be generated from pulses generated from transitions of a periodic signal (e.g., CLK**0** and CLK**1**; see FIGS. **3** and **4**). A logic gate providing a NOR or OR function (an "OR-type logic gate") is adequate for generating control signals and/or pulses for this single-register embodiment. Consequently, register **152** operates in essentially the same manner as register **14** in FIG. **3**.

The Detailed RAM Architecture

As shown in FIGS. **7A** and **7B**, the present random access memory (RAM) architecture may further comprise separate first and second ports (e.g., "DATA OUTPUT" [FIG. **7A**] and "DATA INPUT" [FIG. **7B**]) to access the memory array. The ports may be unidirectional, in which case each pair of ports (e.g., an input/output pair) may have a dedicated address bus.(e.g., "READ ADDR [FIG. **7A**] and WRITE ADDR" [FIG. **7B**]), in accordance with the embodiment described above for "Two (or More) Address Busses." Each data port and address path may comprise n inputs, a buffer or driver, and an n-bit register (as described above), where n is an integer of one or more, to maintain complete independence of the ports and their associated control logic. Separate data inputs and outputs eliminates the need to "turn around" the data bus as may be required with common or bidirectional I/O devices.

Accesses to the array through input and output ports may be somewhat independent of one another and are initiated synchronously with one or more periodic signals (e.g., an internal or external clock signal; a set of differential input clocks; etc.). In order to maximize data throughput, the input port transfers data on one of the rising or falling edges or during one of the sustained logic levels of the periodic signal cycle(s), and the output port transfers data on the other of the rising or falling edges or sustained logic levels of the periodic signal cycle(s). As described herein, data transfer may also be logic level-triggered; i.e., it may occur in response to a particular or predetermined logic level of one or more periodic signal(s).

The depth of the memory array may be, in effect, expanded with two or more arrays and/or independent RAM devices (e.g., integrated circuit chips), and their associated select logic circuitry. The control signals carried by such logic circuitry (e.g., port select inputs) allow each port to operate as if it was an independent device, thereby further allowing depth expansion independently on each port.

All synchronous data inputs may be passed through one or more write registers (or input registers) controlled by the

periodic signal(s). All data outputs may be passed through one or more read registers (and/or output registers), also controlled by the same or different periodic signal(s).

All writes may be conducted with on-chip synchronous self-timed write circuitry to simplify the interface logic.

EXAMPLES

As shown in FIGS. **7**A and **7**B, the present RAM architecture is, in a preferred embodiment, configured as a synchronous pipelined burst static RAM (SRAM). Data may flow unidirectionally into the SRAM through the Data In bus, and/or unidirectionally out through the Data Out bus. Each bus may have its own pads for receiving or transmitting external signals. The present RAM array receives address information on a read address bus or a write address bus and may store or latch the address information in an address register. By separating the data input and data output ports, the present RAM avoids possible data contention and/or eliminates any need to "turn-around" the data bus.

All data inputs may pass through one or more n- or 2n-bit-wide input registers (e.g., n-bit-wide registers **220** and **222** as shown in FIG. **7**B), controlled by the rising or falling edge of a positive input clock (e.g., clkraw, generated from the crossover of differential input clocks CLK and CLK*). In the 2n-bit-wide input register case, the data input bus may have the same width as the input register(s).

The present random access memory may comprise one or more arrays (e.g., "128K×36") configured to store and/or retrieve data at a random read and/or write address therein. The arrays are generally oriented in rows and columns, where the nuimber of rows may be from 1 to 2^x+c, preferably from 4 to 2^x+c, and more preferably from 16 to 2^x+c, where x may be an integer of from 2 to 15, preferably from 3 to 14, and more preferably from 4 to 12, and c represents the number of redundant rows, which may be an integer of from 0 to 12, preferably from 0 to 8, and more preferably from 0 to (2^x/8), and the number of columns may independently be from 1 to 2^y+d, preferably from 4 to 2^y+d, and more preferably from 8 to 2^y+d, where y may be an integer of from 0 to 10, preferably from 2 to 9, and more preferably from 3 to 8, and d represents the number of redundant columns, which may be an integer of from 0 to 8, preferably from 0 to 4, and more preferably from 0 to (2^y/8).

The address is defined by n signals on the address bus, where n is an integer of one or more, preferably 3 or more and more preferably of from 5 to 2^y+d, where y and d are as defined above. Address information reaches the array from the address register through an address decoder **230** (FIG. **7**A) or **232** (FIG. **7**B), the signals from which identify the locafion(s) in the array where an operation is to be performed. The array, which may be n or mn bits wide, preferably has the same total width as the total width of the input register(s) and/or the data input bus.

The present random access memory may further comprise an output data register, which may also be n or m-n bits wide, and may have the same width as the total width of the input register(s), the array, and/or the data input bus. Preferably, the data output bus is also n or m·n bits wide, more preferably the same width as the data input bus, the input register(s), the array, and/or the output register(s). The output port (e.g., "DATA OUTPUT" in FIG. **7**A) may further comprise a plurality of pads for providing the data externally.

When the random access memory comprises a plurality of arrays, the first random access memory array may receive data from a first data input bus and/or write data register, and the second random access memory array may receive data from a second data input bus and/or write data register. Similarly, a random access memory comprising a plurality of arrays may further comprise a plurality of data output busses and/or read data registers, the first and second read data registers respectively storing data transferred from the first and second random access memory arrays, and the first and second data output busses respectively transmitting data from the first and second random access memory arrays or read data registers. In this case, each random access memory array may further comprise (a) first circuitry operable to write data to the random access memory array(s) at a first random address and (b) second circuitry operable to read data from the random access memory array(s) at a second random address, each in response to successive transitions or logic levels of a periodic signal, the second random address being the same as or different from the first random address. Each array may also have a unique address bus for providing both read and write address information.

As shown in FIG. **7**A, the present random access memory may further comprise an n-bits-wide data output bus, first and second (three-state) output buffers (e.g., buffers **210** and **212**), and first, second and third n-bits-wide output registers (e.g., **202**, **204** and **208**), wherein:

- each of the first and second output registers store data from the output register in response to a first periodic signal transition or level,
- the third output register stores data from the first output register in response to a second, complementary periodic signal transition or level,
- the first output buffer is enabled to provide data to the output data bus from the third output register by a third periodic signal transition or level (which may be [i] the same as or different from the second, complementary periodic signal transition or level, or [ii] a complement of the first periodic signal transition or level, and which preferably enables data output when in a particular or predetermined logic level or state), and
- the second output buffer is enabled to provide data to the output data bus from the second output register in response to a fourth periodic signal transition or level (which may be [i] the same as or different from the first periodic signal transition or level or [ii] a complement of the second periodic signal transition or level, and which also preferably enables data output when in a particular or predetermined logic level or state).

Control inputs (e.g., "SYNCH CTRLD" and "ASYNCH CTRL" in FIG. **7**A, "SYNCH CTRL" in FIG. **7**B) may comprise one or more synchronous or synchronous external control signals. Such control signals may include one or more data input or write port select signals WPS or WPS*, one or more data output or read port select signals RPS or RPS*, a conventional asynchronous output enable signal (see OE* in FIG. **7**A), one or more conventional chip select signals (for multiple RAM applications; see, e.g., CS**1*** and/or CS**2** in FIGS. **7**A and **7**B), one or more address strobe or validity signals (e.g., "ADS*" in FIGS. **7**A and **7**B), etc. Synchronous external control signals may pass along the same or similar input path as address information, including passing through a control input register controlled by an edge or logic level of a periodic signal (e.g., clkraw).

One may advantageously employ multiple port select signals (e.g., WPS**1**, WPS**2**, WPS**1***, WPS**2***, RPS**1**, RPS**2**, RPS**1***, RPS**2***, etc.) when one includes multiple random

access memories in a given application (e.g., a data, voice and/or video communications device, such as a network switch or router). Preferably, each RAM in a given multiple-RAM application has at least one unique combination of read and at write port select signals that activate the particular port (e.g., WPS1* and WPS2, WPS1 and WPS2*, RPS1* and RPS2, RPS1 and RPS2*, etc.). Altematively, the different input and/or output port select signals can select (enable or disable) one read or write register of a multiple-register configuration.

The RAM shown in FIGS. 7A and 7B may further comprise one or more conventional logic circuits configured to control and/or gate the passage of address information to an address (post)decoder in response to a periodic signal and/or control pulse (e.g., clk0 [see FIG. 7A] or clk1 [see FIG. 7B]); one or more sense amplifiers interposed between the memory array and the output latch and/or output register (s); conventional sense line equalization circuitry, which may equalize one or more 2n-bit-wide busses, and which may respond to one or more periodic signals and/or control pulses (e.g., clkraw and/or clk0*; see FIG. 7A); one or more n- or 2n-bit-wide output latches which may latch output data is response to one or more periodic signals and/or control pulses (e.g., clk0; see FIG. 7A), which in turn may be the same as or different from the periodic signals and/or control pulses that latch output data into the output register(s); one or more write drivers interposed between the data input register(s) and the memory array, which may be configured to write data into the array in response to a periodic signal and/or control pulse (e.g., clk1 [see FIG. 7B]); conventional bitline equalization circuitry, which may equalize a predetermined number of bitlines and which may respond to one or more periodic signals and/or control pulses (e.g., clkraw* and/or clk1*; see FIG. 7B); one or more differential clock input buffers and one or more clock phase generators to generate the periodic signal(s) and/or control pulse(s) from the signal(s) output from the differential clock input buffer (s).

While the invention has been described in connection with certain preferred embodiments, it is not intended to limit the scope of the invention to the particular form set forth, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A circuit comprising:

a register configured to store (i) a first address in response to a first periodic signal transition and (ii) a second address in response to a second periodic signal transition, wherein the first and second periodic signal transitions both occur within a single periodic signal cycle.

2. The circuit according to claim 1, wherein said second periodic signal transition is complementary to said first periodic signal transition.

3. The circuit according to claim 1, wherein said first and second periodic signal transitions are complementary transitions of a single periodic signal or are similar transitions of complementary periodic signals.

4. The circuit according to claim 3, wherein said periodic signal comprises a member selected from the group consisting of (a) a clock signal and (b) a pulse generated in response to a clock signal transition.

5. The circuit according to claim 1, further comprising:

a circuit configured to (i) read data from a random access memory array from said first address and (ii) write data into said random access memory array at said second address.

6. The circuit according to claim 1, wherein:

said first address is presented to said register during one of said first and second periodic signal transitions; and

said second address is presented to said register during the remaining one of said first and second periodic signal transitions.

7. The circuit according to claim 6, further comprising:

a first input buffer configured to (i) receive first address information and (ii) provide said first address information to said register; and

a second input buffer configured to (i) receive second address information and (ii) provide said second address information to said register.

8. The circuit according to claim 7, further comprising:

a second register configured to store said second address information in response to a third periodic signal transition and a fourth periodic signal transition, wherein the third and fourth periodic signal transitions occur within said single periodic signal cycle and are the same as or different from said second and first periodic signal transitions, respectively.

9. The circuit according to claim 8, wherein:

said first register further comprises a first logic gate configured to provide said first address information or a complement of said first address information in response to said second periodic signal; and

said second register further comprises a second logic gate configured to provide said second address information or a complement of said first address information in response to a third periodic signal, said second and third periodic signals being independently the same as or different from (i) each other and/or (ii) said first periodic signal.

10. The circuit according to claim 8, wherein:

said second periodic signal transition is a first pulse signal generated in response to said first periodic signal transition, and

said third periodic signal is a second pulse signal generated in response to a transition complementary to said first periodic signal transition.

11. The circuit according to claim 10, further comprising:

a logic gate configured to provide address information or a complement of said address information in response to said third periodic signal transition, said third periodic signal transition being the same as or different from said first and second periodic signal transitions.

12. The circuit according to claim 1, wherein said address register comprises a master-slave type register.

13. The circuit according to claim 1, further comprising:

a pulse generator configured to generate a first pulse in response to at least a first transition of a periodic signal, said first pulse latching at least one of said first and second addresses in said register.

14. The circuit according to claim 13, wherein said pulse generator is further configured to generate a second pulse in response to at least a second transition of said first periodic signal, said pulse latching at least a second one of said first and second addresses into said register.

15. The circuit according to claim **1**, further comprising:

an input buffer configured to receive address information from an address bus to provide said address information to said register.

16. A random access memory, comprising:

the circuit as claimed in claim **1**; and

a decoder configured to activate an address in a random access memory in response to receiving said address from said circuit.

17. The circuit according to claim **1**, wherein said register is further configured to transfer (i) said first address to said random access memory in response to a first control signal and (ii) said second address to said random access memory in response to a second, independent control signal.

18. The circuit according to claim **1**, wherein said register is further configured to transfer said first and second addresses from an address bus to a random access memory within a single periodic signal cycle.

19. A circuit comprising:

means for storing a first address in response to a first periodic signal transition; and

means for storing a second address in response to a second periodic signal transition, wherein the first and second periodic signal transitions both occur within a single periodic signal cycle.

20. A method for writing to/reading from a memory comprising the steps of:

(A) storing a first address in response to a first periodic signal transition; and

(B) storing a second address in response to a second periodic signal transition, wherein the first and second periodic signal transitions both occur within a single periodic signal cycle.

* * * * *

EXHIBIT C

US006385128B1

(12) **United States Patent**
Arcoleo et al.

(10) **Patent No.: US 6,385,128 B1**
(45) **Date of Patent: May 7, 2002**

(54) **RANDOM ACCESS MEMORY HAVING A READ/WRITE ADDRESS BUS AND PROCESS FOR WRITING TO AND READING FROM THE SAME**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

(62) Division of application No. 09/238,954, filed on Jan. 27, 1999, now Pat. No. 6,262,937
(60) Provisional application No. 60/078,029, filed on Mar. 13, 1998.

(51) **Int. Cl.**[7] **G11C 8/00**
(52) **U.S. Cl.** **365/233**; 365/230.05; 365/220; 365/190
(58) **Field of Search** 365/233, 190, 365/230.05, 220, 189.04

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,169,284	A	9/1979	Hogan et al.	711/140
4,245,304	A	1/1981	Porter et al.	711/122
4,456,965	A	6/1984	Graber et al.	710/100
4,539,661	A	9/1985	Oritani	365/233.5
4,575,826	A	3/1986	Dean	365/222
4,599,708	A	7/1986	Schuster	365/174
4,752,871	A	6/1988	Sparks et al.	365/185.11
4,783,732	A	11/1988	Morton	365/230.05
4,849,937	A	7/1989	Yoshimoto	365/189.05
4,882,709	A	11/1989	Wyland	365/189.02
5,023,838	A	6/1991	Herbert	365/189.08
5,309,395	A	5/1994	Dickinson et al.	365/189.04
5,394,361	A	2/1995	Dickinson	365/189.04
5,440,717	A	8/1995	Bosshart	711/159
5,530,673	A	6/1996	Tobita et al.	365/185.09
5,546,569	A	8/1996	Proebsting et al.	713/600
5,561,781	A	10/1996	Braceras et al.	711/131
5,598,545	A	1/1997	Childers et al.	712/221
5,638,534	A	6/1997	Mote, Jr.	711/158
5,648,987	A	7/1997	Yang et al.	375/232
5,752,270	A	5/1998	Wada	711/169
5,781,480	A	7/1998	Nogle et al.	365/189.04
5,828,606	A	10/1998	Mick	365/189.05
5,838,631	A	11/1998	Mick	365/233
5,841,732	A	11/1998	Mick	365/233
5,875,151	A	2/1999	Mick	365/233
5,926,426	A	7/1999	Han	365/205
5,956,286	A	9/1999	Lattimore et al.	365/230.05
5,978,279	A	11/1999	Park	365/189.04
5,983,328	A	11/1999	Potts et al.	711/157
6,069,839	A	5/2000	Pancholy et al.	365/233
6,081,478	A	6/2000	Mick et al.	365/233
6,094,399	A	7/2000	Mick	365/233
6,262,936	B1	7/2001	Arcoleo et al.	365/233
6,262,937	B1	7/2001	Arcoleo et al.	365/233

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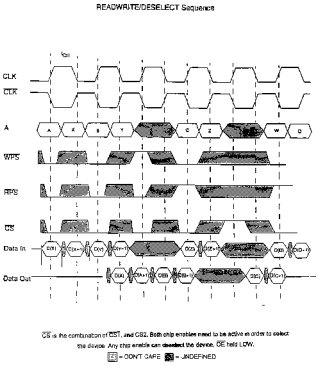
(57) **ABSTRACT**

A random access memory with a data input bus, a data output bus, a random access memory array configured to transfer data to random write addresses and from random read addresses in the random access memory array, an address bus providing the random read addresses and the random write addresses, and a first periodic signal configured to control data transfer operations (i) to the random access memory array in response to a first transition of the periodic signal and (ii) from the random access memory array in response to a second transition of the periodic signal, wherein the second transition of the periodic signal is complementary to the first transition of the periodic signal. One preferred embodiment further includes circuitry operable to write data into and read data from the random access memory array. Other preferred embodiments further include a write data register and/or a read data register. In a further embodiment, each of the data input bus and the data output bus is unidirectional. The invention also concerns a process for reading data from and writing data to a random access memory array.

6 Claims, 5 Drawing Sheets



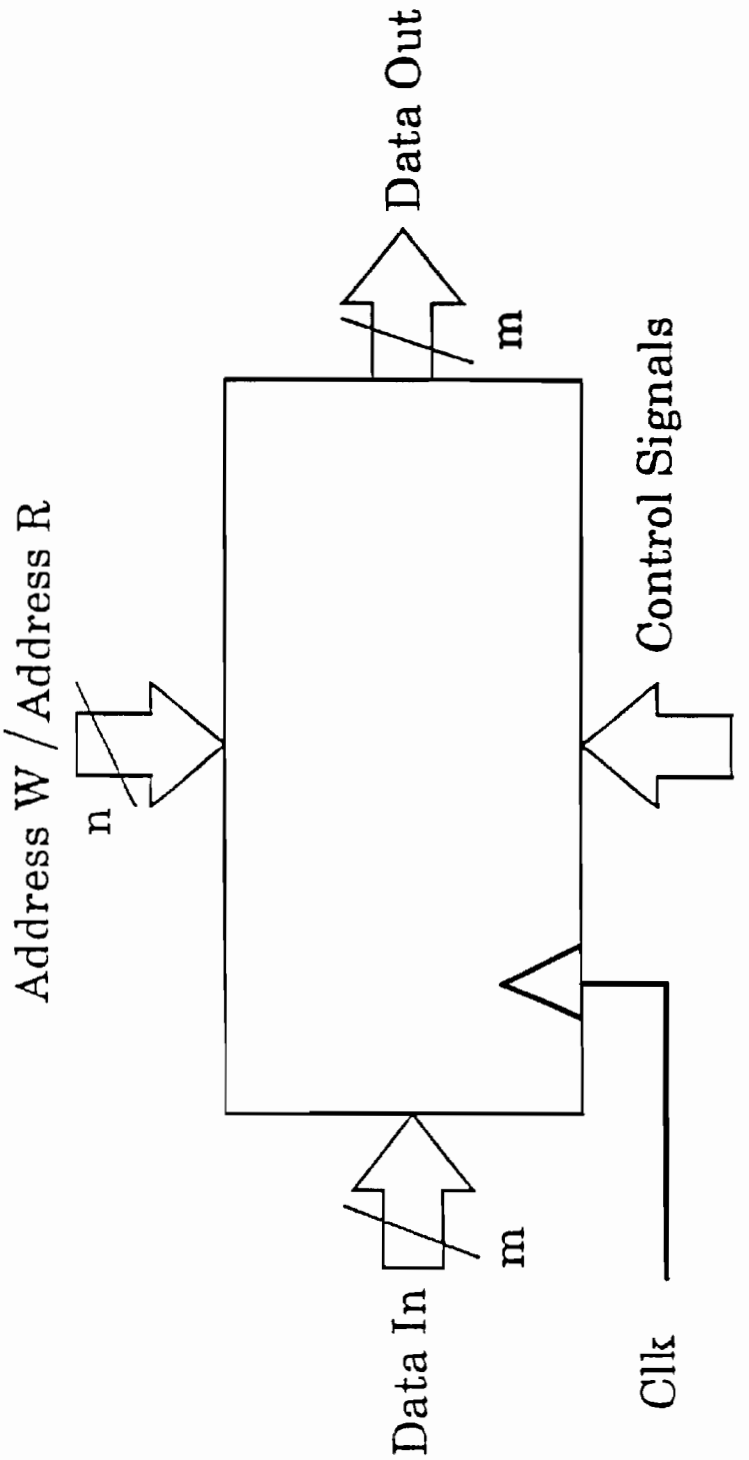


Fig. 1

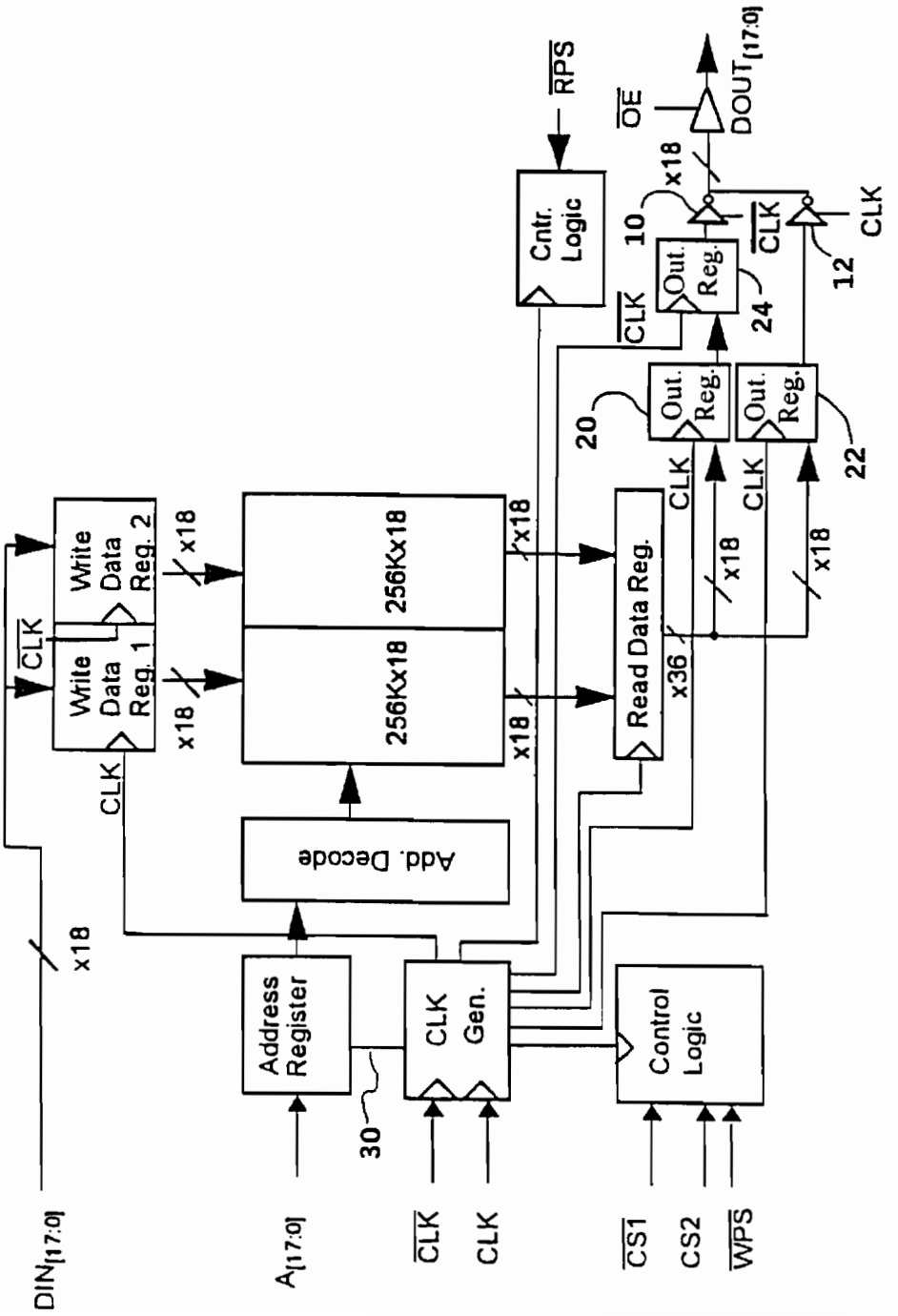
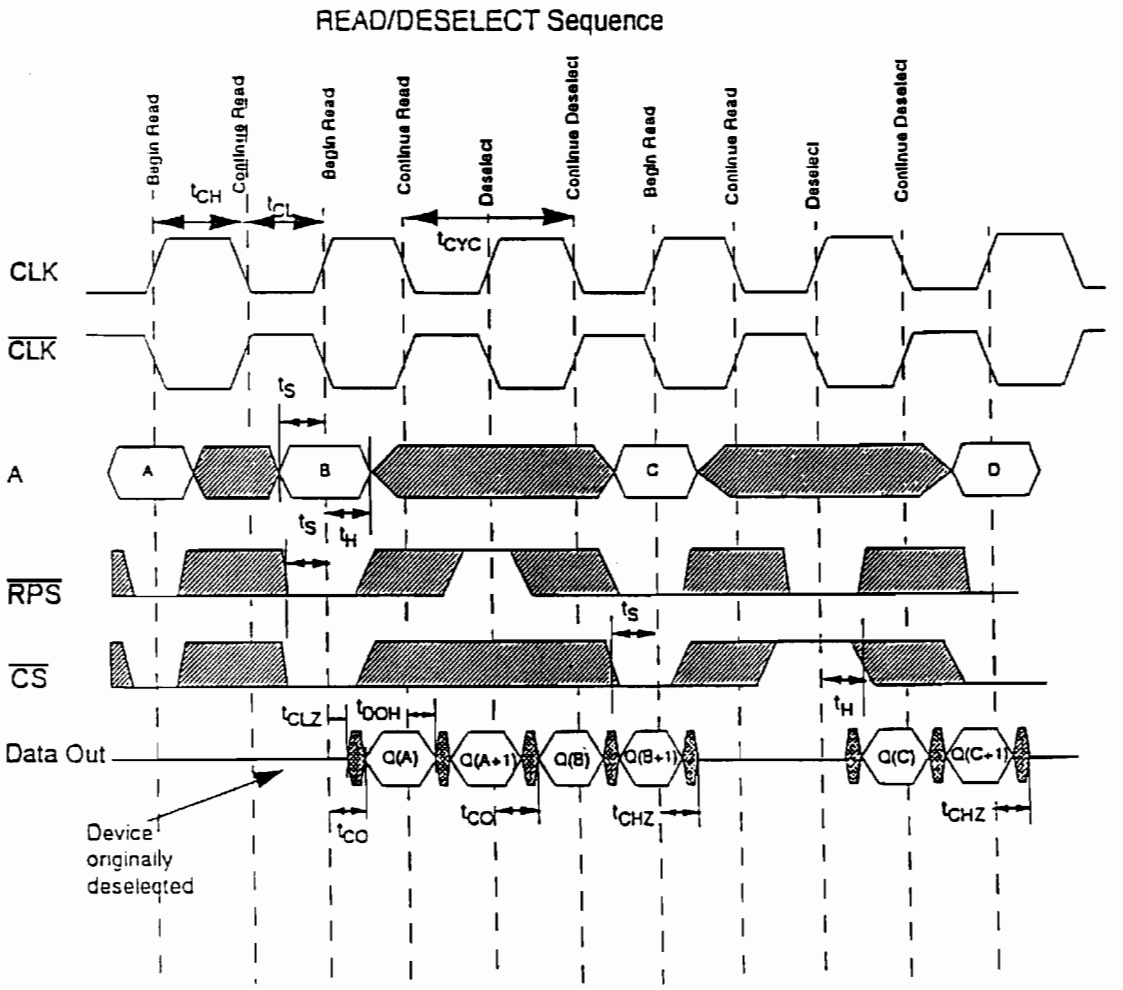

DIN[17:0]
x18
CLK
Write Data Reg. 1
Write Data Reg. 2
x18
CLK
x18
256Kx18
256Kx18
x18
Add. Decode
Address Register
30
A[17:0]
CLK Gen.
CLK
CLK
Control Logic
CS1
CS2
WPS
Cntr. Logic
RPS
Read Data Reg.
x36
x18
CLK
x18
CLK
Out. Reg.
20
Out. Reg.
22
CLK
Out. Reg.
24
CLK
10
x18
OE
DOUT[17:0]
12
CLK

Fig. 2

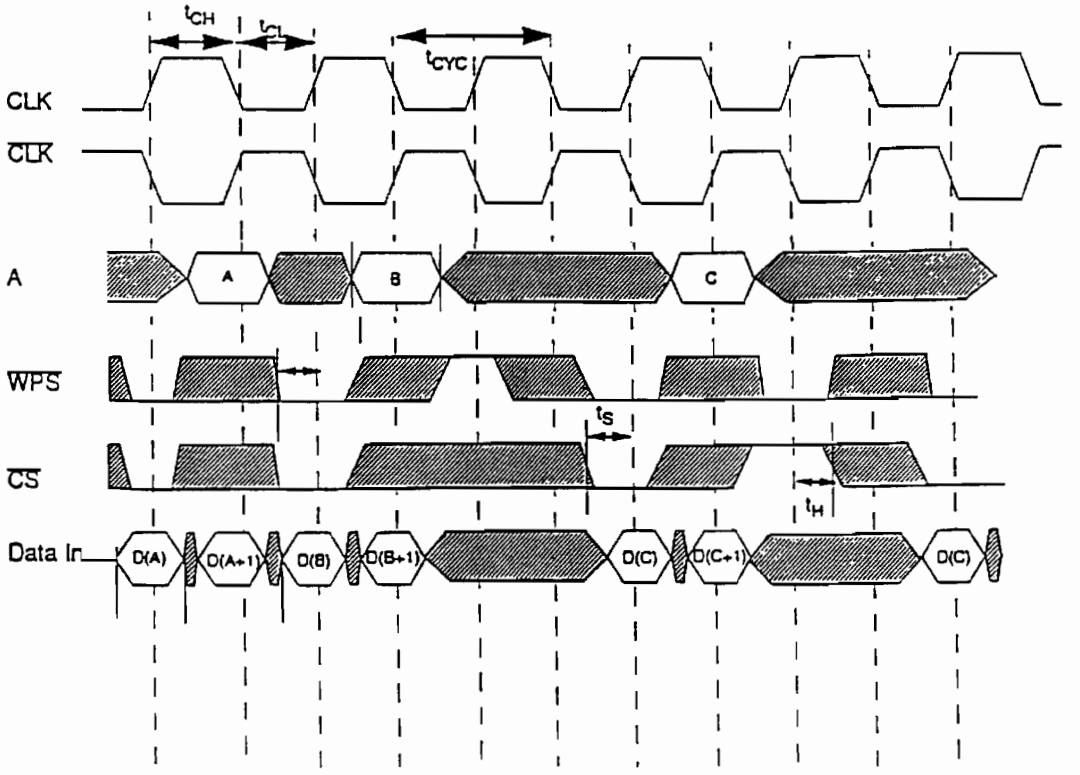


$\overline{CS}$ is the combination of $\overline{CS1}$, and CS2. Both chip enables need to be active in order to select the device. Any chip enable can deselect the device. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Fig. 3

WRITE/DESELECT Sequence

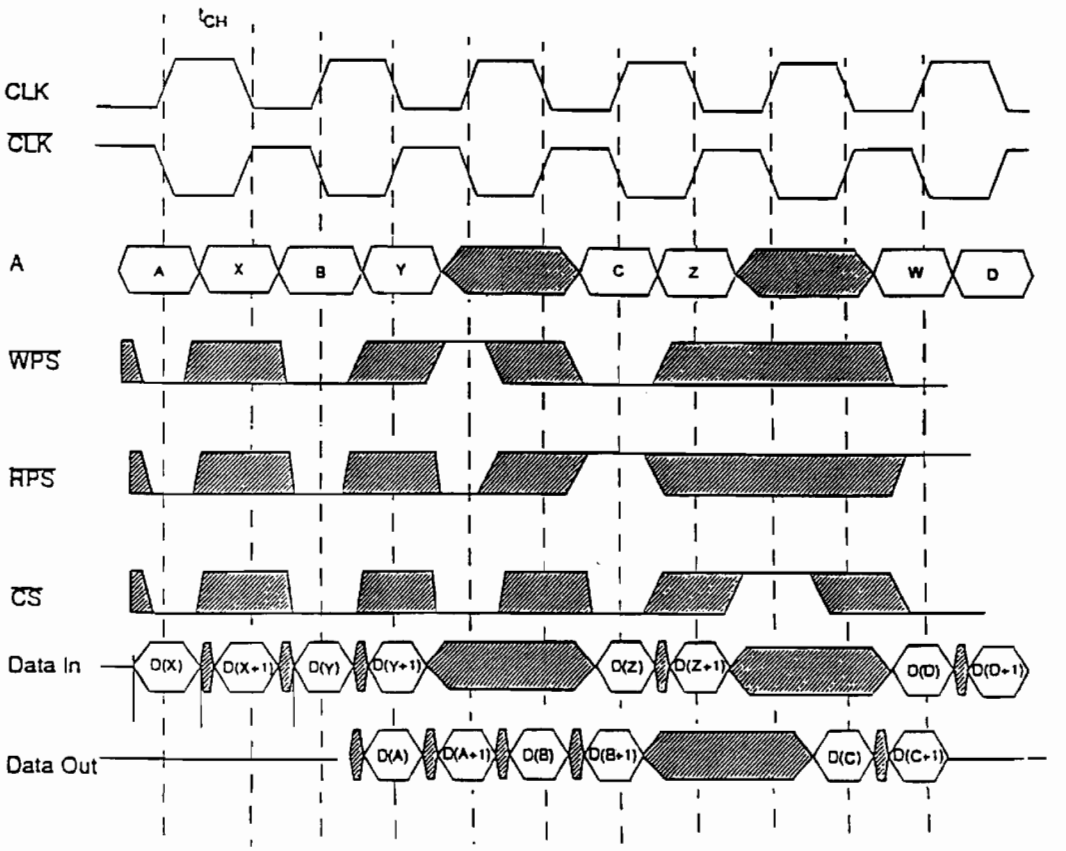


$\overline{CS}$ is the combination of $\overline{CS1}$, and CS2. Both chip enables need to be active in order to select the device. Any chip enable can deselect the device. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Fig. 4

READWRITE/DESELECT Sequence



$\overline{CS}$ is the combination of $\overline{CS1}$, and CS2. Both chip enables need to be active in order to select the device. Any chip enable can deselect the device. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Fig. 5

RANDOM ACCESS MEMORY HAVING A READ/WRITE ADDRESS BUS AND PROCESS FOR WRITING TO AND READING FROM THE SAME

This is a divisional of U.S. Ser. No. 09/238,954, filed Jan. 27, 1999, now issued as U.S. Pat. No. 6,262,937.

This application claims the benefit of U.S. Provisional Application No. 60/078,029, filed Mar. 13, 1998, and is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

This invention relates generally to the field of semiconductor and/or integrated circuit devices, and more particularly to a random access memory and process for writing to and reading from the same.

OBJECTS OF THE INVENTION

The primary object of the invention is to provide a random access memory that increases data throughput.

Another object of the invention is to provide such a random access memory that reduces the chip area dedicated to transmitting and/or storing address information.

Another object of the invention is to provide a random access memory and method of operating the same in which read and write operations may be executed in the same clock cycle.

Yet another object of the invention is to provide such a random access memory and method of operating the same in which fully random addresses may be employed.

Still yet another object of the invention is to provide such a random access memory and method of operating the same in which successive and/or asserted addresses may be completely unrelated.

Another object of the invention is to provide such a random access memory and method of operating the same in which no restrictions are placed on successive and/or asserted addresses.

Another object of the invention is to provide such a random access memory and method of operating the same in which the same address may be used to read from and write to the memory in the same clock cycle.

A further object of the invention is to provide such a random access memory and method of operating the same in which a periodic signal (e.g., a clock) is the only control-type signal essential to operability.

Other objects and advantages of the present invention will become apparent from the following description, taken in connection with the accompanying drawings, wherein, by way of illustration and example, embodiments of the present invention are disclosed.

SUMMARY OF THE INVENTION

The present invention concerns a random access memory comprising: a data input bus, a data output bus, a random access memory array configured to transfer data to random write addresses and from random read addresses in said random access memory array, an address bus providing said random read addresses and said random write addresses, and a periodic signal configured to control data transfer operations (i) to said random access memory array in response to a first transition or logic level of said periodic signal and (ii) from said random access memory array in response to a second transition or logic level of said periodic signal, wherein said second transition or logic level of said periodic signal is complementary to said first transition or logic level of said periodic signal.

In a further embodiment, the present invention concerns a process for reading data from and writing data to a random access memory array, comprising the steps of transferring a first plurality of data bits on a first unidirectional bus either to or from a first random address in said random access memory array in response to a first transition or logic level of a periodic signal, and transferring a second plurality of data bits on a second unidirectional bus either from or to a second, independent random address in said random access memory array in response to a second, complementary transition or logic level of said periodic signal (i.e., in the opposite manner from the first step).

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings constitute a part of this specification and include exemplary embodiments to the invention, which may be embodied in various forms. The features and advantages of the present invention are illustrated by way of example in the drawings, in which:

FIG. **1** shows an overview of the present random access memory (RAM) architecture;

FIG. **2** shows a more detailed embodiment of the RAM architecture shown in FIG. **1**;

FIG. **3** shows various waveforms illustrating relative timing of various signals in conjunction with an exemplary read operation performed according to the invention;

FIG. **4** shows various waveforms illustrating relative timing of various signals in conjunction with an exemplary write operation performed according to the invention; and

FIG. **5** shows various waveforms illustrating relative timing of various signals in conjunction with an exemplary read/write operation performed according to the invention.

It is to be understood that, in some instances, various aspects of the invention may be shown exaggerated or enlarged to facilitate an understanding of the invention, and in other instances, some aspects of the invention considered to be conventional may not be shown so as to avoid obfuscating more important aspects or features of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Detailed descriptions of the preferred embodiments are provided herein. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure or manner.

In the present random access memory, each of the data input bus, data output bus, and random access memory array may independently be m or n·m bits wide, where m is an integer ≥ 2, preferably ≥ 4, and more preferably ≥ 8, and n is independently an integer ≥ 2, preferably of 2–8, and more preferably of 24. In specific examples, m may be 8, 9, 16, 18, 32, 36, 64, 72, 128 or 144. The data input bus may receive data from an external source. In a preferred embodiment, each of the data input bus, data output bus, and address bus is unidirectional (i.e., data flows in one direction only).

In the present invention, a "periodic signal" refers to any signal that has an oscillating waveform, the frequency of

which may be predicted and/or controlled in accordance with techniques known in the art, and that can be configured to control one or more circuit functions performed as part of a read operation or a write operation. The periodic signal may be configured to control one or more data transfer operations to or from the random access memory array in response to first and second transitions of the periodic signal, respectively, where the second transition is complementary to the first transition of the periodic signal. Therefore, the memory operates in a synchronous manner. For synchronous operations, the periodic signal may be an internal or external clock signal, or a periodic control signal such as output enable. There may be more than one independent periodic signal controlling read, write, register and/or data pass gate functions. Where appropriate and/or desirable, the periodic signals may comprise a first clock signal and its complement.

The present random access memory array may be configured to store and/or retrieve data at any random address therein. The address is defined by one or more signals on the address bus.

The present random access memory may further comprise circuitry operable to write data into the array at a first random address in response to at least one transition of the periodic signal. Similarly, the present random access memory may further comprise circuitry operable to read data from a random location in the array in response to at least one transition of the periodic signal. The periodic signal transitions to which the read circuitry and write circuitry respond are preferably complementary to each other.

As shown in FIG. **1**, the present random access memory (RAM) architecture may comprise separate first and second ports (e.g., "Data In" and "Data Out") to access the memory array. The ports may be unidirectional, in which case each pair of ports (e.g., an input/output pair) may have a dedicated address bus comprising n address inputs (e.g., "Address W/Address R" in FIG. **1**), where n is an integer of one or more, to maintain complete independence of the ports and their associated control logic. Separate data inputs and outputs eliminates the need to "turn around" the data bus as may be required with common I/O devices.

Accesses to the array through input and output ports may be somewhat independent of one another and are initiated synchronously with one or more periodic signals (e.g., an internal or external clock signal; a set of differential input clocks; etc.). In order to maximize data throughput, the input port transfers data on one of the rising or falling edges or during one of the sustained logic levels of the periodic signal cycle(s), and the output port transfers data on the other of the rising or falling edges or sustained logic levels of the periodic signal cycle(s) (see, e.g., input clock "Clk" in FIG. **1**). As described herein, data transfer may also be logic level-triggered; i.e., it may occur in response to a particular or predetermined logic level of one or more periodic signal(s).

The depth of the memory array may be, in effect, expanded with two or more arrays and/or independent RAM devices (e.g., integrated circuit chips), and their associated select logic circuitry. The control signals carried by such logic circuitry (e.g., port select inputs) allow each port to operate as if it was an independent device, thereby further allowing depth expansion independently on each port.

All synchronous data inputs may be passed through one or more write registers (or input registers) controlled by the periodic signal(s). All data outputs may be passed through one or more read registers (and/or output registers), also controlled by the same or different periodic signal(s).

All writes may be conducted with on-chip synchronous self-timed write circuitry to simplify the interface logic.

EXAMPLE(S)

As shown in FIG. **2**, the present RAM architecture is, in a preferred embodiment, configured as a synchronous pipelined burst static RAM (SRAM). Data may flow unidirectionally into the SRAM through the Data In bus, and/or unidirectionally out through the Data Out bus. Each bus may have its own pads for receiving or transmitting external signals. The present RAM array receives address information on a single address bus (e.g., $A_{[17:0]}$) and may store or latch the address information in an address register. By separating the data input and data output ports, the present RAM avoids possible data contention and/or eliminates any need to "turn-around" the data bus.

Accesses for both data ports may be controlled by a single input clock or a pair of differential input clocks (CLK/CLK*, where a signal designated "X*" indicates the complement of the corresponding signal "X", similar to the signals in the Figures bearing an overstrike or "bar" designation). All synchronous timing may be referenced from the cross point of the differential input clock signals. Accesses can be initiated on any edge of any periodic signal (preferably on the rising edge of a clock signal, assuming any other control signals are asserted at their active logic levels), but for ease and simplicity of logic circuitry, accesses are initiated on the rising edge of the positive clock (CLK) only.

All data inputs (e.g., synchronous inputs DIN[**17**:**0**]) may pass through one or more m- or 2m-bit-wide input registers (e.g., m-bit-wide Write Data Reg. **1** and Write Data Reg. **2** as shown in FIG. **2**), controlled by the rising or falling edge of the positive input clock (CLK). In such a case, the data input bus may have the same width as the input register(s).

The present random access memory may comprise one or more arrays (e.g., "256K×18") configured to store and/or retrieve data at a random read and/or write address therein. The arrays are generally oriented in rows and columns, where the number of rows may be from 1 to 2^x+c, preferably from 4 to 2^x+c, and more preferably from 16 to 2^x+c, where x may be an integer of from 2 to 15, preferably from 3 to 14, and more preferably from 4 to 12, and c represents the number of redundant rows, which may be an integer of from 0 to 12, preferably from 0 to 8, and more preferably from 0 to (2^x/8), and the number of columns may independently be from 1 to 2^y+d, preferably from 4 to 2^y+d, and more preferably from 8 to 2^y+d, where y may be an integer of from 0 to 10, preferably from 2 to 9, and more preferably from 3 to 8, and d represents the number of redundant columns, which may be an integer of from 0 to 8, preferably from 0 to 4, and more preferably from 0 to (2^y/8).

The address is defined by n signals on the address bus, where n is an integer of one or more, preferably 3 or more and more preferably of from 5 to 2^y+d, where y and d are as defined above. Address information reaches the array from the address register through an address decoder, the signals from which identify the location(s) in the array where an operation is to be performed. The array, which may be m or n.m bits wide, preferably has the same width as the input register(s) and/or the data input bus.

The present random access memory may further comprise an output data register (e.g., Read Data Reg. in FIG. **2**), which may also be m or n·m bits wide, and may have the

same width as the input register(s), the array, and/or the data input bus. Preferably, the data output bus is also m or n·m bits wide, more preferably the same width as the data input bus, the input register(s), the array, and/or the output register (s). The output port may further comprise a plurality of pads (e.g., synchronous data outputs DOUT[**17**:**0**]) for providing the data externally.

When the random access memory comprises a plurality of arrays, the first random access memory array may receive data from a first data input bus and/or write data register, and the second random access memory array may receive data from a second data input bus and/or write data register. Similarly, a random access memory comprising a plurality of arrays may further comprise a plurality of data output busses and/or read data registers, the first and second read data registers respectively storing data transferred from the first and second random access memory arrays, and the first and second data output busses respectively transmitting data from the first and second random access memory arrays or read data registers. In this case, each random access memory array may further comprise (a) first circuitry operable to write data to the random access memory array(s) at a first random address and (b) second circuitry operable to read data from the random access memory array(s) at a second random address, each in response to successive transitions or logic levels of a periodic signal, the second random address being the same as or different from the first random address. Each array may also have a unique address bus for providing both read and write address information.

As shown in FIG. **2**, the present random access memory may further comprise an m-bits-wide data output bus, first and second three-state output buffers (e.g., buffers **10** and **12**), and first, second and third m-bits-wide output registers (e.g., Reg. **20**, Reg. **22** and Reg. **24**), wherein:

each of the first and second output registers store m bits of data from the output register in response to a first periodic signal transition or level,

the third output register stores m bits of data from the first output register in response to a second, complementary periodic signal transition or level,

the first three-state output buffer is enabled to provide data to the output data bus from the third output register by a third periodic signal transition or level (which may be [i] the same as or different from the second, complementary periodic signal transition or level, or [ii] a complement of the first periodic signal transition or level, and which preferably enables data output when in a particular or predetermined logic level or state), and

the second three-state output buffer is enabled to provide data to the output data bus from the second output register in response to a fourth periodic signal transition or level (which may be [i] the same as or different from the first periodic signal transition or level or [ii] a complement of the second periodic signal transition or level, and which also preferably enables data output when in a particular or predetermined logic level or state).

Control inputs (e.g., one or more synchronous data input or write port select signals WPS or WPS*, one or more synchronous data output or read port select signals RPS or RPS*, etc;) may pass through control input registers controlled by an edge or logic level of a periodic signal (e.g., the rising edge of the positive clock input CLK). One may advantageously employ multiple port select signals (e.g., WPS**1**, WPS**2**, WPS**1***, WPS**2***, RPS**1**, RPS**2**, RPS**1***, RPS**2***, etc.) when one includes multiple random access memories in a given application (e.g., a data, voice and/or video communications device, such as a network switch or router). Preferably, each RAM in a given multiple-RAM application has at least one unique combination of read and at write port select signals that activate the particular port (e.g., WPS**1*** and WPS**2**, WPS**1** and WPS**2***, RPS**1*** and RPS**2**, RPS**1** and RPS**2***, etc.). Alternatively, the different input and/or output port select signals can select (enable or disable) one read or write register of a multiple-register configuration.

Transferring Data to and from the Array

In a further embodiment, the present invention relates to a process for reading data from and writing data to a random access memory array, comprising the steps of:

transferring a first plurality of data bits on a first unidirectional bus to a random write address in said random access memory array in response to a first transition or logic level of a write control signal, and

transferring a second plurality of data bits on a second unidirectional bus from a random read address in said random access memory array in response to a second, complementary transition or logic level of said periodic signal.

Alternatively, the present process relates to the steps of:

transferring a first plurality of data bits on a first unidirectional bus from a random read address in said random access memory array in response to a first transition or logic level of a periodic signal, and

transferring a second plurality of data bits on a second unidirectional bus to a random write address in said random access memory array in response to a second, complementary transition or logic level of said periodic signal.

In the present process, the second, complementary transition of the periodic signal is also the next transition following the first transition of the periodic signal. Similarly, the second, complementary logic level of the periodic signal is the logic level following the next transition of the periodic signal.

Reading

As shown in FIG. **3**, read operations may be initiated by asserting an output port select signal (e.g., RPS*) that is active at an appropriate periodic signal edge (e.g., positive clock rise [also see the CLK waveform]). The read address (es) on A[**17**:**0**] may be stored in the address register, preferably on (in response to) the same periodic signal edge as for reading from the array. The RAM may access from one to n m-bit-wide data words and store each in an output register (e.g., Reg. **20** and Reg. **22** in FIG. **2**) on the same clock edge as that which latches the read address, but with one or more (preferably one) cycles of latency.

The RAM may access two data words with each read operation on the same clock edge as that which latches the read address. For example, referring to FIG. **2**, the two data words (or one double-width data word) may be driven from the Read Data Reg. to output registers **20** and **22** on a single clock edge, then the first or lower word of data may be driven through output buffer **12** onto the output data bus DOUT on the clock logic level resulting from the single clock edge that latches the data in output register **22**, provided any applied output control signal (e.g., an output enable signal OE) is asserted in an enabling state (e.g., LOW). On the subsequent clock transition, the second or higher order data word stored in output register **20** may be

latched in output register **24**, then driven through output buffer **10** onto the DOUT signals on the clock logic level resulting from the clock transition that latches the second data word in output register **24**, provided any applied ouput control signal remains asserted in an enabling state. In this configuration, all data may be available, for example, as soon as 3.5 ns after clock rise (assuming a 125 MHz read/write control signal), providing a read operation with essentially no cycles of latency.

On the same transitions of the subsequent clock cycle, the next data word(s) stored in the array is/are latched in the output register(s), then driven through the three-state output buffer onto the DOUT bus/pads on the same clock logic levels as before.

Read accesses can be initiated, for example, on every rising edge of the positive clock. Doing so will "pipeline" the data flow such that data is transferred out of the device on every rising and falling edge of the clock.

When deselected, the present RAM may first complete the pending read transactions. Synchronous internal circuitry may automatically three-state the outputs following the next rising edge of the positive clock. This will allow for a seamless transition between a port in the present RAM and any external device (including without limitation a second RAM according to the invention) without the insertion of wait states.

Table 1 below shows a truth table for the read port in the exemplary read operation. The identity and description of signal names in Table 1 can be found in Table 3 below.

address(es) presented to A[**17**:**0**] may be stored in the address register on the same clock edge as that which initiates the write operation. However, the information presented to the data inputs (e.g., DIN[**17**:**0**]) may be stored in the first input register (e.g., Write Data Reg. **1** in FIG. **2**) on the positive clock rise of CLK. On the falling edge of the positive clock, the information presented to DIN[**17**:**0**] is stored in the second input register (see Write Data Reg. **2** in FIG. **2**). On this falling positive clock edge, the corresponding 2 m-bit-wide word of data is written into the array.

Write accesses can be initiated on every falling edge of the same clock that initiates read accesses (or on the rising edges of the complementary clock). Doing so will pipeline the data flow such that data is transferred into and out of the device on every cycle of the clock.

When deselected, the input port will ignore all inputs thereto.

Table 2 above shows a truth table for the write port in the exemplary write operation. The identity and description of signal names in Table 2 can be found in Table 3 below.

The input and output ports in the present RAM architecture may operate independently of one another. One can read or write to any location in the memory array, regardless of the transaction address on the other port. Should the input and output ports access the same location on the same cycle of the periodic signal, the information presented to the data inputs may be forwarded to the data outputs (by, e.g., conventional bypass logic circuitry responsive to a control signal generated in response to an AND- or NAND-type logic comparison of the read and write addresses), or alternatively, the data stored in the output register may first be output on the data output bus, then the same location written with the new data.

TABLE 1

Read Port Cycle Description Truth Table[1,2]

Operation	Address used	RPS2	$\overline{RPS1}$	CLK	Comments
Deselected	—	X	H	L-H	$\overline{RPS1}$ deselects Read port. Outputs three-state following next rising edge of positive clock (CLK)
Deselected	—	0	X	L-H	RPS2 deselects Read Port. Outputs three-state following next rising edge of positive clock (CLK)
Begin Read	-External	1	0	L-H	Read operation initiated on previous clock rise. Address are stored in the Read Address Register. Following the next clock rise the first (lower order) word will be driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. On the subsequent falling edge of the positive clock (CLK) the second (higher order) word is driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. If the asynchronous $\overline{OE}$ is HIGH, the output buffers will remain in a three-state condition

Notes:
[1]X = Don't Care, 1 = Logic HIGH, 0 = Logic LOW.
[2]Device will power-up deselected and the outputs in a three-state condition, regardless of $\overline{OE}$.

Writing

As shown in FIG. **4**, write operations may be initiated by asserting an input port select signal (e.g., WPS*) that is active at an appropriate periodic signal edge (e.g., positive clock rise of CLK* or a falling edge of CLK). The write

TABLE 2

Write Port Cycle Description Truth Table

Operation	Address used	WPS2	$\overline{WPS}$	CLK	Comments
Deselected	—	X	H	L-H	$\overline{WPS1}$ deselects Write Port. All Write Port inputs are ignored.

TABLE 2-continued

Write Port Cycle Description Truth Table

Operation	Address used	WPS2	$\overline{WPS}$	CLK	Comments
Deselected	—	0	X	L-H	WPS2 deselects Write Port. All Write Port inputs are ignored.
Begin Read	-External	1	0	L-H	Read operation initiated. Address are stored in the Read Address Register. Following the next clock rise the first (lower order) word will be driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. On the subsequent falling edge of the positive clock (CLK) the second (higher order) word is driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. If the asynchronous $\overline{OE}$ is HIGH, the output buffers will remain in a three-state condition

The present RAM architecture may have one or more Port Select inputs for each port, allowing for easy depth expansion. Port Selects may be sampled on a particular edge or logic level of any periodic signal, but the input port select is preferably sampled on the rising edge of the positive clock input (CLK), and the output port select is preferably sampled on the falling edge of the positive clock input (CLK). Either port select input can deselect the specified port (e.g., an active output port select deselects the output port). Deselecting a port will not affect the other ports. All pending transactions (Read and/or Write) are preferably completed prior to the port being deselected.

The identity and description of signal names in FIG. **3** can be found in Table 3 below.

Reading and Writing

FIG. **5** shows the sequence of data transfer events occurring during read and write operations. Table 3 below shows the identity and description of the exemplary input signals shown and/or described in FIGS. **1–5**. The letters "A", "B", "C", etc., refer to addresses (e.g., word addresses for either two m-bit-wide words or one 2 m-bit-wide word) in the RAM array. The terms "D(A)", "D(B)", etc., and "D(A+1)", "D(B+1)", etc., respectively refer to a first or lower order data word and a second or higher order data word written to or read from the corresponding address "A", "B", "C", etc., when writing, e.g., m-bit-wide words and/or latching data into m-bit-wide input registers. Thus, for 2 m-bit-wide circuitry, "D(A)" and "D(A+1)", "D(B)" and "D(B+1)", etc., refer to a single 2 m-bit-wide data word. In this example, the signal "CS*" represents a logical combination of two external chip select signals (see CS**1** and CS**2** in Table 3 below).

As shown in FIG. **5**, address A is latched or written into the address register from the address bus during the positive clock CLK transition from LOW to HIGH. Address A is present on the address bus at a time about t_s ns before the crossover of CLK and CLK* (the "setup time"; see waveform A in FIG. **3**). The address is maintained on the address bus for a period of time of about (t_S+t_H) ns (the "setup and hold time"; see, e.g., waveform A in FIG. **3**). The read port select signal is asserted briefly (and preferably while the periodic signal(s) CLK and/or CLK* is/are transitioning), and the next rising transition of the periodic signal CLK latches the data words D(A) and D(A+1) from address A in the array(s) through the read data register into first and second output registers **20** and **22**. The HIGH logic level of CLK resulting from this transition enables output buffer **12** and outputs D(A) to the data output bus. For m-bit-wide circuitry, a complementary transition of the periodic signal may then latch data word D(A+1) from output register **20** and into a shadow register (e.g., register **24** in FIG. **2**). The LOW logic level of CLK resulting from this complementary CLK transition enables output buffer **10** and outputs D(A+1) onto the data output bus and the data output pads.

The first transition of the periodic signal CLK also latches the data word D(X) on the Data In bus into the first write register. Similar but complementary to the read operation described immediately above, address X is latched or written into the address register from the address bus during the second, falling CLK transition from HIGH to LOW. The new address signal, or address transition from A to X, occurs at least about t_S ns before the crossover of CLK and CLK*. The falling transition of the CLK pulse, sent on the clock generator-to-address register bus (see bus **30** in FIG. **2**), enables the address register to store the X address that is on the address bus at the time of the transition. Address X is also maintained for a period of time of about (t_S+t_H) ns.

Address X is latched into the address register from address bus A while the write port select signal is asserted (and while the periodic signal is transitioning). The second, complementary CLK transition (i.e., relative to the CLK transition that latches data word D(X) into the first write register) also latches data word D(X+1) on the Data In bus into the second write register, and writes the data words D(X) and D(X+1) at address X in the first and second arrays, respectively, as shown for example in FIG. **2**. Alternatively, for 2 m-bit-wide circuitry, the rising transition of the positive periodic signal CLK latches a single 2 m-bit-wide data word in a single write data register.

While the invention has been described in connection with certain preferred embodiments, it is not intended to limit the scope of the invention to the particular form set forth, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

TABLE 3

Pin Number	Name	I/O	Description
	$DIN_{[17:0]}$	Input-Synchronous	Data input signals, sampled on the rising and subsequent falling edge of CLK during the data portion of the write operations. The Data presented to $DIN_{[17:0}$ can be read from the device on $DOUT_{[17:0]}$.
	$\overline{WPS1}$ WPS2	Input-Synchronous	Write Port Selects, active LOW and HIGH, respectively. Sampled on the rising edge of CLK. When active, a write operation is intiated. $\overline{WPS1}$ and WPS2 are qualified with chip selects ($\overline{CS1}$ and CS2)
	$WA_{[17:0]}$	Input-Synchronous	Write Address inputs. Sampled on the rising edge of the CLK during a write operation. These inputs are ignored during the falling edge of the positive clock (CLK). These inputs are qualified with $\overline{WPS}$, $\overline{CS1}$ and CS2.
	$DOUT_{[17:0]}$	Outputs-	Data Outputs signals. These pins drive out the requested data during a Read operation. The data driven out on $DOUT_{[17:0]}$ is the same data written in on $DIN_{[17:0]}$.
	$\overline{RPS1}$ RPS2	Input-Synchronous	Read Port Selects, active LOW and HIGH, respectively. Sampled on the rising edge of CLK. When active, a read operation is intiated. $\overline{RPS1}$ and RPS2 are qualified with chip selects ($\overline{CS1}$ and CS2)
	$RA_{[17:0]}$	Input-Synchronous	Read Address inputs. Sampled on the rising edge of the CLK during a read operation. These inputs are ignored during the falling edge of the positive clock (CLK). These inputs are qualified with $\overline{RPS}$, $\overline{CS1}$ and CS2.
	$\overline{OE}$	Input-Asynchronous	Output Enable, active LOW. This is an asynchronous input that controls the output drivers of the device. When deselected using $\overline{RPS}$, the output drivers are automatically three-stated, regardless of the state of $\overline{OE}$.
	$\overline{CS1}$	Input-Synchronous	Chip Selects 1, active LOW. Sampled on the rising edge of the positive clock (CLK). This signal is used in conjunction with CS2 to select or deselect the device.
	CS2	Input-Synchronous	Chip Selects 2, active HIGH. Sampled on the rising edge of the positive clock (CLK). This signal is used in conjunction with $\overline{CS1}$ to select or deselect the device.
	CLK	Input-Clock	Positive Clock input. Used to capture all synchronous inputs to the device. All accesses are initiated on the rising edge of CLK. The crosspoint of CLK and $\overline{CLK}$ are used to capture all synchronous inputs to the device.
	$\overline{CLK}$	Input-Clock	Negative Clock input. Complimentary to CLK. The crosspoint of CLK and $\overline{CLK}$ are used to capture all synchronous inputs to the device. CLK is used to capture DIN and drive DOUT.
	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 2.5 V power supply.
	V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
	V_{DDQ}	Power Supply	Power supply inputs for the outputs of the device. Should be connected to 2.5 V power supply.
	V_{SSQ}	Ground	Ground for the outputs of the device. Should be connected to ground of the system.

What is claimed is:

1. A process for reading data from and writing data to a random access memory array, comprising the steps of:

transferring a first plurality of data bits on a first unidirectional bus to a random write address in said random access memory array in response to a first transition of a periodic signal, and

transferring a second plurality of data bits on a second unidirectional bus from a random read address in said random access memory array in response to a second, complementary transition of said periodic signal.

2. The process of claim **1**, wherein said second, complementary transition of said periodic signal is also the next transition following said first transition of said periodic signal.

3. A process for reading data from and writing data to a random access memory array, comprising the steps of:

transferring a first plurality of data bits on a first unidirectional bus from a random read address in said random access memory array in response to a first transition of a periodic signal, and

transferring a second plurality of data bits on a second unidirectional bus to a random write address in said random access memory array in response to a second, complementary transition of said periodic signal.

4. The process of claim **3**, wherein said second, complementary transition of said periodic signal is also the next transition following said first transition of said periodic signal.

5. The process according to claim **1**, wherein said periodic signal comprises a differential input clock pair having a first clock signal configured to generate said first transition and a second clock signal configured to generate said second transition.

6. The process according to claim **3**, wherein said periodic signal comprises a differential input clock pairs having a first clock signal configured to generate said first transition and a second clock signal configured to generate said second transition.

* * * * *

EXHIBIT D

US006445645B2

(12) **United States Patent**
Arcoleo et al.

(10) **Patent No.: US 6,445,645 B2**
(45) **Date of Patent: Sep. 3, 2002**

(54) **RANDOM ACCESS MEMORY HAVING INDEPENDENT READ PORT AND WRITE PORT AND PROCESS FOR WRITING TO AND READING FROM THE SAME**

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(73) Assignee: **Cypress Semiconductor Corporation**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/878,434**

(22) Filed: **Jun. 11, 2001**

Related U.S. Application Data

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(60) Provisional application No. 60/077,982, filed on Mar. 13, 1998.

(51) **Int. Cl.**[7] **G11C 8/00**

(52) **U.S. Cl.** **365/233**; 365/230.05; 365/189.04; 365/189.12; 365/189.05

(58) **Field of Search** 365/233, 233.5, 365/230.05, 189.04, 189.12, 189.05

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,169,284	A	9/1979	Hogan et al.	711/140
4,245,304	A	1/1981	Porter et al.	711/122
4,456,965	A	6/1984	Graber et al.	710/100
4,539,661	A	9/1985	Oritani	365/233.5
4,575,826	A	3/1986	Dean	365/222
4,599,708	A	7/1986	Schuster	365/174
4,752,871	A	6/1988	Sparks et al.	365/185.11
4,783,732	A	11/1988	Morton	365/230.05
4,849,937	A	7/1989	Yoshimoto	365/189.05
4,882,709	A	11/1989	Wyland	365/189.02
5,023,838	A	6/1991	Herbert	365/189.08
5,309,395	A	5/1994	Dickinson et al.	365/189.04
5,394,361	A	2/1995	Dickinson	365/189.04
5,440,717	A	8/1995	Bosshart	711/159
5,530,673	A	6/1996	Tobita et al.	365/185.09
5,546,569	A	8/1996	Proebsting et al.	713/600
5,561,781	A	10/1996	Braceras et al.	711/131
5,598,545	A	1/1997	Childers et al.	712/221
5,638,534	A	6/1997	Mote, Jr.	711/158
5,648,987	A	7/1997	Yang et al.	375/232
5,752,270	A	5/1998	Wada	711/169
5,781,480	A	7/1998	Nogle et al.	365/189.04
5,784,331	A *	7/1998	Lysinger	365/230.06
5,805,523	A *	9/1998	Lysinger	365/230.08
5,828,606	A	10/1998	Mick	365/189.05
5,838,631	A	11/1998	Mick	365/233
5,841,732	A	11/1998	Mick	365/233
5,875,151	A	2/1999	Mick	365/233
5,923,615	A *	7/1999	Leach et al.	365/238.5

(List continued on next page.)

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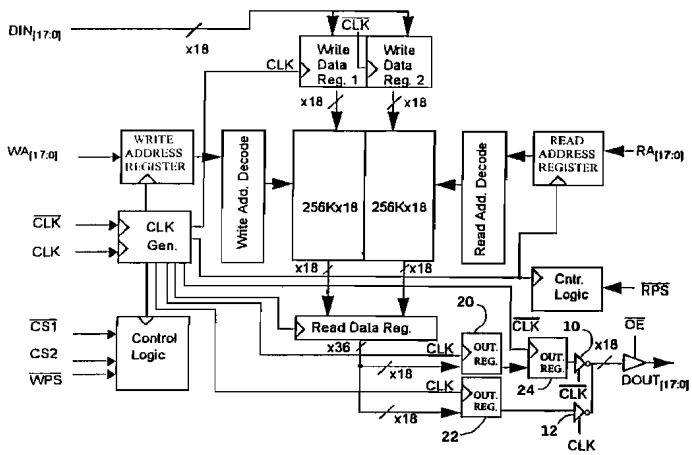
(57) **ABSTRACT**

A random access memory with a read port, a write port, a read/write control signal configured to control data transfer operations at the read port and/or the write port on both rising and falling transitions, and a first random access memory array configured to store and/or retrieve data at a first random address in the first random access memory array defined by one or more signals on a write address bus and/or a read address bus. One preferred embodiment further includes a write data register storing or latching data in response to a first transition of the read/write control signal, and the array storing data in response to a second transition of the read/write control signal. Other preferred embodiments further include an n·m-bits-wide input data bus coupling a set of data inputs to the write data register, and/or an n·m-bits-wide output data bus coupling the read data register to a set of data outputs, where n and m are each independently an integer >2.

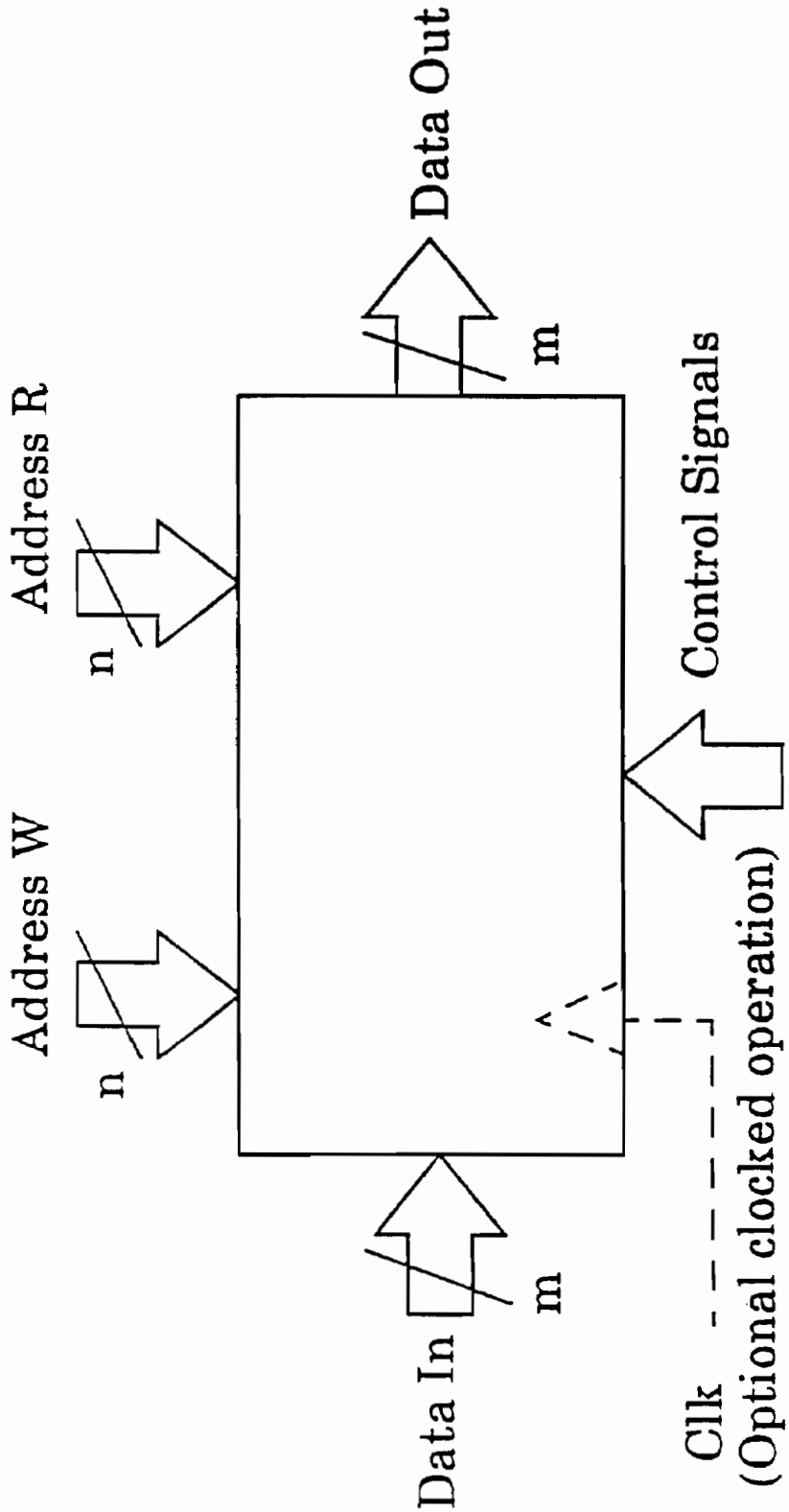
5 Claims, 5 Drawing Sheets



U.S. PATENT DOCUMENTS

5,926,426	A	7/1999	Han	365/205
5,956,286	A	9/1999	Lattimore et al.	365/230.05
5,978,279	A	11/1999	Park	365/189.04
5,983,328	A	11/1999	Potts et al.	711/157
6,069,839	A	5/2000	Pancholy et al.	365/233
6,081,478	A	6/2000	Mick et al.	365/233
6,094,399	A	7/2000	Mick	365/233
2001/0043506	A1 *	11/2001	Arcoleo et al.	365/233

* cited by examiner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Address R
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Address W
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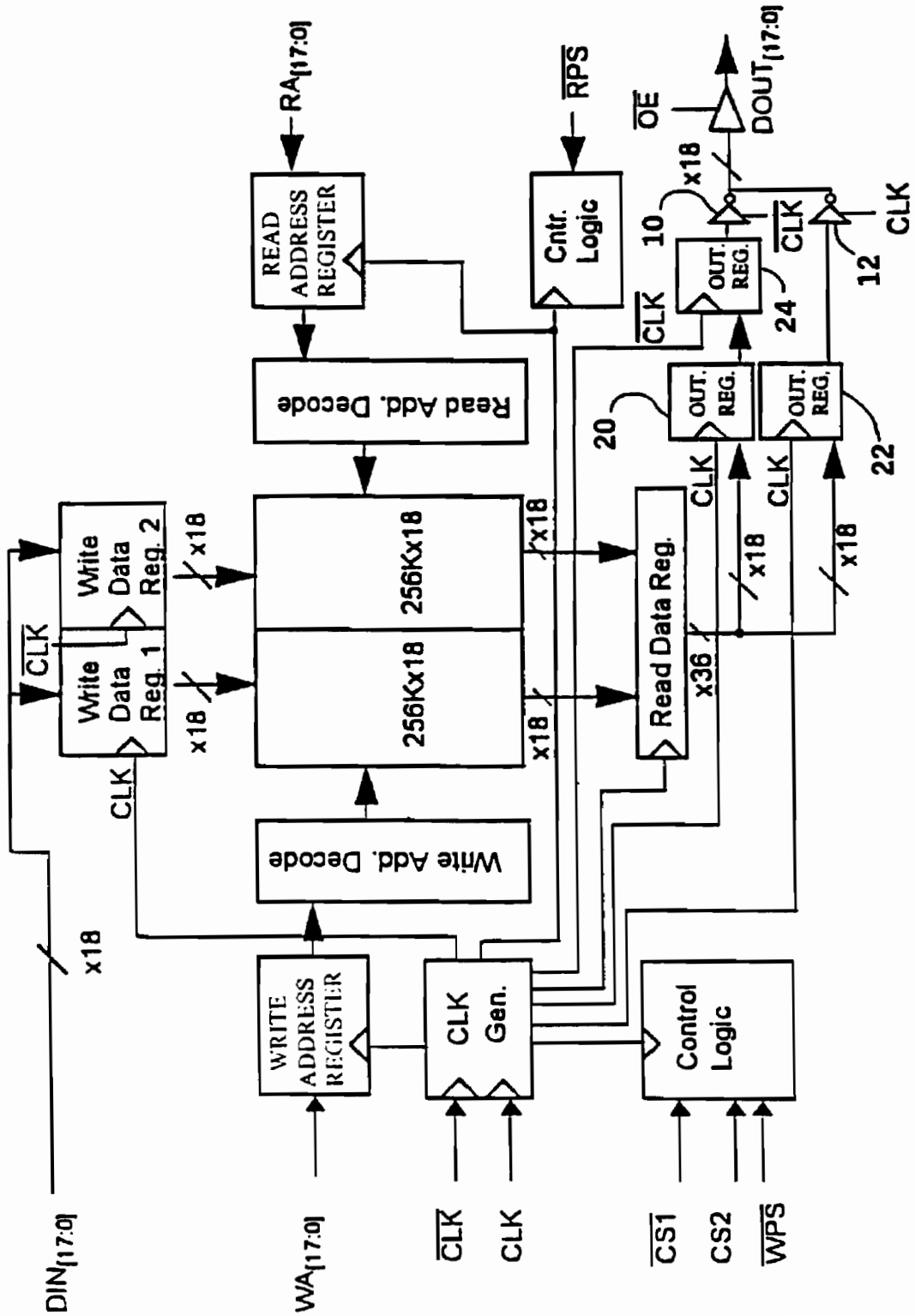
Control Signals
Data In
m
Clk
(Optional clocked operation)

Fig. 1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DOUT[17:0]
READ ADDRESS REGISTER
Cntr. Logic
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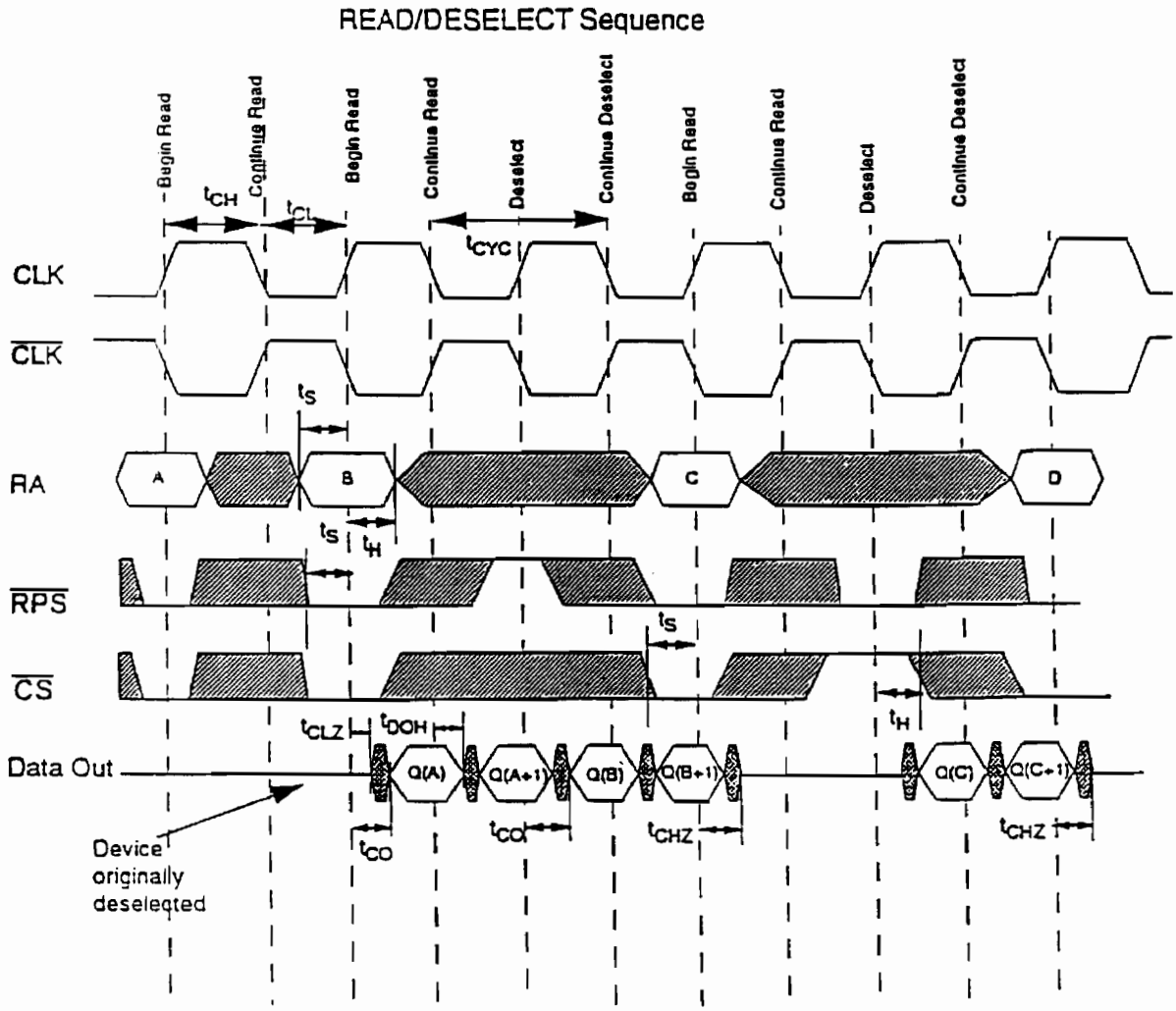
CLK
12
24
Read Add. Decode
20
OUT. REG.
OUT. REG.
22
Write Data Reg. 2
Write Data Reg. 1
x18
256Kx18
256Kx18
Read Data Reg.
x36
x18
x18
x18
x18
CLK
Write Add. Decode
x18
WRITE ADDRESS REGISTER
CLK Gen.
Control Logic
DIN[17:0]
WA[17:0]
CS1
CS2
WPS

Fig. 2

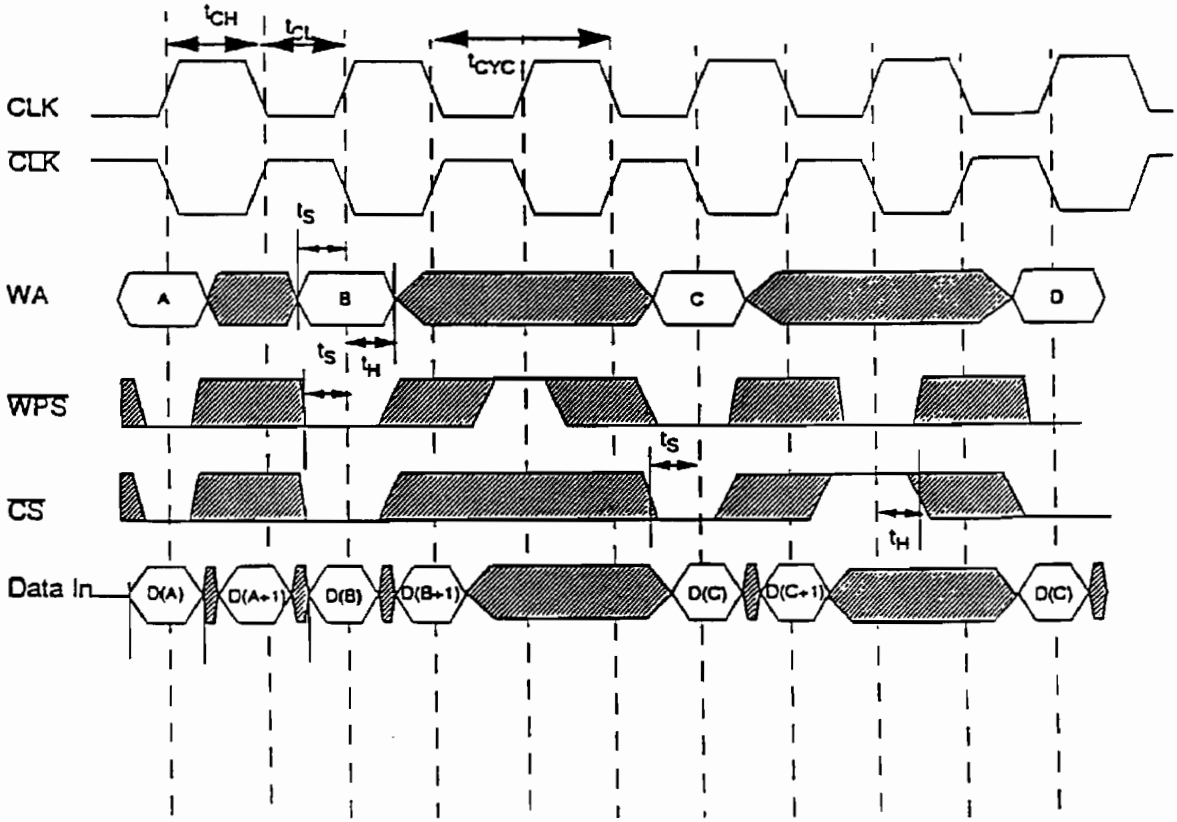


$\overline{CS}$ is the combination of $\overline{CS1}$, and CS2. Both chip enables need to be active in order to select the device. Any chip enable can deselect the device. $\overline{OE}$ held LOW. $\overline{RPS}$ is the combination of $\overline{RPS1}$ and RPS2.

= DON'T CARE = UNDEFINED

Fig. 3

WRITE/DESELECT Sequence

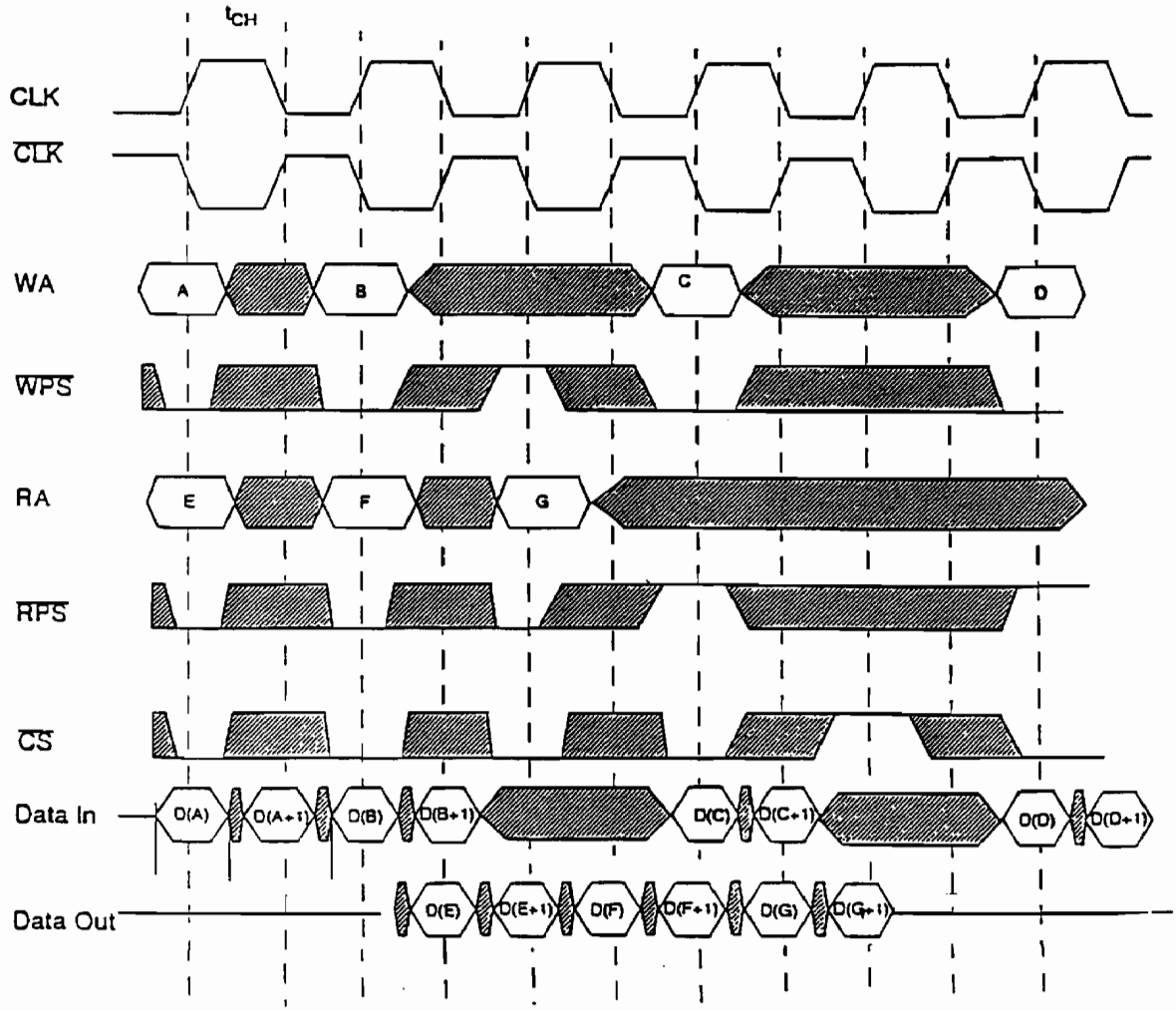


$\overline{CS}$ is the combination of $\overline{CS1}$, and CS2. Both chip enables need to be active in order to select the device. Any chip enable can deselect the device. $\overline{OE}$ held LOW. $\overline{WPS}$ is the combination of $\overline{WPS1}$ and WPS2.

= DON'T CARE = UNDEFINED

Fig. 4

READWRITE/DESELECT Sequence



$\overline{CS}$ is the combination of $\overline{CS1}$, and CS2. Both chip enables need to be active in order to select the device. Any chip enable can deselect the device. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Fig. 5

RANDOM ACCESS MEMORY HAVING INDEPENDENT READ PORT AND WRITE PORT AND PROCESS FOR WRITING TO AND READING FROM THE SAME

This is a divisional of U.S. Ser. No. 09/238,953, filed Jan. 27, 1999, now U.S. Pat. No. 6,262,936.

This application claims the benefit of U.S. Provisional Application No. 60/077,982, filed Mar. 13, 1998, and is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

This invention relates generally to the field of semiconductor and/or integrated circuit devices, and more particularly to a random access memory and process for writing to and reading from the same.

Summary of the Invention

The primary object of the invention is to provide a random access memory that increases data throughput.

Another object of the invention is to provide such a random access memory that may have either synchronous or asynchronous operation.

Another object of the invention is to provide a random access memory and method of operating the same in which read and write operations may be executed in the same clock cycle.

A further object of the invention is to provide a random access memory and method of operating the same in which read and write operations may be asynchronously enabled.

Yet another object of the invention is to provide such a random access memory and method of operating the same in which fully random addresses may be employed.

Still yet another object of the invention is to provide such a random access memory and method of operating the same in which successive and/or asserted addresses may be completely unrelated.

Another object of the invention is to provide such a random access memory and method of operating the same in which no restrictions are placed on successive and/or asserted addresses .

Another object of the invention is to provide such a random access memory and method of operating the same in which the same address may be used to read from and write to the memory in the same clock cycle.

A further object of the invention is to provide such a random access memory and method of operating the same in which a read/write control signal (e.g., a clock or control pulse) is the only control-type signal essential to operability.

Other objects and advantages of the present invention will become apparent from the following description, taken in connection with the accompanying drawings, wherein, by way of illustration and example, embodiments of the present invention are disclosed.

The present invention concerns a random access memory comprising: a write port comprising a set of data inputs and a write address bus, a read port comprising a set of data outputs and a read address bus,a read/write control signal configured to control data transfer operations at said write port and/or said read port in response to either (i) both rising and falling transitions or (ii) each of two logic levels of said read/write control signal, and a first random access memory array configured to store and/or retrieve data at a first random address in said first random access memory array defined by one or more signals on said write address bus and/or said read address bus.

In a further embodiment, the present invention concerns a process for reading data from and/or writing data to a random access memory array, comprising the steps of: (a) transferring a first plurality of data bits to or from a first random address in said random access memory array in response to a first transition of a read/write control signal, and (b) independently transferring a second plurality of data bits to or from a second random address in said random access memory array in response to a second transition of said read/write control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings constitute a part of this specification and include exemplary embodiments to the invention, which may be embodied in various forms. The features and advantages of the present invention are illustrated by way of example in the drawings, in which:

FIG. **1** shows an overview of the present random access memory (RAM) architecture;

FIG. **2** shows a more detailed embodiment of the RAM architecture shown in FIG. **1**;

FIG. **3** shows various waveforms illustrating relative timing of various signals in conjunction with an exemplary read operation performed according to the invention;

FIG. **4** shows various waveforms illustrating relative timing of various signals in conjunction with an exemplary write operation performed according to the invention; and

FIG. **5** shows various waveforms illustrating relative timing of various signals in conjunction with an exemplary read/write operation performed according to the invention.

It is to be understood that, in some instances, various aspects of the invention may be shown exaggerated or enlarged to facilitate an understanding of the invention, and in other instances, some aspects of the invention considered to be conventional may not be shown so as to avoid obfuscating more important aspects or features of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Detailed descriptions of the preferred embodiments are provided herein. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure or manner.

In the present random access memory, each of the read port and write port elements (i.e., the write address bus, the set of data inputs, the read address bus and the set of data outputs) may independently be m or n·m bits wide, where m is an integer $\geqq 2$, preferably $\geqq 4$, and more preferably $\geqq 8$,

and n is independently an integer ≧2, preferably of 2–4, and more preferably equal to 2. In specific examples, m may be 8, 9, 18, 32, 36, 64, 72, 128 or 144. When the port is, for example, a read port or an input port, the port may receive data from an external source. In a preferred embodiment, each port is unidirectional (i.e., data flows in one direction only; e.g., a read port functions as a dedicated output port and a write port functions as a dedicated input port).

The read/write control signal may be configured to control one or more data transfer operations at the first port and/or the second port on both its rising and falling transitions in a synchronous or asynchronous manner. Thus, a "read/write control signal" refers to any signal that controls any circuit function performed as part of a read operation or a write operation. For asynchronous operations, the read/write control signal may be a pulse signal generated, for example, in response to a first transition of a write address signal or an input data signal. For synchronous operations, the read/write control signal may be a periodic signal, such as an internal or external clock signal. There may be more than one independent read/write control signal controlling read, write, register and/or data pass gate functions. Where appropriate and/or desirable, the read/write control signals may comprise a first pulse or clock signal and its complement.

The present random access memory array may be configured to store and/or retrieve data at any random address therein. The address is defined by one or more signals on the write address bus and/or the read address bus.

The present random access memory may further comprise circuitry operable to write data into the array at a first random address in response to at least one transition of a read/write control signal. Preferably, the transition(s) of the read/write control signal to which such write circuitry responds generates a write enable or other write operation control signal in accordance with techniques and circuitry known to those skilled in the art.

Similarly, the present random access memory may further comprise circuitry operable to read data from a random location in the array in response to at least one transition of the read/write control signal, where the transition(s) of the read/write control signal to which such read circuitry responds generates a read enable or other read operation control signal in accordance with techniques and circuitry known to those skilled in the art.

As shown in FIG. **1**, the present random access memory (RAM) architecture comprises separate first and second ports (e.g., "Data In" and "Data Out") to access the memory array. Each port may have one or more dedicated address inputs (e.g., "Address W" and "Address R") to maintain complete independence of the ports and their associated control logic.

When one of the ports operates as a read port, it may have dedicated Data Outputs from the array to support Read operations. Similarly, when one of the ports operates as a write Port, it may have dedicated Data inputs to the array to support Write operations. Separated data inputs and outputs substantially or completely eliminates the need to "turn around" the data bus as may be required with common I/O devices. Accesses to the Read and Write ports may be completely independent of one another and may be initiated synchronously with one or more read/write control signals (e.g., a control pulse generated in response to a first transition of a data input signal or write address signal; an internal or external clock signal; a set of differential input clocks; etc.). In order to maximize data throughput, both Read and Write ports may transfer data on one or both of the rising and falling edges of the read/write control signal(s) (e.g., optional input clock "Clk"). Data transfer may also be logic level-triggered; i.e., it may occur in response to a particular or predetermined logic level of one or more read/write control signal(s).

The depth of the memory array may be, in effect, expanded with two or more RAM devices (e.g., integrated circuit chips) and their associated select logic circuitry. The port select inputs allow each port to operate as if it was an independent device, thereby further allowing depth expansion independently on each port.

All synchronous inputs may be passed through one or more write registers (or input registers) controlled by the read/write control signal(s). All data outputs may be passed through one or more read registers (and/or output registers), also controlled by the same or different read/write control signal(s).

All writes may be conducted with on-chip synchronous self-timed write circuitry to simplify the interface logic.

EXAMPLE(S)

As shown in FIG. **2**, the present RAM architecture is, in a preferred embodiment, configured as a synchronous pipelined Burst static RAM (SRAM) equipped with both an Input (write) Port and an Output (read) Port. The Read port is dedicated to Read operations and the Write Port is dedicated to Write operations. Data flows into the SRAM through the Write port, and out through the Read Port. Each port has its own address inputs (which may store or latch address data in separate read and write address registers) that allow it to operate independently. By separating the input and output ports, the present RAM avoids possible data contention and/or eliminates any need to "turn-around" the data bus.

Accesses for both ports may be controlled by a single clock or a pair of differential input clocks (CLK/CLK*, where a signal designated "X*" indicates the complement of the corresponding signal "X", similar to the signals in the Figures bearing an overstrike or "bar" designation). All synchronous timing may be referenced from the cross point of the differential input clock signals. Accesses can be initiated on any edge of any read/write control signal (preferably on the rising edge of a clock signal, assuming any other control signals are asserted at their active logic levels), but for ease and simplicity of logic circuitry, accesses are initiated on the rising edge of the positive clock (CLK) only.

All data inputs (e.g., synchronous inputs DIN[**17**:**0**]) may pass through one or more input registers (e.g., first and second registers WRITE DATA REG. **1** and WRITE DATA REG. **2** as shown in FIG. **2**) controlled by the rising and falling edge of the positive input clock (CLK). Although the random access memory shown in FIG. **2** comprises first and second write data registers, a single 2 m-bit-wide write data

register can substitute for the two m-bit-wide registers. In such a case, a 2 m-bit-wide data input bus may also be substituted for the m-bit-wide data input bus shown. The first m-bit or single n·m-bit write data register may store data in response to a first transition of the read/write control signal, and when present, the second write data register may store data in response to a second transition of the read/write control signal. In either case, the data in the write data register(s) is written into the array on the second transition of the read/write control signal, when the full 2 m-bit-wide word in latched into the write register(s).

The present random access memory may comprise first and second m-bit-wide arrays configured to store and/or retrieve data at a random address in each cell array defined by one or more signals on the write address bus and/or the read address bus, respectively. Alternatively, the present random access memory may comprise a n·m-bit-wide array, in which case the write data register and read data register are also n·m bits wide, and preferably, the internal and/or external data input and output busses are also n·m bits wide.

When the random access memory comprises a plurality of arrays (e.g., as shown in FIG. **2**), the first random access memory array receives data from the first write data register, and the second random access memory array receives data from the second write data register. Similarly, a random access memory comprising a plurality of arrays may further comprise a plurality of read data registers, the first read data register storing data transferred from the first random access memory array, and the second write data register storing data transferred from the second random access memory. In this case, the present random access memory may further comprise (a) first circuitry operable to write data to the random access memory array(s) at a first random address and (b) second circuitry operable to read data from the random access memory array(s) at a second random address, in response to successive or non-successive transitions of a read/write control signal, the second random address being the same as or different from the first random address.

All data outputs (e.g., synchronous outputs DOUT[17:0]) may pass through one or more output registers (e.g., 2m-bit-wide READ DATA REG., which may in the alternative be configured as first and second m-bit-wide read data registers) controlled by the rising and falling edge of the positive input clock (CLK). The read data register(s) may store data transferred from the random access memory array in response to a first transition of a read/write control signal. The random access memory shown in FIG. **2** may further comprise an m-bits-wide output data bus having first and second inputs respectively coupled to first and second read data registers. Alternatively, the present random access memory may comprise an n·m-bits-wide output data bus receiving n·m bits of data from an n·m-bits-wide read data register (or n m-bits-wide read data registers; the same principles may apply to the data input bus and the write data register[s]).

As shown in FIG. **2**, the present random access memory may further comprise an m-bits-wide data output bus, first and second three-state output buffers (e.g., buffers **10** and **12**), and first, second and third m-bits-wide output registers (e.g., Reg. **20**, Reg. **22** and Reg. **24**), wherein:

each of the first and second output registers store m bits of data from the read data register in response to a first read/write control signal,

the third output register stores m bits of data from the first output register in response to a second read/write control signal (which may be a complement of the first read/write control signal),

the first three-state output buffer is enabled to provide data to the output data bus from the third output register by a third read/write control signal (which may be [i] the same as or different from the second read/write control signal or [ii] a complement of the first read/write control signal, and which preferably enables data output in a particular or predetermined logic level or state), and

the second three-state output buffer is enabled to provide data to the output data bus from the second output register in response to a fourth read/write control signal (which may be [i] the same as or different from the first read/write control signal or [ii] a complement of the second read/write control signal, and which also preferably enables data output in a particular or predetermined logic level or state).

Alternatively, where the output data bus is n·m bits wide, one may substitute a single n·m-bits-wide output register and an optional output buffer (which may have three-state enablement as set forth above), n m-bits-wide output registers each with an optional output buffer (having optional three-state control as described above), or one may simply omit the output register(s) and/or output buffers completely.

Control inputs (e.g., one or more synchronous read port select inputs RPS or RPS*, one or more synchronous write port select inputs WPS or WPS*, etc.) may pass through input registers controlled by an edge of a read/write control signal (e.g., the rising edge of the positive clock input CLK). One may advantageously employ multiple read and/or write port select inputs (e.g., RPS1, RPS2, RPS1*, RPS2*, WPS1, WPS2, WPS1*, WPS2*, etc.) when one includes multiple random access memories in a given application (e.g., a data, voice and/or video communications device, such as a network switch or router). Preferably, each RAM in a given multiple-RAM application has at least one unique combination of read and at write port select signals that activate the particular port (e.g., RPS1* and RPS2, RPS1 and RPS2*, WPS1* and WPS2, WPS1 and WPS2*, etc.). Alternatively, the different read and/or write port select signals can select (enable or disable) one read or write register of a multiple-register configuration.

Transferring Data To and From the Array

In a further embodiment, the present invention relates to a process for reading data from and/or writing data to a random access memory array, comprising the steps of:

transferring a first plurality of data bits to or from a first random address in said random access memory array in response to a first transition of a read/write control signal, and

independently transferring a second plurality of data bits to or from a second random address in said random access memory array in response to a second transition of said read/write control signal.

Reading

As shown in FIG. **3**, read operations may be initiated by asserting a read port select signal (e.g., RPS*) that is active at an appropriate read/write control signal edge (e.g., posi-

tive clock rise [also see the CLK waveform]). The addresses on RA[17:0] may be stored in the Read address register, preferably on (in response to) the same read/write control signal edge as for reading from the array. The RAM may access two data words with each read operation on the same clock edge as that which latches the read address. For example, referring to FIG. **2**, the two data words (or double-width data word) may be driven from the Read Data Reg. to output registers **20** and **22** on a single clock edge, then the first or lower word of data may be driven through output buffer **12** onto the output data bus DOUT on the clock logic level resulting from the single clock edge that latches the data in output register **22**, provided any applied output control signal (e.g., an output enable signal OE) is asserted in an enabling state (e.g., LOW). On the subsequent clock transition, the second or higher order data word stored in output register **20** may be latched in output register **24**, then driven through output buffer **10** onto the DOUT signals on the clock logic level resulting from the clock transition that latches the second data word in output register **24**, provided any applied out control signal remains asserted in an enabling state. In this configuration, all data may be available, for example, as soon as 3.5 ns after clock rise (assuming a 125 MHz read/write control signal), providing a read operation with essentially no cycles of latency.

Read accesses can be initiated on every rising edge of the positive clock. Doing so will "pipeline" the data flow such that data is transferred out of the device on every rising and falling edge of the clock.

When deselected, the present RAM may first complete the pending read transactions. Synchronous internal circuitry may automatically three-state the outputs following the next rising edge of the positive clock. This will allow for a seamless transition between a port in the present RAM and any external device (including without limitation a second RAM according to the invention) without the insertion of wait states.

Table 1 below shows a truth table for the read port in the exemplary read operation. The identity and description of signal names in Table 1 can be found in Table 3 below.

TABLE 1

Read Port Cycle Description Truth Table[1,2]

Operation	Address used	RPS2	$\overline{RPS1}$	CLK	Comments
Deselected	—	X	H	L-H	$\overline{RPS1}$ deselects Read Port. Outputs three-state following next rising edge of positive clock (CLK)
Deselected	—	0	X	L-H	RPS2 deselects Read Port. Outputs three-state following next rising edge of positive clock (CLK)
Begin Read	External	1	0	L-H	Read operation initiated on previous clock rise. Address are stored in the Read Address Register. Following the next clock rise the first (lower order) word will be driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. On the subsequent failing edge of the positive clock (CLK) the second (higher order) word is driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. If the asynchronous $\overline{OE}$ is HIGH, the output buffers will remain in a three-state condition

Notes:
[1]X = Don't Care.
1 = Logic HIGH.
0 = Logic LOW.
[2]Device will power-up deselected and the outputs in a three-state condition, regardless of $\overline{OE}$.

Writing

As shown in FIG. **4**, write operations may be initiated by asserting a write port select signal (e.g., WPS*) that is active at an appropriate read/write control signal edge (e.g., positive clock rise [also see the CLK waveform]). The addresses presented to WA[17:0] may be stored in the write address register on the same positive clock rise as that which initiates the write operation. In addition, the information presented to the data inputs (e.g., DIN[17:0]) may be stored in the first (or a single) Write Data register on this same positive clock rise. On the following edge of the read/write control signal (e.g., the falling edge of the positive clock), the information presented to DIN[17:0] is stored in the second Write Data Register (see also the architecture example shown in FIG. **2**). On this following read/write control signal edge (and optionally, a subsequently asserted write contol signal such as a write enable signal WE generated by a conventional pulse generator from a rising clock transition, and applied to the wordline(s) of the RAM array corresponding to the address stored in the write address register), the corresponding 2m-bit-wide word of data is written into the array.

Write accesses can be initiated on every rising edge of the positive clock (or its complement). Doing so will pipeline the data flow such that data is transferred into the device on every rising and falling edge of the clock.

When deselected, the write port will ignore all inputs to the write port.

Table 2 below shows a truth table for the write port in the exemplary write operation. The identity and description of signal names in Table 2 can be found in Table 3 below.

TABLE 2

Write Port Cycle Description Truth Table

Operation	Address used	WPS2	$\overline{WPS1}$	CLK	Comments
Deselected	—	X	H	L-H	$\overline{WPS1}$ deselects Write Port. All Write Port inputs are ignored.
Deselected	—	0	X	L-H	WPS2 deselects Write Port. All Write Port inputs are ignored.
Begin Read	External	1	0	L-H	Read operation initiated. Address are stored in the Read Address Register. Following the next clock rise the first (lower order) word will be driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. On the subsequent falling edge of the positive clock (CLK) the second (higher order) word is driven out onto $DOUT_{[17:0]}$ provided $\overline{OE}$ is driven LOW. If the asynchronous $\overline{OE}$ is HIGH, the output buffers will remain in a three-state condition

The Read and Write ports in the present RAM architecture may operate completely independently of one another. Since each port may have an independent address input, one can Read or Write to any location in the memory array, regardless of the transaction on the other port. Should the Read and Write ports access the same location on the same edge of the read/write control signal (e.g., on the rising edge of the positive clock), the information presented to the data inputs is forwarded to the data outputs (by, e.g., conventional bypass logic circuitry responsive to a control signal generated in response to an AND- or NAND-type logic comparison of the read and write addresses). Alternatively, the data stored in the read data register may first be output on the data output bus, then the same location written with the new data.

The present RAM architecture may have one or more Port Select inputs for each port, allowing for easy depth expansion. Port Selects may be sampled on any edge of any read/write control signal, but is preferably sampled on the rising edge of the positive clock input (CLK). Either port select input can deselect the specified port (e.g., an active read port select deselects the read port). Deselecting a port will not affect the other port. All pending transactions (Read and/or Write) are preferably completed prior to the port being deselected.

Reading and Writing

FIG. **5** shows the sequence of data transfer events occurring during substantially simultaneous read and write operations. Table 3 below shows the identity and description of the exemplary input signals shown and/or described in FIGS. **1–5**. The letters "A", "B", "C", etc., refer to addresses (e.g., word addresses for m-bit-wide words) in the RAM array. The terms "D(A)", "D(B)", etc., and "D(A+1)", "D(B+1)", etc., respectively refer to a first or lower order data word and a second or higher order data word written to or read from the corresponding address "A", "B", "C", etc. (Alternatively, for 2 m-bit-wide circuitry, "D(A)" and "D(A+1)", "D(B)" and "D(B+1)", etc., refer to a single 2 m-bit-wide data word.) In this example, the signal "CS*" represents a logical combination of two external chip select signals (see CS**1** and CS**2** in Table 3 below).

As shown on FIG. **5**, when an address A is written into the write address register along bus WA, the write port select signal is asserted briefly (and preferably while the read/write control signal(s) CLK and/or CLK* is/are transitioning). The first transition of the read/write control signal CLK latches the first data word D(A) on the Data In bus in the first write register, and the next transition of the read/Write control signal CLK latches the next data word D(A+1) on the Data In bus into the second write register. (Alternatively, for 2 m-bit-wide circuitry, the first transition of the read/write control signal CLK latches a single 2 m-bit-wide data word in a single write data register.) The data words D(A) and D(A+1) may then be written into address A in the first and second arrays, respectively, as shown for example in FIG. **2**. Writing into the array(s) may be controlled by a synchronous or asynchronous control signal as described above (e.g., a rising CLK edge or a subsequently asserted, independently generated write enable signal), or alternatively, writing to the array(s) may not be gated or controlled by a control signal.

Similarly, when an address E is latched into the read address register along bus RA, the read port select signal is asserted briefly (and preferably while the read/write control signal is transitioning). The first transition of the read/write control signal latches data word(s) D(E) and D(E+1) from address E in the array(s) (e.g., into registers **20** and **22** in FIG. **2**) and outputs D(E) to the data outputs. For m-bit-wide circuitry, a complementary transition of the read/write control signal may then latch data word D(E+1) through a shadow register (e.g., register **24** in FIG. **2**) and onto the data output bus and the data outputs.

While the invention has been described in connection with certain preferred embodiments, it is not intended to limit the scope of the invention to the particular form set forth, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

TABLE 3

Pin Number	Name	I/O	Description
	$DIN_{[17:0]}$	Input-Synchronous	Data input signals, sampled on the rising and subsequent falling edge of CLK during the data portion of the write operations. The Data presented to $DIN_{[17:0}$ can be read from the device on $DOUT_{[17:0]}$.
	$\overline{WPS1}$ WPS2	Input-Synchronous	Write Port Selects, active LOW and HIGH, respectively. Sampled on the rising edge of CLK. When active, a write operation is initiated. $\overline{WPS1}$ and WPS2 are qualified with chip selects ($\overline{CS1}$ and CS2)
	$WA_{[17:0]}$	Input-Synchronous	Write Address inputs. Sampled on the rising edge of the CLK during a write operation. These inputs are ignored during the falling edge of the positive clock (CLK). These inputs are qualified with $\overline{WPS}$, $\overline{CS1}$ and CS2.
	$DOUT_{[17:0]}$	Outputs	Data Outputs signals. These pins drive out the requested data during a Read operation. The data driven out on $DOUT_{[17:0]}$ is the same data written in on $DIN_{[17:0]}$.
	$\overline{RPS1}$ RPS2	Input-Synchronous	Read Port Selects, active LOW and HIGH, respectively. Sampled on the rising edge of CLK. When active, a read operation is initiated. $\overline{RPS1}$ and RPS2 are qualified with chip selects ($\overline{CS1}$ and CS2)
	$RA_{[17:0]}$	Input-Synchronous	Read Address inputs. Sampled on the rising edge of the CLK during a read operation. These inputs are ignored during the falling edge of the positive clock (CLK). These inputs are qualified with $\overline{RPS}$, $\overline{CS1}$ and CS2.
	$\overline{OE}$	Input-Asynchronous	Output Enable, active LOW. This is an asynchronous input that controls the output drivers of the device. When deselected using $\overline{RPS}$, the output drivers are automatically three-stated, regardless of the state of $\overline{OE}$.
	$\overline{CS1}$	Input-Synchronous	Chip Selects 1, active LOW. Sampled on the rising edge of the positive clock (CLK). This signal is used in conjunction with CS2 to select or deselect the device.
	CS2	Input-Synchronous	Chip Selects 2, active HIGH. Sampled on the rising edge of the positive clock (CLK). This signal is used in conjunction with $\overline{CS1}$ to select or deselect the device.
	CLK	Input-Clock	Positive Clock input. Used to capture all synchronous inputs to the device. All accesses are initiated on the rising edge of CLK. The crosspoint of CLK and $\overline{CLK}$ are used to capture all synchronous inputs to the device.
	$\overline{CLK}$	Input-Clock	Negative Clock input. Complimentary to CLK. The crosspoint of CLK and $\overline{CLK}$ are used to capture all synchronous inputs to the device. CLK is used to capture DIN and drive DOUT.
	V_{DD}	Power Supply	Power supply inputs to the core cf the device. Should be connected to 2.5 V power supply.
	V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
	V_{DDQ}	Power Supply	Power supply inputs for the outputs of the device. Should be connected to 2.5 V power supply.
	V_{SSQ}	Ground	Ground for the outputs of the device. Should be connected to ground of the system.

What is claimed is:

1. A process for reading data from and/or writing data to a random access memory array, comprising the steps of:

(A) transferring a first plurality of data bits either to or from a first random address in response to a first transition or logic level of a read/write control signal, and

(B) independently transferring a second plurality of data bits either to or from a second random address in response to a second, complementary transition or logic level of said read/write control signal.

2. The process of claim **1**, wherein step (A) comprises a write operation and step (B) comprises a read operation.

3. The process of claim **1**, wherein step (A) comprises a read operation and step (B) comprises a write operation.

4. The process of claim **1**, wherein step (A) comprises a first read operation and step (B) comprises a second read operation.

5. The process of claim **1**, wherein step (A) comprises a first write operation and step (B) comprises a second write operation.

* * * * *

EXHIBIT E

US006967861B2

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Braceras et al.

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(45) **Date of Patent: Nov. 22, 2005**

(54) **METHOD AND APPARATUS FOR IMPROVING CYCLE TIME IN A QUAD DATA RATE SRAM DEVICE**

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(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

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(22) Filed: **Feb. 27, 2004**

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(51) **Int. Cl.**[7] **G11C 11/00**
(52) **U.S. Cl.** **365/154**; 365/156; 365/230.05
(58) **Field of Search** 365/154, 156, 365/230.05, 233, 194

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,381,363	A *	1/1995	Bazes	365/51
6,091,629	A *	7/2000	Osada et al.	365/156
6,201,757	B1 *	3/2001	Ward et al.	365/230.05
6,381,684	B1	4/2002	Hronik et al.	711/167
6,424,198	B1	7/2002	Wolford	327/291
6,600,693	B2	7/2003	Kim	365/233
6,862,208	B2 *	3/2005	Palmer et al.	365/154
2002/0060949	A1	5/2002	Kim	365/233

* cited by examiner

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(74) *Attorney, Agent, or Firm*—Robert A. Walsh; Cantor Colburn LLP

(57) **ABSTRACT**

A method for implementing a self-timed, read to write operation in a memory storage device. In an exemplary embodiment, the method includes capturing a read address during a first half of a current clock cycle, and commencing a read operation so as to read data corresponding to the captured read address onto a pair of bit lines. A write operation is commenced for the current clock cycle so as to cause write data to appear on the pair of bit lines as soon as the read data from the captured read address is amplified by a sense amplifier, wherein the write operation uses a previous write address captured during a preceding clock cycle. A current write address is captured during a second half of the current clock cycle, said current write address used for a write operation implemented during a subsequent clock cycle, wherein the write operation for the current clock cycle is timed independent of the current write address captured during said second half of the current clock cycle.

34 Claims, 4 Drawing Sheets

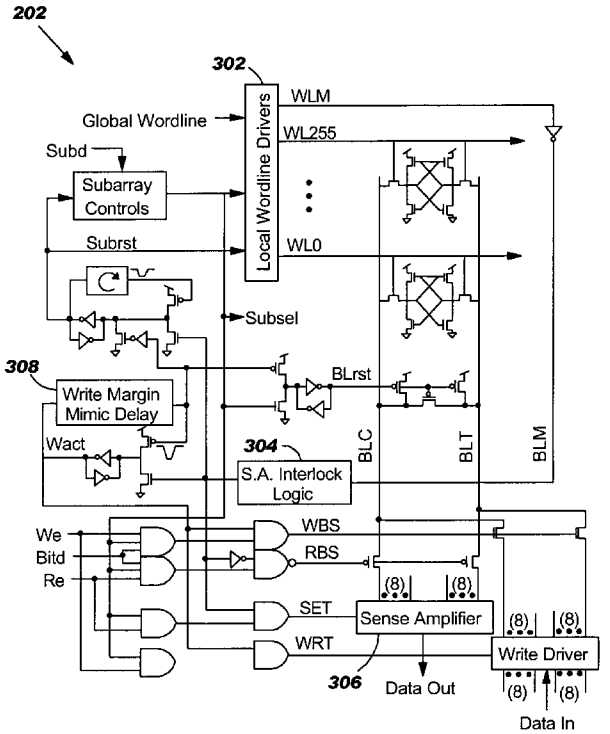


FIG. 1
Prior Art

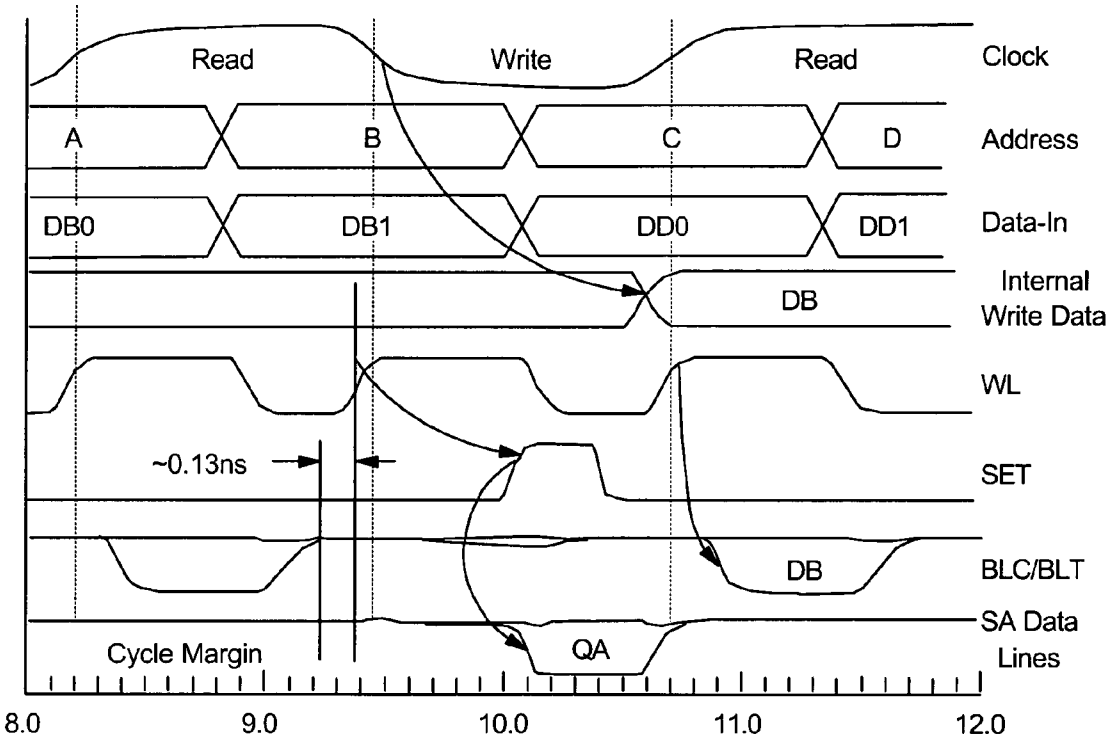


FIG. 2A

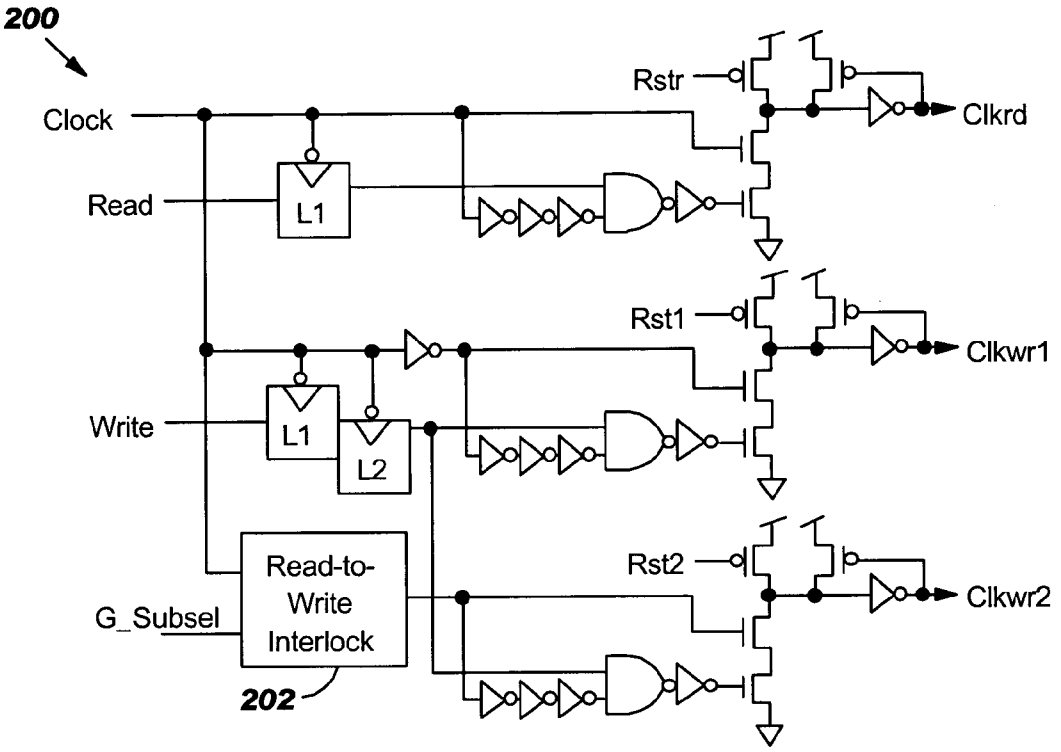


FIG. 2B

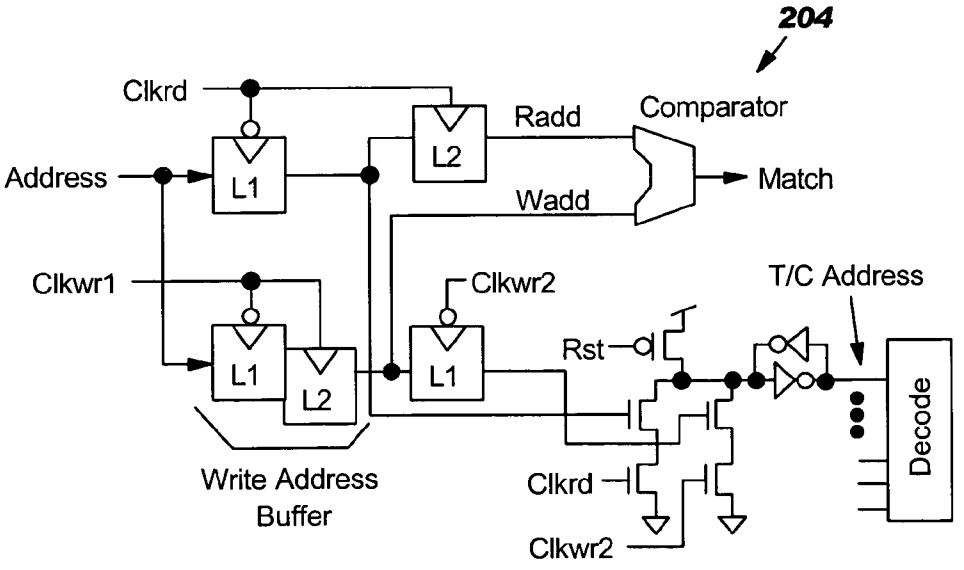


FIG. 3

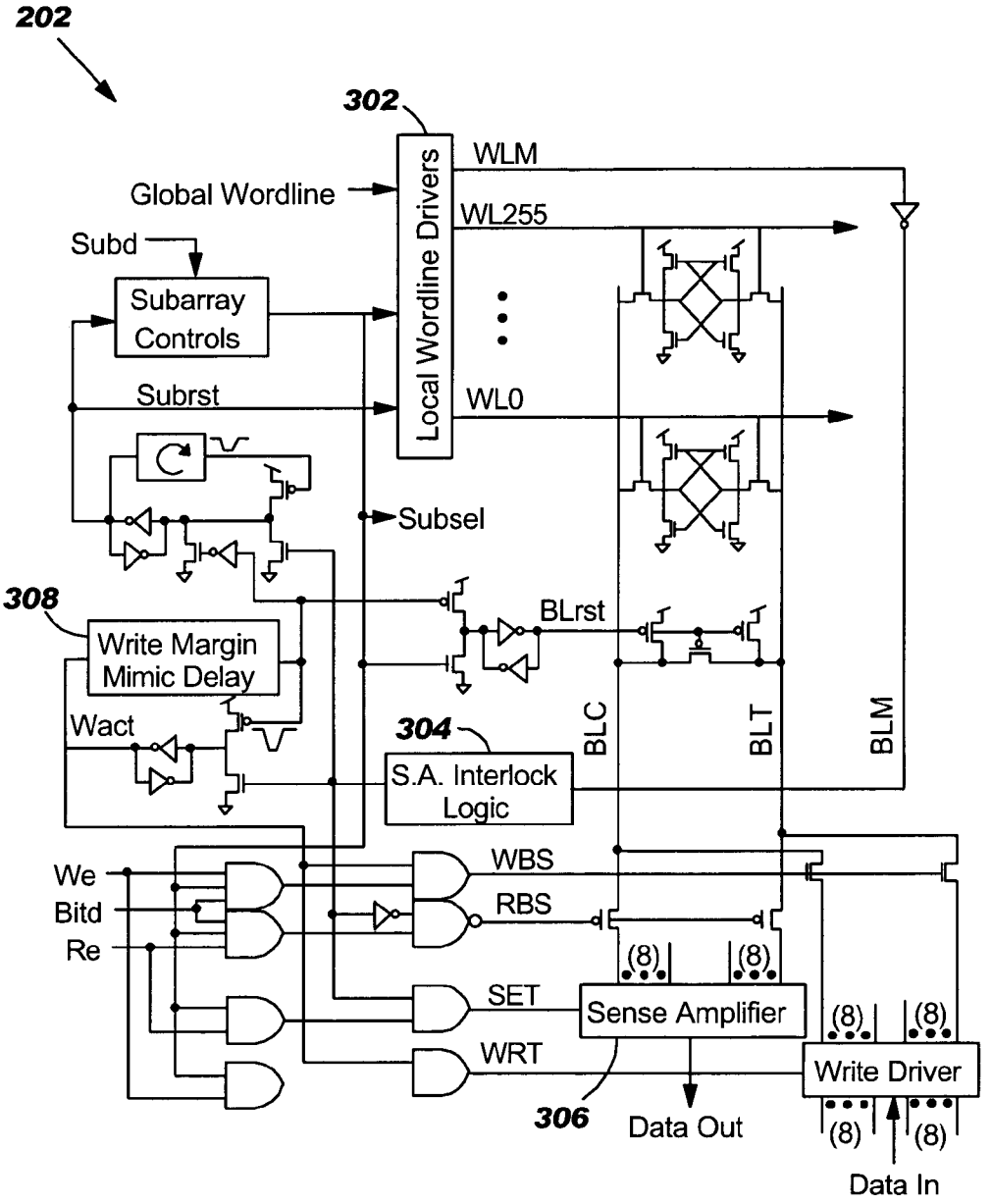
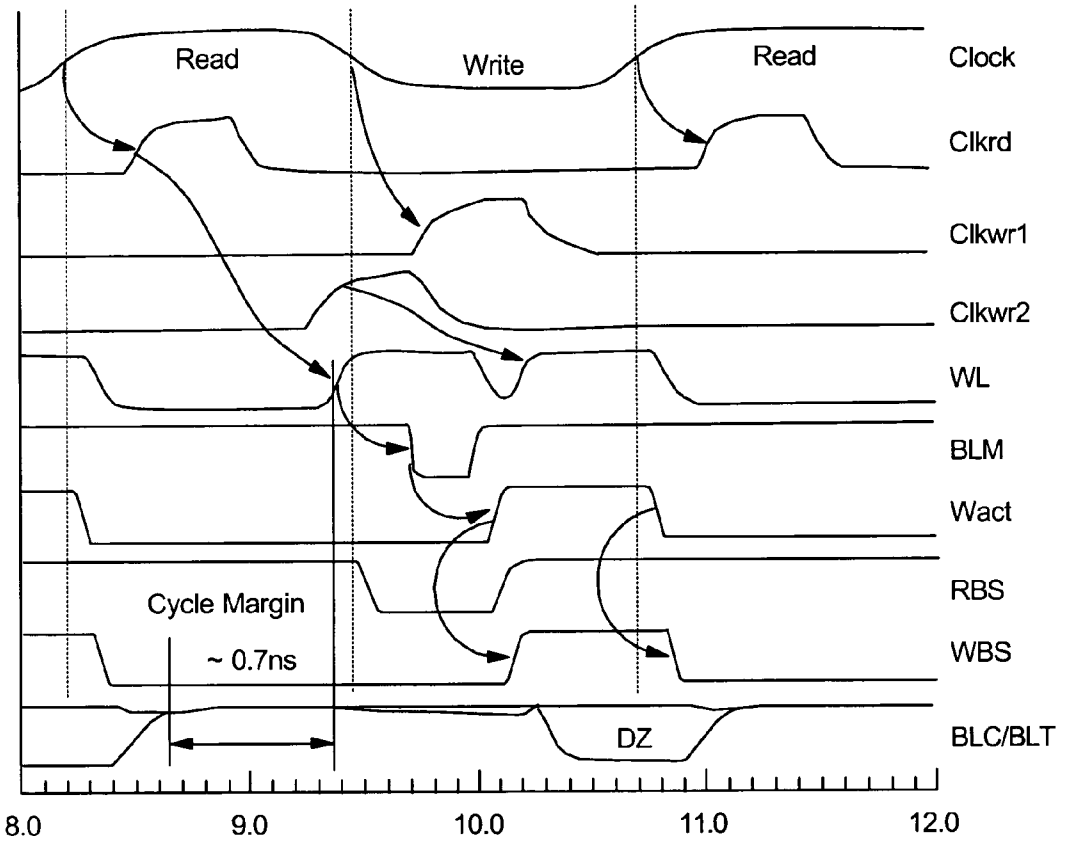


FIG. 4



METHOD AND APPARATUS FOR IMPROVING CYCLE TIME IN A QUAD DATA RATE SRAM DEVICE

BACKGROUND OF INVENTION

The present invention relates generally to integrated circuit memory devices and, more particularly, to a method and apparatus for improving cycle time in a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device.

Quad Data Rate (QDR) SRAM devices are currently being manufactured using a high-speed CMOS fabrication process. At the heart of the QDR architecture are two separate Double Data Rate (DDR) ports to allow simultaneous access to the memory storage array. Each port is dedicated, with one performing read operations while the other performs data write operations. By allowing two-way access to the memory array at DDR signaling rates, a quad data rate (QDR) is established.

A QDR SRAM system employs dual circuitry for both the address registers and logic controllers, thus allowing for the dual port architecture. While the WRITE port stores data into the memory storage array, the READ port can simultaneously retrieve data from therefrom. A single reference clock generator controls the speeds of both ports. One signal is passed to both logic controllers, resulting in a smooth flow of data. In addition, the clock generator controls the speed of the read and write data registers, providing consistent core bandwidth and operating rates. If individual timing signals were employed for each circuit, the signals could be slightly mismatched, thus resulting in a stall or crash of the memory system.

In earlier generation double data rate (DDR) devices, the core operations are directly timed from only the rising edge of the reference clock signal. As each address operation is performed, only two data operations can occur. Address operations are performed only during the rising edge of the clock signal. Because only one common data bus (port) is available, simultaneous read and write operations are not available with this technology. Unfortunately, even at higher megahertz clock speeds, DDR SRAM is challenged to provide sufficient bandwidth required by today's high-speed network communications equipment.

In comparison, the differences of QDR signaling versus DDR are evident. In order to facilitate a quad data rate, all data is carried by separate read and write ports. By using a DDR clock with two ports, information can be transferred at four data items per clock (assuming two operations are needed, one read and one write). However, notwithstanding the improved bandwidth provided by QDR SRAM in performing the read operation during the first half of the clock phase and the write operation during the second half of the clock phase, the maximum cycle time of the QDR SRAM is still limited since both the read and the write operations must be performed within one-half clock cycle. In essence, the SRAM performs a complete read and precharge, then a complete write and precharge, all within the same clock cycle.

Accordingly, it would be desirable to implement even further improvements in the cycle time of a QDR SRAM device, such as those used in high bandwidth applications like networking and communications systems.

SUMMARY OF INVENTION

The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a method for

implementing a self-timed, read to write operation in a memory storage device. In an exemplary embodiment, the method includes capturing a read address during a first half of a current clock cycle, and commencing a read operation so as to read data corresponding to the captured read address onto a pair of bit lines. A write operation is commenced for the current clock cycle so as to cause write data to appear on the pair of bit lines as soon as the read data from the captured read address is amplified by a sense amplifier, wherein the write operation uses a previous write address captured during a preceding clock cycle. A current write address is captured during a second half of the current clock cycle, said current write address used for a write operation implemented during a subsequent clock cycle, wherein the write operation for the current clock cycle is timed independent of the current write address captured during said second half of the current clock cycle.

In another embodiment, a method for implementing a self-timed, read to write protocol for a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device includes capturing a read address during a first half of a current clock cycle, and commencing a read operation so as to read data corresponding to the captured read address onto a pair of bit lines. A write operation is commenced for the current clock cycle so as to cause write data to appear on the pair of bit lines as soon as the read data from the captured read address is amplified by a sense amplifier, wherein the write operation uses a previous write address captured during a preceding clock cycle. A current write address is captured in a write address buffer during a second half of the current clock cycle, the current write address to be used for a write operation implemented during a subsequent clock cycle, wherein the write operation for the current clock cycle is timed independent of the current write address captured during the second half of the current clock cycle.

BRIEF DESCRIPTION OF DRAWINGS

Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures:

FIG. **1** is a timing diagram illustrating the operation of a conventionally configured network QDR SRAM device;

FIGS. **2**(*a*) and **2**(*b*) are schematic diagrams of an apparatus for implementing a self-timed, read to write protocol for a QDR SRAM device, in accordance with an embodiment of the invention;

FIG. **3** is a schematic diagram illustrating the read to write interlock portion of the apparatus shown in FIG. **2**(*a*); and

FIG. **4** is a timing diagram illustrating a simulation of the self-timed, read to write protocol, in accordance with a further embodiment of the present invention.

DETAILED DESCRIPTION

Disclosed herein is a method and apparatus for improving cycle time in a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, in which write addresses and data are captured and buffered to be used in a subsequent read to write cycle thus allowing the write operation to be timed immediately after the read operation. The start of the write operation does not wait until addresses and data are captured. Instead, the write address and data captured in the preceding cycle is used for the write operation of the current cycle, while the write address and data captured the current cycle is actually written in the next cycle.

In a conventionally configured network QDR SRAM device, the protocols dictate a read operation during the first

half of the clock cycle and a write operation during the second half of the clock cycle. For example, as illustrated in the timing diagram of FIG. **1**, addresses A and B correspond to the read and write addresses, respectively. The write data for address B is input in double data rate mode on both the rising and falling edges of the clock signal. The write operation may only start as soon as the corresponding write addresses and data are captured and distributed internally, as reflected by the Internal Write Data signal in FIG. **1**. During the read cycle, activation of the word line (WL) signal starts a bit line signal development as shown by the signal differential on the complement and true bit-lines BLC/BLT. Then, the sense amplifier (SA) data lines are amplified once the SET signal is activated.

Following the read cycle, the write WL is decoded and the write data (DB) is written to the bit lines. In this protocol, cycle time margin is measured from the completion of the previous write cycle to the activation of the read WL for the current cycle. In the example illustrated, the 2.5 ns external cycle simulation of FIG. **1** shows a cycle time margin of only about 0.13 ns.

Therefore, in accordance with an embodiment of the invention, there is disclosed a method and apparatus for improving cycle time in a QDR SRAM device. Briefly stated, an improvement in the cycle time is achieved by implementing a self-timed read to write protocol in which write addresses and data are captured and buffered during a given read to write cycle are actually written in the next read to write cycle. As such, the write operation (of data and address captured in the previous cycle) may be timed immediately after the read operation of the current cycle. This capability is realized, in part, by generating a pair of write clock signals: one write clock for capturing previous cycle write and address data, and another write clock (delayed) for launching the internal write address captured during the previous cycle.

Referring generally now to FIGS. **2**(*a*) and **2**(*b*), there is shown a schematic diagram of one possible embodiment of an apparatus **200** for implementing a self-timed read to write protocol for a QDR SRAM device. In particular, apparatus **200** generates three self-resetting clock signals (labeled "Clkrd", "Clkwr**1**", "Clkwr**2**") from read/write commands, as well as a system clock (labeled "Clock"). The signals Clkrd and Clkwr**1** are used to capture read and write addresses from rising and falling edges of Clock, respectively. In addition, Clkrd is also used to generate internal true and complement data addresses. Clkwr**2** is a delayed version of Clkrd that is used to launch the internal write address from the current buffered write address (i.e., the earlier write-cycle address) previously captured by Clkwr**1**.

It will be appreciated that the Clkwr**2** timing is not critical, since the precise timing between read and write cycles in a given array (or subarray) is locally controlled therein. As described in further detail hereinafter, a read to write interlock **202** includes sense amplifier interlock logic used to drive a set signal to the array sense amplifiers for a read operation, to isolate the sense amplifier from the bit lines through a pair of read bit switches, to enable a subarray (including word line) reset operation, and to enable a write activate signal that activates a pair of write bit switches for beginning the write operation.

As shown in FIG. **2**(*b*), address compare logic **204** is used to fetch read data directly from a write data buffer, rather from than the array itself, whenever data from the address to be read has not yet been written to memory. Thus, the read address (Radd) and the write address (Wadd) are compared with one another on every write cycle, wherein a signal (Match) is generated if the two addresses are equal.

FIG. **3** is a schematic diagram illustrating the read to write interlock **202** shown in FIG. **2**(*a*). As is shown, signals "Subd", "We", "Re"and "Bitd"are subarray-decode, write, read and bit-decode pulse input controls signals to the subarray, which is accessed through a plurality of local word line drivers **302**. For a selected subarray, the signal "Subsel"disables the bit line restore (i.e., precharging) devices through the signal labeled "BLrst", and also enables the individual word lines (e.g., WL**0** . . . WL**255**) and read bit switches (through signal RBS). In addition, through the use of a mimic (i.e., dummy) word line (WLM) and bit line (BLM), a signal sent therethrough is capable of tracking the delay through an actual word line and bit line. Moreover, WLM/BLM is also used to time the bit line signal development to as to ensure an adequate signal development at the sense amplifier.

As indicated earlier, the sense amplifier interlock logic **304** includes four functions: driving the SET signal to the sense amplifier(s) **306**; disabling the read bit switches (through signal RBS) in order to isolate the sense amplifier from the bit lines; enabling a subarray reset (including read word line reset); and enabling signal WRT to activate a pair of write bit switches (activated by signal WBS) to start the write operation. Once the write operation begins, a Write Margin Mimic Delay circuit **308** times the duration of the write operation. The mimic delay circuit **308** provides a more precise timing of the write to the cell, as compared to the previous approach of using a read mimic bit line delay. The end of the write operation occurs when the mimic delay circuit disables signal WBS, enables precharging signal BLrst, and regenerates a second "Subrst"pulse that restores the write word line. Thus, the subarray timings are restored twice: first at the setting of the sense amplifier, and then again at the end of the write duration pulse.

FIG. **4** is a timing diagram illustrating a simulation of the self-timed, read to write protocol, in accordance with a further embodiment of the present invention. At the first rising edge of the main clock, the read portion of the read to write cycle commences. Internally, it is noted the write operation for the previous half-cycle is finishing up, as reflected by the deactivation of the previously addressed word line (signals WL, Wact go from high to low), and the deactivation of the write bit switches (WBS also goes low) to decouple the bit line pair from the write driver. In addition, the fully developed data signal on the bit lines BLC/BLT disappears as the voltage on both is restored to the precharge value of V_{DD}.

At some point during the read half-cycle, the internally generated read clock signal Clkrd (from FIG. **2**(*a*)) goes high to capture the read data and address for the current cycle. Once the addressed wordline signal (WL) is activated by going high and the read bit switches are activated (by RBS going low), an appropriate signal development takes place on the bit line pair BLC/BLT which will then be set and driven to the full swing value by the sense amplifier. It will also be noted, however, that at about the same point in time as the word line signal goes high for the read operation, the internally generated clock signal Clkwr**2** (the delayed version of Clkrd) is activated to begin the write operation immediately after the sense amplifier captures the read data.

Again, the write operation for a given cycle does not depend upon waiting to capture write data and address information during the second half of the current clock cycle, because such information was already captured in the prior cycle. Thus, Clkwr**2** is generated from Clkrd to launch

the previously captured write address after the current read address is launched. The active low signal on the mimic bit line (BLM) activates write activation signal Wact, which in turn enables signal WBS for immediate writing of the write data (DZ) onto the bit line pair. There is no need to precharge the bit line pair once the read data is captured by the sense amplifier BL restore after the read operation; as can be seen in FIG. **4**, once the read word line signal is reset and the read bit switches are disabled (RBS goes high), the bit line pair is driven by write data. Finally, after the execution of the write margin mimic delay (i.e., the falling edge of signal Wact) the write bit switches are uncoupled, the write word line is restored and the bit lines BLC/BLT are precharged.

As will be appreciated, the cycle time margin achieved in the simulation of FIG. **4** is about 0.7 ns, which is a significant improvement over 0.13 ns in the conventional scheme of FIG. **1**. Given a 2.5 ns external cycle, then, a cycle time margin of 0.7 ns allows the external cycle time to be reduced to about 1.8 ns.

While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A method for implementing a self-timed, read to write operation in a memory storage device, the method comprising:

capturing a read address during a first half of a current clock cycle;

commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;

commencing a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

capturing a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

2. The method of claim **1**, further comprising:

generating an internal read clock signal from a main clock signal;

generating a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and

generating a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;

wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

3. The method of claim **2**, further comprising implementing sense amplifier interlock logic to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier.

4. The method of claim **3**, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

5. The method of claim **4**, wherein said sense amplifier interlock logic is used to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, and said sense amplifier interlock logic is further used to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

6. The method of claim **5**, wherein said sense amplifier interlock logic is used to reset a subarray of the memory storage device and disable a read-operation word line prior to the start of said write operation.

7. The method of claim **6**, wherein said sense amplifier interlock logic is used to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit configured to simulate the timing margin of said write operation.

8. The method of claim **6**, wherein said sense amplifier interlock logic is used to control the operation of said write driver.

9. A method for implementing a self-timed, read to write protocol for a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, the method comprising:

capturing a read address during a first half of a current clock cycle;

commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;

commencing a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

capturing, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

10. The method of claim **9**, further comprising:

generating an internal read clock signal from a main clock signal;

generating a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and

generating a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;

wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

11. The method of claim **10**, further comprising implementing sense amplifier interlock logic to enable said write operation to cause write data to appear on said pair of bit

lines as soon as said read data from said captured read address is amplified by said sense amplifier.

12. The method of claim **11**, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

13. The method of claim **12**, wherein said sense amplifier interlock logic is used to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, and said sense amplifier interlock logic is further used to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

14. The method of claim **13**, wherein said sense amplifier interlock logic is used to reset a subarray of the memory storage device and disable a read-operation word line prior to the start of said write operation.

15. The method of claim **14**, wherein said sense amplifier interlock logic is used to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit configured to simulate the timing margin of said write operation.

16. The method of claim **14**, wherein said sense amplifier interlock logic is used to control the operation of said write driver.

17. The method of claim **9**, further comprising:

comparing said current write address in said write address buffer with said current read address; and

upon determining a match between said current read address and said current write address, fetching said read data from a write data buffer.

18. A semiconductor memory storage device, comprising:

circuitry configured to capture a read address during a first half of a current clock cycle;

circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;

circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

circuitry configured to capture a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

19. The memory storage device of claim **18**, further comprising:

circuitry configured to generate an internal read clock signal from a main clock signal;

circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and

circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;

wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

20. The method of claim **19**, further comprising sense amplifier interlock logic configured to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier.

21. The memory storage device of claim **20**, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

22. The memory storage device of claim **21**, wherein said sense amplifier interlock logic is configured to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, said sense amplifier interlock logic further configured to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

23. The method of claim **22**, wherein said sense amplifier interlock logic is configured to reset a subarray of the memory storage device and disable a read-operation word line prior to the start of said write operation.

24. The memory storage device of claim **23**, wherein said sense amplifier interlock logic is configured to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit configured to simulate the timing margin of said write operation.

25. The memory storage device of claim **22**, wherein said sense amplifier interlock logic is configured to control the operation of said write driver.

26. A Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, comprising:

circuitry configured to capture a read address during a first half of a current clock cycle;

circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;

circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

circuitry configured to capture, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

27. The QDR SRAM device of claim **26**, further comprising:

circuitry configured to generate an internal read clock signal from a main clock signal;

circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and

circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;

wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

28. The QDR SRAM device of claim 27, further comprising sense amplifier interlock logic configured to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier.

29. The QDR SRAM device of claim 28, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

30. The QDR SRAM device of claim 29, wherein said sense amplifier interlock logic is configured to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, said sense amplifier interlock logic further configured to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

31. The QDR SRAM device of claim 30, wherein said sense amplifier interlock logic is configured to reset a subarray of the memory storage device and disable a read-operation word line prior to the start of said write operation.

32. The QDR SRAM device of claim 31, wherein said sense amplifier interlock logic is configured to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit configured to simulate the timing margin of said write operation.

33. The QDR SRAM device of claim 30, wherein said sense amplifier interlock logic is configured to control the operation of said write driver.

34. The QDR SRAM device of claim 26, further comprising:

a comparator configured to compare said current write address in said write address buffer with said current read address; and

circuitry configured to fetch said read data from a write data buffer upon determination of a match between said current read address and said current write address.

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