JS 44 CAND (Rev. 12/11)

CIVIL COVER SHEET

ORIGINAL

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. *(SEE INSTRUCTIONS ON NEXT PAGE OF THIS FORM.)*

I. (a) PLAINTIFFS
STMicroelectronics, Inc.

(b) County of Residence of First Listed Plaintiff Dallas County, TX
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorneys *(Firm Name, Address, and Telephone Number)*
Sean Pak, Quinn Emanuel Urquhart & Sullivan, LLP
50 California St., 22nd Floor, San Francisco, CA 94111
415-875-6600

DEFENDANTS
InvenSense, Inc.

County of Residence of First Listed Defendant Santa Clara, CA
(IN U.S. PLAINTIFF CASES ONLY)

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE TRACT OF LAND INVOLVED.

Attorneys *(If Known)*

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12-2475 JSC

II. BASIS OF JURISDICTION *(Place an "X" in One Box Only)*

- ☐ 1 U.S. Government Plaintiff
- ☒ 3 Federal Question *(U.S. Government Not a Party)*
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity *(Indicate Citizenship of Parties in Item III)*

III. CITIZENSHIP OF PRINCIPAL PARTIES *(Place an "X" in One Box for Plaintiff and One Box for Defendant)*
(For Diversity Cases Only)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated *or* Principal Place of Business In This State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated *and* Principal Place of Business In Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. NATURE OF SUIT *(Place an "X" in One Box Only)*

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- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
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- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
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- ☐ 290 All Other Real Property

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- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury
- ☐ 362 Personal Injury - Med. Malpractice

PERSONAL INJURY
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- ☐ 368 Asbestos Personal Injury Product Liability

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- ☐ 371 Truth in Lending
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- ☐ 535 Death Penalty
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition
- ☐ 560 Civil Detainee - Conditions of Confinement

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- ☐ 864 SSID Title XVI
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V. ORIGIN *(Place an "X" in One Box Only)*

☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district *(specify)* ☐ 6 Multidistrict Litigation

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing *(Do not cite jurisdictional statutes unless diversity)*:
Patent Laws of the United States, 35 U.S.C. §§ 1 et seq.

Brief description of cause:
Patent Infringement

VII. REQUESTED IN COMPLAINT:

☐ CHECK IF THIS IS A CLASS ACTION UNDER F.R.C.P. 23

DEMAND $

CHECK YES only if demanded in complaint:
JURY DEMAND: ☒ Yes ☐ No

VIII. RELATED CASE(S) IF ANY *(See instructions)*:

JUDGE _____ DOCKET NUMBER _____

IX. DIVISIONAL ASSIGNMENT (Civil L.R. 3-2)

(Place an "X" in One Box Only) ☐ SAN FRANCISCO/OAKLAND ☐ SAN JOSE ☐ EUREKA

DATE 5/15/12

SIGNATURE OF ATTORNEY OF RECORD Sean Pak

ORIGINAL

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E-filing

FILED
MAY 16 2012
RICHARD W. WIEKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

CV 12 2475

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

STMICROELECTRONICS, INC., Plaintiff, vs. INVENSENSE, INC., Defendant.	CASE NO. **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

Plaintiff STMicroelectronics, Inc. ("STI") alleges for its complaint against Defendant InvenSense, Inc. ("InvenSense") as follows:

INTRODUCTION

1. This is an action for patent infringement brought before this Court pursuant to 28 U.S.C. §§ 1331 and 1338(a). STI seeks remedies for InvenSense's infringement of one or more claims of each of United States Patents Nos. 6,504,253; 6,846,690; 6,405,592; 6,546,799; 6,928,872; 7,450,332; 7,409,291; 5,874,850; and 5,986,861 (collectively, "the Asserted Patents"). True and correct copies of the Asserted Patents are attached hereto as Exhibits A-I.

PARTIES

2. STMicroelectronics, Inc. is a corporation organized and existing under the laws of the State of Delaware, having its corporate headquarters and principal place of business at 750 Canyon Drive, Coppell, Texas 75019. STI is a subsidiary of STMicroelectronics NV, a Netherlands corporation, and does business in the Northern District of California. STI, STMicroelectronics N.V., and their various subsidiaries and affiliates are hereinafter referred to as "ST."

3. On information and belief, InvenSense: (i) is a corporation organized under the laws of the state of Delaware, having its corporate headquarters and principal place of business at 1197 Borregas Avenue, Sunnyvale, CA 94089; (ii) may be served with process by serving its Delaware registered agent The Corporation Trust Company, The Corporation Trust Center, 1209 Orange Street, Wilmington, Delaware 19801; and (iii) does business in the Northern District of California.

JURISDICTION AND VENUE

4. This lawsuit is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 101, *et seq.* Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. This Court has personal jurisdiction over InvenSense for at least the following reasons: (i) on information and belief, InvenSense's corporate headquarters and principal place

of business are located in the Northern District of California; (ii) InvenSense has committed acts of patent infringement, and/or contributed to or induced acts of patent infringement by others, in this District and elsewhere in California and the United States; (iii) InvenSense regularly does business or solicits business, engages in other persistent courses of conduct, and/or derives substantial revenue from products and/or services provided to individuals in this District and in this State; and (iv) InvenSense has purposefully established substantial, systematic, and continuous contacts with this District and expects or should reasonably expect to be sued here. Thus, this Court's exercise of jurisdiction over InvenSense will not offend traditional notions of fair play and substantial justice.

6. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391(b)-(c) and 1400(b) because InvenSense does business in the State of California, has committed acts of infringement in this State and in this District, a substantial part of the events or omissions giving rise to this complaint occurred in this District, and InvenSense is subject to and has previously subjected itself to personal jurisdiction in this District. Moreover, InvenSense's corporate headquarters are located in this District.

INTRADISTRICT ASSIGNMENT

7. This is an Intellectual Property Action to be assigned on a district-wide basis pursuant to Civil Local Rule 3-2(c).

BACKGROUND

ST's MEMS Innovations

8. ST is a global leader in the semiconductor market serving customers across the spectrum of sense and power technologies and multimedia convergence applications. Since its inception, ST has maintained an unwavering commitment to research and development ("R&D"). STI and the other ST companies make a substantial investment in the research and development of inventions and other intellectual property. Almost one quarter of the world-wide employees of ST work in R&D and/or product design, and ST has advanced research and development centers around the world including in the United States. Today, STI and the other

ST companies own over 21,500 patents and pending patent applications worldwide, including over 7,500 issued U.S. patents and 2,500 pending U.S. patent applications.

9. One area in which ST has made a substantial and long-term R&D investment is in the field of Micro-Electro-Mechanical Systems ("MEMS"). ST launched the consumer MEMS revolution through the combination of innovative product design, manufacturing know-how, deep application expertise, and bold and timely infrastructure investments. ST was the first major manufacturer in the world to start producing MEMS on 8-inch silicon wafers. ST also developed the THELMA (Thick Epi-Poly Layer for Microactuators and Accelerometers) surface micro-machining process for use in manufacturing both accelerometers and gyroscopes. In addition, ST introduced the world's first high-performance 3-axis MEMS gyroscope.

10. One of the first applications of ST's MEMS was the "Free Fall" feature in notebook computers to protect data. ST's MEMS are also used in devices such as smart phones, tablets, personal media players, game consoles, digital still camera, remotes and other applications with motion-activated interfaces.

11. ST is the leading supplier by revenue of MEMS devices for consumer and mobile MEMS. Building on its track record of success, ST continues to invest in MEMS R&D and innovative applications for MEMS.

The Asserted Patents

12. STI is the owner by assignment of all rights, title, and interest in the Asserted Patents, including the right to bring this suit for injunctive relief and damages.

13. **U.S. Patent No. 6,504,253** ("the '253 patent"), entitled "Structure For Electrically Connecting A First Body Of Semiconductor Material Overlaid By A Second Body Of Semiconductor Material Composite Structure Using Electric Connection Structure," was duly and legally issued by the United States Patent and Trademark Office on January 7, 2003.

14. **U.S. Patent No. 6,846,690** ("the '690 patent"), entitled "Integrated Circuit Comprising An Auxiliary Component, For Example A Passive Component Or A Microelectromechanical System, Placed Above An Electronic Chip, And The Corresponding

Fabrication Process," was duly and legally issued by the United States Patent and Trademark Office on January 25, 2005.

15. **U.S. Patent No. 6,405,592** ("the '592 patent"), entitled Hermetically-Sealed Sensor With A Movable Microstructure," was duly and legally issued by the United States Patent and Trademark Office on June 18, 2002.

16. **U.S. Patent No. 6,546,799** ("the '799 patent"), entitled "Method For Compensating The Position Offset Of A Capacitive Inertial Sensor, And Capacitive Inertial Sensor," was duly and legally issued by the United States Patent and Trademark Office on April 15, 2003.

17. **U.S. Patent No. 6,928,872** ("the '872 patent"), entitled "Integrated Gyroscope Of Semiconductor Material With At Least One Sensitive Axis In The Sensor Plane," was duly and legally issued by the United States Patent and Trademark Office on August 16, 2005.

18. **U.S. Patent No. 7,450,332** ("the '332 patent"), entitled "Free-Fall Detection Device And Free-Fall Protection System For A Portable Electronic Apparatus," was duly and legally issued by the United States Patent and Trademark Office on November 11, 2008.

19. **U.S. Patent No. 7,409,291** ("the '291 patent"), entitled "Device For Automatic Detection Of States Of Motion and Rest, And Portable Electronic Apparatus Incorporating It," was duly and legally issued by the United States Patent and Trademark Office on August 5, 2008.

20. **U.S. Patent No. 5,874,850** ("the '850 patent"), entitled "MOS Voltage Elevator Of The Charge Pump Type," was duly and legally issued by the United States Patent and Trademark Office on February 23, 1999.

21. **U.S. Patent No. 5,986,861** ("the '861 patent"), entitled "CLAMP," was duly and legally issued by the United States Patent and Trademark Office on November 16, 1999.

InvenSense Infringes STI's Patents

22. On information and belief, InvenSense was incorporated in California in June 2003 and reincorporated in Delaware in January 2004.

23. InvenSense competes, or seeks to compete, with STI in the United States and other ST companies around the world in the MEMS market. On information and belief, InvenSense offers four primary product families: (1) MPU (MotionProcessing Units); (2) IMU (Inertial Measurement Units); (3) Digital Gyroscopes; and (4) Analog Gyroscopes.

24. InvenSense has infringed, and continues to infringe, the Asserted Patents. As of April 3, 2011, InvenSense claims to have sold over 110 million units of MEMS products.

25. InvenSense's infringing MEMS products are sold by InvenSense with the expectation that they will be incorporated into consumer electronic products that are purchased, used and/or sold in, or imported to, the United States, including in the Northern District of California. As stated on its website, InvenSense's MEMS gyroscopes "have been designed into digital still cameras and camera phones for image stabilization; GPS devices for dead reckoning; and 3D peripherals such as 3D mice, TV remote controls, and game controllers. There are millions of consumer electronic products and applications incorporating the Company's integrated dual-axis gyros."

26. On information and belief, InvenSense designs its MEMS products in the United States and particularly in the Northern District of California.

27. InvenSense's Registration Statement, as amended, for its initial public offering ("Registration Statement") further touted that "in 2011, its ITG/IMU/MPU-3000 family of products started high volume shipments for the portable gaming, digital television and set-top box remote control, smart phone and tablet markets." In a September 14, 2011 press release, InvenSense announced that "it is shipping in volume the MPU-6050 product to handset and tablet OEMs and ODMs." On information and belief, by way of example, InvenSense's infringing products are intended for use in, and are incorporated into, devices such as the following in order to enable motion-based applications:

- Gaming devices, such as Nintendo Wii MotionPlus Accessory, Nintendo Wii Remote Plus Controller, Nintendo 3DS and Roku 2 XS (which incorporate, by way of example, InvenSense's infringing MEMS products, such as ITG-3205, IDG-600, ITG-3270 and/or IMU-3000)

- TV remotes, such as LG's Magic Motion Remote Control (which incorporate, by way of example, InvenSense's infringing products, such as IXZ-500);

- Air mice, such as Logitech MX Air Mouse and the Air Mouse Elite from Gyration (which incorporate, by way of example, InvenSense's infringing products, such as IDG-300); and

- Smart phones, such as LG's Optimus Black P970 (which incorporate, by way of example, InvenSense's infringing products, such as MPU-3050).

28. In addition, InvenSense indirectly infringes the Asserted Patents. InvenSense induces distributors, consumers, and end-users to directly infringe the Asserted Patents by selling or using its MEMS products, including those identified above and herein. InvenSense's marketing, sales, and customer support materials instruct customers to use infringing features of its MEMS products in an infringing manner. For example, InvenSense's website provides customers and potential customers with product specifications, technical papers and other marketing materials for InvenSense's MEMS products that tout their infringing features and instruct customers to use them in an infringing manner. On information and belief, InvenSense also provides verbal and written instructions, including sales support and technical know-how, to its distributors and customers that intentionally aid, assist, and encourage infringement.

29. InvenSense's MEMS products – which it sells directly, as well as through its distribution partners, to consumers and assemblers – are designed to be used (and are used by said parties) in an infringing manner. Additionally, on information and belief, InvenSense's MEMS products were especially designed, made, and/or adapted for use in an infringing manner. InvenSense's MEMS products either embody the claimed inventions on their own or are material, non-staple components of end-user products that embody the claimed inventions, which components have no substantial non-infringing uses. In fact, as part of its Registration Statement, InvenSense touted its "direct customer engagement model": "We work directly with

large original equipment manufacturer (OEM) customers to assist them in developing solutions and applications that may lead to more demand for our products. . . . For our larger OEM customers, we believe that our direct customer engagement approach, ecosystem partnerships and adoption of our APIs into major software operating systems provides us with significant differentiation in the customer sales process by aligning us more closely with the changing needs of these OEM customers and their end markets. We actively utilize field application engineers as part of our sales process to better engage the customer with our products. . . . Our direct customer engagement model extends to service and support."

InvenSense Knowingly Induced And Contributed To The Infringement Of Others

30. InvenSense is, and has been on notice of, one or more of the Asserted Patents and its infringement thereof since at least February 2012. In or around December 2011, the parties engaged in license negotiations during which ST identified particular patents that InvenSense was infringing. In or around February 2012, ST made various presentations to InvenSense that demonstrated how certain InvenSense products infringed certain patent claims of various ST patents, including the '253, '592, '332, '291, '850 and '861 patents-in-suit. Despite such notice, InvenSense has failed to cease its infringement. Instead, InvenSense continues to sell its infringing products and encourage its customers to use InvenSense products in an infringing manner.

InvenSense's Infringement Harms STI

31. STI is harmed by InvenSense's use of STI's patented technologies in a way that cannot be remedied by monetary damages alone. InvenSense has received substantial revenue and increased its market share by selling products that incorporate STI's technology without having to incur the costs of developing or licensing this technology.

32. On information and belief, InvenSense's infringement has caused STI to suffer irreparable harm due to, among other things, lost business opportunities, lost market share, and price erosion. Even if InvenSense were to subsequently pay past due royalties, lost profits, or other damages, there is no reason to believe that InvenSense would stop infringing, and it would

still enjoy the market share it has developed while infringing upon the Asserted Patents. Due to the difficulty in predicting whether, if at all, STI can recover this market share, STI's harm cannot be compensated by payment of monetary damages alone.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 6,504,253

33. STI incorporates by reference the preceding averments set forth in paragraphs 1-32.

34. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '253 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's ITG-3200 product line.

35. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

36. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

37. STI has been and continues to be damaged by InvenSense's infringement of the '253 Patent in an amount to be determined at trial.

38. On information and belief, InvenSense's infringement of the '253 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 6,846,690

39. STI incorporates by reference the preceding averments set forth in paragraphs 1-38.

40. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '690 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's ITG-3200 product line.

41. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

42. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

43. STI has been and continues to be damaged by InvenSense' infringement of the '690 Patent in an amount to be determined at trial.

44. On information and belief, InvenSense's infringement of the '690 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 6,405,592

45. STI incorporates by reference the preceding averments set forth in paragraphs 1-44.

46. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '592 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's ITG-3200 product line.

47. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

48. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

49. STI has been and continues to be damaged by InvenSense's infringement of the '592 Patent in an amount to be determined at trial.

50. On information and belief, InvenSense's infringement of the '592 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 6,546,799

51. STI incorporates by reference the preceding averments set forth in paragraphs 1-50.

52. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '799 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's MPU-6050 product line.

53. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

54. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

55. STI has been and continues to be damaged by InvenSense's infringement of the '799 Patent in an amount to be determined at trial.

56. On information and belief, InvenSense's infringement of the '799 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT V: INFRINGEMENT OF U.S. PATENT NO. 6,928,872

57. STI incorporates by reference the preceding averments set forth in paragraphs 1-56.

58. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '872 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's ITG-3200 product line.

59. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

60. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

61. STI has been and continues to be damaged by InvenSense's infringement of the '872 Patent in an amount to be determined at trial.

62. On information and belief, InvenSense's infringement of the '872 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 7,450,332

63. STI incorporates by reference the preceding averments set forth in paragraphs 1-62.

64. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '332 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's MPU-6050 product line.

65. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

66. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

67. STI has been and continues to be damaged by InvenSense's infringement of the '332 Patent in an amount to be determined at trial.

68. On information and belief, InvenSense's infringement of the '332 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT VII: INFRINGEMENT OF U.S. PATENT NO. 7,409,291

69. STI incorporates by reference the preceding averments set forth in paragraphs 1-68.

70. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '291 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States

without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's MPU-6050 product line.

71. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

72. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

73. STI has been and continues to be damaged by InvenSense's infringement of the '291 Patent in an amount to be determined at trial.

74. On information and belief, InvenSense's infringement of the '291 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT VIII: INFRINGEMENT OF U.S. PATENT NO. 5,874,850

75. STI incorporates by reference the preceding averments set forth in paragraphs 1-74.

76. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '850 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's IDG-500 product line.

77. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

78. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

79. STI has been and continues to be damaged by InvenSense's infringement of the '850 Patent in an amount to be determined at trial.

80. On information and belief, InvenSense's infringement of the '850 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT IX: INFRINGEMENT OF U.S. PATENT NO. 5,986,861

81. STI incorporates by reference the preceding averments set forth in paragraphs 1-80.

82. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '861 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's IMU-3000 product line.

83. On information and belief, InvenSense's infringement, contributory infringement and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

84. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

85. STI has been and continues to be damaged by InvenSense's infringement of the '861 Patent in an amount to be determined at trial.

86. On information and belief, InvenSense's infringement of the '861 Patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

REQUEST FOR RELIEF

WHEREFORE, Plaintiff STMicroelectronics, Inc. respectfully requests that:

(a) Judgment be entered that InvenSense has infringed one or more claims of each of the Asserted Patents;

(b) Judgment be entered permanently enjoining InvenSense, its directors, officers, agents, servants and employees, and those acting in privity or in concert with them, and their subsidiaries, divisions, successors and assigns, from further acts of infringement, contributory infringement, or inducement of infringement of the Asserted Patents;

(c) Judgment be entered awarding STI all damages adequate to compensate it for InvenSense's infringement of the Asserted Patents including all pre-judgment and post-judgment interest at the maximum rate permitted by law and enhanced damages;

(d) Judgment be entered that this is an exceptional case and awarding STI attorneys' fees and costs; and

(e) Judgment be entered awarding STI such other and further relief as this Court may deem just and proper.

DATED: May 16, 2012

QUINN EMANUEL URQUHART & SULLIVAN, LLP

By Sean Pak
Sean Pak
Attorneys for STMicroelectronics, Inc.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

STMICROELECTRONICS, INC., Plaintiff, vs. INVENSENSE, INC., Defendant.	Case No. **DEMAND FOR JURY TRIAL**

TO EACH PARTY AND TO THE COUNSEL OF RECORD FOR EACH PARTY:

Plaintiff STMicroelectronics, Inc. hereby demands a jury trial in the above-titled action pursuant to Rule 38(b) of the Federal Rules of Civil Procedure.

DATED: May 16, 2012

Respectfully submitted,

QUINN EMANUEL URQUHART & SULLIVAN, LLP

By: Sean Pak

Sean Pak
Attorneys for STMicroelectronics, Inc.

EXHIBIT A

US006504253B2

(12) **United States Patent**
Mastromatteo et al.

(10) **Patent No.: US 6,504,253 B2**
(45) **Date of Patent: Jan. 7, 2003**

(54) **STRUCTURE FOR ELECTRICALLY CONNECTING A FIRST BODY OF SEMICONDUCTOR MATERIAL OVERLAID BY A SECOND BODY OF SEMICONDUCTOR MATERIAL COMPOSITE STRUCTURE USING ELECTRIC CONNECTION STRUCTURE**

(75) Inventors: **Ubaldo Mastromatteo**, Bareggio (IT); **Fabrizio Ghironi**, Bareggio (IT); **Roberto Aina**, Bareggio (IT); **Mauro Bombonati**, Abbiategrasso (IT)

(73) Assignee: **STMicroelectronics S.r.l.**, Agrate Brianza (IT)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/844,180**

(22) Filed: **Apr. 27, 2001**

(65) **Prior Publication Data**

US 2001/0038148 A1 Nov. 8, 2001

(30) **Foreign Application Priority Data**

Apr. 28, 2000 (EP) 00830314

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52; H01L 29/40

(52) **U.S. Cl.** **257/758**; 257/723; 257/686; 257/688; 438/622; 438/118; 438/107

(58) **Field of Search** 257/723, 686, 257/777, 698, 774, 688, 680, 678, 758; 438/106, 108, 109, 110, 107, 118, 622

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,239,312 A		12/1980	Myer et al.	339/17 N
4,660,066 A		4/1987	Reid	357/30
4,807,021 A	*	2/1989	Okumura	257/75
4,939,568 A		7/1990	Kato et al.	357/75
5,270,261 A	*	12/1993	Bertin et al.	438/209
5,640,049 A	*	6/1997	Rostoker et al.	257/758
5,756,395 A		5/1998	Rostoker et al.	438/622
6,087,719 A	*	7/2000	Tsunashima	257/723
6,362,518 B1	*	3/2002	Yatsuda	257/678

FOREIGN PATENT DOCUMENTS

EP 0 317 084 A2 5/1989

OTHER PUBLICATIONS

Schmidt, M., "Wafer–to–Wafer Bonding for Microstructure Formation," *Proceedings of the IEEE*, 86(8):1575–1585, Aug. 1998.

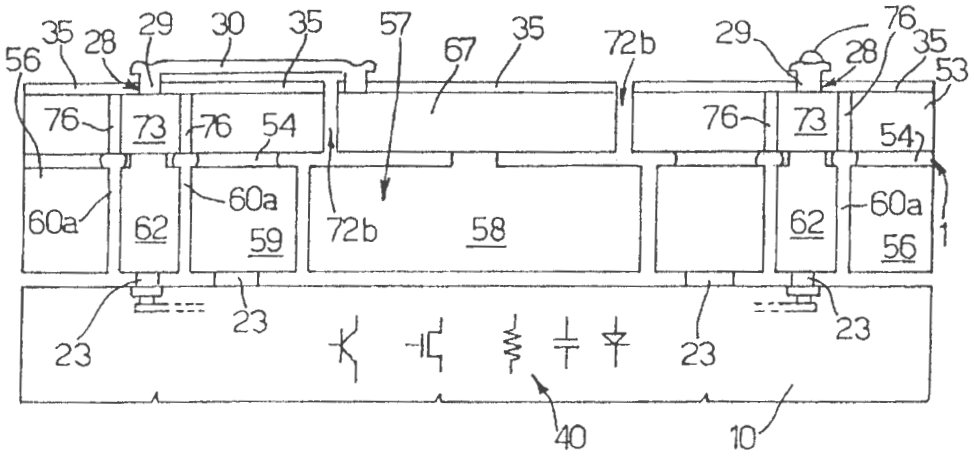
* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—Andy Huynh
(74) *Attorney, Agent, or Firm*—Lisa K. Jorgenson; Robert Iannucci; Seed IP Law Group PLLC

(57) **ABSTRACT**

An electric connection structure connecting a first silicon body to conductive regions provided on the surface of a second silicon body arranged on the first body. The electric connection structure includes at least one plug region of silicon, which extends through the second body; at least one insulation region laterally surrounding the plug region; and at least one conductive electromechanical connection region arranged between the first body and the second body, and in electrical contact with the plug region and with conductive regions of the first body. To form the plug region, trenches are dug in a first wafer and are filled, at least partially, with insulating material. The plug region is fixed to a metal region provided on a second wafer, by performing a low-temperature heat treatment which causes a chemical reaction between the metal and the silicon. The first wafer is thinned until the trenches and electrical connections are formed on the free face of the first wafer.

26 Claims, 6 Drawing Sheets



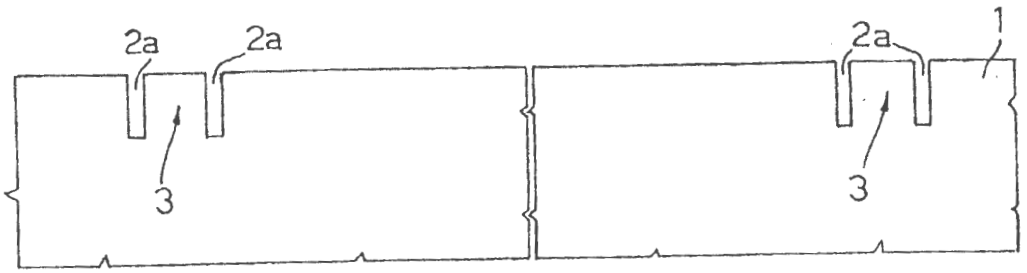


Fig.1

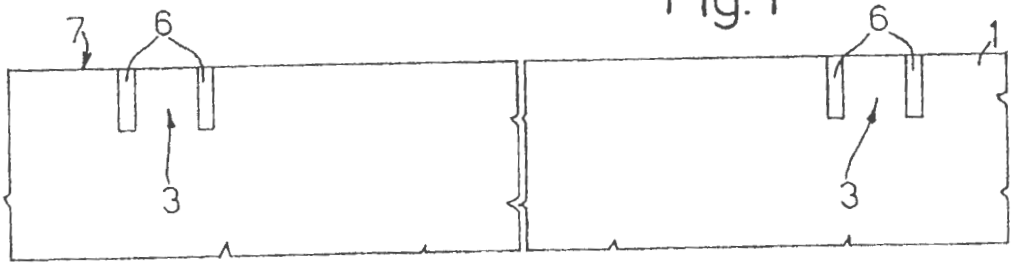


Fig.2

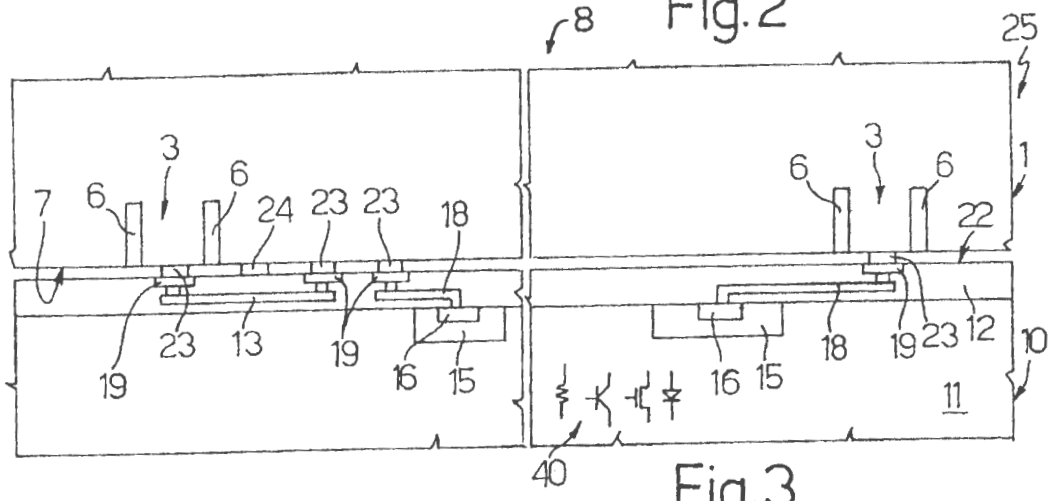


Fig.3

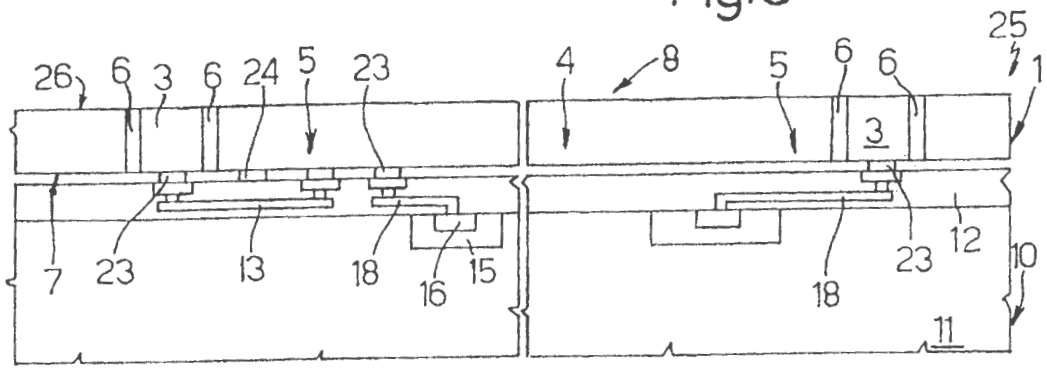


Fig.4

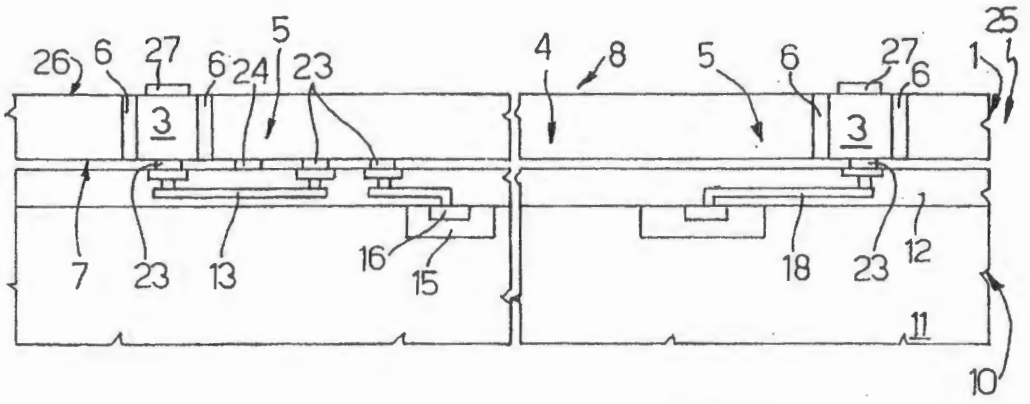


Fig.5

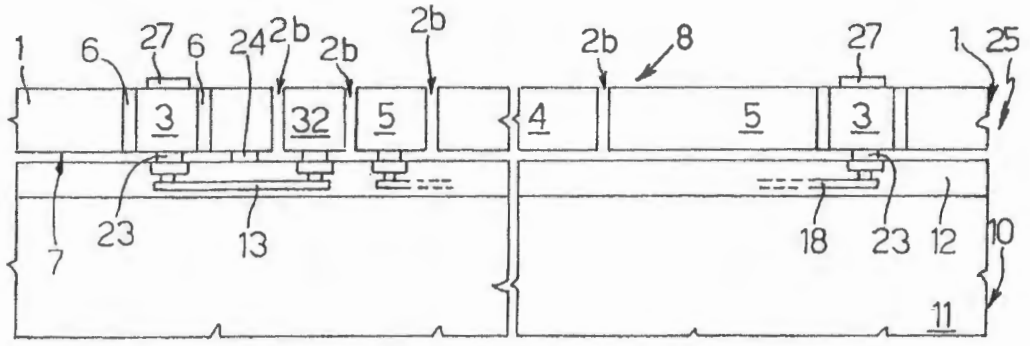


Fig.6

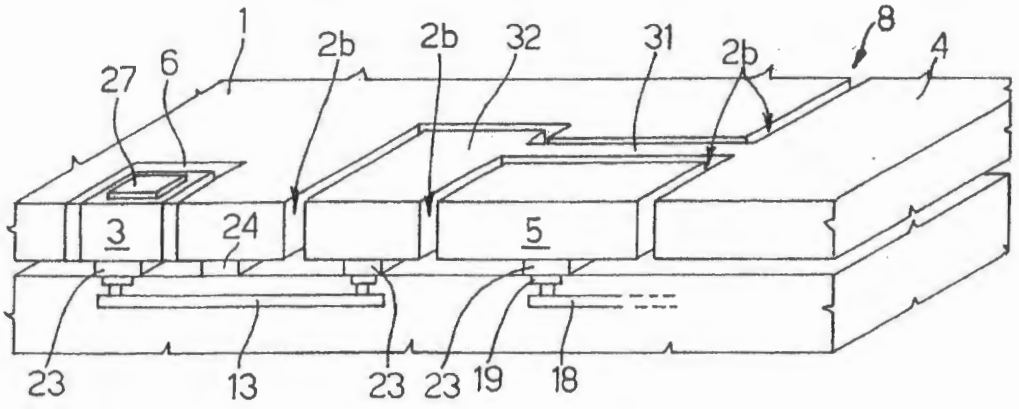


Fig.7

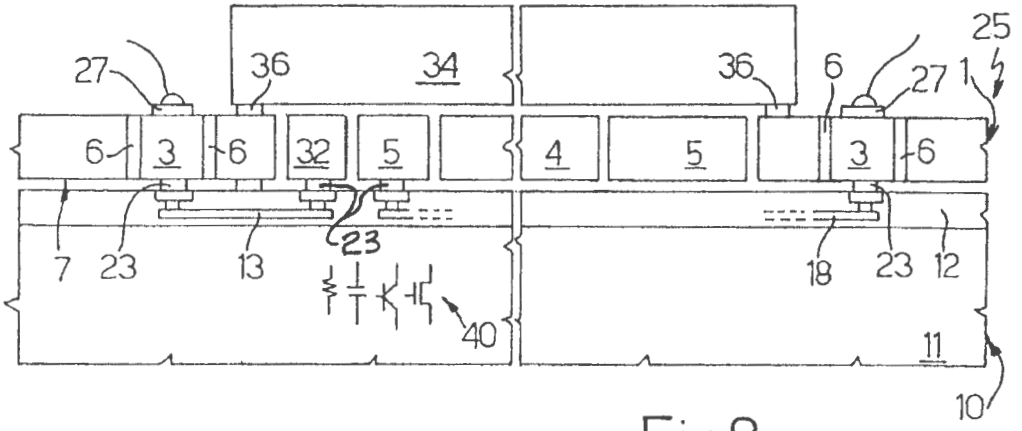


Fig.8

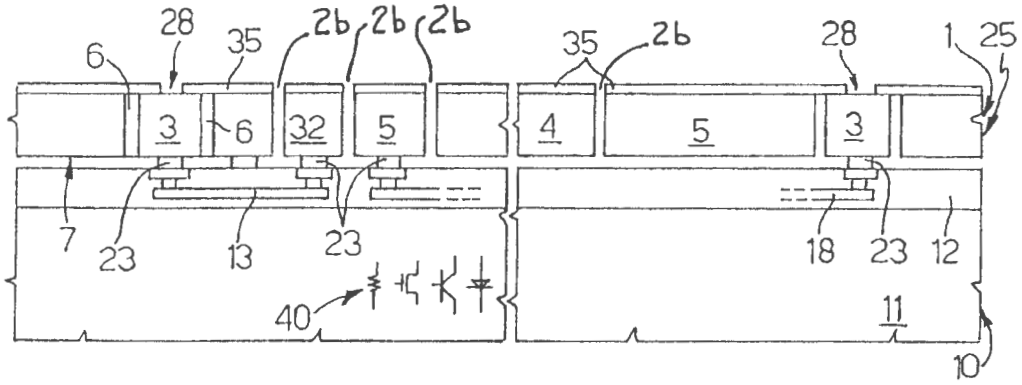


Fig.9

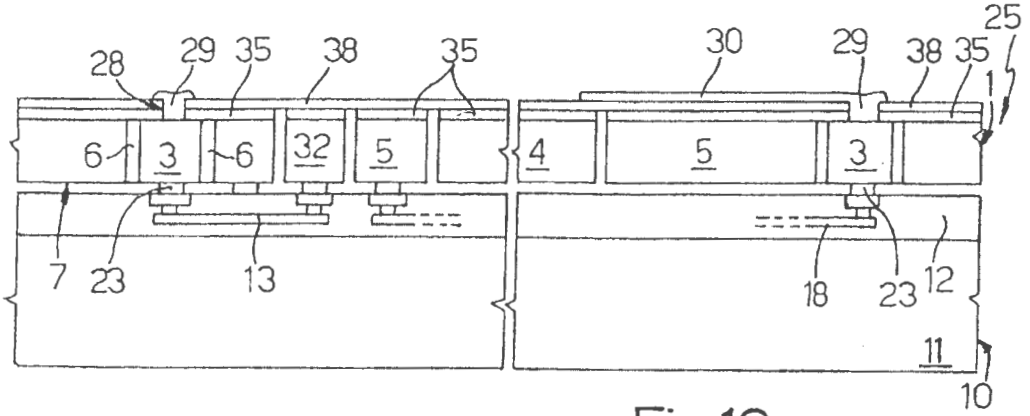


Fig.10

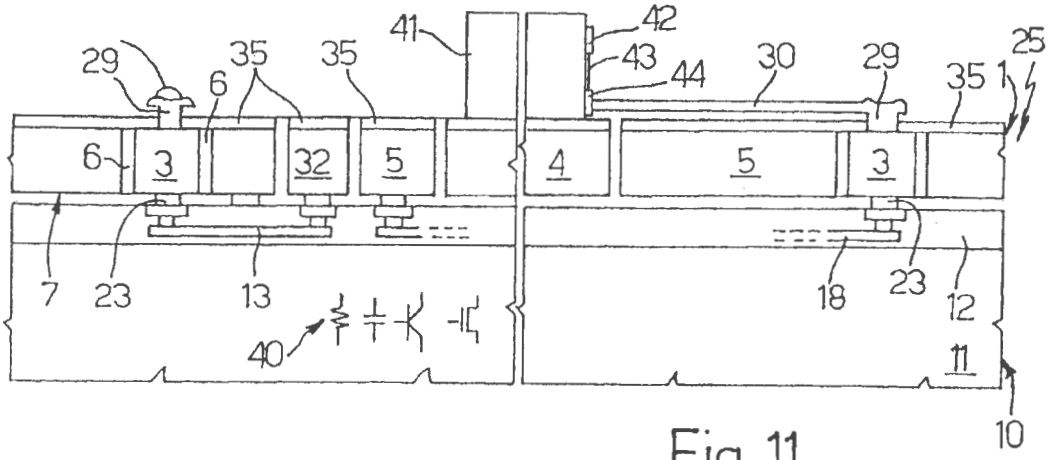


Fig. 11

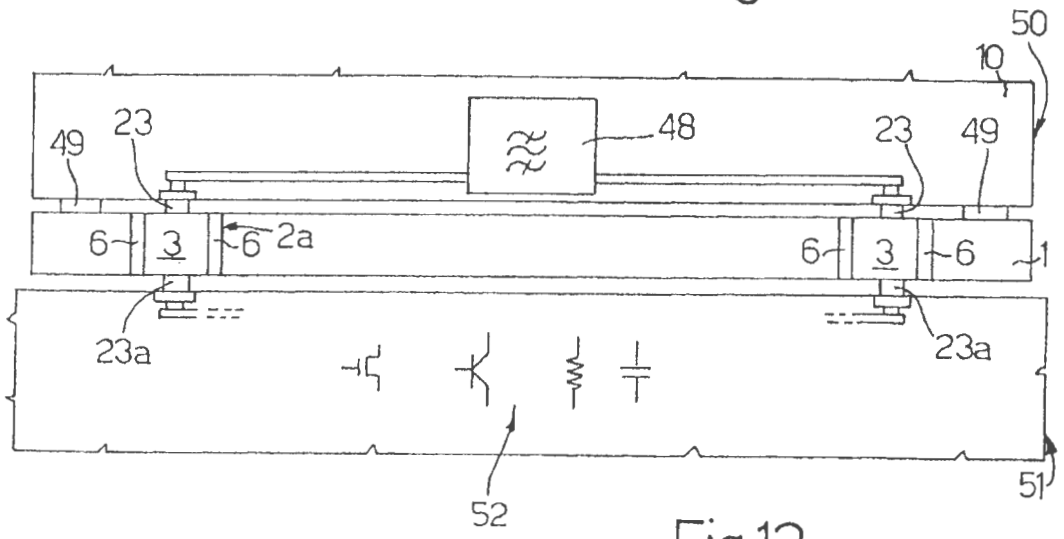


Fig.12

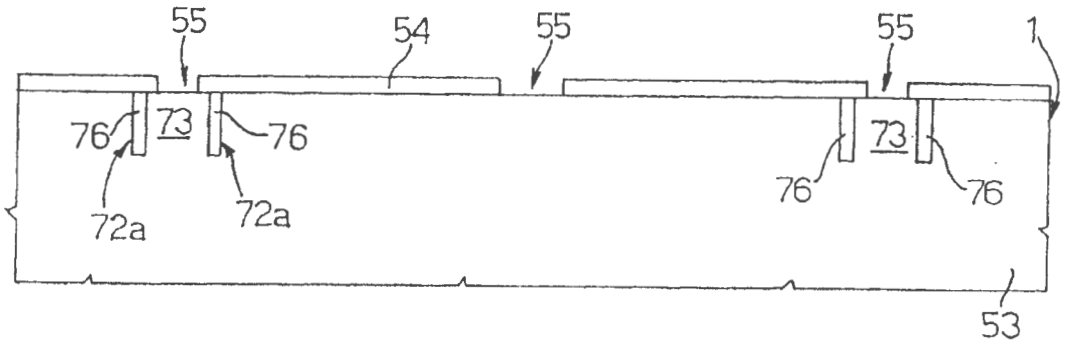


Fig.13

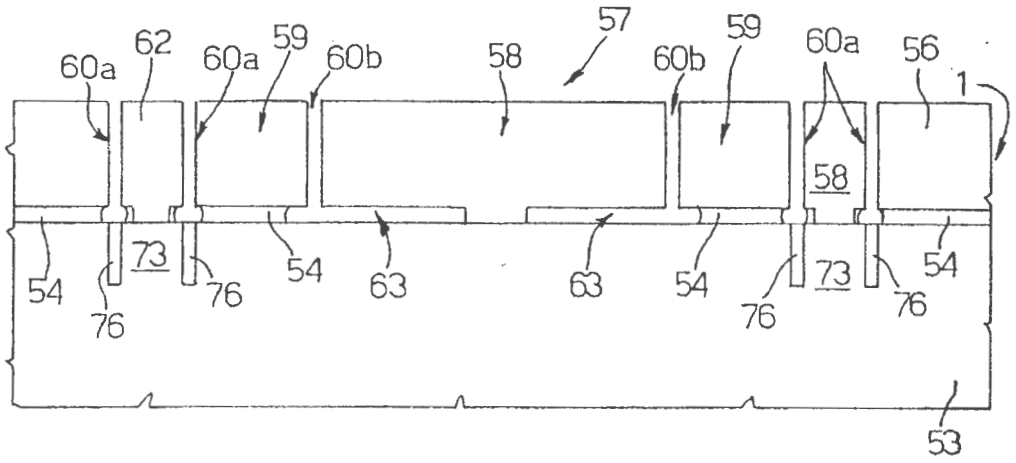


Fig. 14

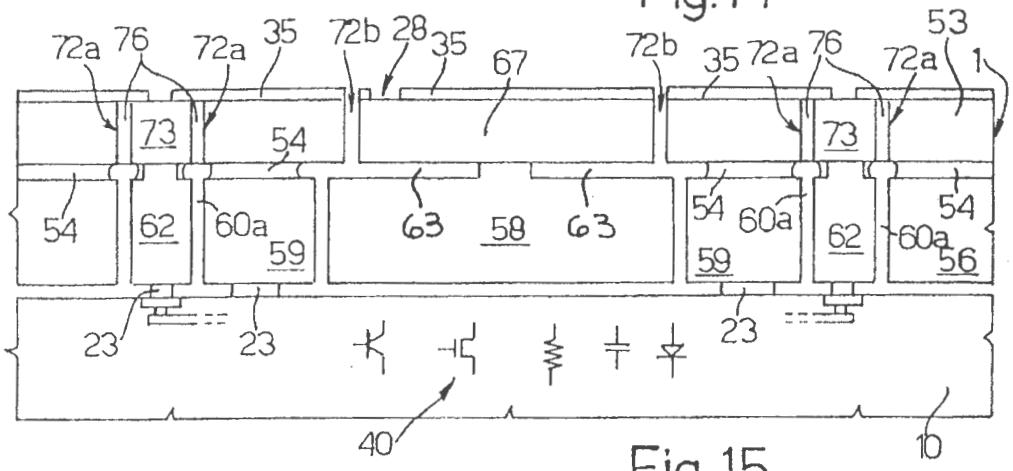


Fig. 15

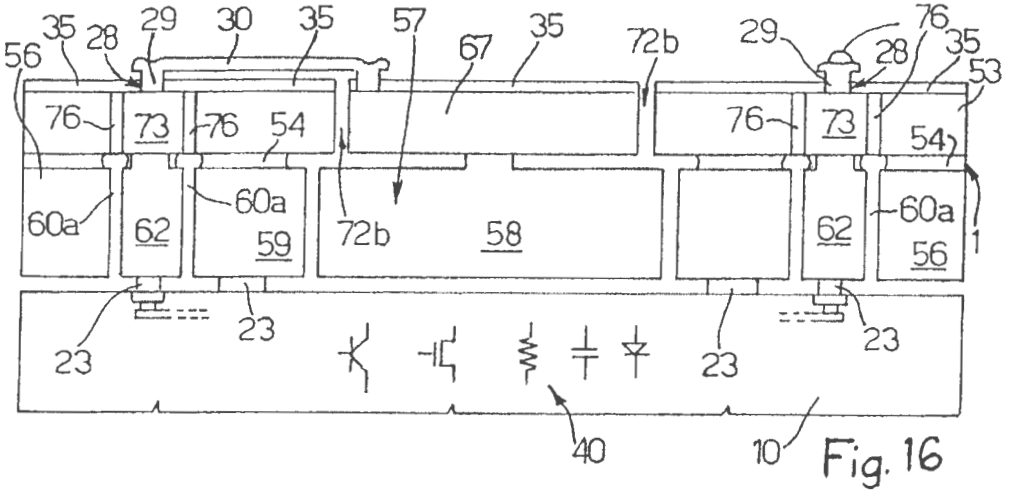


Fig. 16

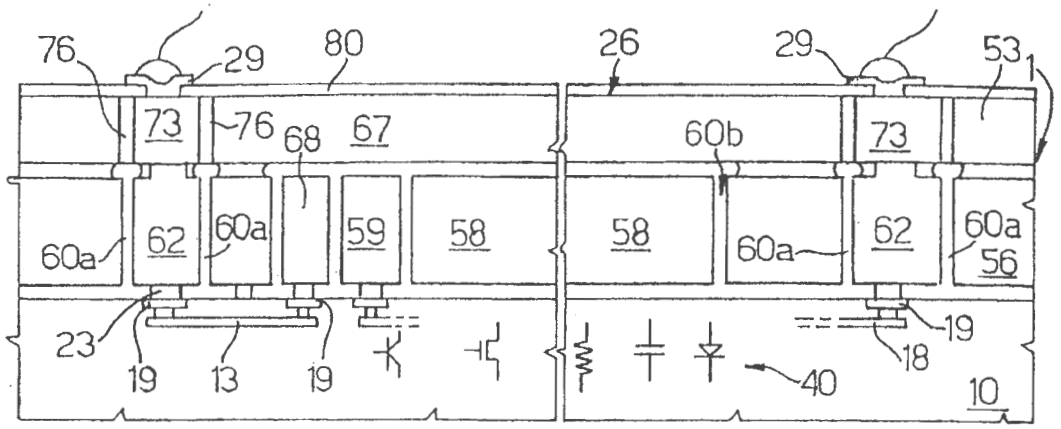


Fig. 17

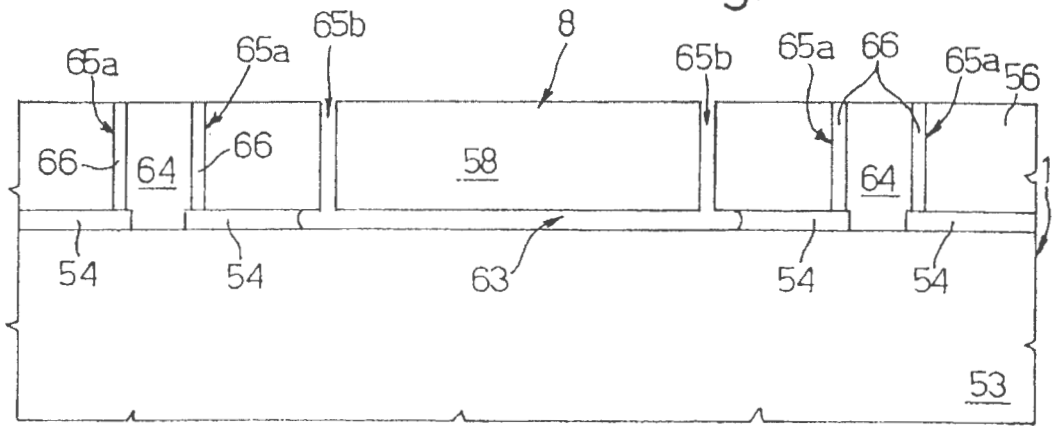


Fig. 18

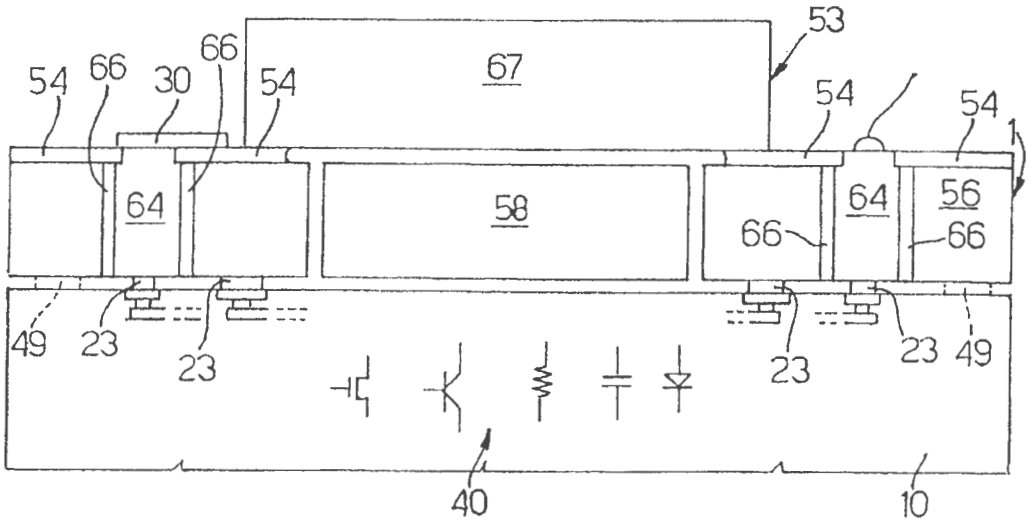


Fig. 19

STRUCTURE FOR ELECTRICALLY CONNECTING A FIRST BODY OF SEMICONDUCTOR MATERIAL OVERLAID BY A SECOND BODY OF SEMICONDUCTOR MATERIAL COMPOSITE STRUCTURE USING ELECTRIC CONNECTION STRUCTURE

TECHNICAL FIELD

The present invention regards a structure for electrically connecting a first body of semiconductor material overlaid by a second body of semiconductor material, a composite structure using the electric connection structure and a manufacturing process.

BACKGROUND OF THE INVENTION

In particular, the invention can be used for electrically connecting a first silicon wafer incorporating electronic components to a second silicon wafer incorporating a micromechanical structure and/or to the outside. The invention can likewise be used for electrically connecting the first wafer to a third body carried by the second wafer, as well as for connecting the first wafer to the outside when the first wafer is covered by a protection structure, and thus is not directly accessible. An example of a particular application is represented by a micro-electromechanical system including a first wafer incorporating a circuit for controlling the parameters defining the state of a micro-electromechanical structure (for example, the position of a microactuator); a second wafer incorporating the micro-electromechanical structure; and a third wafer forming a cap for protecting the micro-electromechanical structure.

Various techniques are known for mechanically connecting two semiconductor material bodies (see, for example, Martin A. Schmidt, "Wafer-to-Wafer Bonding for Microstructure Formation", Proceedings of the IEEE, Vol. 86, No. 8, August 1998). However, such techniques do not enable two or three wafers to be electrically connected, in addition to be mechanically connected, or covered components of one of the wafers to be electrically accessed.

SUMMARY OF THE INVENTION

An embodiment of the present invention provides a connection structure that enables semiconductor material bodies made on different substrates to be overlaid and to be connected mechanically and electrically together and to the outside.

According to embodiments of the present invention, an electric connection structure, a composite structure, and a process for manufacturing a composite structure are provided. The electric connection structure connects a first silicon body to conductive regions provided on the surface of a second silicon body arranged on the first body. The electric connection structure includes at least one plug region of silicon, which extends through the second body; at least one insulation region laterally surrounding the plug region; and at least one conductive electromechanical connection region arranged between the first body and the second body, and in electrical contact with the plug region and with conductive regions of the first body. To form the plug region, trenches are dug in a first wafer and are filled, at least partially, with insulating material. The plug region is fixed to a metal region provided on a second wafer, by performing a low-temperature heat treatment which causes a chemical reaction between the metal and the silicon. The first wafer is thinned until the trenches and electrical connections are formed on the free face of the first wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, preferred embodiments thereof are now described, merely to provide non-limiting examples, with reference to the attached drawings, wherein:

FIGS. **1** and **2** are cross-sections through a semiconductor material wafer, in two successive manufacture steps, according to a first embodiment of the invention;

FIG. **3** shows a cross-section through the wafer of FIG. **2**, after bonding to a second semiconductor material wafer;

FIGS. **4–6** show cross-sections of the multiwafer structure of FIG. **3**, in successive manufacture steps;

FIG. **7** is a perspective view of the left-hand half of the multiwafer structure of FIG. **6**;

FIG. **8** shows a cross-section of the multiwafer structure of FIG. **6**, in a final manufacture step;

FIGS. **9–11** show cross-sections of a micro-electromechanical system according to a second embodiment of the invention;

FIG. **12** shows a cross-section of a composite structure formed starting from three semiconductor material substrates, according to a third embodiment of the invention;

FIGS. **13** and **14** show cross-sections of a semiconductor material wafer, in two successive manufacture steps according to a fourth embodiment of the invention;

FIG. **15** shows a cross-section of the wafer of FIG. **14** after bonding to a second semiconductor material wafer;

FIG. **16** shows a cross-section of a composite structure obtained from the double wafer of FIG. **15**, in a subsequent manufacture step;

FIG. **17** shows a cross-section of a composite wafer, according to a fifth embodiment of the invention; and

FIGS. **18** and **19** show cross-sections of a composite wafer, according to a sixth embodiment of the invention, in two successive manufacture steps.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. **1–8** show a first embodiment of a process for manufacturing a micro-electromechanical system, including a control and sensing circuitry and a micro-electromechanical sensor, for example an acceleration sensor.

Initially, as illustrated in FIG. **1**, a first wafer **1** of semiconductor material, typically P^{++} or N^{++} doped monocrystalline silicon, illustrated as sectioned along two parallel half-planes so as to show different areas in the left-hand half and in the right-hand half, is masked and etched to form first deep trenches **2***a*. For example, the first wafer **1** may have a conductivity of between 5 and 15 mΩ/cm, preferably 10 mΩ/cm. As shown in FIG. **2**, the first trenches **2***a* have a closed shape and enclose monocrystalline silicon plug regions **3** intended to form through connections, as explained more clearly hereinafter.

Subsequently, the first trenches **2***a* are filled, either completely or partially, with insulating material **6**, for example silicon dioxide. To this end, a silicon dioxide layer is deposited or grown, and is subsequently removed from a first surface **7** of the first wafer **1**, to obtain the structure shown in FIG. **2**.

Next, as illustrated in FIG. **3**, the first wafer **1** is bonded to a second wafer **10** formed of a monocrystalline silicon substrate **11** and an insulation and/or passivation layer **12**. In particular, the substrate **11** houses conductive and/or insulating regions forming electronic components for biasing the acceleration sensor **8** and for detecting and processing electrical signals generated by the acceleration sensor **8**. As an example, FIG. **3** shows conductive regions **15–16** of the N/P-type belonging to an electronic circuit **40**, which is shown only schematically. In addition, the insulation and/or passivation layer **12** houses metal regions **13**, **18**, which terminate, at one or both of their ends, with pad regions **19** facing the surface **22** of the second wafer **10**.

Connection regions **23** are provided on the surface **22** of the second wafer **10**, on top of the pad regions **19**, and are of a metal that is able to react at a low temperature with the silicon of the first wafer **1** to form a gold/silicon eutectic or a metallic silicide. Typically, the connection regions **23** are made of gold, in the case where the aim is to obtain a eutectic, or of a metal chosen from among the group comprising palladium, titanium, and nickel, in the case where the aim is to obtain a silicide. Bonding regions **24** are also provided on the surface **22** and are preferably formed at the same time as the connection regions **23**.

For bonding the first wafer **1** to the second wafer **10**, the first wafer **1** is turned upside down so that the first surface **7** of the first wafer **1** faces the second wafer **10**. The plug regions **3** of the first wafer **1** are brought into contact with the connection regions **23** of the second wafer **10**, and subsequently a heat treatment at low temperature, for example 350–450° C., is carried out for a period of 30–45 minutes, so that the metal of the connection regions **23** of the second wafer **10** react with the silicon of the plug regions **3** and form a metallic silicide which bonds the first and the second wafers **1**, **10**. Thereby, a double wafer **25** is obtained, as shown in FIG. **3**.

Subsequently, as illustrated in FIG. **4**, the first wafer **1** is thinned from the back mechanically, for example by grinding, preferably so as to obtain a thickness of 30–40 μm. The first wafer **1** then has a second surface **26** opposite to the first surface **7**.

Next, as illustrated in FIG. **5**, a metal layer, for example, an aluminum layer, is deposited and defined, so as to form metal regions **27** extending above the plug regions **3** and in direct electrical contact with the latter.

Subsequently, the first wafer **1** is masked and etched so as to form second trenches **2***b* defining an acceleration sensor **8**. In particular, as may be seen in FIGS. **6** and **7**, the second trenches **2***b* separate a mobile region, forming a rotor **4**, and a fixed region, forming a stator **5**, from the rest of the wafer **1** and from one another. The rotor **4** is connected, through elastic-connection regions, also referred to as springs **31**, to fixed biasing regions **32**, which are set in areas corresponding to respective connection regions **23**, connected, through the metallic regions **13**, to the plug regions **3**.

Next, as illustrated in FIG. **8**, a cap element **34** is fixed to the wafer **1** through adhesive regions **36**, in a per se known manner, and then the double wafer **25** is cut into individual dice. Finally, the metal region **27** is contacted applying the usual wire-bonding technique.

Thereby, the connection regions **23** ensure mechanical connection between the monocrystalline silicon wafers **1** and **10** and electrical connection between the surface **22** of the second wafer **10** and the plug regions **3**. In turn, the plug regions **3** allow the second wafer **10** to be contacted from above. In particular, some plug regions **3** enable the second wafer **10**, not directly accessible from the front, to be connected to the outside, without requiring costly processes to be carried out from the back. In addition, as is shown in the left-hand half of FIG. **8**, this solution also enables connection of regions formed in the first wafer **1** to the outside. Here the rotor **4** is connected to the outside through a first connection region **23** (beneath the biasing region **32**), a metal region **13**, a second connection region **23** (beneath the plug region **3**), and the plug region **3**. The plug regions **3** are insulated by insulation regions formed by the insulating material **6** and possibly by the air present in the first deep trenches **2***a*, and are thus electrically insulated from the rest of the first wafer **1**, except, obviously, for the regions connected to them via electric connection lines **30**, shown in FIG. **10**.

With the solution of FIGS. **1–8** a pressure sensor, instead of an acceleration sensor, may be formed.

FIGS. **9–11** show a second embodiment of the invention regarding a unit for micrometric regulation of the read/write head of a hard-disk driver. In detail, initially the same steps are carried out as described previously with reference to FIGS. **1–4**. After thinning the first wafer **1**, an oxide layer **35** is deposited and removed selectively at the plug regions **3** to form openings **28**. The second trenches **2***b* are then formed through the oxide layer **35** and through the wafer **1**.

Subsequently, as illustrated in FIG. **10**, an insulating layer **38** is deposited, for example a stick foil which does not enter the second trenches **2***b*. The insulating layer is removed from above the openings **28**, and metal connection regions are formed by depositing and defining a metal layer. In particular, in the illustrated example the metal layer fills the openings **28**, where it forms contacts **29**. In addition, an electric connection line **30** is formed and extends from the contact **29** arranged above the plug region **3** furthest to the right, up to above the rotor **4**.

Subsequently, the composite wafer **25** is cut into dice, the insulating layer **38** is removed in oxygen plasma, and a ceramic body, referred to as slider **41**, is bonded to the rotor **4** in a per se known manner (FIG. **11**). The slider **41** carries a transducer **42** for data reading/writing on a hard disk (not shown). The transducer **42** is electrically contacted through connection regions **43**, one of which may be seen in FIG. **11**, which are formed directly on one side of the slider **41**. Each connection region **43** extends from the transducer **42** as far as a pad **44** in electrical contact with an electric connection line **30**.

Thereby, the plug region **3** furthest to the right enables electrical connection between the transducer **42** on the slider **41** and the electrical circuit **40**, which can thus transmit to the transducer **42** the data to be written, or process the signal picked up by the transducer **42**. In addition, in a known manner, the electrical circuit **40** controls movement of the rotor **4**, and consequently of the slider **41**. Finally, a connection via an intermediate plug region (not shown) enables connection of the electrical circuit **40** to the outside, in a way similar to that illustrated in the right-hand part of FIG. **8**.

Consequently, also in this case the plug regions **3** enable connection of non-accessible regions of the second wafer **10** to elements arranged above them (here, the transducer **42**), as well as to the outside.

FIG. **12** shows a third embodiment regarding the manufacture of circuits or structures to be kept in vacuum conditions. In the illustrated example, the wafer **1**, after forming the plug regions **3** by digging the first trenches **2***a* and filling them with insulating material **6**, has been bonded to a second wafer **10**, wherein a filter **48** has been previously

made, for example of the band-pass type for high frequencies. The first wafer **1** is bonded to the second wafer **10**, not only through the connection regions **23**, but also through a sealing region **49** which extends between the first wafer **1** and the second wafer **10**, and completely surrounds the area in which the filter **48** is formed, as well as the plug regions **3**. The sealing region **49** is, for example, made using a low-melting temperature glass and has a closed shape. If bonding of the first wafer **1** and second wafer **10** is carried out in a low-pressure environment, the filter **48** remains vacuum encapsulated.

Next, the first wafer **1** is thinned as described above, and the double wafer **1**, **10** is cut into dice **50**. The dice **50** are then bonded to a third wafer **51** which houses a circuit **52** and which has previously been provided with connection regions **23***a* similar to the connection regions **23**. The thinned side of the first wafer **1** faces the third wafer **51**, and the plug regions **3** must be aligned to the connection regions **23***a*.

In this case, the first wafer **1**, in addition to protecting and isolating the filter **48** from the outside environment and maintaining it in vacuum conditions, enables its electrical connection with the circuit **52** incorporated in the third wafer **51**. In addition, it is possible to carry out electrical testing of the circuit **52** connected to the filter **48** at the wafer level (EWS-Electric Wafer Sort test).

FIGS. **13–16** show a fourth embodiment of the invention. According to FIG. **13**, initially the first wafer **1** comprises a substrate **53** accommodating first trenches **72***a*, and the first trenches **72***a* are filled with insulating material **76** to insulate first plug portions **73**, in a way similar to that described with reference to FIG. **1** for the plug regions **3**. Then a sacrificial layer **54**, for example of silicon dioxide, is deposited or grown, then is masked and etched so as to form openings **55** on top of the first plug portions **73** and in areas where anchorages with the structure on top are to be made, as described hereinafter.

Subsequently (FIG. **14**), a polycrystalline silicon seed layer is deposited on top of the sacrificial layer **54** and in the openings **55**, and then a polycrystalline silicon epitaxial layer **56** is grown. In this way, the epitaxial layer **56** is in direct contact with the substrate **53** at the openings **55**. Next, inside the epitaxial layer **56** third and fourth trenches **60***a*, **60***b* are dug, which reach as far as the sacrificial layer **54**. In particular, the third trenches **60***a* delimit second plug portions **62** aligned vertically with the first plug portions **73** in the substrate **53**, and the third trenches **60***a* define a desired micromechanical structure (in the example illustrated, a microactuator **57** of the rotating type, including a rotor **58** and a stator **59**, with the rotor **58** supported by springs, which are not illustrated).

Subsequently, in a known way, a part of the sacrificial layer **54** is removed through the fourth trenches **60***b*. In particular, the sacrificial layer **54** is removed beneath the rotor **58** to form an air gap **63**, and it substantially remains underneath the stator **59**. The sacrificial layer **54** is removed only to a very small extent through the third trenches **60***a*, given the different geometry (the micromechanical structure is formed by thin regions and/or perforated regions, allowing the sacrificial layer **54** to be substantially removed; this, instead, is not done through the third trenches **60***a*).

In a way not shown, it is then possible to fill the third trenches, at least partially, with insulating material, in a way similar to that described for the first trenches **2***a* of FIG. **1**.

Subsequently, as illustrated in FIG. **15**, the first wafer **1** is turned upside down and bonded to the second wafer **10**, inside which components of the circuit **40** have already been formed, and on top of which the connection regions **23** have already been made. Also in this case, a low-temperature heat treatment is carried out to enable a chemical reaction between the silicon of the epitaxial layer **56**, at the second plug portions **62**, and the metal of the connection regions **23**. Next, the substrate **53** of the first wafer **1** is thinned until the insulating material **76**, or at least the bottom of the first trenches **72***a*, is reached, an oxide layer **35** is deposited, the openings **28** are formed in the oxide layer **35**, and then second trenches **72***b* are made which separate fixed parts from mobile parts in the substrate **53**.

Next, as has been described with reference to FIG. **10**, an insulating layer, for example stick foil, is deposited and selectively removed, and the electrical contacts **29** and electric connection lines **30** are formed. In FIG. **16**, an electric connection line **30** connects the portion of the substrate **53** to which the rotor **58** is anchored, for example at cap region **67**, to the first plug region **73** that is furthest to the left, thus enabling electrical connection of the rotor **58** to the circuit **40** through the cap region **67**, the first plug portion **73** on the left, and the second plug portion **62** on the left. Shown in the right-hand half of FIG. **16** is instead the electrical connection between the circuit **40** and the outside, through the second plug portion **62**, the first plug region **73**, and the connection region **23** on the right.

Subsequently, the insulating layer is removed, and a body to be moved, for example a slider similar to the slider **41** of FIG. **11**, can be fixed to the cap region **67**.

The solution shown in FIGS. **13–16** thus provides a micromechanical structure **57** protected by a cap, for example cap region **67**, and easily connects the circuit **40** both to the micromechanical structure **57** and to the outside.

FIG. **17** shows a variation of the structure of FIG. **16**, in which the rotor **58** is not anchored to the substrate **53**, but is supported by springs (not shown) and biasing regions **60**, similar to the biasing regions **31**, **32** of FIG. **7**. In addition, the cap region **67** is fixed and does not have the second trenches **72***b*. The rotor **58** and stator **59** are connected via connection regions **23** and pad regions **19** to metallic regions **13**, **18** formed in the second wafer **10**. The metallic regions **13** are connected to the outside, as shown in the left-hand half of FIG. **17**, via further connection regions **23** aligned with plug regions **62**, **73** formed in the first wafer **1**, in a way similar to that described with reference to FIGS. **13–16**, and via contacts **29**. In addition, the metallic regions **18** enable connection of the circuit **40** to the stator **59** and, via plug regions **62**, **73** and contacts **29**, to the outside, as shown in the right-hand half of FIG. **17**. An insulating layer **80** covers the surface **26** of the first wafer **1**.

FIGS. **18** and **19** show a sixth embodiment, in which a micromechanical structure, for example an acceleration sensor **8**, is protected by a cap and electrically connected to the biasing and sensing circuit via plug regions.

Initially, as illustrated in FIG. **18**, the first wafer comprises a substrate **53**, which, in contrast to the previous embodiments, is not etched to form trenches. On the substrate **53**, a sacrificial layer **54** is deposited and defined, and is removed only at openings **55**. Next, a polycrystalline silicon seed layer is deposited, and the epitaxial layer **56** is grown, as described with reference to FIG. **14**.

The epitaxial layer **56** is etched to form fifth trenches **65***a* for delimiting second plug portions **64**. Here, the fifth trenches **65***a* are filled, either partially or completely, with insulating material **66**, sixth trenches **65***b* are formed for defining the accelerometric sensor **8**, and the sacrificial layer

54 is partially removed through the sixth trenches 65*b*, so as to free the rotor 58 of the acceleration sensor 8. As for the embodiment shown in FIGS. 1–8, the rotor 58 is carried by the fixed part via springs (not illustrated).

Subsequently, the first wafer 1 is bonded to the second wafer 10 using the connection regions 23 already formed on the surface 22 of the second wafer 10. Then the first wafer 1 is thinned by grinding until the desired thickness for the substrate 53. Next, the substrate 53 is selectively removed so as to form a cap region 67 of larger dimensions than the rotor 58, but of smaller dimensions than the chip housing the circuit 40, obtained after cutting the wafers 1, 10. In this way, the cap region 67 covers the rotor 58 from the back, protecting it mechanically, but leaves the plug regions 64 free.

Finally, the contacts 29 and the electric connection lines 30 are formed, which, in this embodiment, contact directly the silicon of the epitaxial layer 54. In particular, in the example illustrated in FIG. 19, an electric connection line 30 connects a region (not shown), arranged inside the fixed part and is electrically connected to the rotor 58, to the plug region 64 on the left, and thus to the circuit 40. A ball-and-wire connection on the right instead enables connection of the circuit 40 to the outside.

When the acceleration sensor 8 is to be kept at low pressure, for example to reduce friction with air during movement, a sealing region 49 may be provided which surrounds the area of the acceleration sensor 8, then the first wafer 1 may be bonded to the second wafer 10 in vacuum conditions, as already described with reference to FIG. 12.

The advantages of the process and structures described are evident from the above. In particular, they enable mechanical connection of two bodies of semiconductor material, in particular of monocrystalline silicon, arranged on one another, and at the same time the electrical connection of a structure or circuit formed in the underlying body, which is covered by the overlying body, to the outside or to a structure made in the overlying body; or else, they enable electrical connection of the underlying body to regions arranged above the overlying body, without requiring complicated and costly processes to be carried out from the back, without damaging the structures and circuits already made, and applying single manufacture steps that are commonly used in the manufacture of wafers of semiconductor material for forming micro-electromechanical structures.

The described solutions moreover make it possible, when necessary, to isolate preset areas of the underlying body and/or of the overlying body from the outside environment, for example to enclose delicate elements in a low-pressure environment, and/or to isolate and prevent contamination of these elements during manufacture, for example cutting semiconductor material wafers, during subsequent manipulation steps, and during use.

Finally, it is clear that numerous modifications and variations may be made to the connection structure, the composite structure, and to the manufacture process described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims. In particular, the present connection structure may be used for a wide range of applications, both for the connection of electronic circuits integrated in two or more different substrates, and for the connection of micro-electromechanical structures of various kinds to biasing/control/sensing circuits associated to the micro-electromechanical structures. The present connection structure may be used for connecting a high number of substrates, according to the requirements and to general considerations of a mechanical/electrical nature.

What is claimed is:

1. An electric connecting structure for connecting a first body of semiconductor material overlaid by a second body of semiconductor material, the connecting structure comprising:

a plug region extending through a portion of said second body and made of monocrystalline semiconductor material;

an insulation region surrounding laterally said plug region; and

a first electromechanical connection region of electrically conductive material arranged between said first body and said second body and in electrical contact with said plug region and with conductive regions of said first body.

2. The electric connection structure of claim 1, wherein said plug region extends throughout a thickness of said second body and has a first face and a second face, said first face being in contact with said first electromechanical connection region; and

further comprising a contact region of electrically conducting material in contact with said second face of said plug region.

3. The electric connection structure of claim 2, further comprising an electric connection line extending above said second body and having a first end forming said contact region.

4. The electric connection structure of claim 3, wherein said electric connection line has a second end in electrical contact with a conductive region of said second body.

5. The electric connection structure of claim 3, wherein said electric connection line has a second end in electrical contact with a contact region formed on a third body fixed to said second body.

6. The electric connection structure of claim 2, for electrically connecting said second body to a third body of semiconductor material arranged on said second body, wherein said contact region further comprises at least one second electromechanical connection region made of a material resulting from the chemical reaction of said semiconductor material with a metal, said second electromechanical connection regions being arranged between said second body and said third body.

7. The electric connection structure according to claim 1, wherein said insulation region comprises a trench having a closed shape filled at least partially with insulating material.

8. The electric connection structure according to claim 1, wherein said first electromechanical connection region is made of a material resulting from the chemical reaction of said semiconductor material with a metal.

9. The electric connection structure according to claim 1, wherein said first electromechanical connection region is made of a metal resulting from the chemical reaction of silicon with a metal chosen from among a group comprising gold, palladium, titanium, and nickel.

10. The electric connection structure of claim 1 wherein said plug region and said second body are made of the same material.

11. An electric connecting structure for connecting a first body of semiconductor material overlaid by a second body of semiconductor material comprising a substrate region and an epitaxial region arranged on each other and partially insulated from one another by insulating regions, the connecting structure comprising:

a plug region extending through a portion of said second body and made of semiconductor material;

an insulation region surrounding laterally said plug region; and

a first electromechanical connection region of electrically conductive material arranged between said first body and said second body and in electrical contact with said plug region and with conductive regions of said first body, wherein:

said plug region further comprises a first plug portion extending throughout the thickness of said substrate region, and a second plug portion formed inside said epitaxial region, said second plug portion being aligned and in direct electrical contact with said first plug portion;

said insulation region further comprises a first insulation portion laterally surrounding said first plug portion, and a second insulation portion laterally surrounding said second plug portion;

a contact region of electrically conducting material extends on a free face of said substrate region in electrical contact with said first plug portion; and

said second plug portion faces and is in direct electrical contact with said first electromechanical connection region.

12. The electric connection structure of claim **11** wherein said plug region and said second body are formed from a common material.

13. The electric connection structure of claim **11** wherein said plug region is made of monocrystalline semiconductor material.

14. An electric connecting structure for connecting a first body of semiconductor material overlaid by a second body of semiconductor material comprising a substrate region and an epitaxial region arranged on one another and reciprocally insulated by insulating regions, the connection structure comprising:

a plug region extending through a portion of said second body and made of semiconductor material;

an insulation region surrounding laterally said plug region; and

a first electromechanical connection region of electrically conductive material arranged between said first body and said second body and in electrical contact with said plug region and with conductive regions of said first body, wherein said substrate region has a smaller area than said epitaxial region, said plug region extends throughout the thickness of said epitaxial region, and has a first face and a second face, said first face being in contact with said first electromechanical connection region, and said second face being in direct contact with at least one electric connection region of electrically conducting material.

15. The electric connection structure of claim **14** wherein said plug region and said second body are both formed from a common material.

16. The electric connection structure of claim **14** wherein said plug region is made of monocrystalline semiconductor material.

17. A composite structure comprising:

a first body of semiconductor material;

a second body of semiconductor material arranged on said first body); and

an electric connection structure, including:

a plug region extending through a portion of said second body and made of monocrystalline semiconductor material,

an insulation region laterally surrounding said plug region, and

a first electromechanical connection region of electrically conductive material arranged between said first body and said second body and in electrical contact with said plug region and with conductive regions of said first body.

18. The composite structure according to claim **17**,

wherein said plug region extends throughout the thickness of said second body and has a first face and a second face, said first face being in contact with said first electromechanical connection region;

further comprising a contact region of electrically conducting material, in contact with said second face of said plug region; and

wherein said first body houses an electronic circuit); and

said second body houses a micro-electromechanical device comprising a fixed part and a mobile part separated from each other by at least one delimitation trench extending through said second body.

19. The composite structure of claim **18**, further comprising an external electric connection wire bonded to said contact region.

20. The composite structure of claim **18**, wherein said electric connection structure further comprises an electric connection line extending above said second body and having a first end forming said contact region, and a second end in electrical contact with said micro-electromechanical device.

21. The composite structure of claim **18**, further comprising a third body fixed to said second body, said electric connection structure further comprising an electric connection line having a first end forming said contact region and a second end in electrical contact with a contact region formed on said third body.

22. The composite structure of claim **21**, wherein said third body is a slider, and said composite structure forms an actuator unit for micrometric position regulation of a hard-disk driver.

23. The composite structure of claim **17**, wherein the first body of semiconductor material further houses a first electronic circuit;

further comprising a third body of semiconductor material and housing a second electronic circuit, said third body fixed to said second body; and

the electric connection structure, wherein:

said plug region includes a first face and a second face, said plug region connecting together said first and second electronic circuits,

said first electromechanical connection region arranged between said first body and said second body is further in electrical contact with said first face of said plug region, and

further comprising a contact region of electrically conducting material in contact with said second face of said plug region, the contact region having at least one second electromechanical connection region made of a material resulting from the chemical reaction of said semiconductor material with a metal, said second electromechanical connection regions being arranged between said second body and said third body.

24. The composite structure of claim **23**, further comprising a sealing region having a closed shape and arranged between said first and said second bodies, outside one of said first and second electronic circuits.

25. A composite structure comprising:

a first body of semiconductor material;

a second body of semiconductor material arranged on said first body and comprising a an epitaxial region housing a micro-electromechanical device having a fixed part and a mobile part separated from one another by a delimitation trench extending through said epitaxial region and a substrate region forming a cap region and arranged over the mobile part of said epitaxial region, said epitaxial region and said substrate region being arranged on each other and partially insulated from one another by first and second insulating regions; and

an electric connection structure, including:

a first plug portion formed of semiconductor material and extending throughout the thickness of said substrate region,

a second plug portion formed of semiconductor material and formed inside said epitaxial region, said second plug portion being aligned and in direct electrical contact with said first plug portion and further facing and in direct electrical contact with a first electromechanical connection region,

said first electromechanical connection region being formed of electrically conductive material arranged between said first body and said second body and in electrical contact with conductive regions of said first body,

said first insulation portion laterally surrounding said first plug portion, and

said second insulation portion laterally surrounding said second plug portion; and

a contact region of electrically conducting material extending on a free face of said substrate region in electrical contact with said first plug portion.

26. A composite structure comprising:

a first body of semiconductor material;

a second body of semiconductor material arranged on said first body and comprising an epitaxial region housing a micro-electromechanical device comprising a fixed part and a mobile part separated from one another by at least one delimitation trench extending through said epitaxial region and a substrate region forming a cap region which has larger dimensions than said mobile part and is fixed to said fixed part, said epitaxial region and said substrate region overlaid to each other and reciprocally insulated from one another by insulating regions; and

an electric connection structure, including:

a plug region extending throughout the thickness of said epitaxial region of said second body and made of semiconductor material, said plug region having a first face and a second face, said first face being in contact with a first electromechanical connection region, and said second face being in direct contact with at least one electric connection region of electrically conducting material,

said first electromechanical connection region of electrically conductive material arranged between said first body and said second body and in electrical contact with said plug region and with conductive regions of said first body, and

an insulation region laterally surrounding said plug region.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 6,504,253 B2
APPLICATION NO.	: 09/844180
DATED	: January 7, 2003
INVENTOR(S)	: Ubaldo Mastromatteo et al,

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, Line 63:
"first body); and" should read, --first body; and--

Column 10, Line 16:
"wherein said first body houses an electronic circuit); and" should read, --wherein said first body houses an electronic circuit; and--.

Signed and Sealed this
Twenty-first Day of February, 2012

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

EXHIBIT B

US006846690B2

(12) **United States Patent**
Farcy et al.

(10) **Patent No.: US 6,846,690 B2**
(45) **Date of Patent: Jan. 25, 2005**

(54) **INTEGRATED CIRCUIT COMPRISING AN AUXILIARY COMPONENT, FOR EXAMPLE A PASSIVE COMPONENT OR A MICROELECTROMECHANICAL SYSTEM, PLACED ABOVE AN ELECTRONIC CHIP, AND THE CORRESPONDING FABRICATION PROCESS**

(75) Inventors: **Alexis Farcy**, La Ravoire (FR); **Philippe Coronel**, Barraux (FR); **Pascal Ancey**, Revel (FR); **Joaquin Torres**, St. Martin le Vinoux (FR)

(73) Assignee: **STMicroelectronics S.A.**, Montrouge (FR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 26 days.

(21) Appl. No.: **10/308,482**

(22) Filed: **Dec. 3, 2002**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Dec. 3, 2001 (FR) 01 15594

(51) **Int. Cl.**[7] **H01L 21/00**; H01L 21/30
(52) **U.S. Cl.** **438/48**; 438/51; 438/455
(58) **Field of Search** 438/48, 51, 455

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,773,972 A 9/1988 Mikkor

FOREIGN PATENT DOCUMENTS

DE	100 27 234	12/2000
EP	0772045	* 7/1995
EP	0 772 045	5/1997
EP	1 079 431	2/2001
EP	1 096 259	5/2001
WO	WO 01/29529	4/2001

OTHER PUBLICATIONS

French Preliminary Search Report dated Jul. 16, 2002 for French Application No. 0115594.

* cited by examiner

Primary Examiner—Alexander Ghyka
(74) *Attorney, Agent, or Firm*—Lisa K. Jorgenson; Jose Gutman; Fleit, Kain, Gibbons, Gutman, Bongini & Bianco P.L.

(57) **ABSTRACT**

The fabrication of an integrated circuit includes a first phase of producing an electronic chip and a second phase of producing at least one auxiliary component placed above the chip and of producing a protective cover which covers the auxiliary component. The first phase of producing the chip is effected from a first semiconductor substrate and comprises the formation of a cavity lying in a chosen region of the chip and emerging at the upper surface of the chip. The second production phase includes the production of the auxiliary component from a second semiconductor substrate, separate from the first, and then the placement in the cavity of the auxiliary component supported by the second substrate and the mutual adhesion of the second substrate to the upper surface of the chip lying outside the cavity. The second substrate then also forms the protective cover.

15 Claims, 4 Drawing Sheets

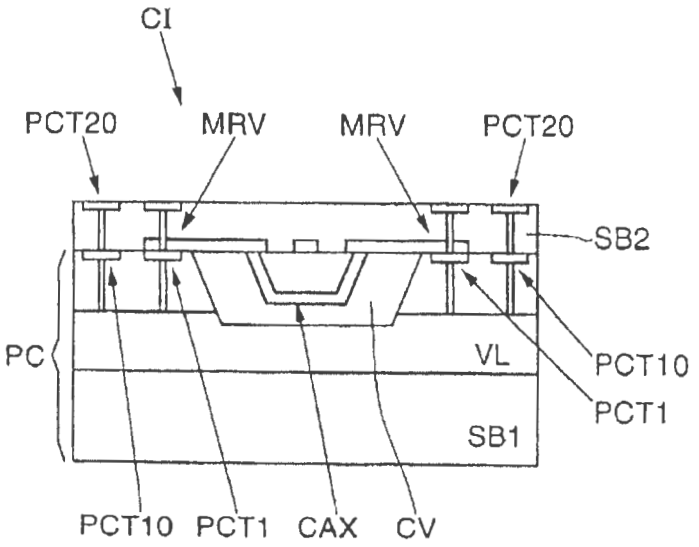


FIG.1

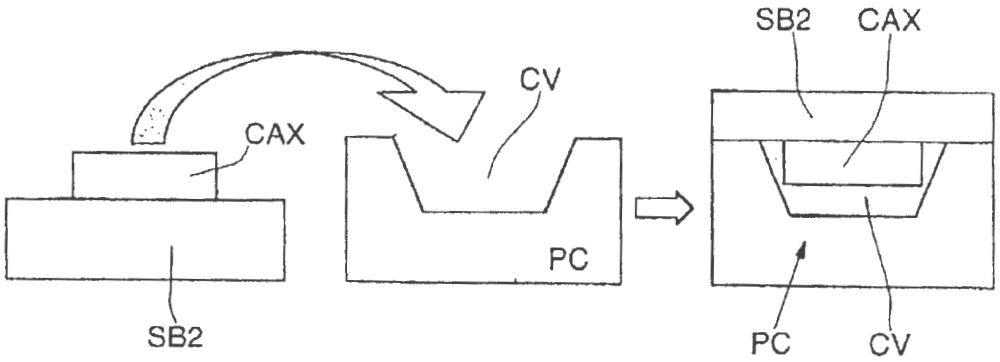


FIG.2a

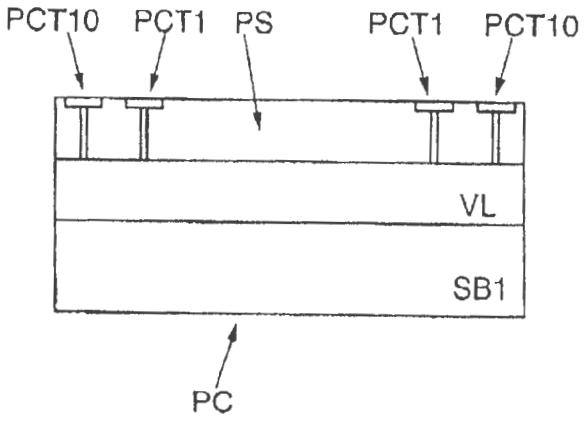


FIG.2b

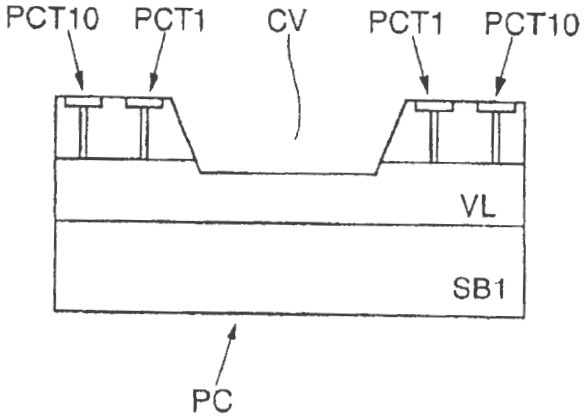


FIG.3a

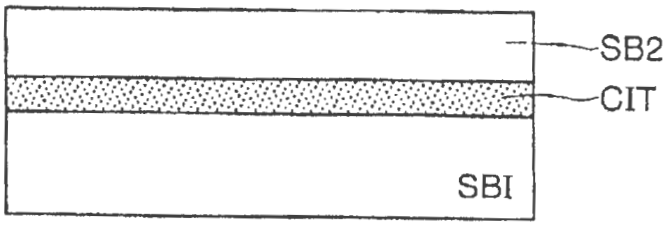
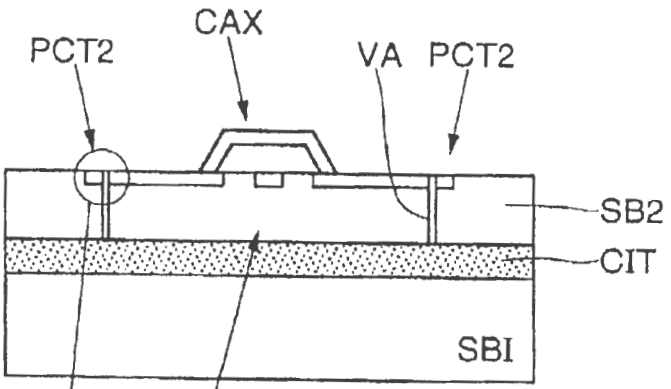


FIG.3b



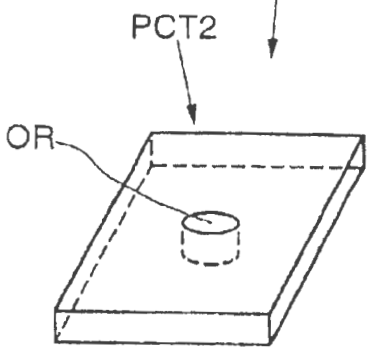


FIG.3c

FIG.4

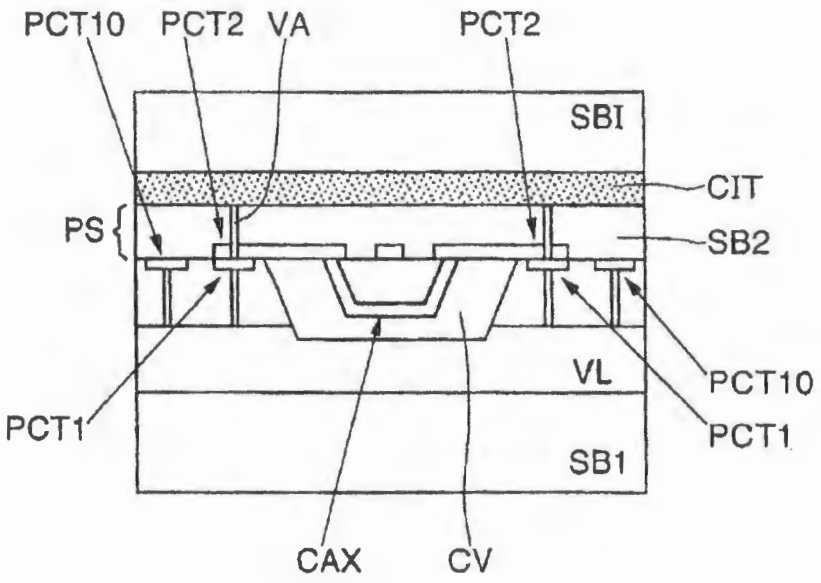

PCT10
PCT2
VA
PCT2
SBI
CIT
PS
SB2
VL
PCT10
PCT1
PCT1
SB1
CAX
CV

FIG.5

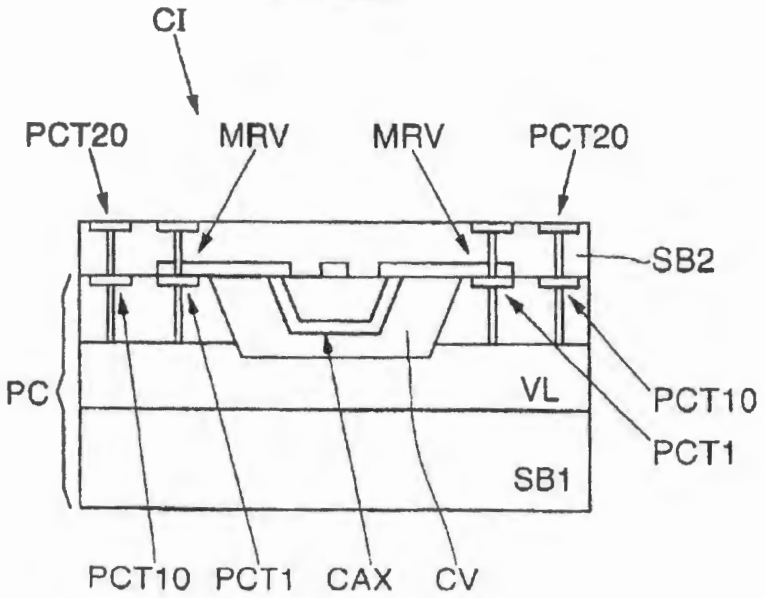

CI
PCT20
MRV
MRV
PCT20
SB2
PC
VL
PCT10
PCT1
SB1
PCT10
PCT1
CAX
CV

FIG.6

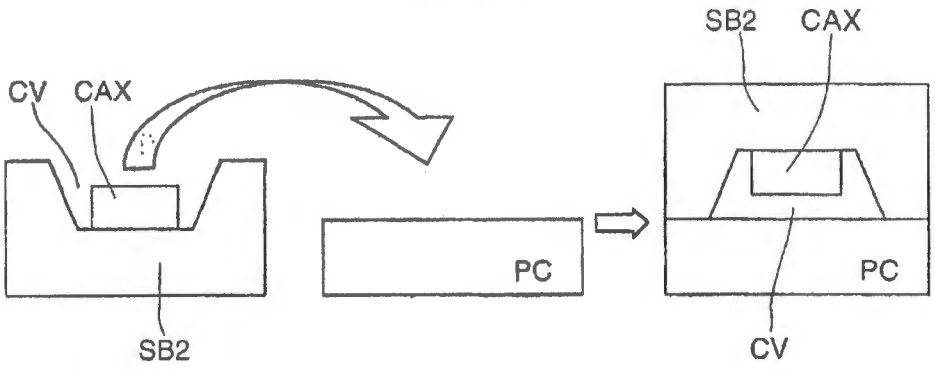
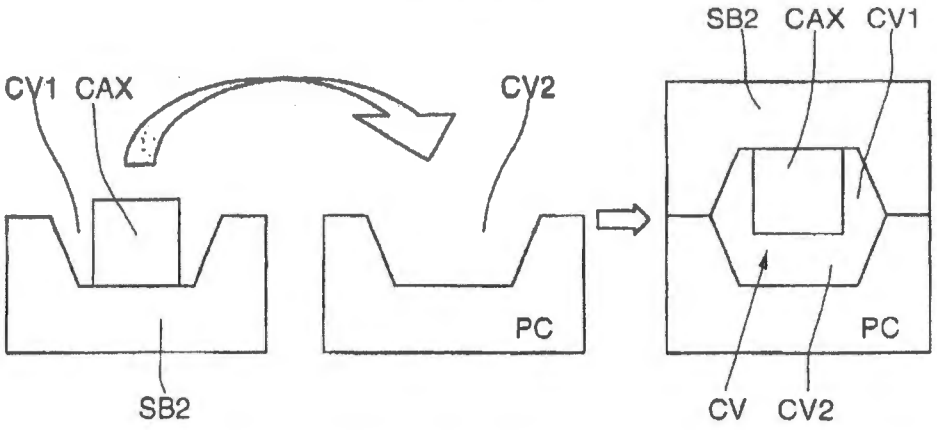

CV
CAX
SB2
PC
SB2
CAX
PC
CV

FIG.7


CV1
CAX
SB2
CV2
PC
SB2
CAX
CV1
PC
CV
CV2

INTEGRATED CIRCUIT COMPRISING AN AUXILIARY COMPONENT, FOR EXAMPLE A PASSIVE COMPONENT OR A MICROELECTROMECHANICAL SYSTEM, PLACED ABOVE AN ELECTRONIC CHIP, AND THE CORRESPONDING FABRICATION PROCESS

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims priority from prior French Patent Application No. 01 15594, filed on Dec. 3, 2001, the entire disclosure of which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to integrated circuits and more particularly to the incorporation of auxiliary components, such as high-performance passive components or microelectromechanical systems, on an electronic chip.

2. Description of the Related Art

The development of microelectronic technologies has been accompanied by an increasingly systematic integration of complex electrical functions, hitherto located outside the package of the integrated circuit. Among these functions, mention may be made of microelectromechanical systems (MEMS) and passive components known to those skilled in the art as above-IC components produced above the passivation layer covering the integrated circuit.

The production of these MEMS systems or passive components requires strict compatibility, especially thermal compatibility, of their steps with those of the production of the lower interconnect levels, and a protective layer before the circuit is packaged.

At the present time, the incorporation of high-performance passive components and microelectromechanical systems is divided into two steps, namely the incorporation of the component on the one hand and the assembly with a protective cover on the other.

The production of the component takes place directly on the chip where the digital and analogue circuits are integrated, above an insulating passivation layer.

The protective cover is produced by means of an additional layer placed above the component, this additional layer having to allow it to be mechanically isolated from the external world without thereby degrading performance or preventing its movement, especially in the case of microelectromechanical systems. In addition, strict compatibility between the "chip/component/protective cover" stack and the standard packaging processes proves to be necessary, in particular in the case of electrical connection of the chip to the package. At the present time, processes are known which ensure one or other of these functions.

By way of indication, mention may be made of the process known to those skilled in the art by the name "flip-chip". This process involves contacts which ensure the mechanical integrity of the stack and the electrical connection between the chip and the lower face of the cover. More specifically, a wafer, aligned with respect to the passivation layer on which the component has been produced, is bonded by partial fusion at a moderate temperature with the aid of solder bumps which then serve as support. This flip-chip procedure damages neither the interconnects nor the component to be covered. However, the discrete nature of the solder bumps does not protect the side walls of the component, for example a microswitch.

According to a second approach, again after having produced the component on the passivation layer covering the integrated circuit, the component is covered with a wafer in which a cavity intended to receive the component has been made. This wafer is fixed to the passivation layer of the integrated circuit with the aid of a polymer material which acts as adhesive. Mechanical isolation is complete. On the other hand, the two wafers remain electrically isolated and only localized etching of the cover above the contact pads will allow contact with the lower circuit by means of additional steps during packaging.

Thus, in the prior art, no method allows both the component to be protected and the electrical contacting, indispensable for packaging, to be guaranteed.

Added to this limitation are further drawbacks which are associated with the contemplated approach and which complicate the integration.

This is because the component is produced above the electronic chip. To avoid any damage to the lower interconnect levels, this production must not involve temperatures above 450° C. However, this constraint in particular prevents the use of specific materials, such as certain dielectrics having a very high permittivity.

Moreover, the processes of the prior art finally end up with a stack substantially greater than 500 microns in height, which no longer allows the standard packaging procedures to be applied. It is then necessary to thin the cover, but its handling then becomes a tricky operation because of its mechanical fragility.

Moreover, once the wafers have been assembled, it becomes difficult to perform further technological operations because of the non-uniformity of the thickness of the adhesive polymer and of the solder bumps which mean that the upper surface has a poor flatness.

Accordingly, there exists a need for overcoming the disadvantages of the prior art as discussed above.

SUMMARY OF THE INVENTION

The invention aims to provide a solution to these problems.

One object of the invention is to provide an assembly which has an almost perfectly plane upper surface allowing further technological steps to be carried out.

The object of the invention is also to make the production of an "electronic chip/component" assembly compatible with standard packaging processes.

The object of the invention is also to ensure at the same time electrical connection of the component to the chip and its mechanical encapsulation.

The invention therefore provides a process for fabricating an integrated circuit, comprising a phase of producing an electronic chip and a phase of producing at least one auxiliary component (for example a passive component or else a MEMS-type component) placed above the chip and of producing a protective cover which covers the auxiliary component.

According to a general feature of the invention, the chip is produced from a first semiconductor substrate, whereas the auxiliary component is produced from a second semiconductor substrate, separate from the first. The second substrate supporting the auxiliary component is made to adhere mutually to the first semiconductor substrate in an

adhesion region lying outside a cavity containing the auxiliary component and extending into one or other of the two substrates or into both substrates, the second substrate then also forming the protective cover.

In other words, according to the invention, the chip on a standard semiconductor wafer and the auxiliary component on another specific wafer are produced independently. Thus, there is no risk of the processes involving the auxiliary component damaging the chip interconnects.

Moreover, the use of a virgin wafer as support for producing the auxiliary component greatly widens the choice of material processes, independently of the constraints associated with the interconnects.

The cavity may be produced only in the chip from it's front face, or else only in the wafer used to produce the auxiliary component. The cavity may also be formed from two cavity portions formed facing each other in the chip and in the wafer, respectively.

Thus, according to a first implementational variant, the phase of producing the chip comprises the formation of the cavity lying in a chosen region of the chip and emerging at the upper surface (i.e. the front face) of the chip, and the phase of producing the auxiliary component and the protective cover comprises the placement, in the cavity, of the auxiliary component supported by the second substrate and the mutual adhesion of the second substrate to the upper surface of the chip lying outside the cavity, the second substrate then also forming the protective cover.

According to a second implementational variant, the phase of producing the auxiliary component and the cover comprises the formation of the cavity in the second substrate and the production of the auxiliary component in the cavity, and then the mutual adhesion of the second substrate to the upper surface of the chip lying outside the cavity, the second substrate then also forming the protective cover.

According to a third implementational variant, the phase of producing the chip comprises the formation of a first cavity portion lying in a chosen region of the chip and emerging at the upper surface of the chip. The phase of producing the auxiliary component and the cover comprises the formation of a second cavity portion in the second substrate and the production of the auxiliary component in the second cavity portion, and then the mutual adhesion of the second substrate to the upper surface of the chip lying outside the cavity which is then formed by the two cavity portions, the second substrate then also forming the protective cover.

According to a method of implementing the process compatible with the three abovementioned variants, the production of the auxiliary component comprises:

- the formation on an initial substrate, for example a silicon substrate, of an intermediate layer composed of at least one sublayer of a material that can be selectively removed with respect to the material forming the second substrate and with respect to the material forming the initial substrate;
- the formation of the second substrate on the intermediate layer; and
- the formation of the auxiliary component on the second substrate, this auxiliary component projecting from the upper surface of the second substrate (it being possible, depending on the implementational variant, for this upper surface to be plane or recessed in order to provide a cavity or a cavity portion).

Moreover, the production of the protective cover comprises, after the upper surface of the chip lying outside the cavity has adhered to the corresponding facing portion of the surface of the second substrate, the removal of the sublayer and of the initial substrate.

The use of a buried layer (intermediate layer) allows fine control of the thickness of the layer which will cover the electronic chip, that is to say the thickness of the second substrate. Etching of the vias (interconnect holes) is thereby considerably facilitated and the thickness of the whole assembly remains compatible with the standard packaging processes. In addition, this process permits, as final passivation, a wide choice of materials compatible with the radiofrequency performance required, should this be necessary.

When the intermediate layer is entirely formed from the removable material, it is completely removed. However, as a variant, the intermediate layer may be formed from a stack of several sublayers, some but not all of which are composed of a material that can be selectively removed with respect to the material forming the second substrate and with respect to the material forming the initial substrate. In this case after the adhesion step, all the removable sublayers and the initial substrate are removed.

In this variant, there then remain sublayers, which may be made of silicon, for example, on which further transistors or other active components may, for example, be produced.

According to one method of implementing the invention, the production of the electronic chip comprises the production of first contact pads emerging at the upper surface of the chip within the adhesion region. The production of the auxiliary component comprises the production of second contact pads within the adhesion region (at the periphery of the auxiliary component). During mutual adhesion, the second contact pads come into contact with the first contact pads.

Thus, if the first and second contact pads are made of metal and at least one of the first contact pads is connected to the chip, while at least one of the second contact pads is connected to the auxiliary component, electrical connection and mechanical connection between the chip and the auxiliary component are made at the time.

Moreover it is particularly advantageous that the production of each second contact pad comprises the formation of an orifice passing through the pad. Thus, after a second pad has been brought into contact with a corresponding first pad, a rivet is made by metallization in the orifice of the second pad. In other words, metallization of the vias which pass through the protective cover electrically connect the two wafers and improve the mechanical strength of the assembly by generating microscopic rivets. The latter may be distributed where the designer chooses, at key points on the chip so as to optimize the mechanical integrity of the whole assembly.

Although various options are provided for carrying out the step of mutual adhesion of the two substrates, such as for example the use of a polymer material, it is particularly advantageous for this adhesion to be carried out by low-temperature molecular bonding. This prevents any circuit from being damaged. Moreover, molecular bonding preserves the option of carrying out both the electrical connection and the mechanical connection, whereas if an adhesion technique using a polymer material between the contact pads is employed, it is necessary to provide an electrical connection at a point other than at the contact pads.

The subject of the invention is also an integrated circuit comprising an electronic chip, at least one auxiliary component placed above the chip and a protective cover which covers the auxiliary component.

According to a general feature of the invention, the auxiliary component projects from the lower face of a

semiconductor substrate and extends into a cavity made in the chip or in the semiconductor substrate or in both. The substrate also forms the protective cover. The lower face of the substrate is fixed to that portion of the upper surface of the chip lying outside the cavity and the upper face of the substrate supporting the auxiliary component is approximately plane.

According to a first embodiment variant, the lower surface of the semiconductor substrate is plane and the upper surface of the chip has a shape which provides the cavity in a chosen region of the chip.

According to a second embodiment variant, the upper surface of the chip is plane and the lower surface of the semiconductor substrate has a shape which provides the cavity in this semiconductor substrate.

According to a third embodiment variant, the lower surface of the semiconductor substrate has a shape which provides a first cavity portion in this semiconductor substrate, and the upper surface of the chip has a shape which provides a second cavity portion in a chosen region of the chip. The cavity is then formed from the two cavity portions facing each other.

According to an embodiment of the invention compatible with these three embodiment variants, the electronic chip includes first contact pads emerging at the upper surface of the chip outside the cavity. The auxiliary component for its part includes second contact pads lying on the periphery of the auxiliary component. The second contact pads are in contact with the first contact pads.

The integrated circuit advantageously includes rivets fastening each second contact pad to the corresponding first pad.

BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages and features of the invention will become apparent on reading the detailed description of entirely non-limiting embodiments and methods of implementation, and the appended drawings in which:

FIG. **1** illustrates in a very general and highly schematic manner, a first method of implementing the process according to the invention, making it possible to end up with a first embodiment of an integrated circuit according to the invention;

FIGS. **2***a* and **2***b* illustrate in greater detail, but again schematically, steps in a method of implementing the process, leading to the furnishing of the electronic chip;

FIGS. **3***a* to **3***c* illustrate in greater detail, but again schematically, certain steps in a method of implementing the process resulting in the production of an auxiliary component;

FIGS. **4** and **5** illustrate in greater detail, but again schematically, assembly steps in the process according to the invention, making it possible to end up with an integrated circuit according to the invention; and

FIGS. **6** and **7** illustrate in a very general and highly schematic manner, two other methods of implementing the process according to the invention, making it possible to end up with two other embodiments of an integrated circuit according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the left-hand part of FIG. **1**, the reference **SB2** denotes a semiconductor substrate on which an auxiliary component CAX, for example a passive component, or else a microelectromechanical system, has been produced.

Moreover, on a substrate separate from the substrate **SB2**, in a conventional manner known per se, an electronic chip PC is produced and a cavity CV intended to house the component CAX is provided, at a chosen point, in the upper portion of this electronic chip PC.

Next, as illustrated in the right-hand part of FIG. **1**, the upper face (which has become the lower face in the right-hand part of FIG. **1**) of the substrate **SB2** is fastened to that part of the upper face of the electronic chip lying outside the cavity CV.

An integrated circuit is then obtained which, after packaging, comprises an assembly consisting of an electronic chip PC and an auxiliary component CAX, the upper surface of which assembly is approximately plane.

This method of implementing the invention will now be explained in greater detail with reference to the following figures.

In FIG. **2***a*, the electronic chip PC is produced in a conventional manner known per se from a silicon substrate **SB1**, above which a certain number of interconnect levels VL are provided. The whole assembly is covered with an insulating passivation layer PS, for example formed from silicon dioxide. Metal tracks and contact pads, **PCT1**, **PCT10**, produced in a conventional manner known per se, emerge at the surface of the passivation layer and allow interconnections with components of the electronic chip located in the silicon substrate, by means of various interconnect levels.

Moreover, a cavity CV, which is intended to house the auxiliary component CAX, is provided in a chosen region of the electronic chip. This cavity CV (FIG. **2***b*) lies in a region which is, for example, stripped of metal and which, in any case, will not interfere with the structure or the operation of the electronic components of the chip. The depth of the cavity depends on the height of the auxiliary component CAX which will be inserted thereinto. Depending on the applications, the cavity may extend only into the passivation layer or else may be etched through the passivation layer, a certain number of interconnect levels VL and possibly right down to the substrate **SB1**.

Moreover, the auxiliary component CAX shall be produced on a second substrate SB2 (FIG. **3***a*) which is completely separate from the substrate of the electronic chip PC.

More specifically, in this method of implementation, the substrate **SB2**, for example made of silicon, is produced from an initial substrate **SB1**, on which a layer, called "intermediate layer CIT", has been produced. The substrate SB2 rests on this intermediate layer CIT.

The intermediate layer CIT is therefore a buried layer. It is formed from a material which can be removed selectively with respect to the material forming the substrate SB2 and the substrate SB1.

As an example, the assembly formed from the initial substrate **SB1**, from the buried layer CIT and from the second substrate **SB2** may be a silicon-on-insulator substrate (SOI) substrate, the structure and the production of which are well known to those skilled in the art. In this case, the substrate **SB2** is, for example, a thin layer of silicon resting on silicon dioxide forming the buried layer CIT.

As a variant, the layer CIT may be formed by epitaxial growth of a silicon-germanium alloy on the initial substrate **SB1** formed from silicon. The second, silicon substrate SB2 is then itself grown epitaxially on the layer CIT.

Next, as illustrated in FIG. **3***b*, an auxiliary component CAX, in this case a microelectromechanical system, is

produced in a conventional manner known per se in and on the substrate SB2.

This component CAX includes peripheral extensions forming contact pads PCT2.

As illustrated in FIG. 3c, each contact pad PCT2 is pierced by a central orifice OR which is extended by a hole or via VA into the substrate SB2 as far as the buried layer CIT. However, as a variant, this central orifice may be etched subsequently, for example at the same time as the cavities PCT20 (FIG. 5), once the adhesion has been effected.

As will be seen in greater detail below, the pads PCT2 which flank the microswitch are intended to connect it electrically and mechanically to the other wafer, that is to say to the electronic chip, on which the control circuits are to be found.

The next step consists in turning the assembly supporting the auxiliary component CAX upside down and then in aligning this assembly with the electronic chip so that the microswitch CAX fits perfectly into the cavity CV provided for this purpose (FIG. 4).

The contact pads PCT2 then come into contact with the contact pads PCT1 of the electronic chip.

The adhesion of the substrate SB2 to the upper surface of the electronic chip lying outside the cavity CV is preferably effected by low-temperature molecular bonding. Such molecular bonding is well known to a person skilled in the art and he may refer, for example, to the article by M. Bruel, B. Aspar and A. J. Auberton-Hervé *"Smart-Cut: a New Silicon-On-Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding"*, Japanese Journal of Applied Physics, Vol. 36, pp. 1636–1641, Part I, No. 3B, March 1997.

This molecular bonding has the advantage of not requiring any additional material to effect the adhesion. Moreover, it damages no circuit and thus makes compatible simultaneous electrical connection with mechanical connection effected at the contact pads PCT1 and PCT2.

The material of the buried layer CIT is then selectively removed, for example by selective etching well known to those skilled in the art, the characteristics of which depend on the material used. Removal of this material of the CIT layer also involves removal of the initial substrate SB1, if the latter had not been removed beforehand by another technique, for example by a process well known to those skilled in the art by the name "smart-cut".

There then only remains (FIG. 5) the second substrate SB2 which supports the component CAX and which consequently forms the upper layer of the integrated circuit formed from the "electronic chip PC/auxiliary component CAX" assembly.

Next, the substrate SB2 is etched so as to produce vias and metal tracks and/or contact pads PCT20 which, after metallization, come into contact with the tracks and/or contact pads PCT10. Likewise, surface cavities are produced in the extension of the vias VA, which will form on the surface, after metallization, the metal tracks and/or contact pads. Moreover, at the interface between the substrate SB2 and the passivation layer of the electronic chip, this metallization of the orifices OR will generate microrivets MRV which will improve the mechanical integrity of the assembly.

The integrated circuit thus obtained has an almost perfectly plane upper surface and if necessary it will be possible to produce, on this upper surface, other levels of vias and metal tracks, or of active components, particularly when the intermediate layer is formed from a stack of sublayers, some of which were not selectively removable, since in this case there remains on the upper surface of the substrate SB2 one or more plane sublayers on which these other levels may be produced.

Although in the variant that has just been described the cavity CV was produced just in the substrate SB2, it is possible to produce this cavity just in the chip PC (FIG. 6) or else both in the substrate SB2 and in the chip PC (FIG. 7). The cavity CV is then composed of two cavity portions CV1 and CV2 facing each other.

While there has been illustrated and described what are presently considered to be the preferred embodiments of the present invention, it will be understood by those of ordinary skill in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the present invention.

Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive concept described herein. Furthermore, an embodiment of the present invention may not include all of the features described above. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A process for fabricating an integrated circuit comprising the production of an electronic chip and the production of at least one auxiliary component placed above the chip and of a protective cover which covers the auxiliary component, wherein the chip is produced from a first semiconductor substrate, in that the auxiliary component is produced from a second semiconductor substrate, separate from the first and in that the second substrate supporting the auxiliary component is made to adhere mutually to the first semiconductor substrate in an adhesion region lying outside a cavity containing the auxiliary component and extending into one or other of the two substrates or into both substrates, the second substrate then also forming the protective cover.

2. The process according to claim 1, wherein the phase of producing the chip comprises the formation of the cavity lying in a chosen region of the chip and emerging at the upper surface of the chip and in that the phase of producing the auxiliary component and the protective cover comprises the placement, in the cavity, of the auxiliary component supported by the second substrate and the mutual adhesion of the second substrate to the upper surface of the chip lying outside the cavity, the second substrate then also forming the protective cover.

3. The process according to claim 1, wherein the phase of producing the auxiliary component and the cover comprises the formation of the cavity in the second substrate and the production of the auxiliary component in the cavity, and then the mutual adhesion of the second substrate to the upper surface of the chip lying outside the cavity, the second substrate then also forming the protective cover.

4. The process according to claim 1, wherein the phase of producing the chip comprises the formation of a first cavity portion lying in a chosen region of the chip and emerging at the upper surface of the chip, in that the phase of producing the auxiliary component and the cover comprises the formation of a second cavity portion in the second substrate and the production of the auxiliary component in the second cavity portion, and then the mutual adhesion of the second substrate to the upper surface of the chip lying outside the cavity formed by the two cavity portions, the second substrate then also forming the protective cover.

5. A process for fabricating an integrated circuit comprising the production of an electronic chip and the production of at least one auxiliary component placed above the chip and of a protective cover which covers the auxiliary component, wherein the chip is produced from a first semiconductor substrate, in that the auxiliary component is produced from a second semiconductor substrate, separate from the first and in that the second substrate supporting the auxiliary component is made to adhere mutually to the first semiconductor substrate in an adhesion region lying outside a cavity containing the auxiliary component and extending into one or other of the two substrates or into both substrates, the second substrate then also forming the protective cover, wherein the adhesion step is effected by molecular bonding.

6. A process for fabricating an integrated circuit comprising the production of an electronic chip and the production of at least one auxiliary component placed above the chip and of a protective cover which covers the auxiliary component, wherein the chip is produced from a first semiconductor substrate, in that the auxiliary component is produced from a second semiconductor substrate, separate from the first and in that the second substrate supporting the auxiliary component is made to adhere mutually to the first semiconductor substrate in an adhesion region lying outside a cavity containing the auxiliary component and extending into one or other of the two substrates or into both substrates, the second substrate then also forming the protective cover, wherein the production of the auxiliary component comprises the formation on an initial substrate of an intermediate layer composed of at least one sublayer of a material that can be selectively removed with respect to the material forming the second substrate and with respect to the material forming the initial substrate, the formation of the second substrate on the intermediate layer and the formation of the auxiliary component on the second substrate, this auxiliary component projecting from the upper surface of the second substrate and in that the production of the protective cover comprises, after the upper surface of the chip lying outside the cavity has adhered to the corresponding facing portion of the surface of the second substrate, the removal of the sublayer and of the initial substrate.

7. The process according to claim 6, wherein the intermediate layer is formed from a stack of several sublayers, some but not all of which are composed of a material that can be selectively removed with respect to the material forming the second substrate and with respect to the material forming the initial substrate, and in that, after the adhesion step, all the removable sublayers and the initial substrate are removed.

8. The process according to claim 6, wherein the adhesion step is effected by molecular bonding.

9. A process for fabricating an integrated circuit comprising the production of an electronic chip and the production of at least one auxiliary component placed above the chip and of a protective cover which covers the auxiliary component, wherein the chip is produced from a first semiconductor substrate, in that the auxiliary component is produced from a second semiconductor substrate, separate from the first and in that the second substrate supporting the auxiliary component is made to adhere mutually to the first semiconductor substrate in an adhesion region lying outside a cavity containing the auxiliary component and extending into one or other of the two substrates or into both substrates, the second substrate then also forming the protective cover, wherein the production of the electronic chip comprises the production of first contact pads emerging at the upper surface of the chip inside the adhesion region, in that the production of the auxiliary component comprises the production of second contact pads within the adhesion region and in that, during the mutual adhesion, the second contact pads come into contact with the first contact pads.

10. The process according to claim 9, wherein the first and second contact pads are made of metal, at least one of the first contact pads being connected to the chip while at least one of the second contact pads is connected to the auxiliary component, so as to ensure electrical connection between the chip and the auxiliary component.

11. The process according to claim 10, wherein the formation of the orifice passing through a second contact pad comprises the piercing of the second contact pad and the etching of the second substrate in the extension of the hole in the second contact pad and in that the production of the rivet comprises the metallization of the etched orifice of the second substrate and of the through-orifice of the second connection pad.

12. The process according to claim 9, wherein the production of each second contact pad comprises the formation of an orifice passing through the pad and in that, after a second pad has been brought into contact with a corresponding first pad, a rivet is produced in the orifice of the second pad.

13. The process according to claim 12, wherein the first and second contact pads are made of metal, at least one of the first contact pads being connected to the chip while at least one of the second contact pads is connected to the auxiliary component, so as to ensure electrical connection between the chip and the auxiliary component.

14. The process according to claim 13, wherein the formation of the orifice passing through a second contact pad comprises the piercing of the second contact pad and the etching of the second substrate in the extension of the hole in the second contact pad and in that the production of the rivet comprises the metallization of the etched orifice of the second substrate and of the through-orifice of the second connection pad.

15. The process according to claim 12, wherein the adhesion step is effected by molecular bonding.

* * * * *

EXHIBIT C

US006405592B1

(12) **United States Patent**
Murari et al.

(10) **Patent No.: US 6,405,592 B1**
(45) **Date of Patent: Jun. 18, 2002**

(54) **HERMETICALLY-SEALED SENSOR WITH A MOVABLE MICROSTRUCTURE**

(75) Inventors: **Bruno Murari**, Monza; **Benedetto Vigna**, Potenza; **Paolo Ferrari**, Gallarate, all of (IT)

(73) Assignee: **STMicrlelectronics S.r.l.**, Agrate Brianza (IT)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Jun. 19, 1998**

(30) **Foreign Application Priority Data**

Jun. 19, 1997 (EP) 97830290

(51) **Int. Cl.**[7] **G01P 1/02**; G01P 15/125
(52) **U.S. Cl.** **73/493**; 73/514.32
(58) **Field of Search** 73/493, 514.32, 73/514.16, 514.29, 431, 718, 719, 720, 721, 724, 756, 754; 257/417, 415

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,314,225	A	2/1982	Tominaga et al.	338/4
4,399,707	A	8/1983	Wamstad	73/727
4,528,853	A	7/1985	Lerch et al.	73/624
5,111,693	A	5/1992	Greiff	73/514
5,164,328	A	11/1992	Dunn et al.	437/54
5,168,344	A	12/1992	Ehlert et al.	257/693
5,259,247	A	11/1993	Bantien	73/718
5,285,690	A	2/1994	Koen et al.	73/727
5,438,859	A *	8/1995	Yamashita et al.	73/514.34
5,650,567	A *	7/1997	Ueda et al.	73/493
5,719,334	A *	2/1998	Parsons	73/514.32
5,723,904	A *	3/1998	Shiga	257/698
5,750,926	A	5/1998	Schulman et al.	174/52.3
5,864,063	A *	1/1999	Otani et al.	73/514.32

FOREIGN PATENT DOCUMENTS

EP	0773443 A1	5/1997
EP	0732594 B1	11/1998
WO	WO 96/39632 *	12/1996

* cited by examiner

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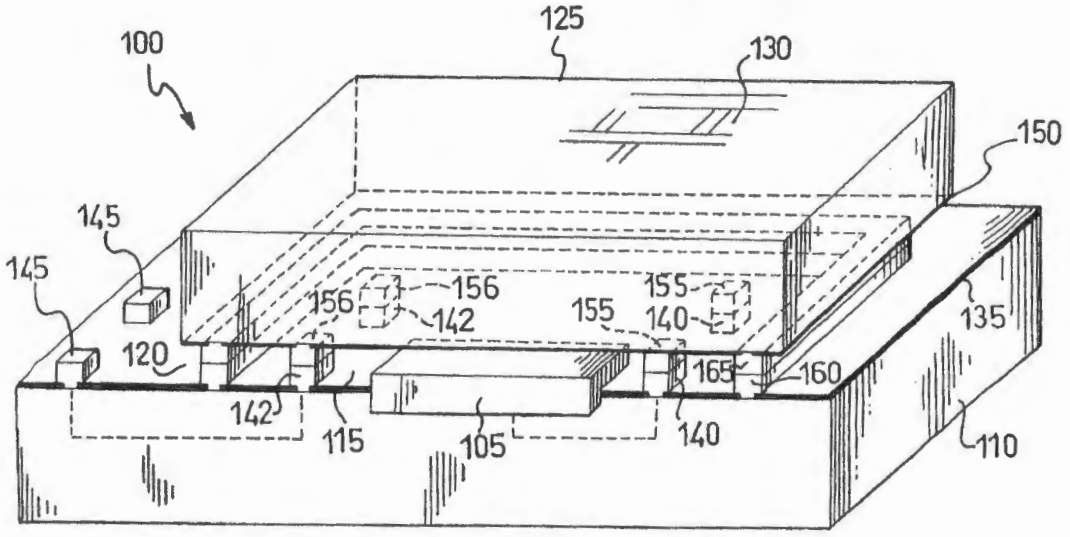
(57) **ABSTRACT**

A sensor with a movable microstructure including a sensitive element, formed in a first chip of semiconductor material for producing an electrical signal dependent on a movement of at least one movable microstructure relative to a surface of the first chip. The sensitive element is enclosed in a hollow hermetic structure, and circuitry for processing the electrical signal is formed in a second chip of semiconductor material. The hollow hermetic structure includes a metal wall disposed on the surface of the first chip around the sensitive element, and the second chip is fixed to the metal wall.

15 Claims, 1 Drawing Sheet



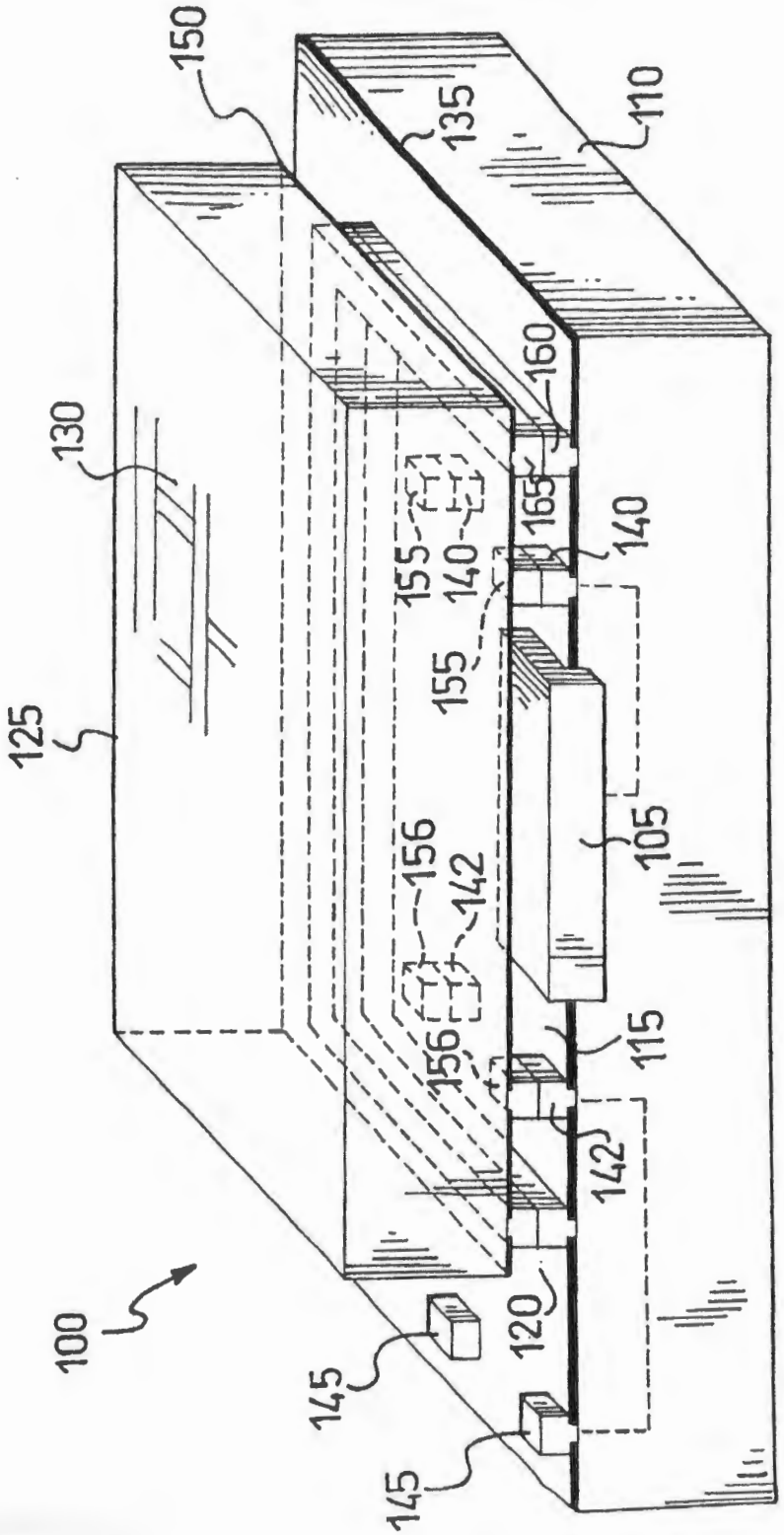

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FIG.1

HERMETICALLY-SEALED SENSOR WITH A MOVABLE MICROSTRUCTURE

TECHNICAL FIELD

The present invention relates to a sensor with a movable microstructure.

BACKGROUND OF THE INVENTION

Sensors with movable microstructures such as, for example, inertial sensors which can measure a physical quantity relating to a movement of the sensor and produce an output signal dependent on the quantity are used in various applications, for example, in the automotive field for monitoring various devices such as air bags, anti-slip braking systems (ABS), and active suspensions, or in other fields such as consumer electronics, computers and the like. Sensors with movable microstructures are formed on a microscopic scale in chips of semiconductor material; a sensor of this type comprises a sensitive element which can produce an electrical signal relating to the movement of a microstructure movable relative to a surface of the chip.

In sensors with movable microstructures, the sensitive element has to be suitably protected by being enclosed in a hermetic structure to ensure that it operates in a controlled environment; this allows the microstructure of the sensitive element, which has a very small mass, to move with little resistance and minimal damping so as to ensure good sensitivity of the sensor. A sensor of this type also includes a circuitry which processes the electrical signal generated by the sensitive element and which, in turn, has to be encapsulated in a suitable container or package which protects the processing circuitry from external environmental conditions, ensuring that it operates correctly.

A known technique for protecting a sensor with a movable microstructure consists in the encapsulation of the sensitive element and the processing circuitry in a hermetic, for example, ceramic or metal package; the sensitive element and the processing circuitry can thus be incorporated in the same semiconductor chip.

However., this technique is extremely expensive, resulting in a high final product cost.

A different known technique consists in the production of a hollow structure on a microscopic scale (a micro-cavity) which houses the sensitive element. This isolation method involves micromachining of a silicon or glass chip which is then connected to the chip on which the sensitive element is formed, for example, by an anodic bonding technique; this technique allows inexpensive standard plastic packages to be used for encapsulating the final product. However, the known solution described above is quite complex and expensive. Moreover, this technique does not allow the sensitive element and the processing circuitry to be incorporated in the same chip since the bonding step requires the surfaces joined to be perfectly flat (with a peak-valley roughness of the order of a hundred angstroms); generally, the plate containing the sensitive element and that containing the processing circuitry are arranged side by side and are connected electrically by means of suitable metal wires.

The sensitive elements of sensors with movable microstructures are usually made in large numbers in several identical areas of a wafer of semiconductor material which are subsequently separated by a suitable cutting operation. The cutting is generally carried out by means of a high-velocity, water-cooled, diamond-blade saw. A further disadvantage of the known sensors is that, during the drying of the water used for cooling the blade, permanent sticking or "stiction" of the movable microstructure to an underlying surface of the semiconductor chip may occur. This physical phenomenon renders the sensor unusable.

SUMMARY OF THE INVENTION

According to principles of the present invention, a sensor is provided having a sensitive element in a first chip of semiconductor material. The sensitive element produces an electrical signal dependent on a movement of a movable microstructure relative to a surface of the first chip of semiconductor material. The sensitive element is enclosed in a hollow hermetic structure, and a processing circuit formed in the second chip of semiconductor material is coupled to receive and process the electrical signal from the sensitive element. The hermetic structure includes a metal wall around the sensitive element that is fixed between the first chip and the second chip.

The sensor with a movable microstructure according to an embodiment of the present invention is particularly compact, simple and inexpensive. This sensor permits the optional use of a plastic, and hence extremely inexpensive, package for encapsulating the final product.

A method of producing the sensor according to another embodiment of the present invention does not require micromachining of a further silicon or glass wafer or connection thereof to the wafer on which the sensitive elements are formed. Moreover, both of the semiconductor chips used in the structure of the present invention contain active elements (the sensitive element and the processing circuitry, respectively) so that there is no wastage of material.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows a sensor in a partially-sectioned schematic view according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows a sensor **100** according to an embodiment of the present invention having a movable microstructure and, in particular, an inertial sensor comprising a sensitive element **105** which can detect a physical quantity relating to the inertia of one or more movable microstructures and can produce a corresponding electrical signal. The sensitive element **105** includes, for example, a micro-mechanical structure (a micro-electro-mechanical structure, or MEMS) formed on an upper surface of a chip **110** of semiconductor material, typically silicon. The sensitive element **105** generally has a seismic mass anchored to the chip **110** at predetermined points and movable relative thereto, its movement being converted into a suitable electrical signal. For example, the seismic mass may comprise a first electrode of a capacitor having a second electrode which is provided on the chip **110**; a movement of the seismic mass brings about a change in the capacitance of the capacitor which in turn is measured by a suitable circuit. The sensor **100** may be, for example, an accelerometer, an angular velocity sensor (a gyroscope) or a vibration sensor, in which the microstructure of the sensitive element **105** moves as a result of linear/angular acceleration or of an angular velocity of a system (for example, a motor-car) on which it is mounted, enabling the desired physical quantity to be measured. In alternative embodiments of the present invention, the sensor is a resonant sensor in which the movable microstructure of the sensitive element **105** vibrates at a frequency which varies in dependence on the quantity to be detected.

The sensitive element **105** is sealed within a hollow hermetic structure **115** which protects the sensitive element **105** from microscopic particles and from damage resulting from assembly operations, as well as ensuring a leak tight structure with respect to an internal gas (for example, air or nitrogen, typically at a pressure lower than atmospheric pressure) for regulating the damping of the movable microstructure of the sensitive element **105**. In the sensor **100** of the present invention, the hollow hermetic structure **115** is defined laterally by a wall **120** (formed, for example, of a metal such as aluminium, nickel, copper, or the like) which is disposed on the upper surface of the chip **110** around the sensitive element **105**, the shape (for example, circular or rectangular) of which varies according to the shape of the sensitive element **105**. The hollow hermetic structure **115** is closed at the top by a further chip of semiconductor material **125** (having a size at least equal to that of a cavity of the hermetic structure **115**) which is fixed to the wall **120**. Circuitry **130** for processing an electrical signal produced by the sensitive element **105** is integrated in the semiconductor chip **125** and, for example, can amplify, control, compensate, and calibrate the signal. It should be noted that the movable microstructure (enclosed in a metal cavity) is advantageously screened from electromagnetic interference, for example, by a connection of the chip **125** to a reference terminal or to ground.

Contact electrodes formed on the upper surface of the chip **110**, which is covered with an insulating layer **135** (typically silicon dioxide), are comprised by one or more conductive pads **140, 142** (four in the embodiment shown in FIG. 1) arranged inside the hollow hermetic structure **115** and by one or more conductive pads **145** (two in the embodiment shown in FIG. 1) arranged outside the hollow hermetic structure **115**. Similarly, contact electrodes comprised by one or more pads **155** and **156** (four in the embodiment shown in FIG. 1) are formed on a lower surface of the chip **125**, which is covered by an insulating layer **150**. Each of the pads **155, 156** formed on the chip **125** is arranged facing and connected to a corresponding pad **140, 142** formed on the chip **110**. The pads **140** are connected electrically to the sensitive element **105** in order to transmit the electrical signal generated by the sensitive element **105** to the corresponding pads **155** and hence to the processing circuitry **130**; the connection between the sensitive element **105** and the pads **140** is achieved, for example, by means of a low-resistance diffusion in the semiconductor chip **110** brought about before or after the growth of an epitaxial layer or by means of metal connections at a level below that at which the metal wall **120** is formed. The electrical signal processed by the circuitry **130** is transferred to the pads **142** by means of the corresponding pads **156**.

The pads **142** are connected electrically to the pads **145** in a similar manner in order to transmit the processed electrical signal to an external circuit. Alternative embodiments of the present invention may be implemented with different methods of electrical connection between the chip containing the sensitive element and the chip containing the processing circuitry. For example, the contact electrodes connected to the sensitive element may be arranged outside the hermetic cavity and the contact electrodes connected to the processing circuitry may be arranged on the upper surface of the respective chip and then connected by means of metal wires.

The sensor **100** described above may be produced starting with a first semiconductor wafer on an upper surface of which a large number of sensitive elements **105** are formed by known micromachining techniques. A metallic aluminium layer (typically 1μm thick) is deposited on the entire upper surface of the wafer and the pads **140, 142, 145** and a lower frame **160**, used (as described below) for forming the metal wall **120**, are defined therein by known masking and selective etching techniques. The wafer is then covered with the insulating layer **135** in which openings or windows are similarly formed in the regions of the pads **140, 142, 145** and of the lower frame **160**. A thin layer (a flash) of gold which protects against oxidation and improves the quality of the welding is preferably deposited on the pads **140, 142, 145** and on the lower frame **160**.

A large number of processing circuits **130** corresponding to the sensitive elements **105** are formed in a second wafer by known integration techniques. The pads **155, 156** and an upper frame **165** used (as described below) to define the metal wall **120** are then formed in the manner described above. The invention may, however, also be implemented with the metal wall **120** formed entirely on a single wafer.

In an alternative embodiment of the present invention, the upper frame **165** (or alternatively, the lower frame **160** or both of the frames **160, 165**) is subjected to a growth process in order to increase its thickness (similar remarks apply to the pads **140, 142** and **155, 156** which have to be connected to one another within the hollow hermetic structure **115**). This additional step is useful when the height of the metal wall **120** produced by the process described above (generally 2–3μm) is not sufficient to ensure correct movement of the microstructure of the sensitive element **105**. In particular, a projection (a bump) made, for example of nickel or copper, is grown on the upper frame **165** (and on the pads **155** and **156**). This bump is formed by means of a non-electrolytic (electroless) growth process. In detail, a layer of more noble metal, for example zinc, is deposited and prevents the formation of oxide and hydroxide layers on the aluminium. The wafer is then immersed in an autocatalytic chemical solution in order to grow a layer of nickel; finally, a thin layer (a flash) of gold which protects against oxidation and improves the quality of the welding, is deposited. The process described above is particularly inexpensive and flexible since it is compatible with machining of the wafers in batches and does not require any additional masks. Alternatively, electro-deposition (electroplating), evaporation, or dispensing methods, and the like, are used.

The wafer containing the processing circuitry **130** is then cut to form the various chips **125**. The chips **125** are fixed to the wafer (as yet uncut) containing the sensitive elements **105**. In particular, the upper frame **165** and the pads **155,156** of each chip **125** are fixed to a corresponding lower frame **160** and to the corresponding pads **140, 142**, respectively. For this purpose, a welding process, for example, a thermal compression process, in which the heated parts are joined simply by pressure, or a thermal-ultrasonic process which provides for the simultaneous application of heat and ultrasound, is preferably used. Alternatively, the fixing is achieved by different techniques, for example, with the use of a suitable adhesive.

Upon completion of the operations on the wafer containing the sensitive elements **105** (and the respective checking) this wafer is cut to form the various chips **110**. The sensitive elements **105** are thus protected in the hollow hermetic structure **115** so that they are not damaged during the cutting operation and are not exposed to the danger of "stiction". This enables an extremely high production yield to be achieved.

The production of the sensor is then completed by known and conventional operations. Each chip **110** is fixed to a suitable frame by soldering with an alloy having a low

melting point, for example, lead-tin, or by gluing with a suitable adhesive. The pads **145** are connected to the corresponding electrodes by means of thin metal, for example, gold wires. Typically, the metal wires are soldered to the pads **145** on the one hand and to the inner ends of the electrodes on the other hand with an alloy having a low melting point, by a thermal-ultrasonic method. The sensor unit thus produced can be used directly if it is fitted in a system in a controlled environment, as in hard-disk drivers. Alternatively, the unit may be mounted in a suitable die into which a plastic material, for example, a thermosetting epoxy resin, is injected in a liquid state. After polymerization of the resin, a device comprising an insulating body which incorporates the elements described above and from which the electrodes project for connection to an external circuit is thus produced. The sensor of the present invention may, however, also be used in different devices, for example, ball-grid array (or BGA) devices and the like.

Naturally, in order to satisfy contingent and specific requirements, an expert in the art may apply to the above-described sensor with a movable microstructure many modifications and variations all of which, however, are included within the scope of protection of the invention as defined by the following claims.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

What is claimed is:

1. A sensor with a movable microstructure, comprising a sensitive element formed in a first chip of semiconductor material for producing an electrical signal dependent on a movement of at least one movable microstructure relative to a surface of the first chip, the sensitive element being enclosed in a hollow hermetic structure formed by a second chip of semiconductor material attached to the first chip of semiconductor material over the sensitive element, and a processing circuit for processing said electrical signal formed in the second chip of semiconductor material and in electrical connection with the electrical signal produced by the sensitive element formed in the first chip, the hollow hermetic structure including a metal wall disposed on a surface of the first chip around the sensitive element, the second chip being fixed to said wall.

2. The sensor according to claim **1** wherein the metal wall is comprised substantially of nickel.

3. The sensor according to claim **1**, further comprising at least one first conductive pad formed on the surface of the first chip within the hollow hermetic structure and connected electrically to the sensitive element, each at least one first conductive pad being connected to a second, facing conductive pad formed on a surface of the second chip for transmitting the electrical signal to the processing circuit.

4. The sensor according to claim **3**, further comprising at least one third conductive pad formed on the surface of the first chip within the hollow hermetic structure, each at least one third pad being connected to a fourth, facing conductive pad formed on the surface of the second chip for receiving an electrical signal processed by the processing circuitry.

5. The sensor according to claim **4**, further comprising at least one fifth conductive pad formed on the surface of the first chip outside the hollow hermetic structure, each at least one fifth pad being connected electrically to a corresponding sixth pad for transmitting the processed electrical signal outside of the sensor.

6. The sensor according to claim **1** wherein the sensor comprises an inertial sensor.

7. An electronic device comprising the sensor according to claim **1** and a plastic package in which the sensor is encapsulated.

8. A sensor comprising:

a first chip of semiconductor material;

a sensor element having a movable microstructure, the sensor element supported by the first chip and structured to generate a first signal in response to a movement of the microstructure relative to the first chip;

a second chip of semiconductor material covering the sensor element and configured to receive the first signal, the second chip of semiconductor material comprising a processing circuit formed therein and electrically coupled to the sensor element to receive the first signal, the processing circuit structured to process the first signal and generate a second signal based on the first signal; and

a wall formed on the first chip and surrounding the sensor element and connecting the first chip to the second chip, the wall defining a hermetically scaled chamber between the first chip and the second chip and enclosing the sensor element.

9. The sensor according to claim **8** wherein the wall is comprised of a metal.

10. The sensor according to claim **8** wherein the processing circuit is formed in the second chip.

11. The sensor according to claim **8**, further comprising:

a plurality of conductive pads connected between the first chip and the second chip; and

a low resistance diffusion in the first chip between the sensor element and the pads.

12. The sensor according to claim **11**, further comprising at least one output terminal outside the sealed chamber and coupled to the processing circuit to receive the second signal.

13. The sensor according to claim **8** wherein the sensor element comprises an inertial sensor.

14. The sensor according to claim **8** wherein the sensor element comprises a resonant sensor.

15. The sensor according to claim **8** wherein the sealed chamber encloses a gas at a pressure below atmospheric pressure.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,405,592 B1
DATED : June 18, 2002
INVENTOR(S) : Bruno Murari et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [73], "**STMicrlelectronics S.r.l.**" should read as -- **STMicroelectronics S.r.l.** --.

Column 6,
Line 33, "a hermetically scaled chamber" should read as -- a hermetically sealed chamber --.
Lines 51 and 52, "the sensor clement" should read as -- the sensor element --.

Signed and Sealed this

Twenty-second Day of October, 2002

Attest:

Attesting Officer

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

EXHIBIT D

US006546799B1

(12) **United States Patent**
Vigna et al.

(10) **Patent No.: US 6,546,799 B1**
(45) **Date of Patent: *Apr. 15, 2003**

(54) **METHOD FOR COMPENSATING THE POSITION OFFSET OF A CAPACITIVE INERTIAL SENSOR, AND CAPACITIVE INERTIAL SENSOR**

(75) Inventors: **Benedetto Vigna**, Pietrapertosa (IT); **Alberto Gola**, Montu' Beccaria (IT); **Sarah Zerbini**, Fontanellato (IT); **Dario Cini**, deceased, late of Cornaredo (IT), by Carlo Cini, executor

(73) Assignee: **STMicroelectronics S.r.l.**, Agrate Brianza (IT)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/658,294**

(22) Filed: **Sep. 8, 2000**

(30) **Foreign Application Priority Data**

Sep. 10, 1999 (EP) 99830568

(51) **Int. Cl.**[7] **G01P 15/00**
(52) **U.S. Cl.** **73/514.01**; 73/504.12
(58) **Field of Search** 73/504.14, 504.02, 73/504.03, 504.04, 504.08, 504.09, 504.12, 504.13, 514.32, 514.01, 514.02, 1.37, 1.38

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,025,346 A	6/1991	Tang et al.	.....	361/283
5,565,625 A	10/1996	Howe et al.	.....	73/514.16
5,618,989 A	4/1997	Marek	.....	73/1.38
5,650,568 A *	7/1997	Greiff et al.	.....	73/504.09
5,869,760 A *	2/1999	Geen	.....	73/504.12
5,911,157 A	6/1999	Biebl	.....	73/514.16
6,257,062 B1 *	7/2001	Rich	.....	73/514.32
6,370,954 B1 *	4/2002	Zerbini et al.	.....	73/514.01

FOREIGN PATENT DOCUMENTS

WO	86/00416	1/1986
WO	97/45699	12/1997

OTHER PUBLICATIONS

Kuehnel, Wolfgang, Modelling of the mechanical behavior of a differential capacitor acceleration sensor, Sensors and Actuators A 48 (1995). Nov. 29, 1994: pp. 101–108.

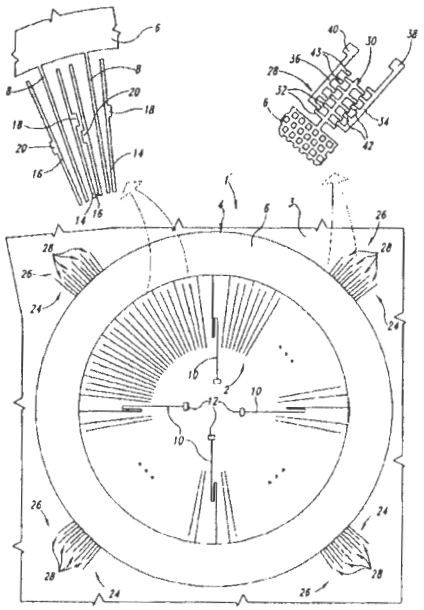
* cited by examiner

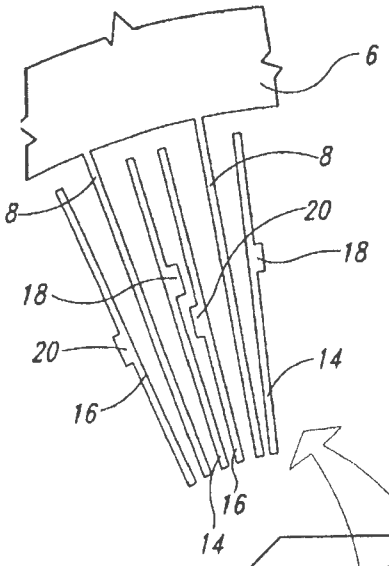
Primary Examiner—Helen Kwok
(74) *Attorney, Agent, or Firm*—Lisa K. Jorgenson; E. Russell Tarleton; Seed IP Law Group PLLC

(57) **ABSTRACT**

An inertial sensor having a stator and a rotor made of semiconductor material and electrostatically coupled together, and a microactuator also made of semiconductor material, coupled to the rotor and controlled so as to move the rotor itself and thus compensate for the position offset thereof.

25 Claims, 3 Drawing Sheets





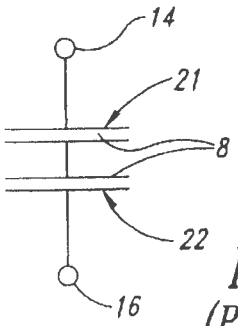


FIG. 2
(Prior Art)

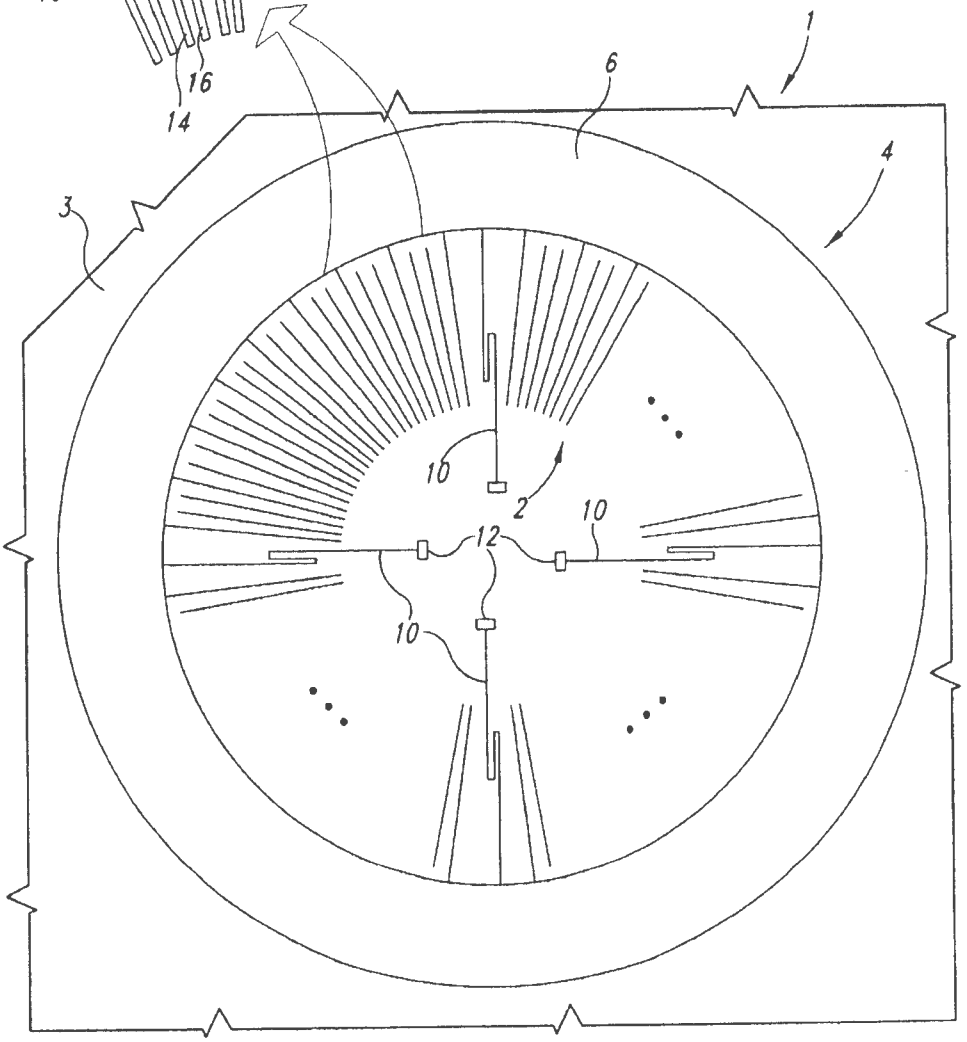


FIG. 1 (Prior Art)

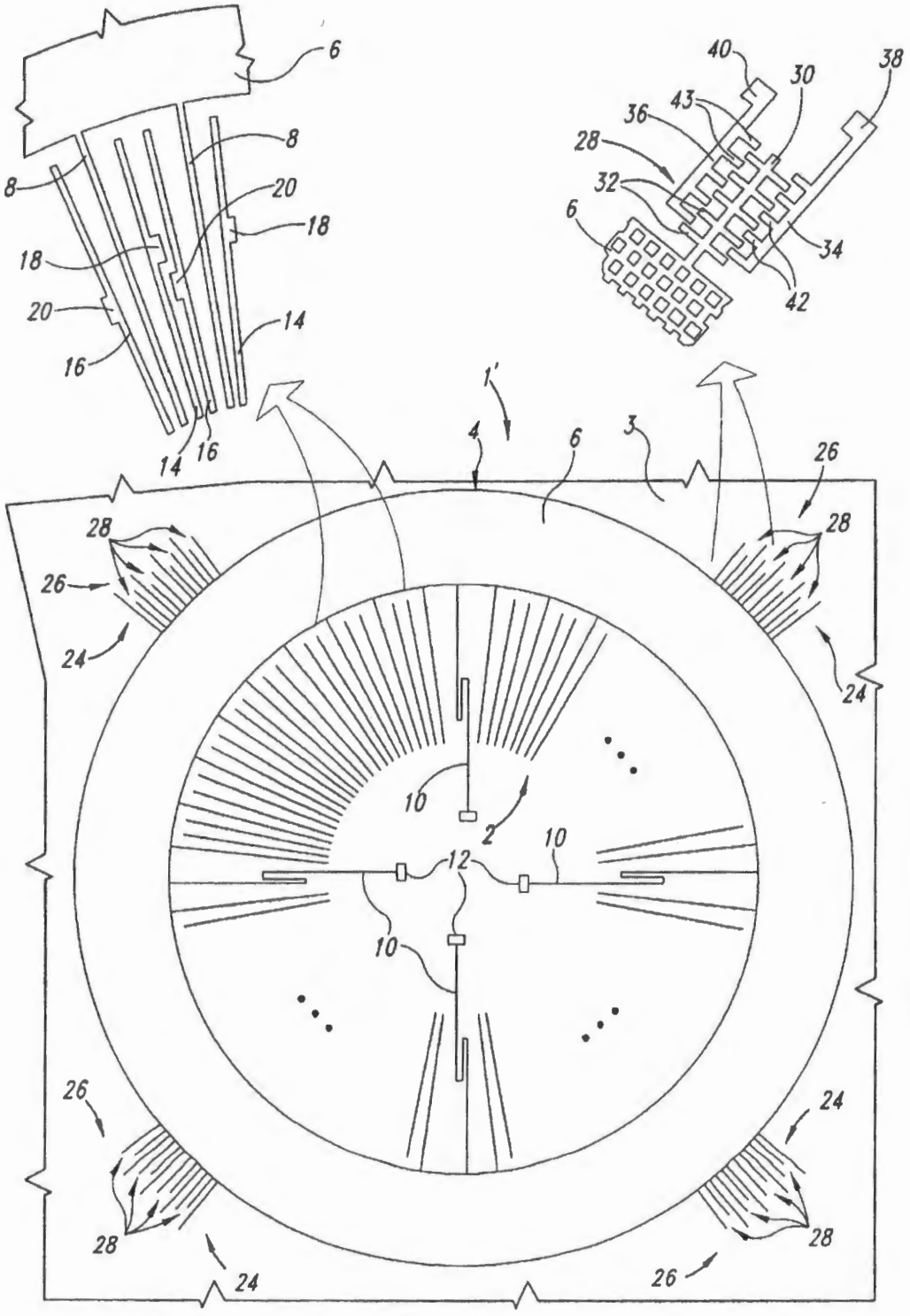

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FIG. 3

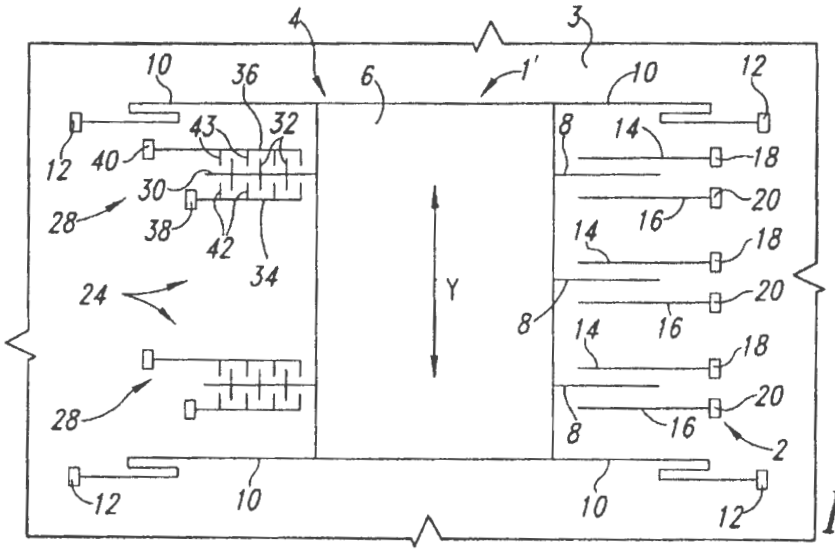
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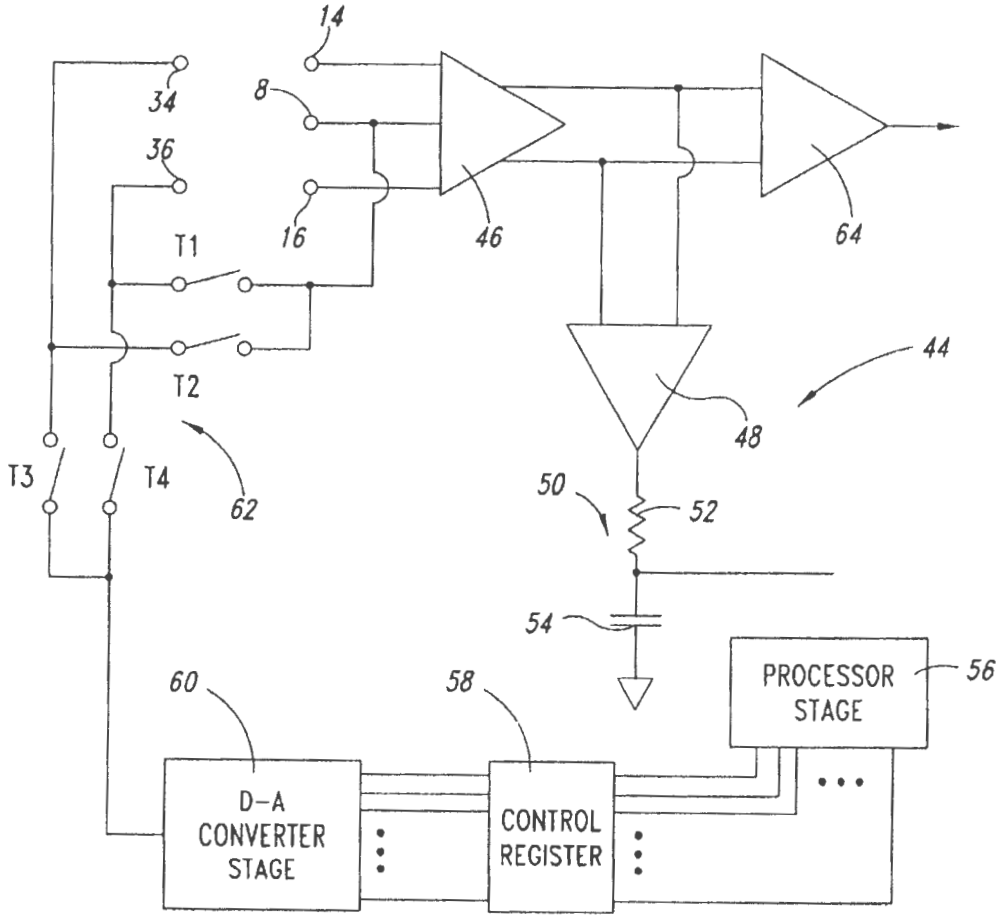
FIG. 5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60
58
D-A CONVERTER STAGE
CONTROL REGISTER

FIG. 4

METHOD FOR COMPENSATING THE POSITION OFFSET OF A CAPACITIVE INERTIAL SENSOR, AND CAPACITIVE INERTIAL SENSOR

TECHNICAL FIELD

The present invention regards a method for compensating the position offset of a capacitive inertial sensor, and a capacitive inertial sensor.

BACKGROUND OF THE INVENTION

As is known, owing to their reduced size, excellent technical characteristics, high reliability, and low cost, integrated capacitive inertial sensors manufactured using the micromachining technique are progressively laying claim to market segments up to now occupied by conventional inertial sensors. One of the main applications of the above inertial sensors is in the field of airbag systems for motor vehicles as a means for measuring the deceleration to which a motor vehicle is subjected upon impact.

To provide an example, FIG. **1** presents the structure of an integrated rotary inertial sensor of a known type.

The inertial sensor, indicated as a whole by **1**, is made of semiconductor material, has a circular structure, and comprises an inner stator **2**, which is integral with the die **3** in which the inertial sensor **1** is formed, and an outer rotor **4**, which is electrostatically coupled to the stator **2**.

The rotor **4** comprises a suspended mass **6** having an annular shape, a plurality of mobile arms **8**, extending radially towards the stator **2** from the suspended mass **6**, identical to each other and angularly equispaced, and elastic-suspension and anchorage elements **10** (represented schematically as springs) elastically connecting the suspended mass **6** to fixed anchoring and biasing regions **12**, through which the suspended mass **6** and the mobile arms **8** are biased (typically at a potential of 1.5 V).

The stator **2** comprises a plurality of pairs of fixed arms **14**, **16**, one for each mobile arm **8** of the rotor **4**, which extend radially with respect to the suspended mass **6** towards the suspended mass **6**. They are arranged in such a way that between each pair of fixed arms **14**, **16**, a corresponding mobile arm **14** of the rotor **4** is arranged and are connected to respective fixed anchoring and biasing regions **18**, **20**, through which the fixed arms **14**, **16** are biased (typically at a potential ranging between 1.5 and 2.2 V).

The fixed arms **14**, **16** are connected, via the fixed anchoring and biasing regions **18**, **20**, to a measuring circuit having the purpose of measuring the acceleration or deceleration to which the inertial sensor **1** is subjected.

In particular, the inertial sensor **1** can be electrically modeled as shown in FIG. **2**, i.e., by means of two capacitive elements **21**, **22** connected in series, wherein the two outer plates are defined by the fixed arms **14** and **16**, respectively, of the stator **2**, and the two inner plates are defined by the mobile arms **8** of the rotor **4**, which although they are illustrated as being separate, in fact constitute a single plate.

The rotational motion of the rotor **4** determines a modulation in phase opposition of the capacitances of the capacitive elements **21**, **22**, which should assume, in the absence of acceleration or deceleration applied to the inertial sensor **1**, equal values. Consequently, by measuring these capacitances, it is possible to detect the unknown inertial quantity, i.e., the acceleration or deceleration to which the inertial sensor **1** is subjected.

It is also known, however, that, on account of the imperfect configuration of the elastic-suspension and anchoring elements **10** and on account of the residual mechanical stress of the material of which the inertial sensor **1** is made, the rotor **4** is generally affected by a position offset; i.e., the effective zero position of the rotor **4** does not coincide with the nominal zero position envisaged in the design phase.

The position offset consequently gives rise to a corresponding capacitive offset, defined as the difference between the capacitances of the capacitive elements **21**, **22** in the absence of acceleration or deceleration, which has an adverse effect on the overall performance of the system comprising the inertial sensor **1** and the corresponding driving and measuring circuitry.

A known technique used for compensating the aforesaid capacitive offset involves the use, within the measuring circuit, of regulatable compensation capacitors, which are connected in parallel to the capacitive elements **21**, **22** and have the purpose of compensating the differences which, in the absence of acceleration or deceleration, the capacitances of the said capacitive elements **21**, **22** present as compared to the nominal values which they ought to assume in the absence of position offset. In this way, then, even in the presence of a capacitive offset, the equivalent capacitances measured by the measuring circuit in static conditions, i.e., in the absence of acceleration or deceleration, again assume the same value.

This technique presents, however, the drawback of compensating the capacitive offset only under static conditions, i.e., in the absence of acceleration or deceleration applied to the inertial sensor, but not under dynamic conditions, i.e., in the presence of acceleration or deceleration applied to the inertial sensor, and this is typically a cause of errors in the measurement of the unknown inertial quantity.

In fact, after the compensation performed as described above, the rotor **4** continues in any case to assume a zero position that is not the nominal one, and because of the position offset the application of an acceleration or deceleration to the inertial sensor **1** does not bring about any modulation in phase opposition of the capacitances of the capacitive elements **21**, **22** that occurs in the absence of position offset, but causes asymmetrical variations of these capacitances which depend both on the direction of rotation of the rotor **4** and on the amount of the position offset; these variations consequently lead to measuring errors.

SUMMARY OF THE INVENTION

The present invention provides a method for compensating the offset and a capacitive inertial sensor that is free from the drawbacks of the known art.

According to the disclosed embodiments of the present invention, the inertial sensor is made of semiconductor material and comprises a stator element and a rotor element electrostatically coupled together and an actuator made of semiconductor material coupled to the rotor element and controlled to compensate the position offset of the rotor element with respect to the stator element.

In accordance with another aspect of the present invention, an inertial sensor is provided that includes a sensor element having a stator and a rotor, and an actuator formed on the sensor element, the actuator comprising a fixed arm connected to one of the stator and the rotor and a mobile arm connected to the other of the stator and the rotor, the actuator configured to adjust the positions of the stator and the rotor relative to one another in response to a driving signal.

In accordance with another aspect of this embodiment of the invention, a driver circuit is provided that is coupled to the sensor element and the actuator and configured to determine a position offset of the stator and rotor relative to one another and to generate the driving signal in response thereto.

In accordance with yet another embodiment of the present invention, a method for compensating the position offset of an inertial sensor made of semiconductor material and having a stator element and a rotor element electrostatically coupled together is provided. The method includes moving the rotor element relative to the stator element to compensate for the position offset thereof.

In accordance with another aspect of the method of the present invention, the moving of the rotor includes driving at least one actuator element made of semiconductor material coupled to the rotor element. More particularly, driving includes applying a potential difference between a mobile arm and a fixed arm in the actuator element.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, two preferred embodiments thereof are now described, merely to provide non-limiting examples, with reference to the attached drawings, in which:

FIG. **1** is a schematic representation of the structure of a known rotary capacitive inertial sensor;

FIG. **2** presents an equivalent electrical diagram of the inertial sensor of FIG. **1**;

FIG. **3** is a schematic representation of the structure of a rotary capacitive inertial sensor according to the present invention;

FIG. **4** is a schematic representation of a control circuit for the inertial sensor of FIG. **3**; and

FIG. **5** is a schematic representation of the structure of a linear capacitive inertial sensor according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. **3** an inertial sensor according to the present invention is designated, as a whole, by **1'**, wherein the parts that are identical to those of the capacitive inertial sensor **1** of FIG. **1** are designated by the same reference numbers.

The inertial sensor **1'** has a structure similar to that of the inertial sensor **1** and differs from the latter in that it further comprises an integrated microactuator **24** made of semiconductor material, coupled to the rotor **4** and having the purpose of rotating the rotor **4** by an amount equal to the position offset to bring it back into the nominal zero position.

In particular, the microactuator **24** comprises four distinct actuator groups **26**, each of which is arranged in a respective quadrant of the inertial sensor **1'** and is formed of a plurality of actuator elements **28**, numbering four in the example illustrated in FIG. **3**, identical to one another and angularly equispaced.

In detail, each actuator element **28** comprises a mobile arm **30** integral with the suspended mass **6** of the rotor **4** (and consequently biased at the same potential as that of the suspended mass **6**), extending radially outwards from the suspended mass **6**, and carrying a plurality of mobile electrodes **32** extending from either side of the respective mobile arm **30** in a substantially circumferential direction and arranged parallel to one another and equispaced along the respective mobile arms **30**.

Each actuator element **28** further comprises a pair of fixed arms **34, 36** extending radially with respect to the suspended mass **6**, arranged on opposite sides of, and facing, the respective mobile arm **30**, connected to respective fixed anchoring and biasing regions **38, 40**, through which the fixed arms **34, 36** are biased (typically at a potential ranging between 1.5 and 5 V). Each of the fixed arms **34, 36** carries a plurality of fixed electrodes **42, 43** extending in a substantially circumferential direction towards the respective mobile arm **30** and interleaved, or "comb-finger" shaped, with the mobile electrodes **32** of the respective mobile arm **30**.

In addition, the actuator elements **28** are defined on the wafer together with the suspended mass **6** of the rotor **4**, and consequently do not require additional fabrication phases other than those already envisaged for the fabrication of the inertial sensor **1'**.

The fixed arms **34, 36** of the actuator elements **28** are connected, through the fixed anchoring and biasing regions **38, 40**, to a driving circuit **44**—shown in FIG. **4** and described in detail in what follows—having the purpose of applying a biasing voltage to either one or the other of the two fixed arms **34, 36** of each actuator element **28** in such a way that the potential difference between the fixed arm **34, 36** thus biased and the corresponding mobile arm **30** causes a rotation of the rotor **4** in one direction or the other, sufficient for bringing the rotor **4** back into the nominal zero position.

In particular, as a result of the electrostatic coupling existing between each mobile arm **30** and the corresponding fixed arms **34, 36**, the rotor **4** is subjected to a transverse force proportional to the number of pairs of fixed arms and mobile arms **30, 34, 36**. This force tends to move the mobile arm **30** away from the fixed arm **34, 36**, with respect to which the mobile arm **30** has a smaller potential difference, and to bring the mobile arm **30** closer to the fixed arm **34, 36**, with respect to which the mobile arm **30** has a greater potential difference, thus causing rotation of the suspended mass **6**.

Owing to the presence of the comb-finger shaped electrodes **32, 42, 43**, the force necessary to bring the rotor **4** back from the effective zero position to the nominal zero position is altogether independent of the amount of offset with respect to the nominal zero position itself.

In addition, the microactuator **24** does not interfere with the operation of the inertial sensor **1'** in that the phenomenon known as "electrostatic softening" is not present; i.e., the microactuator **24** does not modify the mechanical rigidity of the system. Furthermore, there is no interference between the capacitances defined by the fixed arms **34, 36** and corresponding mobile arms **30** of the actuator element **28** and the capacitances defined by the fixed arms **14, 16** and corresponding mobile arms **8** of the stator **2** and rotor **4**.

FIG. **4** is a schematic representation of the circuit structure of the driving circuit **44** for the actuator elements **28**.

The driving circuit **44** comprises a differential preamplifier stage **46** having a first input connected to the fixed arms **14** of the stator **2**, a second input connected to the fixed arms **16** of the stator **2**, a third input connected to mobile the arms **8** of the rotor **4**, and a first and a second output providing a first and, respectively, a second signal indicating the values of the capacitances of the capacitive elements **21, 22**, respectively, previously referred to and defined by the fixed arms **14, 16** with respect to the mobile arms **8**; an amplifier

stage **48** having a first and a second input connected to the outputs of the preamplifier stage **46**, and an output providing a third signal indicating the unbalancing, i.e., the difference, between the aforesaid capacitances; and a first-order low-pass filtering network **50** formed of a resistor **52** and a capacitor **54** connected in series, and having an output node (node intermediate between the resistor **52** and the capacitor **54**) on which there is present a fourth signal having a value equal to the mean value of the third signal, and thus having an amplitude proportional to the position offset.

The driving circuit **44** further comprises a processing stage **56** having an input connected to the output of the filtering network **50** and providing, on an output, an nbit digital correction word, for example with n=6, indicating the compensation potential to be applied to the fixed arms **34, 36** of the actuator elements **28** to compensate the position offset of the rotor **4**. This word is stored in a control register **58** connected to the output of the processing stage **56**.

In particular, the correction word is generated by implementing a simple algorithm which calculates the difference between the amplitude of the fourth signal, proportional to the position offset of the rotor **4**, and a reference amplitude indicating the amplitude that the fourth signal would assume in the absence of position offset and converts the difference thus obtained into the digital correction word.

In addition, the processing stage **56** could alternatively be a stage external to the driving circuit and could form part of the machine performing the testing operation on the inertial sensor **1'**, and in this case the compensation of the position offset would be made only once during the testing phase, or it could be a stage internal to the driving circuit **44**, and in this case the compensation of the position offset could be made continuously; in this latter way, also possible drifts of the position offset over time could be compensated.

The driving circuit **44** further comprises a digital-to-analog converter stage **60** having n inputs connected to the outputs of the control register **58** and an output supplying the compensation potential to be applied to the fixed arms **34, 36** of the actuator elements **28**; and a connection stage **62** arranged between the output of the digital-toanalog converter stage **60** and the fixed arms **34, 36** of the actuator elements **28** and having the purpose of selectively connecting the fixed arms **34, 36** that are to be biased to the output of the digital-to-analog converter **60**.

In particular, FIG. **4** shows only one part of the connection stage **62** for just one actuator element **28** and, as illustrated, for each pair of fixed arms **34, 36** to be biased, the connection stage **62** comprises two pairs of controlled switches T1, T2, T3, T4, made, for example, using MOS transistors.

In particular, the switches T3 and T4 are connected between the output of the digital-to-analog converter stage **60** and the corresponding fixed arms **34, 36**, and are controlled in phase opposition so as to connect the output of the digital-to-analog converter stage **60** to only one of the two fixed arms **34, 36**, whilst the switches T1 and T2 are connected between the third terminal of the preamplifier stage **46** and the fixed arms **34, 36** and are also controlled in phase opposition so as to bias the fixed arm **34, 36** that is not connected to the output of the digital-to-analog converter stage **60** at the same potential at which the mobile arms **14, 16** of the rotor **4** are biased.

Furthermore, connected to the outputs of the preamplifier stage **46** are a first and a second input of a preprocessing stage **64** having the purpose of processing, under normal operating conditions, the first and the second signal provided by the preamplifier stage **46**, in a way which is known and hence not described in detail, so as to supply information on the acceleration or deceleration to which the inertial sensor **1'** is subjected.

The advantages of the inertial sensor **1'** according to the present invention are evident from the above description.

In particular, it is emphasized that the construction of the microactuator **24** dedicated to effecting the movement of the rotor **4** to bring it back into the nominal zero position does not involve additional phases in the process of fabrication of the inertial sensor **1'** and does not interfere in any way with the operation of the said inertial sensor **1'**.

Finally, it is clear that modifications and variations may be made to the inertial sensor **1'** described and illustrated herein, without thereby departing from the scope of protection of the present invention.

For example, the number of actuator groups **26** and the number of actuator elements **28** in each actuator group **26** could be different from what has been described. In particular, even a single actuator element **28** connected to the suspended mass **6** could be envisaged, or else four actuator elements **28**, each arranged in its respective quadrant, or two actuator elements **28** arranged on diametrically opposite sides of the suspended mass **6**, or two actuator groups **26** arranged on diametrically opposite sides of the suspended mass **6**.

In addition, the inertial sensor **1'** could be of the linear type, as represented in FIG. **5**, in which the various parts of the inertial sensor are designated by the same reference numbers as those used in FIG. **3**. In this case, the microactuator **24** is driven in such a way as to impress on the mobile mass **6** a translational motion with respect to the stator along a direction Y, and the mobile and fixed electrodes **32, 42, 43** are parallel to the direction Y.

Although representative embodiments of the invention have been illustrated and described, it is to be understood that various changes may be made therein without departing from the spirit and scope of the invention. Thus, the invention is to be limited only by the claims that follow and the equivalents thereof.

What is claimed is:

1. An inertial sensor made of semiconductor material, comprising a stator element and a rotor element electrostatically coupled together; and an actuator made of semiconductor material, coupled to said rotor element and controlled so as to compensate a position offset of the rotor element.

2. The inertial sensor of claim **1**, wherein said actuator means comprise at least an actuator element comprising a first mobile arm extending from said rotor element and at least a first fixed arm facing said first mobile arm.

3. The inertial sensor of claim **2**, wherein said first mobile arm is provided with a plurality of mobile electrodes extending transversely with respect to the first mobile arm towards said first fixed arm; and wherein said first fixed arm is provided with a plurality of fixed electrodes extending transversely with respect to said first fixed arm towards said first mobile arm.

4. The inertial sensor of claim **3**, wherein said mobile electrodes are arranged parallel to one another along said first mobile arm and in that said fixed electrodes are arranged parallel to one another along said first fixed arm and are interleaved with said mobile electrodes.

5. The inertial sensor of claim **2**, wherein said actuator element comprises a pair of said first fixed arms arranged on opposite sides of said first mobile arm.

6. The inertial sensor of claim **2**, wherein said actuator comprises a plurality of actuator elements.

7. The inertial sensor of claim 6, wherein said rotor element has a circular structure and said actuator comprises at least one pair of said actuator elements arranged on diametrically opposite sides of said rotor element.

8. The inertial sensor of claim 7, wherein said actuator comprise two actuator groups, each actuator group formed of at least two said actuator elements and arranged on diametrically opposite sides of said rotor element.

9. The inertial sensor of claim 6, wherein said rotor element has a circular structure and said actuator comprises four said actuator elements, each actuator element arranged in a respective quadrant of said rotor element.

10. The inertial sensor of claim 9, wherein said actuator comprises four actuator groups, each actuator group formed of at least two said actuator elements and each actuator group arranged in a respective quadrant of said rotor element.

11. The inertial sensor of claim 2, wherein said rotor element comprises a suspended mass and a plurality of second mobile arms extending from said suspended mass, and said stator element comprises a plurality of second fixed arms, each facing a respective said second mobile arm.

12. The inertial sensor of claim 11, wherein said stator element further comprises a plurality of third fixed arms, each facing a respective said second mobile arm, each second mobile arm being arranged between a respective second fixed arm and a respective third fixed arm.

13. A method for compensating the position offset of an inertial sensor made of semiconductor material and having a stator element and a rotor element electrostatically coupled together; comprising moving said rotor element to compensate for a positon offset thereof.

14. The method of claim 13, wherein said moving comprises driving at least one actuator element, made of semiconductor material, coupled to said rotor element.

15. The method of claim 14, the actuator element having a mobile arm extending from said rotor element and at least one fixed arm facing said mobile arm, wherein said driving comprisies applying a potential difference between said mobile arm and said fixed arm.

16. The method of claim 15, wherein said applying a potential difference comprises generating an unbalancing signal correlated to the position offset of said rotor element and generating said potential difference as a function of said unbalancing signal.

17. The method of claim 16, wherein said generating said potential difference comprises calculating a difference between said unbalancing signal and a reference signal and generating said potential difference as a function of said calculated difference.

18. The method of claim 17, wherein said generating said potential difference comprises generating a digital correction word as a function of said difference between said unbalancing signal and said reference signal, and carrying out a digital-to-analog conversion of said digital correction word.

19. An inertial sensor, comprising:

a sensor element, comprising:

a stator;

a rotor; and

an actuator formed on the sensor element, the actuator comprising a fixed arm connected to one of the stator and the rotor and a mobile arm connected to the other of the stator and the rotor, the actuator configured to adjust positions of the stator and the rotor relative to one another in response to a driving signal.

20. The sensor of claim 19, further comprising a driver circuit coupled to the sensor element and the actuator and configured to determine a position offset of the stator and the rotor relative to one another and to generate the driving signal in response thereto.

21. The sensor of claim 20, wherein the stator and the rotor are configured to form a capacitive element that generate a first capacitive signal and a second capacitive signal, and wherein the driver circuit is coupled to the capacitive element and is configured to receive the first capacitive signal and the second capacitive signal and to generate a difference signal, the driver circuit further configured to compare the different signal to a reference signal and to generate the driving signal in response thereto.

22. The sensor of claim 20, wherein the stator and the rotor are configured to form a capacitive element that generate a first capacitive signal and a second capacitive signal, and wherein the driver circuit comprises a first amplifier stage coupled to the capacitive element and configured to receive the first and second capacitive signals and to generate first and second capacitive value signals; a second amplifier stage coupled to the first amplifier stage and configured to receive the first and second capacitive value signals and to generate a difference signal in response thereto.

23. The sensor of claim 22, wherein the driver circuit further comprises a processing stage coupled to the second amplifier and configured to receive the difference signal and to compare the difference signal to a reference signal and to generate a driver signal in response thereto.

24. The sensor of claim 23, wherein the driver circuit further comprises a filter network coupled between the second amplifier stage and the processing stage, the filter network configured to receive the difference signal from the second amplifier stage and to output a modified difference signal having a value equal to a mean value of the difference signal.

25. The sensor of claim 20, further comprising a connection stage coupled to the actuator and to the driver circuit, the connection stage configured to reactive the driving signal and to selectively couple the driving signal to the actuator in response to the driving signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,546,799 B1
DATED : April 15, 2003
INVENTOR(S) : Benedetto Vigna et al.

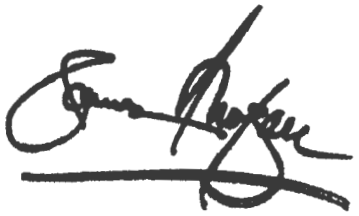
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6,
Lines 47 and 48, "said actuator means comprise at least" should read as -- said actuator comprise at least --.

Column 8,
Line 52, "to reactive the driving signal" should read as -- to receive the driving signal --.

Signed and Sealed this

Nineteenth Day of August, 2003



JAMES E. ROGAN
Director of the United States Patent and Trademark Office