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Attorneys for Plaintiff
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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

PANAVISION IMAGING, LLC, Plaintiff, v. OMNIVISION TECHNOLOGIES, INC., CANON U.S.A., INC., MICRON TECHNOLOGY, INC., AND APTINA IMAGING CORPORATION, Defendants.	Case No. CV09-1577 SJO (CTx) **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

TO THE HONORABLE JUDGE OF SAID COURT:

Plaintiff Panavision Imaging, LLC ("Panavision") for its Complaint against Defendants, Omnivision Technologies, Inc. ("Omnivision"), Canon U.S.A., Inc. ("Canon"), Micron Technology, Inc. ("Micron"), and Aptina Imaging Corporation ("Aptina"), alleges:

SUBJECT MATTER JURISDICTION

1. This is an action arising under the patent laws of the United States. Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

THE PARTIES

2. Plaintiff Panavision is a limited liability company duly organized and existing under the laws of Delaware, having a place of business at 6219 De Soto Ave., Woodland Hills, CA 91367.

3. Defendant Omnivision is a corporation duly organized and existing under the laws of Delaware, having a principal place of business at 4275 Burton Drive, Santa Clara, CA 95054. Omnivision's agent for service of process, registered with the California Secretary of State, is Xiao-Ying Shaw Hong, at 1341 Orleans Drive, Sunnyvale, CA 94089.

4. Defendant Canon is a corporation duly organized and existing under the laws of New York, having a principal place of business at One Canon Plaza, Lake Success, NY 11042. Canon's agent for service of process, registered with the California

Secretary of State, is CT Corporation System, at 818 West Seventh Street, Los Angeles, CA 90017.

5. Defendant Micron is a corporation duly organized and existing under the laws of Delaware, having a principal place of business at 8000 South Federal Way, Boise, ID 83716. Micron's agent for service of process, registered with the California Secretary of State, is CSC Lawyers Incorporating Service, at 2730 Gateway Oaks Drive, Suite 100, Sacramento, CA 95833.

6. Defendant Aptina is a subsidiary of Defendant Micron and is a corporation duly organized and existing under the laws of Delaware, having a principal place of business at 3080 North 1st Street, San Jose, CA 95134. Aptina's agent for service of process, registered with the California Secretary of State, is CSC Lawyers Incorporating Service, at 2730 Gateway Oaks Drive, Suite 100, Sacramento, CA 95833.

PERSONAL JURISDICTION

7. This Court has personal jurisdiction over Defendants in that Omnivision, Canon, Micron, and Aptina (hereinafter "Defendants") have established sufficient minimum contacts with the forum. Each Defendant manufactures and/or assembles electronic products that are and have been used, offered for sale, sold, and/or purchased in California, including in this Judicial District. Each Defendant, directly and/or through its distribution network, places its image sensors within the stream of commerce, which stream is directed at this Judicial District. Jurisdiction over the Defendants in this matter is also proper inasmuch as they have voluntarily submitted

themselves to the jurisdiction of the courts of this State by registering agents for service of process with the California Secretary of State. Therefore, the exercise of jurisdiction over said Defendants would not offend traditional notions of fair play and substantial justice.

VENUE

8. Each of the Defendants do business in this district, including providing electronic products that are used, offered for sale, sold, and/or have been purchased in California and in this district. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), (c), and 1400(b).

FACTUAL ALLEGATIONS

9. United States Patent No. 6,818,877 ("the '877 patent"), entitled *Pre-charging a Wide Analog Bus for CMOS Image Sensors*, was duly and lawfully issued November 16, 2004. Panavision is the current owner of all rights, title, and interest in the '877 patent and has the right to sue for past damages. A true and correct copy of the '877 patent is attached hereto as Exhibit A.

10. United States Patent No. 6,633,029 ("the '029 patent"), entitled *Video Bus for High Speed Multi-resolution Imagers and Method Thereof*, was duly and lawfully issued October 14, 2003. Panavision is the current owner of all rights, title, and interest in the '029 patent and has the right to sue for past damages. A true and correct copy of the '029 patent is attached hereto as Exhibit B.

11. United States Patent No. 6,590,198 ("the '198 patent"), entitled *Video Bus*

for High Speed Multi-resolution Imagers, was duly and lawfully issued July 8, 2003. Panavision is the current owner of all rights, title, and interest in the '198 patent and has the right to sue for past damages. A true and correct copy of the '198 patent is attached hereto as Exhibit C.

12. United States Patent No. 7,057,150 ("the '150 patent"), entitled *Solid State Imager with Reduced Number of Transistors per Pixel*, was duly and lawfully issued June 6, 2006. Panavision is the current owner of all rights, title, and interest in the '150 patent and has the right to sue for past damages. A true and correct copy of the '150 patent is attached hereto as Exhibit D.

FIRST COUNT

(Infringement of the '877 patent)

13. Panavision incorporates by reference the allegations set forth in Paragraphs 1-12 of this Complaint as though fully set forth herein.

14. Each of the Defendants has infringed and is infringing the '877 patent by making, using, importing, offering for sale and/or selling in the United States, without authority, products—including image sensors—that embody the inventions patented within the '877 patent, and, on information and belief, by actively inducing and/or contributing to infringement of said patent by others.

15. Upon information and belief, Defendants will continue to directly infringe, induce infringement and/or contribute to the infringement of the '877 patent unless enjoined by this Court.

16. Upon information and belief, Defendants' infringement of the '877 patent is willful, entitling Panavision to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

17. Defendants' acts of infringement have caused damage to Panavision and Panavision is entitled to recover from Defendants the damages sustained by Panavision as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' acts of infringement will continue to damage Panavision, causing irreparable harm, for which there is no adequate remedy at law, unless enjoined by this Court.

SECOND COUNT

(Infringement of the '029 patent)

18. Panavision incorporates by reference the allegations set forth in Paragraphs 1-17 of this Complaint as though fully set forth herein.

19. Defendants Canon and Omnivision have infringed and are infringing the '029 patent by making, using, importing, offering for sale and/or selling in the United States, without authority, products—including image sensors—that embody the inventions patented within the '029 patent, and, on information and belief, by actively inducing and/or contributing to infringement of said patent by others.

20. Upon information and belief, Canon and Omnivision will continue to directly infringe, induce infringement and/or contribute to the infringement of the '029 patent unless enjoined by this Court.

21. Upon information and belief, Canon's and Omnivision's infringement of the '029 patent is willful, entitling Panavision to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

22. Canon's and Omnivision's acts of infringement have caused damage to Panavision and Panavision is entitled to recover from Canon and Omnivision the damages sustained by Panavision as a result of Canon's and Omnivision's wrongful acts in an amount subject to proof at trial. Canon's and Omnivision's acts of infringement will continue to damage Panavision, causing irreparable harm, for which there is no adequate remedy at law, unless enjoined by this Court.

THIRD COUNT

(Infringement of the '198 patent)

23. Panavision incorporates by reference the allegations set forth in Paragraphs 1-22 of this Complaint as though fully set forth herein.

24. Defendants Micron and Aptina have infringed and are infringing the '198 patent by making, using, importing, offering for sale and/or selling in the United States, without authority, products—including image sensors—that embody the inventions patented within the '198 patent, and, on information and belief, by actively inducing and/or contributing to infringement of said patent by others.

25. Upon information and belief, Micron and Aptina will continue to directly infringe, induce infringement and/or contribute to the infringement of the '198 patent

unless enjoined by this Court.

26. Upon information and belief, Micron's and Aptina's infringement of the '198 patent is willful, entitling Panavision to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

27. Micron's and Aptina's acts of infringement have caused damage to Panavision and Panavision is entitled to recover from Micron and Aptina the damages sustained by Panavision as a result of Micron's and Aptina's wrongful acts in an amount subject to proof at trial. Micron's and Aptina's acts of infringement will continue to damage Panavision, causing irreparable harm, for which there is no adequate remedy at law, unless enjoined by this Court.

FOURTH COUNT

(Infringement of the '150 patent)

28. Panavision incorporates by reference the allegations set forth in Paragraphs 1-27 of this Complaint as though fully set forth herein.

29. Defendants Canon and Omnivision have infringed and are infringing the '150 patent by making, using, importing, offering for sale and/or selling in the United States, without authority, products—including image sensors—that embody the inventions patented within the '150 patent, and, on information and belief, by actively inducing and/or contributing to infringement of said patent by others.

30. Upon information and belief, Canon and Omnivision will continue to

directly infringe, induce infringement and/or contribute to the infringement of the '150 patent unless enjoined by this Court.

31. Upon information and belief, Canon's and Omnivision's infringement of the '150 patent is willful, entitling Panavision to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

32. Canon's and Omnivision's acts of infringement have caused damage to Panavision and Panavision is entitled to recover from Canon and Omnivision the damages sustained by Panavision as a result of Canon's and Omnivision's wrongful acts in an amount subject to proof at trial. Canon's and Omnivision's acts of infringement will continue to damage Panavision, causing irreparable harm, for which there is no adequate remedy at law, unless enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Panavision prays for judgment and seeks relief against Defendants as follows:

(a) For judgment that the '877 patent has been and/or continues to be infringed by each of the Defendants;

(b) For judgment that the '029 patent has been and/or continues to be infringed by Canon and Omnivision;

(c) For judgment that the '198 patent has been and/or continues to be infringed by Micron and Aptina;

(d) For judgment that the '150 patent has been and/or continues to be infringed by Canon and Omnivision;

(e) For an accounting of all damages sustained by Panavision as the result of Defendants' acts of infringement;

(f) For preliminary and permanent injunctions enjoining the aforesaid acts of infringement by Defendants, their officers, agents, servants, employees, subsidiaries, successors, assigns, and all other persons acting in concert or participation with any of the Defendants, including related individuals and entities, customers, representatives, dealers, distributors, and importers;

(g) For actual damages together with prejudgment interest;

(h) For enhanced damages pursuant to 35 U.S.C. § 284;

(i) For an award of attorneys' fees pursuant to 35 U.S.C. § 285 or as otherwise permitted by law;

(j) For all costs of suit; and

(k) For such other and further relief as the Court may deem just and proper.

DATED: March 6, 2009

HOWREY LLP

By: _____
Don F. Livornese

Attorney for Plaintiff
PANAVISION IMAGING, LLC

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure and Local Rule 38-1, Plaintiff Panavision demands a trial by jury of this action.

DATED: March 6, 2009

HOWREY LLP

By: _____
Don F. Livornese

Attorney for Plaintiff
PANAVISION IMAGING, LLC

EXHIBIT A

US006818877B2

(12) **United States Patent**
Boemler

(10) **Patent No.: US 6,818,877 B2**
(45) **Date of Patent: Nov. 16, 2004**

(54) **PRE-CHARGING A WIDE ANALOG BUS FOR CMOS IMAGE SENSORS**

(75) Inventor: **Christian Boemler**, Cortland, NY (US)

(73) Assignee: **Silicon Video, Inc.**, Ithaca, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.

(21) Appl. No.: **10/151,220**

(22) Filed: **May 17, 2002**

(65) **Prior Publication Data**

US 2002/0171034 A1 Nov. 21, 2002

Related U.S. Application Data

(60) Provisional application No. 60/291,402, filed on May 17, 2001.

(51) **Int. Cl.**[7] **H01L 27/00**

(52) **U.S. Cl.** ..... **250/208.1**; 250/214 A

(58) **Field of Search** ..... 250/214 A, 208.1, 250/241 A; 327/514; 330/308; 348/300, 308, 310, 241

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,892,540	A *	4/1999	Kozlowski et al.	348/300
5,898,168	A *	4/1999	Gowda et al.	250/208.1
5,900,623	A *	5/1999	Tsang et al.	250/208.1
6,084,229	A *	7/2000	Pace et al.	250/208.1
6,128,039	A *	10/2000	Chen et al.	348/294
6,493,030	B1 *	12/2002	Kozlowski et al.	348/310

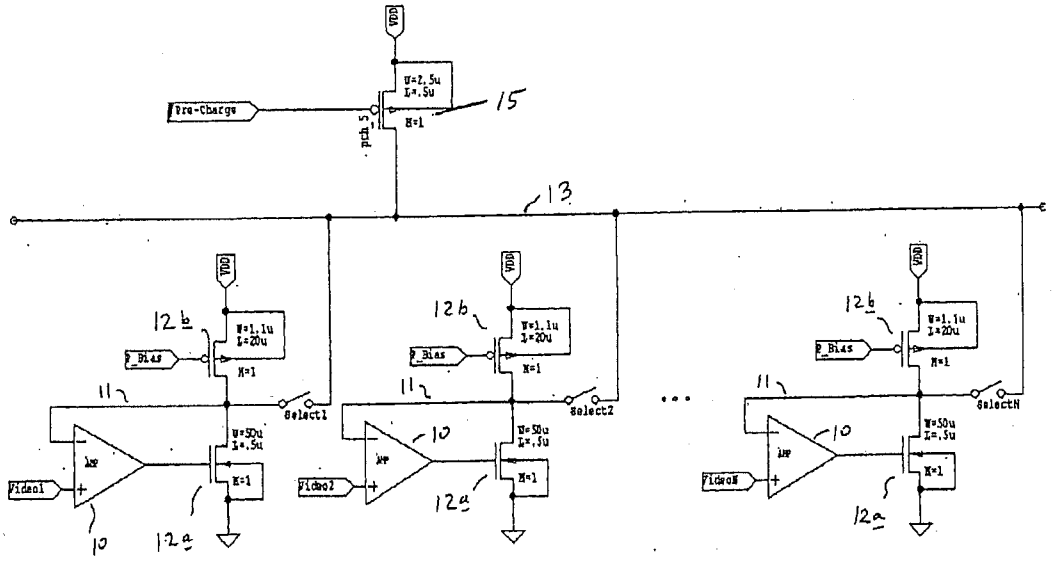
* cited by examiner

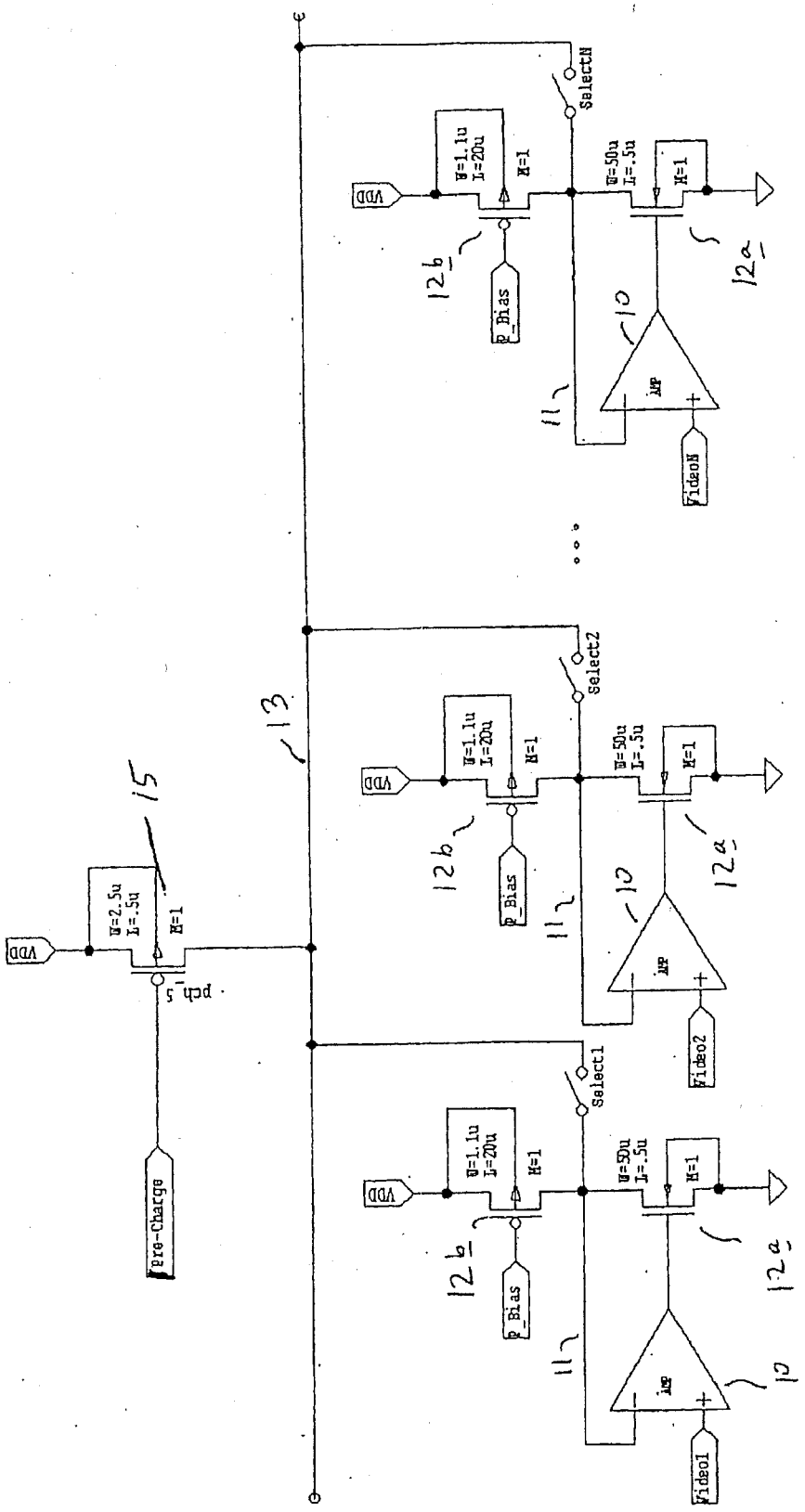
Primary Examiner—Stephone B. Allen
Assistant Examiner—Patrick J. Lee
(74) *Attorney, Agent, or Firm*—Bernhard P. Molldrem, Jr.

(57) **ABSTRACT**

A video bus for an array of pixel amplifiers is designed for a minimum quiescent current draw. The pixel amplifiers (or column amplifiers) are designed with high impedance pull-ups and low impedance pull-downs to conserve over-all power dissipation. The video bus is provided with a high-impedance P-FET to reset the bus to drain voltage V_{DD} for a very short time between the time one pixel (or column) is selected the time the next is selected, so that the video bus only has to be discharged through the low impedance N-FET. The bus does not have to be current-sourced by the P-FET.

7 Claims, 1 Drawing Sheet

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Select2
Select1
VDD
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L=.5u
M=1
P_Bias
AMP
VideoN
Video2
Video1
W=2.5u
L=.5u
M=1
Pre-Charge
12a
12b
10
11
13
15

PRE-CHARGING A WIDE ANALOG BUS FOR CMOS IMAGE SENSORS

This application claims the benefit of Provisional Application No. 60/291,402, filed May 17, 2001.

BACKGROUND OF THE INVENTION

This invention concerns means of pre-charging an analog bus in-between the selection periods to speed up the bus, minimize supply current in video bus driver circuit and reduce the physical size of arrayed analog driver circuitry. The invention concerns solid state imagers, and in particular is directed to an arrangement for obtaining high uniformity and improved image quality and reliability. Solid state image sensors are used in a wide variety of applications, and there has been much interest in pursuing low-cost, high-reliability image sensors. CMOS technology is well suited for imagers that are intended for portable applications, because of their need for a only a single power supply voltage, their ruggedness, and their inherent low power consumption. There has been great interest in achieving extremely high resolution also.

DESCRIPTION OF THE PRIOR ART

An active column sensor (ACS) architecture has recently been developed, as disclosed in Pace et al. U.S. Pat. No. 6,084,229, and which permits a CMOS image sensor to be constructed as a single-chip video camera with a performance equal to or better than that which may be achieved by CCD or CID imagers.

The majority of the current image sensors designs use one or more analog bus(ses) in order to sequentially scan the signals stored in a very large array. Wide-bus analog multiplexing has significant problems with highly capacitive loads and noise cross coupling from neighboring circuits. A surge in the analog current from charging and discharging the bus, can inject a significant amount of noise to the extremely sensitive pixel-site or pixel amplifier voltage storage nodes. If the arrayed analog buffer has to be able to drive the capacitive bus (even at moderate speeds) it will need a higher quiescent supply current in the output stage and that current gets multiplied by the number of arrayed elements to yield a very high undesired power consumption for the entire array.

A conventional analog bus driver design consists of a push-pull stage with a constant current source or resistor from drain voltage supply V_{DD} and an N-FET stage going to ground where the gate voltage of the N-FET stage is regulated to achieve a desired output voltage. The output voltages from all the analog bus drivers in the array are sequentially selected onto the bus by a transmission gate signal in order to read out all the signals from the arrayed drivers. This construction needs to be able to source a current to be able to pull the analog video bus to voltage that is higher than the previous voltage and so that there is a quiescent current when the bus driver is not selected onto the analog bus. With any arrayed devices, a quiescent current gets multiplied by the number of elements in the array and produces an undesirable high current draw.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object to provide a high quality output bus for a video array and at the same time to keep the quiescent current to a minimum.

It is an object to provide an bus and bus driver design that is of straightforward construction.

The Invention is straightforward: Quiescent power consumption of the arrayed circuits is reduced to an absolute minimum. A dead-band occurs between the time when any one of the transmission gates are closed and the time the next is closed (break-before-make), and in that short time the highly capacitive analog bus is pulled high by a P-FET to drain voltage V_{DD} and this is achieved using a simple digital control (for instance, NOR-ing the two-phase clock used for readout). This means that the array drivers do not need to source current to the highly capacitive analog bus in order to drive it to a higher voltage. Consequently, a much lower quiescent power consumption is possible for the entire device.

According to an aspect of the invention, an analog bus for a solid state video imager, comprises a) one or more conductive channels; b) a plurality of column output amplifiers, each connected with a selected pixel of its associated column, and having a low-impedance amplifier device; c) switching means for selectively connecting outputs of the column amplifiers to said one or more conductive channels; and d) a pre-charging high-impedance pull-up amplifier periodically charging up the one or more conductive channels between connections of said switching means.

The invention will be more fully understood from the ensuing description of a preferred embodiment, when read in connection with the accompanying Drawing.

BRIEF DESCRIPTION OF THE DRAWING

The sole FIGURE shows a portion of the column output amplifier circuits, and video bus, and a pre-charging amplifer, with a P-channel CMOS high-impedance pull-up amplifer and each pixel or column output circuit having an low-impedance N-channel pull-down circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The sole Drawing FIGURE illustrates an embodiment of this invention, in which there are an array of pixels which are configured in a number of columns, each having one or more pixels, i.e., defining rows. In this case, there are a plurality of pixel or column amplifiers **10**, **10**, etc., each with a respective video input, Video**1**, Video**2** . . . VideoN, applied to one input, and with a feedback input loop **11**. The output of the amplifier **10** has an output going to a push-pull bus driver that is formed of N-FET **12***a* and a current sourcing FET **12***b*. The output or drain side of the N-FET **12***a* is connected through a column select switch Select**1**, Select**2**, . . . SelectN, respectively, to the analog bus **13**, and also through the feedback loop **11** to an input of the associated amplifier **10**.

Pixel amplifiers are designed with high impedance pull-ups and low impedance pull-downs to conserve over-all power dissipation. The bus **13** is provided with a high-impedance P-FET **15** to reset the bus to V_{DD} for a very short time between the time one pixel (or column) is selected the time the next is selected, so that the video bus only has to be discharged through the low impedance N-FET. The bus **13** does not have to be current-sourced by the P-FET **15**.

Instead of pulling "up" to V_{DD}, it would be equivalent design for the amplifier **15** to pre-charge to ground or to a negative voltage, and have the low-impedance drivers charge the video bus **13** to a more positive level.

While the invention has been described with reference to a preferred embodiment, it should be understood that many

modifications and variations are possible without departing from the scope and spirit of the invention, as defined in the appended Claims.

I claim:

1. Analog bus for a solid state video imager, comprising

a) one or more conductive channels;

b) a plurality of column output amplifiers, each connected with a selected pixel of its associated column, and having a low-impedance amplifier device;

c) respective switching means for selectively connecting outputs of the column amplifers to said one or more conductive channels; and

d) a pre-charging high-impedance pull-up amplifier coupled to said one or more conductive channels for periodically charging up the one or more conductive channels between connections of said switching means.

2. Analog bus according to claim 1, said pull-up amplifier including a P-FET.

3. Analog bus according to claim 1, said pull-up amplifer including means providing a gating signal that occurs between times of actuation of the respective switching means.

4. Analog bus according to claim 2 wherein said P-FET has a predetermined PRE-CHARGE bias applied to a gate terminal thereof.

5. In a solid state video imager of the type that comprises an array of pixels arranged into a plurality of successive columns, with each said column including a column amplifier with a video input coupled to the pixels of the respective column, an output, and a respective column switch; and a video output bus comprising one or more conductive channels, with the column select switches periodically connecting the outputs of the column amplifiers to the one or more conductive channels of the video output bus; the improvement wherein the video output bus further includes a pre-charging high-impedance pull-up amplifier periodically charging up the one or more conductive channels of said output bus between actuations of said column select switches.

6. The imager as set forth in claim 5 wherein said pull-up amplifer includes a P-FET pull-up amplifier.

7. The imager as set forth in claim 6 wherein said P-FET has a predetermined PRE-CHARGE bias applied to a gate terminal thereof.

* * * * *

EXHIBIT B

US006633029B2

(12) **United States Patent**
Zarnowski et al.

(10) **Patent No.: US 6,633,029 B2**
(45) **Date of Patent: Oct. 14, 2003**

(54) **VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS AND METHOD THEREOF**

(75) Inventors: **Jeffrey Zarnowski**, McGraw, NY (US); **Matthew Pace**, Cortland, NY (US); **Thomas Vogelsong**, Jamesville, NY (US); **Michael Joyner**, North Syracuse, NY (US)

(73) Assignee: **Silicon Video, Inc.**, Ithaca, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 6 days.

(21) Appl. No.: **09/768,124**

(22) Filed: **Jan. 23, 2001**

(65) **Prior Publication Data**

US 2001/0030702 A1 Oct. 18, 2001

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/490,374, filed on Jan. 24, 2000, which is a continuation-in-part of application No. 09/039,835, filed on Mar. 16, 1998, now Pat. No. 6,084,229.

(51) **Int. Cl.**[7] **H01J 40/14**

(52) **U.S. Cl.** ..... **250/214 R**; 250/208.1

(58) **Field of Search** ..... 250/214 R, 208.1, 250/214 LA, 214 A; 257/291–293; 348/294–307

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,590,609	A	5/1986	Chevalet et al.	382/50
5,635,705	A	6/1997	Saunders	250/214 RC
5,712,932	A *	1/1998	Alexander et al.	102/344

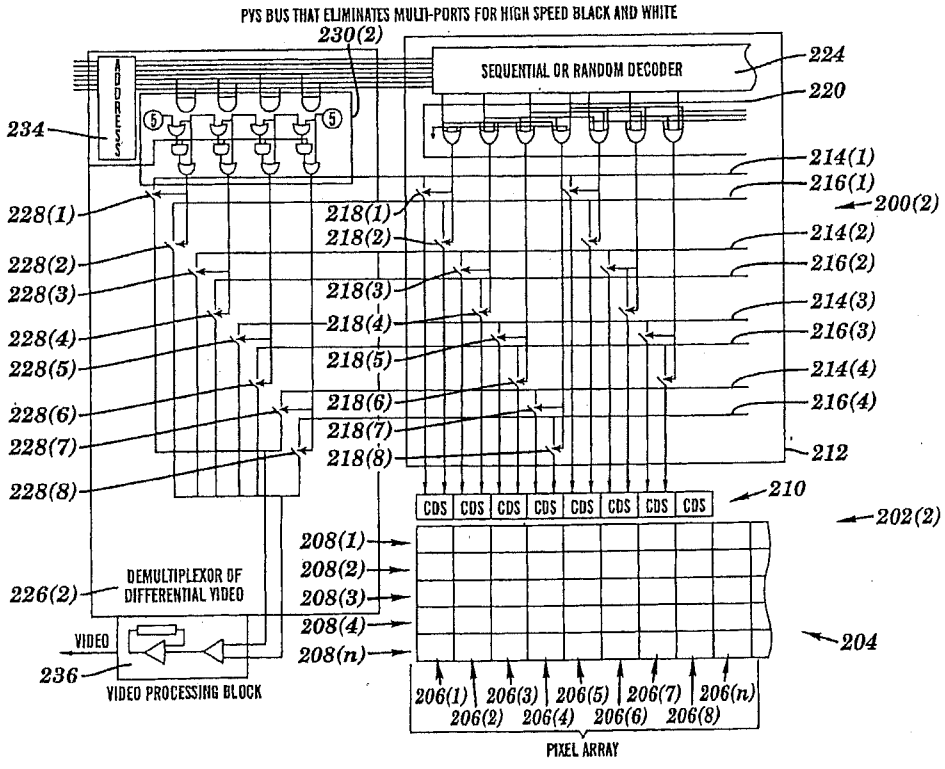
* cited by examiner

Primary Examiner—Que T. Le
(74) *Attorney, Agent, or Firm*—Bernhard P. Molldrem, Jr.

(57) **ABSTRACT**

A bus system and an imager for transferring signals from a plurality of signal streams to an output includes a plurality of signal buses in parallel and a control system. The control system multiplexes the signals from two or more of the plurality of signal streams onto two or more of the plurality of signal buses and allows the signals to substantially charge each of the two or more of the plurality of signal buses before demultiplexing the signals to the output. A method for transferring signals includes multiplexing signals on to two or more of a plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses before demultiplexing the signals to an output.

28 Claims, 12 Drawing Sheets



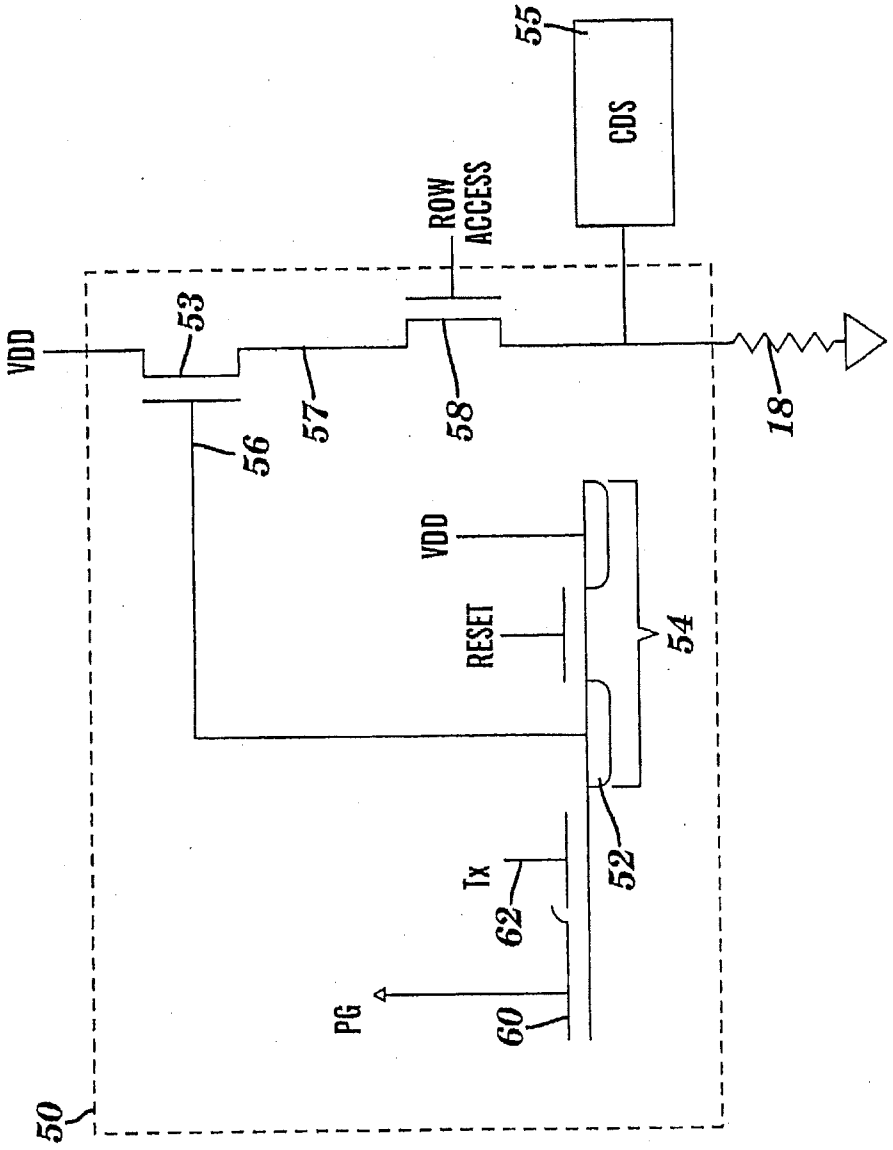
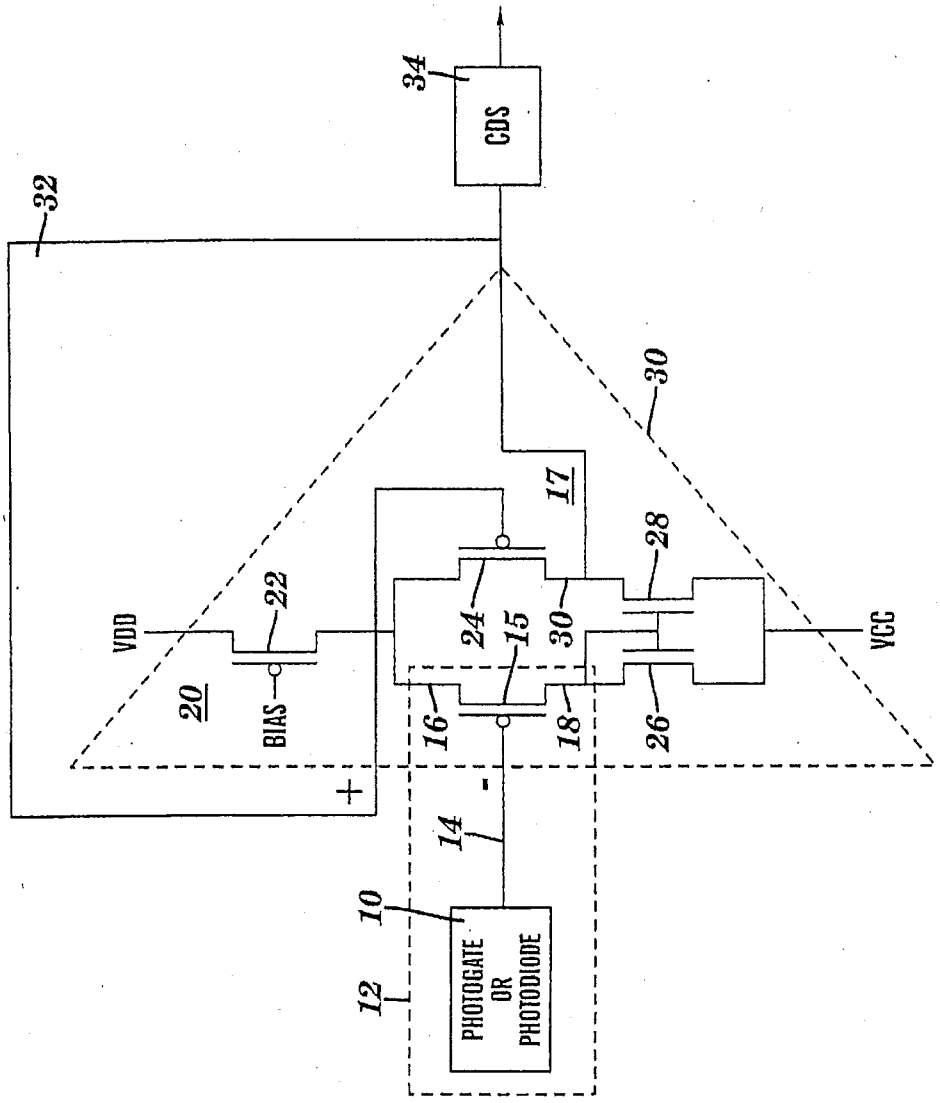


FIG. 1
PRIOR ART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CDS
32
30
17
28
VDD
22
24
15
30
VCC
20
BIAS
16
18
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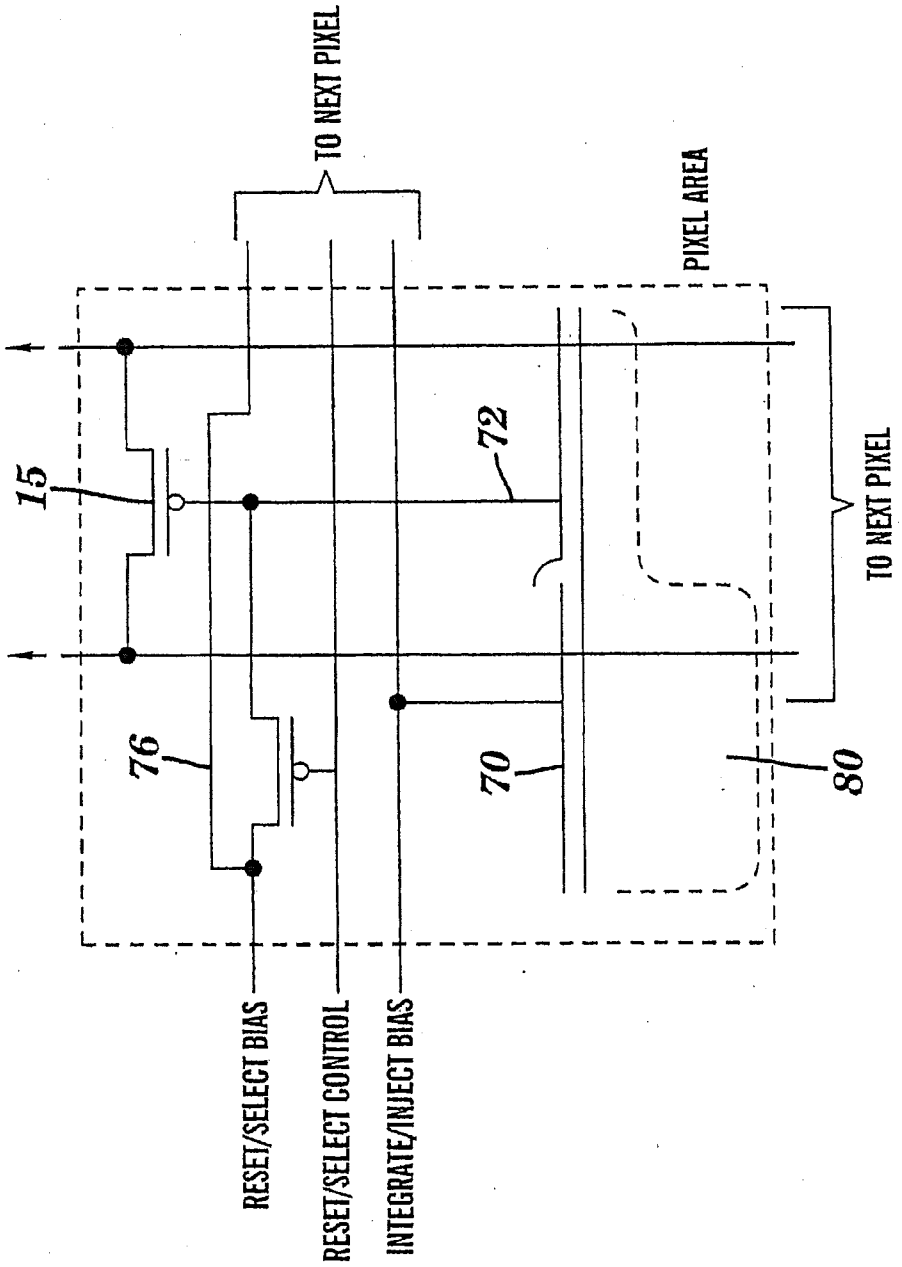
+
-
14
10
12
PHOTOGATE OR PHOTODIODE

FIG. 2


TO NEXT PIXEL
PIXEL AREA
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TO NEXT PIXEL
76
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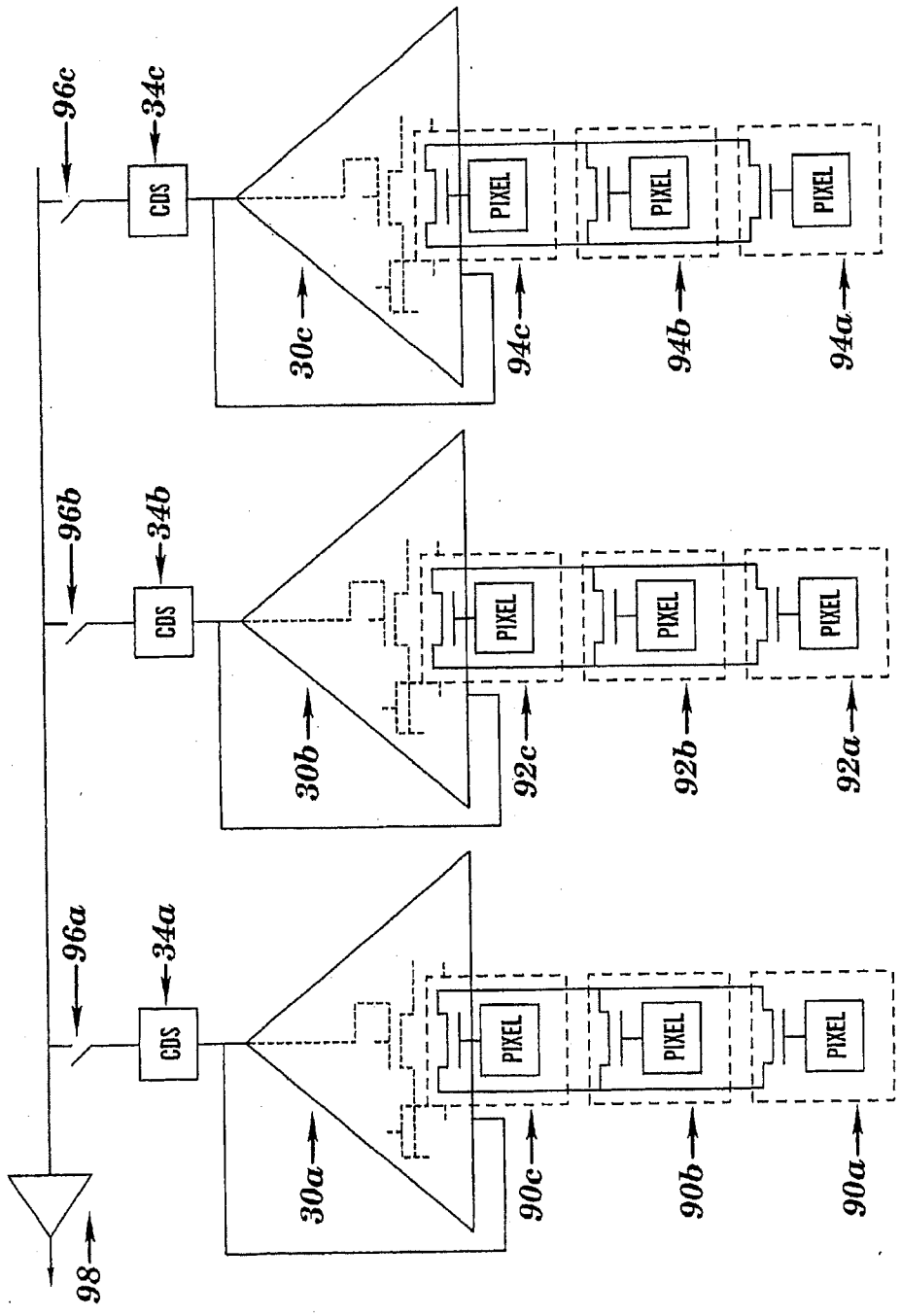
80
RESET/SELECT BIAS
RESET/SELECT CONTROL
INTEGRATE/INJECT BIAS

FIG. 3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PIXEL
PIXEL
30b
92c
92b
92a
96a
34a
CDS
PIXEL
PIXEL
PIXEL
30a
90c
90b
90a
98

FIG. 4

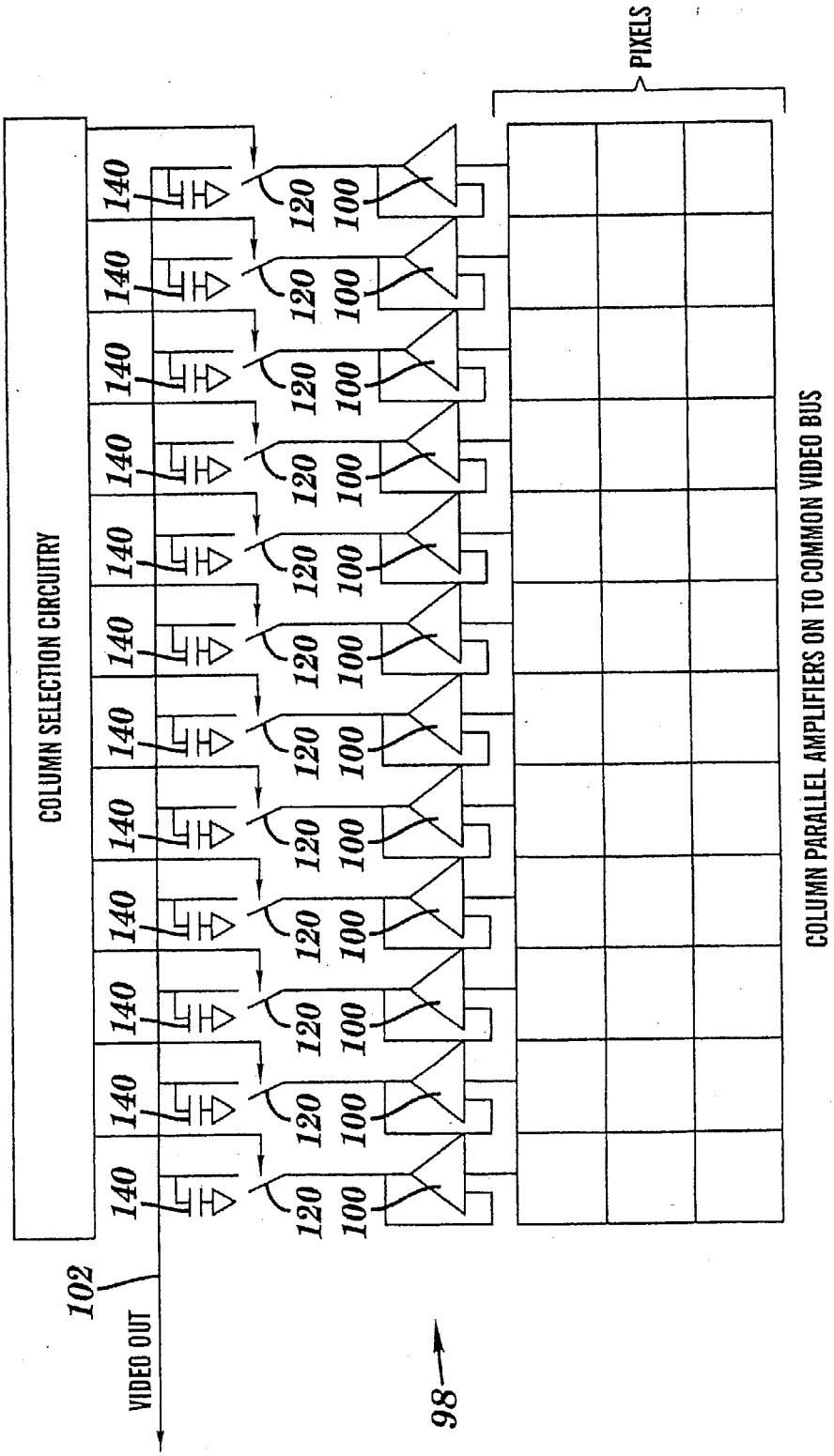
PIXELS
COLUMN SELECTION CIRCUITRY
COLUMN PARALLEL AMPLIFIERS ON TO COMMON VIDEO BUS
VIDEO OUT
102
98
140
120
100

FIG. 5

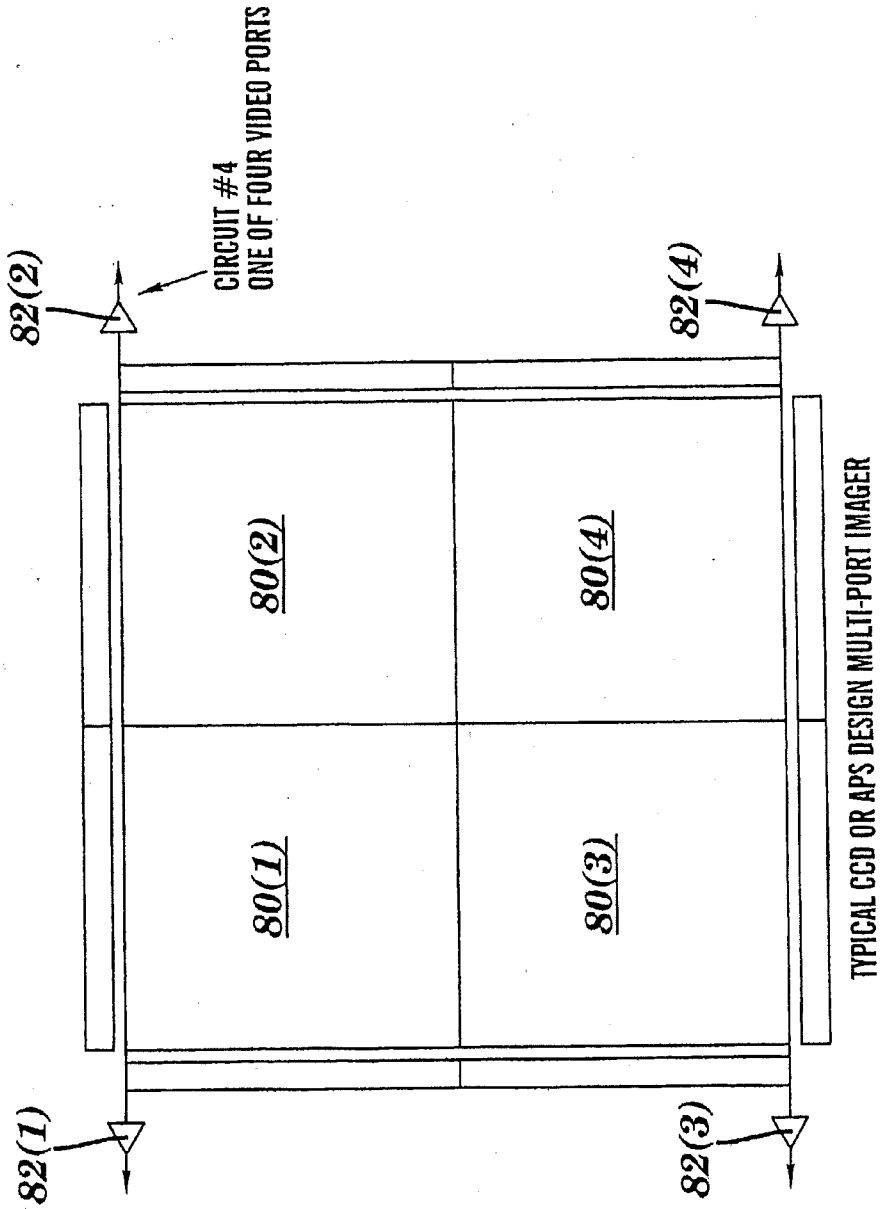
CIRCUIT #4
ONE OF FOUR VIDEO PORTS
82(2)
82(4)
80(2)
80(4)
80(1)
80(3)
82(1)
82(3)
TYPICAL CCD OR APS DESIGN MULTI-PORT IMAGER

FIG. 6

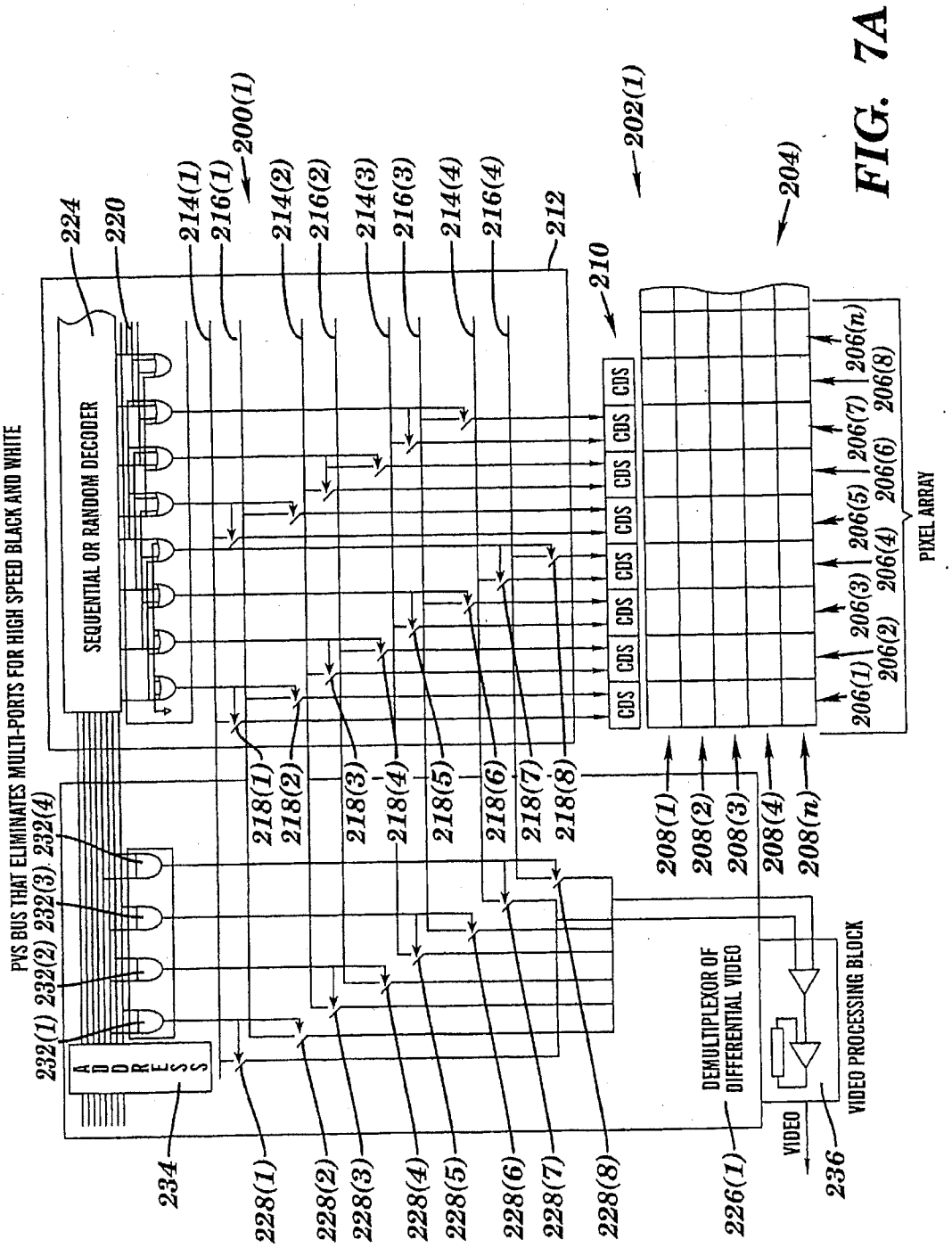
PVS BUS THAT ELIMINATES MULTI-PORTS FOR HIGH SPEED BLACK AND WHITE
SEQUENTIAL OR RANDOM DECODER
ADDRESS
DEMULTIPLEXOR OF DIFFERENTIAL VIDEO
VIDEO PROCESSING BLOCK
VIDEO
PIXEL ARRAY
CDS
224
220
214(1)
216(1)
200(1)
214(2)
216(2)
214(3)
216(3)
214(4)
216(4)
212
210
202(1)
204
206(1)
206(2)
206(3)
206(4)
206(5)
206(6)
206(7)
206(8)
206(n)
218(1)
218(2)
218(3)
218(4)
218(5)
218(6)
218(7)
218(8)
208(1)
208(2)
208(3)
208(4)
208(n)
232(1)
232(2)
232(3)
232(4)
234
228(1)
228(2)
228(3)
228(4)
228(5)
228(6)
228(7)
228(8)
226(1)
236

FIG. 7A

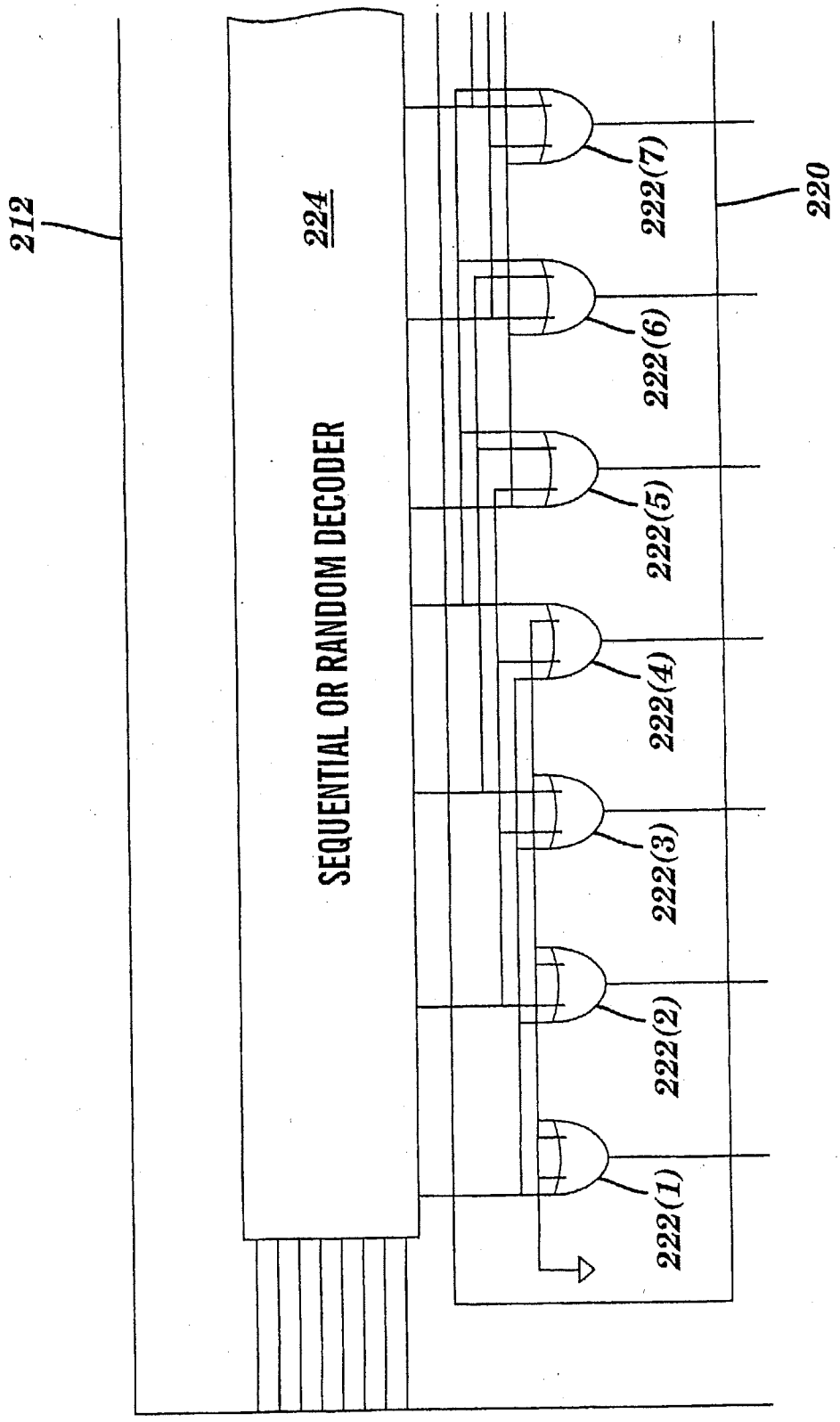
212
224
SEQUENTIAL OR RANDOM DECODER
222(7)
222(6)
222(5)
222(4)
222(3)
222(2)
222(1)
220

FIG. 7B

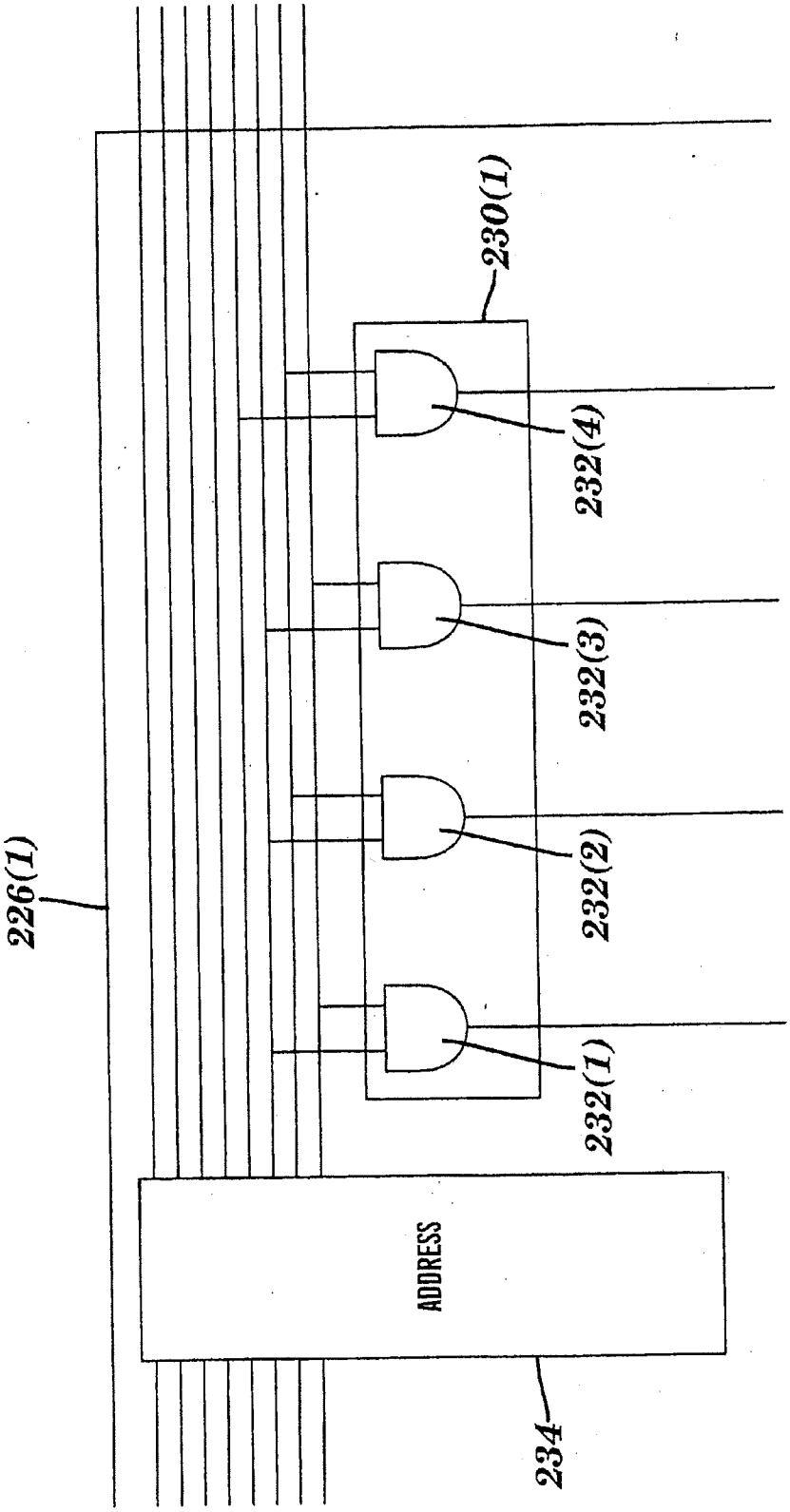

FIG. 7C

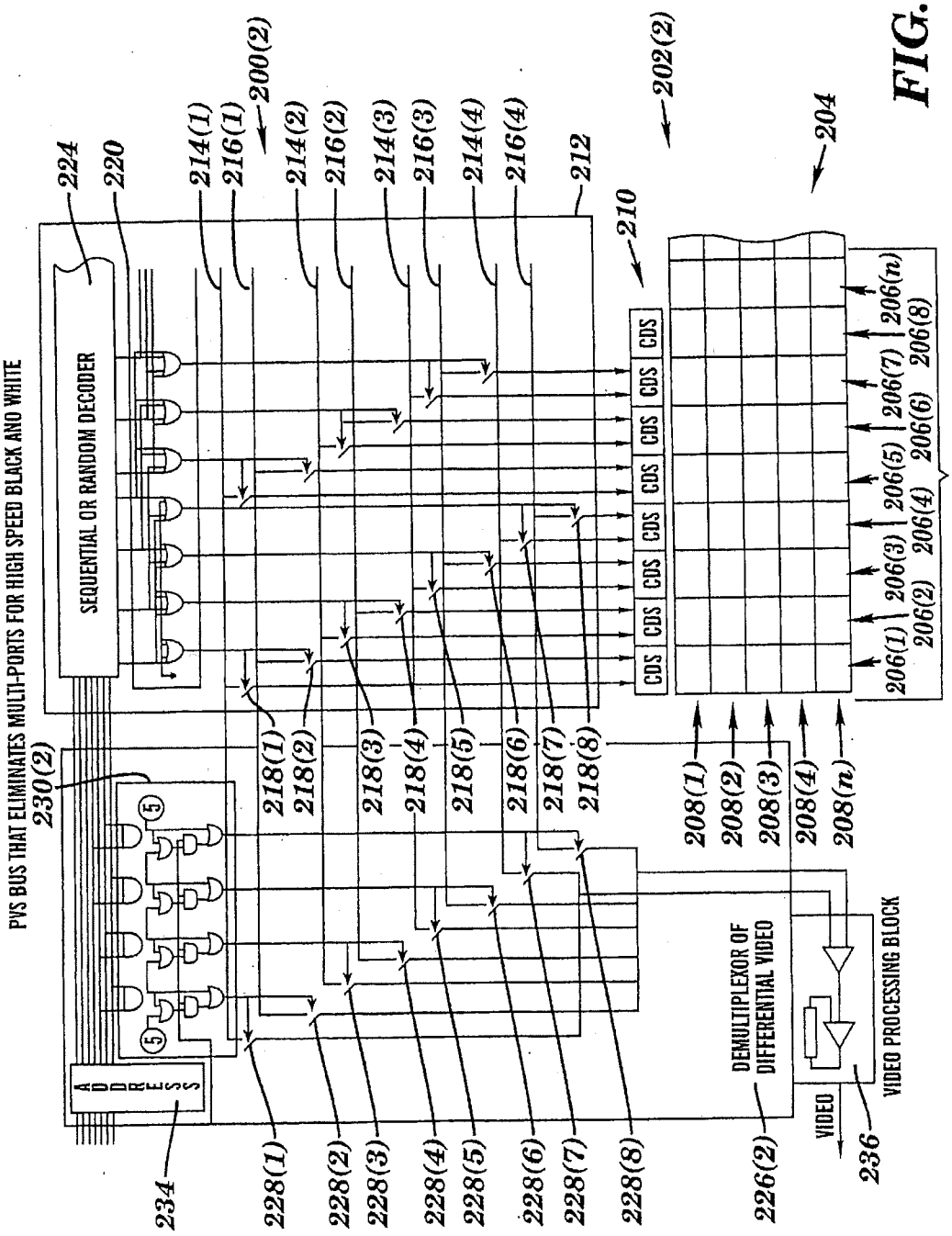
PVS BUS THAT ELIMINATES MULTI-PORTS FOR HIGH SPEED BLACK AND WHITE
SEQUENTIAL OR RANDOM DECODER
ADDRESS
DEMULTIPLEXOR OF DIFFERENTIAL VIDEO
VIDEO PROCESSING BLOCK
VIDEO
PIXEL ARRAY
CDS
224
220
230(2)
234
200(2)
202(2)
204
210
212
214(1)
214(2)
214(3)
214(4)
216(1)
216(2)
216(3)
216(4)
218(1)
218(2)
218(3)
218(4)
218(5)
218(6)
218(7)
218(8)
206(1)
206(2)
206(3)
206(4)
206(5)
206(6)
206(7)
206(8)
206(n)
208(1)
208(2)
208(3)
208(4)
208(n)
226(2)
228(1)
228(2)
228(3)
228(4)
228(5)
228(6)
228(7)
228(8)
236

FIG. 8A

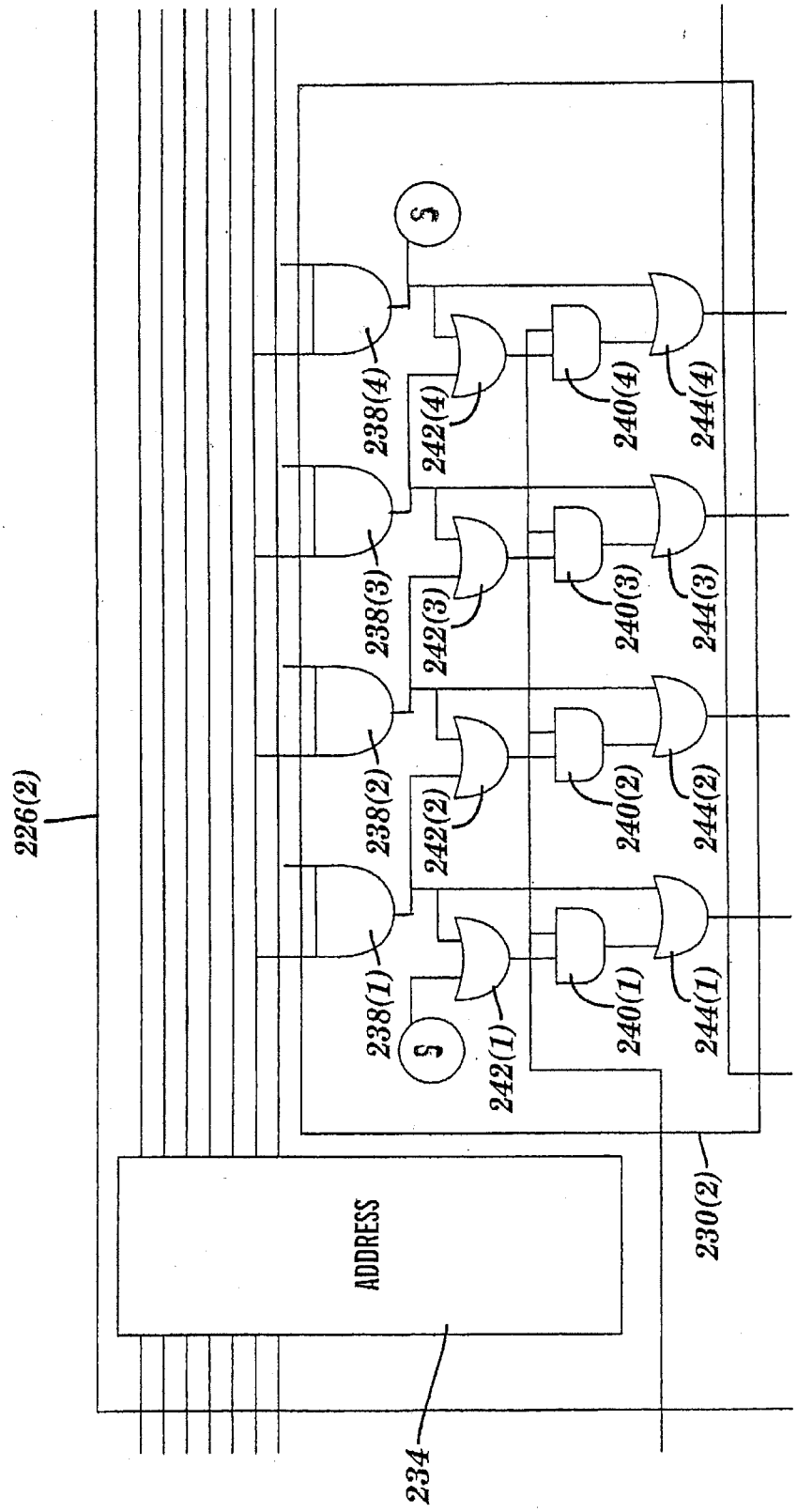
226(2)
238(4)
242(4)
240(4)
244(4)
238(3)
242(3)
240(3)
244(3)
238(2)
242(2)
240(2)
244(2)
238(1)
242(1)
240(1)
244(1)
S
S
ADDRESS
230(2)
234

FIG. 8B

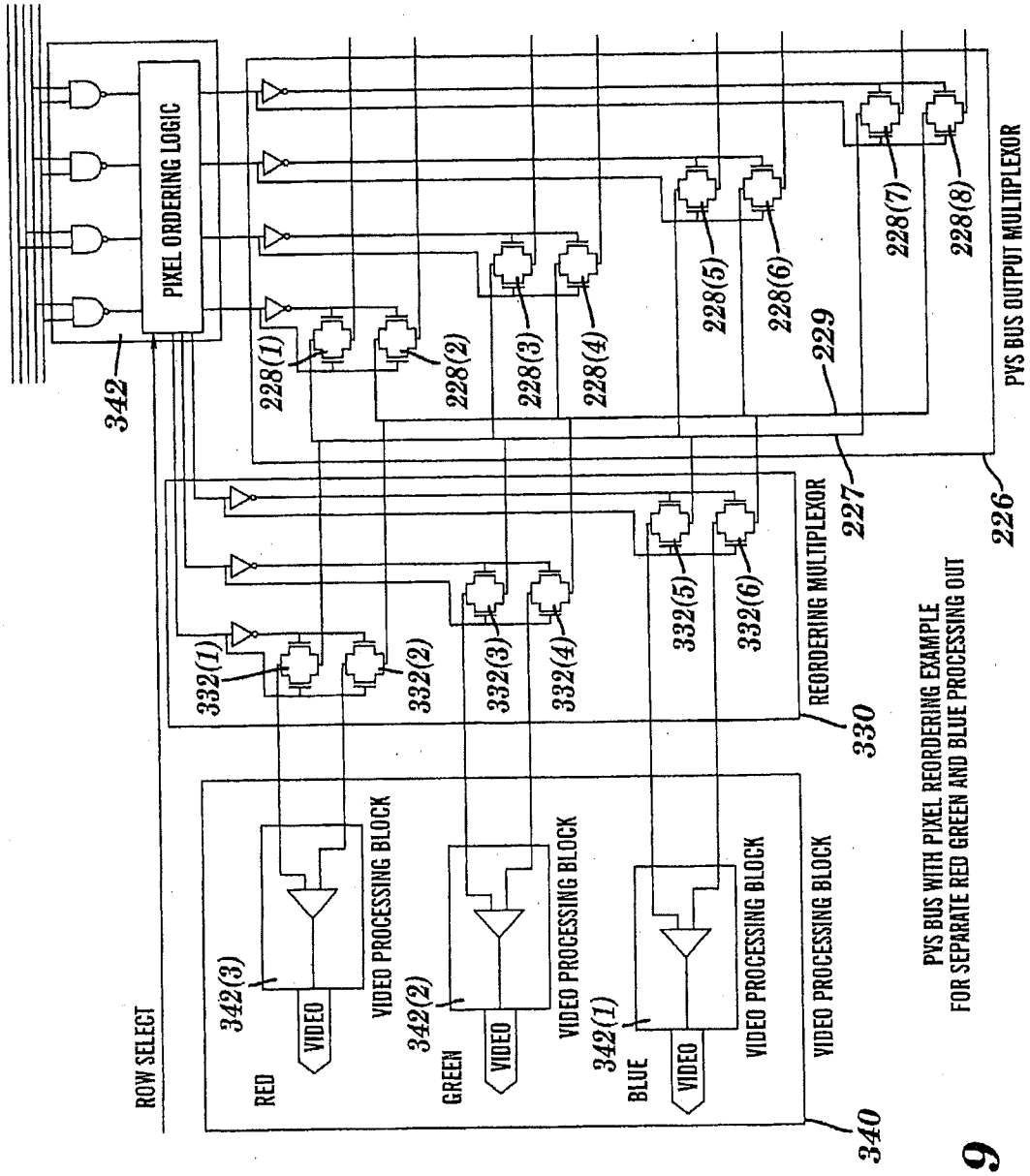
PIXEL ORDERING LOGIC
342
228(1)
228(2)
228(3)
228(4)
228(5)
228(6)
229
228(7)
228(8)
PVS BUS OUTPUT MULTIPLEXOR
226
227
REORDERING MULTIPLEXOR
330
332(1)
332(2)
332(3)
332(4)
332(5)
332(6)
PVS BUS WITH PIXEL REORDERING EXAMPLE
FOR SEPARATE RED GREEN AND BLUE PROCESSING OUT
ROW SELECT
340
VIDEO PROCESSING BLOCK
342(3)
RED
VIDEO
342(2)
GREEN
342(1)
BLUE

FIG. 9

VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS AND METHOD THEREOF

This application is a continuation-in-part application of application Ser. No. 09/490,374 filed on Jan. 24, 2000 which is a continuation-in-part application of Ser. No. 09/039,835 filed Mar. 16, 1998, U.S. Pat. No. 6,084,229 issued on Jul. 4, 2000.

FIELD OF THE INVENTION

This invention relates generally to a bus and, more particularly, to a video bus for high speed multi-resolution imagers.

BACKGROUND OF THE INVENTION

A solid state imager is a semiconductor device capable of converting an optical image into an electronic signal. Imagers can be arranged in a matrix and utilized to generate video signals for video cameras, still photography, or anywhere incident radiation needs to be quantified. When incident radiation interacts with a photogate, charge carriers are liberated and can be collected for sensing. The number of carriers collected in a photogate represents the amount of incident light impinging on the site in a given time-period.

There are two basic devices with many variants, employed to collect and sense, charge carriers in a photogate. The two basic devices are photodiodes and photogates. Variants of photodiodes include, but are not limited to: Pinned, P-I-N, Metal-Semiconductor, Heterojunction, and Avalanche. Photogate structures include: Charge Couple Devices (CCD), Charge Injection Devices (CID) and their variants that include virtual phase, buried channel and other variations that utilize selective dopants. The selective dopants are used to control charge collection and transfer underneath and between the photogate(s) and the sense node.

The solid state imagers heretofore used have been dominated by CCD's because of their low noise as compared to Photodiodes and CIDs. The low noise advantage of CCD imagers is the result of collecting the photon generated charge at the pixel site and then coupling or shifting the actual charge to an amplifier at the periphery of the array. This eliminates the need for the long polysilicon and metal busses that degrade the signal with their associated resistance and capacitance. However, the low noise of the CCD requires the imager to be read in a fixed format and once the charge is read it is destroyed. The requirement of coupling the collected photon charge from the pixel to the periphery amplifier (a.k.a. CTE), requires proprietary processing steps not compatible with industry standards CMOS or BiCMOS processes.

Solid state imaging devices have developed in parallel with CMOS technology and as a result all imager manufacturers developed their own proprietary processes to maximize imager performance characteristics and wafer yield. Specialized silicon wafer processing kept imager prices relatively high. Linear active pixel sensors have been commercially produced since 1986. Beginning in the early 90's the move to transfer the proprietary processes to an industry standard CMOS processes was on. The advantages of using an industry standard process include: competitive wafer processing pricing, and the ability to provide on chip timing, control and processing electronics. By the end of the year. 1992, a 612x512 CMOS compatible, CID imager with a preamplifier and CDS per column had been fabricated. The

imager could either be operated as a random access 512x512 CID, or all the columns could be summed together and operated as a linear active pixel sensor.

Area arrays utilizing active pixel sensors in which a photodiode or photogate is coupled to an output source follower amplifier which in turn drives a Correlated Double Sampling (CDS) circuit, where the two outputs of the CDS cell then drives two more source followers circuits that in turn are fed into a differential amplifier are shown in U.S. Pat. No. 5,471,515 which is herein incorporated by reference. This uses source follower circuits, that typically have gains less than unity that vary from one source follower to another. The source follower gain variation is due to variations of FET thresholds. The source follower gain variation results in a pixel to pixel gain mismatch. Also, the active pixel sensors suffer gain variations due to the CDS circuit per column, when the CDS employs a source follower pair to drive its output. The resulting CDS signal and its corresponding offset can have different gains that are not correctable by the differential amplifier. Also, the source follower configuration of active pixel doesn't allow for binning of pixels.

The voltage mode of operation of prior art does not allow for binning, which, is the summation to two or more pixel signals at once.

What is needed is an imager which has the low noise level of a CCD, the random access, and binning of a CID, and uniform gain and response from all pixels; while, maintaining low power, ease of use and high analog video frame rates.

In addition to finding an imager which has the low noise level of a CCD, the random access, and binning of a CID, and uniform gain and response from all pixels, imagers suitable for industrial and/or scientific applications are also needed. Over the last 30 years the CCD sensor and camera electronics technology has evolved to meet most of the demands for industrial and/or scientific applications. However, the resulting cameras require a state-of-the-art, large pixel, multi-port CCD chip plus several extra chips and usually several circuit boards filled with electronics to accomplish this. Thus, the cameras cannot physically fit in certain applications, the power consumed is significant, and the resulting cameras are far too expensive for many applications. The necessary recombination of the video data from several ports, further increases the video processing complexity and ultimately drives-up the cost and size of the video system.

As discussed earlier over the past several years, thanks to design rule shrinkage, image sensors using sub-micron CMOS process technology have become practical. By using CMOS technology for the sensor array itself, the problem of integrating extra circuitry on chip becomes straightforward. Elements such as A/D converters, timing generators, control circuitry and interface circuitry can easily be added. In addition, the operation of CMOS imagers is simplified by the elimination of the need for precise timing and level control of multiple clocks required to drive the large capacitance transfer gates inherent in CCD'S. Even with all of these factors, including the exceptional speed and picosecond gate delays of sub-micron processes, the analog video bandwidth per port has not changed much over the past twenty years.

Active pixel sensors (APS) have been proposed as the means to achieve the flexible benefits of CMOS cameras on a chip. Unfortunately, there are performance issues with the fundamental APS approach that limit its performance and

functionality. While these limitations may be acceptable for low-end consumer imaging applications, the demands of scientific, professional and industrial applications have, up until now, been largely unmet by CMOS image sensors.

More specifically, industrial and scientific imaging applications require much higher performance and functionality than that required for low-end consumer imaging products. Many of the applications require high readout speeds for video rate or even faster imaging without sacrificing image quality. In addition to image quality, the applications have come to demand greater functionality in the camera. Features such as flexible shuttering and electronic zoom, random access and selectable region of interest for maximizing frame rates and minimizing data storage (especially useful in tracking applications). Lowering the cost of machine system development is the recent advancement of single chip CMOS cameras. Newly developed CMOS cameras have all the flexibility previously listed, however the analog video bandwidth per port has not changed from the traditional CCD, CID or Photodiode technologies.

Most mega-pixel image sensors, including both CCD imagers and APS imagers, have a maximum pixel rate inadequate to meet the frame rate needs of industrial and scientific imaging. CCD devices are limited by both clocking rates and the speeds of the Correlated Double Sampled (CDS) circuitry. In addition the higher amplifier bandwidth required for higher pixel rates increases noise levels. With the column parallel nature of CMOS imagers, the amplifier and CDS can be run at the line rate rather than the pixel rate. The video bandwidth constraints come in terms of the multiplexing speed. CMOS imagers typically multiplex their signals onto a common analog video bus. The more signals that are multiplexed or switched onto the bus, the greater the capacitive load of that bus. Therefore, as more signals are connected to the bus, the bandwidth of the bus is reduced. Alternatively, greater power is needed to charge and discharge the bus with its associated capacitance to maintain bandwidth. This traditional bus structure described above involves N signals that are switched onto one bus.

One example of a CMOS imager **98** with column parallel amplifiers **100** that drive a common video bus **102** is illustrated in FIG. **5**. In this example, the common video bus **102** is seen mostly as a capacitive load **140** to each individual column amplifier **100**. In order for each amplifier **100** to truly represent the pixel value onto the common video bus **102**, each amplifier **100** must charge or discharge the bus **102** with in one pixel time constant. The pixel value signal must be stable long enough for a sample and hold circuit (or similar) to accurately present the resultant signal to an A to D converter (not shown). Typically, at least 5τ (tau or time constants) is desired to accurately allow the video bus **102** to settle the video value presented by each individual column amplifier **100**, although this can vary between applications. At higher video bus speeds each amplifier **100** is unable to properly charge or discharge the video bus **102** resulting in a loss of contrast ratio. At higher pixel element rates where the contrast ratio is compromised, the individual column amplifier characteristic and the video switch characteristics begin to affect the resultant video. Each individual column amplifiers **140** has a slightly different offsets with slightly different drive capabilities and each video switch **120** will have slightly different resistances and slightly different thresholds. This combination of column amplifier and video switch characteristics results in each column amplifier **100** having different time constants relative to charging and discharging the video bus **102**. The column amplifier **100** and video switch **120** are common to every pixel in that column. Thus, variations in the video switch characteristics result in what appears to be column based Fixed Pattern Noise (FPN). As more columns are added, each video switch **120** adds more associated capacitance **140** due to the source and drain junctions of MOSFET or Bipolar transistors. The more columns added to the bus **102**, the higher the total capacitance.

In order to overcome these constraints, one prior solution by designers of CCD's and APS sensors has been to divide up the imager into halves, quarters, or smaller groupings of sub-imagers jammed together. One example of this prior design solution is shown in FIG. **6**. In this example, the imager **80** is divided up it to four sub-imagers **80(1)–80(4)**. The signal from each of these sub-imagers **80(1)–80(4)** is brought out to its own port **82(1)–82(4)**. This structure or architecture also involves getting many signal streams of N signals on to one bus. This design has been used to provide high frame rate devices and to meet standard frame rates with large mega-pixel imagers. Unfortunately, this design adds system size, complexity, power and cost to handle the multiple analog amplifier chains. Additionally, it is an extremely challenging task to balance the amplifier chains completely over all possible pixel rates and temperatures. This issue has become even more of a problem in recent years as imagers have grown larger, now up to full wafer size. The process variations across an array can lead to further balance problems, and even variations in noise characteristics due to process variations across a wafer.

SUMMARY OF THE INVENTION

A bus system for transferring signals from a plurality of signal streams to an output in accordance with one embodiment of the present invention includes a plurality of signal buses in parallel and a control system. The control system multiplexes the signals from two or more of the plurality of signal streams onto two or more of the plurality of signal buses and allows the signals to substantially charge each of the two or more of the plurality of signal buses before selecting the signals to the output multiplexor.

An imager in accordance with another embodiment of the present invention includes a plurality of streams of signals, a plurality of signal buses in parallel, an output, and a control system. The control system multiplexes the signals from two or more of the plurality of signal streams onto two or more of the plurality of signal buses (i.e. an input multiplexor) and allows the signals to substantially charge each of the two or more of the plurality of signal buses before demultiplexing the signals to the output multiplexor.

A bus system for transferring signals from a plurality of signal streams to an output in accordance with another embodiment of the present invention includes a plurality of signal buses coupled to the plurality signal streams, a plurality of first switches, a plurality of second switches, and a control system. Each of the plurality of first switches is coupled between one of the plurality of signal streams and one of the plurality of signal buses. Each of the plurality of second switches coupled between one of the plurality of signal buses and the output. The control system is coupled to the first and second switches and closes two or more of the plurality of first switches to couple signals from the two or more of the plurality of signal streams to two or more of the plurality of signal buses and allows the signals to substantially charge each of the two or more of the plurality of signal buses before closing one or more of the plurality of second switches of the output multiplexor to couple the signals to the output. In other words, this system described

above involves N signals multiplexed to two or more busses (or M busses) and then multiplexed on to one bus or in other words a two stage multiplexor with an input multiplexor and an output multiplexor. A two stage multiplexing system allows for a variety of different operations, such as allowing signal or pixel signal skipping and allowing multiple signals or pixels signals to be selected at once. By way of example, pixel signals could be alternately individually selected and then two adjacent signals could be selected to allow signal averaging or interpolation, effectively changing the native resolution of pixel for either higher or lower resolution. This present invention coupled with Active Column Technology as described in U.S. Pat. No. 6,084,229, which is herein incorporated by reference, allows for binning or skiping of pixels along the rows as well as the columns.

A method for transferring signals in accordance with yet another embodiment of the present invention includes multiplexing signals on to two or more of a plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses also known as input multiplexing before demultiplexing select signals by the output multiplexor. Also, included in this particular embodiment is a reordering multiplexor that redirects signals from the output multiplexor to one or more outputs.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a prior art double polysilicon active pixel sensor;

FIG. **2** is an active column sensor in accordance with this invention;

FIG. **3** is an implementation of a pixel in accordance with the invention;

FIG. **4** is a schematic illustration of a matrix of pixels connected to incorporate a full operational amplifier per pixel forming an Active Column Sensor;

FIG. **5** is a view of a conventional method of driving a common video bus on an imager;

FIG. **6** is a view of a traditional CCD and CMOS sensor method of increasing video bandwidth with multiple ports;

FIG. 7A is a diagram of an imager with a high speed, low noise bus system in accordance with one embodiment of the present invention;

FIG. 7B is an enlarged view of a decoder and a preselection circuit in the imager shown in FIG. 7A;

FIG. 7C is an enlarged view of an address counter and control circuit in the image shown in FIG. 7A;

FIG. 8A is a diagram of an imager with a bus system for pixel interpolation for increased resolution in accordance with another embodiment of the present invention;

FIG. 8B is an enlarged view of an address counter and a control circuit in the imager shown in FIG. 8A; and

FIG. **9** is a block diagram of a bus system with another bus output multiplexor, control circuit, and video processing block in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION

Before discussing the Active Column Sensor (ACS) circuit of FIG. **2** of the present invention and described in conjunction with a discussion of ACS below, it will be useful to discuss the structure of a typical double-polysilicon active pixel sensor of prior art as shown in FIG. **1**.

In FIG. **1** each pixel **50** has a photogate **60** that has an output FET **53** configured as a source follower. The source follower **53** is used to drive a subsequent signal conditioning circuitry, such as a Correlated Double Sampled Circuit (CDS) **55**. The gain through a source follower **53** is less than unity. If the source follower located at the pixel site **50** has a given gain other pixels and their respective source followers in the same column may or may not have the same gain. The technique relies on wafer processing for all FETs in the array to have the same threshold. It isn't uncommon for FET thresholds, during operation, to vary by 100 mV for a linear active pixel array.

The active pixel **50** of the prior art includes a photogate **60** and a transfer gate **62** that are used to couple photo generated charge onto the floating diffusion node **52** which is connected to the gate **56** of source follower **53**. The drain of the output FET **53** is connected directly to a power supply rail VDD. The source follower output FET is in turn connected to the source **57** of row access FET **58**. When the row access FET **58** is selected for reading, the FET **58** is turned on, allowing output FET **53** to be connected to a load **18** and drive the CDS circuitry **55** directly.

FIG. **2** is a schematic diagram of a pixel **12** in accordance with the present invention in which the threshold variations from pixel to pixel of the prior art are eliminated. All pixels **12** in a row or column are in parallel and for simplicity only one is shown. Pixel **12** which can consist of any photosensitive device **10** is coupled to a FET **15** to isolate the pixel from the readout circuitry. The FET **15** is one FET of a differential input pair of an operational amplifier **30** that includes FET **24**. For simplicity, in FIG. **2** the amplifier circuit **30** is configured as a positive feedback unity gain amplifier. A feedback path **32** connects the output of amplifier **30** to input **17** which in this case is the gate of FET **24**. The amplifier **30** could be configured to have gain, a full differential input or any operational amplifier configuration as the application required. The fixed gain of amplifier **30** eliminates the gain variability of the prior art. The output of the unity gain amplifier is connected to a Correlated Double Sampler (CDS) which is utilized to eliminate any fixed pattern noise in the video.

A current source **20** comprising an FET **22** has its source connected to a power source VDD and its drain connected to the sources of differential input FETs **15** and **24**.

The drains of input FETs **15** and **24** are connected to a current mirror formed from FETs **26** and **28**. The gates of FETs **26** and **28** are connected together and to the source **18** of input FET **15**. The sources of FETs **26** and **28** are connected to a negative power source, VCC.

The drain **30** of FET **24** is the output of the differential pair and is connected to CDS **34**.

The input FET **15** could be either a N channel or P channel FET as the application requires. The pixel **80** could be either a photogate or photodiode.

FIG. **3** is a detailed schematic of pixel **12** of the active column sensor shown in FIG. **2**. In this implementation a photogate **76** is utilized. Selection and reset of a sense node **72** is controlled by an FET **76**. This Active Column Sensor pixel eliminates the separate selection/access FET **58** of prior art. All biasing and controls signals are supplied from the periphery of the pixel array.

The pixel can be operated in the following manner. An N type substrate is used and the substrate is biased the most positive potential, e.g. 5.0 volts. The photogate **70** preferably a layer of polysilicon is biased to an integrate level (e.g. 0.0 volts). The region **80** under the photogate **70** is depleted and as light strikes the immediate area, it will collect (integrate) photon generated carriers. Photogate **72** is biased to the 5.0

volts and will not collect photon generated carriers during the integration because it is biased to the same potential as the substrate. Photogate **72** is biased by selecting control FET **76** with the reset/Select Control signal. In this configuration control FET **76** is a P channel FET that is selected by a negative signal relative to the substrate, for example 0.0 volts. During integration FET **76** is selected, the photogate is biased by the reset/select bias that preferably is at 5.0 volts. After a predetermined integration time period the pixel is read.

Reading the pixel is preferably accomplished in the following manner. The reset/select control is changed to 2.5 volts, causing the region beneath photogate **72** to be depleted, and the background level is read. Reset/select FET **76** is turned off by setting the reset/select control to 5.0 volts. Photogate **70** has its potential removed, and in this example 5.00 volts. Reading the signal will occur as the collected photon generated charge transfers from the region beneath photogate **70** to the region beneath photogate **72**. The transferred photon generated charge modulates the gate of input FET **15**, according to the amount of collected.

Fixed Pattern Noise (FPN) can be eliminated from the video information by utilizing CDS circuit **34**. The first sample applied to the CDS circuit is the background level. The signal information is then applied to the CDS. The difference of the two signals provides for a fixed pattern noise free signal.

FIG. **4** is a schematic diagram of an array of pixels in accordance with this invention. A plurality of pixels **90***a*, **90***b*, **90***c* form a first column of the array, and similar columns **92***a–c* and **94***a–c* complete the array. Within each column, the pixels are connected with their output FETs in parallel, the combination forming the first one of the differential input pair of operational amplifier **30**. In all other respects, amplifiers **30***a*, **30***b* and **30***c* are identical to FIG. **2**. Each amplifier **30** is connected to a CDS **34***a*, **34***b*, and **34***c* respectively. The outputs of CDS **34***a, b, c* are connected through column select switches **96***a*, **96***b*, and **96***c*, the common terminals of which are connected to output buffer **98** which can be a source follower, or a more complex signal conditioner as required by the specific application.

As discussed earlier, industrial and scientific imaging applications require much higher performance and functionality than that typically required for consumer imaging products. More specifically, many of these applications require high readout speeds for video rate or even faster imaging without any sacrifice in image quality. One of the advantages of the present invention is that it provides an on-board, high-speed bus system **200** or PVS bus that allows pixel rates exceeding those of prior single port CCD or APS devices and other prior analog buses. This bus system **200** in combination with the highly parallel nature of amplifier per column techniques of CMOS sensors provides the functionality and the high speed performance required for scientific and industrial applications. This speed increase has been achieved without increasing power consumption while maintaining full video bandwidth even at the higher speeds. Additionally, the present invention is able to eliminate common mode noise pickup through the use of fully differential processing. Further, the high speed, low noise, low power, analog PVS bus utilizes either standard sequential or random access decoders for selection of a particular column. In addition to selecting a column, the bus system **200** has the added preselection circuitry to pre-select the next multiple columns in the read sequence in parallel. The number of columns pre-selected can be scaled to meet the application requirements.

Referring more specifically to FIG. **7A**, a diagram of an imager **202(1)** with a high speed, low noise bus system **200(1)** in accordance with one embodiment of the present invention is illustrated, although the bus system **200** could be used with a variety of different types of devices, such as video cross point switch, and for a variety of different types of applications. In this particular embodiment, the imager **202(1)** includes a pixel array **204** with a plurality of columns **206(1)–206(*n*)** and rows **208(1)–208(*n*)** of pixels along with image processing circuitry, such as that described earlier with reference to FIGS. **2–4**. An optional correlated double sampling ("CDS") circuit **210** is coupled to the end of each of the columns **206(1)–206(*n*)** in this example. Although in this particular example the bus system **200(1)** is coupled to the end of the columns **206(1)–206(*n*)** for the array **204**, the bus system **200(1)** could also be coupled in to other locations, such as to the end of the rows **208(1)–208(*n*)** of the array **204**.

A multiplexor **212** is coupled to one of the ends of the columns **206(1)–206(*n*)** for the array **204**, although the multiplexor **212** could be coupled to other locations and to other sources of data. In this particular embodiment, the multiplexor **212** comprises a plurality of multiplexing buses **214(1)–214(4)** and **216(1)–216(4)**, a plurality of switches **218(1)–218(8)**, and a preselection or control circuit **220**, although the multiplexor **212** could be made of other components. The multiplexor **212** selects multiple columns **206(1)–206(*n*)** or rows **208(1)–208(*n*)** of the array **204** and then multiplexes signals from those columns **206(1)–206(*n*)** or rows **208(1)–208(*n*)** on to the multiplexing buses **214(1)–214(4)** and **216(1)–216(4)** at the same time.

More specifically, in this particular embodiment each column **206(1)–206(*n*)** of the array **204** through the CDS circuit **210** is coupled to one of the plurality of multiplexing buses **214(1)–214(4)** and **216(1)–216(4)**. There are four pairs of multiplexing buses: **214(1)**, **216(1)**; **214(2)**, **216(2)**; **214(3)**, **216(3)**; and **214(4)**, **216(4)**, with one pair of multiplexing video buses coupled to each column of the array **206(1)–206(4)**, although the total number and types of buses as well as the number of buses coupled to each column or row of the array **204** can vary as needed or desired. In this particular embodiment, a pair of multiplexing buses are coupled to each column of the array to permit differential processing.

The switches **218(1)–218(8)** are each coupled between one of the columns **206(1)–206(4)** of the array **204** and one of the multiplexing buses **214(1)–214(4)** and **216(1)–216(4)**. Each of the switches **218(1)–218(8)** has an open position and a closed position. In an open position, the switches **218(1)–218(8)** disconnect the columns **206(1)–206(4)** of the array **204** from the multiplexing bus **214(1)–214(4)** and **216(1)–216(4)** and in a closed position the switches **218(1)–218(8)** couple the columns **206(1)–206(4)** of the array **204** to the multiplexing buses **214(1)–214(4)** and **216(1)–216(4)**.

The preselection circuit **220** (also shown in FIG. **7B**) is coupled to each of the switches **218(1)–218(8)** and controls whether each of the switches **218(1)–218(8)** is in an open or a closed position. Since control circuits to control the opening and closing of switches are well known to those of ordinary skill in the art, the preselection circuit **220** will not be described in detail here. In this particular embodiment, the preselection circuit **220** comprises a plurality of "OR" Boolean logic function gates ("OR gate") **222(1)–222(*n*)** that each have four inputs and one output, although other types of components with other numbers of inputs and outputs and other types of logic functions could be used for the preselection circuit **220**.

A decoder **224** (also shown in FIG. 7B) with a plurality of inputs and a plurality of outputs is coupled to the preselection circuit **220**. A variety of different types of decoders **224** could be used, such as a sequential decoder or a random decoder. The decoder **224** transmits input signals to each of the OR gates **222(1)–222(*n*)**. The output of each OR gate **222(1)–222(*n*)** is coupled to one of the switches **218(1)–218(*n*)** and depending upon the signals received via the inputs to the OR gates **222(1)–222(*n*)**, the signal from the output of the OR gate **222(1)–222(*n*)** coupled to each switch **218(1)–218(*n*)** will either open or close that switch **218(1)–218(*n*)**. In this particular embodiment, the decoder **224** and preselection circuit are designed to couple multiple columns of the pixel array to the different multiplexing buses **214(1)–214(4)** and **216(1)–216(4)** at one time.

An output multiplexor **226** is coupled to each of the multiplexing buses **214(1)–214(4)** and **216(1)–216(4)** and is designed to match the configuration of the multiplexor **212**. In this particular embodiment, the output multiplexor **226(1)** comprises the plurality of multiplexing buses **214(1)–214(4)** and **216(1)–216(4)**, a plurality of switches **228(1)–228(8)**, and a control circuit **230(1)**, although the output multiplexor **226** could be constructed of other components. The switches **228(1)–228(*n*)** remain closed at least until the signal(s) from the columns **206(1)–206(*n*)** have changed the bus(es) **214(1)–214(4)** and **216(1)–216(4)** in this particular example. The timing for the output multiplexor **226** is generated via external control (not shown), such an on chip counter, a small shift register, or a controller.

In this particular embodiment, the control circuit **230(1)** (also shown in FIG. 7C) comprises a plurality of AND gates **232(1)–232(4)** which each have a pair of inputs and an output, although other types of components with other numbers of inputs and outputs and other types of logic functions could be used for the control circuit **230**. An address counter **234** transmits input signals to each of the AND gates **232(1)–232(4)**. The output of each AND gate **232(1)–232(4)** is coupled to one of the switches **228(1)–228(8)** and depending upon the signals received via the inputs to the AND gates **232(1)–232(4)**, the signal from the output of the AND gates **232(1)–232(4)** will either open or close the switches **228(1)–228(8)** coupled to the AND gates **232(1)–232(4)**. In this example, the control circuit **230(1)** is used to select the signal from one column **206(1)**, **206(2)**, **206(3)**, or **206(4)** of the pixel array **204** at a time, although the control circuit **230(1)** can be configured with other components and controlled with other input signals to select one or more signals from one or more other columns **206(1)–206(4)** of the pixel array **204** at a time.

In this particular embodiment, a video processing circuit **236** is coupled to the output of the output multiplexor **226**, although other types of processing circuits can also be used. The video processing circuit **236** takes the differential video from the two buses: **214(1)**, **216(1)**; **214(2)**, **216(2)**; **214(3)**, **216(3)**; and **214(4)**, **216(4)**, coupled to the video processing circuit **236** and provides gain, offset, filtering, and/or any other desired processing function in manners well known to those of ordinary skill in the art.

Referring to FIG. **8A**, an imager **202(2)** with a high speed, low noise bus system **200(2)** in accordance with another embodiment of the present invention is illustrated. FIGS. **8A** and **8B** illustrate how this particular embodiment can be utilized to change the native resolution of an imager. Since the imager **202(2)** and bus system **200(2)** in FIG. **8A** is the same as the imager **202(1)** and bus system **200(1)** in FIG. **7A** except for the control circuit **230(2)**, only the control circuit **230(2)** of FIGS. **8A** and **8B** will be described here. In FIGS. **8A** and **8B** the control circuit **230(2)** comprises an address counter **234** with a plurality of inputs and a plurality of outputs along with a plurality of AND gates **238(1)–238(4)** and **240(1)–240(4)** and OR gates **242(1)–242(4)** and **244(1)–244(4)** which each have a pair of inputs and an outputNode **5** is connected to itself. Since control circuits to control the opening and closing of switches are well known to those of ordinary skill in the art, the control circuit **230(2)** will not be described in detail here. In this particular embodiment, the control circuit **230(2)** with the address counter **234**, and interpolation control signal **243**, is configured to interpolate the signals from the columns **206(1)–206(*n*)** of the pixel array **204** as explained in greater detail later. In this example, the address counter **234** transmits input signals to the control circuit **230(2)**. The control circuit **230(2)** is coupled to the switches **228(1)–228(8)** and depending upon the signals received at the inputs to the control circuit **230(2)**, the signals from the control circuit **230(2)** will either open or close the switches **228(1)–228(8)** to provide column interpolation in this example.

Referring to FIGS. **7A–7C**, by pre-selecting the three columns ahead of time, the column processing circuitry only has to drive the multiplexing buses **214(1)–214(4)** and **216(1)–216(4)** at one quarter the actual pixel read rate (one-fourth the bandwidth). Only the demultiplexing in is done at the normal bandwidth. Thus, the column processing circuit, such as the active column sensor technology described in FIGS. **2–4**, can be made smaller and requires less power than it would otherwise have to be. Also, since only one out of every four columns **206** of the pixel array **204** is coupled to each multiplexing bus in this example, each of the multiplexing buses **214(1)–214(4)** and **216(1)–216(4)** has only one-fourth of the capacitance, because there are only one fourth of the switches or transmission gates to drive. Further, with the present invention the column selection sequence remains conventional, with out the need for post processing reconstruction of the original image as is required of multi-port imagers, such as the one shown in FIG. **6**.

Another useful approach to the column parallel nature of the imager **202(1)** with the bus system **200(1)** in accordance with the present invention is the ability to select multiple columns at once to average the video signal. This is possible because the column amplifiers in the processing circuitry for the pixel array **204** are identical in every detail and when more than one is selected at once, the outputs from each amplifier try to drive each other and the result is that the two or more signals are averaged. This allows for higher speed of operation and it also gives a new method of binning or interpolating pixels. Binning is a term used to combine two or more pixel signals together. The higher speed of operation is due to two or more amplifiers driving the same video bus and as a result there is up to two times (or more) the ability to drive the same amount of capacitance. The binning is a result of combining two or more signals at the same time on the same bus **214** or **216**. The control circuit **230(1)** in the output multiplexor **226(1)** can be configured and controlled with signals to couple two pairs of multiplexing buses: **214(1)**, **216(1)**; **214(2)**, **216(2)**; **214(3)**, **216(3)**; and **214(4)**, **216(4)** to the video processing circuit **236** at one time for binning.

This multi-resolution ability of the bus system **200(1)** can also be used to effectively increase the resolution through interpolation, not just decrease the resolution through binning as shown in FIGS. **8A** and **8B**. The imager **202(2)** with the bus system **200(2)** in FIGS. **8A** and **8B** operates in the same manner as the imager **202(1)** with the bus system

200(1) in FIGS. 7A–7C, except that with the control circuit 230(2) in FIGS. 8A and 8B column interpolation is possible. In this embodiment, the increase of resolution is through the use of selectively binning adjacent signals in between reading individual signals with the control circuit 230(2). In this manner, the time sequence would be select the multiplexing buses 214(1) and 216(1) coupled to column 206(1) for coupling via closing switches 228(1) and 228(2) to the video processing circuit 236 and read the signal. Next in sequence leave column 206(1) selected and also select the multiplexing buses 214(2) and 216(2) coupled to column 206(2) via closing switches 228(3) and 228(4) for coupling to the video processing circuit 236. Read the combined (binned or averaged) signal and deselect column 206(1) by opening switches 228(1) and 228(2) to disconnect the multiplexing buses 214(1) and 216(1) coupled to column 206(1) from the video processing circuit 236 and only read the signal from the multiplexing buses 214(2) and 216(2) coupled to column 206(2). In this manner for every two adjacent signals read, a third interpolated signal can be read effectively increasing the resolution through interpolation. By way of example, an imager with a pixel array having 640 columns would have the effective resolution of 1279 pixels through interpolation or an imager with a pixel array having 480 rows would have an interpolated resolution of 969 rows. In either case, for binning or interpolation the column or row averaging is done by the output multiplexor.

Referring to FIG. 9, a bus system 329 with another output multiplexor, control circuit, and video processing block in accordance with another embodiment of the present invention. This bus system 200(3) in FIG. 9 is the same as either the bus system 200(1) shown in FIGS. 7A–7C or the bus system 200(2) shown in FIGS. 8A and 8B, except that this bus system 200(3) also has a reordering multiplexor circuit 330. The reordering circuit 330, is coupled to the output multiplexor circuit 226 of FIG. 9, and is identical in function to the output multiplexer circuit of FIG. 8A. One possible implementation of the reordering circuit 330 is shown in more detail in FIG. 9. More specifcially, in this particular embodiment the reordering circuit 330 is made up of switches implemented as illustrated using transmission gates 332(1–6). The signals provided by the output multiplexer on nodes 226 and 227 can be controlled to be switched to one or more of the video processing block circuits 343(1–3) by the pixel ordering logic device 342. The details of the ordering logic device 342 are not shown here, but would be obvious to one of ordinary skill in the art. The particular implementation of ordering logic device 342 would depend on the specific application and the desired reordering of signals. The function of the control logic provided by the ordering logic device 342 in combination with the reordering multiplexor circuit 330 is to redirect a signal to one or more locations. As signals on nodes 227 and 229 of FIG. 9 can be redirected to one or more of the video amplifiers 342(1–3) of the video processing block 340.

Differential signals are shown on FIGS. 7A, 7B, 7C, 8A, 8B, and 9 which can be described as a signal and a reference signal that are utilized for noise immunity. A single ended configuration or multiple input, output and reording buses could be utilized for an application as well.

Having thus described the basic concept of the invention, it will be rather apparent to those skilled in the art that the foregoing detailed disclosure is intended to be presented by way of example only, and is not limiting. Various alterations, improvements, and modifications will occur and are intended to those skilled in the art, though not expressly stated herein. These alterations, improvements, and modifications are intended to be suggested hereby, and are within the spirit and scope of the invention. Accordingly, the invention is limited only by the following claims and equivalents thereto.

What is claimed is:

1. A bus system for transferring signals from a plurality of signal streams to an output, the bus system comprising:

a plurality of signal buses; and

a control system that couples the signals from two or more of the plurality of signal streams onto two or more one of the plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses before coupling the signals to the output,

wherein the control system provides binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

2. A method for transferring signals comprising:

coupling signals on to two or more of a plurality of signal buses;

allowing the signals to substantially charge each of the two or more of the plurality of signal buses before coupling the signals to an output; and

binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

3. A bus system comprising:

a plurality of signal buses; and

a control system that couples the signals from two or more of a plurality of signal streams onto two or more one of the plurality of signal buses and allows the signals to substantially charge each of the two or more of the plurality of signal buses before coupling the signals to an output,

wherein the control system provides interpolation by coupling the two or more of the signals from the plurality of signal buses to the output separately and between coupling the two or more of the signals from the plurality of signal buses to the output separately, coupling each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time to obtain an interpolated signal.

4. The bus system as set forth in claim 1 wherein one of the plurality of signal buses is coupled to each of the plurality of signal streams.

5. The bus system as set forth in claim 1 wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.

6. The bus system as set forth in claim 1 wherein the control system comprises:

a decoder;

a first control circuit coupled to the decoder; and

a plurality of first switches coupled to the first control circuit, each of the plurality of first switches also being coupled between one of the plurality of signal streams and one of the plurality of signal buses.

7. The bus system as set forth in claim 6 wherein the decoder is a sequential decoder.

8. The bus system as set forth in claim 6 wherein the decoder is a random decoder.

9. The bus system as set forth in claim 6 wherein the control system further comprises:

an address counter coupled to the decoder;

a second control circuit coupled to the address counter; and

a plurality of second switches coupled to the second control circuit, each of the plurality of second switches also being coupled between one of the plurality of signal buses and the output.

10. An imager comprising:

a plurality of streams of signals from a source;

a plurality of signal buses in parallel;

an output; and

a control system that couples the signals from two or more of the plurality of signal streams onto two or more of the plurality of signal buses and allows the signals to substantially charge each of the two or more of the plurality of signal buses before coupling the signals to the output;

wherein the control system provides binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

11. The method as set forth in claim **2** further comprising binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

12. An imager comprising:

a plurality of signal buses; and

a control system that couples the signals from two or more of a plurality of signal streams onto two or more one of the plurality of signal buses and allows the signals to substantially charge each of the two or more of the plurality of signal buses before coupling the signals to an output;

wherein the control system provides interpolation by coupling the two or more of the signals from the plurality of signal buses to the output separately and between coupling the two or more of the signals from the plurality of signal buses to the output separately, coupling each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time to obtain an interpolated signal.

13. The imager as set forth in claim **10** wherein one of the plurality of signal buses is coupled to each of the plurality of signal streams.

14. The imager as set forth in claim **10** wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.

15. The imager as set forth in claim **10** wherein the control system comprises:

a decoder;

a first control circuit coupled to the decoder; and

a plurality of first switches coupled to the first control circuit, each of the plurality of first switches also being coupled between one of the plurality of signal streams and one of the plurality of signal buses.

16. The imager as set forth in claim **15** wherein the decoder is a sequential decoder.

17. The imager as set forth in claim **15** wherein the decoder is a random decoder.

18. The imager as set forth in claim **15** wherein the control system further comprises:

an address counter coupled to the decoder;

a second control circuit coupled to the address counter; and

a plurality of second switches coupled to the second control circuit, each of the plurality of second switches also being coupled between one of the plurality of signal buses and the output.

19. The imager as set forth in claim **10** further comprising a video processing circuit coupled to the output.

20. The imager as set forth in claim **19** wherein the video processing circuit provides differential processing.

21. A bus system for transferring signals from a plurality of signal streams to an output, the bus system comprising:

a plurality of signal buses coupled to the plurality signal streams;

a plurality of first switches, each of the plurality of first switches coupled between one of the plurality of signal streams and one of the plurality of signal buses;

a plurality of second switches, each of the plurality of second switches coupled between one of the plurality of signal buses and the output; and

a control system coupled to the first and second switches, the control system closing two or more of the plurality of first switches to couple signals from the two or more of the plurality of signal streams to two or more of the plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses before closing one or more of the plurality of second switches to couple the signals to the output;

wherein the control system provides binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

22. A method for transferring signals comprising:

coupling signals on to two or more of a plurality of signal buses;

allowing the signals to substantially charge each of the two or more of the plurality of signal buses before coupling the signals to an output; and

interpolating by coupling the two or more of the signals from the plurality of signal buses to the output separately and between coupling the two or more of the signals from the plurality of signal buses to the output separately, coupling each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time to obtain an interpolated signal.

23. A bus system for transferring signals from a plurality of signal streams to an output, the bus system comprising:

a plurality of signal buses coupled to the plurality signal streams;

a plurality of first switches, each of the plurality of first switches coupled between one of the plurality of signal streams and one of the plurality of signal buses;

a plurality of second switches, each of the plurality of second switches coupled between one of the plurality of signal buses and the output; and

a control system coupled to the first and second switches, the control system closing two or more of the plurality of first switches to couple signals from the two or more of the plurality of signal streams to two or more of the plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses before closing one or more of the plurality of second switches to couple the signals to the output;

wherein the control system provides interpolation by coupling the two or more of the signals from the plurality of signal buses to the output separately and between coupling the two or more of the signals from the plurality of signal buses to the output separately coupling each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time to obtain an interpolated signal.

24. The bus system as set forth in claim **21** wherein one of the plurality of signal buses is coupled to each of the plurality of signal streams.

25. The bus system as set forth in claim **21** wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.

26. The bus system as set forth in claim **21** wherein the control system comprises:

a decoder;

a first control circuit coupled to the decoder and the plurality of first switches

an address counter coupled to the decoder; and

a second control circuit coupled to the address counter and to the plurality of second switches.

27. The bus system as set forth in claim **26** wherein the decoder is a sequential decoder.

28. The bus system as set forth in claim **26** wherein the decoder is a random access decoder.

* * * * *

EXHIBIT C

US006590198B1

(12) **United States Patent**
Zarnowski et al.

(10) **Patent No.: US 6,590,198 B1**
(45) **Date of Patent: Jul. 8, 2003**

(54) **VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS**

(75) Inventors: **Jeffrey Zarnowski**, McGraw, NY (US); **Matthew Pace**, Cortland, NY (US); **Thomas Vogelsong**, Jamesville, NY (US); **Michael Joyner**, North Syracuse, NY (US)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/490,374**

(22) Filed: **Jan. 24, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/039,835, filed on Mar. 16, 1998, now Pat. No. 6,084,229.

(51) **Int. Cl.**[7] **H01J 40/14**
(52) **U.S. Cl.** ..... **250/214 LS**; 250/208.1
(58) **Field of Search** ..... 250/227.21, 208.1, 250/208.2, 214 R, 214.1, 214 LS; 348/301–311, 281–283

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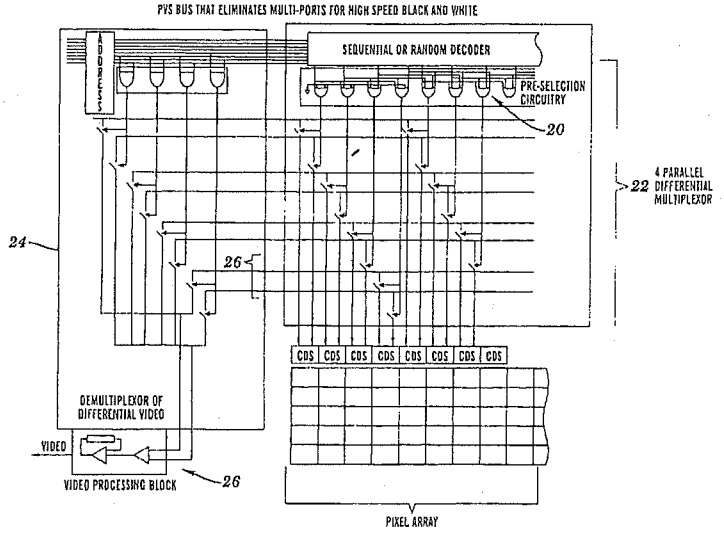
(74) *Attorney, Agent, or Firm*—Nixon Peabody LLP

(57) **ABSTRACT**

An analog video bus architecture that utilizes the column parallel nature of CMOS imagers and more specifically Active Column Sensors, that eliminates the need for multi-port imagers, by increasing the useable bandwidth of single port imagers. An adaptation of this invention allows for either binning or interpolation of pixel information for increased or decreased resolution along the columns and more specifically for ACS imagers binning or interpolation along the rows. In this bus, the single video bus is replaced by multiple video buses and instead of selecting only one column for reading multiple columns are also pre-selected in-order to pre-charge the video bus. The video buses are then de-multiplexed back on to one port at the desired element rate. This architecture utilizes the column oriented video bus of CMOS imagers. It divides the large video bus capacitance by the number of video buses used. In addition, it allows multiple pixel time constants to precharge the video bus. The best commercially available imager designs now claim 40 MHz per analog port and suffer from reduced signal to noise ratios. To overcome this fundamental bandwidth limitation, imager designs in the past have had to increase the number of video ports per imager to achieve high frame rates. Multiple ports per imager breaks the focal plane into segments that are typically reassembled via post processing in a host computer. The other problem with multiple ports is each segment of the imager will have its own offsets and resultant Fixed Pattern Noise (FPN). PVS-Bus™ eliminates the objectionable segmentation and simplifies high-speed system design. Also, by utilizing the column parallel nature of CMOS video buses a method and improved method of using the PVS-Bus of binning and interpolation is described which results in increased frame rate, and for decreased or increased resolution.

17 Claims, 9 Drawing Sheets



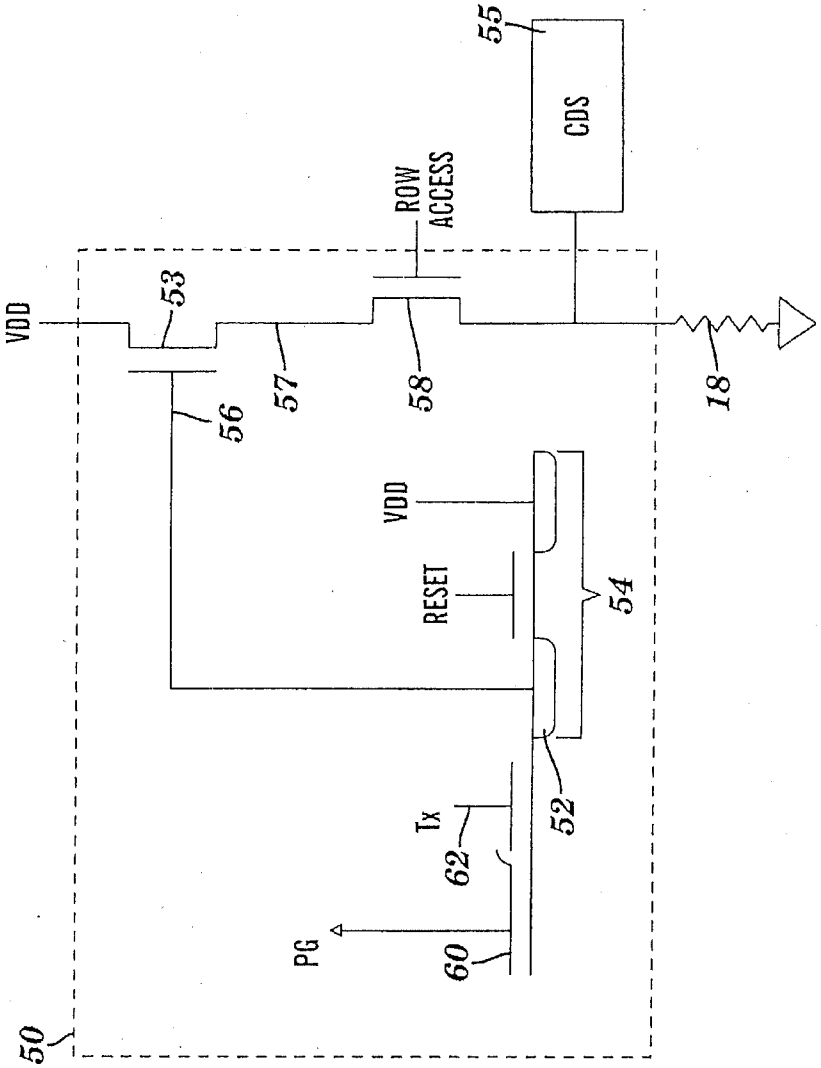


FIG. 1
PRIOR ART

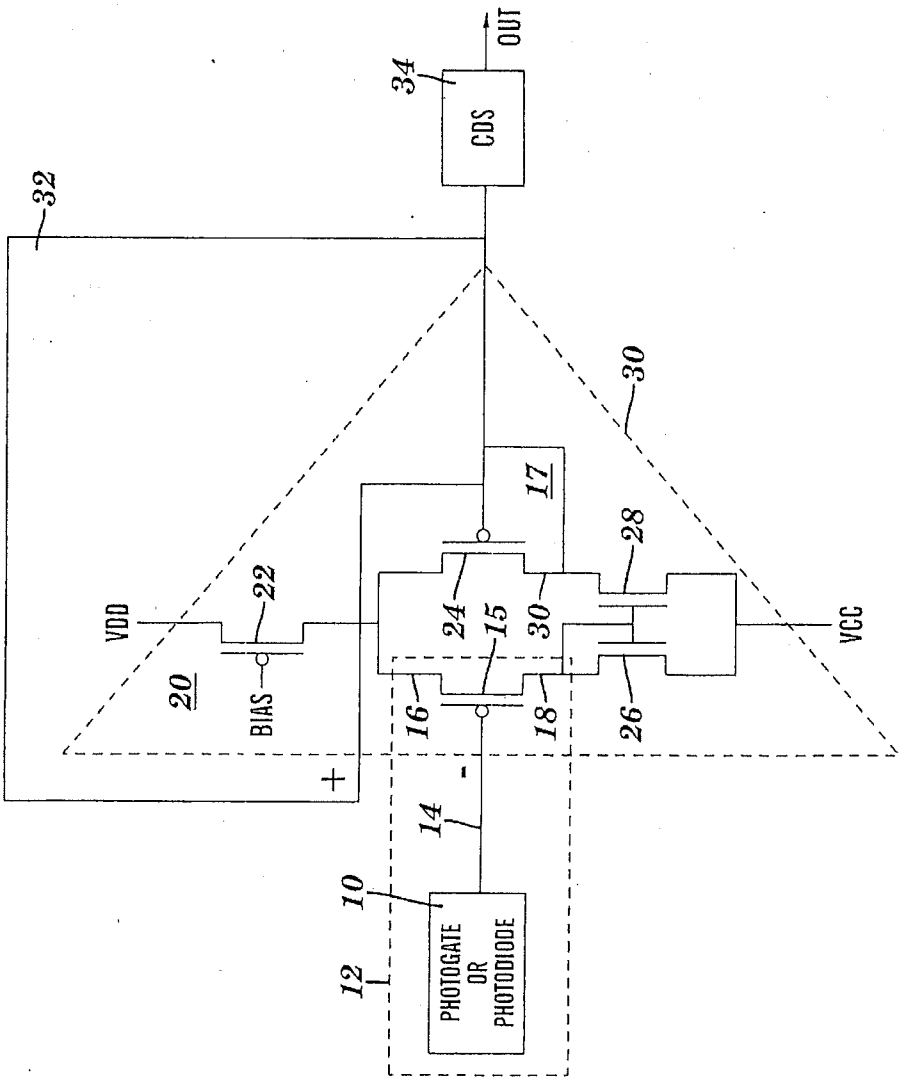

OUT
34
CDS
32
30
17
28
VDD
22
24
15
30
VCC
20
BIAS
16
18
26
+
-
14
10
12
PHOTOGATE
OR
PHOTODIODE

FIG. 2

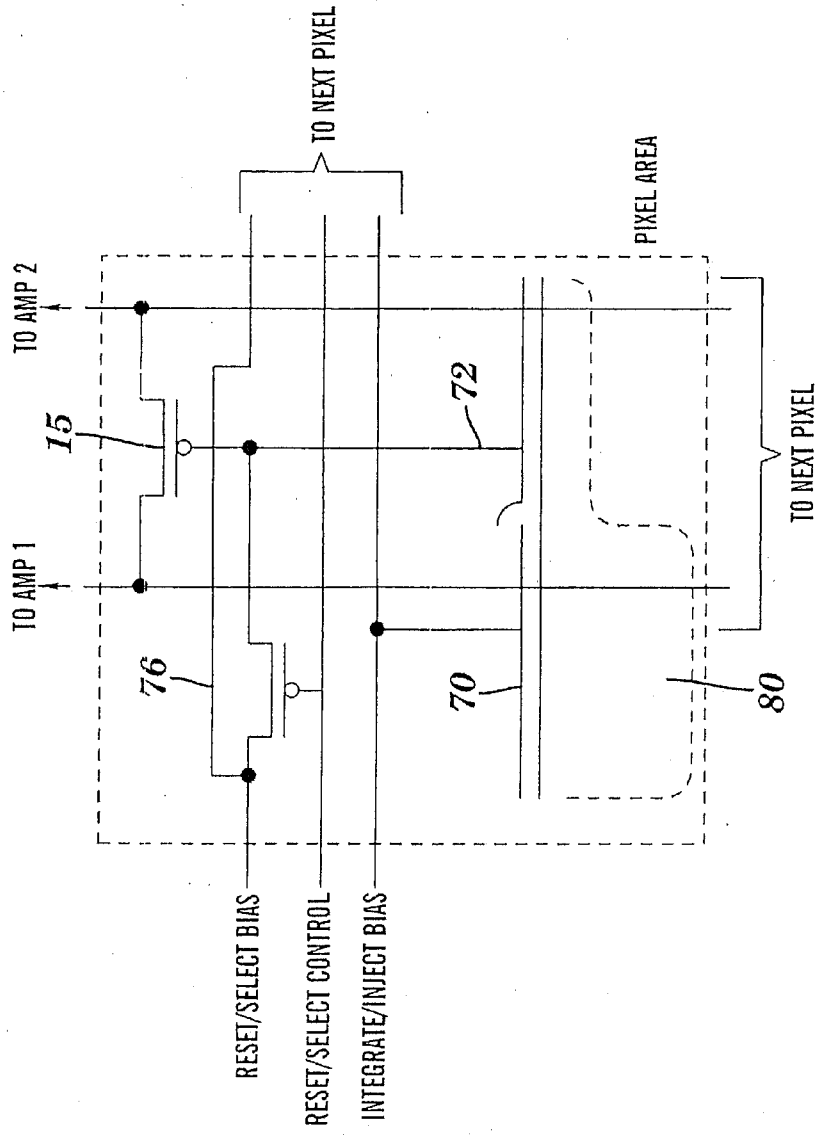

TO NEXT PIXEL
PIXEL AREA
TO AMP 2
15
72
TO NEXT PIXEL
TO AMP 1
76
70
80
RESET/SELECT BIAS
RESET/SELECT CONTROL
INTEGRATE/INJECT BIAS

FIG. 3

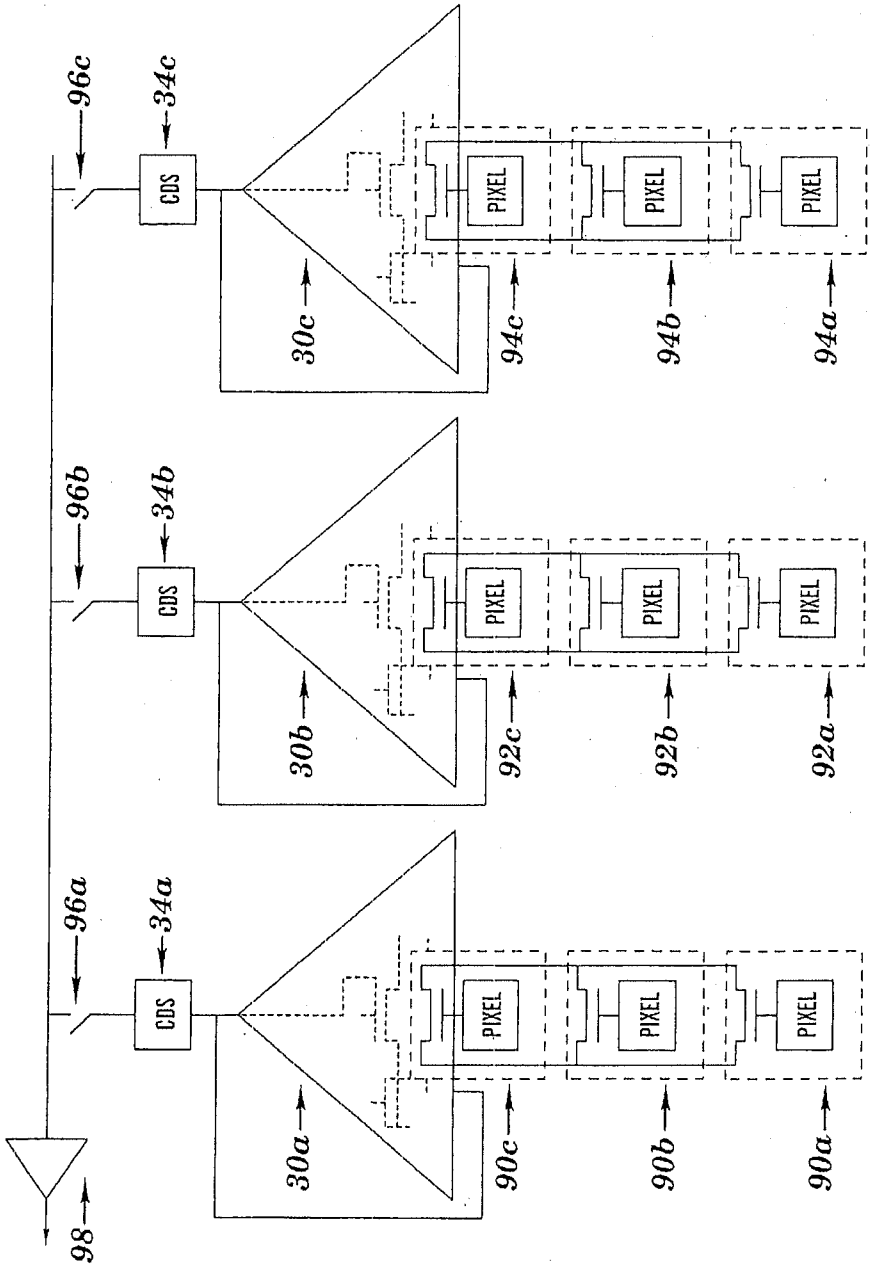

96c
34c
CDS
PIXEL
PIXEL
PIXEL
30c
94c
94b
94a
96b
34b
CDS
PIXEL
PIXEL
PIXEL
30b
92c
92b
92a
96a
34a
CDS
PIXEL
PIXEL
PIXEL
30a
90c
90b
90a
98

FIG. 4

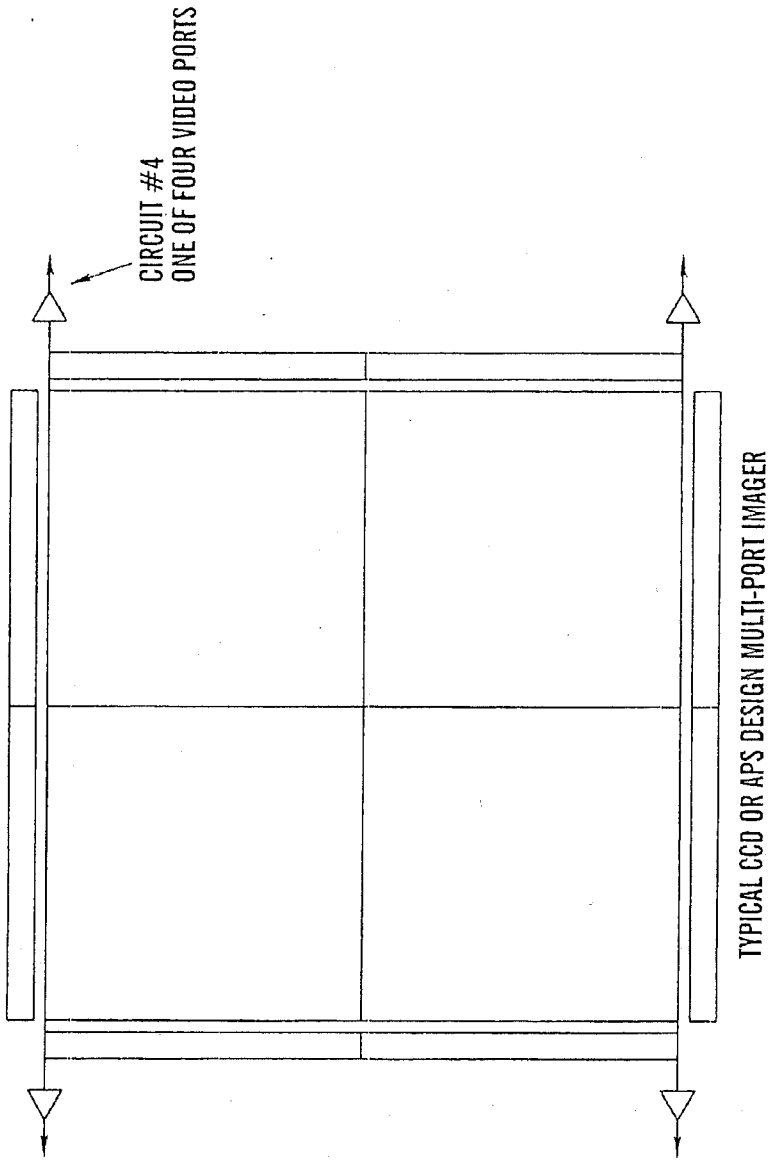

CIRCUIT #4
ONE OF FOUR VIDEO PORTS
TYPICAL CCD OR APS DESIGN MULTI-PORT IMAGER

FIG. 5

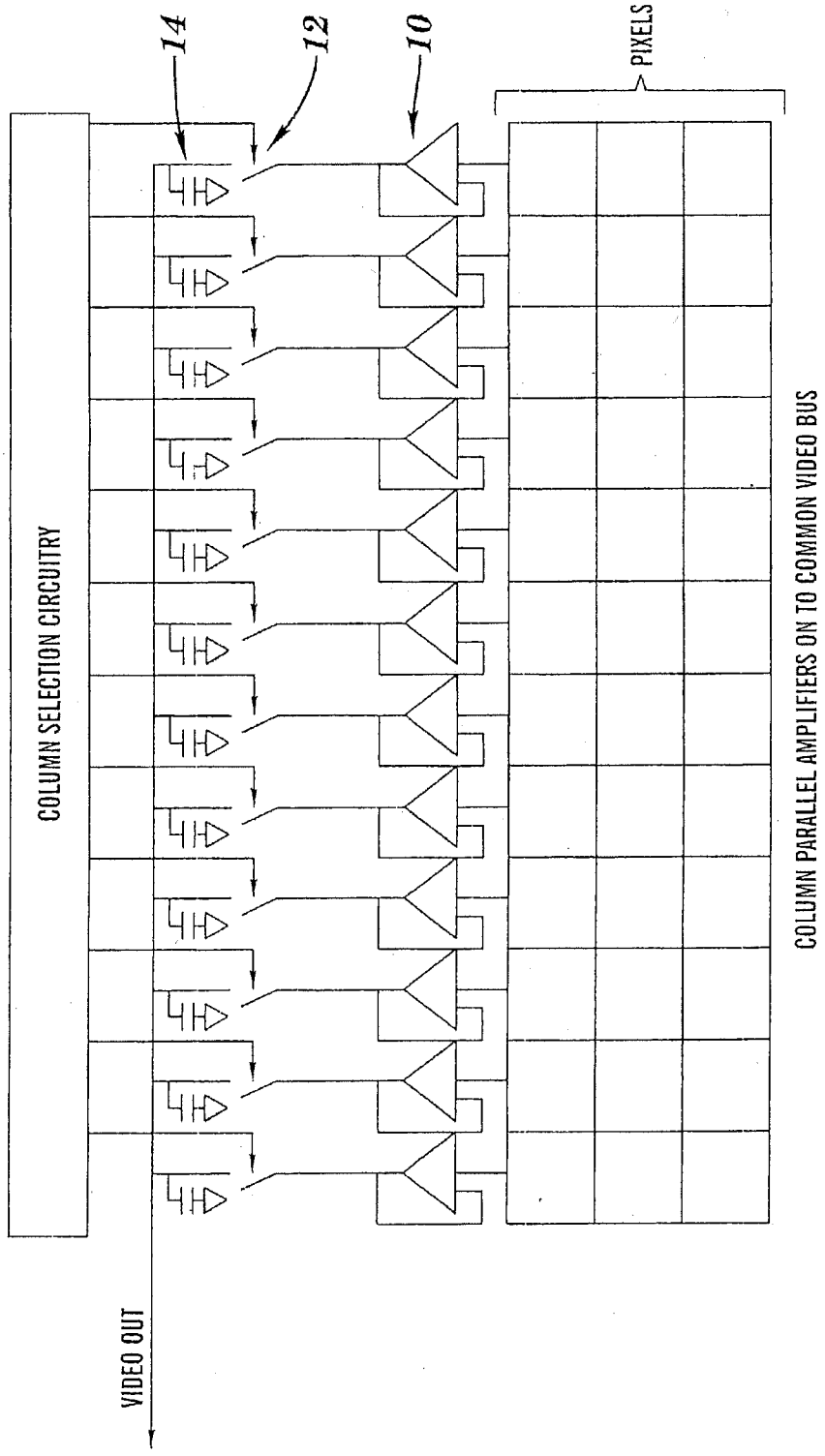

14
12
10
PIXELS
COLUMN SELECTION CIRCUITRY
COLUMN PARALLEL AMPLIFIERS ON TO COMMON VIDEO BUS
VIDEO OUT

FIG. 6

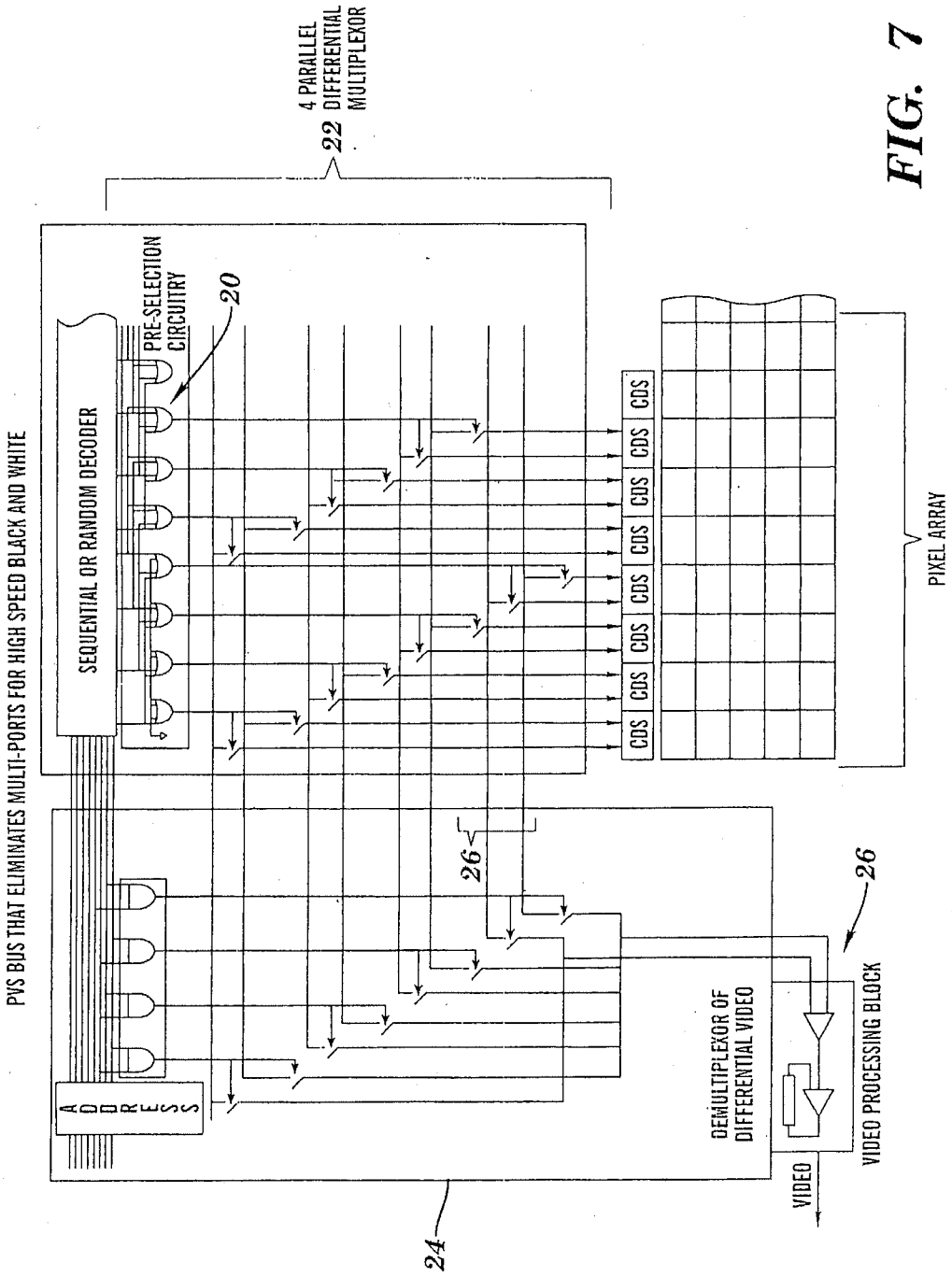

4 PARALLEL DIFFERENTIAL MULTIPLEXOR
22
PRE-SELECTION CIRCUITRY
20
SEQUENTIAL OR RANDOM DECODER
PVS BUS THAT ELIMINATES MULTI-PORTS FOR HIGH SPEED BLACK AND WHITE
CDS
PIXEL ARRAY
26
26
ADDRESS
DEMULTIPLEXOR OF DIFFERENTIAL VIDEO
VIDEO PROCESSING BLOCK
VIDEO
24

FIG. 7

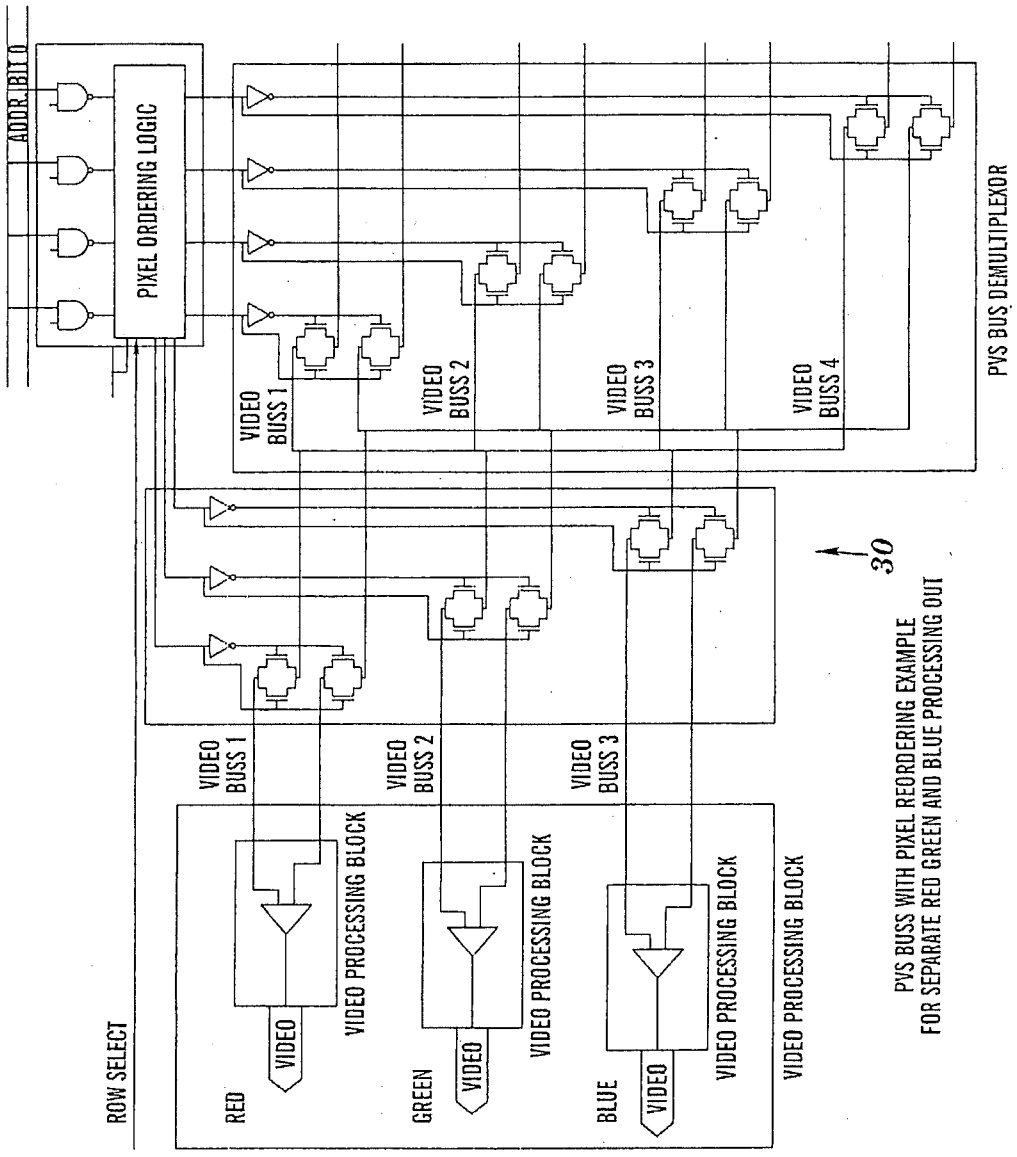

ADDR. BIT 0
PIXEL ORDERING LOGIC
VIDEO BUSS 1
VIDEO BUSS 2
VIDEO BUSS 3
VIDEO BUSS 4
PVS BUS DEMULTIPLEXOR
30
PVS BUSS WITH PIXEL REORDERING EXAMPLE
FOR SEPARATE RED GREEN AND BLUE PROCESSING OUT
VIDEO BUSS 1
VIDEO BUSS 2
VIDEO BUSS 3
ROW SELECT
VIDEO PROCESSING BLOCK
VIDEO PROCESSING BLOCK
VIDEO PROCESSING BLOCK
VIDEO PROCESSING BLOCK
RED
GREEN
BLUE
VIDEO
VIDEO
VIDEO

FIG. 8

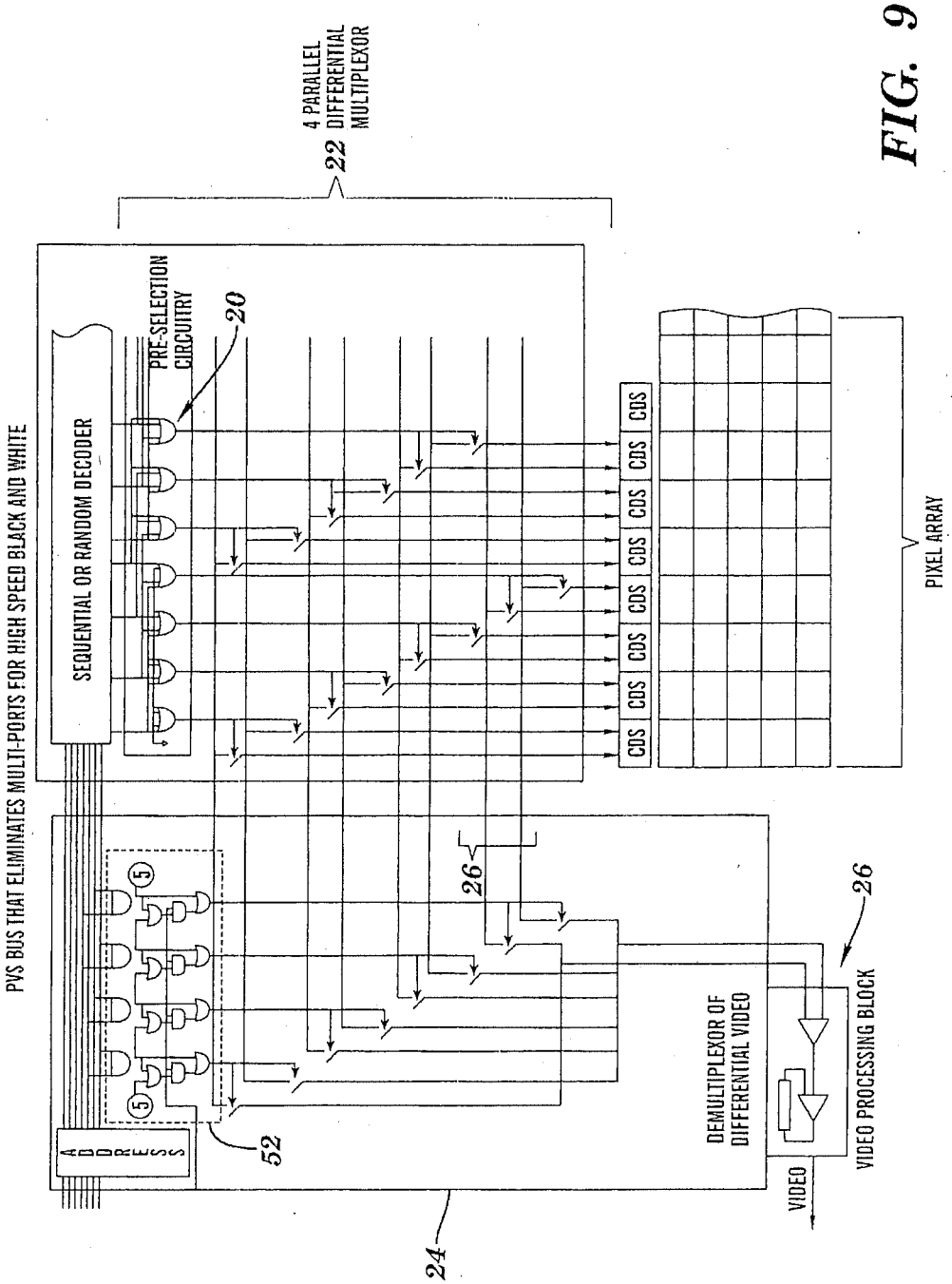

4 PARALLEL DIFFERENTIAL MULTIPLEXOR
22
PRE-SELECTION CIRCUITRY
20
SEQUENTIAL OR RANDOM DECODER
PVS BUS THAT ELIMINATES MULTI-PORTS FOR HIGH SPEED BLACK AND WHITE
CDS
PIXEL ARRAY
26
DEMULTIPLEXOR OF DIFFERENTIAL VIDEO
VIDEO PROCESSING BLOCK
VIDEO
ADDRESS
52
24

FIG. 9

VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION IMAGERS

This application is a continuation-in-part application of application Ser. No. 09/039,835 filed on Mar. 16, 1998, now U.S. Pat. No. 6,084,229.

FIELD OF THE INVENTION

This invention relates generally to busses and, more particularly, to a video bus for high speed multi-resolution imagers.

BACKGROUND OF THE INVENTION

An active pixel is a semiconductor device capable of converting an optical image into an electronic signal. Active pixels can be arranged in a matrix and utilized to generate video signals for video cameras, still photography, or anywhere incident radiation needs to be quantified. When incident radiation interacts with a photosite, charge carriers are liberated and can be collected for sensing. The number of carriers collected in a photosite represents the amount of incident light impinging on the site in a given time-period.

There are two basic devices with many variants, employed to collect and sense, charge carriers in a photosite. The two basic devices are photodiodes and photogates. Variants of photodiodes include, but are not limited to: Pinned, P-I-N, Metal-Semiconductor, Heterojunction, and Avalanche. Photogate structures include: Charge Couple Devices (CCD), Charge Injection Devices (CID) and their variants that include virtual phase, buried channel and other variations that utilize selective dopants. The selective dopants are used to control charge collection and transfer underneath and between the photogate(s) and the sense node.

The solid state imagers heretofore used have been dominated by CCD's because of their low noise as compared to Photodiodes and CIDs. The low noise advantage of CCD imagers is the result of collecting the photon generated charge at the pixel site and then coupling or shifting the actual charge to an amplifier at the periphery of the array. This eliminates the need for the long polysilicon and metal busses that degrade the signal with their associated resistance and capacitance. However, the low noise of the CCD requires the imager to be read in a fixed format and once the charge is read it is destroyed. The requirement of coupling the collected photon charge from the pixel to the periphery amplifier (a.k.a. CTE), requires proprietary processing steps not compatible with industry standards CMOS or BiCMOS processes.

Solid state imaging devices have developed in parallel with CMOS technology and as a result all imager manufacturers developed their own proprietary processes to maximize imager performance characteristics and wafer yield. Specialized silicon wafer processing kept imager prices relatively high. Linear active pixel sensors have been commercially produced since 1985. Beginning in the early 90's the move to transfer the proprietary processes to an industry standard CMOS processes was on. The advantages of using an industry standard process include: competitive wafer processing pricing, and the ability to provide on chip timing, control and processing electronics. By the end of the year 1992 a 512x512 CMOS compatible, CID imager with a preamplifier and CDS per column had been fabricated. The imager could either be operated as a random access 512x512 CID, or all the columns could be summed together and operated as a linear active pixel sensor.

Area arrays utilizing active pixel sensors in which a photodiode or photogate is coupled to an output source follower amplifier which in turn drives a Correlated Double Sampling (CDS) circuit, where the two outputs of the CDS cell then drives two more source followers circuits that in turn are fed into a differential amplifier are shown in U.S. Pat. No. 5,471,515. This uses source follower circuits, that typically have gains less than unity that vary from one source follower to another. The source follower gain variation is due to variations of FET thresholds. The source follower gain variation results in a pixel to pixel gain mismatch. Also, the active pixel sensors suffer gain variations due to the CDS circuit per column, when the CDS employs a source follower pair to drive its output. The resulting CDS signal and its corresponding offset can have different gains that are not correctable by the differential amplifier. Also, the source follower configuration of active pixel doesn't allow for binning of pixels.

The voltage mode of operation of prior art does not allow for binning, which, is the summation to two or more pixel signals at once.

What is needed is an imager device which has the low noise level of a CCD, the random access, and binning of a CID, and uniform gain and response from all pixels.

Conventional Approaches to Industrial/Scientific Cameras

The CCD sensor and camera electronics technology has evolved over the last 30 years to meet most of these demands. However the resulting cameras require a state-of-the-art, large pixel, multi-port CCD chip plus several extra chips and usually several circuit boards filled with electronics to accomplish this. Thus, the cameras cannot physically fit in certain applications, the power consumed is significant, and last but not least, the resulting cameras are far too expensive for many applications. The necessary recombination of the video data from several ports, further increases the video processing complexity and ultimately drives-up the cost and size of the video system.

Over the past several years, thanks to design rule shrinkage, image sensors using sub-micron CMOS process technology have become practical. By using CMOS technology for the sensor array itself, the problem of integrating extra circuitry on chip becomes straightforward. Elements such as A/D converters, timing generators, control circuitry and interface circuitry can easily be added. In addition, the operation of CMOS imagers is simplified by the elimination of the need for precise timing and level control of multiple clock required to drive the large capacitance transfer gates inherent in CCD's. Even with all of these factors, including the exceptional speed and pico-second gate delays of sub-micron processes, the analog video bandwidth per port hasn't changed much over the past 20 years.

Active pixel sensors (APS) have been proposed as the means to achieve the flexible benefits of CMOS cameras on a chip. Unfortunately, there are performance issues with the fundamental APS approach that limit its performance and functionality. While these limitations may be acceptable for consumer imaging applications, the demands of scientific and industrial applications have, up until now, been largely unmet by CMOS image sensors.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a prior art double polysilicon active pixel sensor;

FIG. 2 is an active column sensor in accordance with this invention;

FIG. 3 is an implementation of a pixel in accordance with the invention;

FIG. 4 is a schematic illustration of a matrix of pixels connected to incorporate a full operational amplifier per pixel forming an Active Column Sensor;

FIG. 5 is a view of a traditional CCD and CMOS sensor method of increasing video bandwidth with multiple ports;

FIG. 6 is a view of a conventional method of driving a common video buss on an imager;

FIG. 7 is a view of a high speed low noise video bus;

FIG. 8 is a view of a bus for pixel reordering with a video processing block and a bus demultiplexor;

FIG. 9 is a view of a bus for pixel interpolation for increased resolution; and

FIG. 10 is a photograph of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Before discussing the Active Column Sensor (ACS) circuit of FIG. 2 of the present invention and described in conjunction with a discussion of ACS below, it will be useful to discuss the structure of a typical double-polysilicon active pixel sensor of prior art as shown in FIG. 1.

In FIG. 1 each pixel 50 has a photosite 60 that has an output FET 53 configured as a source follower. The source follower 53 is used to drive a subsequent signal conditioning circuitry, such as a Correlated Double Sampled Circuit (CDS) 55. The gain through a source follower 53 is less than unity. If the source follower located at the pixel site 50 has a given gain other pixels and their respective source followers in the same column may or may not have the same gain. The technique relies on wafer processing for all FETs in the array to have the same threshold. It isn't uncommon for FET thresholds, during operation, to vary by 100 mV for a linear active pixel array.

The active pixel 50 of the prior art includes a photogate 60 and a transfer gate 62 that are used to couple photo generated charge onto the floating diffusion node 52 which is connected to the gate 56 of source follower 53. The drain of the output FET 53 is connected directly to a power supply rail VDD. The source follower output FET is in turn connected to the source 57 of row access FET 58. When the row access FET 58 is selected for reading, the FET 58 is turned on, allowing output FET 53 to be connected to a load 18 and drive the CDS circuitry 55 directly.

FIG. 2 is a schematic diagram of a pixel 12 in accordance with the present invention in which the threshold variations from pixel to pixel of the prior art are eliminated. All pixels 12 in a row or column are in parallel and for simplicity only one is shown. Pixel 12 which can consist of any photosensitive device 10 is coupled to an FET 15 to isolate the pixel from the readout circuitry. The FET 15 is one FET of a differential input pair of an operational amplifier 30 that includes FET 24. For simplicity, in FIG. 2 the amplifier circuit 30 is configured as a positive feedback unity gain amplifier. A feedback path 32 connects the output of amplifier 30 to input 17 which in this case is the gate of FET 24. The amplifier 30 could be configured to have gain, a full differential input or any operational amplifier configuration as the application required. The fixed gain of amplifier 30 eliminates the gain variability of the prior art. The output of the unity gain amplifier is connected to a Correlated Double Sampler (CDS) which is utilized to eliminate any fixed pattern noise in the video.

A current source 20 comprising an FET 22 has its source connected to a power source VDD and its drain connected to the sources of differential input FETs 15 and 24.

The drains of input FETs 15 and 24 are connected to a current mirror formed from FETs 26 and 28. The gates of FETs 26 and 28 are connected together and to the source 18 of input FET 15. The sources of FETs 26 and 28 are connected to a negative power source, VCC.

The drain 30 of FET 24 is the output of the differential pair and is connected to CDS 34.

The input FET 15 could be either a N channel or P channel FET as the application requires. The pixel 80 could be either a photogate or photodiode.

FIG. 3 is a detailed schematic of pixel 12 of the active column sensor shown in FIG. 2. In this implementation a photogate 76 is utilized. Selection and reset of a sense node 72 is controlled by an FET 76. This Active Column Sensor pixel eliminates the separate selection/access FET 58 of prior art. All biasing and controls signals are supplied from the periphery of the pixel array.

The pixel can be operated in the following manner. An N type substrate is used and the substrate is biased the most positive potential, e.g. 5.0 volts. The photogate 70 preferably a layer of polysilicon is biased to an integrate level (e.g. 0.0 volts). The region 80 under the photogate 70 is depleted and as light strikes the immediate area, it will collect (integrate) photon generated carriers. Photogate 72 is been biased to the 5.0 volts and will not collect photon generated carriers during the integration because it is biased to the same potential as the substrate. Photogate 72 is biased by selecting control FET 76 with the reset/Select Control signal. In this configuration control FET 76 is a P channel FET that is selected by a negative signal relative to the substrate, for example 0.0 volts. During integration FET 76 is selected, the photogate is biased by the reset/select bias that preferably is at 5.0 volts. After a predetermined integration time period the pixel is read.

Reading the pixel is preferably accomplished in the following manner. The reset/select control is changed to 2.5 volts, causing the region beneath photogate 72 to be depleted, and the background level is read. Reset/select FET 76 is turned off by setting the reset/select control to 5.0 volts. Photogate 70 has its potential removed, and in this example 5.00 volts. Reading the signal will occur as the collected photon generated charge transfers from the region beneath photogate 70 to the region beneath photogate 72. The transferred photon generated charge modulates the gate of input FET 15, according to the amount of collected.

Fixed Pattern Noise (FPN) can be eliminated from the video information by utilizing CDS circuit 34. The first sample applied to the CDS circuit is the background level. The signal information is then applied to the CDS. The difference of the two signals provides for a fixed pattern noise free signal.

FIG. 4 is a schematic diagram of an array of pixels in accordance with this invention. A plurality of pixels 90*a*, 90*b*, 90*c* form a first column of the array, and similar columns 92*a–c* and 94*a–c* complete the array. Within each column, the pixels are connected with their output FETs in parallel, the combination forming the first one of the differential input pair of operational amplifier 30. In all other respects, amplifiers 30*a*, 30*b* and 30*c* are identical to FIG. 2. Each amplifier 30 is connected to a CDS 34*a*, 34*b*, and 34*c* respectively. The outputs of CDS 34*a, b, c* are connected through column select switches 96*a*, 96*b*, and 96*c*, the common terminals of which are connected to output buffer 98 which can be a source follower, or a more complex signal conditioner as required by the specific application.

Industrial and scientific imaging applications require much higher performance and functionality than that

required for consumer imaging products. Typical applications of this class of cameras include machine vision for automated inspection. Many of the applications require high readout speeds for video rate or even faster imaging without sacrificing image quality. In addition to image quality, the applications have come to demand greater functionality in the camera. Features such as flexible shuttering and electronic zoom, random access and selectable region of interest for maximizing frame rates and minimizing data storage (especially useful in tracking applications). Lowering the cost of machine system development is the recent advancement of single chip CMOS cameras. Newly developed CMOS cameras have all the flexibility previously listed; however, the analog video bandwidth per port hasn't changed from the traditional CCD, CID or Photodiode technologies. This invention relates to high speed video bus requirements in general and more specifically to solid state imagers.

The following section describes one embodiment of an on-board, high-speed bus that allows pixel rates exceeding those of single port CCD or APS devices in accordance with the present invention. This bus in combination with the highly parallel nature of amplifier per column techniques of CMOS sensors that provides both the functionality and high speed performance required for scientific and industrial applications. Experimental results of one embodiment of the present invention are also presented.

1. Conventional Video Bus Issues

Most mega-pixel image sensors, including both CCD imagers and APS imagers, have a maximum pixel rate inadequate to meet the frame rate needs of industrial and scientific imaging. CCD devices are limited by both clocking rates and the speeds of the Correlated Double Sampled (CDS) circuitry. In addition the higher amplifier bandwidth required for higher pixel rates increases noise levels. With the column parallel nature of CMOS imagers, the amplifier and CDS can be run at the line rate rather than the pixel rate. The video bandwidth constraints come in terms of the multiplexing speed. CMOS imagers typically multiplex their signals onto a common analog video bus. The more signals that are multiplexed or switched onto the bus, the greater the capacitive load of that bus. Therefore, as more signals are connected to the bus, the bandwidth of the bus is reduced. Alternatively, greater power is needed to charge and discharge the bus with its associated capacitance to maintain bandwidth. In order to overcome the constraints, designers of CCD's and APS sensors have resorted to dividing up the imager into halves, quarters, or smaller groupings of sub-imagers, jammed together. The signal from each of these sub-imagers is brought out to its own port, as shown in FIG. **5**. Circuit **2** of FIG. **5** is a video port that is replicated four times in this example. This approach has been used to provide high frame rate devices, or even to meet standard frame rates with large mega-pixel imagers. This adds system size, complexity, power and cost to handle the multiple analog amplifier chains. In addition, it is an extremely challenging task to balance the amplifier chains completely over all possible pixel rates and temperatures. This issue has become even more of a problem in recent years as imagers have grown larger, now up to full wafer size. The process variations across an array can lead to further balance problems, and even variations in noise characteristics, due to process variations across a wafer.

Often CMOS imagers have column parallel amplifiers that drive a common video bus. The common video bus is seen mostly as a capacitive load to each individual column amplifier as shown in FIG. **6**, circuit **14**. In order for each amplifier to truly represent the pixel value onto the common video bus, the amplifier must charge or discharge the bus with in one pixel time constant. It must be stable long enough for a sample and hold circuit (or similar) to accurately present the resultant signal to an A to D converter. A conservative engineer will want at least 5τ (tau or time constants) to accurately allow the video bus to settle the video value presented by each individual column amplifier. At higher video bus speeds the individual column amplifier, FIG. **6**, circuit **10**, is unable to properly charge or discharge the video bus and results in a loss of contrast ratio. At higher pixel element rates where the contrast ratio is compromised, the individual column amplifier characteristic and the video switch characteristics begin to affect the resultant video. The individual column amplifiers will have slightly different offsets, FIG. **6**, circuit **10**, with slightly different drive capabilities and each video switch, FIG. **6**, circuit **12**, will have slightly different resistances and slightly different thresholds. This combination of column amplifier and video switch characteristics results in each column amplifier having different time constants relative to charging and discharging the video bus. The column amplifier and video switch are common to every pixel in that column. Thus, variations in the video switch characteristics result in what appears to be column based Fixed Pattern Noise (FPN). As more columns are added, each video switch adds more associated capacitance, FIG. **6**, circuit **14**, due to the source and drain junctions of MOSFET or Bipolar transistors. The more columns added to the bus, the higher the total capacitance. Having identified the source of column based FPN and knowing that the pixel element rates cannot exceed the ability of the weakest column amplifier on the video bus a solution should be identifiable, without requiring high power amplifiers per column.

2. High Speed PVS Bus

A preferred approach over the segmented four port imager of FIG. **5**, would be to read out the imager four times faster on a single port. The ACS series of imagers incorporates a novel method of increasing the read rate of analog buses called the PVS bus. This speed increase has been achieved without increasing power consumption, and full video bandwidth is maintained even at the higher speeds. Common mode noise pickup is eliminated through the use of fully differential processing.

The high speed, low noise, low power analog PVS bus for imagers as shown in FIG. **7** utilizes either standard sequential or random access decoders for selection of a particular column. In addition to selecting that column, it has the added preselection circuitry to pre-select the next three columns in the read sequence in parallel. The number of columns pre-selected can be scaled to meet the application requirements; four buses are used in FIG. **7** for illustration purposes only. Preselection, circuitry **20** of FIG. **7** is effectively a four input "or" Boolean logic function. Now instead of having separate quadrants of pixels as in FIG. **5**, there is only now only one. Preselection circuitry works in conjunction with parallel multiplexors, where the four columns are selected in parallel and are multiplexed to a separate differential video bus, FIG. **7**, circuit **26**, for each column selected. Parallel multiplexors, Circuit **22**, FIG. **7**. as shown in FIG. **7**, circuit **26** utilizes differential video per column and has two video buses for each column address. Therefore the total number of video buses is eight for FIG. **7**.

The purpose of selecting the current column and pre-selecting the next three columns is to allow the video bus to charge up to the proper value and settle prior to being demultplexed by circuit **24** as shown in FIG. **7**. By pre-

selecting the three columns (or pixel time constants) ahead of time, the column video processing circuitry only has to drive the video bus at one quarter the actual pixel read rate (one-fourth the bandwidth) and therefore can be made smaller and lower power than they would otherwise have to be. Also, since each column is connected to only one out of every four columns the video bus has only one-fourth of the capacitance, because there are only one fourth of the transmission gates (or switches) to drive. As a result, each column selected also pre-selects the next three columns in sequence. The column selection sequence remains conventional, with out the need for post processing reconstruction of the original image required of multi-port imagers. The analog pre-charging is done at a one-fourth the bandwidth in FIG. **7** than the prior art conventional single ended video bus and only the demultiplexing is done at the normal bandwidth.

The demultiplexor of FIG. **7**, **24** is a fully differential video bus designed to match the fully differential multiplexor of FIG. **7**, circuit **26**. Parallel multiplexors isolate all the different video buses. The timing for the demultiplexor circuit is generated via external control, an on chip counter, a small shift register, or a controller. The demultiplexor timing control logic which in the implementation shown, is a counter with count decode logic. The video processing block that takes the differential video, provides gain, offset, filtering, or any video processing function. The demultiplexor timing control logic may decode the video bus circuit in any sequence that the application requires.

By utilizing the highly parallel nature of CMOS imagers and more specifically the fully differential video provided by the Active Column Sensor(ACS patent approved) technology, the PVS Bus is able to maintain near ideal MTF with high video bandwidths. The parallel nature of the PVS Bus also allows pixel reordering as shown in FIG. **8**, circuit **30**. Pixel reordering can be column and/or row based. An example of row and column based reordering is the Bayer (or other) color filter. FIG. **8** illustrates how the PVS Bus demultiplexor can go to another demultiplexor to reorder pixels as columns are read. The manner that the pixels are reordered can be row dependent, as is the case for color filters.

3. Combining Columns

Another useful approach to the column parallel nature of CMOS imagers is the ability to select multiple columns at once to average the video signal. This is possible because the column amplifiers of FIG. **6**, circuit **10** are identical in every detail and when more than one is selected at once the outputs from each amplifier try to drive each other and the result is that the two or more signals are averaged. This allows for higher speed of operation and it also gives a new method of binning or interpolating pixels. Binning is a term used to combine two or more pixel signals together. The higher speed of operation is due to two or more amplifiers driving the same video bus and as a result there is up to two times (or more) the ability to drive the same amount of capacitance. The binning is a result of combining two or more signals at the same time on the same video bus. The net result of combining multiple signals (a.k.a. averaging) onto the same bus is to effectively a multi-resolution imager.

This multi-resolution ability of the video bus can be used to effectively increase the resolution, through interpolation, not just decrease the resolution through binning. The increase of resolution is through the use of selectively binning adjacent signals in between reading individual signals. In this manner, the time sequence would be for a conventional column orientated CMOS video bus, as in FIG. **6**, would be select column **1** and read the signal. Next in sequence leave column **1** selected and also select column **2**. Read the combined (binned or averaged) signal and deselect column **1** and now only read column **2** signal. In this manner for every two adjacent signals read, a third interpolated signal can be read effectively increasing the resolution through interpolation. This allows a typical imager with 640 columns to have the effective resolution of 1279 pixels through interpolation.

4. Row Binning

The ACS series of imagers has been developed specifically for scientific and industrial applications and utilizes a bus in accordance with the present invention. The design incorporates the Active Column Sensor design approach that uses a unity gain amplifier per column with a selectable input transistor at every pixel along that column. An ACS technology imager will uniquely allow binning or interpolation along the row in a similar manner as the columns were just described above. The ability to bin (or average) is described in the ACS imager patent. Interpolation that the ACS technology uniquely allows, would utilize the just described method in the previous paragraph for the first row of video. The ACS imager would then select two adjacent rows of video (rows **1** and **2**) and the above interpolation would be repeated and followed again by only selecting row **2** and rereading only row **2**. In this manner a typical imager with 480 rows, can have an interpolated resolution of 959 rows.

What has just been described in the previous two paragraphs can be done at a much higher rate with the bus in accordance with the present invention described herein. Utilizing the PVS Bus where the current pixel being read and the next three(or more) pixels are pre-selected and pre-charging the remaining video buses in parallel, the column(pixel) averaging is done by the demultiplexor. Where the demultiplexor of FIG. **7**, circuit **24**, is used to select adjacent pixels at the same time. FIG. **9** illustrates in circuit **52** how simple the added circuitry can be to allow column to column interpolation.

While the invention has been described in connection with a presently preferred embodiment thereof, many modifications and changes may be apparent to those skilled in the art without departing from the true spirit and scope of the invention, which is intended to be defined solely by the appended claims.

What is claimed is:

1. A bus system for transferring signals from a plurality of signal streams to an output, the bus system comprising:

a plurality of signal buses in parallel, each of the plurality of signal buses is coupled to the output;

a plurality of first switches, each of the plurality of first switches is coupled between one of the plurality of signal streams and one of the plurality of signal buses; and

a control system coupled to each of the first plurality of switches, the control system controls when at least one of the first plurality of switches is closed to allow the signal from one of the plurality of signal streams coupled to the closed one of the first plurality of switches to substantially charge one of the plurality of signal buses which is also coupled to the closed one of the first plurality of switches and which is not currently being read at the output.

2. The bus system as set forth in claim **1** wherein the control system controls when at least another one of the first plurality of switches is closed to allow the signal from another one of the plurality of signal streams coupled to the closed another one of the first plurality of switches to be read

at the output from another one of the plurality of signal buses which is also coupled to the closed another one of the first plurality of switches.

3. The bus system as set forth in claim 1 further comprising a plurality of second switches, each of the plurality of second switches is coupled between one of the plurality of signal buses and the output, the control system controls when each of the of the plurality of second switches is closed to allow the signal on one or more of the plurality of signal buses to be read at the output.

4. The bus system as set forth in claim 1 wherein the control system provides binning by coupling the signals from two or more of the plurality of signals buses to be read at the output at substantially the same time to average the signals together.

5. The bus system as set forth in claim 1 wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.

6. The bus system as set forth in claim 1 wherein the control system further comprises:

a decoder; and

a first control circuit coupled between the decoder and each of the first plurality of switches.

7. The bus system as set forth in claim 6 wherein the decoder is a sequential decoder.

8. The bus system as set forth in claim 6 wherein the decoder is a random decoder.

9. The bus system as set forth in claim 6 wherein the control system further comprises:

an address counter coupled to the decoder; and

a second control circuit coupled between the address counter and each of the second plurality of switches.

10. A method for transferring signals from a plurality of signal streams to an output, the method comprising:

reading at least one of the signals at an output from at least one of a plurality of signal buses, each of the plurality of signal buses is coupled to the output;

allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses that is not being read at the output while the one of the signals is being read; and

reading the at least another one of the signals at the output after the at least another one of the plurality of signal buses is substantially charged with the another one of the signals.

11. The method as set forth in claim 10 further comprising controlling when each of the plurality of signal buses is charged with one of the signals.

12. The method as set forth in claim 10 further comprising controlling when the reading at the output from each of the plurality of signal buses occurs.

13. The method as set forth in claim 10 wherein the reading at least one of the signals comprises binning the signals from two or more of the plurality of signals buses together to be read at the output at substantially the same time to average the signals together.

14. The method as set forth in claim 10 wherein the reading further comprises differential processing of the signals read from a pair of the plurality of signal buses, wherein each of the pair of the plurality of signal buses are coupled to one of the plurality of signal streams.

15. The method as set forth in claim 10 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals in a sequential order.

16. The method as set forth in claim 10 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals in a random order.

17. The method as set forth in claim 10 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals at substantially the same time.

* * * * *

EXHIBIT D

US007057150B2

(12) **United States Patent**
Zarnowski et al.

(10) **Patent No.: US 7,057,150 B2**
(45) **Date of Patent: Jun. 6, 2006**

(54) **SOLID STATE IMAGER WITH REDUCED NUMBER OF TRANSISTORS PER PIXEL**

(75) Inventors: **Jeffrey J. Zarnowski**, McGraw, NY (US); **Samuel D. Ambalavanar**, Rochester, NY (US); **Michael E. Joyner**, Cortland, NY (US); **Ketan V. Karia**, Cortland, NY (US)

(73) Assignee: **Panavision Imaging LLC**, New York, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 296 days.

(21) Appl. No.: **10/673,591**

(22) Filed: **Sep. 29, 2003**

(65) **Prior Publication Data**

US 2004/0069930 A1 Apr. 15, 2004

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/768,124, filed on Jan. 23, 2001, now Pat. No. 6,633,029, which is a continuation-in-part of application No. 09/490,374, filed on Jan. 24, 2000, now Pat. No. 6,590,198, which is a continuation-in-part of application No. 09/039,835, filed on Mar. 16, 1998, now Pat. No. 6,084,229.

(51) **Int. Cl.**
H01J 40/14 (2006.01)

(52) **U.S. Cl.** ..... **250/214 R**; 250/208.1

(58) **Field of Classification Search** ..... 250/214 R, 250/208.1
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,898,168 A * 4/1999 Gowda et al. 250/208.1

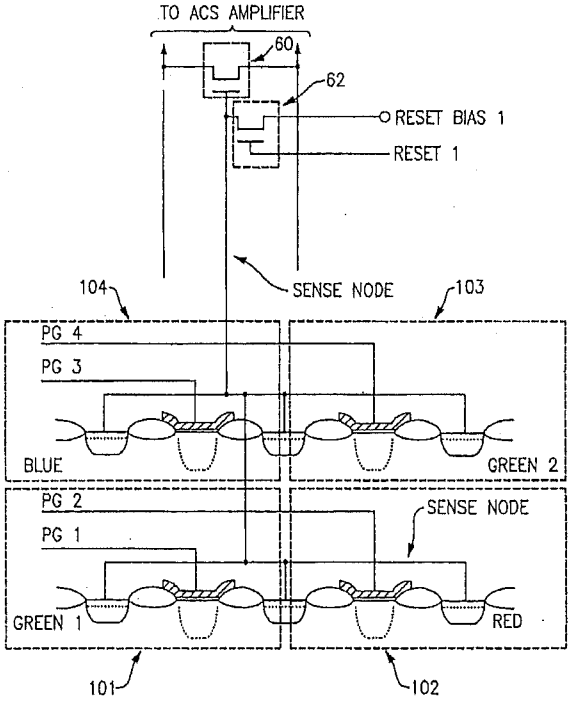
* cited by examiner

Primary Examiner—Que T. Le
(74) *Attorney, Agent, or Firm*—Bernhard P. Molldrem, Jr.

(57) **ABSTRACT**

A solid state imager with pixels arranged in columns and rows has the pixels are configured into groups of at least a first pixel and a second pixel, each said group sharing a pixel output transistor having a sense electrode and an output electrode and a reset transistor having a gate coupled to receive a reset signal and an output coupled to the sense electrode of the associated shared pixel output transistor. Each of the pixels has a photosensitive element whose output electrode is coupled to the sense electrode of the shared pixel output transistor and a gate electrode coupled to receive respective first and second pixel gating signals. This configuration reduces the number of FETs to two transistors for each pair of pixels, and also can achieve true correlated double sampling correction of FPN.

18 Claims, 6 Drawing Sheets



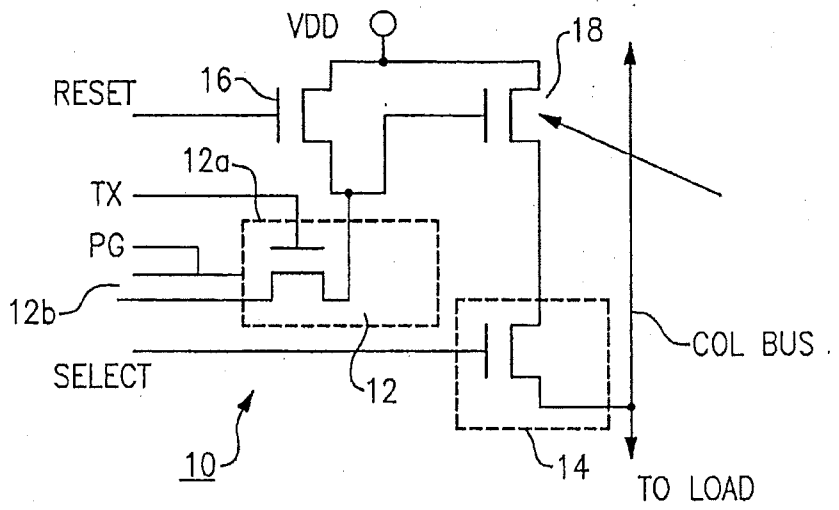


FIG.1
Prior Art

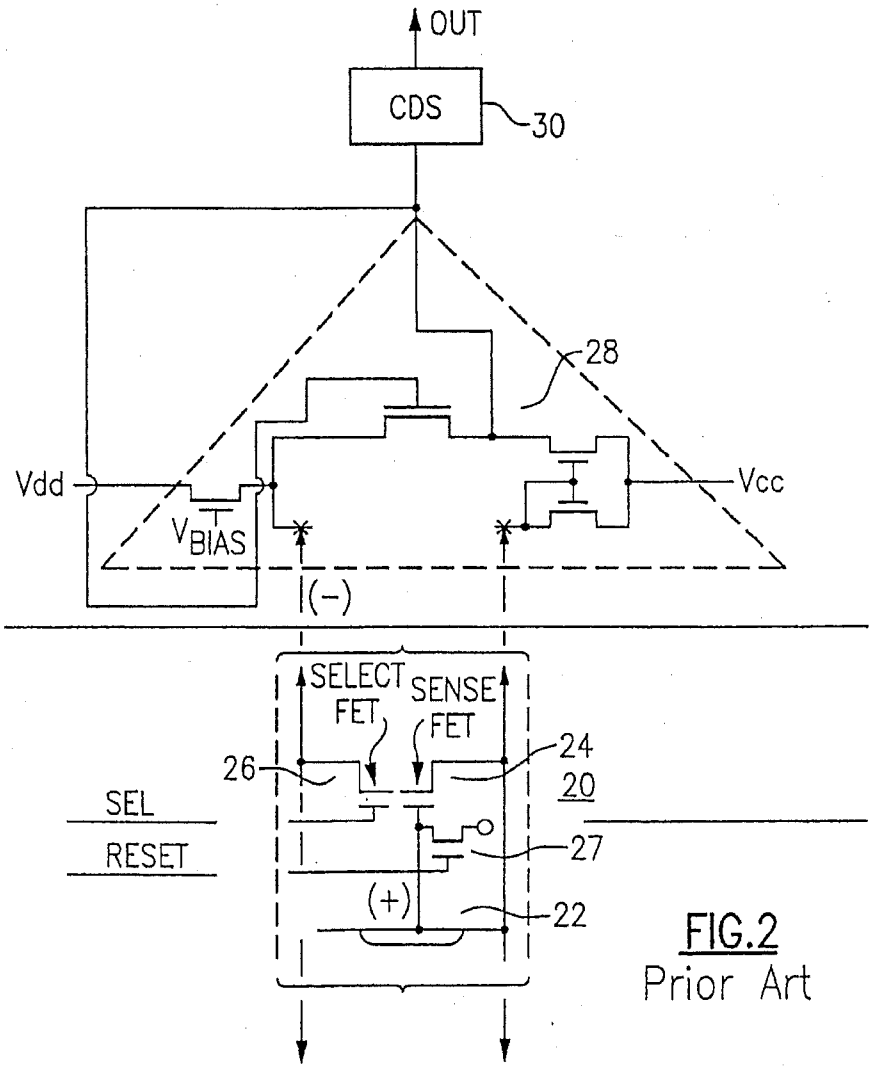


FIG.2
Prior Art

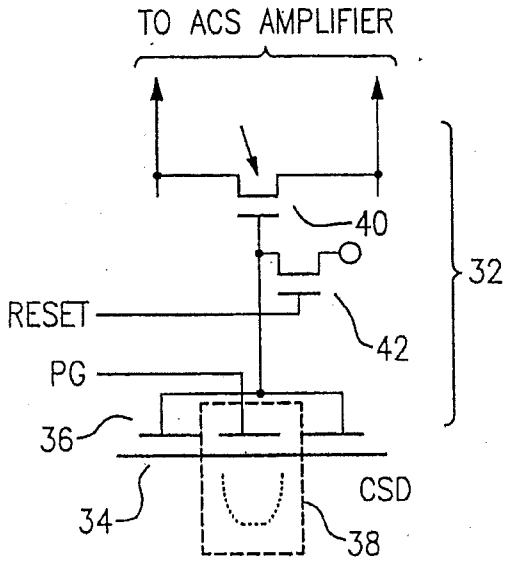


FIG.3
Prior Art

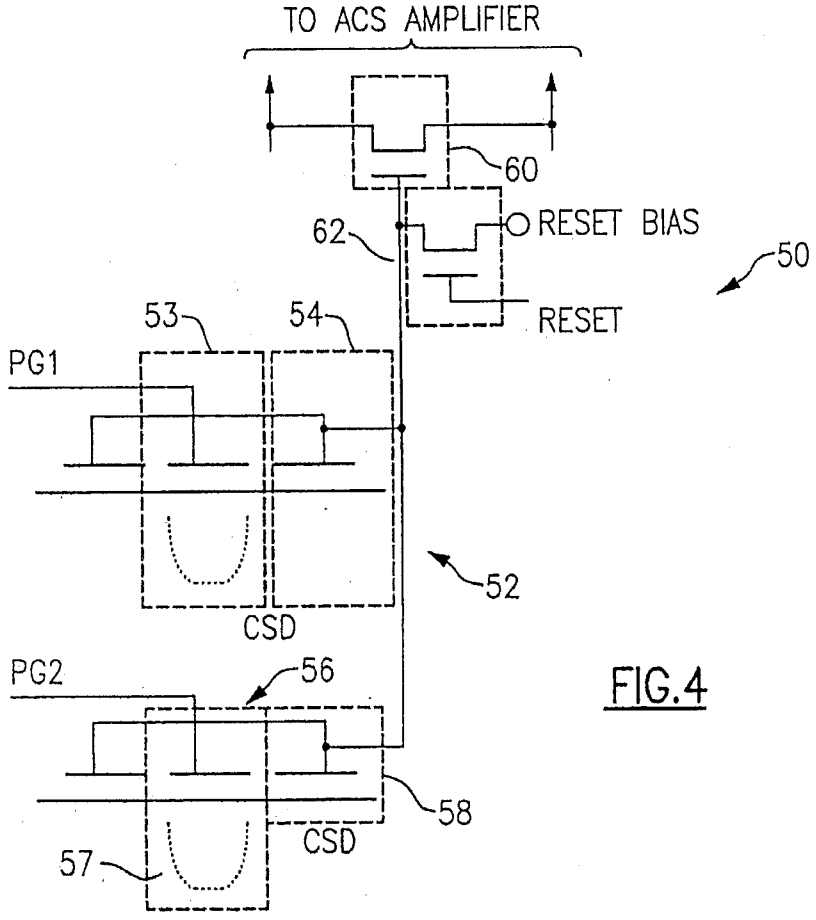


FIG.4

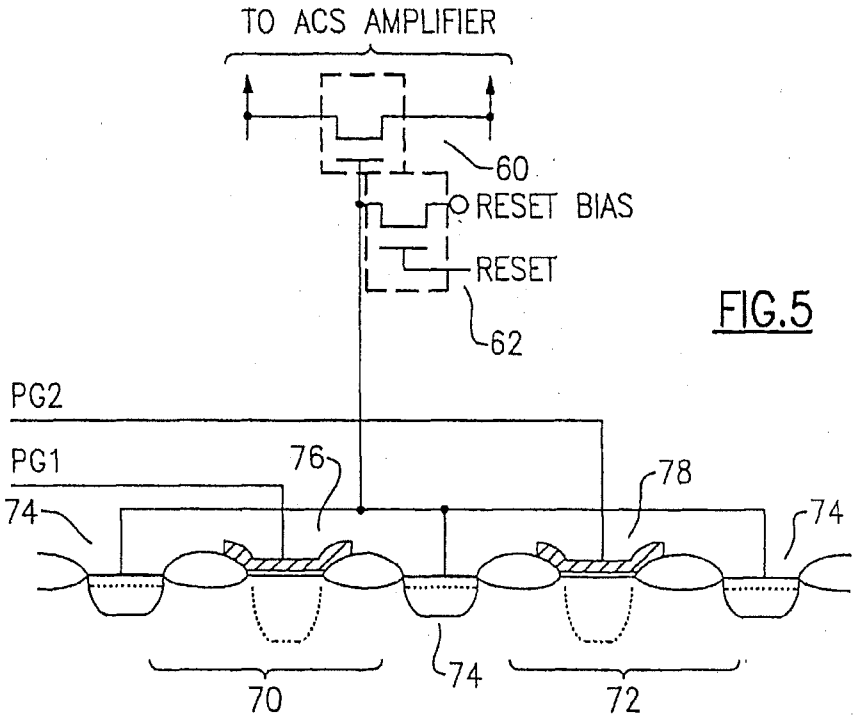

TO ACS AMPLIFIER
60
RESET BIAS
RESET
62
PG2
PG1
76
78
74
74
74
70
72

FIG.5

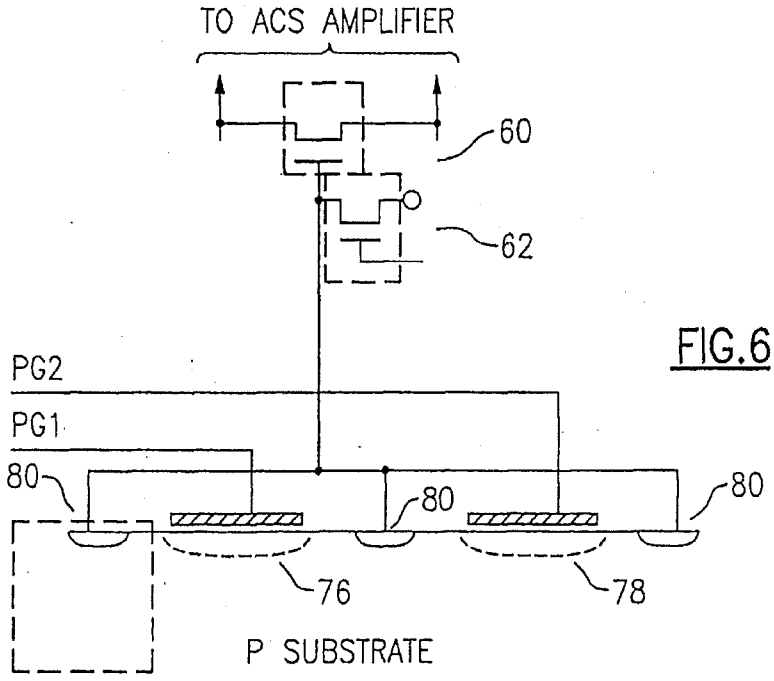

TO ACS AMPLIFIER
60
62
PG2
PG1
80
80
80
76
78
P SUBSTRATE

FIG.6

FIG.7A

FIG.7B

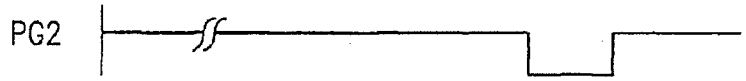


FIG.7C

FIG.7D

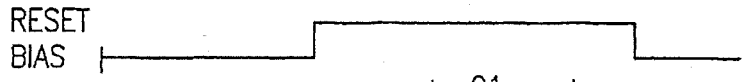


FIG.7E

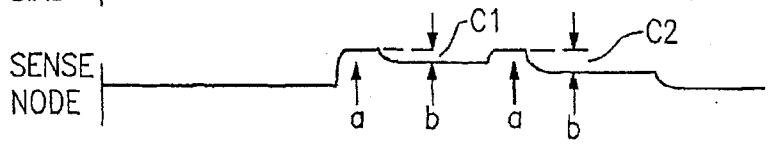
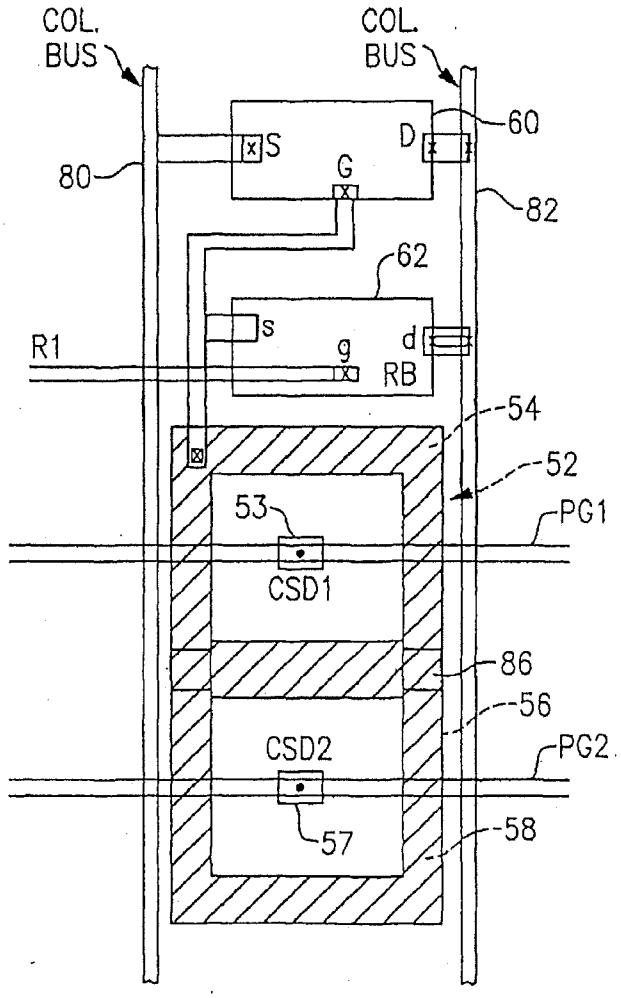


FIG.8



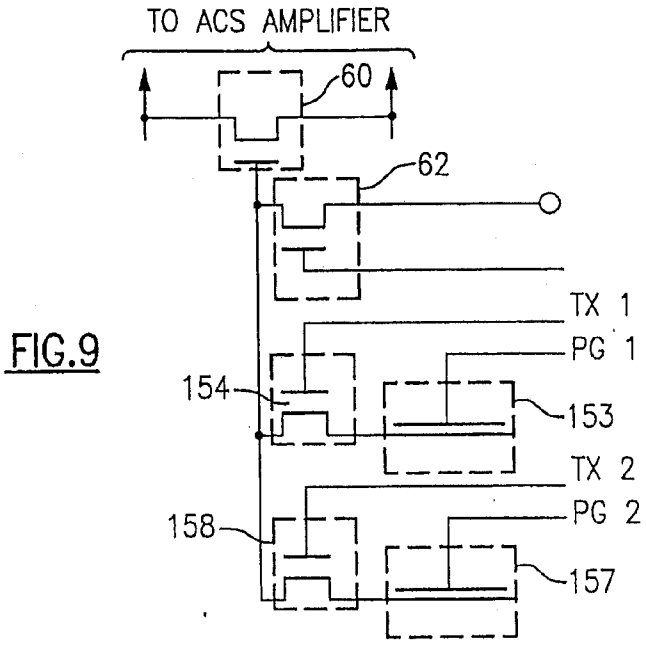

TO ACS AMPLIFIER
60
62
TX 1
PG 1
154
153
TX 2
PG 2
158
157

FIG.9

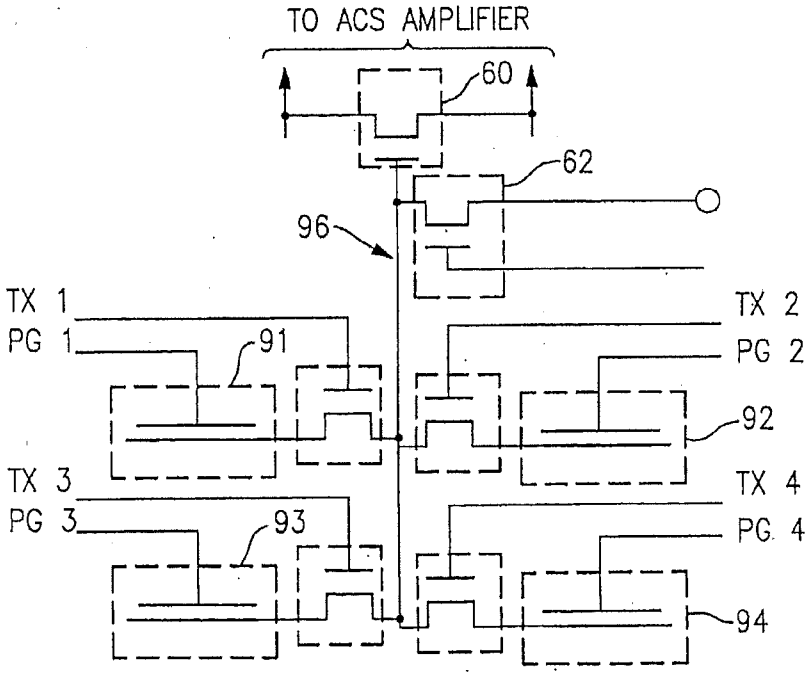

TO ACS AMPLIFIER
60
62
96
TX 1
PG 1
91
TX 2
PG 2
92
TX 3
PG 3
93
TX 4
PG 4
94

FIG.10

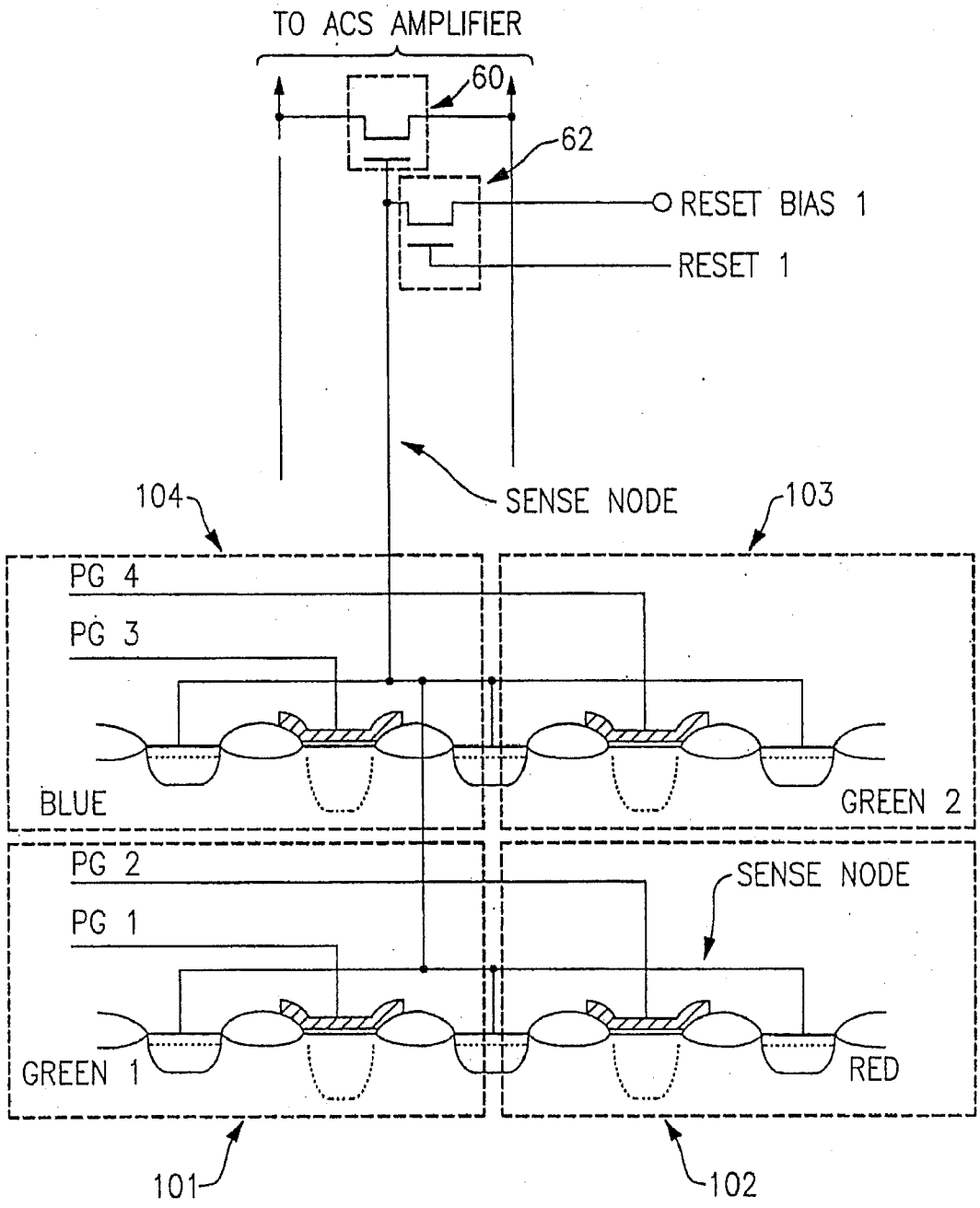

TO ACS AMPLIFIER
60
62
RESET BIAS 1
RESET 1
SENSE NODE
104
103
PG 4
PG 3
BLUE
GREEN 2
PG 2
PG 1
SENSE NODE
GREEN 1
RED
101
102

FIG.11

SOLID STATE IMAGER WITH REDUCED NUMBER OF TRANSISTORS PER PIXEL

CONTINUING APPLICATION DATA

This is a continuation in part of earlier patent application Ser. No. 09/768,124 filed Jan 23, 2001 now U.S. Pat. No. 6,633,029, which is a continuation in part of application Ser. No. 09/490,374, filed Jan. 24, 2000, now U.S. Pat. No. 6,590,198, Jul. 8, 2003, issued Jul. 8, 2003 which is a continuation in part of application Ser. No. 09/039,835, filed Mar. 16, 1998, now U.S. Pat. No. 6,084,229, Jul. 4, 2000 issued Jul. 4, 2000.

BACKGROUND OF THE INVENTION

This invention concerns solid state imagers, and in particular is directed to an improved configuration of the pixels within a given column of a solid state imager. The invention is more particularly concerned with a pixel configuration that reduces the number of FETs associated with each given pixel so as to maximize the area available for collection of light.

Solid state image sensors are used in a wide variety of applications, and there has been much interest in pursuing low-cost, high-resolution, high-reliability image sensors for such applications. CMOS technology is well suited for imagers that are intended for portable applications, because of their need for a only a single power supply voltage, their ruggedness, and their inherent low power consumption. There has been great interest in achieving extremely high resolution also, which requires increased pixel density.

In imaging systems, there is a great desire for each pixel to have low noise, a high fill factor, and the smallest possible number of transistors per pixel, while maintaining quality and maximizing yield, i.e., imager chips per wafer. Pixels having only one transistor per pixel have been available only in passive imager designs, which have an inherent high noise threshold. Passive pixel designs are pixels that do not buffer the photon-generated charge during read out, with the result that there is either high noise, such as with photodiodes and charge-injection devices (CIDs) or else the information is destroyed during read out, as in charge-coupled devices (CCDs). The single FET per pixel is thus used only for addressing during reading, and not for buffering.

Imager designs that employ pixels that buffer their signal prior to read out are known, such as active pixel sensors (APSs) and active column sensors (ACSs). These designs typically have three FETs per pixel, and achieve a much lower thermal noise than seen in passive pixel designs. However, because much of the available surface area of each pixel is occupied by these transistors, and by various power and control wires that have to cross the pixels, there is less area available for the active photosensor elements.

The ideal imager will have its pixels designed to have low noise, a high fill factor, require few or no transistors, a 100% manufacturing yield, and close to zero unit cost.

Active pixel sensors, or APS sensors suffer from fixed-pattern noise or FPN and typically require three or more transistors per pixel. Numerous APS designs have added many extra FETs to overcome FPN, with some designs having as many as thirty-seven FETs per pixel (S. Kleinfleder, S. Lim, X. Liw and A. El Gamal, "A 10000 Frames/S CMOS Digital Pixel Sensor," IEEE Journal of Solid State Circuits, Vol. 36, No. 12, December 2001). However, adding more transistors to each pixel reduces the fill factor and increases the unit cost for the imager.

ACS imagers enjoy very low fixed pattern noise, but still require at least two FETs, and normally three to four FETs per pixel, and reducing the number of FET's below this requirement will increase manufacturing yield as well as improve fill factor. An active column sensor (ACS) architecture has recently been developed, as disclosed in Pace et al. U.S. Pat. No. 6,084,229, which permits a CMOS image sensor to be constructed as a single-chip video camera with a performance equal to or better than that which may be achieved by CCD or CID imagers.

As mentioned above, APS and ACS sensors have three to four FETs for each pixel. As APS sensors suffer from FPN, many designs have added extra FETs to minimize this source of noise and distortion. Also pixel complexity has increased in many designs in order to provide additional pixel functions, such as shuttering capabilities for exposure control. However, even with only three FETs per pixel, a 1.3 mega-pixel imager will require 3.9 million transistors for the pixel array alone. The three transistor limit how small each pixel can be for a given set of process rules. Once most of the pixel area has been consumed by transistors, there is little room left to collect light, and so the conventional approach is to add micro-lenses to the imager to increase the fill factor optically. While micro-lenses permit smaller pixel size for a given set of process rules, the micro-lenses add cost to the wafer processing, and require yet another process step that can generate defects and reduce wafer yield. Therefore, the micro-lens approach is less attractive than an alternative that would increase the area of each pixel that is available for collecting light. Also, using fewer transistors per pixel would permit a number of design options, such as maintaining the pixel size and avoiding the need for micro-lenses, or increasing the pixel density by making the pixel size smaller and adding micro-lenses, or else following older and lower cost design rules for the same size pixel and also adding micro-lenses.

In order to obtain the lowest cost for a solid-state sensor, where cost is based on size or total area, it has been a goal to produce an imager which achieves the smallest size possible for an equivalent number of pixels. Typically, this would require reducing pixel size or size of the photosensitive areas down to the design limits of the process. This is especially important if the same chip has to devote a significant amount of area for its various output multiplexers and output amplifiers. Ideally, size reduction should be achieved, not by reducing the pixel photosensitive areas, but rather by reducing the area consumed by the other circuitry which is located within the pixels.

By combining the ACS technology of U.S. Pat. No. 6,084,229 and an improved pixel structure of U.S. Pat. No. 6,232,589, that is, a so-called Charge Snare Device or CSD, a pixel can designed that needs only two FETs per pixel. One of the two FETs is a sense FET, or pixel output transistor, that forms a part of the pixel column amplifier, and the other FET is a reset FET, which is needed to reset the sense node at the gate of the sense FET. In the CSD pixel arrangement, two of the usual FETs found in the prior photo-gate design, namely, the transfer FET and the select FET, are eliminated.

In the CSD-based imager of U.S. Pat. No. 6,232,589, the pixels operate without a separate selection gate. First the sense node, i.e., the input to the pixel output amplifier FET, is set to ground by gating the reset FET (which is an N-FET), so that the sense node FET is biased off and therefore isolated from the rest of the shared FETs in the same column. Thereafter, addressing of the sense FET is carried out by resetting the sense node FET from ground to 2.5 volts (for a 3.3 volt process). The photon-generated charge is collected

by the photogate when a bias is applied and the active region of the silicon has been depleted. After the desired integration time, the sense node FET is selected by setting it to 2.5 volts, as just discussed. The collected photon-generated charge is transferred to the sense node when the bias applied to the photogate is removed, e.g., to 0.0 volts. The sense node, which is tied to the gate of the sense FET, physically surrounds the photogate, either completely or nearly so. The sense node connects with the gate of the sense node FET and the drain of the reset FET, as well as the sense gate of the CSD. The collected photon generated charge drifts and diffuses to the sense node. The sense node captures all or nearly all the collected charge at the photogate, as the photon-generated charge is surrounded or "snared." This technique of sensing photon-generated charge has very low noise, as the thermal noise on the sense node can be removed by first sampling the sense node just after reset to measure background that contains such noise, and then remeasuring the sense node after the photon-generated charge has been transferred, and taking the difference between these two measurements as a pixel output. The thermal noise that is generated is correlated and subtracted, that is, the device carries out true correlated double sampling or CDS.

It would be desirable to use the same general concepts to create an imager in which the pixels had only a single FET associated with the photogate thereof, and which had the advantages of low noise and true CDS, but a single-FET design has eluded those working in this art.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a solid-state imager that avoids the drawbacks of the prior art.

It is another object to provide an imager that increases the amount of each pixel that is occupied by its photosensitive portion, without encountering other problems, such as fixed pattern noise.

It is another object to simplify the pixel structure of the solid state imager.

Likewise, it is an object to provide a solid-state imager that achieves a reduction in the number of FETs required, i.e., requiring on average a single FET per pixel.

In accordance with one aspect of the present invention, a solid-state area or linear imager is made as an array of pixel elements extending in columns and rows. The objective of reducing the number of FET's per pixel is achieved by sharing the reset and sense node FETs between two or more photo sensitive regions, i.e., between two or more pixels. This is possible because the sense node is idle for the overwhelming majority of the time, during which frame integration takes place, and the sense node is only actuated for a very brief interval just after a given row is reset for selection and reading of the pixel information. The pixel (e.g., charge snare device) that has a gate signal applied to it is the pixel that has its photon-generated charge transferred to the sense node. The sense node can be a photogate as discussed, or may alternatively be a reverse-biased diode, as the signal timing is the same for either.

According to any of a number of embodiments of the invention, the photosensitive array is comprised of a plurality of pixels arranged in columns and rows, wherein the pixels are configured into groups of at least a first pixel and a second pixel. There may be two or more than two pixels in the group sharing the FETs. A shared pixel output transistor, i.e., the sense FET, has a sense electrode and an output electrode, and a shared reset transistor has a gate coupled to receive a reset signal and an output, i.e., drain, coupled to the sense electrode of the associated shared pixel output transistor. Each of the first and second pixels has a photosensitive element with an output electrode coupled to the sense electrode of the shared pixel output transistor, and a gating electrode coupled to receive a respective first and second pixel gating signal.

The pixels of the group that share a common FETs can be in successive rows in the same column, or can be in adjacent columns in the same row. The group of pixels can comprise four pixels sharing a single output FET, or four pixels with two sharing one output FET and one reset FET and the other two sharing a second output FET and a second reset FET. By controlling the timing of the gate and reset signal, it is possible to "bin" or combine the photon-generated charge from the two pixels. Banning is useful for increasing sensitivity in low-light level environments. The imager can be configured as monochromatic or polychromatic (i.e., color), and the shared FET architecture of this invention can be used to great advantage where a Bayer pattern of color pixels is employed.

The solid-state imager of this advantage has the advantages of fewer FETs and fewer metallized strips or wires to carry signal and power to the pixels. This leaves more pixel area available for light collection, and also results in a significantly lower manufacturing scrap rate, i.e., higher manufacturing yield and reduced manufacturing costs.

The above and many other objects, features, and advantages of this invention will be more fully appreciated from the ensuing description of a preferred and exemplary embodiment, which is to be read in conjunction with the accompanying Drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a schematic diagram of an active pixel sensor configuration of the prior art.

FIG. **2** is a schematic diagram of an active column sensor configuration of the prior art.

FIG. **3** is a schematic diagram of a two-transistor charge snare device (CSD) of the prior art.

FIG. **4** is a schematic diagram of a pair of pixels that share a common ACS amplifier transistor and reset FET, according to one possible embodiment of this invention.

FIG. **5** is a schematic diagram of another embodiment of this invention.

FIG. **6** is a schematic diagram of another embodiment.

FIG. **7**A to FIG. **7**E are timing charts for explaining the operation of the FET per pixel sensors of the embodiments of this invention.

FIG. **8** is a diagram of a pixel layout of an embodiment of this invention.

FIGS. **9** and **10** illustrates further embodiments of the invention, employing transfer gate technology.

FIG. **11** illustrates an embodiment employing transfer gates and color binning.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference now to the Drawing, and initially to FIG. **1** thereof, a CMOS imager **10**, of the type that is known as an Active Pixel Sensor or APS, is shown here with a rather large number of components, including a photogate **12** which is the light sensitive member, with a transfer FET **12***a*, a row select transistor **14**, a reset transistor **16**, a sense FET

18, and various metallized leads including the row select lead SELECT, photogate lead PG, transfer lead TX, reset lead RESET, input drain voltage VDD, and output column bus COL BUS, which is connected to an output load. The APS imagers tend to have at least three and often many more FETs for each pixel, with pixel complexity increasing in many designs due to the addition of other pixel functions such as shuttering capabilities for exposure control. Even with only three FETs per pixel, a 1.3 megapixel imager will have 3.9 million transistors in the pixel array alone. The three transistors are a lower limit of complexity in the APS system, and limit how small a pixel can be for a given set of process rules. Once most of the pixel area has been consumed by the transistors, there is little area left for collecting light. In many cases, microlenses are added to increase the light collection or optical fill factor, by concentrating the light into one portion of each pixel. However, this technique does add to the complexity, and hence cost, of the imager, and adds another step that can generate defects and hence reduce wafer yield. Therefore, it would be preferable, if possible, to employ fewer transistors and increase the photosensitive area of each pixel, or else (using microlenses) to reduce pixel size even further. By reducing the number of transistors per pixel, it would also be possible to reduce processing costs and increase reliability and yield, even if the pixel size is unchanged.

Active Column Sensor technology has been described earlier, e.g., in Pace et al. U.S. Pat. No. 6,084,229, which is incorporated herein by reference. Active Column Sensor (ACS) architecture can be applied to either a linear array or to a two-dimensional array. An illustration of an ACS imager is shown here in FIG. **2**. As explained in U.S. Pat. No. 6,084,229, each pixel has a photodiode **22**, and a pair of FETs in series, that is, a sense FET **24** and a select FET **26** incorporated into it, with the source electrode of the sense FET **24** and the drain electrode of the select FET **26** being connected by means of a pair of vertical conductors to respective inputs of an associated column amplifier circuit **28**. A reset FET **27** has its drain connected with the gate of the sense FET **24**. In the ACS sensor, the column amplifier is configured as a closed-loop unity gain amplifier (UGA), thereby ensuring gain and offset uniformity among all pixels of the respective column. The column amplifier **28** is followed by a correlated double sampling (CDS) circuit **30** that corrects for offset voltages while providing a differential output voltage. The outputs of the various column amplifiers are supplied to respective inputs of a multiplexer circuit (not shown) that combines the output levels of the pixels of each selected row, in turn, and this combined output is then fed through a video output amplifier to provide an output video signal. SELECT and RESET signals and Reset Bias are supplied to each row of pixels, in turn, so that the pixel FETs of the selected row connect to the column amplifier **28**. This technology has the useful advantages over the prior APS technology of a smaller FET count per pixel, and a capability of cancelling out fixed pattern noise.

FIG. **3** illustrates the general construction of an imager **32** in the form of a charge snare device as described in Pace et al. U.S. Pat. No. 6,232,589, which is also incorporated herein by reference. In the CSD imager **32** each pixel **34** has a two-FET construction in addition to a sense gate **36**. Here a photogate **38** is supplied with a photogate signal PG, and a sense node of the sense gate **36** is coupled to the gate of a sense FET **40**. A reset FET **42** has a drain connected to a supply of Reset Bias, a source connected to the sense node, and a gate connected to receive a reset signal RESET. The source and drain electrodes of the sense FET **40** are connected to a column amplifier in the manner as shown in FIG. **2**. The CSD architecture results in a two-FET pixel, as a separate selection gate can be avoided. The reset FET **44** is needed to restore the sense node and the gate level of the FET **42**. The transfer FET and the row select FET are eliminated.

The operation of the CSD imager is straightforward. The sense node is set to ground (reset bias) by actuating the reset FET **42** (in this example, the reset FET **42** is an N-FET). Then the sense node is biased off, and is therefore isolated from the rest of the shared FETs in the column. Thus, addressing of the sense FET **40** in this example is carried out by resetting the sense node from ground to 2.5 volts (for a 3.3 volt process). The photon-generated charge is collected by the photogate **38** when a bias is applied and the active region of the silicon (shown in dash lines) has been depleted. After the desired integration time, the sense node is selected by resetting it to 2.5 volts via the reset FET **42**. The collected photon-generated charge is transferred to the sense node, i.e., to the gate of the sense FET **40**, when the reset transistor is gated off and the bias applied to the photogate **38** is removed. As explained in the U.S. Pat. No. 6,232,589, the sense gate **36** of the pixel image area at least substantially surrounds the photogate **38**, and preferably completely surrounds the photogate **38**. In this architecture, the sense node is comprised of the sense gate **36**, the gate electrode of the sense FET **40** and the drain of the Reset FET **42**. The collected photon-generated charge drifts and diffuses to the sense node, which captures all or nearly all the collected charge of the photogate **38**, such that the photon-generated charge of the photogate is surrounded or "snared." This technique of sensing the photon-generated charge has very low noise, as the thermal noise or KTC noise on the sense node can be removed by first sampling the sense node just after reset (to measure the background that contains KTC noise) and then re-measuring the sense node level after the photon-generated charge has been transferred to it, and employing the difference of the two levels as an output. The KTC noise that is present is correlated and is subtracted out for true Correlated Double Sampling or CDS.

An arrangement that reduces the number of FETs per pixel is shown in FIG. **4**, in which the sense or output FET and the Reset FET are shared between two (or more) pixels of a column, or in the same row in adjacent columns. Here, a pair **50** of pixels includes a first pixel device **52** formed as a charge snare device with a photogate **53** and a sense gate **54**, and a second pixel device **56** also with a photogate **57** and a sense gate **58**. The sense gates **54**, **58** form a part of the sense node together with a gate electrode of an output or sense FET **60** that is common to both pixel devices **52** and **56**. A common reset bias FET **62** has its source connected to the sense node, and has drain and gate terminals connected to a supply of reset bias and to a line that supplies a RESET signal, respectively. The photosensitive regions or pixel devices can be composed of either photodiodes of photogates. The sense node is available for sharing between the two pixel devices **52** and **56** because the sense node is idle for the overwhelming majority of the time during frame integration and is only utilized for a small period of time just after a row is reset for selection and reading of the pixel information. Timing for a sense node that is either a reverse biased diode or a photogate is the same. Each pixel device accumulates photon-generated charge and each has its charge transferred to the sense node only at the time that the pixel device is to be read.

A simple form of the embodiments of this invention can be implemented with the two pixel devices of each pair

located in successive rows in the same column. Actually, if the sense node is common between any two pixels in the same column, the operation would be the same. The readout of each pixel occurs by first resetting the sense FET **60** to the reset value, e.g., 2.5 volts, by actuating the reset FET **62**. The readout of the photogate **53** comes by application of a gating signal PG1, and readout of the pixel value is accomplished by removing the bias from the photogate **53**, e.g., going from 2.5 volts down to 0.0 volts, after the desired integration time. To read out the pixel value of the other pixel device **56**, the process is repeated, but using a gating signal PG2 for controlling the photogate **57**. This technique has a benefit of allowing true summation of pixels that are common to the same sense node, that is, a process commonly referred to a "binning." Binning is accomplished by transferring the photon generated charge onto the sense node from both pixel devices **52** and **56** at the same time, after the sense node FET **60** has been reset.

The embodiments such as the one described in connection with FIG. **4** have an architecture of two FETs for each pair of pixel devices, i.e., one FET per pixel, as the two FETs are shared between two pixels.

FIG. **5** illustrates an embodiment in which two pixels in the same row (and in adjacent columns) can share the same pixel amplifier FET **60** and the same reset FET **62**, and share the same sense node. Here, the shared sense node along a common row is associated with a pair of photogate elements **70** and **72**, with nodes controlled by photogate signals PG1 and PG2. The timing of signals is the same as described above in connection with the embodiment of FIG. **4**. Here, there is a common conductive element **74** surrounding each of the photogates **76** and **78** of the respective pixels and defining the sense gate for both pixels. Photogates **76** and **78** for both pixels are isolated from the sense node in this illustration using field oxidation; any processing method of isolation including shallow trench, implants, and physical distance can provide the necessary separation between the sense node and photogates. The photogates herein are of polysilicon construction; but can also be a pinned photodiode, or any optical gate construction including an implanted virtual gate often used in CCDs, including the HyperHAD construction offered by Sory Corporation. This element **74** and the gate of the FET **60** define the sense node. In this embodiment, the element **74** can be formed of an N+ or N− region, with an optional P+ surface implant to minimize surface defects and the resulting dark current, and a metallization can be used for the photogates **76** and **78**. An alternative arrangement is illustrated in FIG. **6**, wherein, in place of the element **74**, a well **80** of N+ or N− material is used. Other elements shown in FIG. **6** can be identical with what is shown in respect to FIG. **5**.

FIGS. **7**A to **7**E show the signal timing sequence for reading out the optical signal from any of the three embodiments described just above. Initially, at the commencement of a readout sequence, the Reset Bias level goes from low to high (FIG. **7**D), and permits sampling of background readout values. For the first of the two pixel elements of the pair, i.e., **52** or **70**, the reset gating pulse RESET (FIG. **7**C) samples the background value (a in FIG. **7**E) by removing bias on the element **54** or **74**, and then the photogate signal PG1 (FIG. **7**A) is applied to photogate **53** or **76**. This transfers the photon-generated charge onto the common sense node, and provides an output level (b in FIG. **7**E). The process is repeated for the second pixel **56** or **72**, except using the second pixel photogate signal PG2 (FIG. **7**B), producing a respective second background value a and readout output level b as shown in FIG. **7**E. The difference values c1 and c2 represent output pixel values that are corrected by means of true correlated double sampling. After readout, a new integration period begins, and other pixels in the array are sampled.

FIG. **8** illustrates, in very general terms, a possible layout for the pixels **52**, **56** of the embodiment of FIG. **4**, with vertical conductors **80** and **82** constituting a column bus, and horizontal conductors formed to include reset R1 and photogate signal conductors PG1 and PG2. The photosensitive areas are surrounded respectively by a pair of closed-geometry conductors as the sense gates **54** and **58**, with one section being common to both sense gates to unify the same. The reset FET **62** and the pixel sense FET **60** are situated here above the two pixels **52** and **56**. The sense gates **54**, **58** completely surround the respective photogates **53**, **57**. In other possible embodiments, the sense gate substantially surround, or encompass a majority of the pixel photosensitive area, so as to capture all or nearly all of the photon-generated charge. A reverse-based diode can be used, composed as an N-type well in a P-type substrate. Other reverse biased diodes can be constructed, depending on the actual CMOS semiconductor process used to fabricate the pixels, so long as the sense nodes completely or nearly completely surround the photogates, so as to maximize charge-transfer efficiency or CTE. Ideally, the CTE should be at 100% or nearly 100%; however, in some applications, a known lower CTE can be employed to extend the dynamic range of the sensor.

In the embodiments in which one amplifier and one reset FET are shared between two columns, the layout would be configured in a similar fashion, but with the two pixels arranged side by side in the same row. The arrangement of the pixel amplifier is described in U.S. Pat. No. 6,084,226 and the layout of the pixels using CSD architecture is described in U.S. Pat. 6,232,589.

Transfer-gate based pixel technology can be used in the pixel arrays according to this invention, and an example is shown here in FIG. **9**. In FIG. **9**, elements that are shared in common with the schematic of the embodiment of FIG. **4** are identified with similar reference numbers. Here, instead of CSD pixel devices, a first pixel is formed of a photogate device **153** and a transfer gate FET **154** connecting the same to a common sense node, with the second pixel also being formed of a photogate device **157** and a transfer gate FET **158**. In this embodiment, additional conductors are provided in each row to bring transfer signals TX1 and TX2 to the transfer gate FETs **154** and **158**. The pixel sense FET **60** and reset FET **62** are shared with both pixels, as in the previous embodiment. The readout sequence is also similar to those of the previous embodiments, providing true correlated double sampling or CSD.

An embodiment of this invention in which the sense FET **60** and the reset FET **62** are shared by a larger number of pixels is illustrated in FIG. **10**. Here, there are four pixels **91**, **92**, **93**, and **94**, in each of two rows in two adjacent columns. The pixels here are formed using transfer gates, as in FIG. **9**. However, other technology, such as CSD technology, could be used. Signal conductors are provided to transfer signals TX1, TX2, TX3, and TX4 and for photogate signals PG1, PG2, PG3, and PG4. The four transfer gates of these pixels all feed into a common sense node **95** that is connected with the gate of the pixel sense FET **60** and the drain of the reset FET **62**. The four pixel arrangement as shown here can facilitate binning by reading out two of the pixels at the same time, or by reading out all four. True additive binning can be used for higher speed data transfer or for increased sensitivity. Binning can be carried out on the

column axis or the row axis, or diagonally. All four photogates can be replaced by photodiodes (not shown) and the elimination of the four PG control signals. The operation of the photodiodes is similar except resetting the photodiodes to begin integration. Biasing of the photodiodes is by resetting the sense node to the desired starting level of the photodiode and allowing the transfer signals to be ON (e.g., VDD) to bias the photodiode accordingly. Integration for photodiodes begins when thee reset FET is turned OFF (e.g., 0.0 Volts) and the corresponding transfer signal (TXn) is also turned OFF. Binning with photodiodes is not possible as the charge in the sense nodes will instead average with photodiode charge.

FIG. **11** illustrates an embodiment of this invention in which shared sense nodes are used for a color sensor. Here there are arranged on one column a first sense FET **60** and second sense FET **160**, with associated reset FETs **62** and **162**. Red, green, and blue filters are used, and the pixels are arranged into a Bayer pattern of Green1/Red/Green2/Blue in a two X two matrix. Here, green pixels **101**, **102**, **103** and **104** share the FETs **60** and **62**. If a given application requires a lower resolution image but a higher frame rate or higher sensitivity, the true additive binning of the same color pixels can be easily carried out. This contrasts with the current technology which simply skips over unwanted pixels when it is desired to minimize the amount of data transferred, and which has an additional disadvantage in terms of reduced sensitivity. In this invention, all pixels can be sampled, keeping sensitivity high. Because binning can be carried out here at the level of the pair (or quad) of pixels, there is less need for processing on the periphery of the video imager or for off-chip processing. If all four pixels are binned together for a monochrome image, that would allow low-light-level image acquisition with only one CDS sample per four pixels binned together. The true CDS and the summation (binning) of four pixels allows for very low noise and high dynamic range. Filters can be applied in the same manner to FIG. **10**, although that is not shown. Also, different filter configurations can be utilized and the shared sense node can be altered to match filter configuration.

The principle of sharing an output FET and a reset FET, to eliminate the select and/or transfer FET among one or more pixels could be applied to active pixel sensor (APS) imagers, utilizing a source follower configuration and photodiode pixels as well. Another advantage of using a shared node among a two-by-two matrix of pixels is the reduction of the number of distributed amplifiers from one per column to one per two columns, as shown in FIG. **11**, with higher reductions possible. With pixel geometries going smaller and smaller it is becoming difficult to place the analog and digital processing circuitry on the same pitch as the pixel. Since the processing circuits are repeated on a column by column basis, if the circuits only have to be repeated every other column, or less frequently, the repeat pitch is doubled for FIG. **11**, and higher multipliers are possible if there are more pixels that share the same sense and reset FETs. Previously, the only alternative to the repeat pitch of the processing circuits was to alternate the column electronics, so that even columns had their electronics at the top of the pixel array, and the odd columns had the electronics brought to the bottom of the array (or vice versa). This would in effect break the imager into different sections, as indicated on U.S. Pat. No. 6,590,198 to Zarnowski et al, and as shown in FIG. **5**. The video is effectively broken into different sections that are either brought out to different ports (or to different pins on the same package) or can be multiplexed back together. By utilizing this previously described method in addition to the technique of this invention, the repeat pitch can be doubled again, further facilitating the imager designer.

While the invention has been described with reference to specific preferred embodiments, the invention is certainly not limited to those precise embodiments. Rather, many modifications and variations will become apparent to persons of skill in the art without departure from the scope and spirit of this invention, as defined in the appended claims.

We claim:

1. A photosensitive array comprised of a plurality of pixels arranged in columns and rows, wherein the pixels are configured into a multiplicity of groups of at least a first pixel and a second pixel, each group including

a shared pixel output transistor having a sense electrode and an output electrode; and

a shared reset transistor having a gate coupled to receive a reset signal and an output coupled to the sense electrode of the associated shared pixel output transistor; and

said first and second pixels each including a photosensitive element having an output electrode, with both said output electrodes being coupled together to the sense electrode of the shared pixel output transistor and a respective gate electrode coupled to receive respective first and second pixel gating signals.

2. A photosensitive array according to claim **1** wherein said first and second pixels of each said group are both disposed in the same column.

3. A photosensitive array according to claim **1** wherein the first and second pixels of each said group are disposed in successive columns in a single row.

4. A photosensitive array according to claim **1** wherein the photosensitive element of each said pixel includes a photogate that captures and accumulates photon generated charge; a sense gate positioned on said photogate; and a sense node that surrounds the photogate.

5. A photosensitive array according to claim **4** wherein the photosensitive elements of said first and second pixels are adjacent one another and the sense nodes thereof share a segment in common with one another.

6. A photosensitive array according to claim **1** wherein each said photosensitive element includes a sense node FET having a gate electrode.

7. A photosensitive array according to claim **1** wherein each said photosensitive element is formed of a charge snare device.

8. A photosensitive array according to claim **1** wherein each said photosensitive element is formed of a photogate and a transfer gate transistor, wherein one electrode of the transfer gate transistor is connected to a photo diode and another electrode thereof is connected to said sense electrode, and a gate of said transfer gate transistor is connected to receive a control signal to operate timing of transfer and reset of said photodiode.

9. A photosensitive array according to claim **1** wherein seach said photosensitive element is formed of a photodiode and a transfer gate transistor.

10. A photosensitive array according to claim **9** wherein one electrode of said transfer gate transistor is connected to a photodiode and another electrode is connected to said sense electrode, and a gate of said transfer gate transistor is connected to receive a control signal to operate timing of transfer and reset of said photodiode.

11. A photosensitive array according to claim **1** further comprising color filters on said first and second photosensitive elements.

12. A photosensitive array according to claim 1 wherein said groups each include a third pixel and a fourth pixel, each of which includes a photosensitive element having an output electrode coupled to the sense electrode of said shared pixel output transistor, and a gate electrode to receive a respective gating signal.

13. A photosensitive array according to claim 12 wherein said groups each include a second reset transistor.

14. A photosensitive array according to claim 1 wherein said groups each include a third and fourth pixel, each of which includes a photosensitive element having an output electrode, and a gate electrode to receive a respective gating signal; a second pixel output transistor having a sense electrode coupled to the output electrodes of the third and fourth pixel photosensitive elements; and a second reset transistor having a gate coupled to receive a second reset signal and an output coupled to the sense electrode of said second pixel output transistor.

15. A photosensitive array according to claim 1 wherein said reset transistor is an FET having a drain thereof connected to the sense electrode of said pixel output transistor.

16. A photosensitive array according to claim 15 wherein said pixel output transistor includes an FET having its gate electrode connected to the drain of the FET of said reset transistor.

17. A photosensitive array according to claim 1 wherein said group includes at least a third pixel with the third pixel also having an output electrode coupled to the sense electrode of the shared pixel output transistor.

18. A photosensitive array according to claim 1, wherein said group includes first, second, third, and fourth pixels, in a 2x2 arrangement, said pixel having associated output electrodes coupled together to the sense electrode of the shared pixel output transistor.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

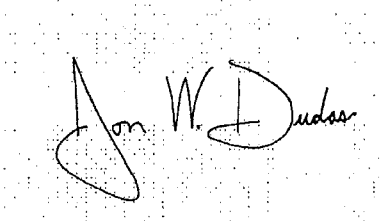
PATENT NO. : 7,057,150 B2
APPLICATION NO. : 10/673591
DATED : June 6, 2006
INVENTOR(S) : Jeffrey Zarnowski et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 12, Claim 18, line 15: "said pixel" should read -- all said pixels --

Signed and Sealed this

Nineteenth Day of September, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

NOTICE OF ASSIGNMENT TO UNITED STATES MAGISTRATE JUDGE FOR DISCOVERY

This case has been assigned to District Judge S. James Otero and the assigned discovery Magistrate Judge is Carolyn Turchin.

The case number on all documents filed with the Court should read as follows:

CV09- 1577 SJO (CTx)

Pursuant to General Order 05-07 of the United States District Court for the Central District of California, the Magistrate Judge has been designated to hear discovery related motions.

All discovery related motions should be noticed on the calendar of the Magistrate Judge

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NOTICE TO COUNSEL

A copy of this notice must be served with the summons and complaint on all defendants (if a removal action is filed, a copy of this notice must be served on all plaintiffs).

Subsequent documents must be filed at the following location:

[X] Western Division
312 N. Spring St., Rm. G-8
Los Angeles, CA 90012

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Santa Ana, CA 92701-4516

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3470 Twelfth St., Rm. 134
Riverside, CA 92501

Failure to file at the proper location will result in your documents being returned to you.

ORIGINAL

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UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

Panavision Imaging, LLC

PLAINTIFF(S)

v.

Omnivision Technologies, Inc.; Canon U.S.A., Inc.; Micron Technology, Inc.; and Aptina Imaging Corporation

DEFENDANT(S).

CASE NUMBER

CV09-1577 SJO (CTx)

SUMMONS

TO: DEFENDANT(S): Omnivision Technologies, Inc.; Canon U.S.A., Inc.; Micron Technology, Inc.; and Aptina Imaging Corporation

A lawsuit has been filed against you.

Within 20 days after service of this summons on you (not counting the day you received it), you must serve on the plaintiff an answer to the attached ☑ complaint ☐ _____ amended complaint ☐ counterclaim ☐ cross-claim or a motion under Rule 12 of the Federal Rules of Civil Procedure. The answer or motion must be served on the plaintiff's attorney, Henry C. Bunsow, Howrey LLP, whose address is 525 Market Street, Suite 3600, San Francisco, California 94105. If you fail to do so, judgment by default will be entered against you for the relief demanded in the complaint. You also must file your answer or motion with the court.

Clerk, U.S. District Court

Dated: 3/6/2009

By: Natalie Gonzalez
Deputy Clerk

(Seal of the Court)

[Use 60 days if the defendant is the United States or a United States agency, or is an officer or employee of the United States. Allowed 60 days by Rule 12(a)(3)].

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

I (a) PLAINTIFFS (Check box if you are representing yourself ☐)

Panavision Imaging, LLC

DEFENDANTS

Omnivision Technologies, Inc.; Canon U.S.A., Inc.; Micron Technology, Inc.; and Aptina Imaging Corporation

(b) Attorneys (Firm Name, Address and Telephone Number. If you are representing yourself, provide same.)

Howrey LLP, 525 Market Street, Suite 3600, San Francisco, California 94105
Telephone: (415) 848-4900

Attorneys (If Known)

Henry C. Bunsow
K.T. Cherian
Scott Wales

II. BASIS OF JURISDICTION (Place an X in one box only.)

☐ 1 U.S. Government Plaintiff
☑ 3 Federal Question (U.S. Government Not a Party)
☐ 2 U.S. Government Defendant
☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES - For Diversity Cases Only
(Place an X in one box for plaintiff and one for defendant.)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business in this State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business in Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. ORIGIN (Place an X in one box only.)

☑ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify): ☐ 6 Multi-District Litigation ☐ 7 Appeal to District Judge from Magistrate Judge

V. REQUESTED IN COMPLAINT: JURY DEMAND: ☑ Yes ☐ No (Check 'Yes' only if demanded in complaint.)

CLASS ACTION under F.R.C.P. 23: ☐ Yes ☑ No ☐ **MONEY DEMANDED IN COMPLAINT: $**

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing and write a brief statement of cause. Do not cite jurisdictional statutes unless diversity.)

35 U.S.C. § 271 - Patent Infringement

VII. NATURE OF SUIT (Place an X in one box only.)

OTHER STATUTES
☐ 400 State Reapportionment
☐ 410 Antitrust
☐ 430 Banks and Banking
☐ 450 Commerce/ICC Rates/etc.
☐ 460 Deportation
☐ 470 Racketeer Influenced and Corrupt Organizations
☐ 480 Consumer Credit
☐ 490 Cable/Sat TV
☐ 810 Selective Service
☐ 850 Securities/Commodities/ Exchange
☐ 875 Customer Challenge 12 USC 3410
☐ 890 Other Statutory Actions
☐ 891 Agricultural Act
☐ 892 Economic Stabilization Act
☐ 893 Environmental Matters
☐ 894 Energy Allocation Act
☐ 895 Freedom of Info. Act
☐ 900 Appeal of Fee Determination Under Equal Access to Justice
☐ 950 Constitutionality of State Statutes

CONTRACT
☐ 110 Insurance
☐ 120 Marine
☐ 130 Miller Act
☐ 140 Negotiable Instrument
☐ 150 Recovery of Overpayment & Enforcement of Judgment
☐ 151 Medicare Act
☐ 152 Recovery of Defaulted Student Loan (Excl. Veterans)
☐ 153 Recovery of Overpayment of Veteran's Benefits
☐ 160 Stockholders' Suits
☐ 190 Other Contract
☐ 195 Contract Product Liability
☐ 196 Franchise

REAL PROPERTY
☐ 210 Land Condemnation
☐ 220 Foreclosure
☐ 230 Rent Lease & Ejectment
☐ 240 Torts to Land
☐ 245 Tort Product Liability
☐ 290 All Other Real Property

TORTS - PERSONAL INJURY
☐ 310 Airplane
☐ 315 Airplane Product Liability
☐ 320 Assault, Libel & Slander
☐ 330 Fed. Employers' Liability
☐ 340 Marine
☐ 345 Marine Product Liability
☐ 350 Motor Vehicle
☐ 355 Motor Vehicle Product Liability
☐ 360 Other Personal Injury
☐ 362 Personal Injury-Med Malpractice
☐ 365 Personal Injury-Product Liability
☐ 368 Asbestos Personal Injury Product Liability

IMMIGRATION
☐ 462 Naturalization Application
☐ 463 Habeas Corpus-Alien Detainee
☐ 465 Other Immigration Actions

TORTS - PERSONAL PROPERTY
☐ 370 Other Fraud
☐ 371 Truth in Lending
☐ 380 Other Personal Property Damage
☐ 385 Property Damage Product Liability

BANKRUPTCY
☐ 422 Appeal 28 USC 158
☐ 423 Withdrawal 28 USC 157

CIVIL RIGHTS
☐ 441 Voting
☐ 442 Employment
☐ 443 Housing/Accommodations
☐ 444 Welfare
☐ 445 American with Disabilities - Employment
☐ 446 American with Disabilities - Other
☐ 440 Other Civil Rights

PRISONER PETITIONS
☐ 510 Motions to Vacate Sentence Habeas Corpus
☐ 530 General
☐ 535 Death Penalty
☐ 540 Mandamus/ Other
☐ 550 Civil Rights
☐ 555 Prison Condition

FORFEITURE / PENALTY
☐ 610 Agriculture
☐ 620 Other Food & Drug
☐ 625 Drug Related Seizure of Property 21 USC 881
☐ 630 Liquor Laws
☐ 640 R.R. & Truck
☐ 650 Airline Regs
☐ 660 Occupational Safety /Health
☐ 690 Other

LABOR
☐ 710 Fair Labor Standards Act
☐ 720 Labor/Mgmt. Relations
☐ 730 Labor/Mgmt. Reporting & Disclosure Act
☐ 740 Railway Labor Act
☐ 790 Other Labor Litigation
☐ 791 Empl. Ret. Inc. Security Act

PROPERTY RIGHTS
☐ 820 Copyrights
☑ 830 Patent
☐ 840 Trademark

SOCIAL SECURITY
☐ 861 HIA (1395ff)
☐ 862 Black Lung (923)
☐ 863 DIWC/DIWW (405(g))
☐ 864 SSID Title XVI
☐ 865 RSI (405(g))

FEDERAL TAX SUITS
☐ 870 Taxes (U.S. Plaintiff or Defendant)
☐ 871 IRS-Third Party 26 USC 7609

CV09-1577

FOR OFFICE USE ONLY: Case Number: _____

AFTER COMPLETING THE FRONT SIDE OF FORM CV-71, COMPLETE THE INFORMATION REQUESTED BELOW.

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

VIII(a). IDENTICAL CASES: Has this action been previously filed in this court and dismissed, remanded or closed? ☑ No ☐ Yes
If yes, list case number(s): _____

VIII(b). RELATED CASES: Have any cases been previously filed in this court that are related to the present case? ☑ No ☐ Yes
If yes, list case number(s): _____

Civil cases are deemed related if a previously filed case and the present case:
(Check all boxes that apply) ☐ A. Arise from the same or closely related transactions, happenings, or events; or
☐ B. Call for determination of the same or substantially related or similar questions of law and fact; or
☐ C. For other reasons would entail substantial duplication of labor if heard by different judges; or
☐ D. Involve the same patent, trademark or copyright, and one of the factors identified above in a, b or c also is present.

IX. VENUE: (When completing the following information, use an additional sheet if necessary.)

(a) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named plaintiff resides.
☐ Check here if the government, its agencies or employees is a named plaintiff. If this box is checked, go to item (b).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Los Angeles County (Panavision Imaging, LLC)	

(b) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named defendant resides.
☐ Check here if the government, its agencies or employees is a named defendant. If this box is checked, go to item (c).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
	Santa Clara County (Omnivision Technologies, Inc. and Aptina Imaging Corporation); New York State (Canon U.S.A., Inc.); and Idaho State (Micron Technology, Inc.)

(c) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** claim arose.
Note: In land condemnation cases, use the location of the tract of land involved.

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Los Angeles, Orange, San Bernardino, Riverside, Ventura, Santa Barbara, and San Luis Obispo Counties	

*** Los Angeles, Orange, San Bernardino, Riverside, Ventura, Santa Barbara, or San Luis Obispo Counties**
Note: In land condemnation cases, use the location of the tract of land involved

X. SIGNATURE OF ATTORNEY (OR PRO PER): _____ **Date** 3/6/09

Notice to Counsel/Parties: The CV-71 (JS-44) Civil Cover Sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law. This form, approved by the Judicial Conference of the United States in September 1974, is required pursuant to Local Rule 3-1 is not filed but is used by the Clerk of the Court for the purpose of statistics, venue and initiating the civil docket sheet. (For more detailed instructions, see separate instructions sheet.)

Key to Statistical codes relating to Social Security Cases:

Nature of Suit Code	Abbreviation	Substantive Statement of Cause of Action
861	HIA	All claims for health insurance benefits (Medicare) under Title 18, Part A, of the Social Security Act, as amended. Also, include claims by hospitals, skilled nursing facilities, etc., for certification as providers of services under the program. (42 U.S.C. 1935FF(b))
862	BL	All claims for "Black Lung" benefits under Title 4, Part B, of the Federal Coal Mine Health and Safety Act of 1969. (30 U.S.C. 923)
863	DIWC	All claims filed by insured workers for disability insurance benefits under Title 2 of the Social Security Act, as amended; plus all claims filed for child's insurance benefits based on disability. (42 U.S.C. 405(g))
863	DIWW	All claims filed for widows or widowers insurance benefits based on disability under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405(g))
864	SSID	All claims for supplemental security income payments based upon disability filed under Title 16 of the Social Security Act, as amended.
865	RSI	All claims for retirement (old age) and survivors benefits under Title 2 of the Social Security Act, as amended. (42 U.S.C. (g))